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(54) **LIGHT EMITTING DEVICE**

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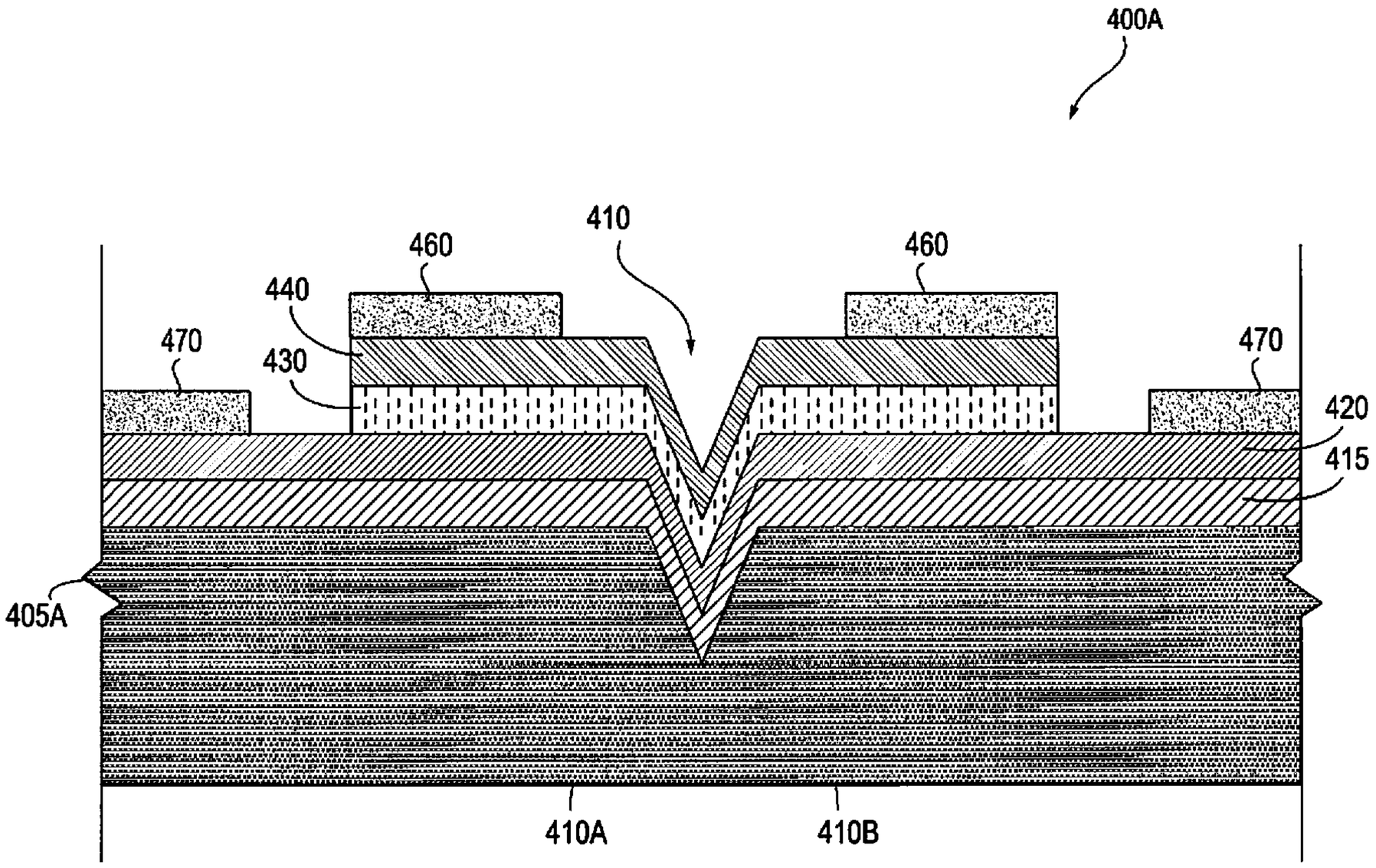
(52) **U.S. Cl.** **257/13**; 257/95; 438/29; 257/E33.003; 257/E33.055; 257/E33.023

(57) **ABSTRACT**

A light emitting device includes a substrate having a first surface and a second surface not parallel to the first surface, and a light emission layer disposed over the second surface to emit light. The light emission layer has a light emission surface which is not parallel to the first surface.



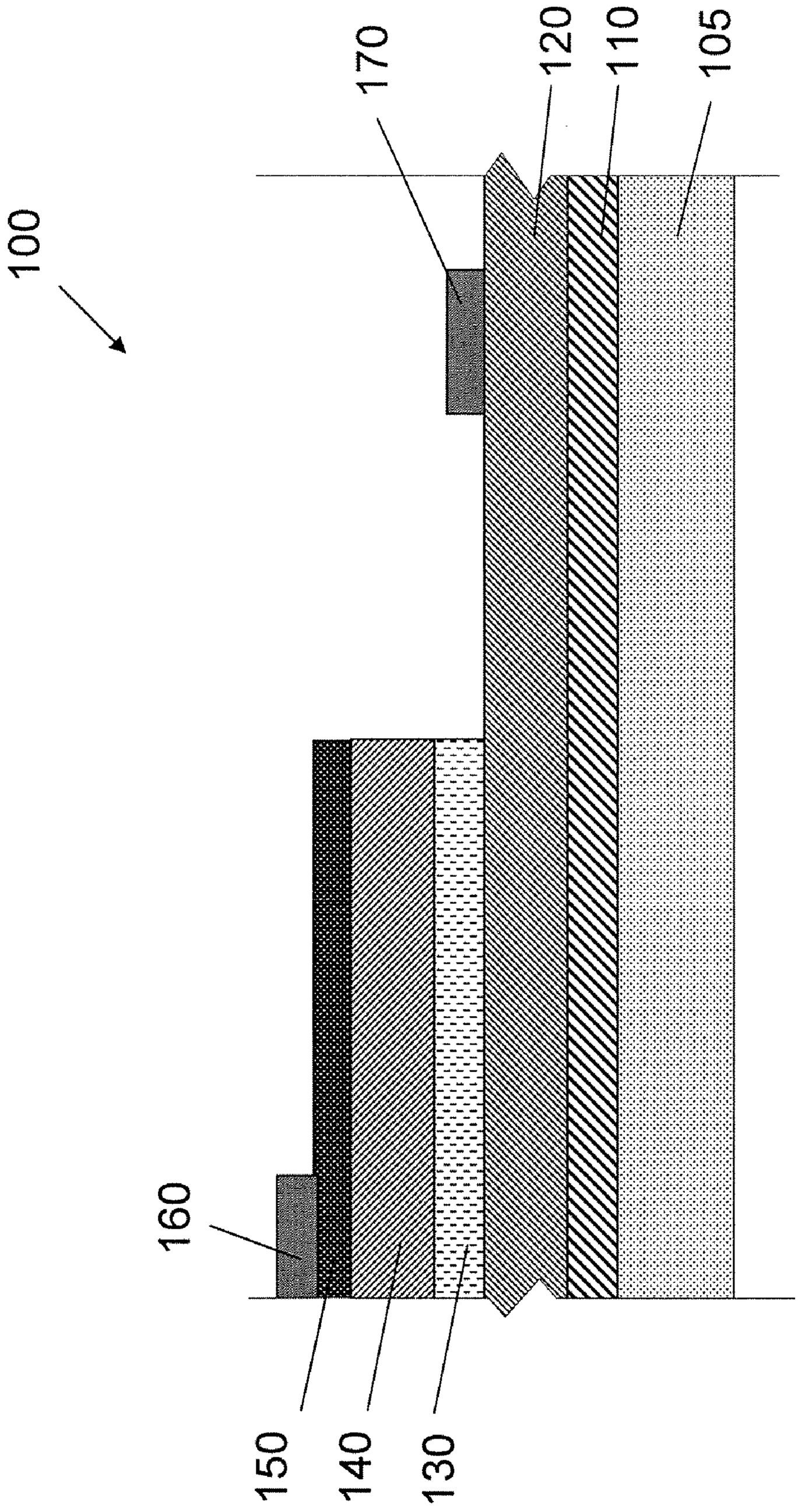


Figure 1 Prior Art

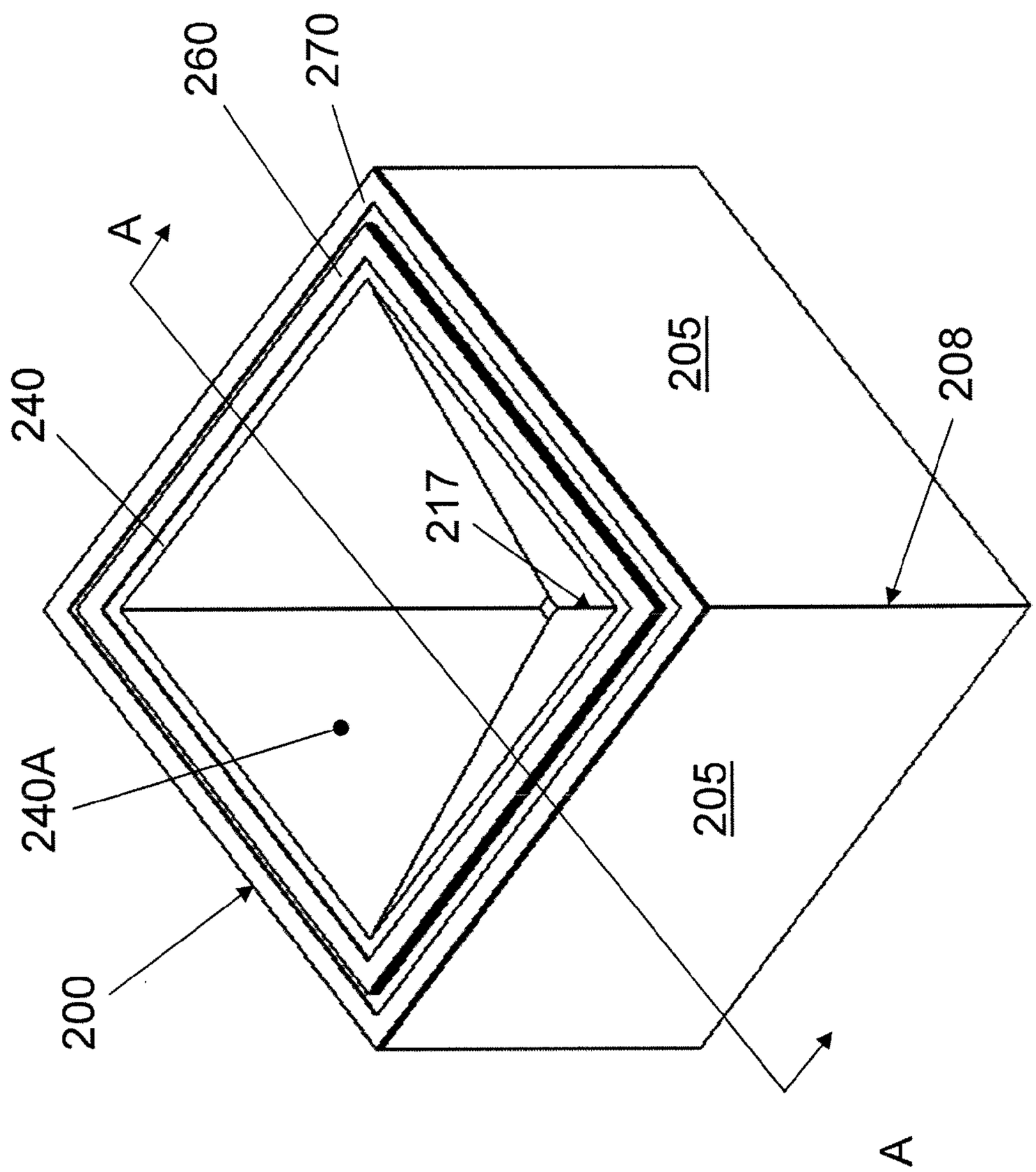


Figure 2A

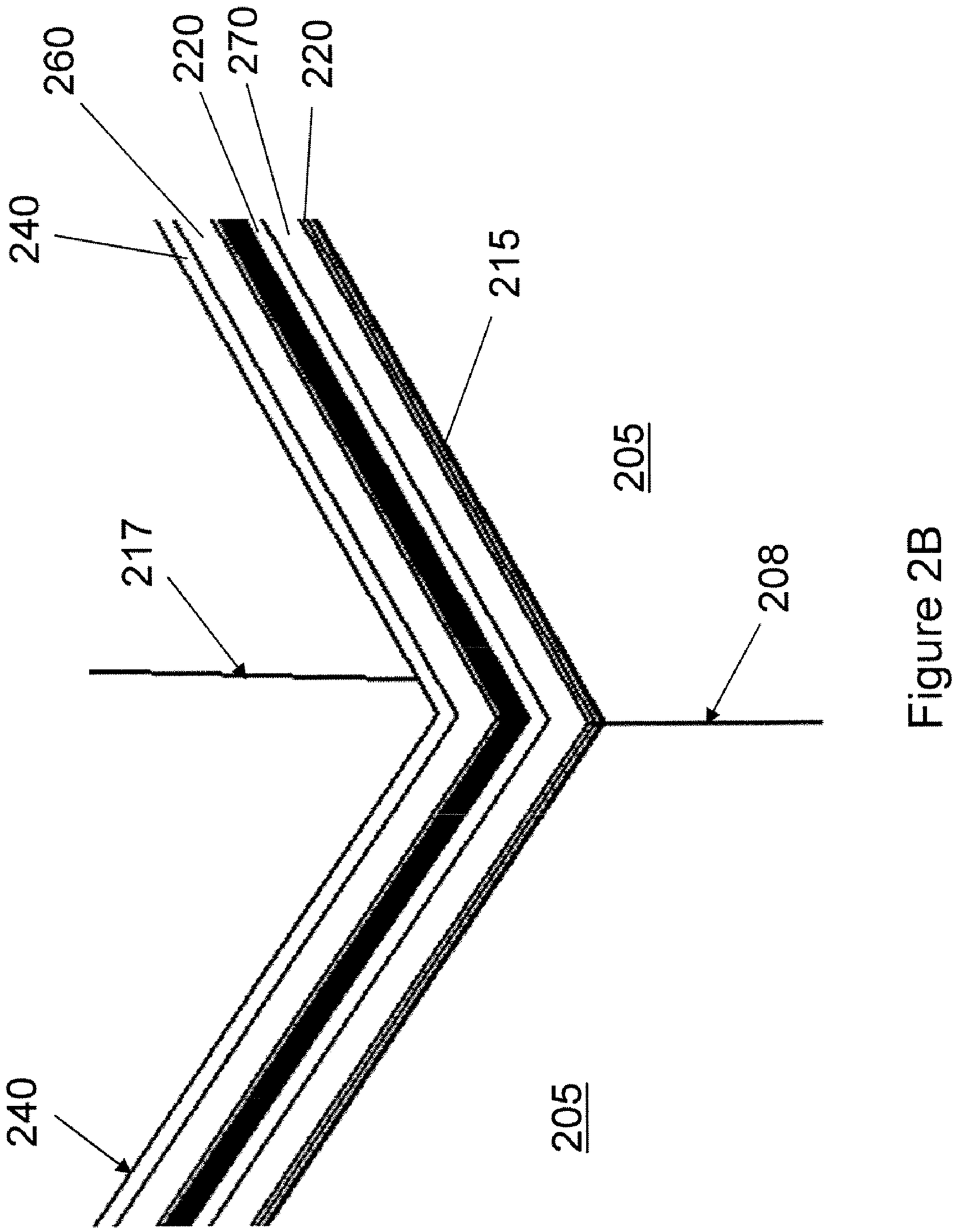


Figure 2B

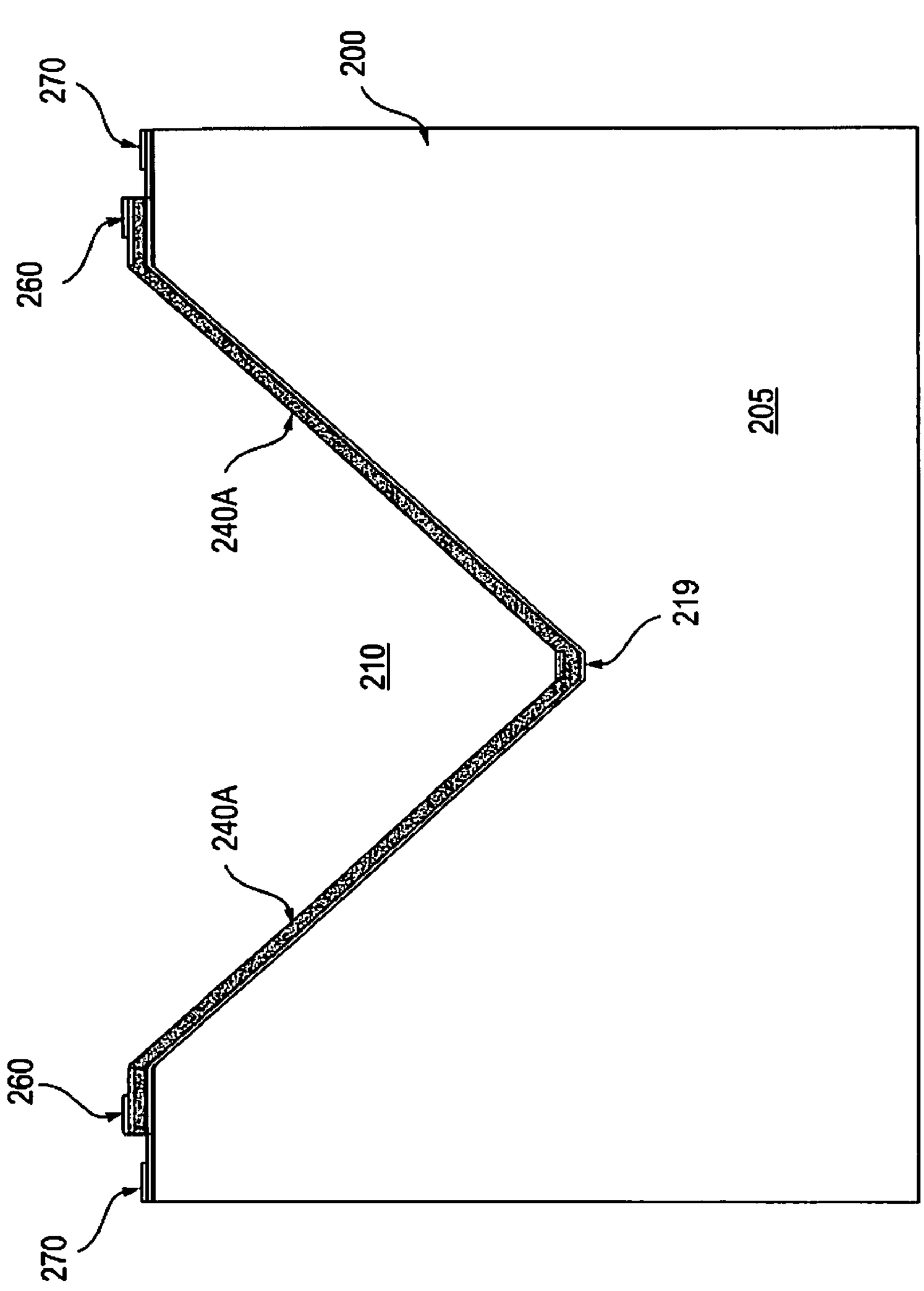


FIG. 3A

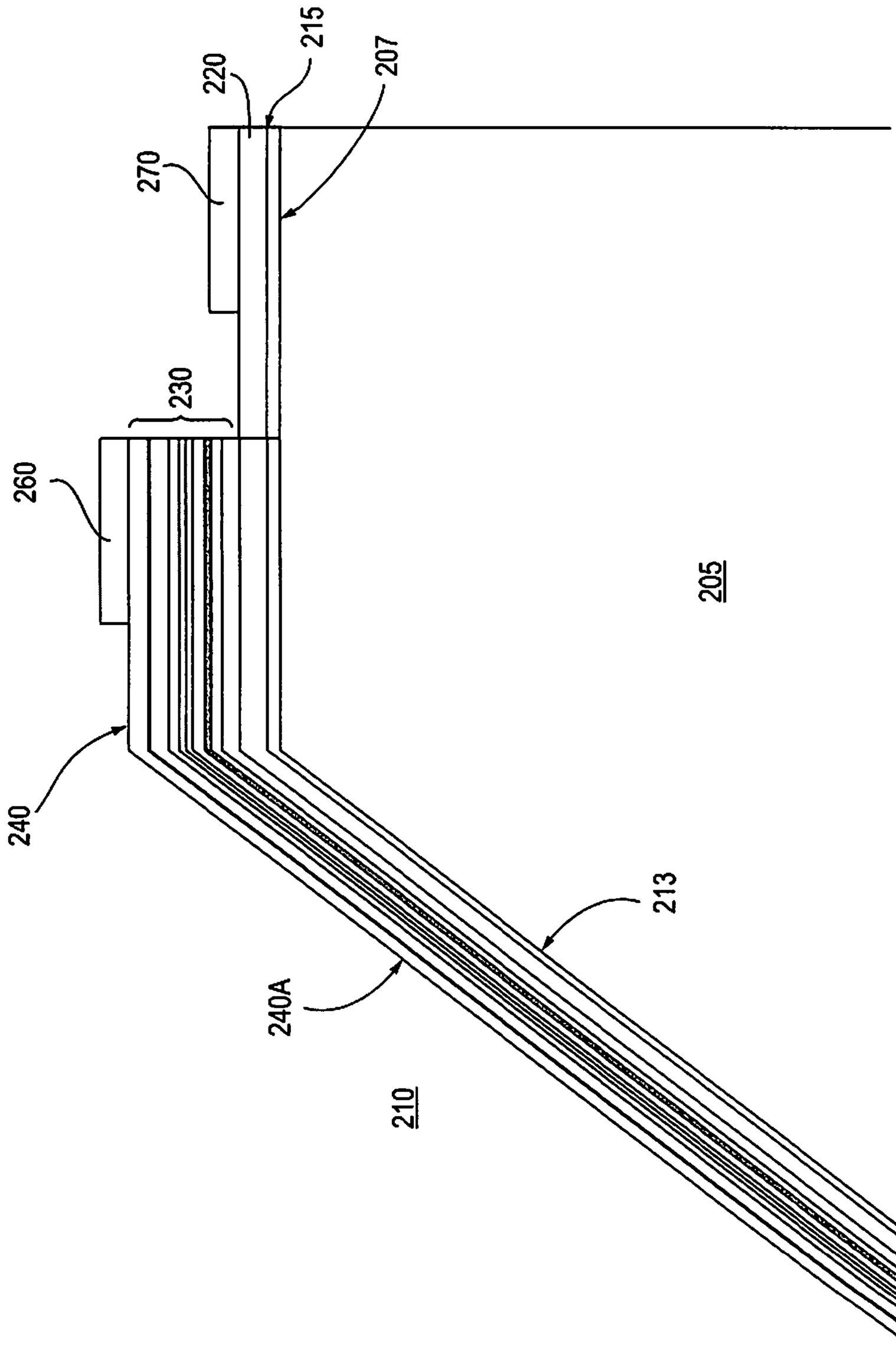


FIG. 3B

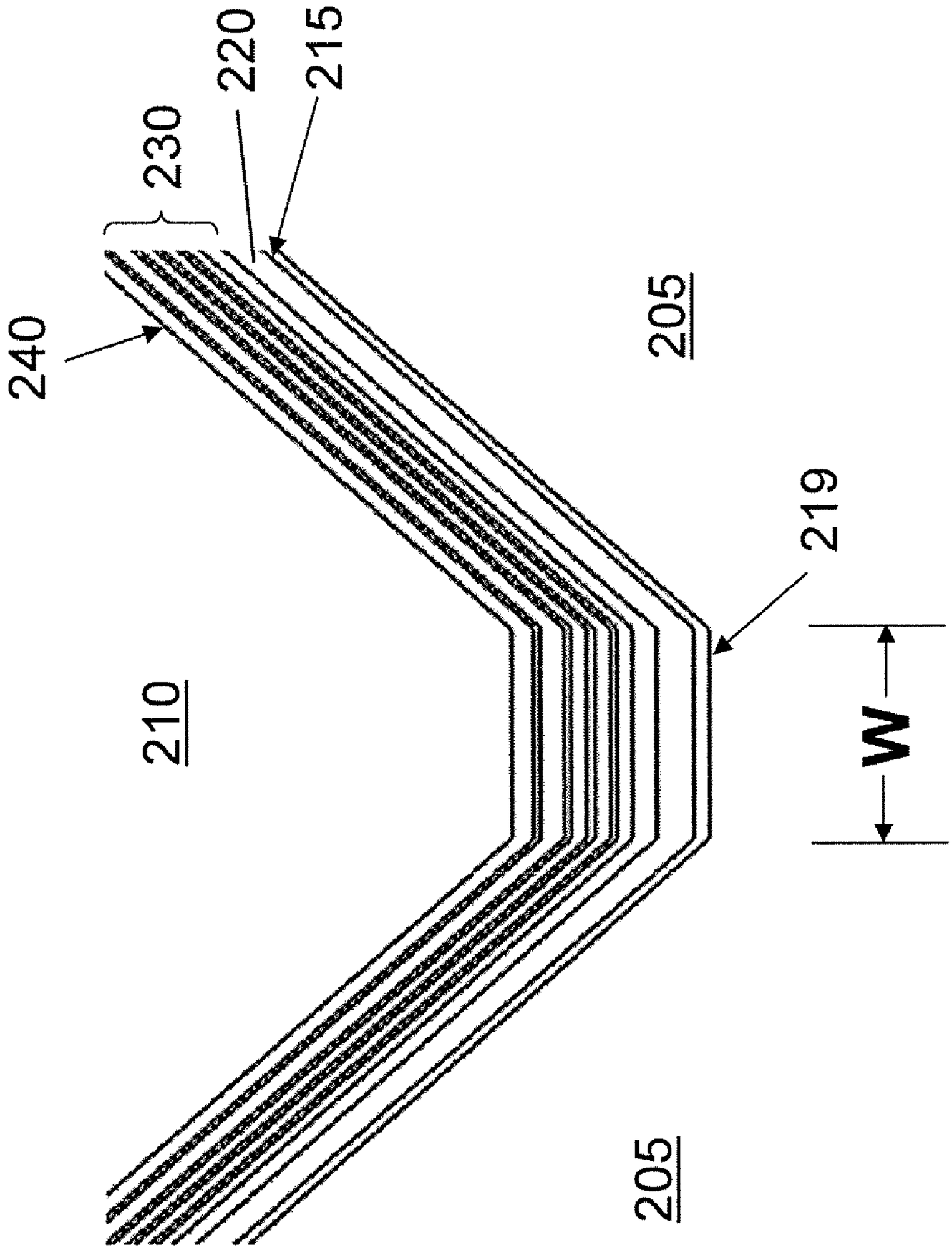


Figure 3C

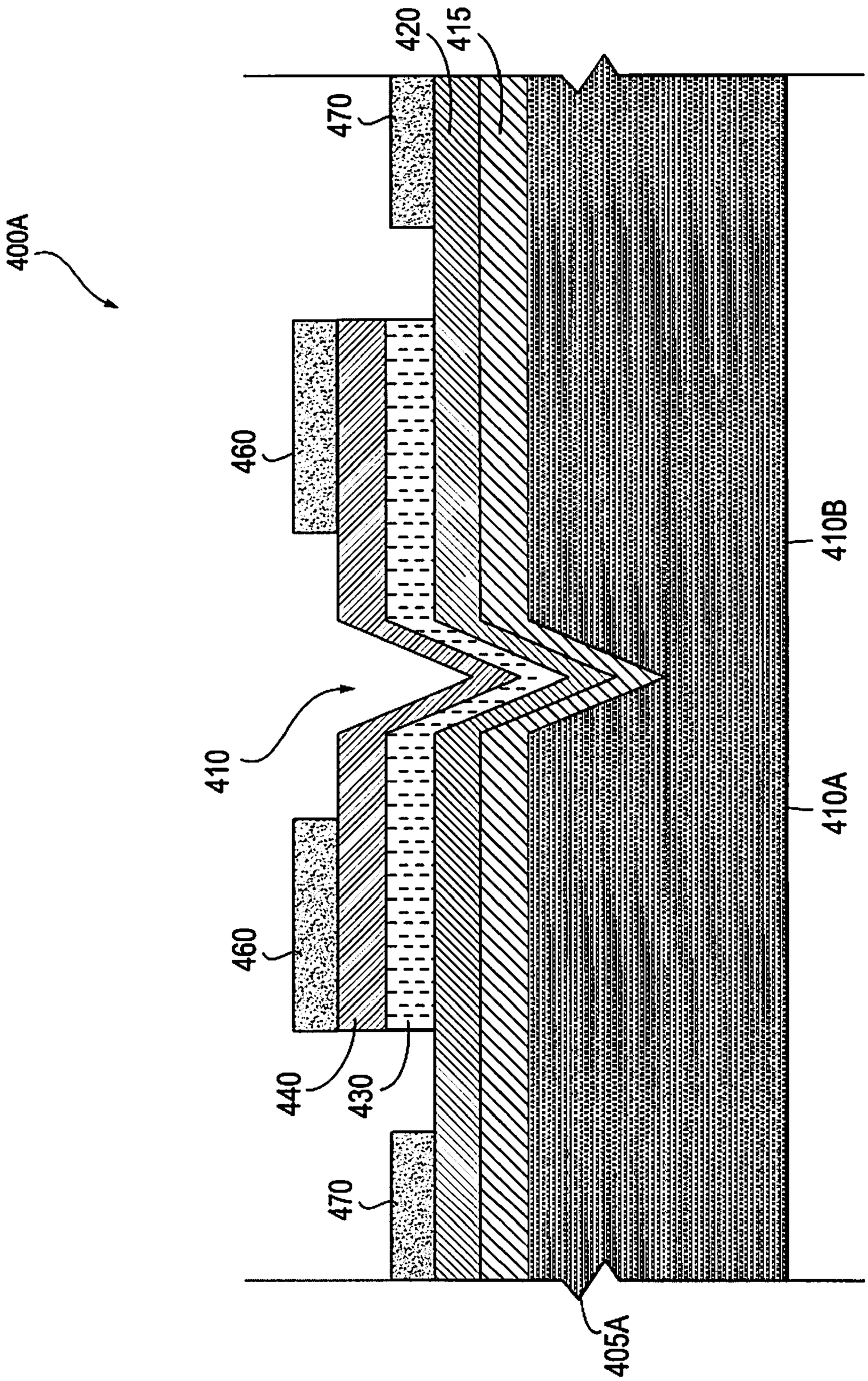


FIG. 3D

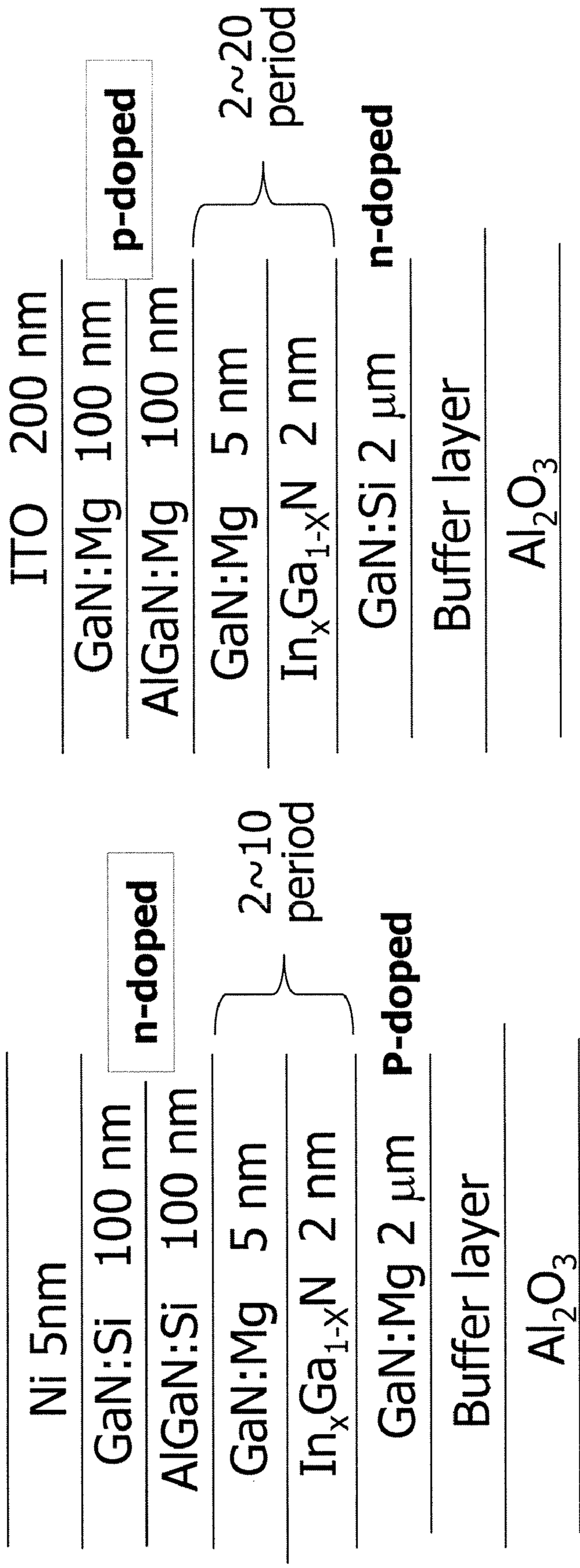

ITO
GaN:Mg 100 nm
p-doped
AlGaN:Mg 100 nm
GaN:Mg 5 nm
2~20 period
$In_xGa_{1-x}N$ 2 nm
GaN:Si 2 µm
n-doped
Buffer layer
Al_2O_3
Au 5nm
Ni 5nm
GaN:Si 100 nm
n-doped
AlGaN:Si 100 nm
GaN:Mg 5 nm
2~10 period
$In_xGa_{1-x}N$ 2 nm
GaN:Mg 2 µm
P-doped
Buffer layer
Al_2O_3

Figure 3E

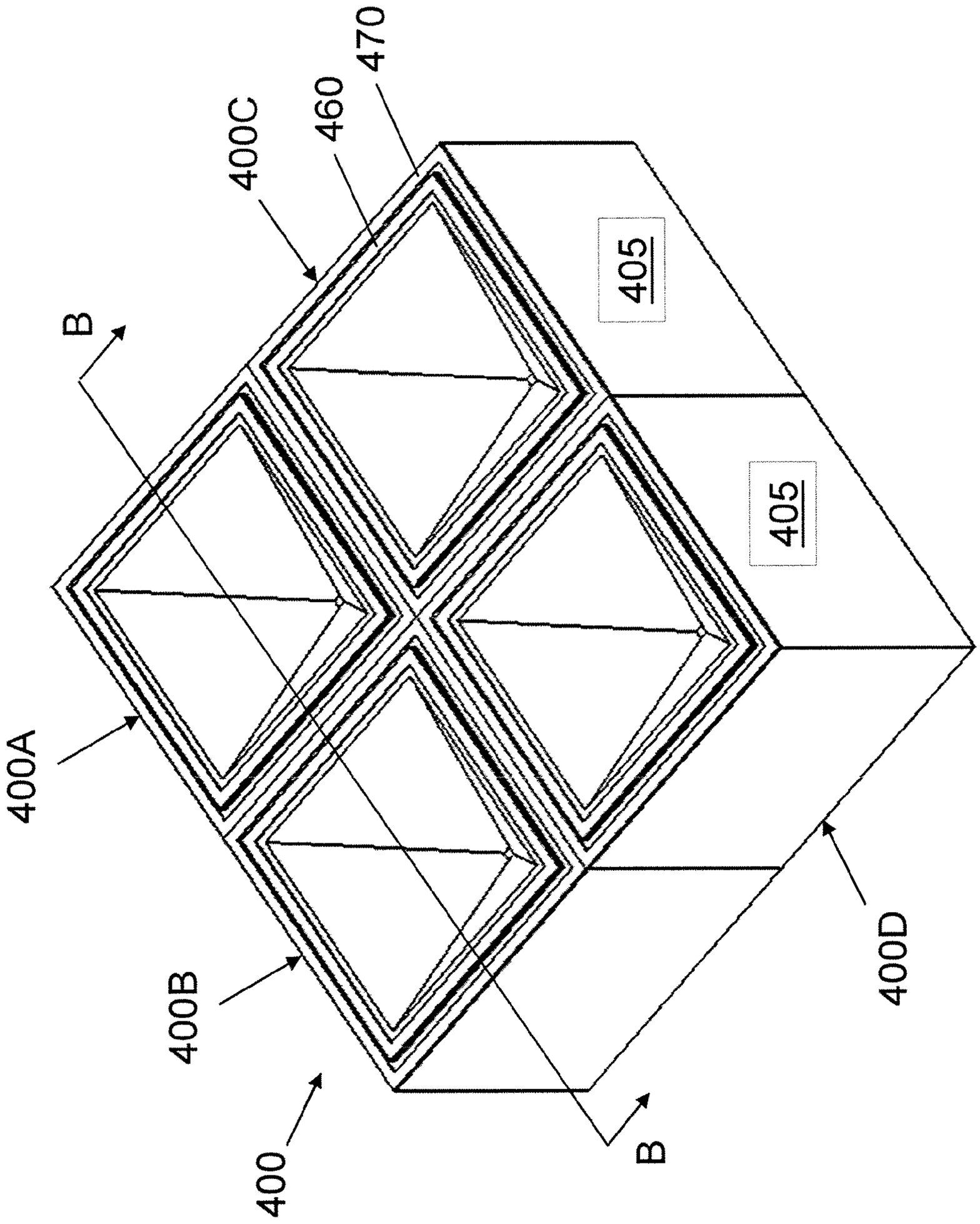


Figure 4A

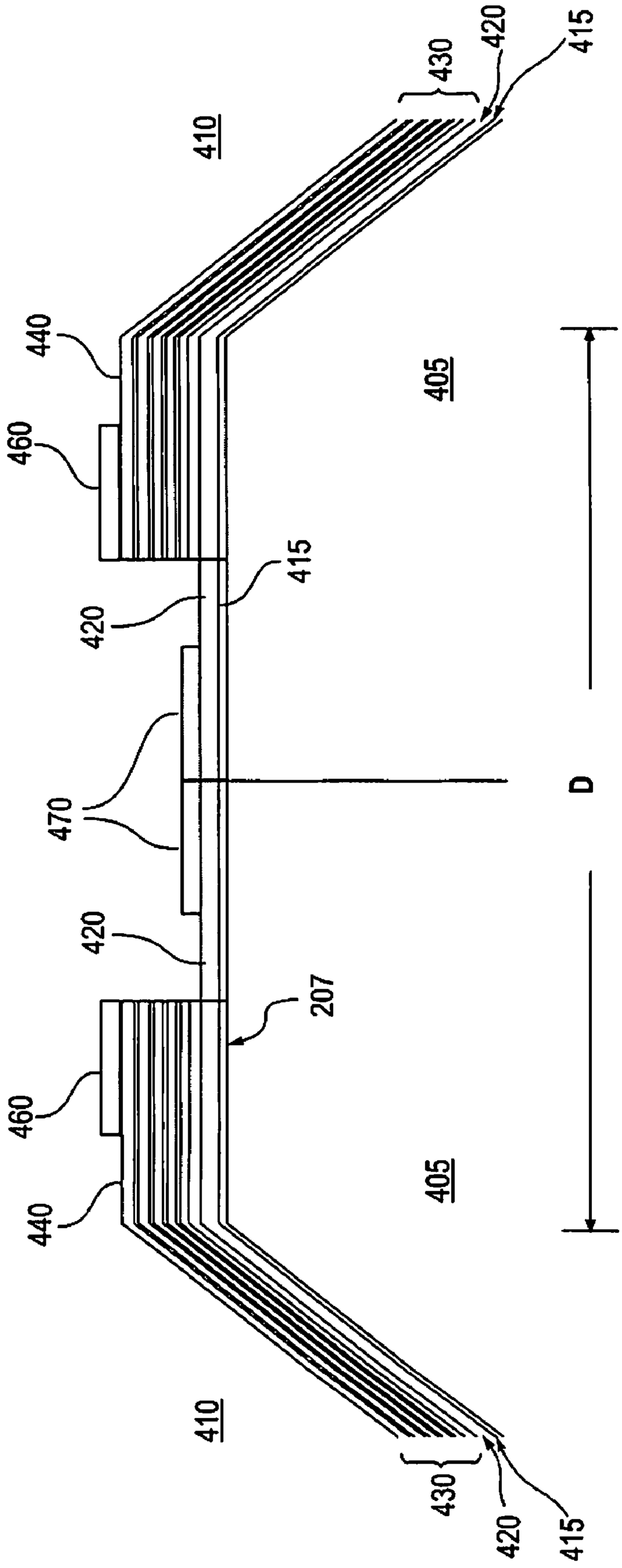

410
430
420
415
440
460
415
420
470
420
207
460
440
405
410
430
420
415
D

FIG. 4B

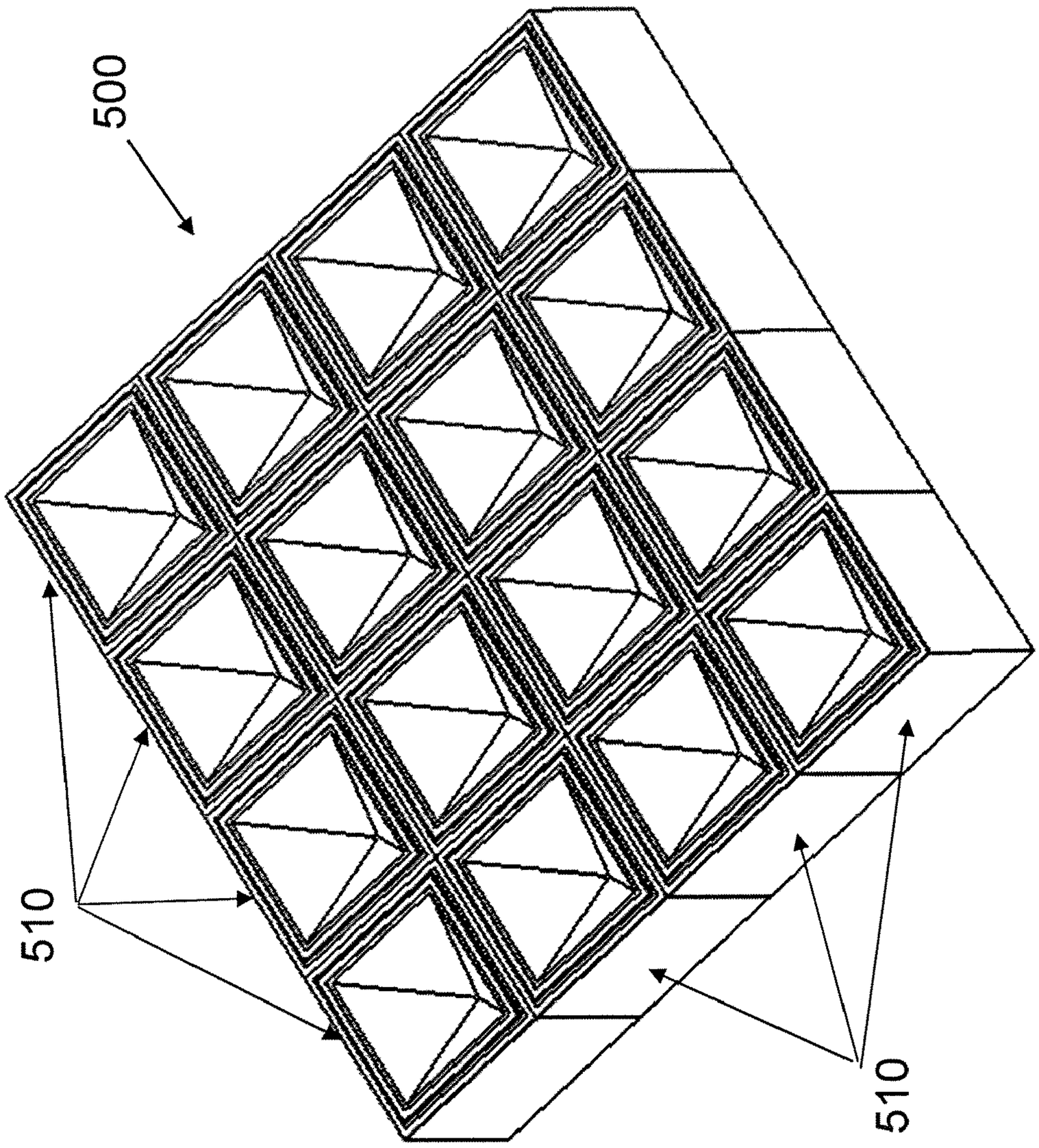


Figure 4C

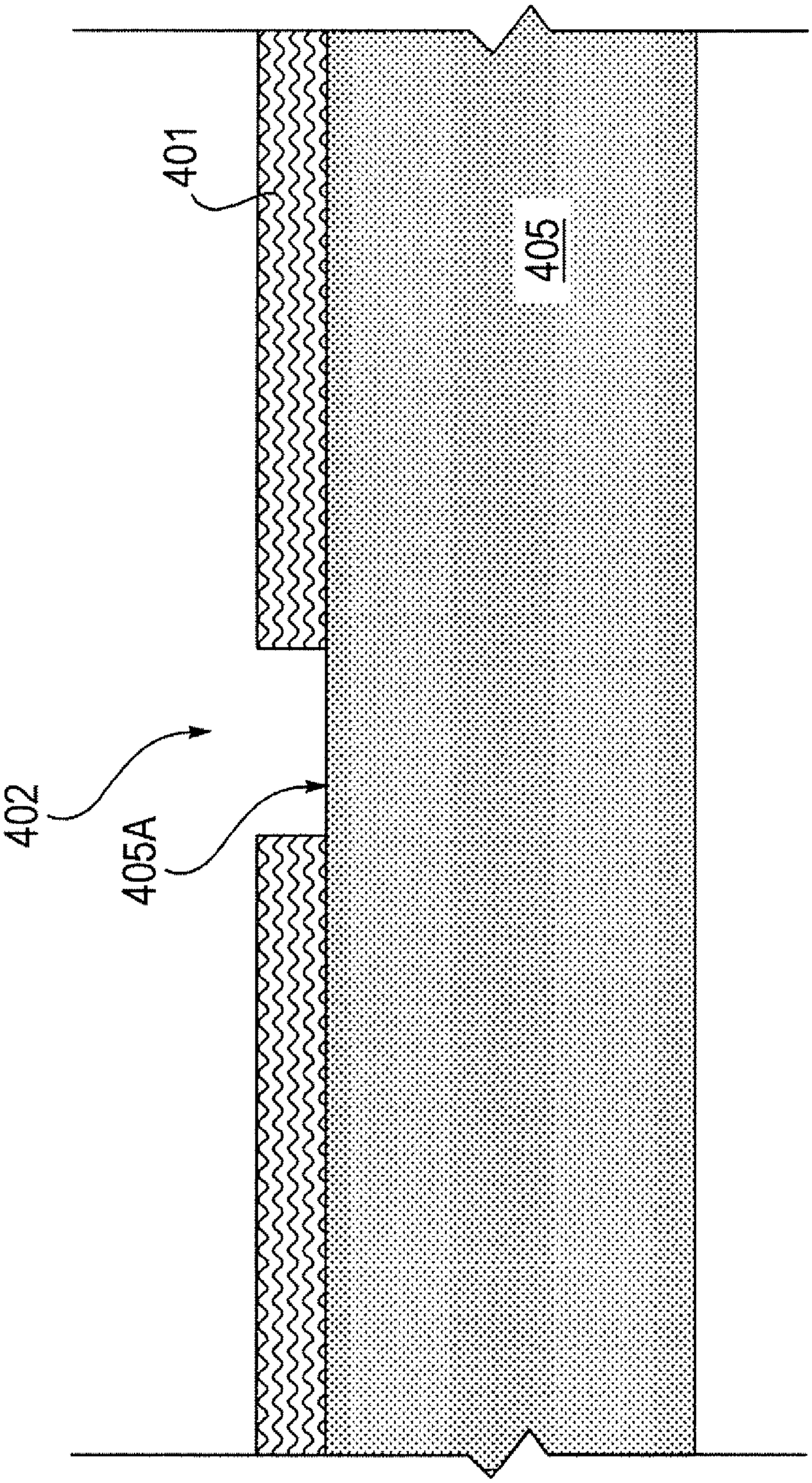


Figure 5A

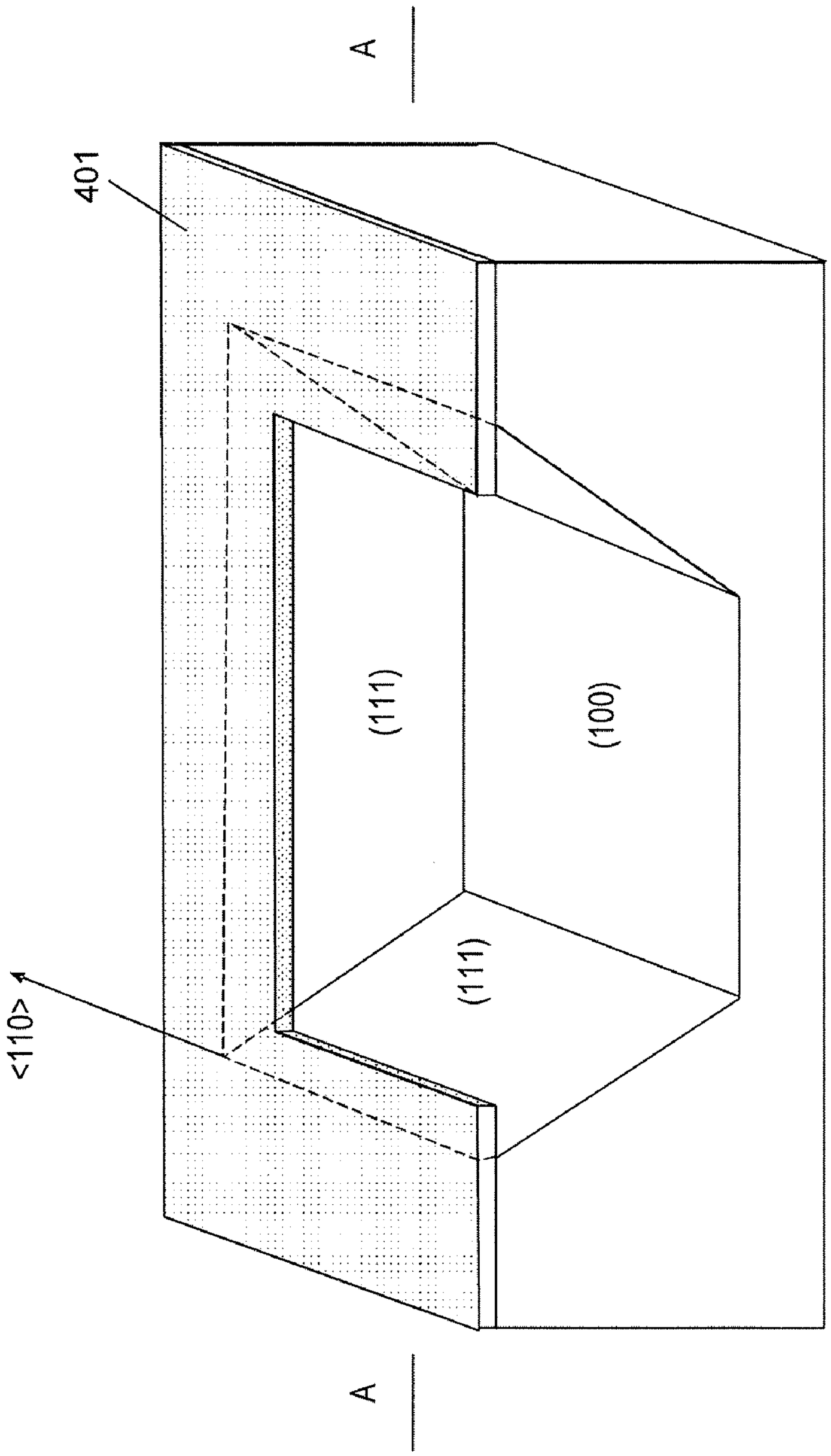


Figure 5B1

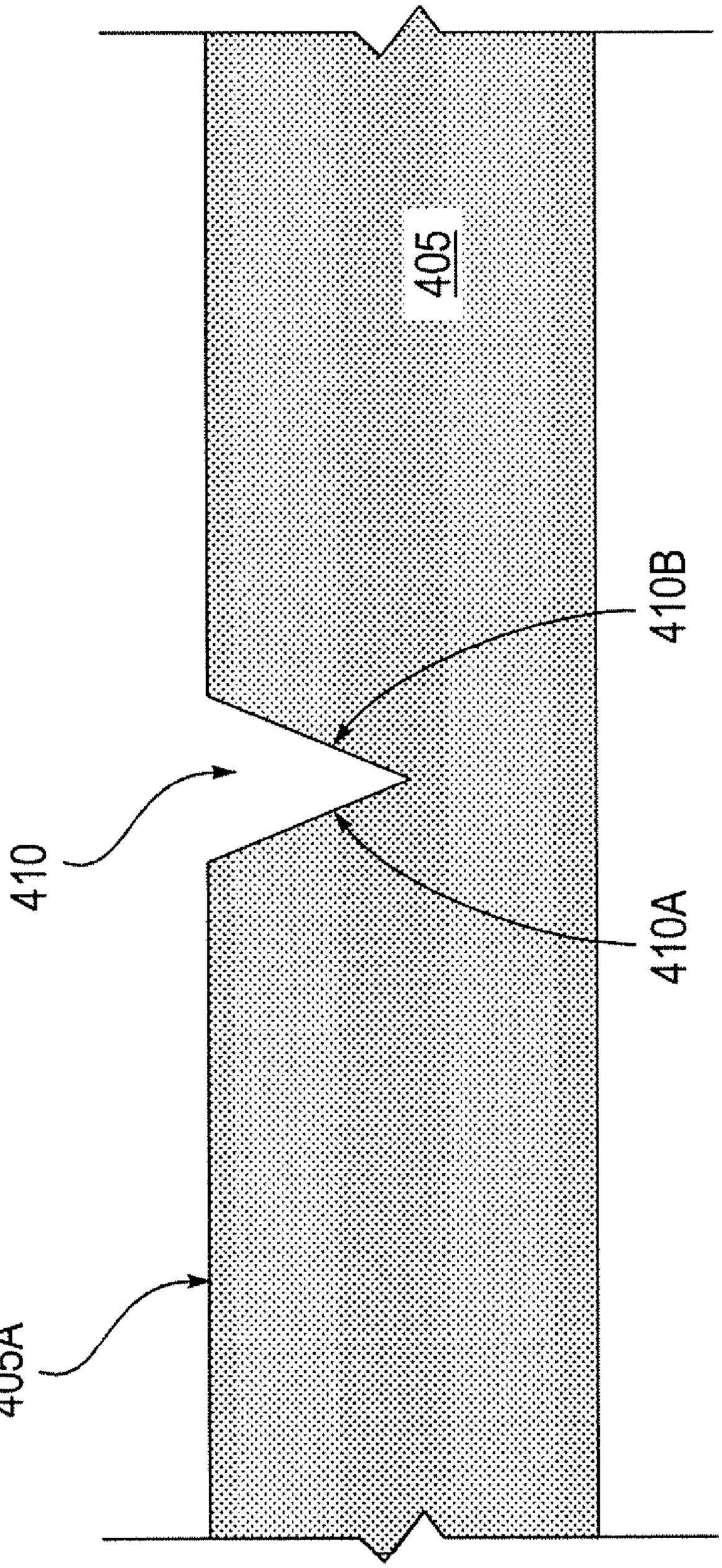


Figure 5B2

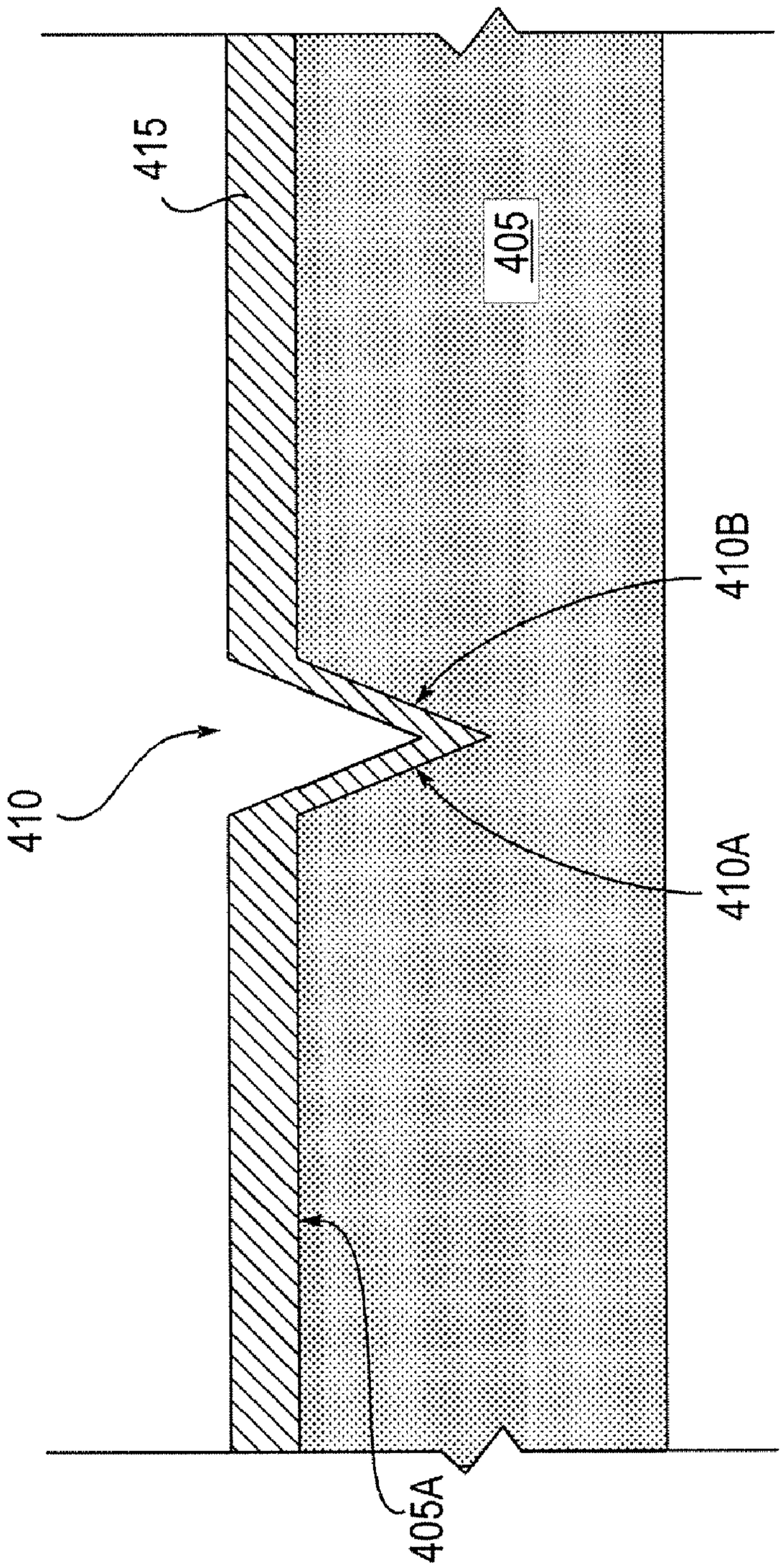


Figure 5C

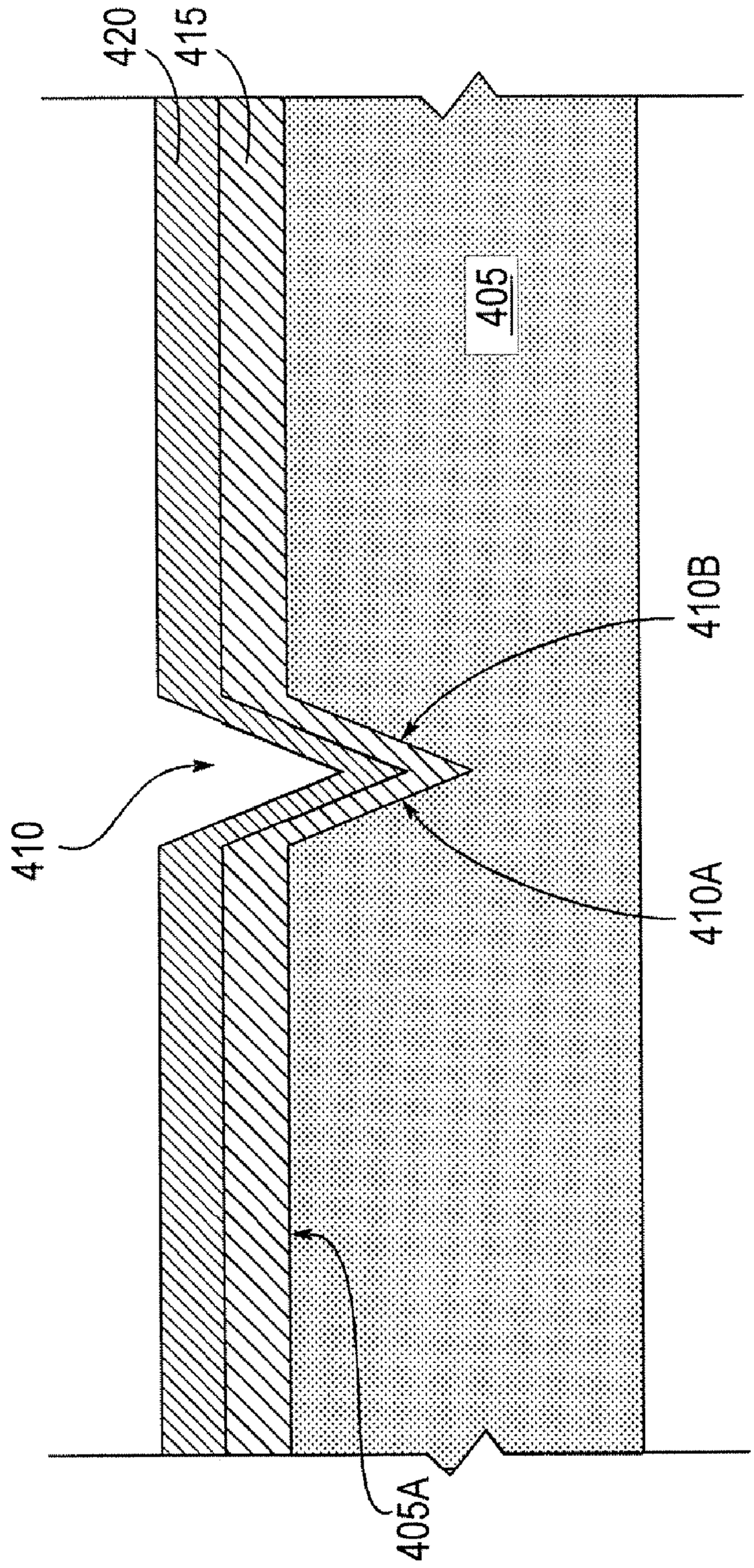


Figure 5D

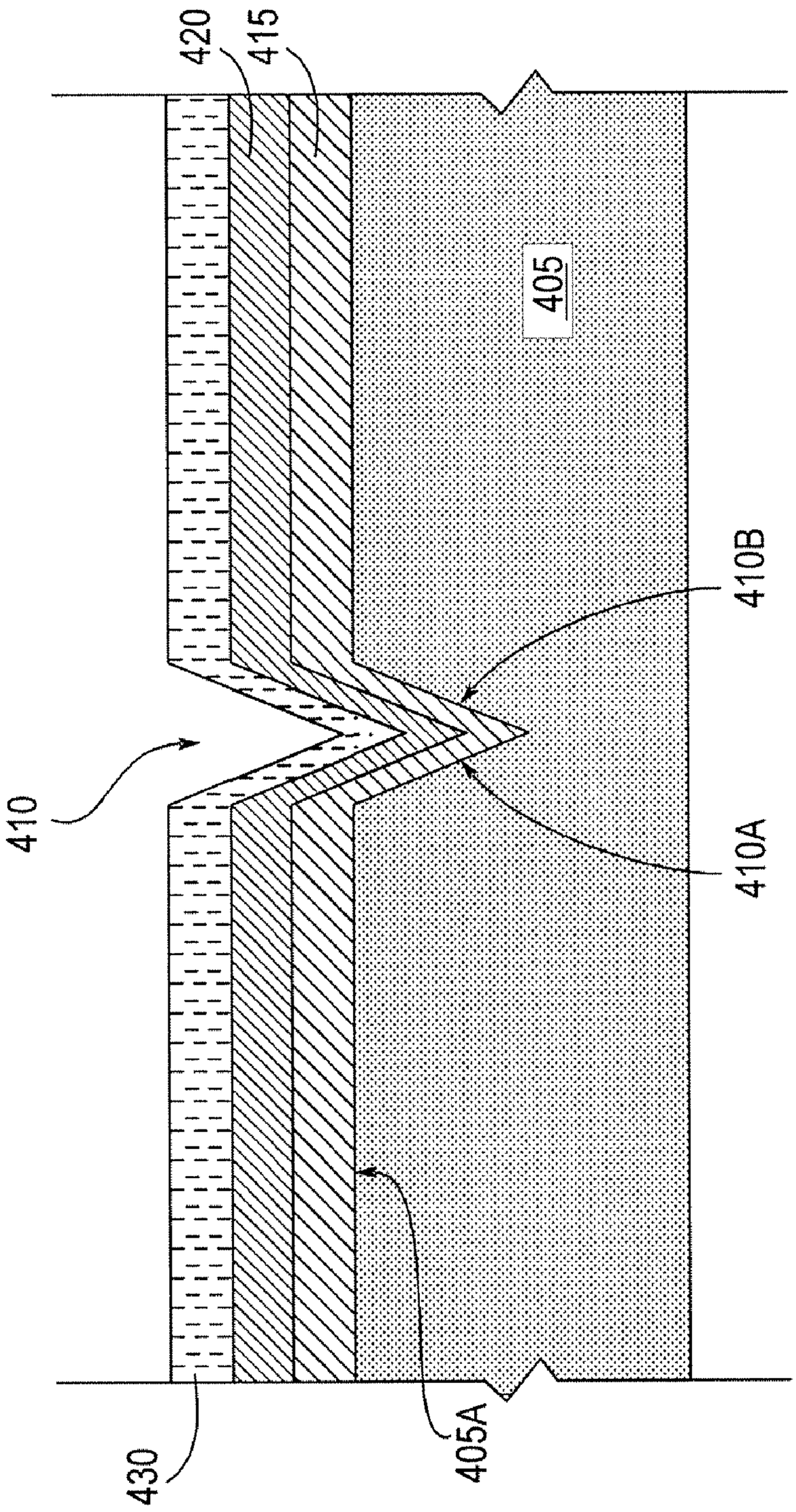


Figure 5E

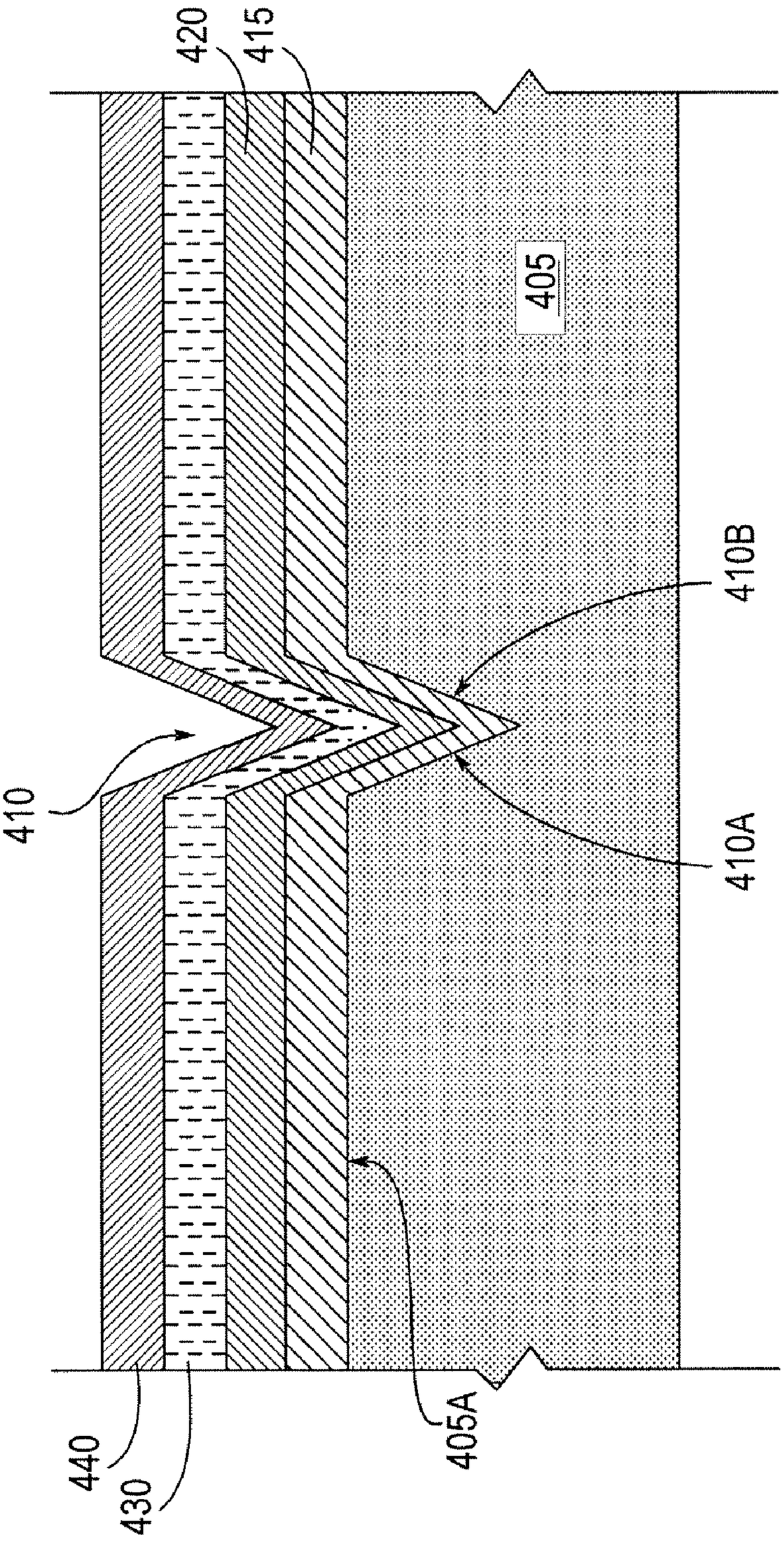


Figure 5F

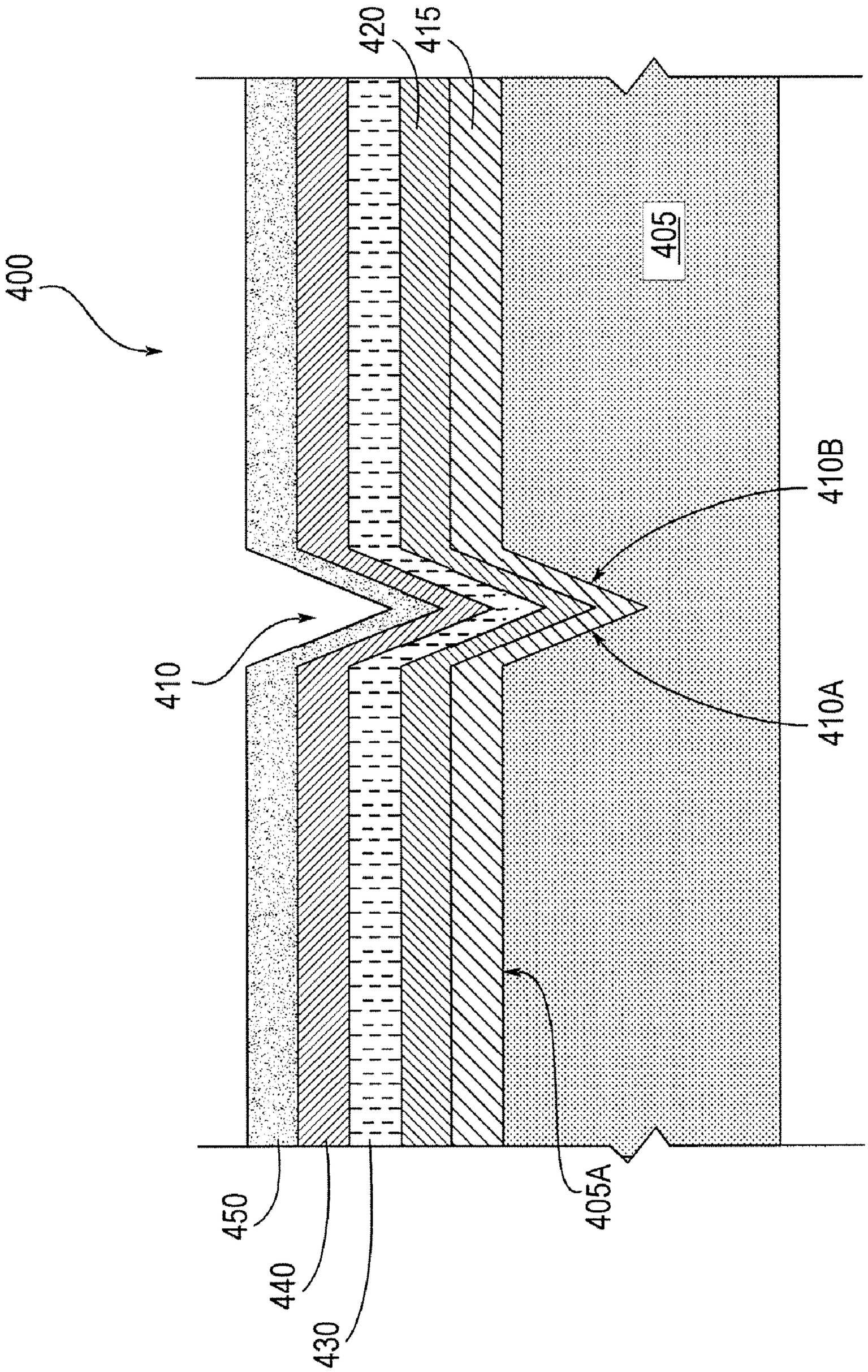


Figure 5G

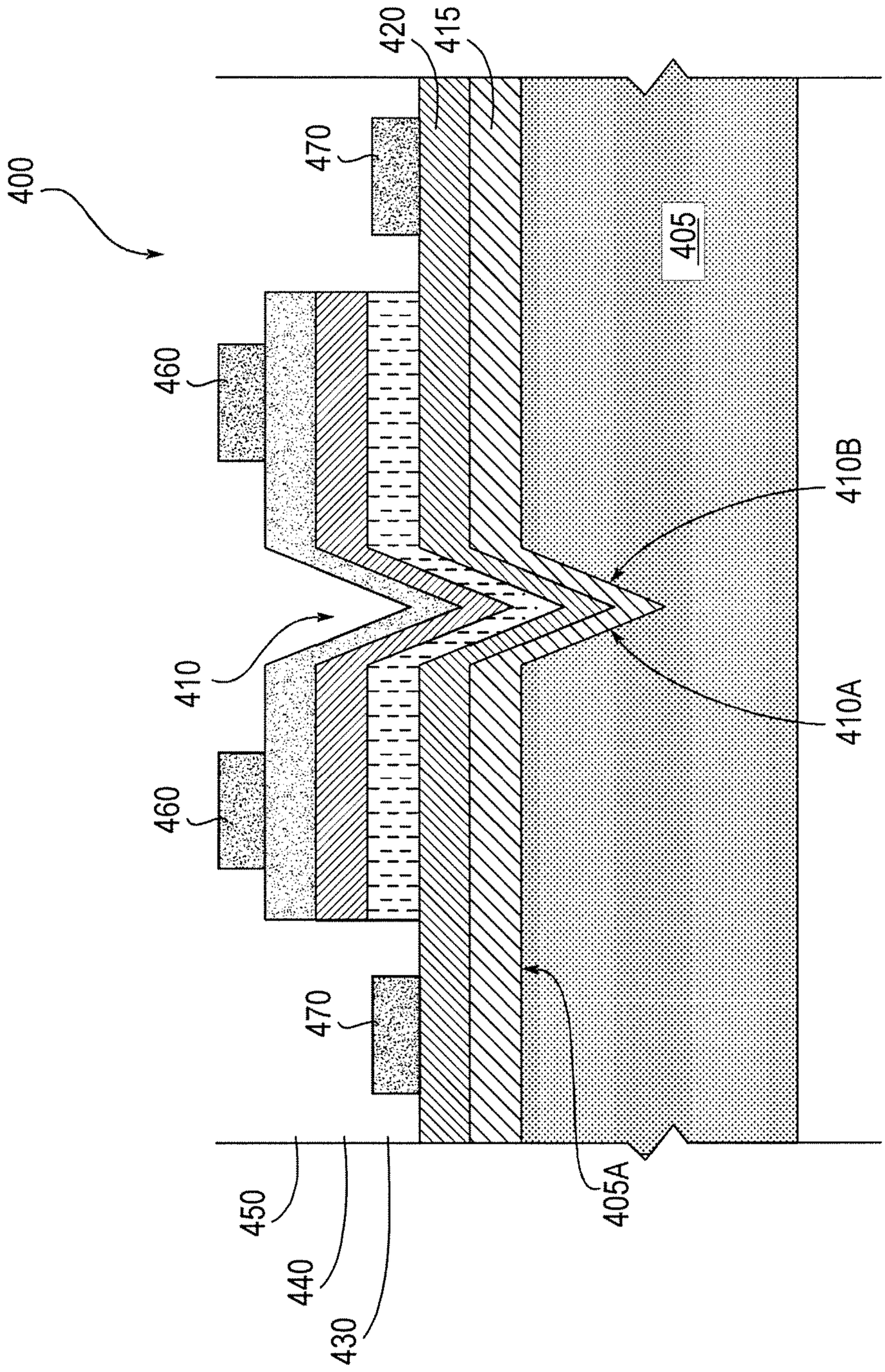


Figure 5H

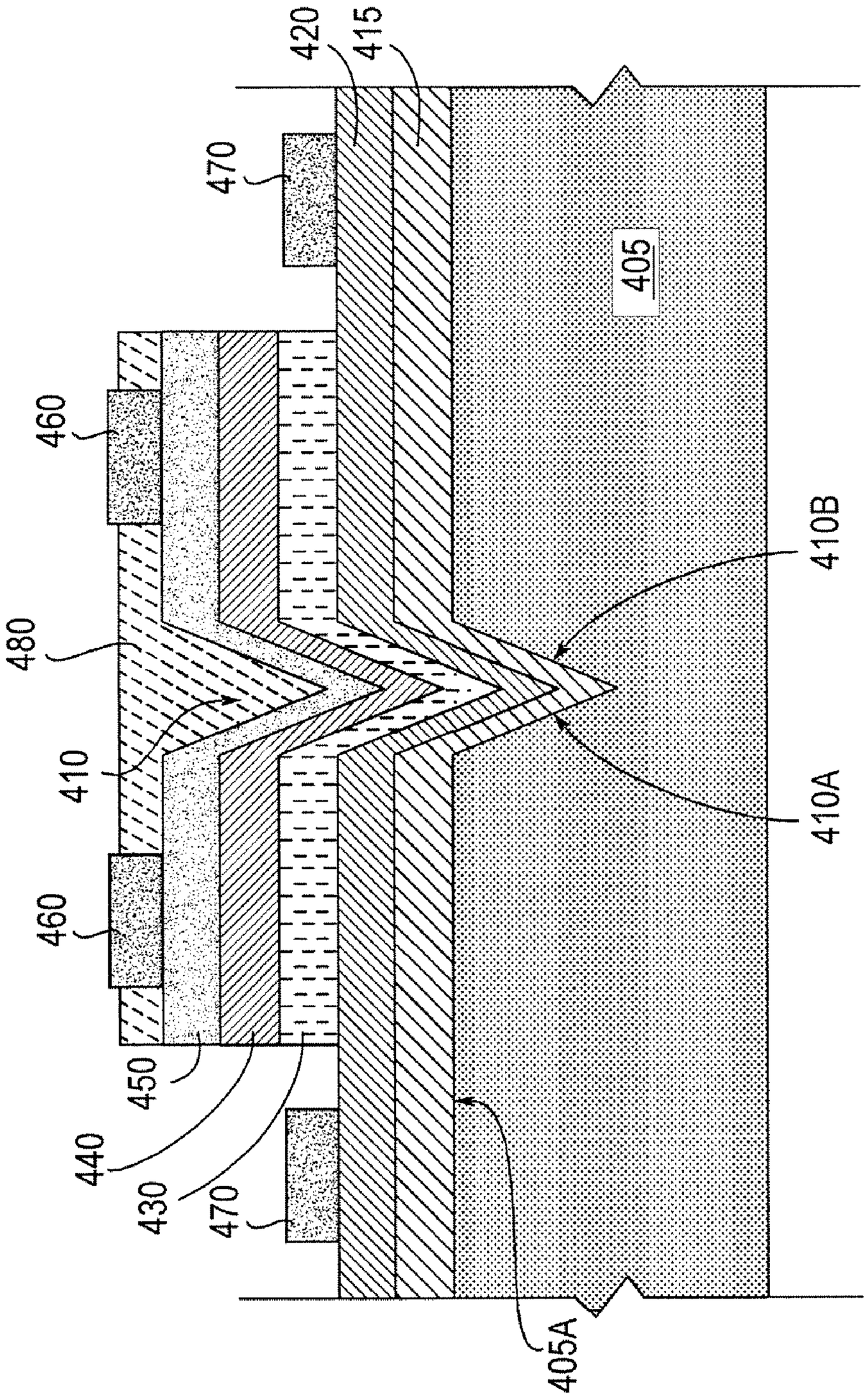


Figure 5I

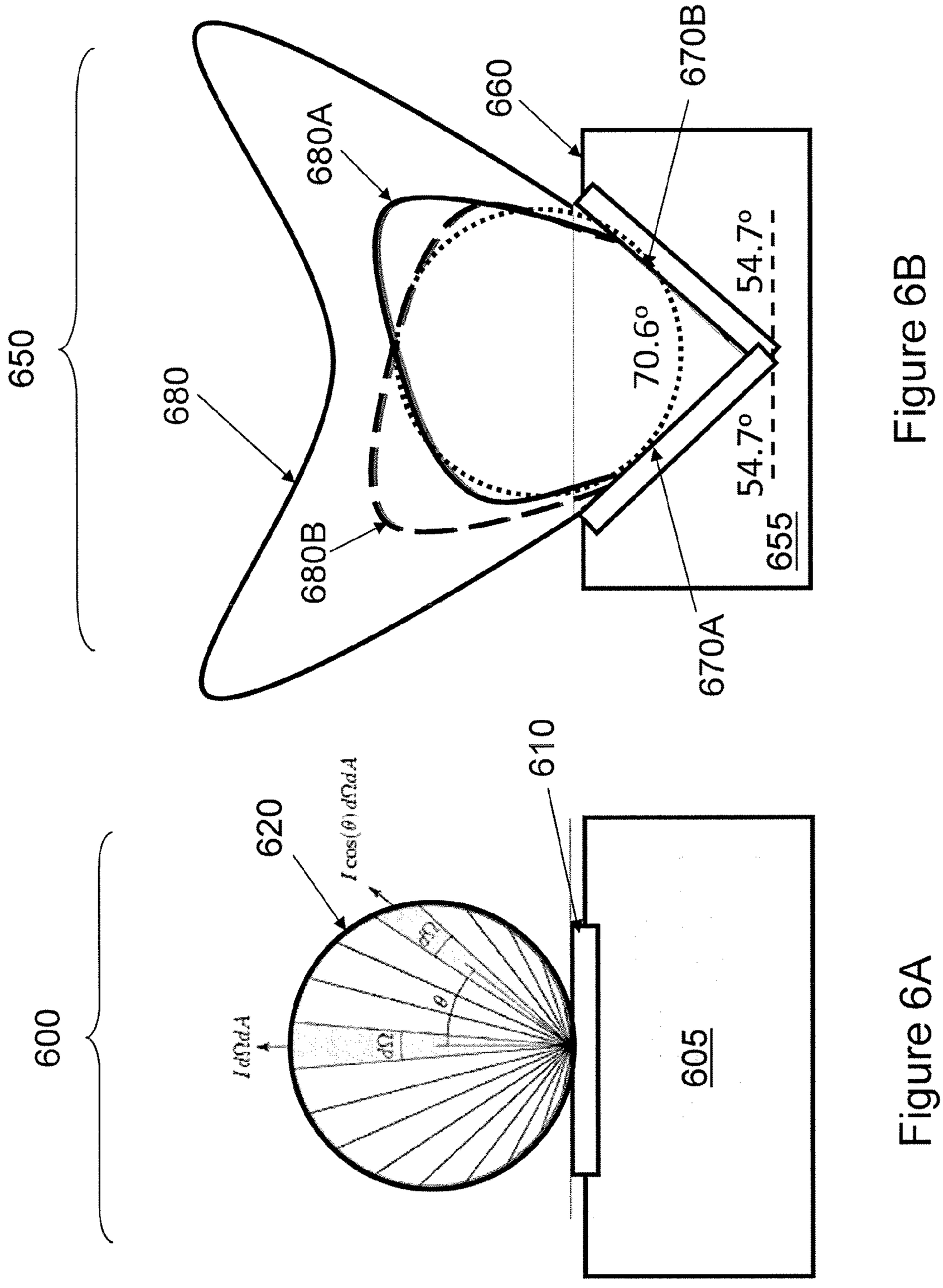


Figure 6A

Figure 6B

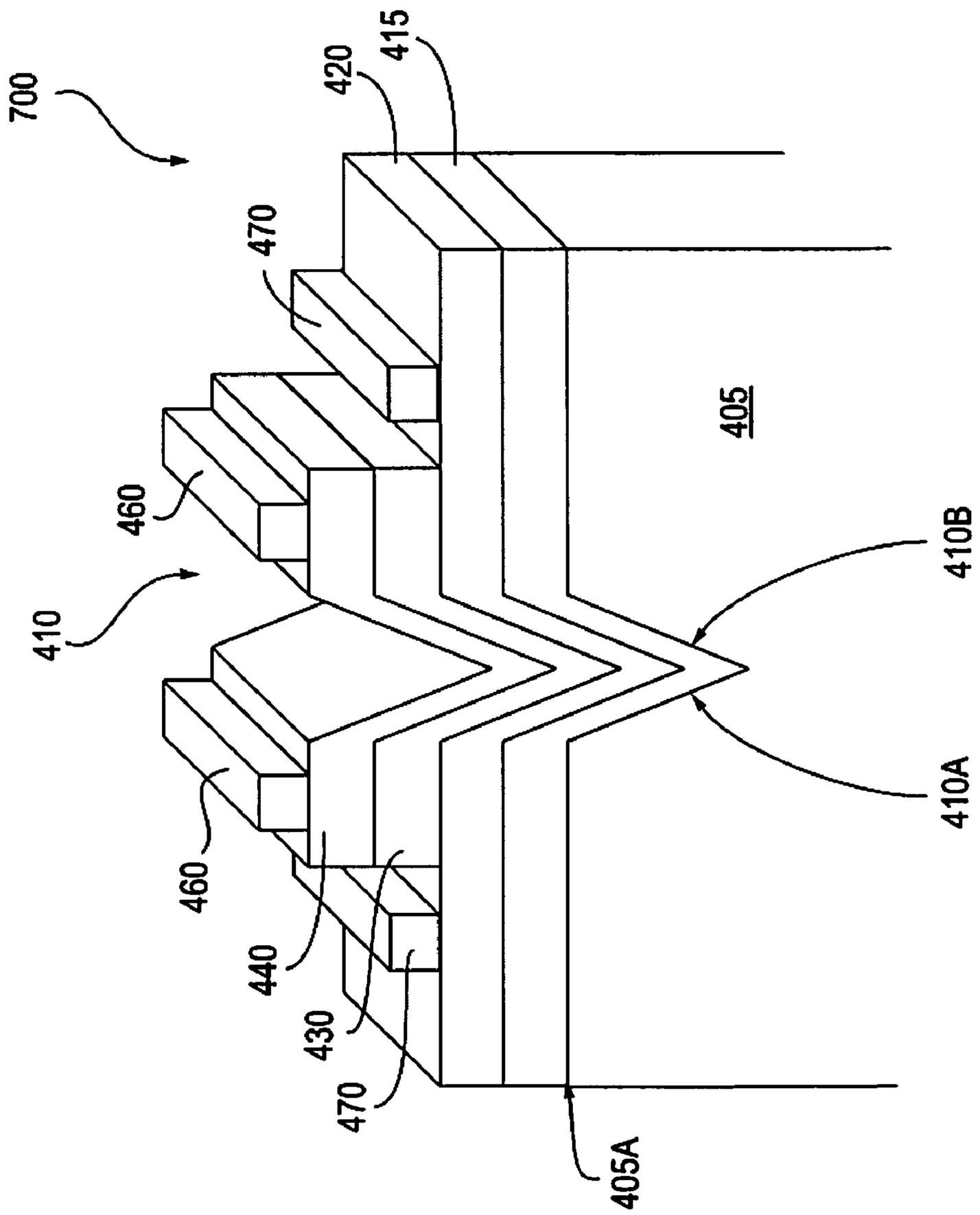


FIG. 7

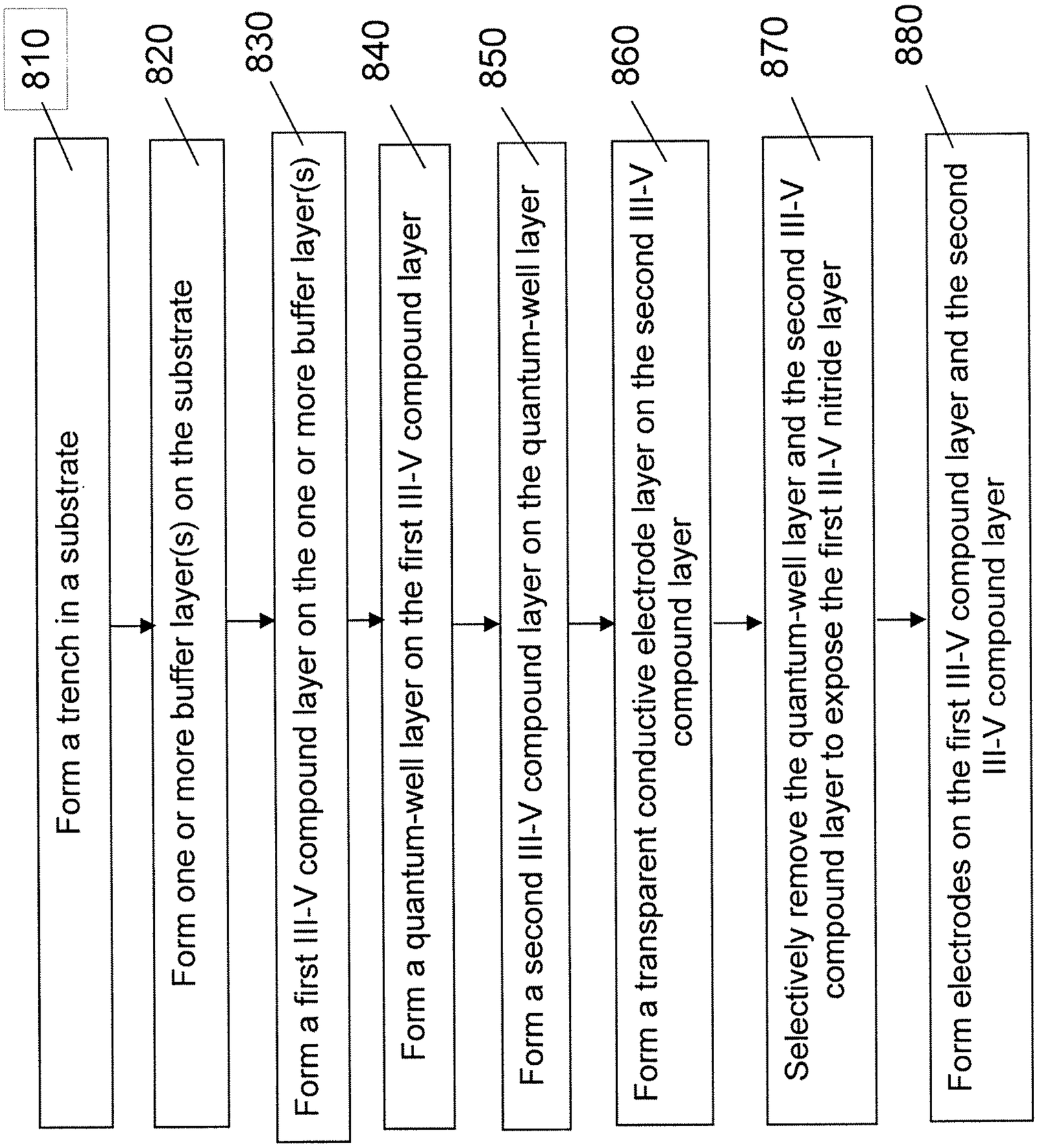

810
Form a trench in a substrate
820
Form one or more buffer layer(s) on the substrate
830
Form a first III-V compound layer on the one or more buffer layer(s)
840
Form a quantum-well layer on the first III-V compound layer
850
Form a second III-V compound layer on the quantum-well layer
860
Form a transparent conductive electrode layer on the second III-V compound layer
870
Selectively remove the quantum-well layer and the second III-V compound layer to expose the first III-V nitride layer
880
Form electrodes on the first III-V compound layer and the second III-V compound layer

Figure 8

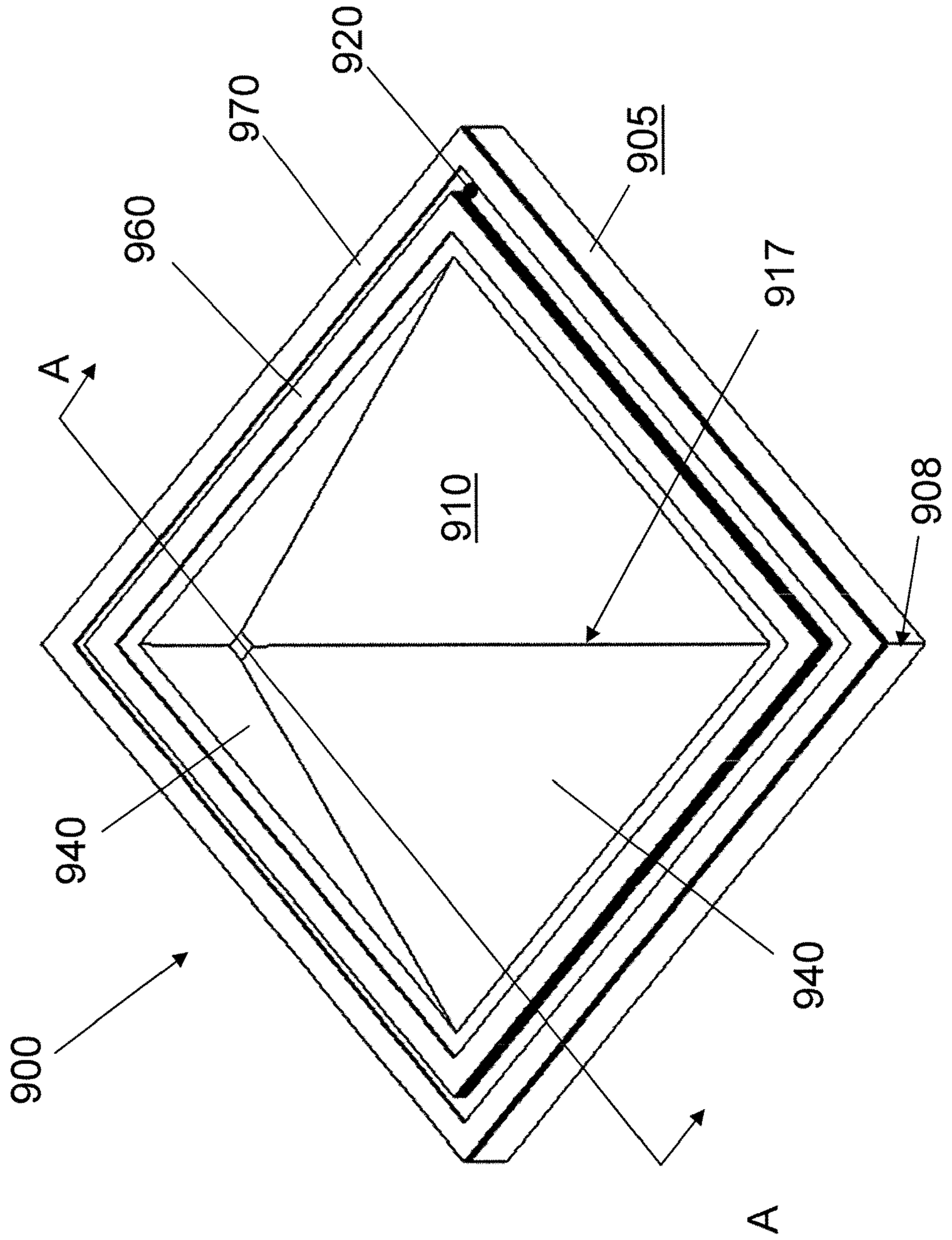


Figure 9A

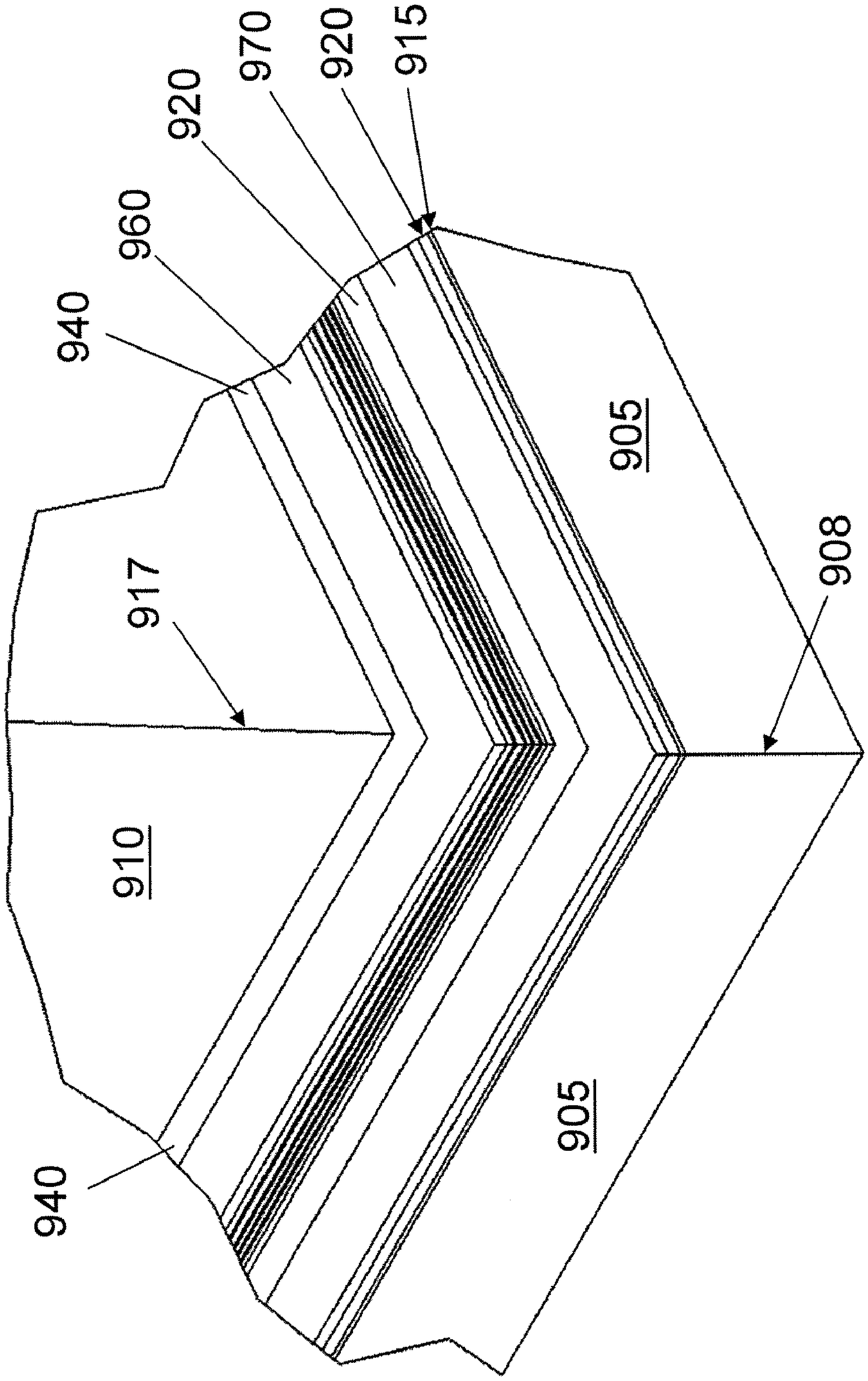


Figure 9B

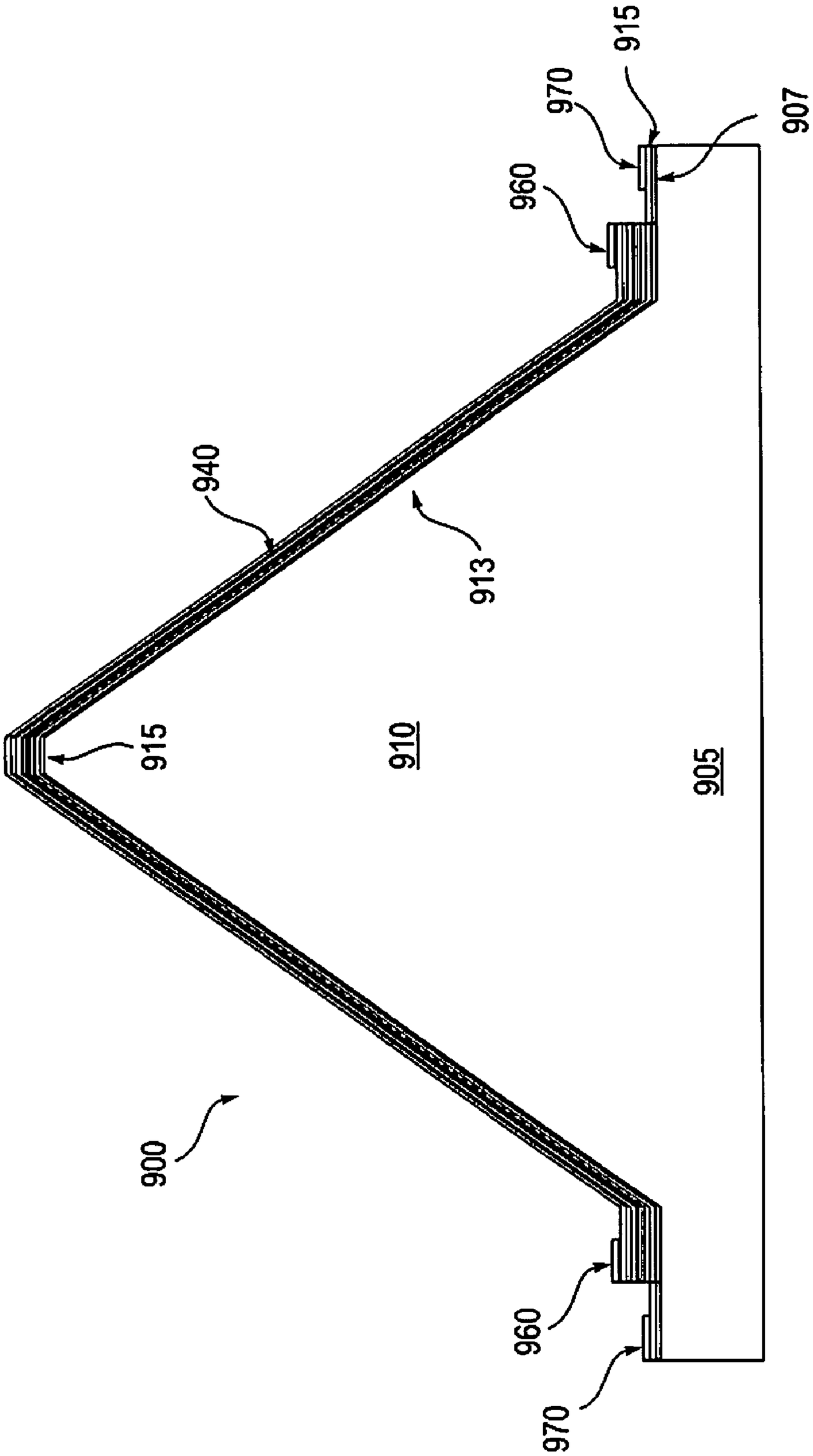


FIG. 10A

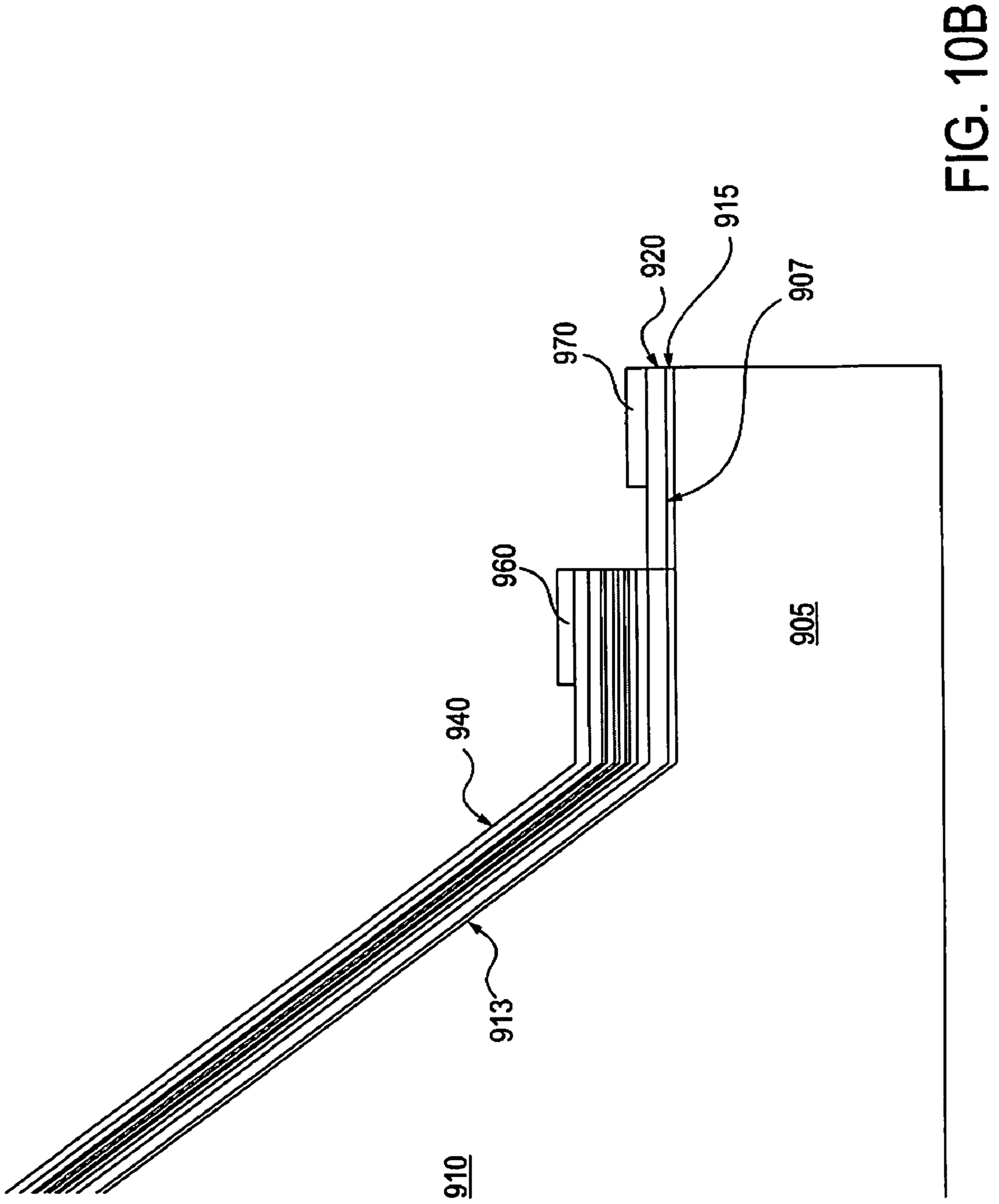


FIG. 10B

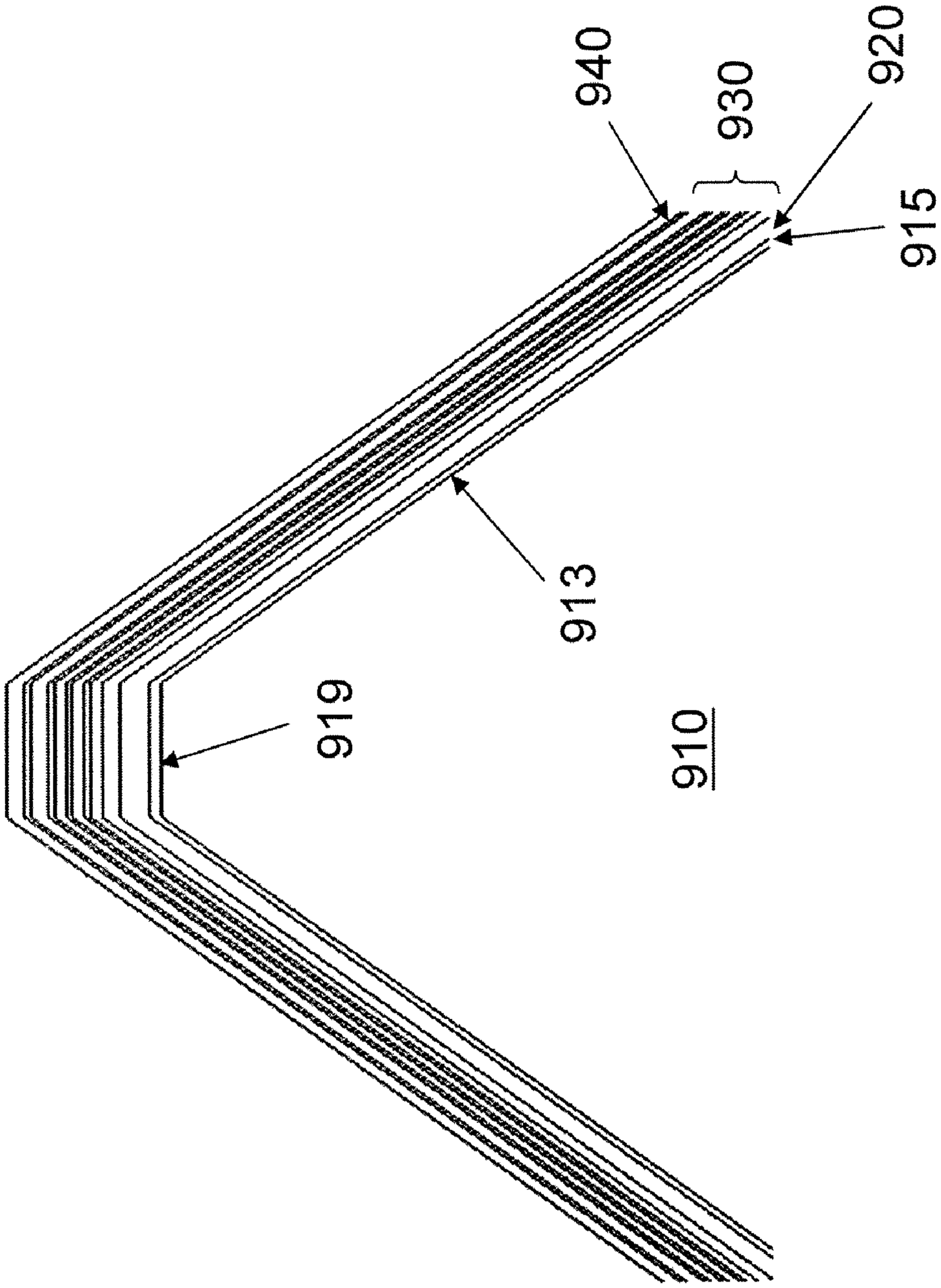


Figure 10C

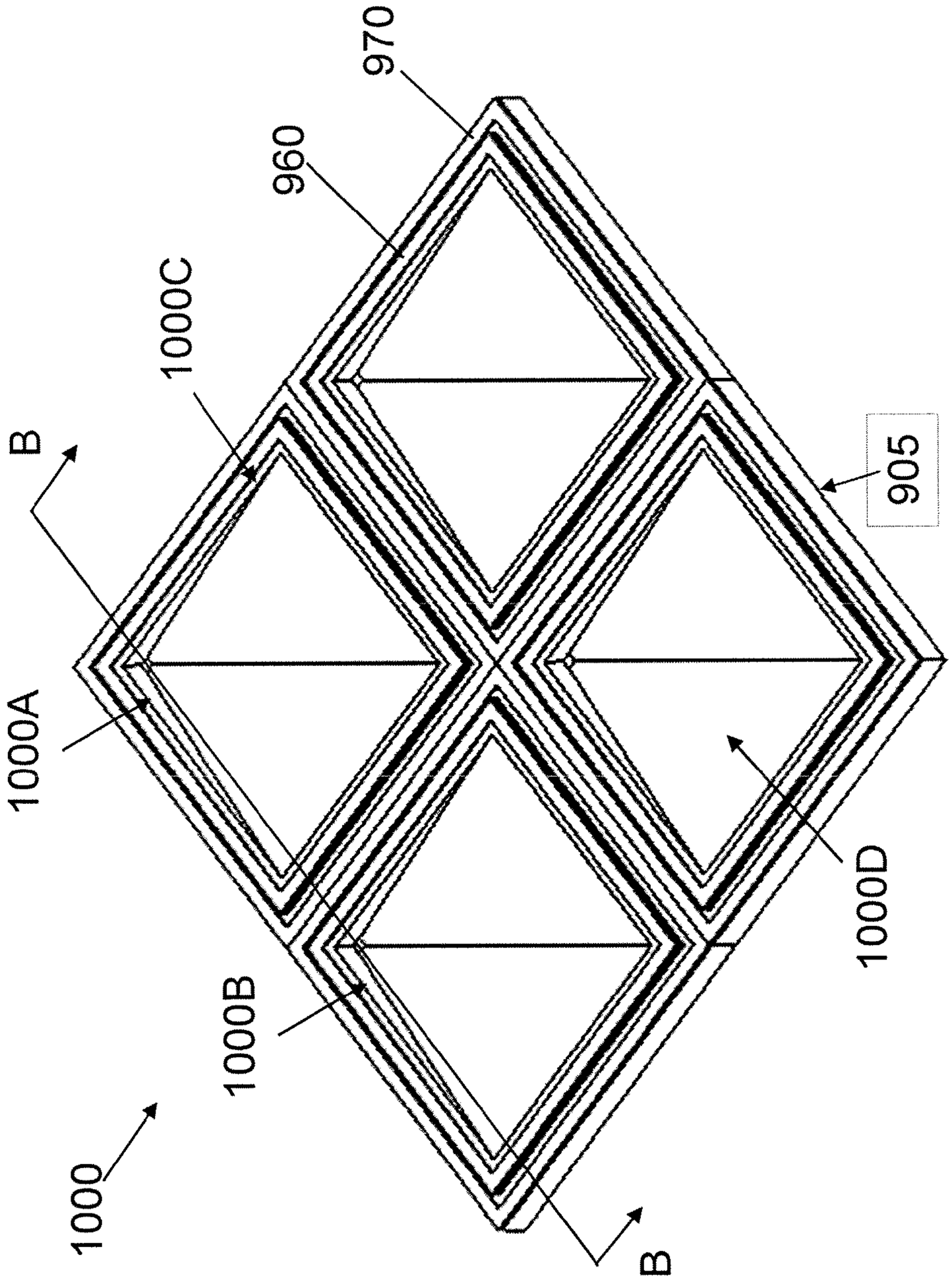


Figure 11A

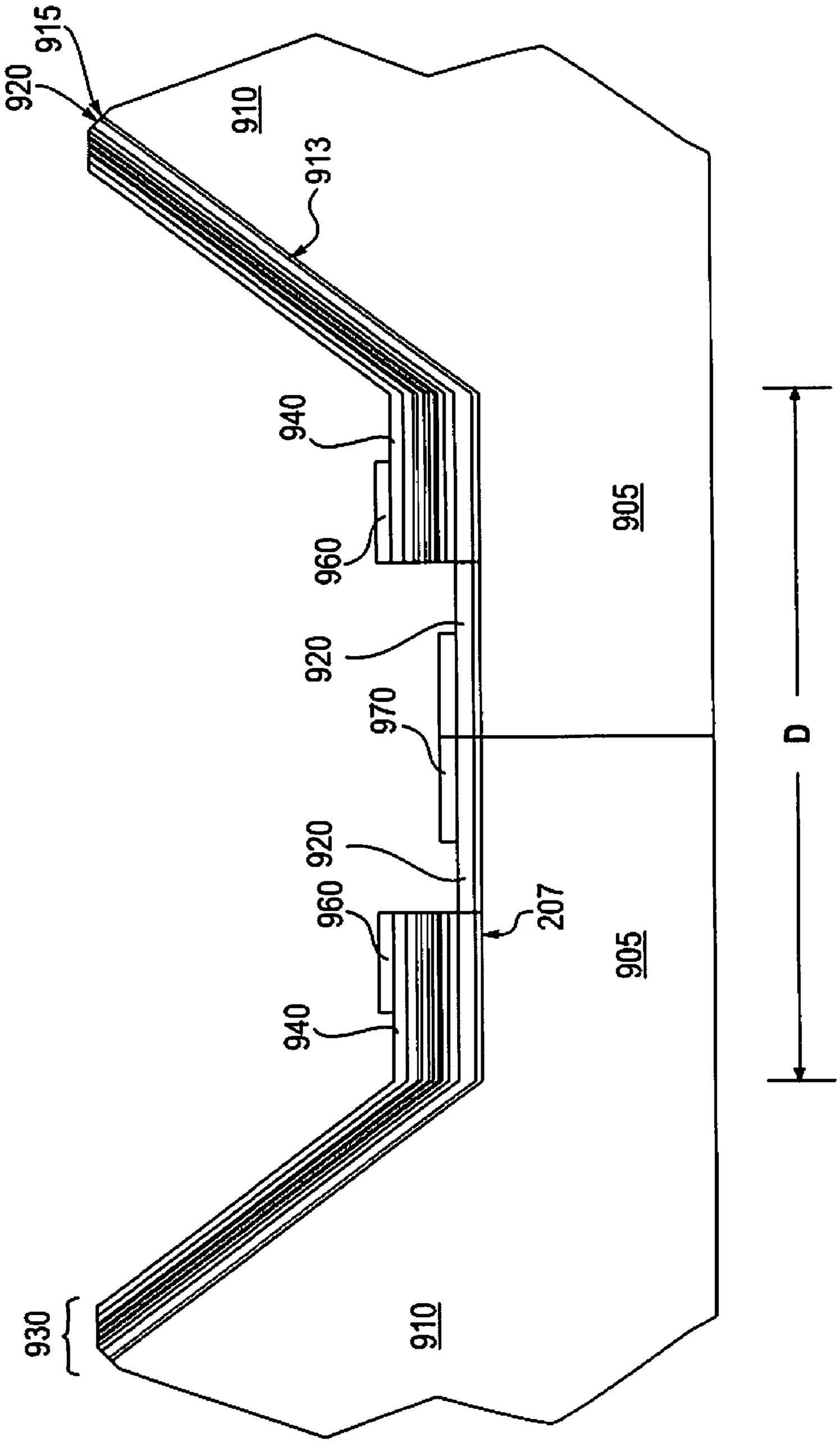


FIG. 11B

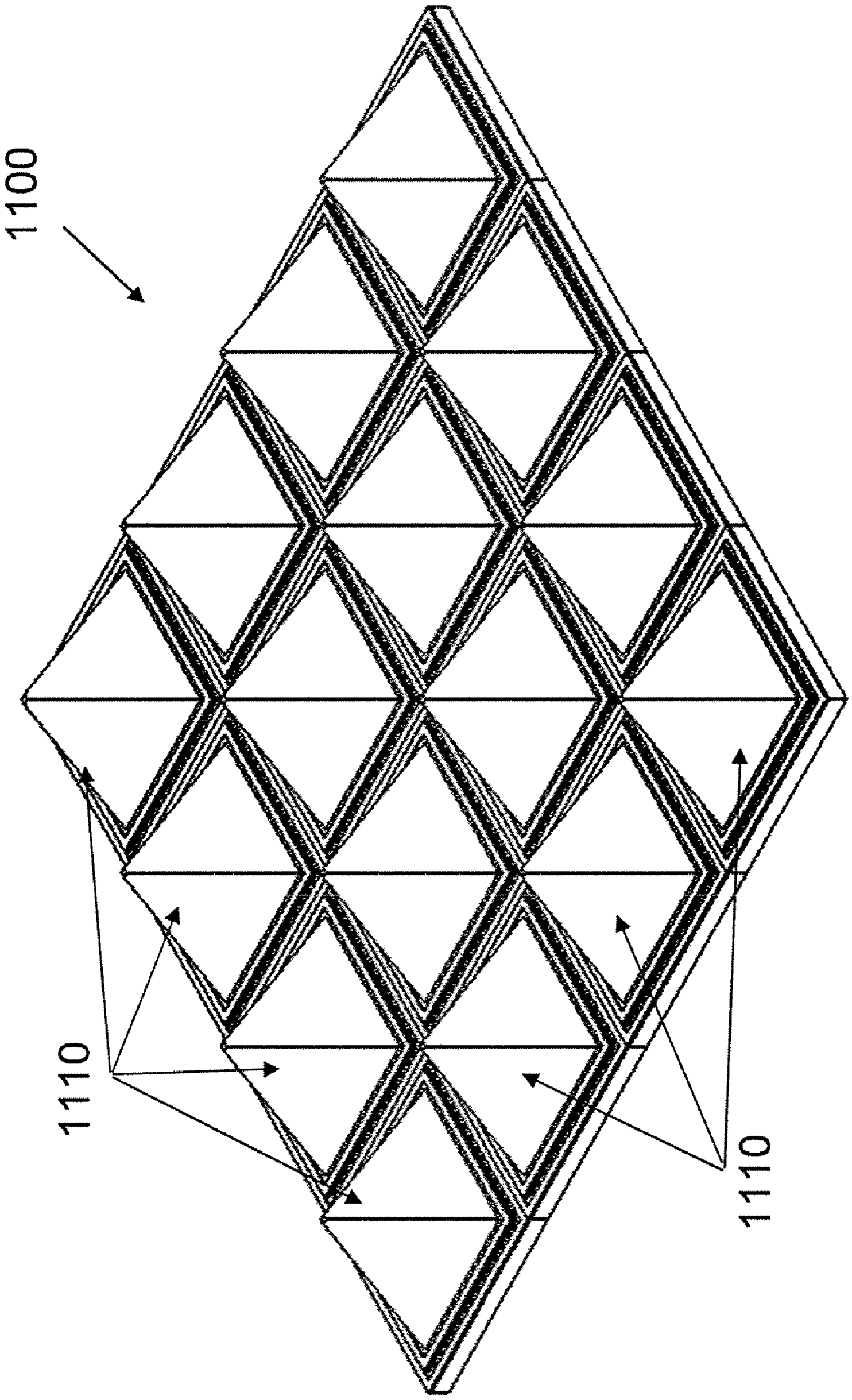


Figure 11C

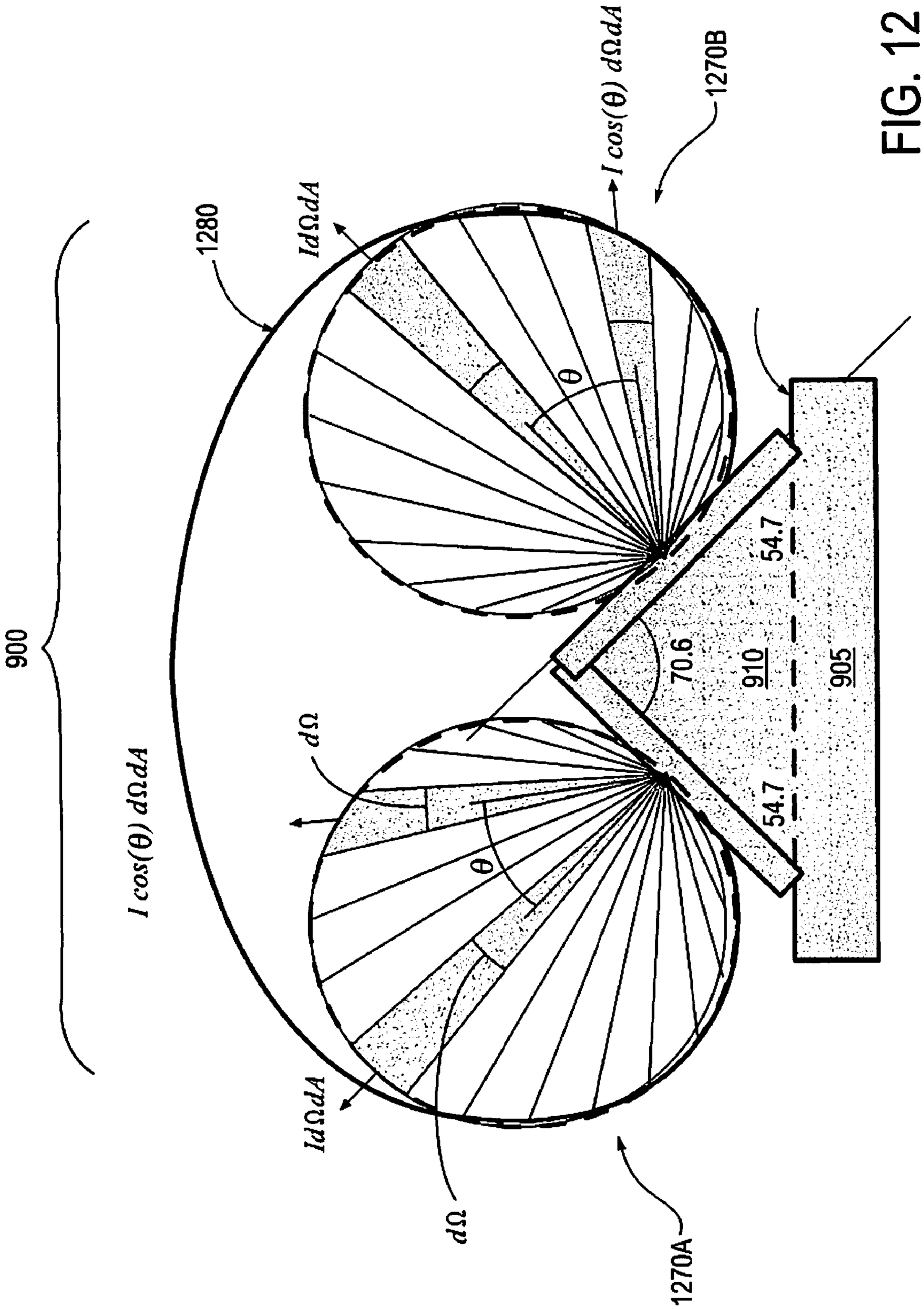

900
1280
$I\cos(\theta)\, d\Omega dA$
$Id\Omega dA$
$I\cos(\theta)\, d\Omega dA$
1270B
$d\Omega$
θ
θ
70.6
54.7
54.7
910
905
$Id\Omega dA$
$d\Omega$
1270A

FIG. 12

LIGHT EMITTING DEVICE

[0001] This application is a continuation-in-part of U.S. patent application Ser. No. 11/761,446 of S. Pan, filed on Jun. 12, 2007, which is incorporated herein by reference.

BACKGROUND

[0002] The present patent application is related to light emitting devices.

[0003] Solid-state light sources, such as light emitting diodes (LEDs) and laser diodes, can offer significant advantages over other forms of lighting, such as incandescent or fluorescent lighting. For example, when LEDs or laser diodes are placed in arrays of red, green and blue elements, they can act as a source for white light or as a multi-colored display. In such configurations, solid-state light sources are generally more efficient and produce less heat than traditional incandescent or fluorescent lights. Although solid-state lighting offers certain advantages, conventional semiconductor structures and devices used for solid-state lighting are relatively expensive. One of the costs related to conventional solid-state light emitting devices is related to the relatively low manufacturing throughput of the conventional solid-state light emitting devices.

[0004] Referring to FIG. **1**, a conventional LED structure **100** includes a substrate **105**, which may, for example, be formed of sapphire, silicon carbide, or spinel. A buffer layer **110** is formed on the substrate **105**. The buffer layer **110** serves primarily as a wetting layer, to promote smooth, uniform coverage of the sapphire substrate. The buffer layer **110** is typically formed of GaN, InGaN, AlN, or AlGaN and has a thickness of about 100-500 Angstroms. The buffer layer **310** is typically deposited as a thin amorphous layer using Metal Organic Chemical Vapor Deposition (MOCVD).

[0005] A p-doped Group III-V compound layer **120** is formed on the buffer layer **110**. The p-doped Group III-V compound layer **120** is typically made of GaN. An InGaN quantum-well layer **130** is formed on the p-doped Group III-V compound layer **120**. An active Group III-V compound layer **140** is then formed on the InGaN quantum-well layer **130**. An n-doped Group III-V compound layer **150** is formed on the layer **140**. The p-doped Group III-V compound layer **120** is n-type doped. A p-electrode **160** is formed on the n-doped Group III-V compound layer **150**. An n-electrode **170** is formed on the first Group III-V compound layer **120**.

[0006] A drawback of the conventional LED structure **100** is the low manufacturing throughput associated with the small substrate dimensions. For example, sapphire or silicon carbide substrates are typically supplied in diameters of 2 to 4 inches. Another drawback of the conventional LED structure **100** is that its layered structure often suffers from cracking. Suitable substrates such as sapphire or silicon carbide are typically not available in single crystalline forms. The p-doped Group III-V compound layer **120** can suffer from cracking or delamination due to differential thermal expansions and lattice mismatching between the p-doped Group III-V compound layer and the substrate even in the presence of the buffer layer **110**. The differential thermal expansions and lattice mismatching can also produce a bowing deformation (i.e. curling up) in the LED structure. As a result, light emitting performance of the LED structure **100** can be compromised.

[0007] Accordingly, there is therefore a need for a light emitting device that can overcome some or all of the drawbacks in the conventional light emitting systems.

SUMMARY OF THE INVENTION

[0008] In one aspect, the present invention relates to a light emitting device that includes a substrate having a first surface and a second surface not parallel to the first surface; and a light emission layer disposed over the second surface to emit light, the light emission layer having a light emission surface which is not parallel to the first surface.

[0009] In another aspect, the present invention relates to a light emitting device that includes a substrate; and a light emission layer disposed over the substrate to emit light, the light emission layer having a footprint area and having a light emission surface area which is greater than the footprint area.

[0010] In another aspect, the present invention relates to a light emitting device that includes a substrate having a first surface; a light emission layer disposed over at least a portion of the substrate, the light emission layer having a light emission surface that is not parallel to the first surface; and a reflective buffer layer disposed over at least a portion of the light emission layer, to reflect light emitted from the light emission layer, and wherein the reflective buffer layer has a reflectance coefficient higher than 30% in a spectral range of light emitted by the light emission layer.

[0011] In another aspect, the present invention relates to a light emitting device that includes a substrate having a first surface and a trench formed in the first surface; and a light emission layer disposed within the trench to emit light, the light emission layer having a light emission surface which is not parallel to the first surface, wherein the first surface outside of the trench can include at least one width dimension narrower than 1000 microns.

[0012] In another aspect, the present invention relates to a light emitting device that includes a substrate having a first surface and a protrusion formed on the first surface; and a light emission layer disposed on the protrusion to emit light, the light emission layer having a light emission surface which is not parallel to the first surface.

[0013] In another aspect, the present invention relates to a light emitting device that includes a substrate having a first surface; a trench formed in the substrate, wherein the trench is defined in part by a plurality of first trench surfaces that are not parallel to the first surface; a reflective buffer layer on at least a portion of the first surface and the plurality of first trench surfaces; and a light emitting layer over the reflective buffer layer, wherein the light emitting layer can emit light away from the reflective buffer layer, wherein the light emitted is confined in an angular range narrower than 150 degrees.

[0014] In another aspect, the present invention relates to a method for fabricating a light emitting device. The method includes forming a light emission layer over a substrate having a first surface and a second surface not parallel to the first surface, wherein the light emission layer has a light emission surface not parallel to the first surface, wherein the light emission layer can emit light.

[0015] Implementations of the system may include one or more of the following. The light emission layer can include a quantum-well layer that can emit light when an electric current is produced in the quantum-well layer. The quantum-well layer can include a layer formed by a material selected from the group consisting of InN, InGaN, GaN, AlGaN, and InGaAlN. The light emitting device can further include a

buffer layer between the substrate and the light emission layer. The buffer layer can have a reflectance coefficient higher than 30% in the spectral range of the light emitted by the light emission layer. The buffer layer can have a reflectance coefficient higher than 50% in the spectral range of the light emitted by the light emission layer. The buffer layer can have a thickness in the range of 200 to 200,000 Angstroms. The buffer layer can include aluminum, aluminum nitride, an aluminum alloy, or Ag and its alloy, as reflective buffer layer. The buffer layer can include a material selected from the group consisting of GaN, ZnO, AlN, HfN, AlAs, SiCN, TaN, and SiC. The light emitting device can further include a lower Group III-V compound layer between the substrate and the light emission layer and an upper Group III-V compound layer over the light emission layer. The substrate can have a trench formed in the first surface, and wherein the light emission layer is disposed within the trench. The first surface outside of the trench can include at least one width dimension narrower than 1000 microns. The substrate can have a protrusion formed on the first surface, and wherein the light emission layer is disposed on the protrusion. The first surface outside of the protrusion can include at least one width dimension narrower than 1000 microns. The substrate can include silicon, silicon oxide, gallium nitride, silicon carbide, or sapphire. The substrate can include a silicon-on-insulator (SOI) structure, or simply a silicon bonded on glass to form a stop layer for interconnect electrodes.

[0016] An advantage associated with the disclosed light emitting device is that it significantly increases light emission intensity comparing to conventional LED light emitting devices. The disclosed light emitting devices and methods provide much larger light emitting surface than conventional LED light emitting devices having the same substrate foot print. A reflective layer under the disclosed light emitting devices can decrease absorption-related light loss and further increase emission efficiency. A transparent conductive layer formed on the upper Group III-V compound layer of the disclosed light emitting device can increase electric contact between the upper electrode and the upper III-V layer, and at the same time, maximize light emission intensity from the disclosed light emitting device.

[0017] Another advantage associated with the disclosed light emitting device is that its light emission is focused in much narrower angular range than conventional LED light emitting devices. The more concentrated angular light emission in the disclosed light emitting device reduces the light loss to unwanted directions and can thus increase brightness in the intended illumination directions and reduce energy consumption.

[0018] Another advantage associated with the disclosed light emitting device is that it is more practical to manufacture, robust, and reliable than some conventional light emitting systems. The disclosed light emitting devices and fabrication processes can overcome differential thermal expansions and lattice mismatch between the lower group compound III-V layer and the substrate and prevent associated layer cracking and delamination, problems known in conventional LED lighting systems.

[0019] The disclosed light emitting device and fabrication processes allow for high-throughput and high-volume manufacturing of the light emitting devices. A large number of solid state LEDs can be fabricated on a large substrate such as a silicon wafer or a glass substrate. Manufacturing throughput can be much improved since silicon wafer can be provided in much larger dimensions (e.g. 6 to 12 inch silicon wafers) compared to the small substrates used in the conventional light emitting devices. The disclosed light emitting device can be fabricated using commercially available semiconductor processing equipment such as ALD and MOCVD systems without using customized fabrication equipments, which makes the disclosed manufacturing process easily implemented. The disclosed light emitting device can thus be fabricated more efficiently in cost and time than some conventional light emitting devices that need.

[0020] Furthermore, the disclosed light emitting devices can be made more integrated, compact, and cost effective compared to some conventional LED devices. The disclosed light emitting devices can be fabricated on a silicon-based substrate which allows the integration of electronic control circuitry in the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The following drawings, which are incorporated in and from a part of the specification, illustrate embodiments of the present invention and, together with the description, serve to explain the principles of the invention.

[0022] FIG. **1** is a cross-sectional view of a conventional LED structure.

[0023] FIG. **2**A is a perspective view of a light emitting device in accordance with one embodiment of the present application.

[0024] FIG. **2**B is a detailed perspective view of the front corner portion of the light emitting device in FIG. **2**A.

[0025] FIG. **3**A is a cross-sectional view of the light emitting device along line A-A in FIG. **2**A.

[0026] FIG. **3**B is a detailed cross-sectional view of a side portion of the light emitting device in FIG. **3**A.

[0027] FIG. **3**C is a detailed cross-sectional view of the bottom portion of the light emitting device in FIG. **3**A.

[0028] FIG. **3**D is a cross-sectional view the light emitting structures along line B-B in FIG. **2**A.

[0029] FIGS. **3**E and **3**F illustrate examples of layer structures and material compositions for the light emitting structures.

[0030] FIG. **4**A is a perspective view of a 2×2 array of light emitting structures fabricated on a substrate in accordance with the present application.

[0031] FIG. **4**B is a partial cross-sectional view of the light emitting structures along line B-B in FIG. **4**A.

[0032] FIG. **4**C is a perspective view of a 4×4 array of light emitting structures fabricated on a substrate in accordance with the present application.

[0033] FIG. **5**A is a cross-sectional view of a substrate having a patterned mask for preparing for forming the light emitting device of FIG. **4**B.

[0034] FIG. **5**B**1** is a perspective view of the light emitting device in FIG. **5**A after etching through the mask shown in FIG. **5**A.

[0035] FIGS. **5**B**2** and **5**C-**5**I are cross-sectional views at different steps of forming the light emitting device of FIG. **4**B.

[0036] FIG. **6**A is a schematic diagram illustrating an example of the emission angular distribution of a conventional LED light emitting device.

[0037] FIG. **6**B is a schematic diagram illustrating angular distribution of light emission from the light emitting device illustrated in FIG. **2**A.

[0038] FIG. **7** is a perspective view of another light emitting device in accordance with the present application.

[0039] FIG. **8** is a flowchart for a fabricating process for the silicon-based light emitting devices of FIGS. **2**-**7**.

[0040] FIG. **9**A is a perspective view of a light emitting device in accordance with another embodiment of the present application.

[0041] FIG. **9**B is a detailed perspective view of the front corner portion of the light emitting device in FIG. **9**A.

[0042] FIG. **10**A is a cross-sectional view of the light emitting device along line A-A in FIG. **9**A.

[0043] FIG. **10**B is a detailed cross-sectional view of a side portion of the light emitting device in FIG. **10**A.

[0044] FIG. **10**C is a detailed cross-sectional view of the top portion of the light emitting device in FIG. **10**A.

[0045] FIG. **11**A is a perspective view of a 2×2 array of light emitting structures fabricated on a substrate in accordance with the present application.

[0046] FIG. **11**B is a partial cross-sectional view of the light emitting structures along line B-B in FIG. **11**A.

[0047] FIG. **11**C is a perspective view of a 4×4 array of light emitting structures fabricated on a substrate in accordance with the present application.

[0048] FIG. **12** is a schematic diagram illustrating angular distribution of light emission from the light emitting device illustrated in FIG. **9**A.

DESCRIPTION OF THE INVENTION

[0049] Referring to FIGS. **2**A to **3**C, a light emitting device **200** is formed on a substrate **205** having an upper surface **207** (FIG. **3**B). The light emitting device **200** includes a trench **210** in the substrate **205** below the upper surface **207**. The trench **210** has one or more trench surfaces **213** (FIG. **3**B) at a slope relative to the upper surface **207**. The trench **210** can also have a bottom surface **219** that is parallel to the upper surface **207**. The area of the bottom surface **219** can be kept smaller than 20% of one of the trench surfaces **213**. The substrate **205** can be silicon based: the upper surface **207** can be parallel to the (100) crystalline plane. The trench surface **213** can be parallel to the (111) crystalline surface. (Alternatively, the upper surface **207** can be parallel to the (111) crystalline plane. The trench surface **213** can be parallel to the (100) crystalline surface.) The trench **210** thus can have the shape of an inverted pyramid or a truncated inverted pyramid in the substrate **205**, which forms a square opening in the upper surface **207**. An internal edge **217** is formed at the intersection of two adjacent trench surfaces **213**. The substrate **205** can have a rectangular or square shape having an outer edge **208**. The light emitting device **200** can be fabricated together with a batch of other light emitting devices on a semiconductor wafer, and diced to form separate dies. The light emitting device **200** can have a rectangular or square die shape defined by a planar area in the plane parallel to the upper surface **207**.

[0050] The light emitting device **200** includes a reflective buffer layer **215** on the upper surface **207** and the trench surfaces **213**, a lower Group III-V compound layer **220** on the reflective buffer layer **215**, one or more quantum-well layers **230** on the lower Group III-V compound layer **220**, and an upper Group III-V compound layer **240**. The lower Group III-V compound layer **220** and the upper Group III-V compound layer **240** each includes a group III element and a group V element. The group III element is typically gallium. The group V element is typically nitride. Group III-V compounds suitable for the lower Group III-V compound layer **220** and the upper Group III-V compound layer **240** can include GaN or InGaAlN. The lower Group III-V compound layer **220** and the upper Group III-V compound layer **240** can be respectively n-type and p-type doped. The portion of the upper Group III-V compound layer **240** over the trench surface **213** is referred to as a sloped upper Group III-V compound layer **240**A and is oriented at an angle relative to the upper surface **207** of the substrate **205**. The light emitting device **200** also includes a lower electrode **270** on the lower Group III-V compound layer **220** and an upper electrode **260** on the upper Group III-V compound layer **240**.

[0051] In some embodiments, as shown in FIG. **4**A, a semiconductor wafer **400** includes a 2×2 array of light emitting structures **400**A-**400**D formed on a substrate **405**. Each of the light emitting structures **400**A-**400**D can have a similar structure as that of the light emitting device **200** as described above. The light emitting structures **400**A-**400**D can be formed in a 2×2 matrix on a semiconductor wafer. The light emitting structures **400**A-**400**D can be used as a single light device, or they can be separated by cutting and dicing to form individual light emitting devices similar to the light emitting device **200**. In another example, a semiconductor wafer **500** comprising a 4×4 array of light emitting structures **510** is shown FIG. **4**C.

[0052] Referring to FIGS. **3**D and **4**B, the light emitting structures **400**A, **400**B can be formed on trenches **410** in a substrate **405**. The substrate **205** can be formed by silicon, silicon oxide, gallium nitride, silicon carbide, sapphire, or glass. The substrate **205** can also be formed by a double-layer structure such as a silicon layer on glass, or simply a silicon-on-insulator (SOI) wafer. The silicon layer can have a (100) upper surface. The thickness of the silicon layer can be used to define the depth of a trench. For a silicon based substrate, the substrate **405** can have an upper surface **405**A in the (100) crystalline plane direction. The surfaces **410**A, **410**B of the trench **410** can be along the (111) crystalline plane direction. The substrate **405** can also include a complimentary metal oxide semiconductor (CMOS) material and a CMOS electric circuitry for driving and controlling the light emitting device **400**.

[0053] A reflective buffer layer **415** is formed on the surface **405**A of the substrate **405** and the sloped surfaces **410**A, **410**B in the trenches **410**. A function of the reflective buffer layer **415** is to reflect light emitted by the light emitting device **400** away from the substrate **405** to prevent the emitted light from being absorbed by the substrate **405**. For example, the substrate **405** can be silicon based, which absorbs light in the visible light range. The reflective buffer layer **415** can have a reflectance coefficient higher than 30%, 50%, or 70% in the spectral range for the emitted light from the light emitting device **400**.

[0054] The reflective buffer layer **415** can be deposited on the substrate **405** using atomic layer deposition (ALD) in a vacuum chamber maintained at a temperature in the range of 550° C. to 850° C., such as about 700° C. The reflective buffer layer **415** can have a thickness of about 200 to 200,000 Angstroms such as 1000 to 10,000 Angstroms. The reflective buffer layer **415** can wet and form a uniform layer on the substrate **405**. The reflective buffer layer **415** can also have crystal structures with lattices epitaxially matched to the substrate **405** and the lower Group III-V compound layer **420** (described below).

[0055] The ALD formation of the reflective buffer layer **415** can involve the use of TaN or TiN and a layer thickness of 10 to 100 angstroms. Atomic layer deposition (ALD) is a "nano" technology, allowing ultra-thin films of a few nanometers to be deposited in a precisely controlled way. ALD has the beneficial characteristics of self-limiting atomic layer-by-layer growth and is highly conformal to the substrate. For the formation of buffer layer in the light emitting devices, ALD can use two or more precursors such as liquid halide or organometallic in vapor form. The ALD can involve heat to dissociate the precursors into the reaction species. One of the precursors can also be a plasma gas. By depositing one layer per cycle, ALD offers extreme precision in ultra-thin film growth since the number of cycles determines the number of atomic layers and therefore the precise thickness of deposited film. Because the ALD process deposits precisely one atomic layer in each cycle, complete control over the deposition process is obtained at the nanometer scale. Moreover, ALD has the advantage of being capable of substantially isotropic depositions. ALD is therefore beneficial for depositing buffer layers on the sloped surfaces **410**A and **410**B in the V-shape trenches, and the vertical surfaces in a U-shape trench.

[0056] A lower Group III-V compound layer **420** is formed on the reflective buffer layer **415**. The lower Group III-V compound layer **420** can be formed by silicon doped n-GaN. The lower Group III-V compound layer **420** can have a thickness in the range of 1 to 50 microns, such as 10 microns.

[0057] The material for the reflective buffer layer **415** is selected to satisfy the requirements of high reflectivity and lattice matching with the substrate **405** and a lower Group III-V compound layer **420**. For example, the reflective buffer layer **415** can be formed by Al, aluminum nitride, Al oxide, Ag, Ag oxide, Au, Au oxide, and their alloys of Al, Au and Ag. The reflective buffer layer **415** can be also formed by one or more materials such as TaN, TiN, GaN, ZnO, AlN, HfN, AlAs, or SiC. The reflective buffer layer **415** can have a thickness in the range of 200 to 200,000 Angstroms, such as 1,000 to 10,000 Angstroms.

[0058] A quantum-well layer **430** is formed on the lower Group III-V compound layer **420**. The quantum-well layer **430** can be made of InN or InGaN with a thickness in the range of 5 to 200 Angstroms, such as 50 Angstroms. An upper Group III-V compound layer **440** is formed on the quantum-well layer **430**. The upper Group III-V compound layer **440** can be formed by p-type doped GaN such as $Al_{0.1}Ga_{0.9}N$. The upper Group III-V compound layer can be an aluminum doped p-GaN layer **440** having a thickness in the range of 0.1 to 10 microns, such as 1 micron. The quantum-well layer **430** forms a quantum well between the lower Group III-V compound layer **420** and the upper Group III-V compound layer **440**. A conductive layer **450** is optionally formed on the upper Group III-V compound layer **440**. The conductive layer **450** is at least partially transparent. Materials suitable for the conductive layer **450** can include ITO or a thin layer p-type ohmic metal such as Ni/Au. An upper electrode **460** can be formed on the conductive layer **450** (or the upper Group III-V compound layer **440** in absence of the conductive layer **450**). The inclusion of the conductive layer **450** can be based on whether the substrate **405** is thinned to all allow more emitted light to exit the light emitting device **400**. The conductive layer **450** is preferably included if the substrate **405** is not thinned so more light can exit the Light emitting device **400**. A lower electrode **470** can then be formed on the lower Group III-V compound layer **420**. The upper electrode **460** and lower electrode **470** can be respectively referred as p-electrode and n-electrode. The use of transparent ITO material in the conductive layer **450** can significantly increase the conductivity between the electrode **460** and the upper Group III-V compound layer **440** while maximizing the transmission light out of the upper surface of the conductive layer **450** emitted from the quantum-well layer **430**.

[0059] The quantum-well layer **430** can form a quantum well for electric carriers in between the lower Group III-V compound layer **420** and the upper Group III-V compound layer **440**. An electric voltage can be applied across the lower electrode **470** and the upper electrode **460** to produce an electric field in the quantum-well layer **430** to excite carriers in the quantum well formed by the quantum-well layer **430**, forming a quantum well for electric carriers in between the lower Group III-V compound layer **420** and the upper Group III-V compound layer **440**. The recombinations of the excited carriers can produce light emission. The emission wavelengths are determined mostly by the bandgap of the material in the quantum-well layer **430**.

[0060] In the present specification, the term "quantum well" refers to a potential well that confines charge carriers or charged particles such as electrons and holes to a substantially two-dimensional planar region. In a semiconductor light emitting device, the quantum well can trap excited electrons and holes and define the wavelength of light emission when the electrons and the holes recombine in the quantum well and produce photons.

[0061] In the present specification, a quantum-well layer can include a uniform layer or a plurality of quantum wells. For example, a quantum-well layer (e.g. **430** in FIGS. **5**E to **5**I) can include a substantially uniform layer made of InN, GaN, InGaN, AlGaN, InAlN, or AlInGaN. A quantum-well layer can also include a multi-layer structure defining one or more quantum wells. A quantum well can for example be formed by an InGaN, an AlGaN, an InAlN, or an InGaAlN layer sandwiched in between two GaN layers. A quantum well can also be formed by an InGaN layer sandwiched in between GaN or AlGaN layers. The quantum-well layer can include one or a stack of such layered structure each defining a quantum well as described above.

[0062] The bandgap for InN is about 1.9 eV, lower than the bandgap for GaN that is at about 3.4 eV. The lower bandgap of the InN or the InGaN layer can define a potential well for trapping charge carriers such as electrons and holes. The trapped electrons and holes can recombine to produce photons (light emission). The bandgap in the InN or the InGaN layer can therefore determine the colors of the light emissions. In other words, the colors of light emissions can be tuned by adjusting the compositions of In and Ga in InGaN. For example, a quantum well can produce red light emission from an InN layer, green light emission from an In(0.5)Ga(0.5)N layer, and blue light emission from an In(0.3)Ga(0.7)N in the quantum-well.

[0063] In one aspect, the disclosed light emitting device can include a substrate having a first surface and a second surface not parallel to the first surface; and a light emission layer disposed over the second surface to emit light, the light emission layer having a light emission surface which is not parallel to the first surface. By stating that one layer is disposed "over" or "above" another layer, this does not necessarily mean that the two layers must be in direct contact with each other; indeed, there may be one or more additional layers in between, as will be further apparent from other portions of

this description. In another aspect, the disclosed light emitting device can include a substrate; and a light emission layer disposed over the substrate to emit light, the light emission layer having a footprint area and having a light emission surface area which is greater than the footprint area. In another aspect, the disclosed light emitting device can include a substrate having a first surface and a protrusion formed on the first surface; and a light emission layer disposed on the protrusion to emit light, the light emission layer having a light emission surface which is not parallel to the first surface.

[0064] FIGS. **3**E and **3**F respectively illustrate other examples of layer structures and material compositions for the light emitting structures, which can include trenches, protrusions such as pyramids, and other structures including a sloped surface not parallel to the upper surface of the substrate. The layers are shown in the horizontal direction only for the purpose of illustration. The sequence, thicknesses, and compositions described the layers on the sloped surfaces in the trenches or on the protrusions as well as the upper surface of the substrate. An Al_2O_3 layer below the buffer layer can provide the reflectivity needed to reflect the light emission away from the substrate. The quantum well layers can be formed by two to ten periods of GaN:Mg and $In_xGa_{1-x}N$ layers. The GaN:Mg layer can for example be about 5 nm thick. The $In_xGa_{1-x}N$ layer can for example be about 2 nm thick. The lower Group III-V compound layer can be made of GaN doped with Mg or Si, and approximately 2 μm in thickness. The upper Group III-V compound layers can be made of GaN doped with Mg or Si, AlGaN doped with Mg or Si, and can be approximately 100 nm in thickness. The upper electrode can be formed by an ITO layer approximately 200 nm in thickness or a bi-layer of respectively made of Ni and Au.

[0065] In some embodiments, more than one reflective buffer layer can be formed on the substrate **405**. A first buffer layer and a second buffer layer are sequentially formed on the substrate **405**. At least the second buffer layer is reflective. The combined reflectance coefficient for the first buffer layer and the second buffer layer are higher than 30%, 50%, or 70% in the spectral range for the emitted light from the light emitting device. A lower Group III-V compound layer is then formed on the second reflective buffer layer. The quantum-well layer, the upper Group III-V compound layer, the conductive layer, the upper electrode, and the lower electrode can then be formed successively to form the light emitting device.

[0066] It should be noted that the light emitting structures in the wafers **400**, **500** can be separated by dicing and cutting to form individual light emitting devices, each of which can be powered to emit light in separate applications. The light emitting structures in the wafers **400**, **500** each can also be used as an integrated light emitting device. The lower electrodes of the light emitting structures in the wafers **400** or **500** can be electrically connected to allow them to be connected to a common external electrode. The upper electrodes of the light emitting structures in the wafers **400** or **500** can be connected to different external electrodes, which allow the light emitting structures in the wafers **400** or **500** to be individually addressed for turning on and off. The upper electrodes of the light emitting structures in the wafers **400** or **500** can also be connected to a common external electrode to allow the light emitting structures in the wafers **400** or **500** to be turned on and off as a group to provide a large-area light emitting device.

[0067] Another advantage of the described light emitting devices is that the disclosed Light emitting devices and fabrication processes can overcome differential thermal expansions and lattice mismatch between the lower Group III-V compound layers and the substrate and prevent associated layer cracking and delamination. It is known that the severity of the lattice mismatch and differential thermal expansions increase as a function of the lateral contact dimensions between the lower Group III-V compound layer and the substrate (or the buffer layer). Conventional LED light devices are often manufactured on 2-inch and 4-inch substrate and can thus suffer from large distress at the contact area between the lower Group III-V compound layer and the substrate (or the buffer layer). The lattice mismatch and differential thermal expansions are much larger for the (100) surface than for the (111) surface for a silicon-based substrate.

[0068] The disclosed light emitting devices breaks down the large (100) surface areas by segmented (111) trench surfaces and the (100) upper surfaces between the trenches. The openings of the trenches (**210** in FIGS. **3**A-**3**C) can be in a range between 100 microns to 100 mm, such as 1 to 20 mm. The width "D" of the (100) upper surface **207** (FIG. **4**B) can be kept narrow, for example, to be less than 1000 microns, which is much shorter than the width of the wafer substrate for fabricating convention LED light emitting devices. Similarly the width "W" of the bottom surface **215** (FIG. **3**C) can be kept narrow, for example, to be less than 200 microns. By keeping these dimensions small, stress related to differential thermal expansions and lattice mismatch can thus be drastically reduced.

[0069] The described light emitting devices can produce significantly higher emission light intensity than conventional LED devices. Referring to FIGS. **6**A and **6**B, a conventional LED light emitting device **600** includes a flat emission surface **610** on a substrate **600**. A light emitting device **650** according to the present application includes a substrate **655** having an upper surface **660** and a trench having sloped emission surfaces **670**. For a silicon based substrate, the upper surface can be along the (100) crystalline plane and the sloped emission surfaces **670**A, **670**B parallel to the (111) crystalline planes. The sloped emission surfaces **670**A, **670**B are at a 54.7° angle relative to the upper surface **660**. For the same foot print on the upper surface **660**, the sum of the areas of the emission surfaces **670**A, **670**B, measured along each of those surfaces, is 1/(cos(54.7°)) of (i.e., approximately 1.73 times) the area of the flat emission surface **610** in the conventional LED device **600**. The disclosed light emitting devices are compatible with other substrate materials and relative orientations of the sloped trench surfaces. It should be understood that the disclosed light emitting devices are compatible with other substrate materials and relative orientations of the sloped trench surfaces. The sloped trench surface can be at an angle between 20 degrees and 80 degrees, or as a more specific example, between 50 degrees and 60 degrees relative to the upper surface of the substrate.

[0070] The emission surfaces in a trench in the disclosed light emitting device can be more than one time, or 1.2, or 1.4, or 1.6 times of the area of the trench openings. The large emission surface areas in the described light emitting devices allow the disclosed light emitting device can thus generate much higher light emission intensity than conventional LED devices. For a light emitting device (e.g. **200** in FIG. **2**A) formed on an individual die, the emission surfaces provided by the sloped trench surfaces in sum can have a larger area than the planar area of the light emitting device (e.g. the footprint area of the light emitting device **200** in FIG. **2**A).

[0071] Another advantage of the described light emitting devices is that they can emit light in more concentrated angular range than conventional LED devices. Referring again to FIGS. **6**A and **6**B, the flat emission surface **610** emits light in a 180 angular range. The angular emission distribution **620** has a 360 degree rotational symmetry relative to the substrate normal direction. The light emitting device **650** includes sloped emission surfaces **670**A and **670**B emit light according to angular distributions **680**A and **680**B respectively, which combine to give an emission angular distribution **680**. The emission angular distribution **680** has a 90 degree rotational symmetry relative to the substrate normal direction and a 70.6° angular width, less than half of the angular range in the angular emission distribution **620** in the conventional LED light emitting device **600**. The emission of the light emitting device **650** is therefore much more concentrated and efficient than conventional LED light emitting devices. The disclosed light emitting devices are compatible with other substrate materials and relative orientations of the sloped trench surfaces. The light emitted from the sloped trench surfaces can be confined in an angular range narrower than 150 degrees, 120 degrees, 100 degrees, or 80 degrees, to provide different degrees of angularly concentrated light emission.

[0072] Referring to FIGS. **5**A-**5**I, and **8**, the fabrication process of the light emitting device **400** (**200**, **300**, or **600**) can include the following steps. It should be noted that the process is described using trenches as an example for the light emitting structure. The process is applicable to other light emitting structures such as protrusions (e.g. pyramids) and other different structures that include sloped surfaces not parallel to their respective upper surfaces of the substrates. A mask layer **401** is formed on the substrate **405** (FIG. **5**A). The substrate **405** has an upper surface **405**A. The openings **402** in the mask layer **401** are intended to define the locations and the openings of the trenches to be formed. One or more trenches **410** are formed in a substrate **405** (step **810**, FIGS. **5**B**1** and **5**B**2**). The trench **410** can be formed by chemically etching of the substrate **405**. Wet etch is isotropic along all directions. For example, an etchant may have a slower etching rate for the (111) silicon crystal plane than in other crystalline plane directions. The etchant (e.g. KOH) can thus create trenches **410** in the substrate **405** wherein the trench surfaces **410**A, **410**B are along the (111) silicon crystal planes. Etching can undercut the silicon underneath the hard mask layer **401** to form the hangover of the (hard) mask layer **401** on top of Si(100) wafer (FIG. **5**B**1**). The hard mask layer **401** is subsequently removed (a shown in FIG. **5**B**2**).

[0073] One or more buffer layers can next be next formed on the substrate **405** using atomic layer deposition (ALD) or MOCVD (step **820**). For example, a first buffer layer **213** (or **210**) is next formed on the substrate **205** using atomic layer deposition (ALD) (step **820**). The substrate **205** can have an upper surface oriented in the (100) crystalline plane. The buffer layer **213** or **210** can be formed of GaN, ZnO, AlN, HfN, AlAs, or SiC. The atomic layer deposition of the buffer material can be implemented using commercial equipment such as IPRINT™ Centura® available from Applied Materials, Inc. The atomic layer deposition can involve the steps of degassing of a vacuum chamber, the application of a precursor material, and deposition of the buffer material monolayer by monolayer. The substrate (or the chamber) temperature can be controlled at approximately 600° C. The layer thickness to form nucleation in an ALD process can be as thin 12 angstrom, much thinner than the approximately thickness of 300 angstrom required by MOCVD for buffer layer formation in some convention LED structure (e.g. the LED structure **100** depicted in FIG. **1**). The step **820** can also be referred as ALD of a low temperature buffer layer.

[0074] A reflective buffer layer is deposited on the substrate **205** using atomic layer deposition (ALD) in a vacuum chamber maintained at a relatively lower temperature in a range of 550° C. to 850° C., such as 6700° C. A second buffer layer can be deposited on the first buffer layer using atomic layer deposition (ALD) in a vacuum chamber maintained at a relatively higher temperature in a range of 850° C. to 1250° C., such as 1,000° C. The reflective buffer layer can be formed of Al, an Al oxide, Ag, an Ag oxide, Au, an Au oxide, and an alloy comprising Al, Ag, or Au. The reflective buffer layer can also include GaN, ZnO, AlN, HfN, AlAs, or SiC. The reflective buffer layer can have a thickness of about 20-300 Angstroms. The crystal structure of the reflective buffer layer can have lattices epitaxially matched to the substrate and the lower Group III-V compound layer to reduce the strain in the lattice structural transition from the substrate to the lower Group III-V compound layer, which can reduce the chance for cracking and delamination in the multi-layer structure.

[0075] For the light emitting device **400**, the reflective buffer layer **415** can be formed by MOCVD, PVD, ALD, or molecular beam epitaxy (MBE) on the surface **405**A of the substrate **405** and the sloped surfaces **410**A, **410**B in the trenches **410**. The reflective buffer layer **415** can be formed by ALD of TaN or TiN materials. In other examples, the formation of the reflective buffer layer **415** can include one of the following procedures: depositions of AlN at 1000° C. and GaN at 1000° C. using MOCVD, deposition of GaN at 700° C. using MOCVD followed by deposition of GaN at 1000° C. using MOCVD, deposition of HfN at 500° C. using PVD followed by deposition of GaN using MBE at 700° C., and deposition of SiCN at 1000° C. using MOCVD followed by deposition of GaN at 1000° C. using MOCVD.

[0076] An advantage for forming the reflective buffer layer **415** on the surfaces **410**A and **410**B in the V-shape trenches **410** is that the (111) crystalline direction of the surfaces **410**A and **410**B can allow better lattice matching between silicon substrate, the reflective buffer layer **415**, and the lower Group III-V compound layer **420**. Better lattice matching can significantly reduce the cracking problems caused by lattice mismatches in some convention light emitting devices.

[0077] A lower Group III-V compound layer **420** is next formed on the reflective buffer layer **415** (step **830**, FIG. **5**D). The lower Group III-V compound layer **420** can be formed by an n-type doped GdN material. GaN can be grown on the reflective buffer layer **415** using MOCVD while silicon is doped. The silicon doping can enhance tensile stresses to make the compression and tensile strengths more balanced. As a result, cracks can be substantially prevented in the formation of the lower Group III-V compound layer **420**.

[0078] A quantum-well layer **430** is next formed on the lower Group III-V compound layer **430** (step **840**, FIG. **5**E). The quantum-well layer **430** can include can include a substantially uniform layer made of InN, GaN, InGaN, AlGaN, InAlN, or AlInGaN. The quantum-well layer **430** can also include a multi-layer structure defining one or more quantum wells. A quantum well can for example be formed by an InGaN, an AlGaN, an InAlN, or an InGaAlN layer sandwiched in between two GaN layers or AlGaN layers. The quantum-well layer **430** can include one or a stack of such layered structure each defining a quantum well.

[0079] An upper Group III-V compound layer **440** is formed on the quantum-well layer **430** (step **850**, FIG. **5**F). Instead of having the lower Group III-V compound layer **420** n-type doped and the upper Group III-V compound layer **440** p-type doped, the lower Group III-V compound layer **420** can be p-type doped and the upper Group III-V compound layer **440** can be n-type doped (as shown in the flow chart of FIG. **9**).

[0080] A transparent conductive layer **450** can next be optionally formed on the upper Group III-V compound layer **440** (step **860**, FIG. **5**G). The formation of the quantum-well layer can include multiple MOCVD steps. For example, each of the multiple steps can include the deposition of a layer 50 Angstroms in thickness.

[0081] The quantum-well layer **430**, the upper Group III-V compound layer **440**, and the conductive layer **450** can also be formed by MOCVD. The MOCVD formations of the lower Group III-V compound layer **420**, the quantum-well layer **430**, the upper Group III-V compound layer **440**, and the conductive layer **450** and the ALD formation of the buffer layers **415** can be formed in a same ALD/CVD chamber system to minimize the number times the substrate's moving in and out of vacuum chambers. The process throughput can be further improved. Impurities during handling an also be reduced.

[0082] The quantum-well layer **430**, the upper Group III-V compound layer **440**, and the conductive layer **450** can next be coated by a photo resist and patterned by photolithography. Portions of the quantum-well layer **430**, the upper Group III-V compound layer **440**, and the conductive layer **450** can then be removed by wet etching to expose a portion of the upper surface of the lower Group III-V compound layer **420** (step **870**, FIG. **5**H).

[0083] The upper electrode **460** is next formed on the conductive layer **450** (step **880**, FIG. **5**H). The upper electrode **460** can include Ni/Au bi-layers that have thicknesses of 12 nm and 100 nm respectively. The fabrication of the upper electrode **460** can involve the coating a photo resist layer on the conductive layer **450** and the exposed upper surface of the lower Group III-V compound layer **420**. The photo resist layer is then patterned using photolithography and selectively removed to form a mask. Electrode materials are next successively deposited in the openings in the mask. The unwanted electrode materials and the photo resist layer are subsequently removed.

[0084] The lower electrode **470** is next formed on the lower Group III-V compound layer **420** (FIG. **5**H). The lower electrode **470** can include AuSb/Au bi-layers. The AuSb layer is 18 nm in thickness whereas the Au layer is 100 nm in thickness. The formation of the lower electrode **470** can also be achieved by forming photo resist mask having openings on the lower Group III-V compound layer **420**, the depositions of the electrode materials and subsequent removal of the unwanted electrode materials and the photo resist layer. The light emitting device **400** is finally formed.

[0085] Optionally, referring to FIG. **5**I, a protection layer **480** can be introduced over the light emitting device **400** for protecting it from moisture, oxygen, and other harmful substance in the environment. The protection layer **480** can be made of a dielectric material such as silicon oxide, silicon nitride, or epoxy. The protection layer can be patterned to expose the upper electrode **460** and the lower electrode **470** to allow them to receive external electric voltages. In some embodiments, the protection layer can also include thermally conductive materials such as Al and Cu to provide proper cooling the light emitting device **400**.

[0086] It should be noted that the lower Group III-V compound layer and the upper Group III-V compound layer can have different doping arrangement as long as their doping content are opposite to each other. The lower Group III-V compound layer can be p-type doped and the upper Group III-V compound layer n-type doped. Alternatively, the lower Group III-V compound layer can be n-type doped and the upper Group III-V compound layer p-type doped.

[0087] FIG. **7** is a perspective view of another light emitting device **700** in accordance with the present application. Instead of a square opening in the mask layer (FIG. **5**A and step **800** below), a rectangle opening is formed in the mask layer **410** to produce an elongated trench after etching. A rectangular opening is sometimes preferred for the long aspect ratio of the trench opening. For example, some light devices require elongated light emission surface(s). For a silicon-based substrate, the upper surface can be parallel to the (100) crystalline plane. The sloped trench surfaces are parallel to the (111) crystalline plane similar to the previous descriptions. The long sloped trench surface can be at least 50% larger in area than the sloped first trench surfaces at the ends of the elongated trench.

[0088] The disclosed light emitting devices and fabrication processes can include one or more of the following advantages. The disclosed light emitting devices and fabrication processes can overcome associated with can overcome latter mismatch between the lower Group III-V compound layer and the substrate and prevent associated layer cracking in conventional light emitting devices. The disclosed light emitting devices and fabrication processes can also prevent cracking or delamination in the p-doped or n-doped Group III-V compound layer caused by different thermal expansions between the p-doped Group III-V compound layer and the substrate. An advantage associated with the disclosed light emitting devices is that light emitting devices can significantly increase light emission efficiency by increasing densities of the light emitting devices and by additional light emissions from the sloped or vertical surfaces in the trenches.

[0089] The light emission layers in the disclosed light emitting devices can be formed on types of structures other than trenches as described above. Referring to FIGS. **9**A to **10**C, for example, a light emitting device **900** is formed on a substrate **905** having an upper surface **907**. The light emitting device **900** includes a protrusion **910** on the upper surface **907**. The protrusion **910** has one or more protrusion surfaces **913** (FIGS. **10**A-**10**C) at a slope relative to the upper surface **907**. The protrusion **910** can also have a top surface **919** that is substantially parallel to the upper surface **907**. The area of the top surface **919** can be kept smaller than 20% of one of the protrusion surfaces **913**. The protrusion **910** can have the shape of a pyramid or a truncated pyramid above the upper surface **907**.

[0090] The substrate **905** can be silicon based: the upper surface **907** can be parallel to the (100) crystalline plane. The protrusion surface **913** can be parallel to the (111) crystalline surface. (Alternatively, the upper surface **907** can be parallel to the (111) crystalline plane. The protrusion surface **913** can be parallel to the (100) crystalline surface.) The substrate **905** can also include a multi-layer silicon-on-insulator (SOI) structure.

[0091] An edge **917** is formed at the intersection of two adjacent protrusion surfaces **913**. The substrate **905** can have

a rectangular or square shape having an outer edge **908**. The light emitting device **900** can be fabricated together with a batch of other light emitting devices on a semiconductor wafer, and diced to form separate dies. The light emitting device **900** can have a rectangular or square die shape defined by a planar area in the plane parallel to the upper surface **907**.

[0092] The light emitting device **900** includes a reflective buffer layer **915** on the upper surface **907** and the protrusion surfaces **913**, a lower Group III-V compound layer **920** on the reflective buffer layer **915**, one or more quantum-well layers **930** on the lower Group III-V compound layer **920**, and an upper Group III-V compound layer **940**. The portion of the upper Group III-V compound layer **940** over the protrusion surface **913** is oriented at an angle relative to the upper surface **907** of the substrate **905**. The light emitting device **900** also includes a lower electrode **970** on the lower Group III-V compound layer **920** and an upper electrode **960** on the upper Group III-V compound layer **940**.

[0093] In some embodiments, as shown in FIGS. **11**A, **11**B, a semiconductor wafer **1000** includes a 2×2 array of light emitting structures **1000**A-**1000**D formed on a substrate **905**. Each of the light emitting structures **1000**A-**1000**D can have a similar structure as that of the light emitting device **900** as described above. The light emitting structures **1000**A-**1000**D can be formed in a 2×2 matrix on a semiconductor wafer. The light emitting structures **1000**A-**1000**D can be used as a single light device, or they can be separated by cutting and dicing to form individual light emitting devices similar to the light emitting device **200**. In another example, as shown FIG. **11**C, a semiconductor wafer **1100** can include a 4×4 array of light emitting structures **1110**.

[0094] As described above, the substrate **905** can be silicon based. The upper surface **907** can be parallel to the (100) crystalline plane. The protrusion surface **913** can be parallel to the (111) crystalline surface. The width "D**1**" of the (100) upper surface **207** (FIG. **11**B) can be kept narrow, for example, to be less than 1000 microns, which is much shorter than the width of the wafer substrate for fabricating convention LED light emitting devices. By keeping this dimension small, stress related to differential thermal expansions and lattice mismatch can thus be drastically reduced.

[0095] The light emitting devices shown in FIGS. **9**A-**11**C can produce different angular distribution from conventional LED devices. Referring to FIG. **12**, a light emitting device **900** includes a protrusion **910** formed on the substrate **905**. Light emitting layers having light emission surfaces **1270**A and **1270**B are formed on the sloped surfaces of the protrusion **910**. For a silicon based substrate, the upper surface **907** can be along the (100) crystalline plane and the sloped light emission surfaces **1270**A, **1270**B parallel to the (111) crystalline planes. The light emission surfaces **1270**A, **1270**B are at a 54.7° angle relative to the upper surface **907**. For the same foot print on the upper surface, the sum of the areas of the emission surfaces on the light emission surfaces **1270**A, **1270**B is approximately 1.73 times the area of the flat emission surface **610** in the conventional LED device **600** (FIG. **6**A). The disclosed light emitting devices are compatible with other substrate materials and relative orientations of the sloped protrusion surfaces. The sloped protrusion surface can be at an angle between 20 degrees and 80 degrees, or as a more specific example, between 50 degrees and 60 degrees relative to the upper surface of the substrate.

[0096] The emission surfaces on a protrusion in the disclosed light emitting device can be more than one time, or 1.2, or 1.4, or 1.6 times of the base area of the protrusion. The large emission surface areas in the described light emitting devices allow the disclosed light emitting device can thus generate much higher light emission intensity than conventional LED devices. The light emission from the light emission surfaces **1270**A, **1270**B can assume a broad distribution **1280** as shown in FIG. **12**.

[0097] Embodiments may include one or more of the following advantages. The disclosed light emitting device and related fabrication processes can provide light emitting devices at higher manufacturing throughput and thus manufacturing cost compared to the conventional light emitting devices. The disclosed light emitting device and related fabrication processes can also provide more-integrated light emitting devices that can include, for example, a light emitting element, a driver, power supply, and light modulation unit integrated on a single semiconductor substrate.

[0098] The foregoing descriptions and drawings should be considered as illustrative only of the principles of the invention. The invention may be configured in a variety of shapes and sizes and is not limited by the dimensions of the preferred embodiment. Numerous applications of the present invention will readily occur to those skilled in the art. Therefore, it is not desired to limit the invention to the specific examples disclosed or the exact construction and operation shown and described. Rather, all suitable modifications and equivalents may be resorted to, falling within the scope of the invention. For example, the n-doped and the p-doped Group III-V compound layers can be switched in position, that is, the p-doped Group III-V compound layer can be positioned underneath the quantum-well layer and n-doped Group III-V compound layer can be positioned on the quantum-well layer. The disclosed light emitting device may be suitable for emitting green, blue, and emissions of other colored lights.

[0099] It should be noted that the disclosed systems and methods are compatible with a wide range of applications such as laser diodes, blue/UV LEDs, Hall-effect sensors, switches, UV detectors, micro electrical mechanical systems (MEMS), and RF power transistors. The disclosed devices may include additional components for various applications. For example, a laser diode based on the disclosed device can include reflective surfaces or mirror surfaces for producing lasing light. For lighting applications, the disclosed system may include additional reflectors and diffusers.

[0100] It should also be understood that the presently disclosed light emitting devices are not limited to the trenches and protrusions described above. A substrate can include a first surface having a first orientation and a second surface having a second orientation. The first and the second surfaces may or may not form a trench or a protrusion. A plurality of Group III-V compound layers can be formed on the substrate. The Group III-V compound layers can emit light when an electric current is produced in the Group III-V compound layers.

What is claimed is:

1. A light emitting device comprising:

a substrate having a first surface and a second surface; and

a light emission layer disposed over the second surface to emit light, the light emission layer having a light emission surface which is not parallel to the first surface.

2. The light emitting device of claim **1**, wherein the substrate comprises a (100) crystal plane and a (111) crystal plane, wherein the first surface is substantially parallel to the

(100) crystal plane of the substrate, and wherein the light emission layer is substantially parallel to the (111) crystal plane of the substrate.

3. The light emitting device of claim **1**, wherein the light emission layer comprises a quantum-well layer that is configured to emit light when an electric current is produced in the quantum-well layer.

4. The light emitting device of claim **3**, wherein the quantum-well layer comprises a layer formed by a material selected from the group consisting of InN, InGaN, GaN, InAlN, AlInGaN, and AlGaN.

5. The light emitting device of claim **1**, further comprising a buffer layer between the substrate and the light emission layer.

6. The light emitting device of claim **5**, wherein the buffer layer has a reflectance coefficient higher than 30% in the spectral range of the light emitted by the light emission layer.

7. The light emitting device of claim **6**, wherein the buffer layer has a reflectance coefficient higher than 50% in the spectral range of the light emitted by the light emission layer.

8. The light emitting device of claim **5**, wherein the buffer layer has a thickness in the range of 200 to 200,000 Angstroms.

9. The light emitting device of claim **5**, wherein the buffer layer comprises Al, an Al oxide, an Al nitride, Ag, an Ag oxide, an Ag nitride, Au, an Au oxide, an Au nitride, and an alloy comprising Al, Ag, or Au.

10. The light emitting device of claim **5**, wherein the buffer layer comprises a material selected from the group consisting of GaN, ZnO, AlN, HfN, AlAs, SiCN, TaN, and SiC.

11. The light emitting device of claim **1**, further comprising:

a lower nitride layer between the substrate and the light emission layer; and

an upper nitride layer over the light emission layer.

12. The light emitting device of claim **1**, wherein the substrate has a trench formed in the first surface, and wherein the light emission layer is disposed within the trench.

13. The light emitting device of claim **12**, wherein the first surface outside of the trench comprises at least one width dimension narrower than 1000 microns.

14. The light emitting device of claim **1**, wherein the substrate has a protrusion formed on the first surface, and wherein the light emission layer is disposed on the protrusion.

15. The light emitting device of claim **13**, wherein the first surface outside of the protrusion comprises at least one width dimension narrower than 1000 microns.

16. The light emitting device of claim **1**, wherein the substrate comprises silicon, gallium nitride, silicon carbide, silicon oxide, or sapphire.

17. The light emitting device of claim **16**, wherein the substrate comprises a silicon-on-insulator (SOI) structure or a bi-layer structure having a silicon layer on a glass substrate.

18. A light emitting device, comprising:

a substrate; and

a light emission layer disposed over the substrate to emit light, the light emission layer having a footprint area and having a light emission surface area which is greater than the footprint area.

19. The light emitting device of claim **18**, wherein the substrate comprises a trench defined in the first surface, and wherein the light emission layer is disposed within the trench.

20. The light emitting device of claim **19**, wherein the first surface outside of the trench comprises at least one width dimension narrower than 1000 microns.

21. The light emitting device of claim **18**, wherein the substrate has a protrusion formed on the first surface, and wherein the light emission layer is disposed on the protrusion.

22. The light emitting device of claim **21**, wherein the first surface outside of the protrusion comprises at least one width dimension narrower than 1000 microns.

23. The light emitting device of claim **18**, wherein the substrate comprises a (100) crystal plane and a (111) crystal plane, wherein the substrate has an upper surface substantially parallel to the 100) crystal plane, and wherein the light emission layer is substantially parallel to the (111) crystal plane of the substrate.

24. The light emitting device of claim **18**, wherein the light emission layer comprises a quantum-well layer that is configured to emit light when an electric current is produced in the quantum-well layer.

25. The light emitting device of claim **24**, wherein the quantum-well layer comprises a layer formed by a material selected from the group consisting of InN, InGaN, GaN, InAlN, AlInGaN, and AlGaN.

26. The light emitting device of claim **18**, further comprising a buffer layer between the substrate and the light emission layer.

27. The light emitting device of claim **18**, wherein the buffer layer has a reflectance coefficient higher than 30% in the spectral range of the light emitted by the light emission layer.

28. The light emitting device of claim **27**, wherein the buffer layer has a reflectance coefficient higher than 50% in the spectral range of the light emitted by the light emission layer.

29. The light emitting device of claim **18**, wherein the buffer layer has a thickness in the range of 200 to 200,000 Angstroms.

30. The light emitting device of claim **18**, wherein the buffer layer comprises Al, an Al oxide, an Al nitride, Ag, an Ag oxide, an Ag nitride, Au, an Au oxide, an Au nitride, and an alloy comprising Al, Ag, or Au.

31. The light emitting device of claim **18**, wherein the buffer layer comprises a material selected from the group consisting of GaN, ZnO, AlN, HfN, AlAs, SiCN, TaN, and SiC.

32. The light emitting device of claim **18**, wherein the substrate comprises silicon, gallium nitride, silicon carbide, silicon oxide, or sapphire.

33. The light emitting device of claim **30**, wherein the substrate comprises a silicon-on-insulator (SOI) structure or a bi-layer structure having a silicon layer on a glass substrate.

34. A light emitting device comprising:

a substrate having a first surface;

a light emission layer disposed over at least a portion of the substrate, the light emission layer having a light emission surface that is not parallel to the first surface; and

a reflective buffer layer disposed under at least a portion of the light emission layer, to reflect light emitted from the light emission layer, and wherein the reflective buffer layer has a reflectance coefficient higher than 30% in a spectral range of light emitted by the light emission layer.

35. The light emitting device of claim **34**, wherein the reflective buffer layer has a thickness in the range of 200 to 200,000 Angstroms.

36. The light emitting device of claim **34**, wherein the reflective buffer layer comprises Al, an Al oxide, an Al nitride, Ag, an Ag oxide, an Ag nitride, Au, an Au oxide, an Au nitride, and an alloy comprising Al, Ag, or Au.

37. The light emitting device of claim **34**, wherein the reflective buffer layer comprises a material selected from the group consisting of GaN, ZnO, AlN, HfN, AlAs, SiCN, TaN, and SiC.

38. The light emitting device of claim **34**, wherein the reflective buffer layer has a reflectance coefficient higher than 50% in the spectral range of the light emitted by light emission layer.

39. The light emitting device of claim **38**, wherein the reflective buffer layer has a reflectance coefficient higher than 70% in the spectral range of the light emitted by the light emission layer.

40. The light emitting device of claim **34**, wherein the substrate has a (100) crystal plane and a (111) crystal plane, wherein the first surface is substantially parallel to the (100) crystal plane, and wherein the light emission surface is substantially parallel to the (111) crystal plane.

41. The light emitting device of claim **34**, wherein the substrate has a (100) crystal plane and a (111) crystal plane, wherein the first surface is substantially parallel to the (111) crystal plane, and wherein the light emission surface is substantially parallel to the (100) crystal plane.

42. The light emitting device of claim **34**, wherein the substrate comprises a trench defined in the first surface, and wherein the light emission layer is disposed within the trench.

43. The light emitting device of claim **42**, wherein the first surface outside of the trench comprises at least one width dimension narrower than 1000 microns.

44. The light emitting device of claim **34**, wherein the substrate has a protrusion formed on the first surface, and wherein the light emission layer is disposed on the protrusion.

45. The light emitting device of claim **44**, wherein the first surface outside of the protrusion comprises at least one width dimension narrower than 1000 microns.

46. The light emitting device of claim **34**, wherein the light emission layer comprises a quantum-well layer that is configured to emit light when an electric current is produced in the quantum-well layer.

47. The light emitting device of claim **46**, wherein the quantum-well layer comprises a layer formed by a material selected from the group consisting of InN, InGaN, GaN, InAlN, AlInGaN, and AlGaN.

48. The light emitting device of claim **34**, wherein the light emission surface is at an angle between 10 degrees and 90 degrees relative to the first surface.

49. The light emitting device of claim **48**, wherein the light emission surface is at an angle between 30 degrees and 60 degrees relative to the first surface.

50. The light emitting device of claim **34**, wherein the substrate comprises silicon, gallium nitride, silicon carbide, silicon oxide, or sapphire.

51. The light emitting device of claim **50**, wherein the substrate comprises a silicon-on-insulator (SOI) structure or a bi-layer structure having a silicon layer on a glass substrate.

52. A light emitting device, comprising:

a substrate having a first surface and a trench formed in the first surface; and

a light emission layer disposed within the trench to emit light, the light emission layer having a light emission surface which is not parallel to the first surface, wherein the first surface outside of the trench comprises at least one width dimension narrower than 1000 microns.

53. The light emitting device of claim **52**, wherein the trench is defined in part by a first trench surface that is not parallel to the first surface.

54. The light emitting device of claim **53**, wherein the substrate has a (100) crystal plane and a (111) crystal plane, wherein the first surface is substantially parallel to the (100) crystal plane, and wherein the first trench surface is substantially parallel to the (111) crystal plane.

55. The light emitting device of claim **53**, wherein the substrate has a (100) crystal plane and a (111) crystal plane, wherein the first surface is substantially parallel to the (111) crystal plane of the substrate, and wherein the first trench surface is substantially parallel to the (100) crystal plane of the substrate.

56. The light emitting device of claim **53**, wherein the second surface is at an angle between 10 degrees and 90 degrees relative to the first surface.

57. The light emitting device of claim **53**, wherein the substrate comprises a silicon-on-insulator (SOI) structure or a bi-layer structure having a silicon layer on a glass substrate.

58. The light emitting device of claim **53**, wherein the trench comprises a second trench surface at a bottom of the trench, the second trench surface being substantially parallel to the first surface.

59. The light emitting device of claim **58**, wherein the area ratio of the second trench surface to the first trench surface is smaller than 50%.

60. The light emitting device of claim **53**, wherein the substrate has a (111) crystal plane, and wherein the trench is defined at least in part by four first trench surfaces substantially parallel to the (111) crystal plane.

61. The light emitting device of claim **53**, wherein the trench has the shape of an inverted pyramid or a truncated inverted pyramid.

62. The light emitting device of claim **53**, wherein the trench has an opening in the first surface of the substrate, wherein the opening has a width in the range of 100 microns to 100 mm.

63. The light emitting device of claim **53**, wherein the trench has an opening in the first surface of the substrate, and wherein the opening has a substantially rectangular shape.

64. The light emitting device of claim **53**, wherein the light emission layer comprises a quantum-well layer configured to emit light when an electric current is produced in the quantum-well layer.

65. The light emitting device of claim **52**, further comprising a buffer layer between the substrate and the light emission layer.

66. The light emitting device of claim **52**, wherein the substrate comprises silicon, gallium nitride, silicon carbide, silicon oxide, or sapphire.

67. A light emitting device, comprising:

a substrate having a first surface and a protrusion formed on the first surface; and

a light emission layer disposed on the protrusion to emit light, the light emission layer having a light emission surface which is not parallel to the first surface.

68. The light emitting device of claim **67**, wherein the first surface outside of the protrusion comprises at least one width dimension narrower than 1000 microns.

69. The light emitting device of claim **67**, wherein the protrusion is defined in part by a first protrusion surface that is not parallel to the first surface.

70. The light emitting device of claim **67**, wherein the substrate has a (100) crystal plane and a (111) crystal plane, wherein the first surface is substantially parallel to the (100) crystal plane, and wherein the first protrusion surface is substantially parallel to the (111) crystal plane.

71. The light emitting device of claim **67**, wherein the substrate has a (100) crystal plane and a (111) crystal plane, wherein the first surface is substantially parallel to the (111) crystal plane of the substrate, and wherein the first protrusion surface is substantially parallel to the (100) crystal plane of the substrate.

72. The light emitting device of claim **67**, wherein the second surface is at an angle between 10 degrees and 90 degrees relative to the first surface.

73. The light emitting device of claim **72**, wherein the first protrusion surface is at an angle between 50 degrees and 60 degrees relative to the first surface of the substrate.

74. The light emitting device of claim **67**, wherein the substrate comprises silicon, gallium nitride, silicon carbide, silicon oxide, or sapphire.

75. The light emitting device of claim **74**, wherein the substrate comprises a silicon-on-insulator (SOI) structure or a bi-layer structure having a silicon layer on a glass substrate.

76. The light emitting device of claim **67**, wherein the protrusion has the shape of a pyramid or a truncated pyramid.

77. A light emitting device, comprising:

a substrate having a first surface;

a trench formed in the substrate, wherein the trench is defined in part by a plurality of first trench surfaces that are not parallel to the first surface;

a reflective buffer layer on at least a portion of the first surface and the plurality of first trench surfaces; and

a light emitting layer over the reflective buffer layer, wherein the light emitting layer is configured to emit light away from the reflective buffer layer, wherein the light emitted is confined in a solid angle smaller than 180 degrees.

78. The light emitting device of claim **77**, wherein the light emitted is confined in an angular range narrower than 160 degrees solid angles.

79. The light emitting device of claim **78**, wherein the light emitted is confined in an angular range narrower than 120 degrees solid angles.

80. The light emitting device of claim **79**, wherein the light emitted is confined in an angular range narrower than 100 degrees solid angles.

81. The light emitting device of claim **77**, wherein the substrate has a (100) crystal plane and a (111) crystal plane, wherein the first surface is substantially parallel to the (100) crystal plane, and wherein the first trench surface is substantially parallel to the (111) crystal plane.

82. The light emitting device of claim **81**, wherein the first surface outside the trench comprises at least one width narrower than 1000 microns.

83. The light emitting device of claim **77**, wherein the first trench surface is at an angle between 10 degrees and 90 degrees relative to the first surface of the substrate.

84. The light emitting device of claim **77**, wherein the trench has an opening in the first surface of the substrate, wherein the opening has a width in the range of 100 microns to 100 mm.

85. The light emitting device of claim **77**, wherein the trench has an opening in the first surface of the substrate, and wherein the opening has a substantially rectangular shape.

86. The light emitting device of claim **77**, wherein the substrate comprises silicon, gallium nitride, silicon carbide, silicon oxide, or sapphire.

87. A method for fabricating a light emitting device, comprising:

forming a light emission layer over a substrate having a first surface and a second surface not parallel to the first surface, wherein the light emission layer has a light emission surface not parallel to the first surface, wherein the light emission layer is configured to emit light.

88. The method of claim **87**, further comprising forming a trench in the first surface, wherein the trench is defined in part by a second surface.

89. The method of claim **87**, further comprising forming a protrusion on the first surface, wherein the protrusion is defined in part by a second surface.

90. The method of claim **89**, wherein the substrate comprises a silicon-on-insulator (SOI) structure or a bi-layer structure having a silicon layer on a glass substrate.

91. The method of claim **87**, further comprising forming a buffer layer on at least a portion of the second surface before the step of forming a light emission layer.

92. The method of claim **91**, wherein the buffer layer is formed by atomic layer deposition (ALD), Metal Organic Chemical Vapor Deposition (MOCVD), Plasma Enhanced Chemical Vapor Deposition (PECVD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), or Physical vapor deposition (PVD).

93. The method of claim **91**, wherein the buffer layer is deposited on the substrate at a temperature in a range of 550° C. to 850° C. or in a range of 850° C. to 1250° C.

94. The method of claim **91**, wherein the buffer layer comprises a material selected from the group consisting of GaN, ZnO, AlN, HfN, AlAs, SiCN, TaN, and SiC.

95. The method of claim **91**, wherein the buffer layer has a reflectance coefficient higher than 30% in the spectral range of the light emitted by the light emission layer.

96. The method of claim **91**, wherein the buffer layer comprises Al, an Al oxide, an Al nitride, Ag, an Ag oxide, an Ag nitride, Au, an Au oxide, an Au nitride, and an alloy comprising Al, Ag, or Au.

97. The method of claim **91**, further comprising:

forming a lower nitride layer on the buffer layer before the step of forming a light emission layer; and

forming an upper nitride layer on the light emission layer.

98. The method of claim **97**, further comprising:

forming a lower electrode on the lower nitride layer; and

forming an upper electrode on the tin oxide layer.

99. The method of claim **87**, wherein the light emission layer comprises one or more quantum-well layers configured to emit light when an electric current is produced in the quantum-well layer.

100. The method of claim **99**, wherein the quantum-well layer comprises a layer formed by a material selected from the group consisting of InN, InGaN, GaN, InAlN, AlInGaN, and AlGaN.

101. The method of claim **87**, wherein the substrate has a (100) crystal plane and a (111) crystal plane, wherein the first surface is substantially parallel to the (100) crystal plane, and wherein the first trench surface is substantially parallel to the (111) crystal plane.

102. The method of claim **87**, wherein the second surface is at an angle between 10 degrees and 90 degrees relative to the first surface.

103. The method of claim **87**, wherein the substrate comprises a glass substrate, silicon-on-insulator (SOI), and a silicon layer on the glass substrate.

104. The method of claim **87**, wherein the substrate comprises silicon, gallium nitride, silicon carbide, silicon oxide, or sapphire.

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