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(54) **GERMANIUM-SILICON-CARBIDE FLOATING GATES IN MEMORIES**

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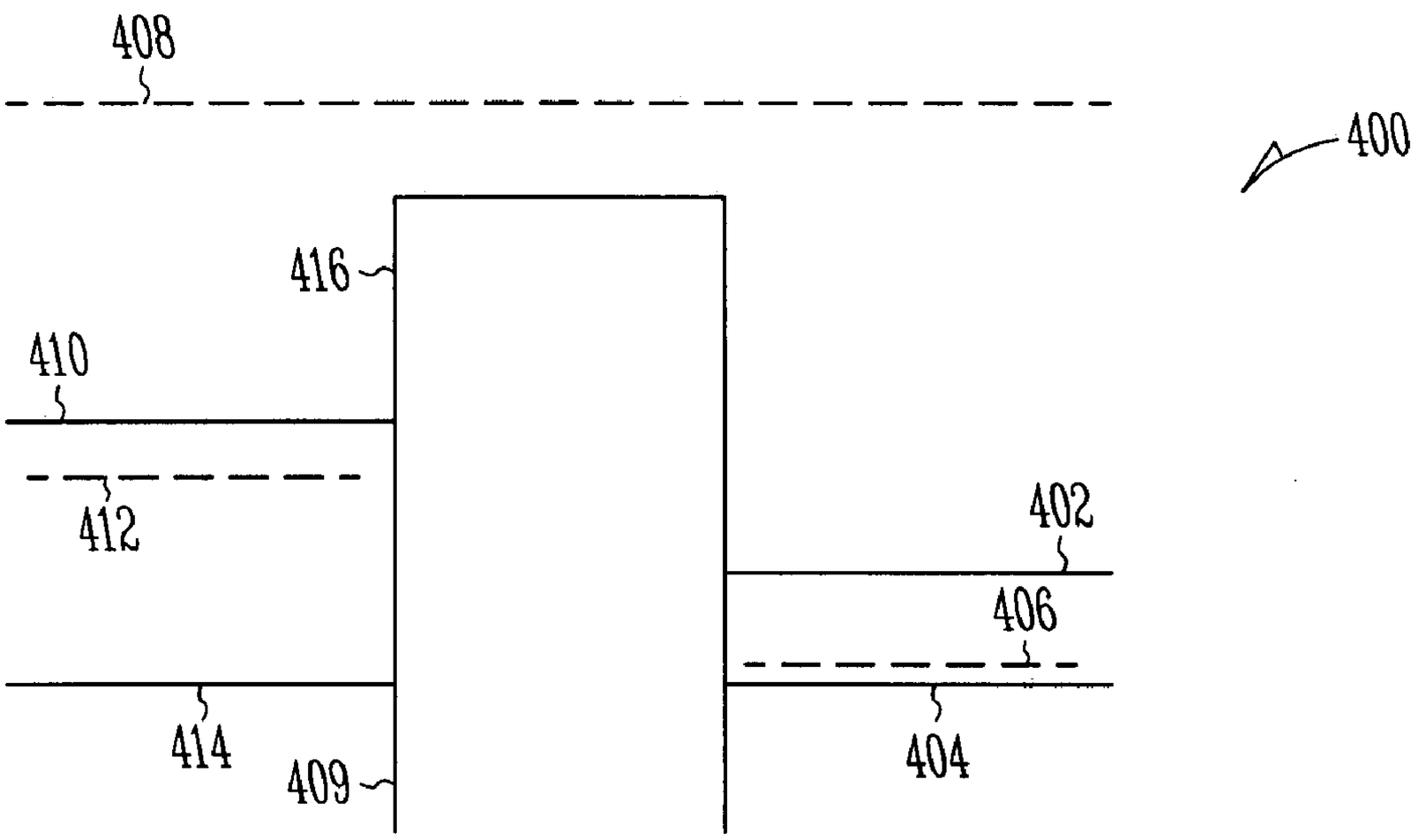
(57) **ABSTRACT**

The use of a germanium carbide (GeC), or a germanium silicon carbide (GeSiC) layer as a floating gate material to replace heavily doped polysilicon (poly) in fabricating floating gates in EEPROM and flash memory results in increased tunneling currents and faster erase operations. Forming the floating gate includes depositing germanium-silicon-carbide in various combinations to obtain the desired tunneling current values at the operating voltage of the memory device.



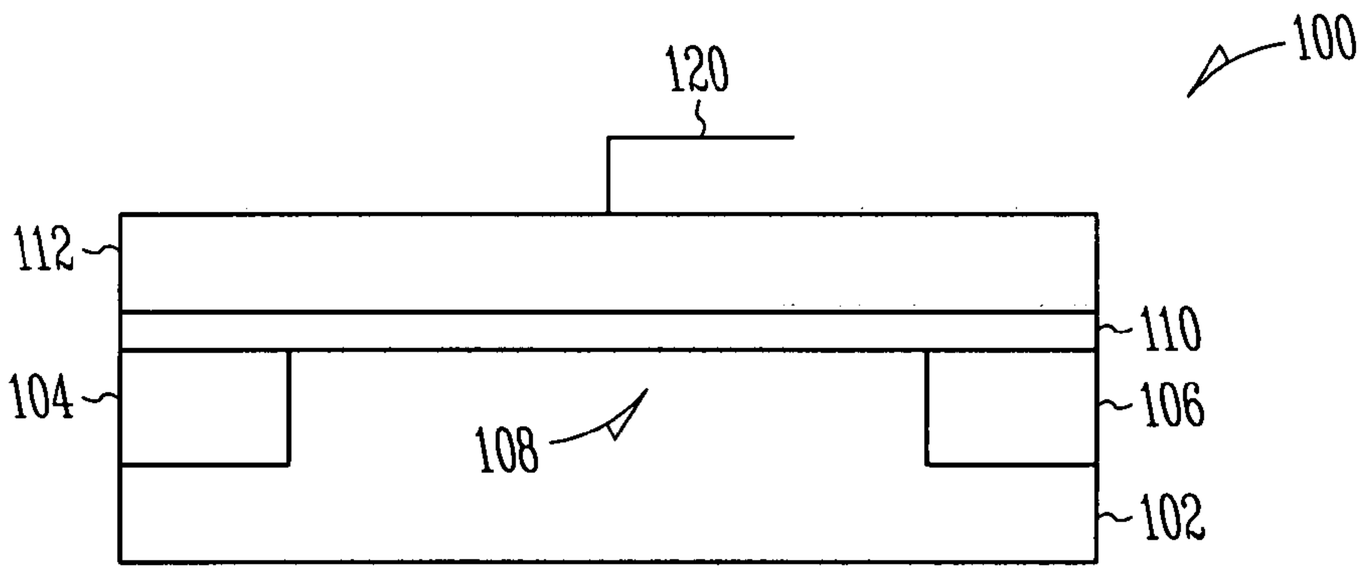

100
120
112
110
104
106
108
102

Fig. 1

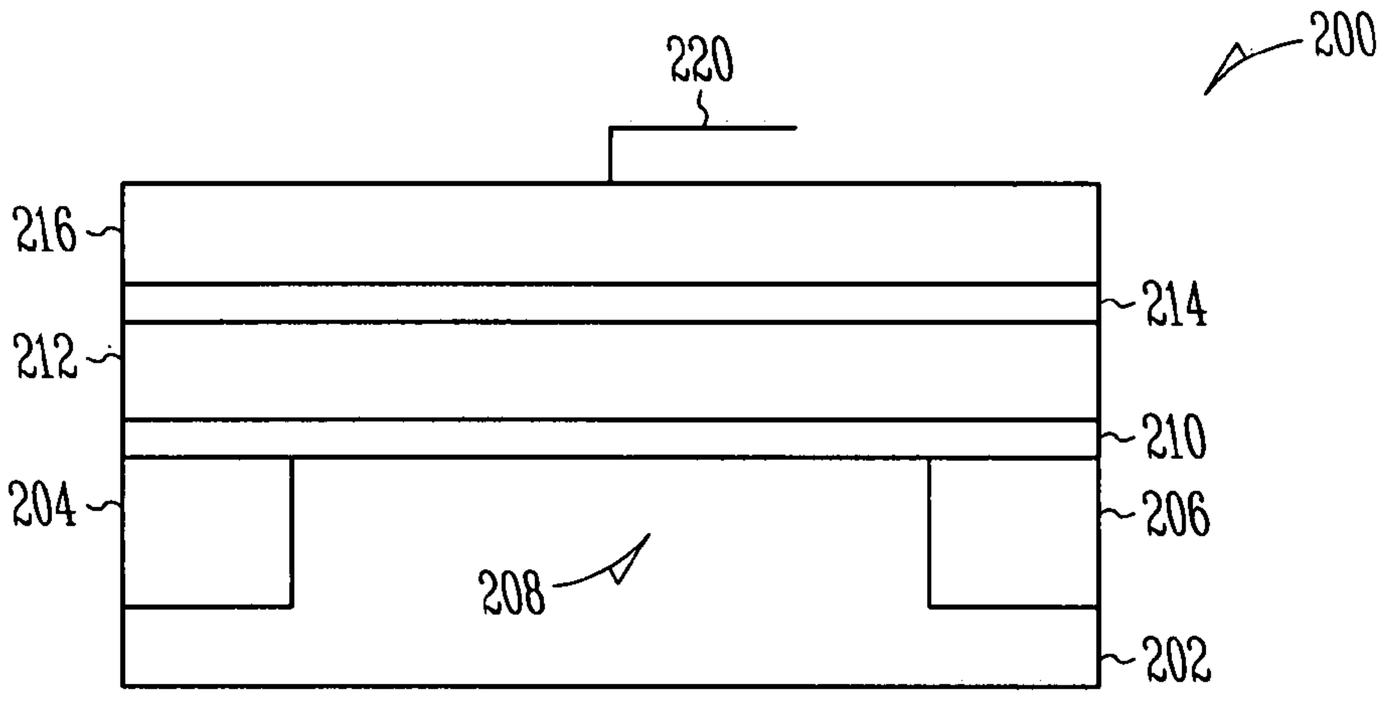

200
220
216
214
212
210
204
206
208
202

Fig. 2

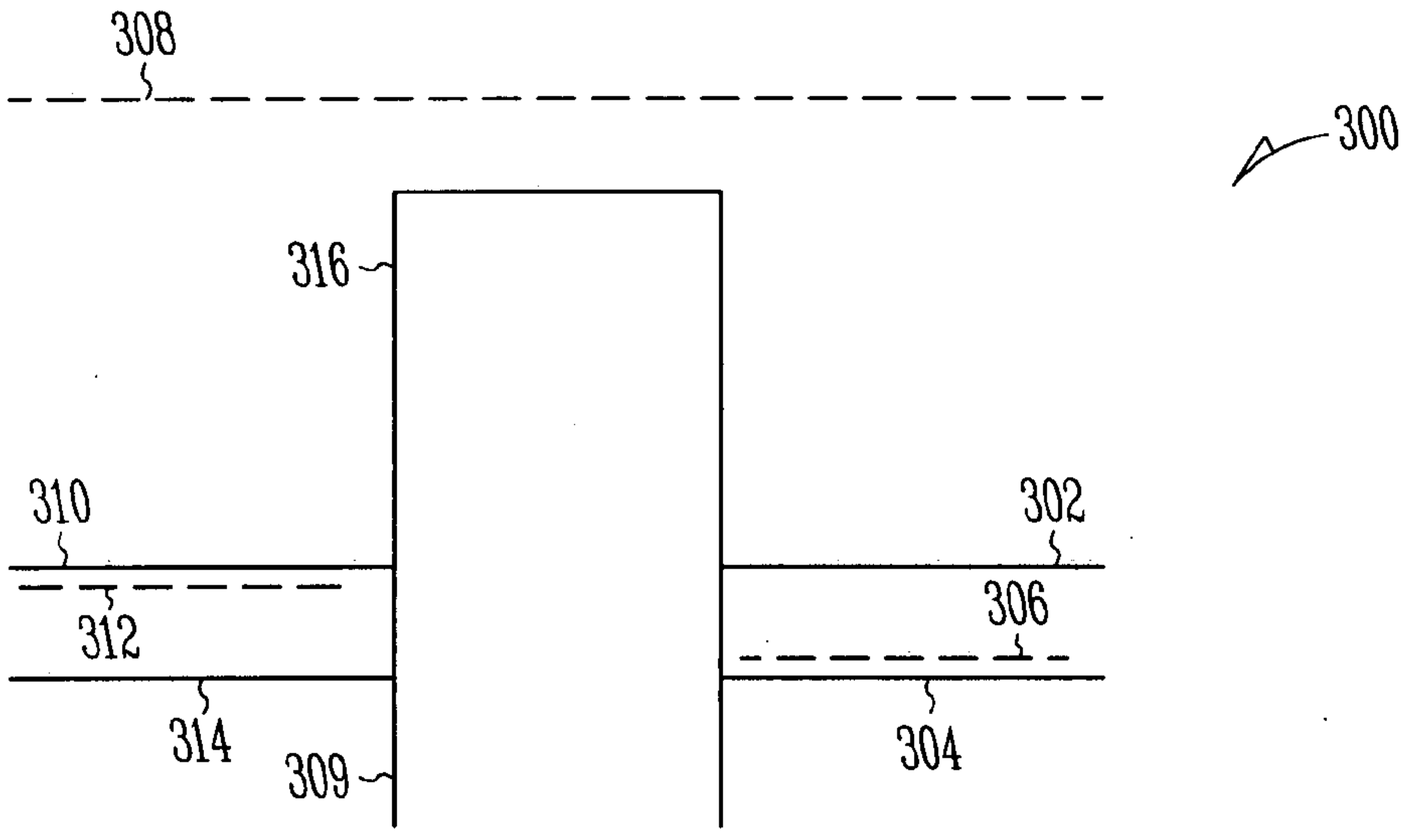

308
300
316
310
302
312
306
314
304
309

Fig. 3

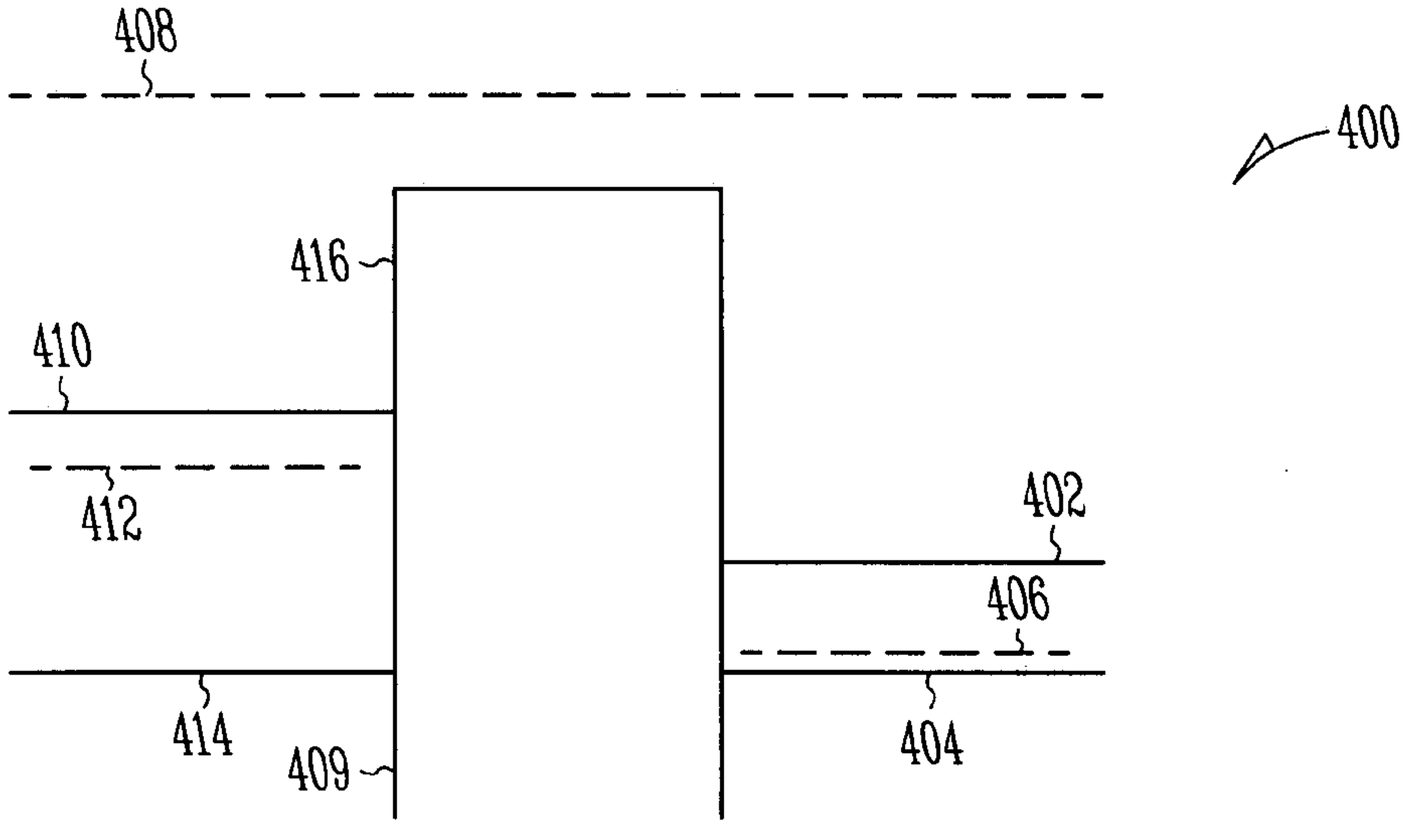
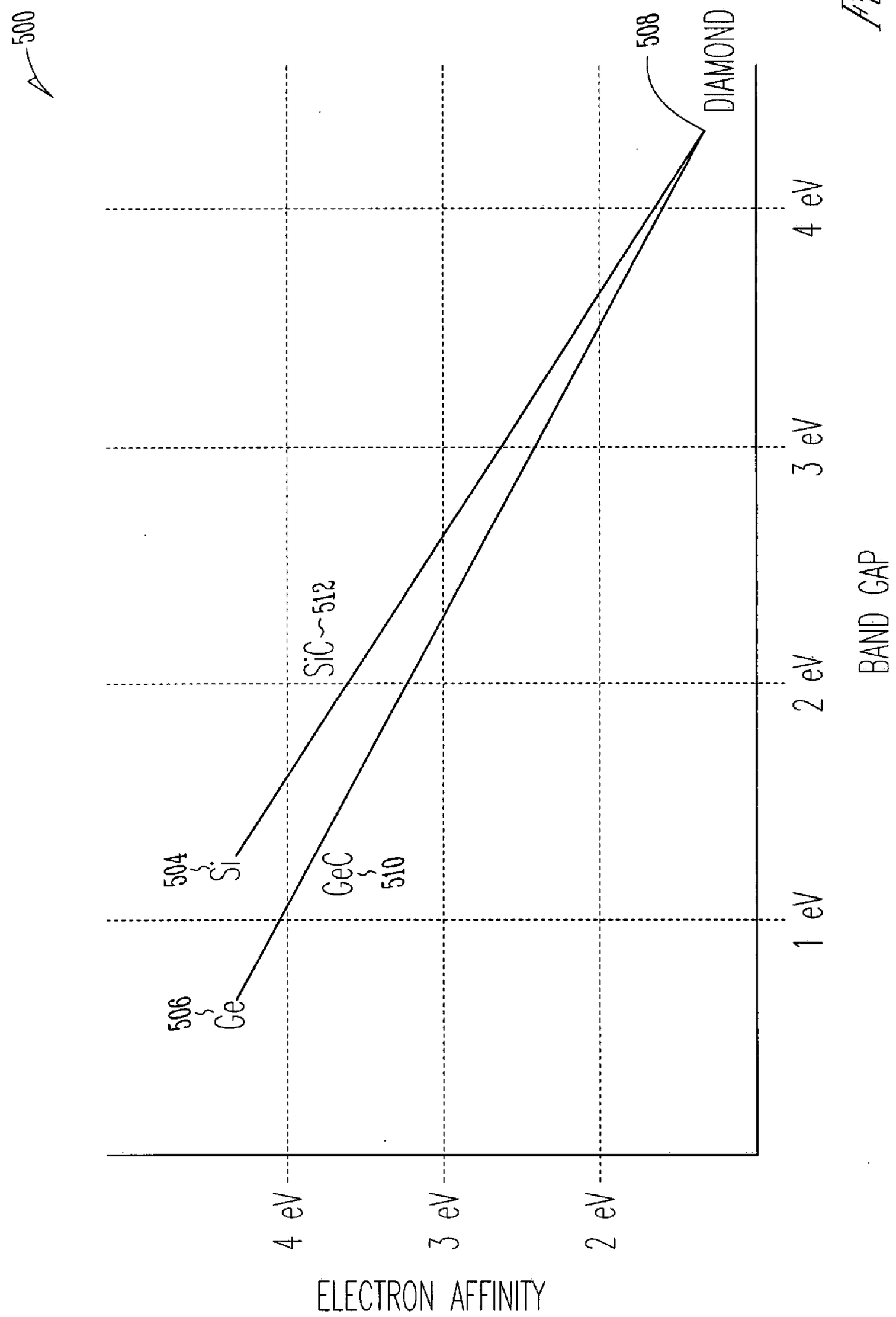

408
400
416
410
402
412
406
414
404
409

Fig. 4

Fig. 5


500
508
DIAMOND
4 eV
3 eV
2 eV
1 eV
BAND GAP
SiC~512
504
Si
GeC
510
506
Ge
4 eV
3 eV
2 eV
ELECTRON AFFINITY

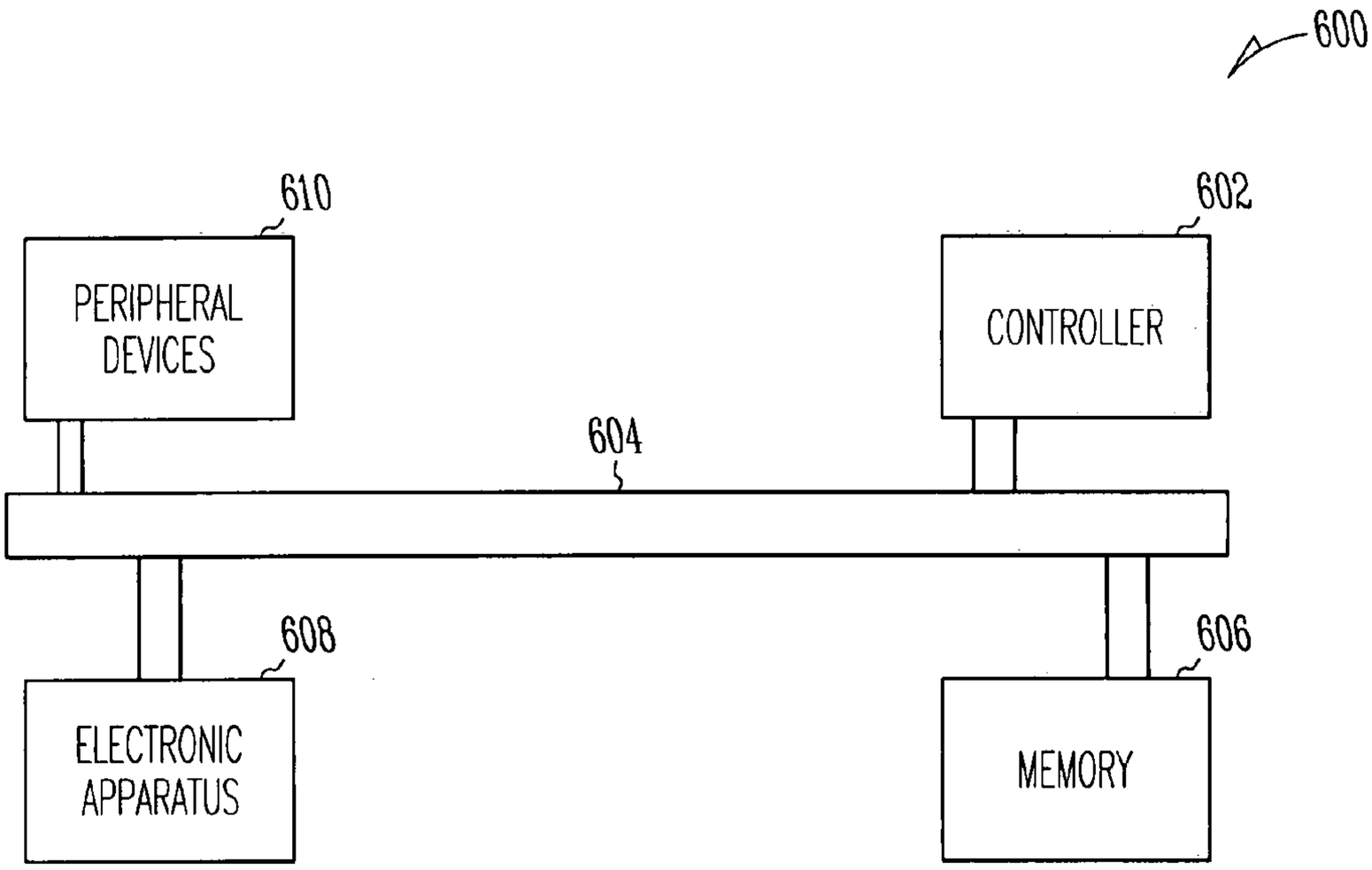

600
610
PERIPHERAL DEVICES
602
CONTROLLER
604
608
ELECTRONIC APPARATUS
606
MEMORY

Fig. 6

GERMANIUM-SILICON-CARBIDE FLOATING GATES IN MEMORIES

[0001] This application is a divisional of U.S. application Ser. No. 11/063,825 filed Feb. 23, 2005, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] This application relates generally to semiconductor devices and device fabrication and, more particularly, to transistor gate materials and their properties, and in particular to floating gate devices.

BACKGROUND

[0003] The electronic device industry uses many different types of memory in computers and other electronic systems, such as automobiles and traffic control systems. Different types of memory have different access speeds and different cost per stored bit. For example, items of memory that require rapid recovery may be stored in fast static random access memory (RAM). Information that is likely to be retrieved a very short time after storage may be stored in less expensive dynamic random access memory (DRAM). Large blocks of information may be stored in low cost, but slow access media such as magnetic disk. Each type of memory has benefits and drawbacks, for example DRAMs lose the stored information if the power is shut off. While the magnetic memory can retain the stored information when the power is off (known as non-volatile), the time to retrieve the information is hundreds of times slower than semiconductor memory such as RAM. One type of non-volatile semiconductor memory device is electrically programmable read-only memory (EPROM). There are also electrically-erasable programmable read-only memory (EEPROM) devices. One type of EEPROM is erasable in blocks of memory at one time, and is known as flash memory. Flash memory is non-volatile like magnetic memory, is much faster than magnetic memory like RAM, and is becoming widely used for storing large amounts of data in computers. However, writing information to a conventional flash memory takes a higher write voltage than it does to write information to conventional RAM, and the erase operation in flash requires a relatively long time period.

[0004] Conventional EEPROM devices, such as flash memory, may operate by either storing electrons on an electrically isolated transistor gate, known as a floating gate, or not storing electrons on the floating gate. Typically the write (or program) operation and the erase operation are performed by another transistor gate, known as the control gate, which is located above the floating gate. A large positive voltage on the control gate will draw electrons from the substrate through the gate oxide and trap them on the floating gate. The erase operation uses a large negative voltage to drive any stored electrons on the floating gate off of the gate and back into the substrate, thus returning the floating gate to a zero state. This operation may occur through various mechanisms, such as Fowler-Nordheim (FN) tunneling. The rate at which the electrons can be transported through the insulating gate oxide to and from the floating gate is an exponential factor of both the thickness of the insulator and of the electrical height of the insulation barrier between the substrate and the floating gate. Grown gate oxides have great height, and slow tunneling.

[0005] Electronic devices have a market driven need to reduce the size and power consumption of the devices, such as by replacing unreliable mechanical memory like magnetic disks, with transistor memory like EEPROM and flash. These increasingly small and reliable memories will likely be used in products such as personal computers (PCs), personal digital assistants (PDAs), mobile telephones, laptop PCs, and even in replacing the slow hard disk drives in full sized computer systems. This is because a solid state device, such as flash memory, is faster, more reliable and has lower power consumption than a complex and delicate mechanical system such as a high speed spinning magnetic disk. What is needed is an improvement in the erase time for EEPROM devices. With improved erase times, the high density of flash memory, and a speed of operation comparable to DRAMs, flash memory might replace both magnetic memory and DRAMs in certain future computer devices and applications.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. **1** illustrates a transistor with a germanium silicon carbide gate, according to embodiments of the present subject matter;

[0007] FIG. **2** illustrates a non-volatile memory element with a germanium silicon carbide gate, according to embodiments of the present subject matter;

[0008] FIG. **3** is an energy band diagram for a polysilicon gate transistor;

[0009] FIG. **4** is an energy band diagram for a silicon carbide gate transistor, according to an embodiment;

[0010] FIG. **5** is a diagram showing bandgap versus electron affinity according to an embodiment; and

[0011] FIG. **6** illustrates a diagram for an embodiment of an electronic system having devices with a floating gate transistor containing a mixture of germanium, silicon and carbon according to an embodiment.

DETAILED DESCRIPTION

[0012] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific aspects and embodiments in which the present invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The various embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

[0013] The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form an integrated circuit (IC) structure. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semicon-

ductor structures well known to one skilled in the art. The term conductor is understood to generally include n-type and p-type semiconductors and the term insulator or dielectric is defined to include any material that is less electrically conductive than the materials referred to as conductors or as semiconductors.

[0014] The term "horizontal" used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

[0015] Field effect transistors (FETs) are used in many different electronic devices, including memory devices. FETs are used both as access transistors and as memory elements. The structure of a typical FET **100** is shown in FIG. **1**, where a lightly doped substrate **102** has a heavily oppositely doped source region **104** and drain region **106**. The portion of the substrate **102** located between the source region **104** and the drain region **106** is known as the channel region **108**, and may have a doping level that is different from the doping level of the substrate **102**, and may even be counter doped to have a doping type opposite of the substrate. The substrate may be either lightly doped P type or N type, and the diffused source and drain regions will be heavily doped with the opposite doping type. There is a gate oxide **110** located over the channel region **108**, and making at least some contact with each of the source region **104** and drain region **106**. The gate oxide **110** is an insulator, such as thermally grown silicon dioxide, and at normal operating voltages prevents current flow from the substrate **102** to a conductive gate electrode **112**. Conductive gate electrode **112** is located on top of the gate oxide **110**, and also extends at least some distance over each of the source region **104** and drain region **106**. Conventional gate electrodes are formed of doped polycrystalline silicon (poly or polysilicon). Embodiments of the present subject matter form gate electrode **112** with a germanium silicon carbide (GeSiC) composition. In operation, when a signal is directed to the gate **112** over an electrical connection **120**, the signal voltage affects the concentration of electrical carriers in the channel region **108**. For example, if a positive voltage having a greater value than what is known as the threshold voltage of the transistor **100** is applied to gate **112**, then the relatively small number of electrons (negative carriers) in the P type substrate **102** will be attracted to the channel region **108** in great enough numbers to overwhelm the positive holes in the channel region, and thus temporarily convert the channel region to be N type as long as the positive voltage is applied to the gate **112**. Thus a large enough positive voltage (known as the threshold voltage) on the gate **112** will electrically connect the source region **104** to the drain region **106** and turn on the transistor **100**. The threshold voltage depends upon the thickness and dielectric constant of the gate insulator **110**, the doping level of the channel region **108**, and the electron affinity of the material forming the gate electrode **112**. Thus, a gate electrode made of a material such as GeSiC may have the threshold voltage of the transistor adjusted to a desired level by changing the electron affinity of the transistor, and may thus reduce the number and size of ion implantation adjustments of the channel doping level.

[0016] The illustrative floating gate transistor **200**, as shown in FIG. **2**, may have a lightly doped substrate **202** with a heavily oppositely doped source region **204** and drain region **206**. For example, the substrate **202** may be a lightly doped P type region, and the source region **204** and drain region **206** would then be heavily doped N+ type. The portion of the substrate **202** located between the source region **204** and the drain region **206** is again known as the channel region **208**, and may have a doping level that is different from the doping level of the substrate **202**. There is a gate oxide **210** located over the channel region **208**, which is an insulator such as thermally grown silicon dioxide. There is an electrically floating conductive gate **212**, located on top of the gate oxide **210**, which unlike the previously discussed transistor **100** of FIG. **1**, has no direct connection to signal voltages, and is typically called a floating gate since it is electrically floating. Conventionally, floating gates are typically formed of doped polysilicon. Embodiments of the present subject matter form floating gate **212** with a germanium silicon carbide composition. There is an inter-gate dielectric or insulator **214** which electrically separates the floating gate **212** from a control gate **216**, which is also typically made of polysilicon. In operation the control gate is connected to signal voltage **220**. The signal voltage **220** must be larger than the signal voltage **120** for the conventional transistor since the control gate is further from the channel region **208** and because the electrons in the channel region must be at a high enough voltage to be injected through the gate oxide **210** to become trapped on floating gate **212**. A given signal voltage level will provide a current of electrons through the gate oxide **210** that depends exponentially upon the level of the signal voltage, the thickness of the gate oxide **206** and the electrical height of the barrier formed by the gate oxide **210** between the energy levels of the substrate at the channel **208** and the energy level of the floating gate **212**. Changing the material of the substrate **202** or of the floating gate **212** changes the electrical height of the barrier formed by the gate oxide **210**, and radically changes the amount of current that tunnels through the gate oxide **206** by means of Fowler-Nordheim tunneling. Thus, changing the tunneling barrier height results in erase operations that have larger currents at a given erase voltage level, and therefore result in faster erase times for memory devices. Another advantage of lowering the tunneling barrier height is that lower erase voltages may be used. Lower erase voltages mean lower electrical fields for a given dielectric thickness, and therefore reduced reliability issues such as time dependent dielectric breakdown of the gate insulator and inter-gate insulator.

[0017] The reason that changing the material of the substrate or of the floating gate changes the electrical height of the tunneling barrier is best understood by examination of what is known as an energy band diagram, as shown in FIG. **3** for the typical memory transistor discussed in FIG. **2** and used in flash memory. As noted above, the excellent quality of grown gate oxides results in a large electrical height of the tunneling barrier formed by the oxide. This high quality oxide results in lower programming currents and lower erase currents and causes slower memory operation. An issue with

other gate insulators besides grown oxides, such as chemical vapor deposited (CVD) oxides, silicon nitride, aluminum oxide, tantalum oxide, and titanium oxides, is that the results have proven unacceptable from a device electrical performance point of view, including high levels of what are known as surface states. If the surface states are reduced by growing a thin oxide underneath the deposited oxide, then the interface between the two insulators may have large numbers of what are known as trap states, and may have band gap discontinuities and differences in the conductivity of the insulator films. Thus, changing the gate insulator to reduce the tunneling barrier height and voltage may pose problems, particularly with maintaining consistent time-dependent device electrical operation.

[0018] Another method of changing the tunneling voltage, and thus equivalently increasing the tunneling current at a particular voltage level, is to change the overall tunneling barrier height by increasing the internal energy level of the conductors on either side of the insulator, rather than by lowering the insulator barrier level. Changing the silicon substrate to some other material may cause numerous practical problems in the fabrication of devices, since so much is known about the use of silicon. Changing the material of the floating gate to a material with what is known as a lower electron affinity, denoted by the lower case Greek letter Chi (χ) results in higher tunneling currents. A lower electron affinity reduces the effective height of the insulator tunneling barrier, which as noted previously has an exponential effect on the amount of tunneling current at a given voltage.

[0019] A transistor built on a single crystal silicon substrate has a band gap diagram **300**, with a conduction level **302**, a valence level **304**, and a Fermi level **306**, as shown for a lightly doped P type silicon substrate with reference to the vacuum level **308**, which represents the amount of energy it would take to remove an electron from the silicon. On the opposite side of a gate oxide **309**, heavily doped N type polycrystalline silicon will have a conduction level **310**, a Fermi level **312** and a valence level **314**. The gate oxide **309** has an energy level value **316**, whose difference from the vacuum level **308** represents the electron affinity χ of the gate oxide, typically thermally grown silicon dioxide. For good quality thermally grown silicon dioxide, the value of χ is 0.9 eV. For electrons on the floating gate conduction band **310**, the value of electron affinity χ is the difference between **310** and the vacuum level **308**, and for doped polysilicon is approximately 4.1 eV. Thus, the barrier that an electron tunneling from the floating gate **212** conduction band **310** to the silicon substrate **202** in the area of the channel **208**, must traverse during an erase operation is the height represented by the difference between the top of the gate oxide **316** and the conduction band **310**, or 4.1 eV minus 0.9 eV, or about 3.2 eV. As noted previously, the tunneling rate is an exponential factor of the height of the barrier, and the width of the oxide, which is controlled by the process parameter of gate oxide thickness.

[0020] The distance between the conduction level **310** and the valence level **314** is known as the band gap, and has a value in silicon of approximately 1.1 eV. Since the value of electron affinity for the gate oxide is not going to change, then the use of a floating gate material that has a larger band gap would result in a lower electron affinity, and thus a reduced tunneling barrier. Changing the electron affinity of the gate material also changes the threshold voltage of the transistor, and may be used in conjunction with channel doping levels and gate insulator thickness and dielectric constant to adjust the threshold voltage level.

[0021] FIG. **4** illustrates the band gap diagram **400** for an embodiment of a silicon carbide gate material. There is still a silicon substrate conduction level **402**, a silicon substrate valence level **404**, and a Fermi level **406** with reference to the vacuum level **408**. On the opposite side of the thermally grown silicon dioxide gate oxide **409**, the illustrative silicon carbide gate will have a conduction level **410**, a Fermi level **412** and a valence level **414**, all of which may be different from the values in the case of polysilicon gates. The gate oxide **409** still has the same energy value **416**, and electron affinity χ of the gate oxide, typically 0.9 eV. The band gap for silicon carbide depends upon the ratio of silicon to carbon, and varies from the silicon value of 1.1, as noted above, to the pure carbon value of approximately 4.2 eV. For a silicon carbide mixture, the value of the band gap is about 2.1 eV to 2.6 eV depending upon the percentage of carbon. Since the conduction band is now closer to the vacuum level **408**, the electron affinity is lower, about 3.7 eV, and the height of the tunneling barrier is now lower, typically below 2.8 eV, which is lower than the tunneling barrier found in the case of polysilicon of about 3.2 eV. Thus, the tunneling barrier is lowered, and even a small difference in tunneling barrier height causes a large change in tunneling current. For germanium carbide, a very similar band diagram shows a tunneling barrier that extends from a larger value than that of polysilicon for a pure germanium gate of 3.6 eV, to a barrier value that is the same as the polysilicon value of 3.2 eV at a 4% carbon content, to lower values for increased carbon content above the 4% level. The values for silicon, silicon carbide and germanium carbide are discussed in more detail with respect to FIG. **5** later in this disclosure. Increased tunneling current flow at a given erase voltage value results in much faster erase operations and improved EEPROM or flash memory operational speeds.

[0022] Crystalline silicon carbide and silicon germanium carbide can be epitaxially grown on a silicon substrate and may be used in both metal oxide semiconductor field effect transistors (MOSFET) or bipolar transistor devices, with the silicon substrate acting as a seed layer for crystal growth. In an embodiment the silicon carbide, germanium carbide and silicon germanium carbide are microcrystalline or amorphous. Such microcrystalline layers or amorphous layers may be grown on insulator layers such as silicon dioxide gate insulator layers, or other insulator layers, by chemical vapor deposition (CVD), laser assisted CVD, plasma CVD, ultra-high vacuum CVD, or sputtering.

[0023] FIG. **5** is a graph **500** that illustrates the ability to adjust the tunneling barrier height, and thus the tunneling barrier current level, for various embodiments of mixtures of silicon **504**, germanium **506**, and carbon in the form of diamond **508**. The values of germanium carbide of varying percentages of germanium are shown by the line connecting **506** and **508**, including the interesting point **510** where a 4% carbon value in germanium provides the same band gap 1.1 eV as pure silicon **504**, but with a lower electron affinity χ and thus improved tunneling currents and faster erase operations without other significant electrical changes in the transistor operation due to changes in the band gap value. Silicon carbide values are projected on the line from **504** to **508**, with silicon carbide having a band gap with a 2.1 eV

value shown at **512**. Various embodiments of the present disclosed methods and devices can be found in the region of the graph between **510** and **512** and the entire area between the lines representing germanium carbide and silicon carbide compositions. An illustrative silicon germanium carbide material with equal amounts of silicon and germanium and varying amounts of carbon would have a band gap to electron affinity χ curve that fits about halfway between the germanium carbide line and the silicon carbide line.

[**0024**] FIG. **6** depicts a diagram of an embodiment of a system **600** having a controller **602** and a memory **606**. Controller **602** and/or memory **606** include a transistor having a gate electrode made of a mixture of germanium, silicon and carbon. System **600** also includes an electronic apparatus **608**, and a bus **604**, where bus **604** may provide electrical conductivity and data transmission between controller **602** and electronic apparatus **608**, and between controller **602** and memory **606**. Bus **604** may include an address, a data bus, and a control bus, each independently configured. Bus **604** also uses common conductive lines for providing address, data, and/or control, the use of which may be regulated by controller **602**. In an embodiment, electronic apparatus **608** includes additional memory devices configured similarly to memory **606**. Electronic apparatus **608** may include, but is not limited to, information handling devices, wireless systems, telecommunication systems, fiber optic systems, electro-optic systems, and computers. An embodiment includes an additional peripheral device or devices **610** coupled to bus **604**. In an embodiment controller **602** is a processor. Any of controller **602**, memory **606**, bus **604**, electronic apparatus **608**, and peripheral device or devices **610** may include a gate electrode formed of a mixture of silicon, germanium and carbon in accordance with the disclosed embodiments.

[**0025**] System **600** may include, but is not limited to, information handling devices, telecommunication systems, and computers. Peripheral devices **610** may include displays, additional storage memory, or other control devices that may operate in conjunction with controller **602** and/or memory **606**. It will be understood that embodiments are equally applicable to any size and type of memory circuit and are not intended to be limited to a particular type of memory device.

CONCLUSION

[**0026**] An embodiment has a floating gate transistor with a gate made of a material having a lower tunneling barrier and thus lower erase times. Another embodiment has the floating gate formed of germanium silicon carbide. Another embodiment has the composition of the floating gate determined by a desired tunneling current. Another embodiment includes a transistor with a conventional gate having the composition of the germanium silicon carbide adjusted to optimize the threshold of a metal oxide semiconductor field effect transistor (MOSFET).

[**0027**] An embodiment for a method for forming a floating gate memory device includes forming a floating gate having a lower tunneling barrier by forming the gate of a mixture of germanium, silicon and carbon. Another embodiment includes a method of storing data by setting the voltage of the control gate, drain diffusion and source diffusion to either trap electrons on a floating gate made of germanium, silicon and carbon, or by ejecting trapped electrons from the floating gate by Fowler-Nordheim tunneling.

[**0028**] Applications include structures for transistors, memory devices such as flash, and electronic systems with gates containing a mixture of germanium, silicon and carbon, and methods for forming such structures.

[**0029**] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. It is to be understood that the above description is intended to be illustrative, and not restrictive, and that the phraseology or terminology employed herein is for the purpose of description and not of limitation. Combinations of the above embodiments and other embodiments will be apparent to those of skill in the art upon studying the above description. The scope of the embodiments of the present invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A method of storing data in a memory device, comprising:

addressing selected ones of a plurality of memory cells with selected ones of a plurality of word lines and a plurality of bit lines;

increasing a voltage applied to a control gate on the selected memory cells, the memory cells each including a substrate, a source region, a drain region and a floating gate disposed beneath the control gate and separated therefrom by an inter-gate insulator layer, the floating gate comprising a conductive film including a mixture of germanium, silicon and carbon;

trapping electrons on the floating gate in response to a positive voltage having at least a first voltage level being applied to the control gate for at least a first time period, changing the memory cell to a first memory state; and

ejecting electrons from the floating gate in response to a negative voltage having at least a second voltage level being applied to the control gate for at least a second time period, changing the memory cell to a second memory state.

2. The method of storing data in a memory device of claim 1, wherein further the floating gate comprises a mixture having a lower electron affinity than a doped polycrystalline silicon floating gate.

3. The method of storing data in a memory device of claim 1, wherein the floating gate composition is selected to obtain a desired tunneling current value for ejecting electrons from the floating gate during the second time period when the negative second voltage level is applied to the control gate.

4. The method of storing data in a memory device of claim 1, wherein the memory device is controlled as a flash memory.

5. The method of storing data in a memory device of claim 1, wherein the floating gate has a structure that is one of micro-crystalline and amorphous.

6. The method of storing data in a memory device of claim 1, further comprising a programming voltage signal of approximately 12 volts on the control gate for the first time

period, a voltage level of approximately 6 volts on the drain region for at least the first time period, a voltage level of a ground on the source region for at least the first time period, and electrons from the substrate trapped on the gate electrode.

7. The method of storing data in a memory device of claim 1, further comprising an erase signal of approximately negative 12 volts on the control gate for the second time period, a voltage level of ground on the source region for at least the second time period, and electrons ejected from the gate electrode to the substrate.

8. A method of storing data in a memory device having a source region and a drain region separated by a channel region in a substrate, a gate insulator adjacent to the channel region, a floating gate on the gate insulator comprising a conductive film including germanium, silicon and carbon, an inter-gate insulator on the floating gate, a control gate on the inter-gate insulator, comprising:

trapping electrons on the floating gate in response to a positive voltage having a first voltage level applied to the control gate for a first time period, changing the memory cell to a first memory state; and

ejecting electrons from the floating gate in response to a negative voltage having a second voltage level applied to the control gate for a second time period, changing the memory cell to a second memory state.

9. The method of storing data in a memory device of claim 8, wherein trapping electrons on the floating gate includes selecting proportions of germanium, silicon and carbon to obtain a material having a lower electron affinity than a polycrystalline silicon floating gate.

10. The method of storing data in a memory device of claim 9, wherein trapping electrons on the floating gate includes selecting proportions of germanium, silicon and carbon to obtain a desired tunneling current value for ejecting electrons from the floating gate.

11. The method of storing data in a memory device of claim 8, wherein storing data further includes a programming voltage signal of 12 volts on the control gate, a voltage level of 6 volts on the drain region, a voltage level of a reference voltage on the source region, resulting in electrons from the substrate becoming trapped on the floating gate.

12. The method of storing data in a memory device of claim 11, wherein storing data further includes maintaining each of the programming voltage signal, the drain voltage level and the source reference voltage level, for at least a desired first time period.

13. The method of storing data in a memory device of claim 11, wherein storing data further includes setting the reference voltage level to a ground voltage level.

14. The method of storing data in a memory device of claim 8, wherein storing data further includes an erase voltage signal of negative 12 volts on the control gate, a voltage level of a reference voltage on the source region, resulting in electrons trapped on the floating gate being ejected to one of the substrate and the drain region.

15. The method of storing data in a memory device of claim 11, wherein storing data further includes maintaining each of the erase voltage signal and the source reference voltage level, for at least a desired second time period.

16. The method of storing data in a memory device of claim 8, wherein trapping electrons on the floating gate further includes a percentage of germanium about 96%, a percentage of silicon about 0%, and a percentage of carbon about 4%, forming germanium carbide having a band gap of approximately 1.1 eV.

17. The method of storing data in a memory device of claim 8, wherein trapping electrons on the floating gate further includes a percentage of germanium about 25%, a percentage of silicon about 25%, and a percentage of carbon about 50%, forming germanium silicon carbide having a band gap of approximately 2.5 eV.

18. The method of storing data in a memory device of claim 8, wherein trapping electrons on the floating gate further includes selecting a percentage of germanium, silicon and carbon to form a germanium-silicon carbide having a band gap greater than 1.1 eV and an electron affinity less than 3.5 eV.

19. The method of storing data in a memory device of claim 8, wherein trapping electrons on the floating gate further includes the floating gate having no direct electrical connection to either of the substrate and the control gate.

20. The method of storing data in a memory device of claim 8, wherein trapping electrons on the floating gate further includes the floating gate having at least enough electrical conductivity to redistribute trapped electrons essentially evenly throughout the film in a time period less than a minimum time period between one of a program and an erase signal, and a next one of a program and an erase signal.

21. The method of storing data in a memory device of claim 8, wherein trapping electrons on the floating gate further includes a percentage of germanium of zero, a percentage of silicon of 50%, and a percentage of carbon of 50%, forming silicon carbide.

22. The method of storing data in a memory device of claim 8, wherein trapping electrons on floating gate further includes a percentage of germanium of 50%, a percentage of silicon of zero, and a percentage of carbon of 50%, forming germanium carbide.

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