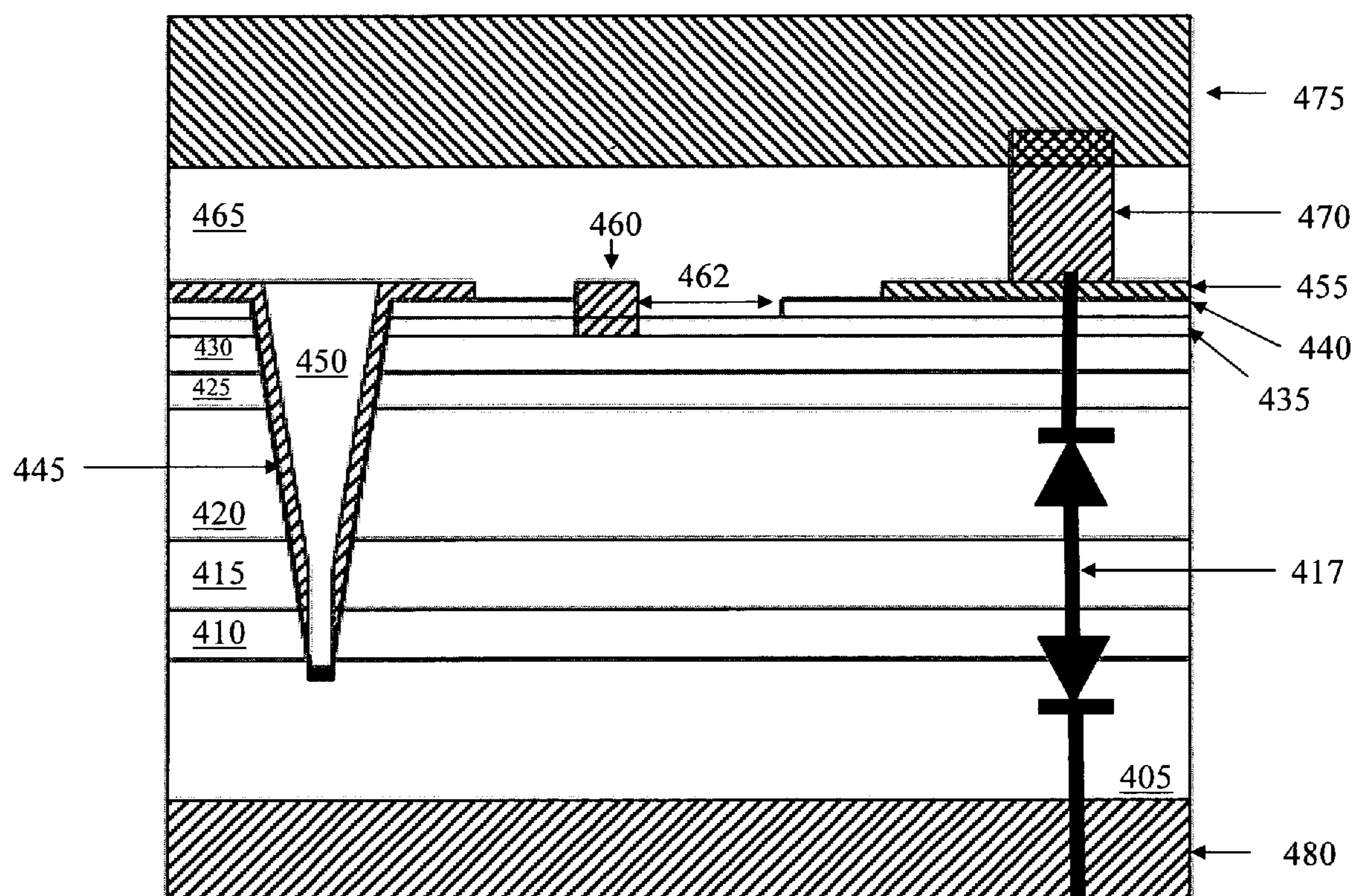




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(19) **United States**(12) **Patent Application Publication**
Brar et al.(10) **Pub. No.: US 2007/0145417 A1**(43) **Pub. Date: Jun. 28, 2007**(54) **HIGH VOLTAGE SEMICONDUCTOR
DEVICE HAVING A LATERAL CHANNEL
AND ENHANCED GATE-TO-DRAIN
SEPARATION****Publication Classification**(51) **Int. Cl.**
H01L 29/76 (2006.01)(52) **U.S. Cl.** **257/213**(76) Inventors: **Berinder P. S. Brar**, Newbury Park,
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DALLAS, TX 75252-5793 (US)(21) Appl. No.: **11/711,340**(22) Filed: **Feb. 27, 2007****Related U.S. Application Data**(63) Continuation-in-part of application No. 11/094,632,
filed on Mar. 29, 2005.(57) **ABSTRACT**

A semiconductor device having a lateral channel with contacts on opposing surfaces thereof. The semiconductor device includes a conductive substrate having a source contact covering a substantial portion of a bottom surface thereof. The semiconductor device also includes an isolation layer above the conductive substrate, a lateral channel above the isolation layer and a drain contact above the lateral channel. The semiconductor device further includes a gate located in a gate recess interposed between the lateral channel and the drain contact and a drain formed by at least one source/drain contact layer interposed between the lateral channel and the drain contact. The drain is offset on one side of the gate by a gate-to-drain separation distance. The semiconductor device still further includes an interconnect that connects the lateral channel to the conductive substrate operable to provide a low resistance coupling between the source contact and the lateral channel.



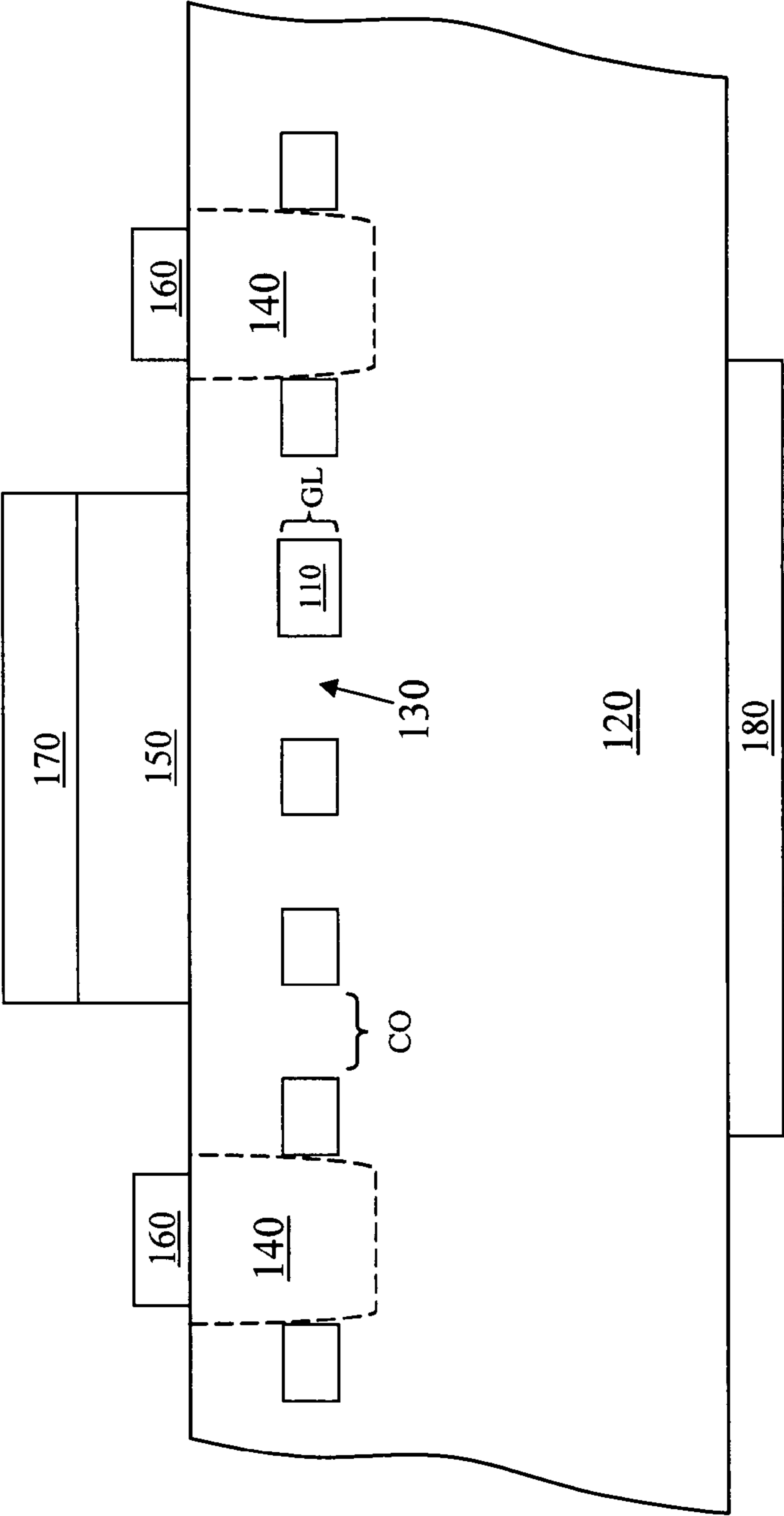


FIGURE 1
PRIOR ART

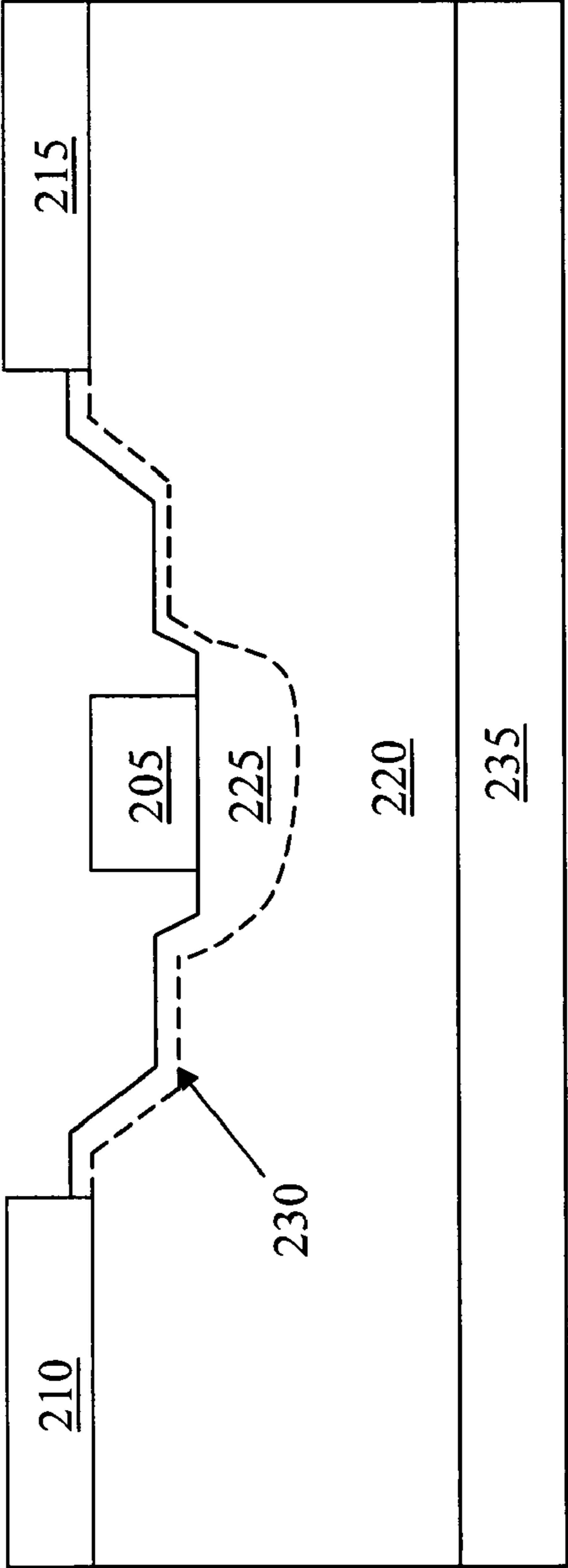


FIGURE 2A
PRIOR ART

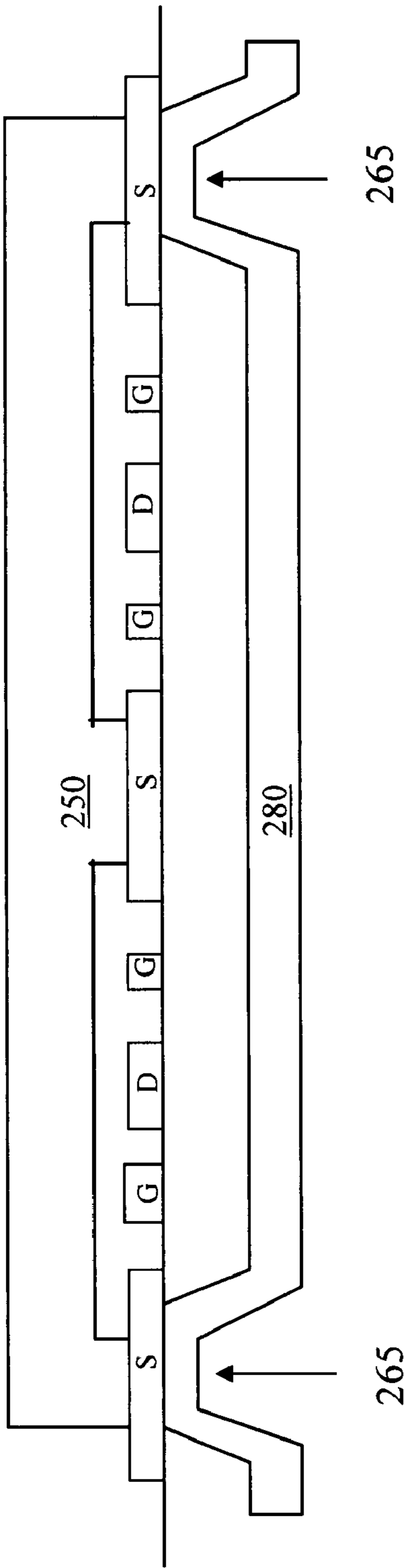


FIGURE 2B
PRIOR ART

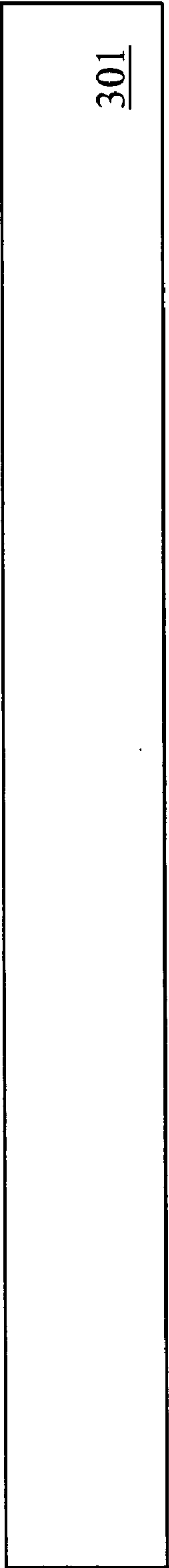


FIGURE 3

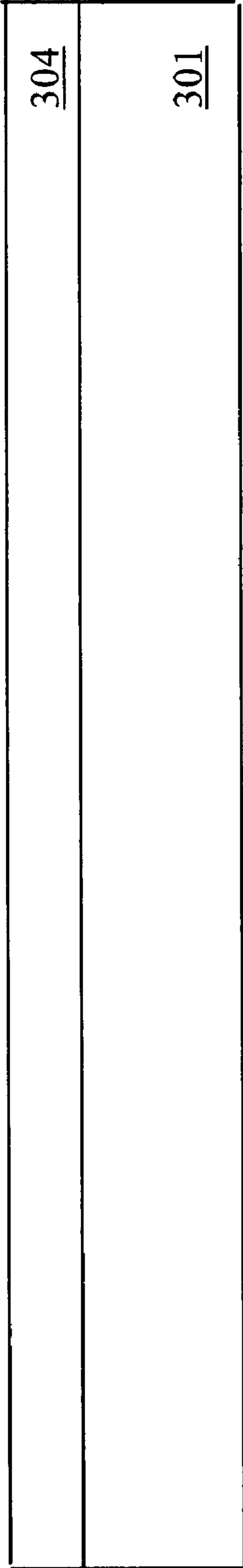


FIGURE 4

<u>307</u>
<u>304</u>
<u>301</u>

FIGURE 5

<u>320</u>
<u>318</u>
<u>315</u>
<u>313</u>
<u>307</u>
<u>304</u>
<u>301</u>

FIGURE 6

<u>325</u>
<u>320</u>
<u>318</u>
<u>315</u>
<u>313</u>
<u>307</u>
<u>304</u>
<u>301</u>

FIGURE 7

<u>339</u>
<u>336</u>
<u>333</u>
<u>325</u>
<u>320</u>
<u>318</u>
<u>315</u>
<u>313</u>
<u>307</u>
<u>304</u>
<u>301</u>

FIGURE 8

<u>340</u>
<u>339</u>
<u>336</u>
<u>333</u>
<u>325</u>
<u>320</u>
<u>318</u>
<u>315</u>
<u>313</u>
<u>307</u>
<u>304</u>
<u>301</u>

FIGURE 9

<u>350</u>
<u>345</u>
<u>340</u>
<u>339</u>
<u>336</u>
<u>333</u>
<u>325</u>
<u>320</u>
<u>318</u>
<u>315</u>
<u>313</u>
<u>307</u>
<u>304</u>
<u>301</u>

FIGURE 10

		<u>355</u>
		<u>350</u>
		<u>345</u>
		<u>340</u>
		<u>339</u>
		<u>336</u>
		<u>333</u>
		<u>325</u>
		<u>320</u>
		<u>318</u>
		<u>315</u>
		<u>313</u>
		<u>307</u>
		<u>304</u>
		<u>301</u>

FIGURE 11

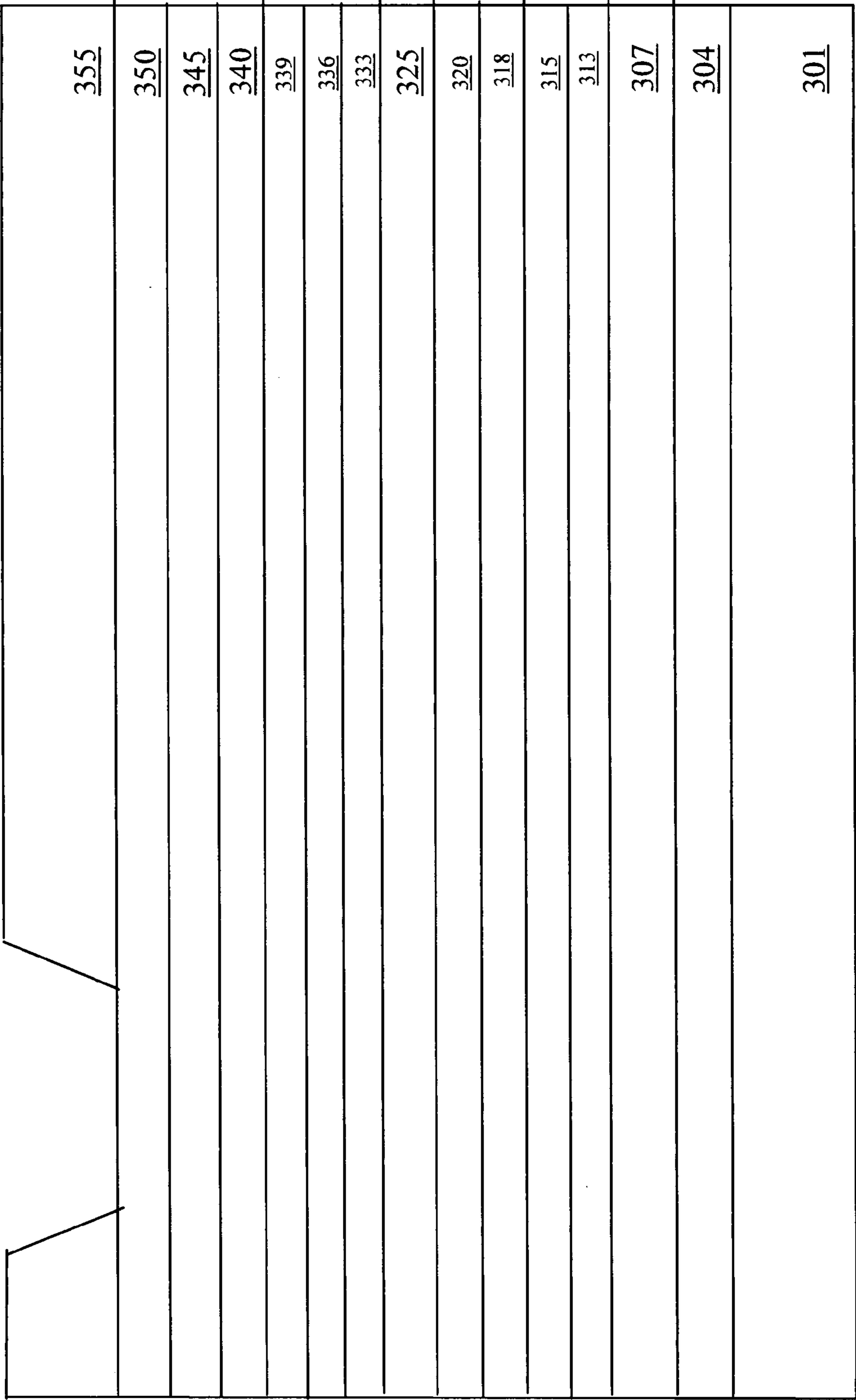


FIGURE 12

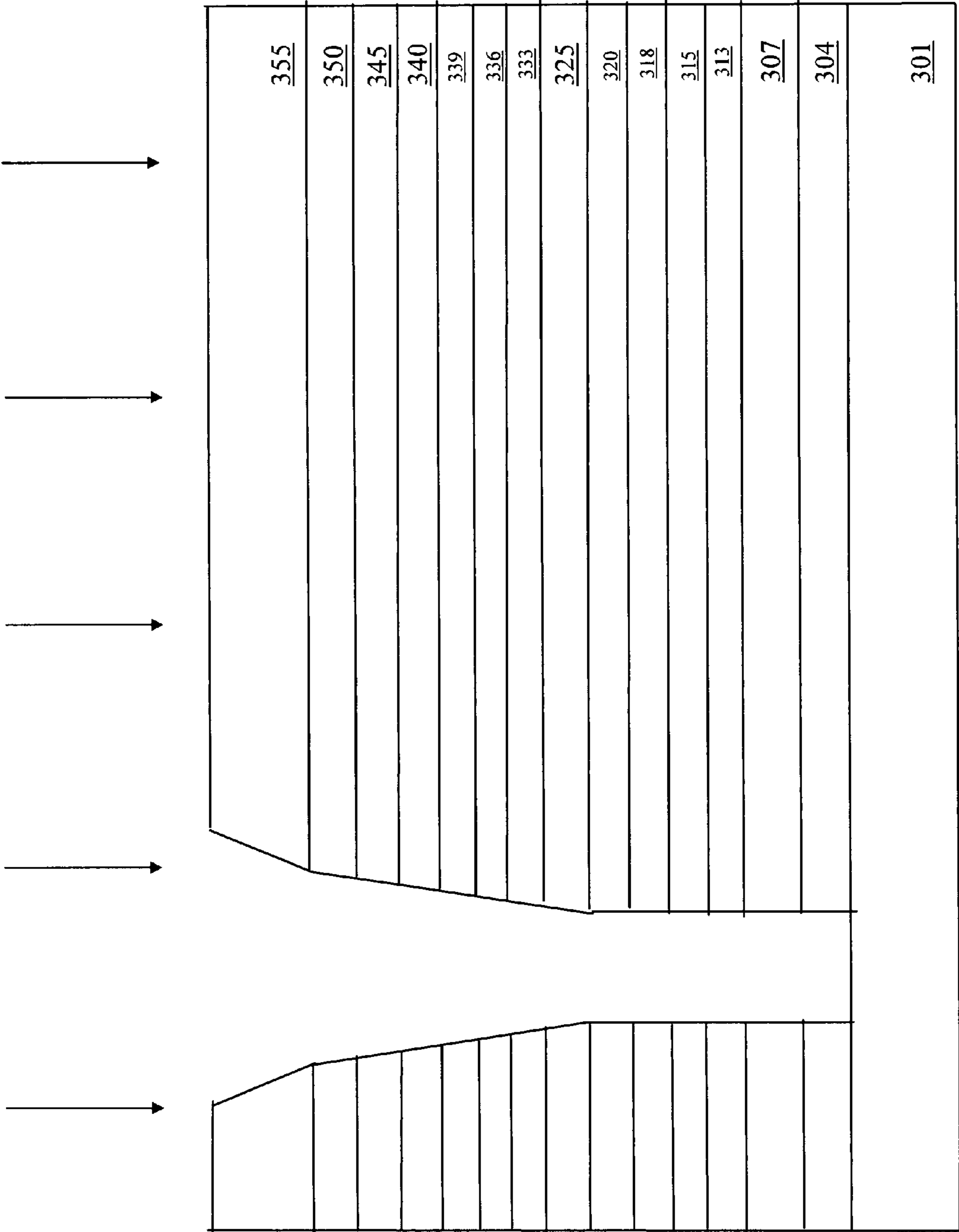


FIGURE 13

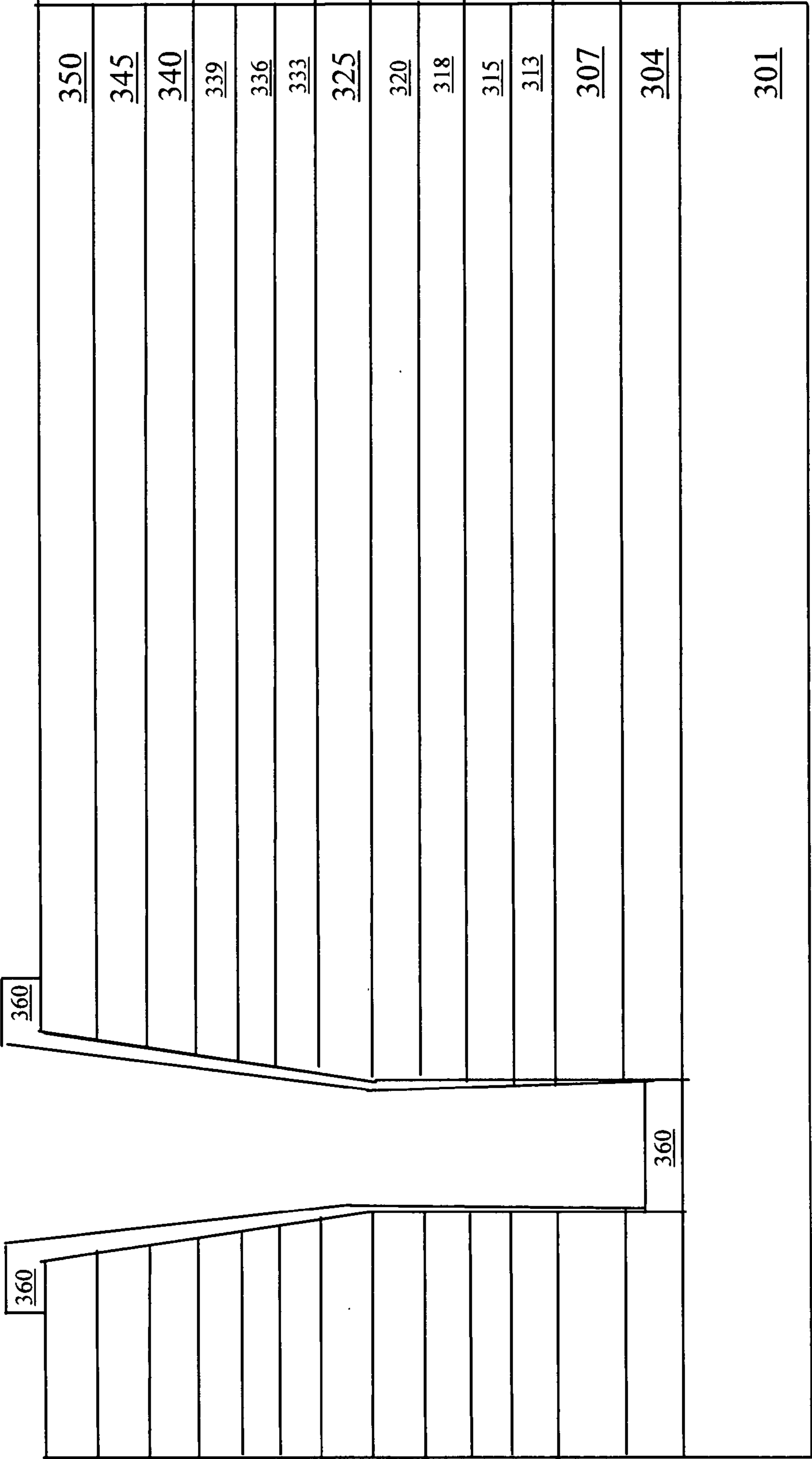


FIGURE 14

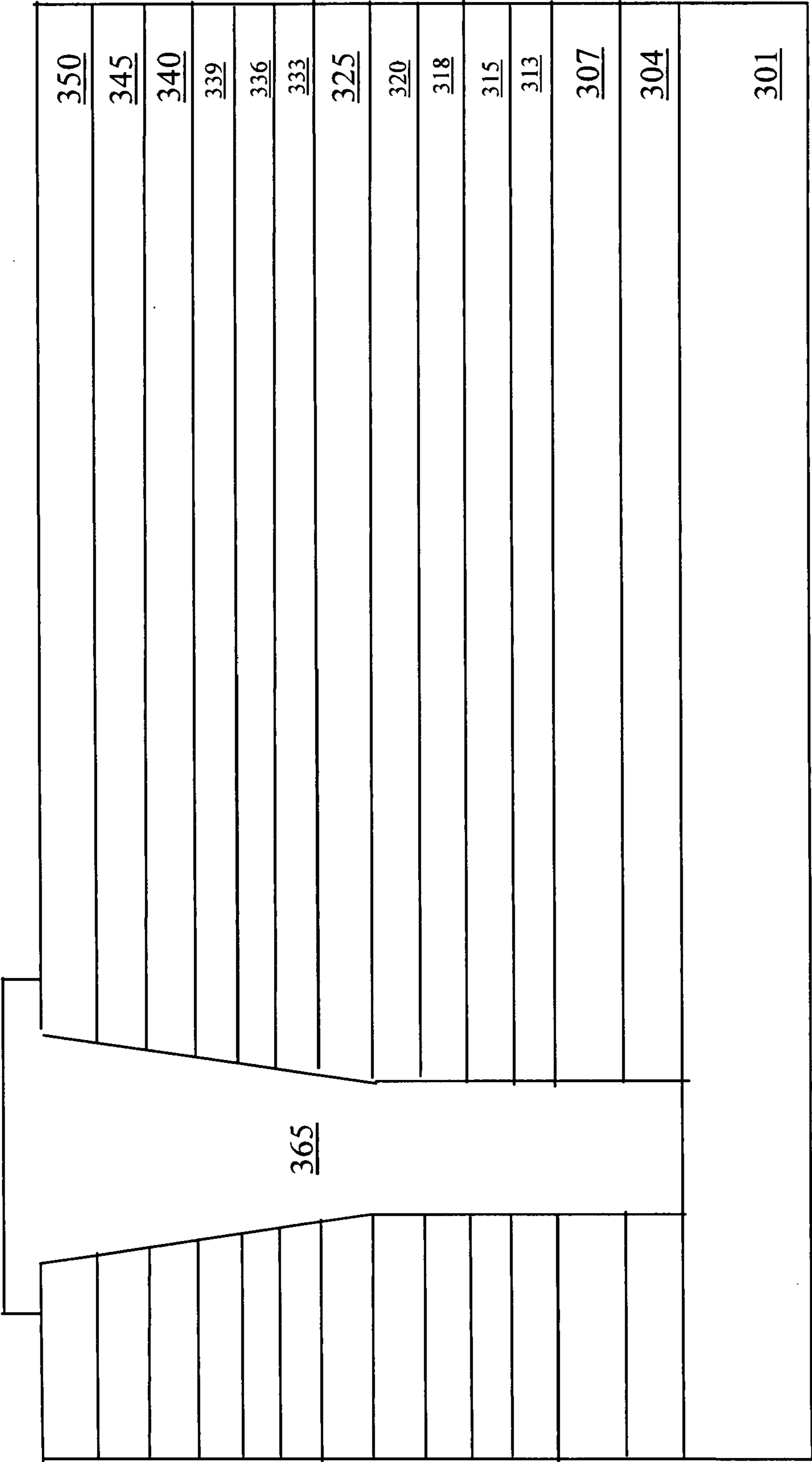


FIGURE 15

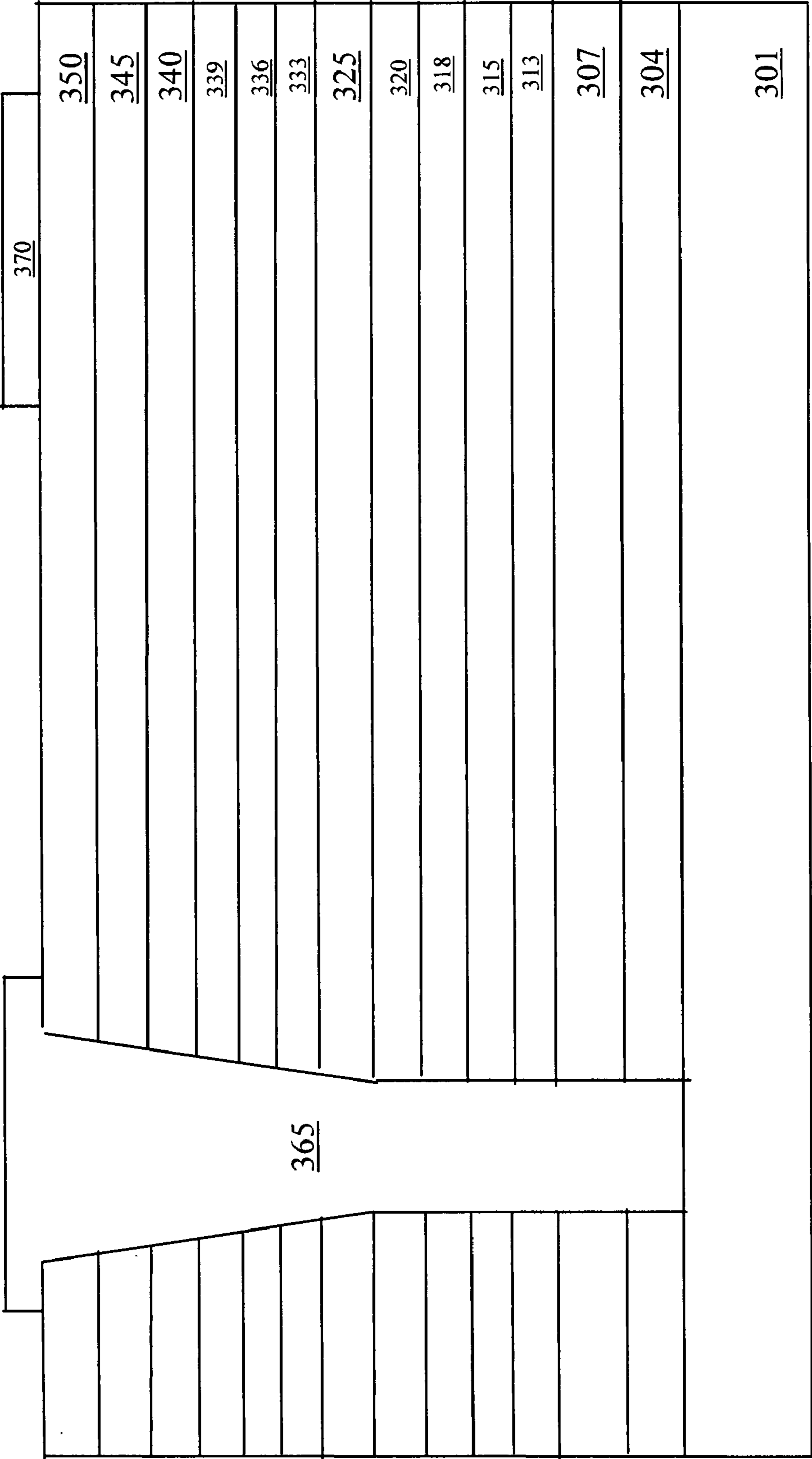


FIGURE 16

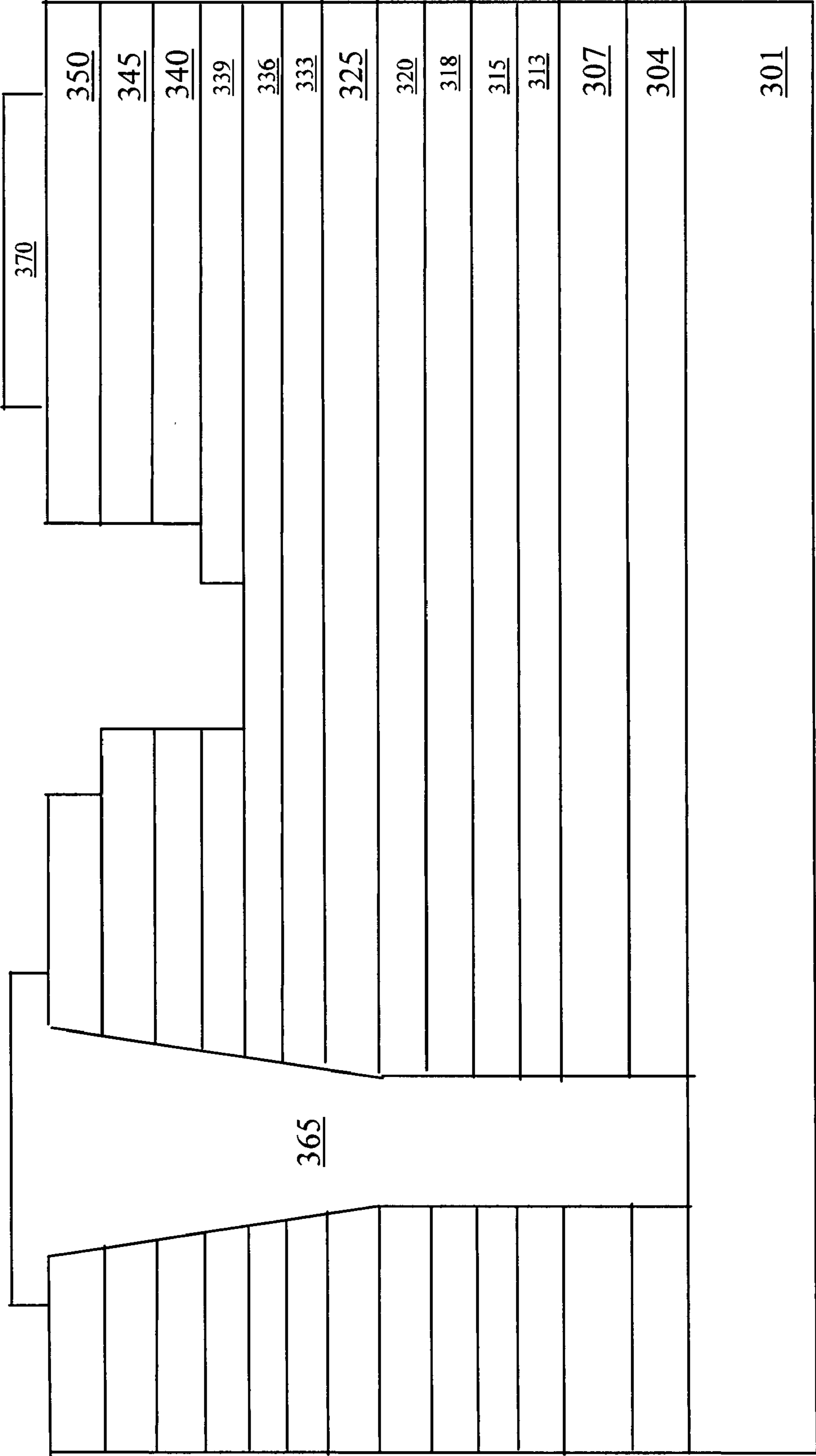


FIGURE 17

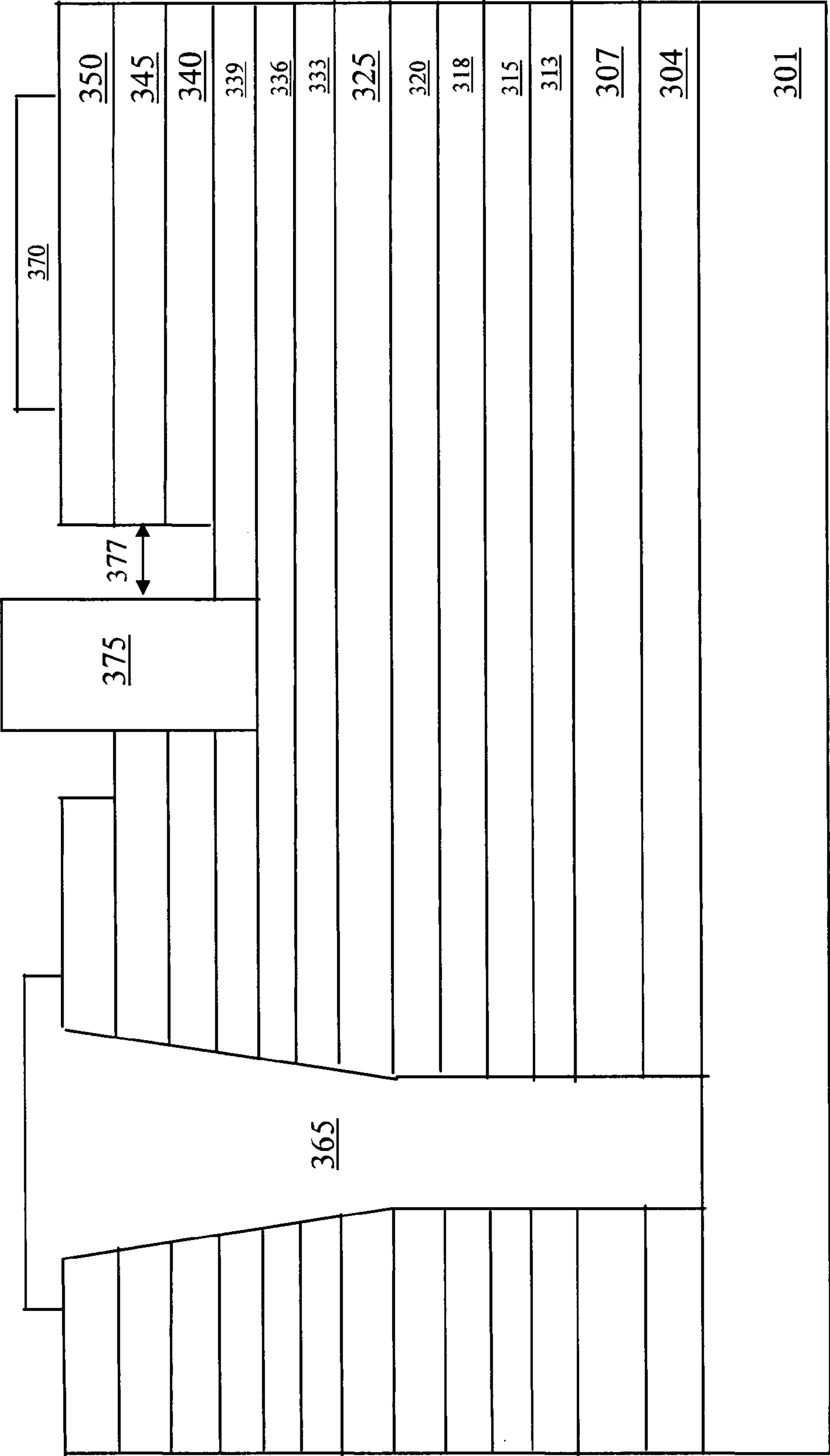


FIGURE 18

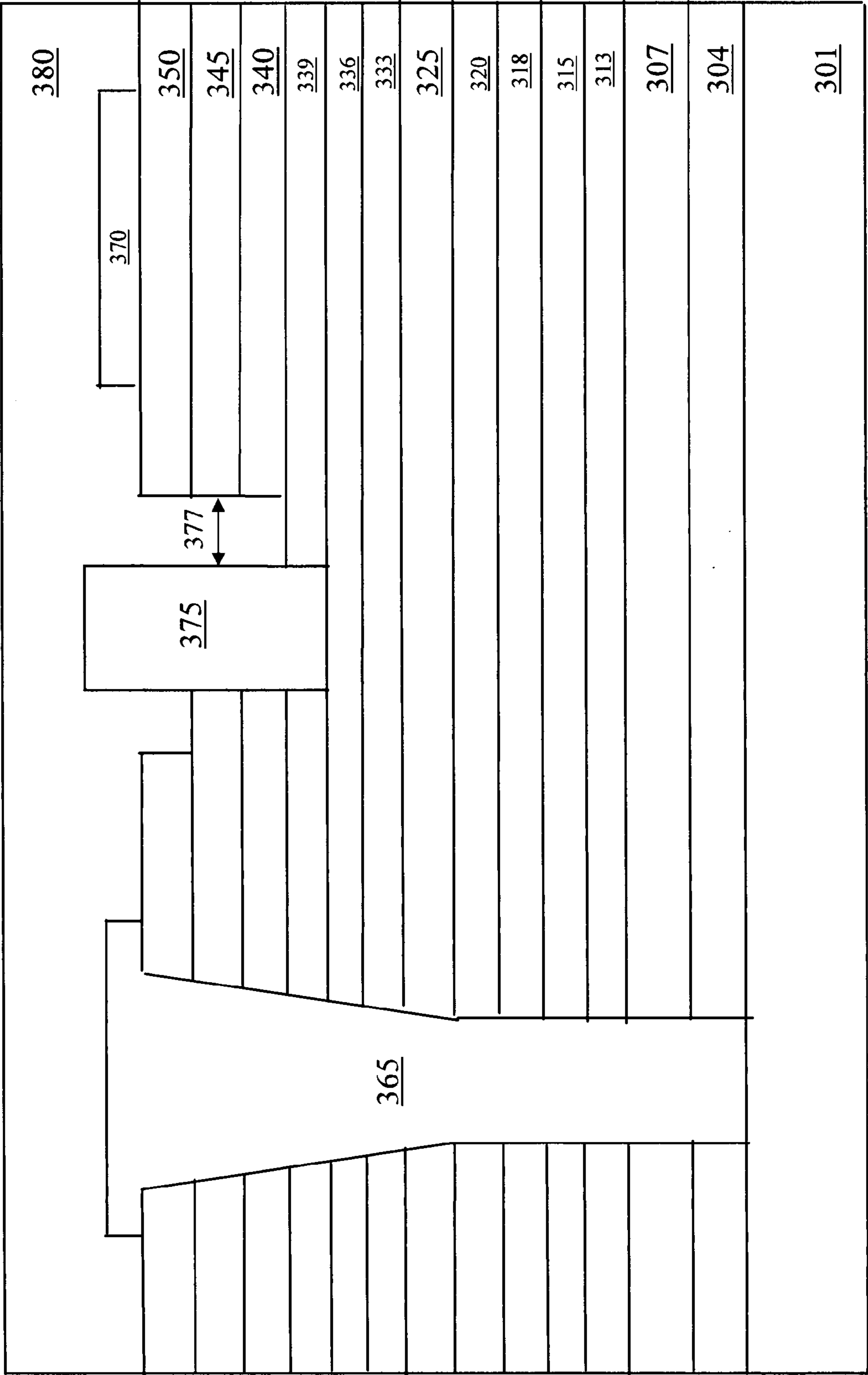


FIGURE 19

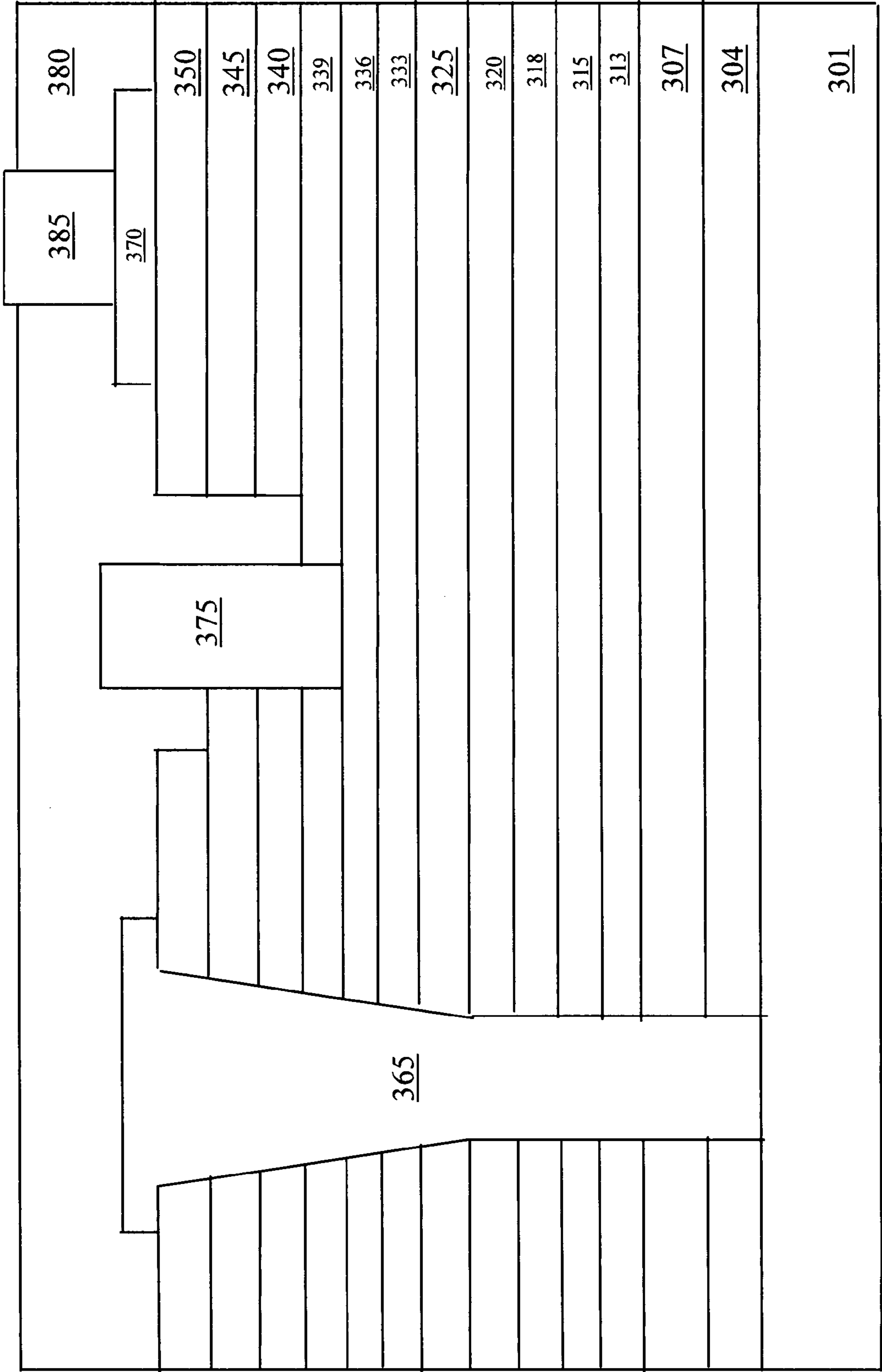


FIGURE 20

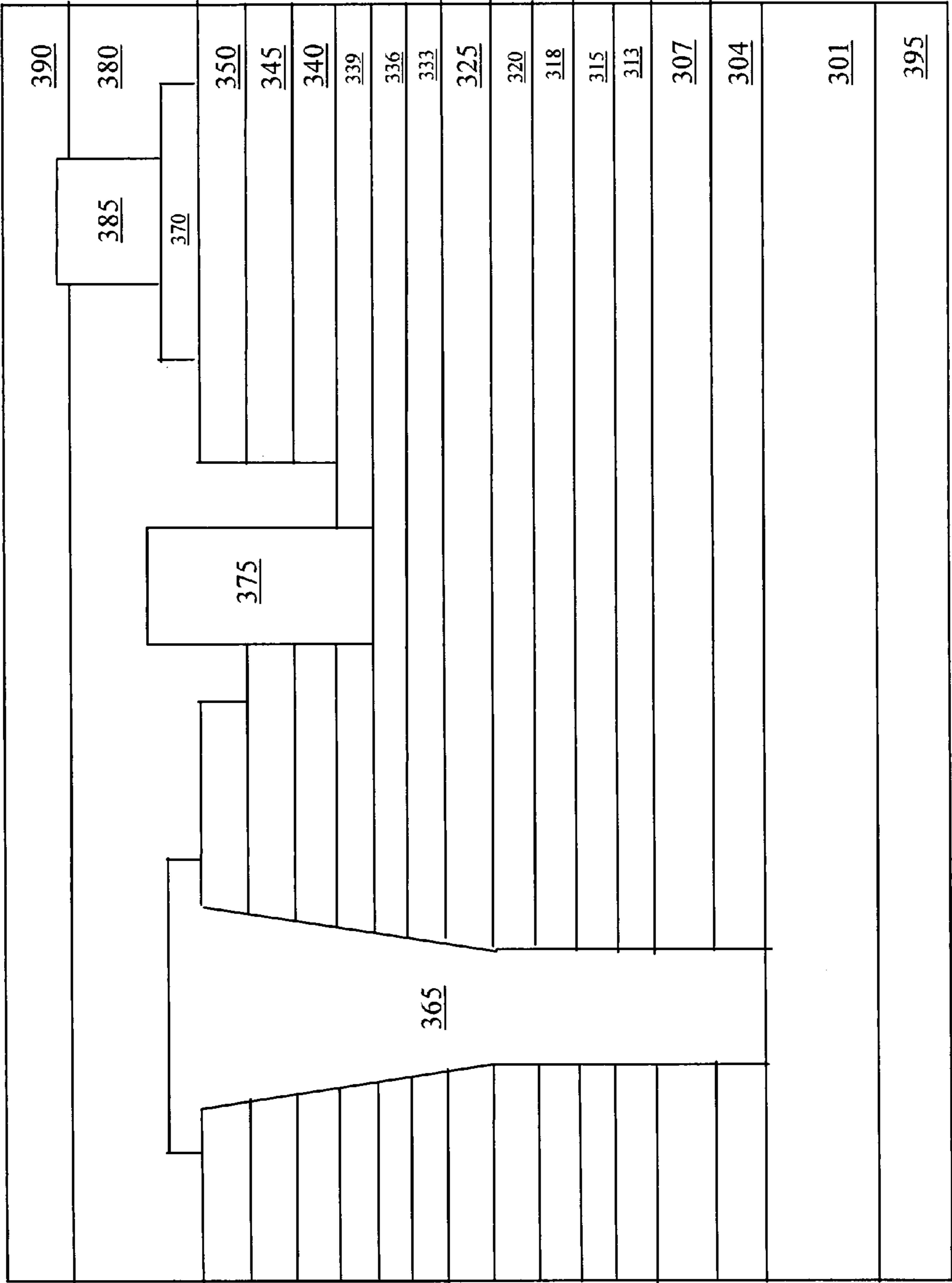


FIGURE 21

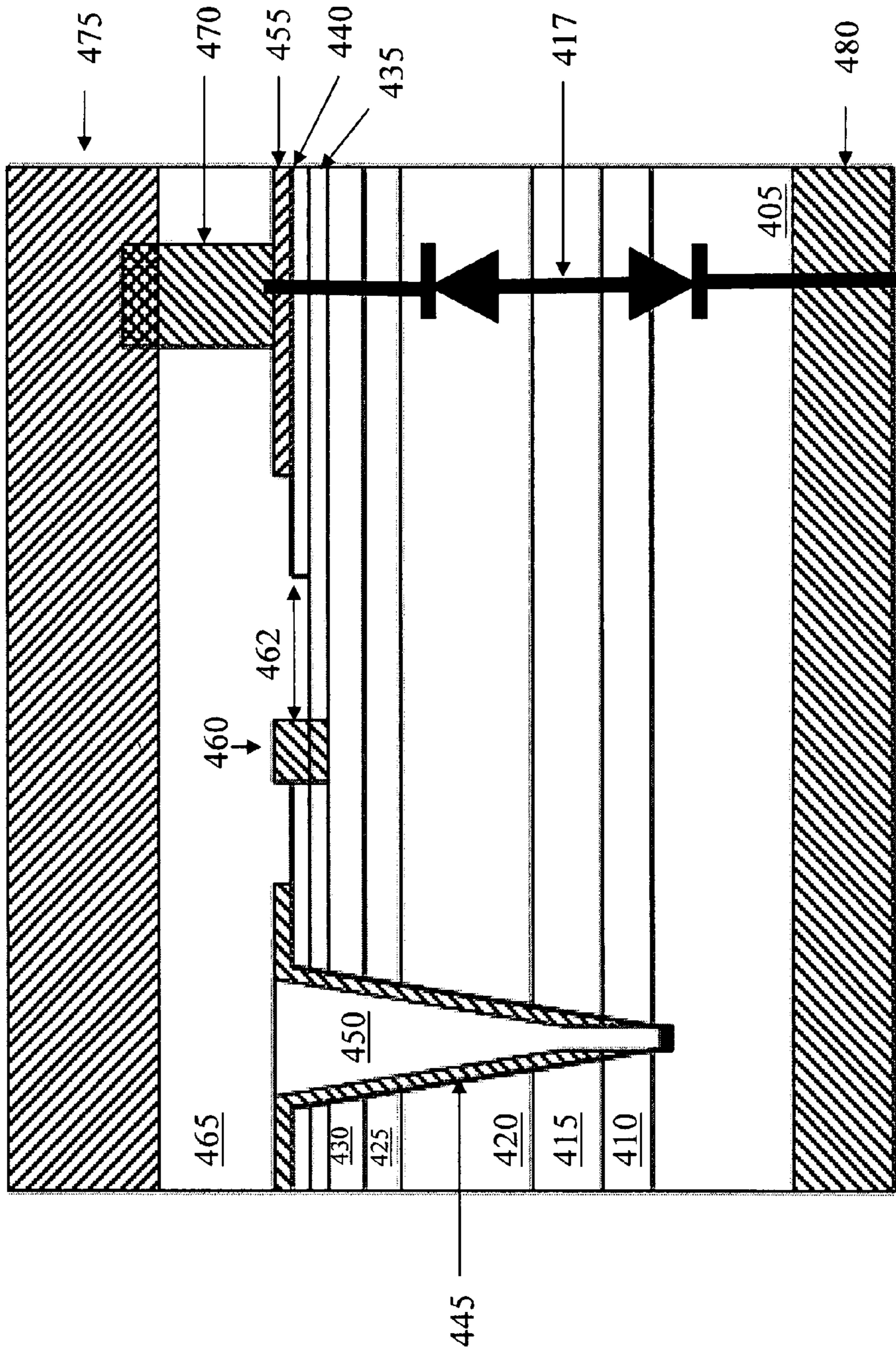


FIGURE 22

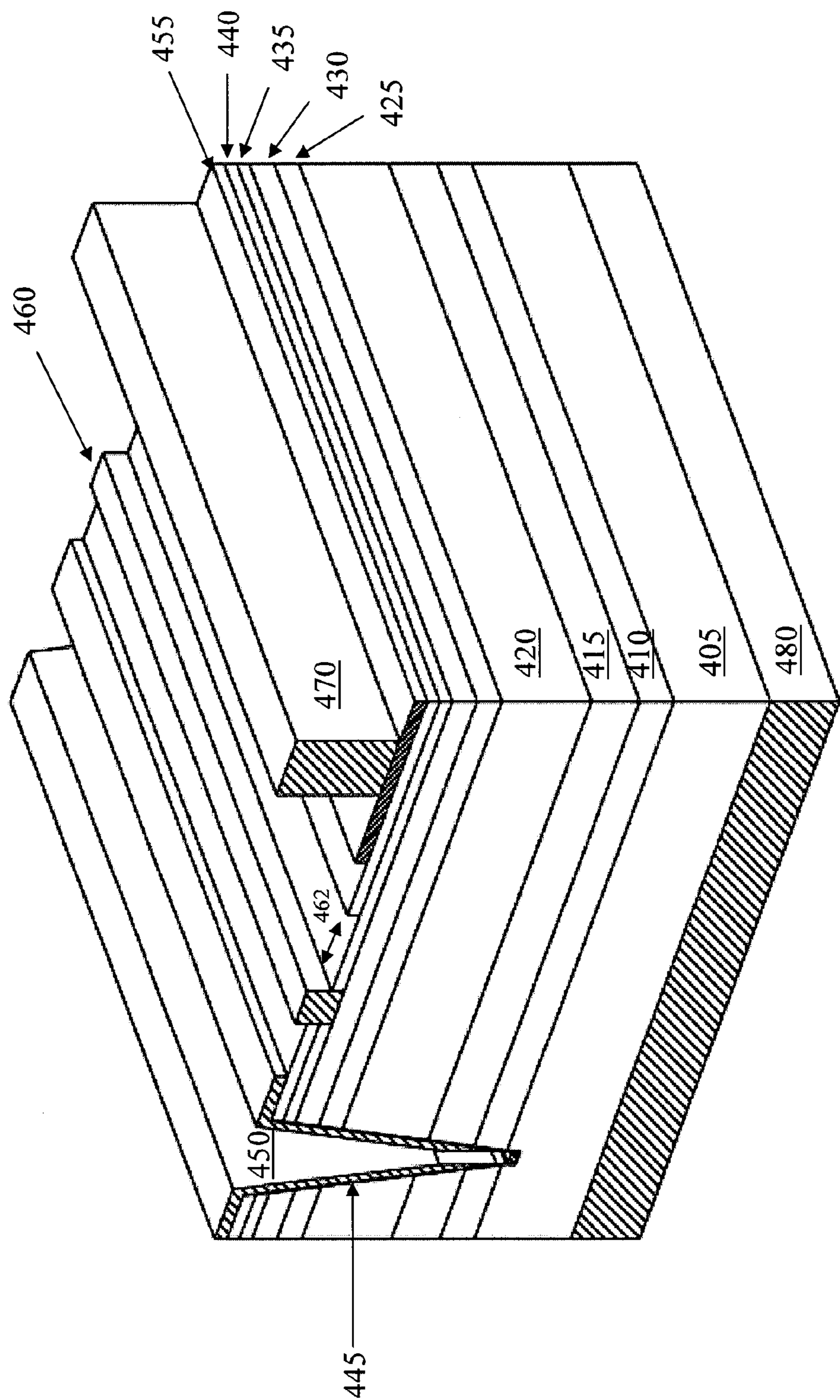


FIGURE 23

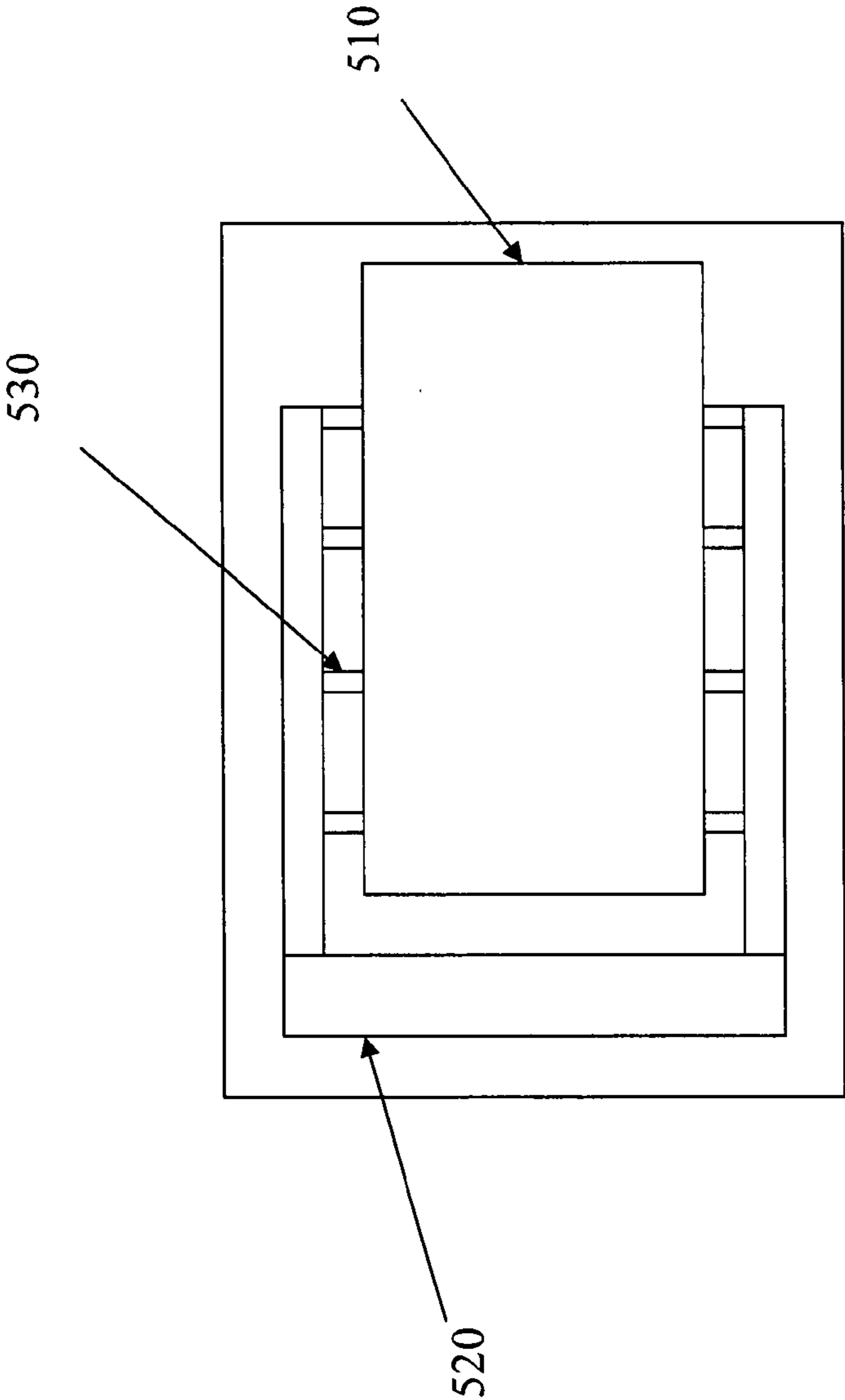


FIGURE 24

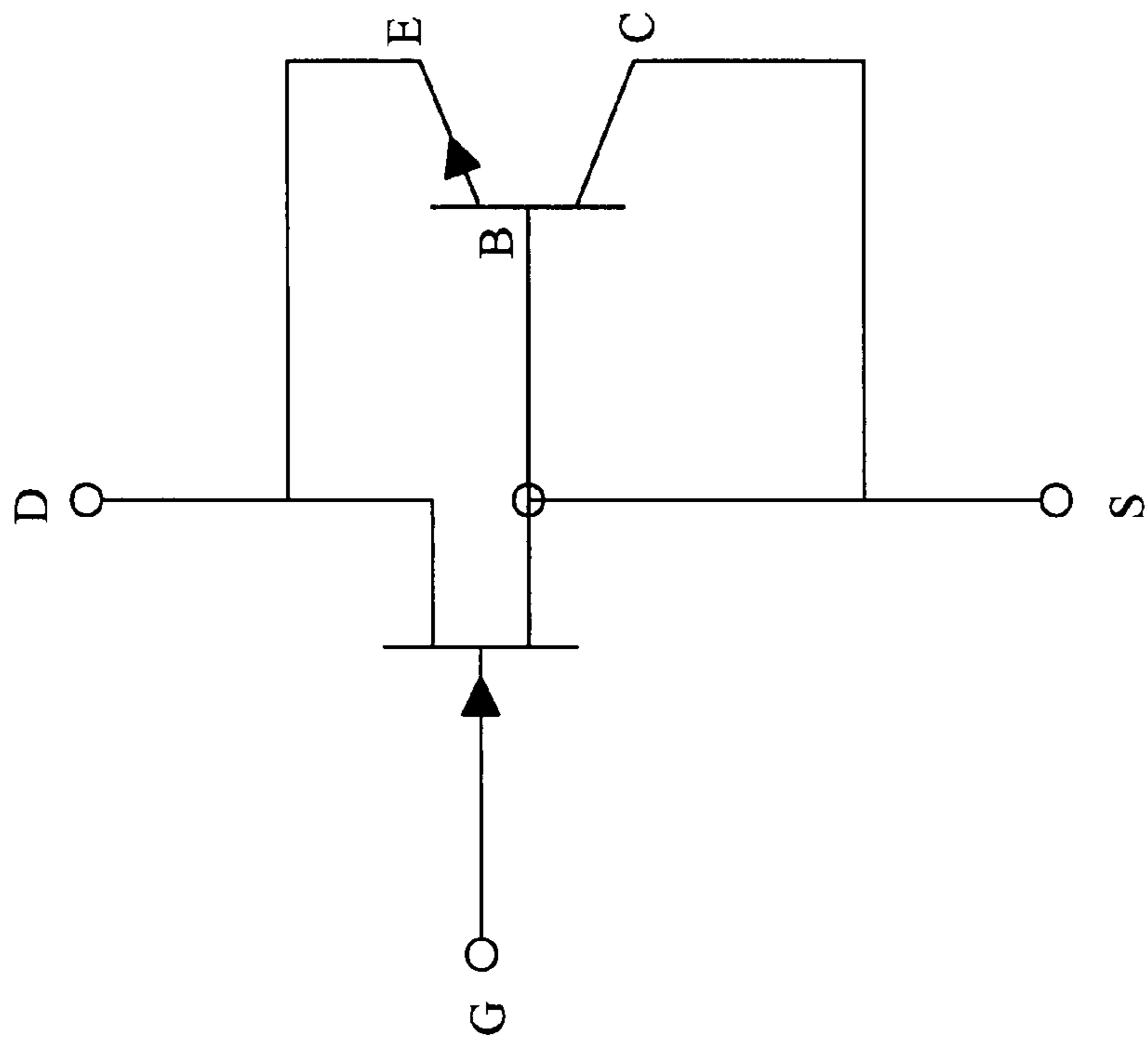


FIGURE 25

FIGURE 26A

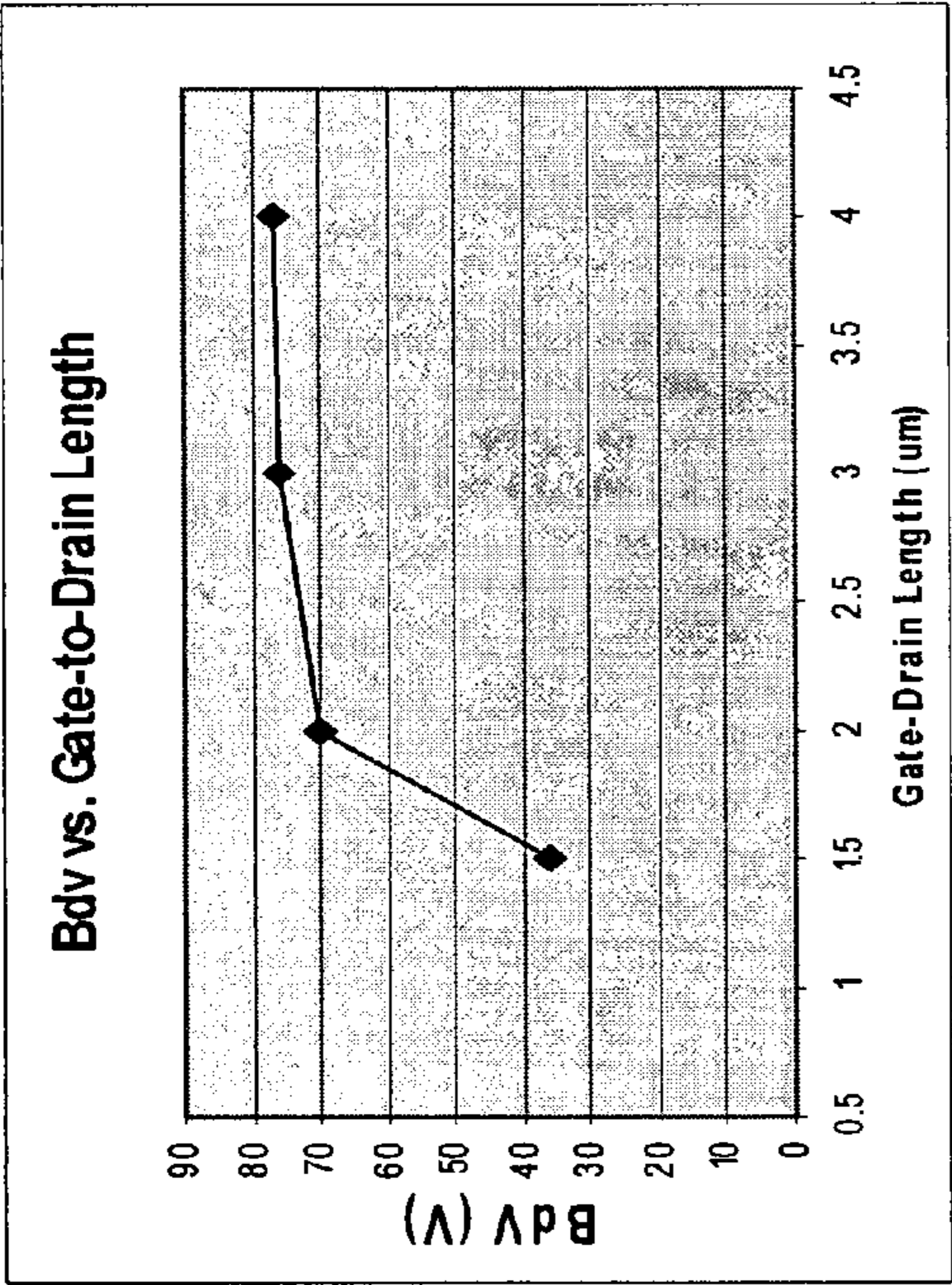


FIGURE 26B

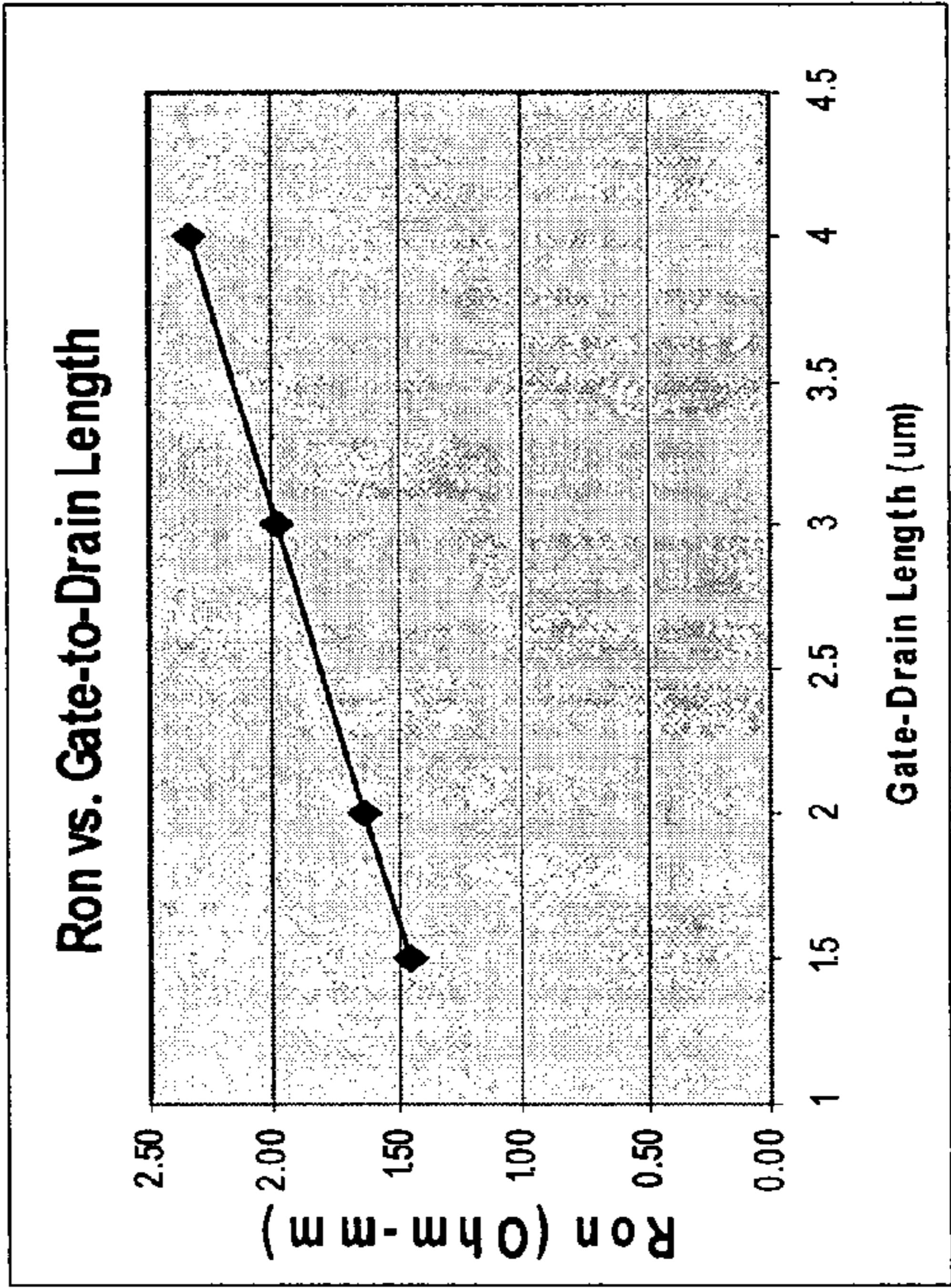


FIGURE 26C

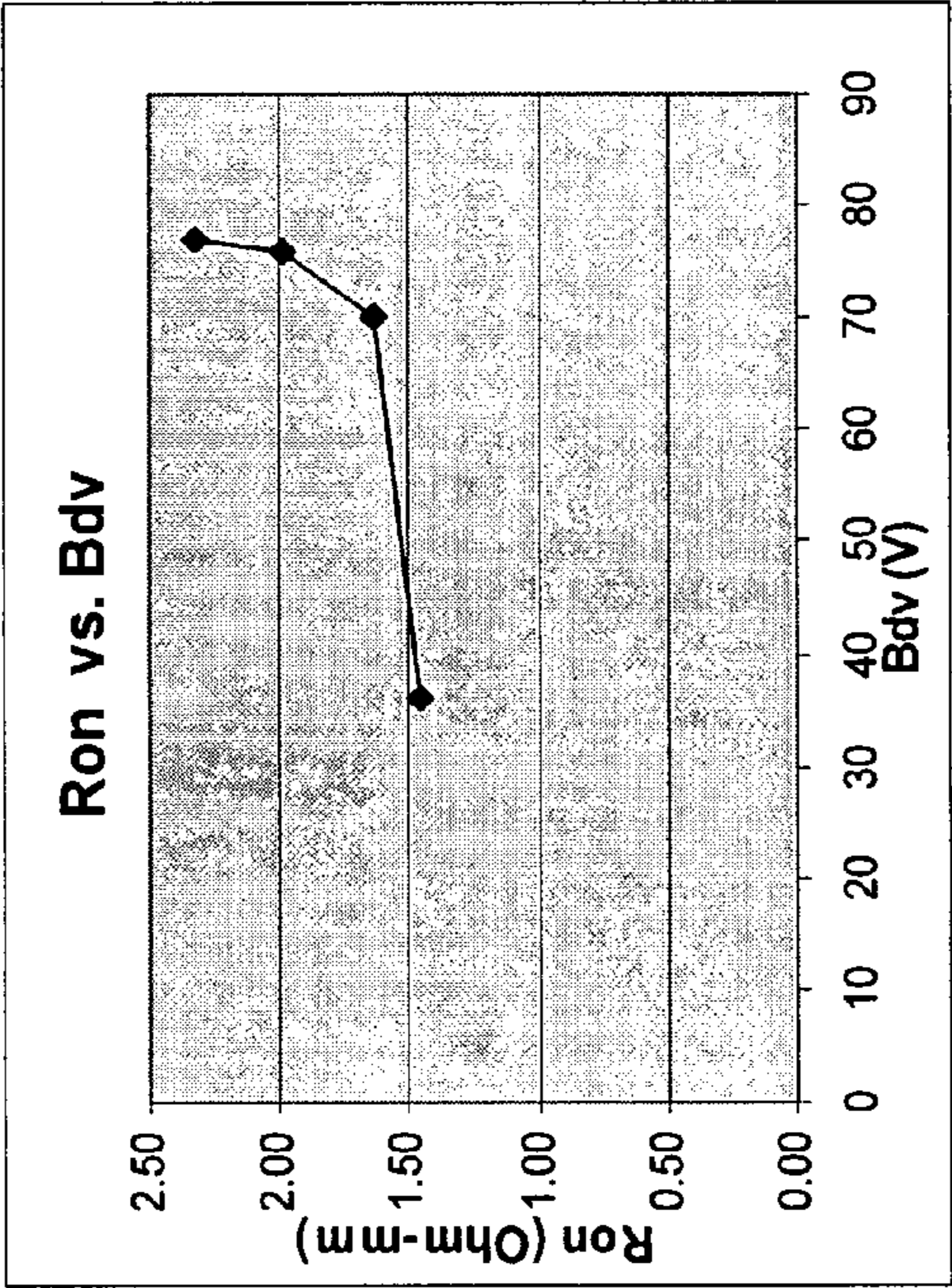


FIGURE 27A

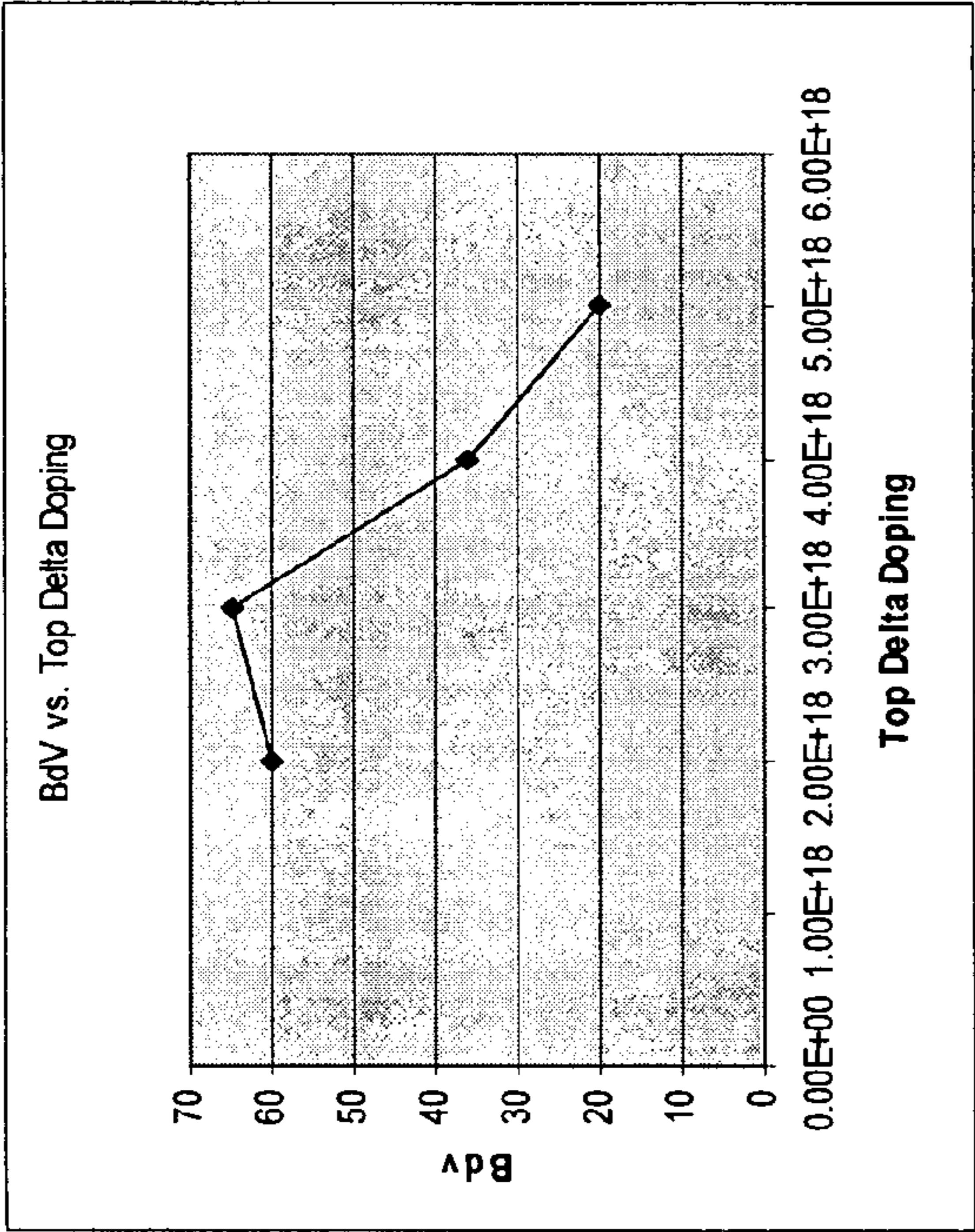


FIGURE 27B

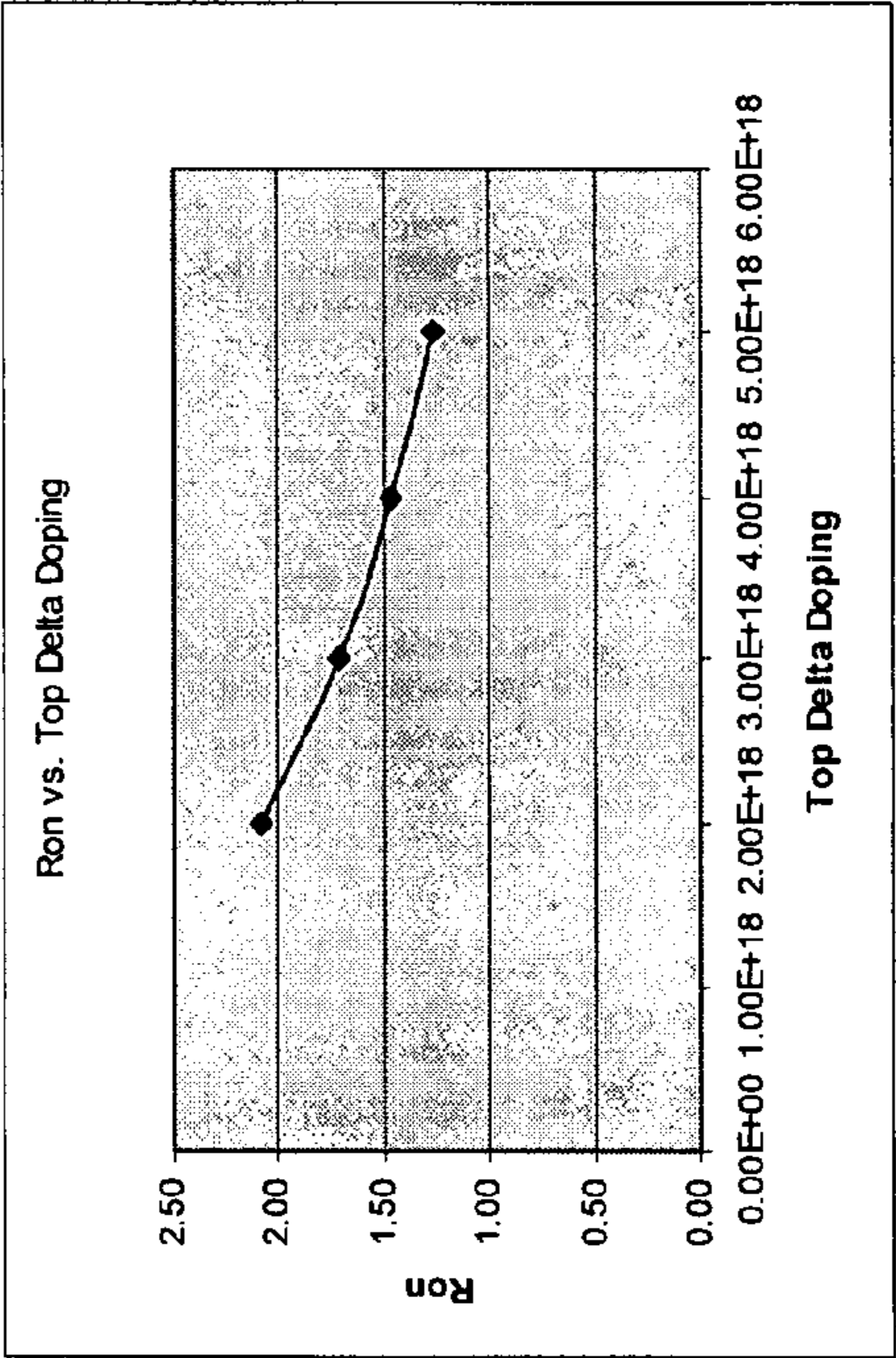
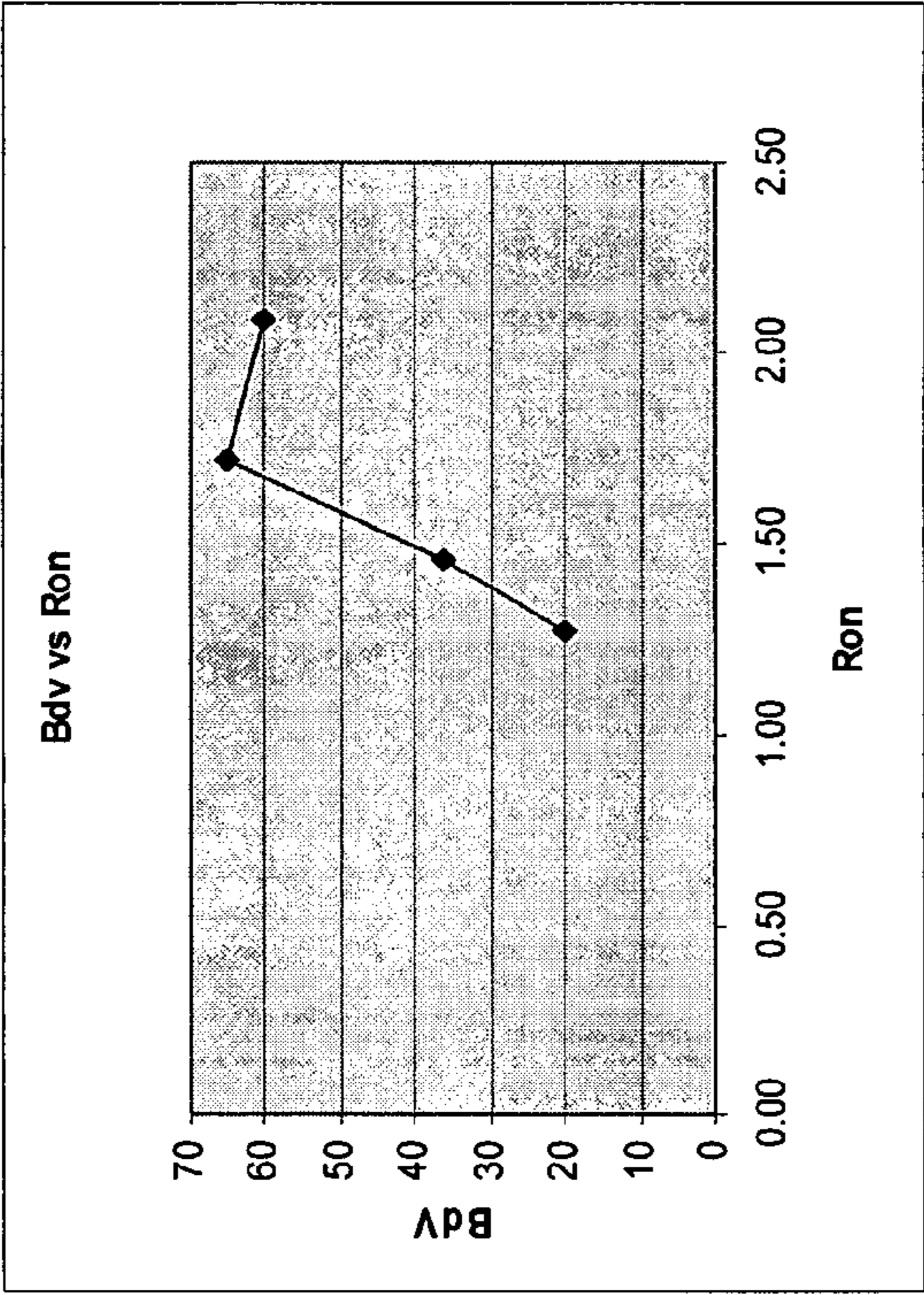


FIGURE 27C



HIGH VOLTAGE SEMICONDUCTOR DEVICE HAVING A LATERAL CHANNEL AND ENHANCED GATE-TO-DRAIN SEPARATION

[0001] This application is a continuation in part of, and claims priority to, U.S. patent application Ser. No. 11/094,632, entitled "Semiconductor Device Having A Lateral Channel and Contacts on Opposing Surfaces Thereof," filed on Mar. 29, 2005, which is incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention is directed, in general, to semiconductor devices and, more specifically, to a semiconductor device having a lateral channel and enhanced gate-to-drain separation and method of forming the same.

BACKGROUND

[0003] A field-effect transistor (also referred to as a "FET") is a conventional semiconductor device employable in switch-mode power supplies for use in data processing and telecommunication systems as well as for other applications that use conditioned power for operation of sensitive electronic circuits. The field-effect transistors have almost universally replaced bipolar transistors previously used for inverters (a type or portion of a power supply) as well as the p-n and Schottky diodes used for rectification. The proliferation of field-effect transistors has, at least in part, been driven by the need to provide highly efficient power supplies with low dc output voltages such as five volts or less at higher current levels. The broad acceptance of field-effect transistors for the aforementioned applications is a consequence of the low forward voltage drop and fast switching speed as well as the low power consumption employed to enable or disable conduction thereof. As a result, the use of field-effect transistors has contributed to compact and efficient power supplies that can be produced at low cost.

[0004] As the loads for the power supplies are generally designed with integrated circuits employing shrinking feature sizes for the circuit elements, a need is continually evolving for new designs with lower output voltages (e.g., one volt or less) at higher current levels (e.g., 50 to 100 amperes or more). In addition, there is a growing need to provide bus voltages of the order of 12 volts or more which require peak reverse voltage ratings of the rectifying circuit elements of 60 volts or more. Present switch-mode power supplies providing input-output circuit isolation (via a transformer) and employing silicon-based field-effect transistors as synchronous rectifiers therein and designed with best current practice are usually operable with switching frequencies only up to several hundred kilohertz ("kHz") due, at least in part, to the slower switching speeds of the silicon-based field-effect transistors. To accommodate continuing developments in integrated circuit technology, however, the power supply switching frequencies above one megahertz ("MHz") are desirable to reduce the size of magnetic devices and the capacitive filtering elements of the power supply without compromising the power conversion efficiency. In accordance therewith, field-effect transistors with previously unrealizable characteristics are not only being requested, but are necessary to satisfy these conditions.

[0005] A material of choice for high performance field-effect transistors is a semiconductor with high electron mobility and wide band gap for high breakdown voltage that

is capable of being processed with conventional equipment and methods not substantially different from those already developed for silicon and present generations of compound semiconductors. A particularly desirable material is the compound semiconductor known as gallium arsenide ("GaAs"), which has been used for integrated circuits operable at frequencies well above one gigahertz, and which has been used to produce power field-effect transistors with high performance characteristics. An exemplary performance of gallium arsenide in comparison to other semiconductor materials for high performance field-effect transistors is described in "Fundamentals of III-V Devices" by W. Liu, published by John Wiley and Sons (1999), and "Modern GaAs Processing Methods" by R. Williams, published by Artech House (1990), which are incorporated herein by reference. Gallium arsenide is an attractive semiconductor alternative to silicon due to its higher electron mobility (8500 cm²/V·sec for GaAs vs. 1400 for Si) and its higher breakdown voltage (400 kV/cm for GaAs vs. 300 for Si).

[0006] Additionally, examples of gallium arsenide field-effect transistors employing a controllable vertical channel between a source and drain thereof with limited performance are provided in the following references, namely, U.S. Pat. No. 5,889,298 entitled "Vertical JFET Field Effect Transistor," by Plumton, et al., issued on Mar. 30, 1999, U.S. Pat. No. 5,342,795 entitled "Method of Fabricating Power VFET Gate-Refill," by Yuan, et al., issued on Aug. 30, 1994, U.S. Pat. No. 5,468,661 entitled "Method of Making Power VFET Device," by Yuan, et al., issued on Nov. 21, 1995, U.S. Pat. No. 5,610,085 entitled "Method of Making a Vertical FET using Epitaxial Overgrowth," by Yuan, et al., issued on Mar. 11, 1997, and U.S. Pat. No. 5,624,860 entitled "Vertical Field Effect Transistor and Method," by Plumton, et al., issued on Apr. 29, 1997, which are incorporated herein by reference.

[0007] An exemplary gallium arsenide field-effect transistor as generally described in the aforementioned references is illustrated with respect to FIG. 1. The gallium arsenide field-effect transistor includes buried and inter-coupled gate fingers (also referred to as a gate and one of which is designated 110) formed in etched trenches in an n-doped drain 120 thereby producing vertical channels 130. The gates 110 exhibit a gate length (generally designated "GL") and the vertical channels 130 provide a channel opening (generally designated "CO"). The trenches are back-filled epitaxially with p-doped gallium arsenide to form the gates 110. A p+ implant 140 provides a top surface contact to the gates 110, and is made through a further n-doped epitaxial layer that forms a source 150. External connection to the gates 110 is made through metallized contacts 160 deposited over the heavily doped p+ implants 140. An external source contact 170 and drain contact 180 are made through metal depositions over further heavily doped areas. The structure produces vertical field-effect transistor channels between the gates 110, and provides source and drain contacts 170, 180, respectively, on opposing sides of the die. The device, therefore, operates with vertical carrier flow and the buried gates 110, typically doped opposite from the vertical channels 130, exhibit limited control over a fill profile thereof.

[0008] Thus, the field-effect transistor as described above does not accommodate a careful doping profiling and epitaxial layer design necessary to produce a modulation-doped channel that can be formed in a lateral channel and that may

be employed to substantially reduce the on-resistance of the device. The field-effect transistor described above is not configured with a channel having a strained material which significantly improves a mobility of the current carrying carriers and, consequently, a switching speed thereof. This design methodology of constructing such gallium arsenide field-effect transistors has been analyzed in the following references, namely, "Comparison of GaAs and Silicon Synchronous Rectifiers in a 3.3V Out, 50 W DC-DC Converter," by V. A. Niemela, et al., 27th Annual, IEEE Power Electronics Specialists Conference, Vol. 1, June 1996, pp. 861-67, "10 MHz PWM Converters with GaAs VFETs," by R. Kollman, et al., IEEE Eleventh Annual Applied Power Electronics Conference and Exposition, Vol. 1, March 1996, pp. 264-69, "A Low On-Resistance High-Current GaAs Power VFET," by D. L. Plumton, et al., IEEE Electron Device Letters, Vol. 16, Issue 4, April 1995, pp. 142-44, and "RF Power Devices for Wireless Communications," by C. E. Weitzel, IEEE MTT-S2002, paper TU4B-1, which are incorporated herein by reference. The structure as generally described in the aforementioned references has higher channel and gate resistance per unit die area than the desired resistance and produces a device operable only in the depletion mode, which may limit the applicability of the device in certain situations. Additionally, the devices described in the aforementioned references do not include an intrinsic body diode. The resulting cost and performance have resulted in limited marketability in view of the presently available silicon-based technology.

[0009] Another example of a vertical channel gallium arsenide field-effect transistor is described in "Manufacturable GaAs VFET for Power Switching Applications," by K. Eisenbeiser, et al., IEEE Electron Device Letters, Vol. 21, No. 4, pp. 144-45 (April 2000), which is incorporated herein by reference. The reference describes forming a source contact on a top surface of the die and a drain contact on the bottom. A vertical channel, however, is still provided in the design proposed by Eisenbeiser, et al. Although economies of manufacture are achieved using implants rather than etching and epitaxial growth as described by Eisenbeiser, et al., possible disadvantages of a channel with a vertical structure limit the switching speed and operation as an enhancement-mode device.

[0010] R. Williams describes a GaAs power field-effect transistor in "Modern GaAs Processing Methods," incorporating both the source and drain contacts on the upper side of a die with a lateral channel and is illustrated with respect to FIG. 2A. The gallium arsenide field-effect transistor acting as a power field-effect transistor includes a gate **205** interposed between a source **210** and drain **215**, creating a lateral channel in an n-doped GaAs layer **220**. A depletion region **225** is formed under the gate **205** and a shallower depletion region **230** forms generally under an upper surface of the die as a result of an inherent existence of surface states at the surface of the crystal (i.e., a surface pinning effect). The gallium arsenide field-effect transistor is formed over a semi-insulating GaAs substrate **235**. Designing the source and drain contacts on the same surface of the die requires a complicated multilayer metallization process and results in increased die area and reduced chip yield. The aforementioned configuration can also lead to increased inductance, which is of significance in applications for microwave signal amplification. Also, the gallium arsenide field-effect transistor does not include an intrinsic body diode.

[0011] Another gallium arsenide field-effect transistor is described by R. Williams at pp. 66-67 of "Modern GaAs Processing Methods," which is configured with source and drain contacts on opposing sides of the die and a lateral channel, and is illustrated with respect to FIG. 2B. The gallium arsenide field-effect transistor includes a plated air bridge **250** coupled to a source (generally designated "S") on an upper side of the die. Gates (generally designated "G") are interposed between drains (generally designated "D"), and are also located on the upper surface of the die. Couplings to the source are brought down to a lower surface of the die by vias **265** that are plated-through holes between the lower surface and the source and are further coupled together by a plated heat sink **280**. Although this arrangement can provide low-inductance external connections to the source, it is limited in its ability to provide a low-resistance channel tightly coupled to the lower surface of a highly conductive substrate, or an intrinsic body diode.

[0012] The aforementioned design also does not accommodate large drain contacts desirable for a higher power device, which will increase the resistive and inductive losses. This configuration requires a complex air-bridge processing step, which will increase the cost and potentially affect the reliability of the device. For the large gate width field-effect transistor, the parasitic resistance in series with the source will increase due to the long air-bridge connection. This design also is incompatible with today's packaging techniques for higher power devices embodied in a vertical device configuration.

[0013] Additionally, U.S. Pat. No. 6,309,918 entitled "Manufacturable GaAs VFET Process," by Huang, et al., issued on Oct. 30, 2001, is directed toward a vertical FET with source and drain contacts on opposing sides of a die. U.S. Pat. No. 5,956,578 entitled "Method of Fabricating Vertical FET with Schottky Diode," by Weitzel, et al., issued on Sep. 21, 1999, and U.S. Pat. No. 6,097,046 entitled "Vertical Field Effect Transistor and Diode," by Plumton, issued on Aug. 1, 2000, are directed toward a vertical FET on a compound semiconductor substrate with an integrated Schottky diode on an upper surface of the die. Neither of the aforementioned references, which are also incorporated herein by reference, provides low on-resistance using a conductivity-enhanced lateral channel.

[0014] Still further references such as U.S. Pat. No. 5,068,756 entitled "Integrated Circuit Composed of Group III-V Compound Field Effect and Bipolar Semiconductors," by Morris, et al., issued on Nov. 26, 1991, and U.S. Pat. No. 5,223,449 entitled "Method of Making an Integrated Circuit Composed of Group III-V Compound Field Effect and Bipolar Semiconductors," by Morris, et al., issued on Jun. 29, 1993, which are incorporated herein by reference, describe an integration of multiple semiconductor devices on a die including n- and p-channel junction field-effect transistors with a lateral channel. These devices include an isolation trench surrounding the devices, etched to a lower semi-insulating gallium arsenide layer and backfilled with silicon nitride. The aforementioned devices, however, are configured with contacts on a top surface, which restricts their application from low voltage, high current systems wherein efficiency is an important design element.

[0015] Low on-resistance compound semiconductor field-effect transistors have been enhanced by the use of a layering

structure called modulation doping as described in "Fundamentals of III-V Devices" by W. Liu (pp. 323-330) and "Ultra-High Speed Modulation-Doped Field-Effect Transistors: A Tutorial Review," L. D. Nguyen, et al., Proceedings of the IEEE, Vol. 80, No. 4, pp. 494-518 (April 1992), which are incorporated herein by reference and are particularly applicable to devices with a lateral channel. The objective of modulation doping is to avoid electron scattering in the current conducting channel by ionized impurities due to dopants, which increases channel resistivity due to the decreased carrier mobility. Channel conductivity may be modulated by a separate control element such as a gate that controls channel depletion.

[0016] The modulation doping technique has been developed for lateral channels using, for instance, gallium arsenide as an undoped, narrower band gap channel and including an adjacent, doped, wider band gap layer of aluminum gallium arsenide, which provides an abundant and controllable source of free carriers to the gallium arsenide channel. Other combinations of compound semiconductors can be used, such as an undoped indium gallium arsenide channel and an adjacent, doped aluminum gallium arsenide layer as the source of free carriers. Successful and repeatable applications of modulation doping, which is based on precision formation of a pseudomorphic layer, employs lateral channel arrangements that are not presently available in devices configured with vertical channels.

[0017] An objective in the design of a field-effect transistor formed with a compound semiconductor is reduction of on-resistance while increasing reverse breakdown voltage between a drain and source. One technique for increasing reverse breakdown voltage between the drain and source is described by Y. Tkachenko, et al., in the paper entitled "Improved Breakdown Voltage and Hot-Electron Reliability PHEMT for High Efficiency Power Amplifiers," Asia Pacific Microwave Conference, Vol. 3, Nov. 30, 1999, pp. 618-621, which is incorporated herein by reference. By increasing a recess width on the drain side of a gate, a pseudomorphic high electron mobility transistor ("PHEMT") breakdown voltage was increased and hot electron radio frequency ("RF") stress was reduced by a factor of 2.5 to 3.5 with minor change in saturated on-resistance. Other attempts to increase reverse breakdown voltage between a drain and source employ the use of field plates as described by Ellen Lan, et al., in the paper entitled "A Field Plate Device by Self-Aligned Spacer Process," GaAsManTech Conference, May 3, 2004, pp. 35-38, and by K. Asano, et al., in the paper entitled "Novel High Power AlGaAs/GaAs HFET with a Field-Modulating Plate Operated at 35V Drain Voltage," International Electron Devices Meeting, Dec. 6, 1998, pp. 59-62, which are incorporated herein by reference. Device structures that include drain and source contacts on the same surface of a die, as described by Y. Tkachenko, et al., do not provide sufficiently low on-resistance in an end product application. Structures that include a field plate as described by Ellen Lan, et al., and by K. Asano, et al., necessarily add additional processing steps and their associated costs to a manufacturing sequence.

[0018] Considering the limitations as described above, a field-effect transistor design is not presently available for the more severe applications that lie ahead. Accordingly, what is needed in the art is a gallium arsenide and other compound semiconductor devices configured for wide acceptance, par-

ticularly in low voltage and high current applications as well as higher voltage applications wherein an internal bus such as a 12-volt bus (or higher) is powered, overcoming many of the aforementioned limitations. In accordance therewith, a compact and efficient power supply, particularly for very low voltage and high current loads such as microprocessors, as well as amplifiers for telecommunications and other applications which operate with a higher voltage such as 12 volts or more, would benefit from a robust field-effect transistor without incurring unnecessary costs or the need to commit a substantial portion of the physical volume of the end device to the power supply. A robust field-effect transistor is particularly needed on the secondary side of a dc-to-dc converter that provides a bus voltage. Such a device should be capable of accommodating large, nearly instantaneous drain-gate voltage excursions, which would lead to better device resistance to hot-electron induced device degradation and longer device lifetime.

SUMMARY OF THE INVENTION

[0019] These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by advantageous embodiments of the present invention, which includes a semiconductor device having a lateral channel with contacts on opposing surfaces thereof and a method of forming the same. A semiconductor device having a lateral channel with contacts on opposing surfaces thereof and a method of forming the same. In one embodiment, the semiconductor device includes a conductive substrate having a source contact covering a substantial portion of a bottom surface thereof. The semiconductor device also includes an isolation layer above the conductive substrate, a lateral channel above the isolation layer and a drain contact above the lateral channel. The semiconductor device further includes a gate located in a gate recess interposed between the lateral channel and the drain contact and a drain formed by at least one source/drain contact layer interposed between the lateral channel and the drain contact. The drain is offset on one side of the gate by a gate-to-drain separation distance. The semiconductor device still further includes an interconnect that connects the lateral channel to the conductive substrate operable to provide a low resistance coupling between the source contact and the lateral channel. In an advantageous embodiment, the semiconductor device is capable of sustaining substantial open-circuit drain-to-source breakdown voltage such as 50 volts or more.

[0020] The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] For a more complete understanding of the present invention, and the advantages thereof, reference is now

made to the following descriptions taken in conjunction with the accompanying drawing, in which:

[0022] FIGS. 1, 2A and 2B illustrate cross sectional views of field-effect transistors according to the prior art;

[0023] FIGS. 3 to 21 illustrate cross sectional views of an embodiment of constructing a semiconductor device according to the principles of the present invention;

[0024] FIGS. 22 and 23 illustrate cross sectional and perspective views, respectively, of another embodiment of a semiconductor device constructed according to the principles of the present invention;

[0025] FIG. 24 illustrates a plan view of another embodiment of a semiconductor device constructed according to the principles of the present invention;

[0026] FIG. 25 illustrates an equivalent circuit diagram of a semiconductor device constructed according to the principles of the present invention;

[0027] FIGS. 26A, 26B, and 26C illustrate graphical representations of a dependence of breakdown voltage and on-resistance on a gate-to-drain separation distance of a semiconductor device constructed according to the principles of the present invention; and

[0028] FIGS. 27A, 27B, and 27C illustrate graphical representations of a dependence of breakdown voltage and on-resistance on a top layer delta doping density of a semiconductor device constructed according to the principles of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0029] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0030] The present invention will be described with respect to exemplary embodiments in a specific context, namely, a semiconductor device and, more particularly, a substrate driven FET. A substrate driven FET is configured with a source contact coupled to a substrate and a drain contact coupled to an opposing surface of the device to provide a low on-resistance switch with very fast switching transition times. The substrate driven FET also includes a lateral channel. The principles of the present invention may be applied to a compound semiconductor FET with a modulation-doped lateral channel and other semiconductor devices that include current-carrying, switched terminals on opposing surfaces thereof. Thus, the principles of the present invention apply to semiconductor devices having a lateral channel and contacts on opposing surfaces thereof.

[0031] Exemplary characteristics and advantages associated with the use of selected embodiments of the substrate driven FET according to the principles of the present invention are set forth below. The substrate driven FET may be capable of switching transition times on the order of nanoseconds, rather than switching transition times on the order

of 35 to 50 nanoseconds realizable with the present silicon-based technology. The substrate driven FET for low-voltage applications may exhibit peak inverse voltage ratings such as 10 to 20 volts or less and should have low on-resistance including the parasitic electrical resistance from the device packaging approaching one milliohm or less. In higher voltage applications, the substrate driven FET may exhibit a peak inverse voltage rating of 80 volts or more. In addition, the substrate driven FET desirably has gates that can be driven with digital logic, with low gate charge and correspondingly low and controllable field-effect transistor threshold voltage. The substrate driven FET also desirably has current ratings of at least a dozen amperes, and should be cost competitive with presently available field-effect transistors having similar power ratings implemented in silicon-based technology. The substrate driven FET also desirably includes an intrinsic body diode that is capable of conducting substantially the full rated device current.

[0032] Additionally, the substrate driven FET having source and drain contacts on opposing sides of the die facilitates low resistance and inductance packaging by providing more area for the contacts. The substrate driven FET may also operate as an enhancement-mode device which implies a normally-off device when a gate voltage is substantially zero volts to avoid short circuits during power supply start-up. The presence of an intrinsic body diode with the anode coupled to a source interconnect and source contact can also provide substantial benefits in circuit design as well as cost reduction, particularly in power supply applications.

[0033] In the drawings, boundaries may be shown as lines to separate semiconductor regions or layers with apparent abrupt changes in doping levels or species. It is recognized that semiconductor manufacturing processes such as implantation and diffusion may cause doping concentrations and atomic species to vary in a continuous and sometimes gradual manner across a semiconductor device. Consequently, graded boundaries of device regions may be shown as lines in the drawings for explanatory purposes without compromising an understanding of the structure of the devices.

[0034] Many steps conventionally used to process a gallium arsenide (also referred to as "GaAs") die or wafer and other compound semiconductors as described herein are well known in the art, and, in the interest of brevity, will not be described in detail. The basic steps include, for example, molecular-beam epitaxy, metal-organic chemical vapor deposition, patterning, exposing, etching, vacuum depositing, plating, doping, alloying, annealing, and cleaning. For reference purposes, R. Williams describes many conventional processes for constructing a gallium arsenide device in "Modern GaAs Processing Methods." Additionally, several separate processing steps may be generally combined into a single step within the scope of the present invention, such as a combined annealing step wherein a number of alloys that are separately deposited are heated together to jointly activate the alloys. Further, alternative methods to perform a processing step such as vacuum deposition, sputtering, or plating processes may be combined or performed separately without further elaboration herein. Also, while selected doping levels and characteristics such as thickness of layers that make up an exemplary substrate driven FET will hereinafter be provided, those skilled in the art under-

stand that alternative doping levels and characteristics may be provided and still be within the broad scope of the present invention. For instance and in the appropriate circumstances, the layers may be oppositely doped, such as a p-type layer may be replaced with an n-type layer.

[0035] A description of an embodiment of a semiconductor device constructed according to the general principles of the present invention will hereinafter be provided. Thereafter, a description of semiconductor device design enhancement to provide higher breakdown voltage with minimal increase in device on-resistance will be given.

[0036] Referring now to FIGS. 3 to 21, illustrated are cross sectional views of an embodiment of constructing a semiconductor device (e.g., substrate driven FET), particularly for a lower-voltage application, according to the principles of the present invention. Beginning with FIG. 3, the substrate driven FET is formed on a substrate (e.g., GaAs substrate) 301. Preferably, the substrate 301 is n-doped and is a highly conductive layer (e.g., a conductive substrate) with a doping level in the range of 7×10^{17} to $5 \times 10^{18} \text{ cm}^{-3}$. The substrate 301 may be chosen to be sufficiently thick to provide mechanical and chemical support for semiconductor processing and handling, and may be supported by a further underlying medium. The substrate 301 provides a source connection for the substrate driven FET, accommodating a low-resistance connection over a substantial portion of the lower surface thereof. Ranges of doping levels, layer thicknesses, etc., including preferred values are provided here and hereinbelow to indicate exemplary ranges of variations for a device design, and are not intended to limit thereby the broad scope of the present invention.

[0037] A preferred n-type doping material for GaAs is silicon ("Si"), but selenium ("Se"), tellurium ("Te") or other doping materials or combinations thereof may be employed within the broad scope of the present invention. Although the substrate driven FET described herein is GaAs based, alternative semiconductor materials may be employed to form the substrate 301 such as a semiconductor material based on indium-phosphide ("InP") as well as oppositely doped semiconductors with essential properties of related materials appropriately altered.

[0038] Turning now to FIG. 4, above the substrate 301 is a first buffer layer (e.g., an n+ epitaxial buffer layer) 304 that is preferably grown via molecular beam epitaxy or metal-organic chemical-vapor deposition to a thickness of about 3000 angstroms ("Å"). A suitable n-type doping material such as Si may be employed, but alternatively Se, Te or other n-type dopant or combination thereof may be employed in the epitaxial growth process. A preferred doping density is in the range of 7×10^{17} to $5 \times 10^{18} \text{ cm}^{-3}$. The addition of the first buffer layer 304 generally provides a more uniform crystal structure for further epitaxial depositions than an ordinary, doped GaAs substrate 301, and thus may be optionally included for the formation of the above layers for improved device characteristics.

[0039] Turning now to FIGS. 5 and 6, above the first buffer layer 304 is an isolation layer (e.g., a p-doped isolation layer) 307 that is epitaxially grown and formed sufficiently thin to prevent substantial recombination of minority carriers that might be injected therein during certain modes of operation of the substrate driven FET. A preferred thickness of the isolation layer 307 is approximately 1000 Å and a

preferred dopant is carbon with a doping density between about $5 \times 10^{18} \text{ cm}^{-3}$ to $5 \times 10^{19} \text{ cm}^{-3}$. A thickness of the isolation layer 307, however, can range from about 300 Å to 2000 Å and beyond, and may be deposited with a doping density roughly inversely proportional to the layer thickness.

[0040] The isolation layer 307 forms a pair of back-to-back diodes with n-doped layers formed thereabove and the buffer layer 304 to substantially block current flow when the substrate driven FET is in a non-conducting state, particularly when a positive voltage is applied between the drain and source contacts thereof. The design parameters for the layers above the isolation layer 307 elicit engineering trade-offs and should be chosen to preserve a lifetime of the minority carriers (i.e., electrons) injected therein so that the minority carriers diffuse through the substrate driven FET with sufficiently limited recombination. Additionally, the above-referenced layers should be designed to provide a high degree of conductivity for the substrate driven FET, limit a breakdown, and limit the internal fields when the layer(s) above the isolation layer 307 act as the cathode for the back-to-back diodes, thereby providing reverse voltage blocking capability. Also, the layers above the isolation layer 307 of the substrate driven FET should be provided to enhance a performance thereof such as sustaining a high drain-to-source voltage (e.g., 20 volts) when the substrate driven FET is in a non-conducting state and to provide support for a lateral channel formed thereover.

[0041] A first spacer layer 313 is a thick, but lightly doped p-type GaAs layer that is epitaxially deposited preferably at about 10000 Å and preferably lightly doped to about $1 \times 10^{15} \text{ cm}^{-3}$ above the isolation layer 307. The thickness of the first spacer layer 313 may be increased and its doping density decreased to provide a higher breakdown voltage as described later hereinbelow. The first spacer layer 313 limits an internal electric field within the substrate driven FET and helps to limit breakdown when the substrate driven FET is transitioned to a non-conducting state. As a result, an applied voltage is substantially blocked between the source and drain terminals thereof. The first spacer layer 313 is lightly doped and sufficiently thick, such as 5000 Å to 25000 Å or more, to provide a sufficiently high voltage blocking capability for the substrate driven FET. Different layer thickness ranging from 5000 Å to 25000 Å and doping levels such as $1 \times 10^{15} \text{ cm}^{-3}$ (or less) to $5 \times 10^{16} \text{ cm}^{-3}$ (or more) may be used depending on, for example, the appropriate level of voltage blocking necessary for the substrate driven FET. An undoped layer or a lightly doped n-type layer can also be used in place of the lightly doped p-type layer.

[0042] A second buffer layer 315 located above the first spacer layer 313 is an alternating aluminum-gallium arsenide/gallium arsenide ("AlGaAs/GaAs") super-lattice buffer that is sequentially deposited epitaxially to improve the smoothness of the surface of the crystal and to increase the mobility of the electrons in the channel to be formed thereabove. The presence of aluminum may also act as a "getter" to capture and disable oxygen atoms that may otherwise be present in the subsequent growth. The second buffer layer 315 is deposited preferably with ten alternating layers of AlGaAs (0.24 Al), preferably about 185 Å thick, and GaAs, preferably about 15 Å thick. The total thickness of the second buffer layer 315 is approximately 2000 Å.

[0043] A first barrier layer 318 located above the second buffer layer 315 is an AlGaAs (0.24 Al) bottom barrier/

spacer that is epitaxially deposited at approximately 400 Å to substantially block the free carriers from flowing down to the layers therebelow. An n-pulse doping with Si (“delta doped”), preferably to a level of about 1×10^{12} cm^{-2} to 3×10^{12} is thereafter performed thereon to supply the free carriers to the channel thereabove by the mechanism of modulation doping. A second spacer layer 320 [e.g., a substantially undoped AlGaAs (0.24 Al) spacer] is then epitaxially deposited at approximately 40 Å above the first barrier layer 318 to separate the effects of dopants from the channel, thereby separating the free carriers from the ionized sites and improving the electron mobility therein.

[0044] The isolation layer 307, therefore, lies between n-doped layers, thereby forming the back-to-back diodes that provide an isolation capability for the substrate driven FET. During transient conditions lasting perhaps a nanosecond when the substrate driven FET is transitioned to a non-conducting state, however, a cloud of free electrons positioned above the isolation layer 307 is not able to substantially recombine therein. The effect is to enable a brief period of conduction in the parasitic n-p-n transistor wherein the n-doped layer above forms the emitter, the p-doped layers form the base, and the n-doped layer below forms the collector. The resulting parasitic transistor is able to shunt current between the source and the drain during transient conditions when, for instance, the substrate driven FET is transitioned to a non-conducting state. When the overlying electron gas is dissipated after the brief transient conditions, the parasitic transistor transitions to a non-conducting state.

[0045] Turning now to FIG. 7, above the second spacer layer 320 is a thin, indium-gallium arsenide (“InGaAs”) layer that is epitaxially deposited with about 20% indium to form a lateral channel 325 with controllable conductivity. The second spacer layer 320 may be undoped or doped to increase the channel conductivity. Due to the substantial lattice mismatch between GaAs and InGaAs, the lateral channel 325 is inherently lattice-strained (i.e., it is “pseudomorphic”) and is preferably less than about 120 Å to prevent lattice dislocations and formation of polycrystalline structure in the layers to be deposited thereabove. The channel may be doped to a level of 1.5×10^{17} cm^{-3} and is preferably undoped. The lattice-strained channel provides higher carrier mobility owing to a reduced effective mass of the carriers. The lateral channel 325 provides the controllable conduction mechanism between the source and drain of the substrate driven FET and provides a modulation-doped channel with reduced crystalline irregularities for the free carriers supplied by adjacent layers.

[0046] Turning now to FIG. 8, above the lateral channel 325 is another region that is epitaxially deposited including sub-layers of AlGaAs (0.24 Al) to provide additional free carriers (electrons) for modulation doping of the lateral channel 325, and to provide a barrier for the free carriers in the lateral channel 325. A third spacer layer 333 is undoped and deposited at about 40 Å to provide a spacer layer separating the free carriers in the lateral channel 325 from ionized impurity sites. A second barrier layer 336 (embodied in an undoped AlGaAs layer) is then epitaxially deposited at about 210 Å with an n-doping level in the range of 1×10^{17} to 5×10^{17} cm^{-3} or undoped. In between the third spacer layer 333 and the second barrier layer 336, a n-pulse doping with Si (“delta doped”), preferably to a level of about 3×10^{12}

cm^{-2} , is performed to induce additional free electrons with enhanced mobility that migrate across the third spacer layer 333 to the lateral channel 325.

[0047] Thus, modulation doping is preferably achieved by separating the channel-conduction carriers from the carrier-contributing donor atoms located in the Si-pulsed areas. The carrier mobility in the lateral channel 325 is thereby improved by providing a conductive path substantially undisturbed by lattice imperfections that would otherwise be affected by in-channel dopants. A recess layer 339 of GaAs is then epitaxially deposited, preferably at about 230 Å and Si-doped with a doping level in the range of 1×10^{17} to 5×10^{17} or undoped.

[0048] Turning now to FIG. 9, an etch-stop layer 340 embodied in a thin aluminum-arsenide (“AlAs”), indium-phosphide (“InP”), or indium-gallium-phosphide (“InGaP”) epitaxial deposition is formed above the recess layer 339. The etch-stop layer 340 provides an etch stop for a later, trench-forming process for GaAs layers to be further deposited and doped thereabove. The etch-stop layer 340 is preferably about 25 Å thick and can be doped n-type with a doping level in the range of 1×10^{17} to 5×10^{18} cm^{-3} or undoped.

[0049] Turning now to FIG. 10, layers of GaAs are epitaxially deposited above the etch-stop layer 340 to form source and drain contact layers for the substrate driven FET. First, a first source/drain contact layer 345 of about 300 Å of an n-doped layer of GaAs is epitaxially deposited, preferably using Si as the dopant with a doping level in the range of 1×10^{17} to 1×10^{18} cm^{-3} . Then, a second source/drain contact layer 350 of about 500 Å of a heavily doped n+ layer of GaAs is epitaxially deposited with a doping level in the range of 1×10^{18} to 1×10^{19} cm^{-3} to improve formation of ohmic contacts for the source and drain and to reduce resistance in the source-to-gate and drain-to-gate regions of the channel.

[0050] Turning now to FIGS. 11 to 15, illustrated are cross sectional views of an embodiment of constructing a source interconnect through the substrate driven FET in accordance with the principles of the present invention. The source interconnect is configured to create a low-resistance ohmic contact between the lateral channel 325 and the substrate 301. A spun-on photoresist 355 is illustrated with respect to FIG. 11 that has been masked, exposed and developed as is well known in the art to form a trench for access to the layers therebelow. The photoresist 355 is then baked (e.g., reflowed) such as on a hot plate or oven at about 110 to 150 degrees Celsius and in a normal atmosphere, which cures the photoresist 355 and causes a lower surface of the photoresist 355 facing the trench to encroach toward the trench, forming a generally angular aspect to the trench as illustrated with respect to FIG. 12. The angle of the slope in the photoresist 355 can be controlled by modifying a duration and temperature profile of the reflow process as is well understood in the art.

[0051] Turning now to FIG. 13, the portion of the substrate driven FET unprotected by the photoresist 355 is anisotropically dry etched, preferably using an inductively coupled plasma (i.e., an “ICP” dry etch). The anisotropic dry etch forms a source via (or trench) through the layers of the substrate driven FET down to the substrate 301 to create a low-resistance contact between the lateral channel 325 and

the substrate **301**. The non-selective etching may further alter a profile of the photoresist **355**. Gallium arsenide is generally etched faster than the photoresist **355** by the ICP dry etching, producing a general slope in the walls of the trench in exposed portions of the GaAs and can also produce sloping walls in exposed intervening layers (some slopes not shown).

[0052] The etching process is preferably continued for a controlled period of time until the source via is opened to the substrate **301**. Alternatively, a thin etch-stop layer such as a heavily n-doped aluminum oxide or indium-gallium phosphide ("InGaP") layer, both being substantially lattice-matched to the GaAs substrate, can be epitaxially deposited above the substrate **301** to form a barrier to limit the depth of the ICP dry etch. The etch-stop layer should not substantially affect conductivity to the substrate **301**, if it is sufficiently thin and doped and can be subsequently removed. Preferably, an aluminum arsenide etch-stop layer would be about 50-100 Å thick depending on the proscribed etch resistance, but an InGaP layer which has better conductivity could be thicker.

[0053] Turning now to FIG. 14, the walls of the source via should be sufficiently sloped so that a thin metal layer (generally designated **360**) can be deposited on horizontal and semi-horizontal surfaces, preferably by a vacuum evaporation and deposition process. The metal material is anisotropically deposited on to the horizontal surfaces such as the bottom of the source via and on the sloped surfaces. Typically, about 3000-4000 Å of gold ("Au"), germanium ("Ge"), nickel ("Ni"), and then gold are preferably sequentially deposited and annealed to produce an alloy with a low-resistance ohmic contact and good adhesion with the lateral channel **325** and the substrate **301**. A low-resistance ohmic contact is also formed with the first buffer layer **304** located above the substrate **301**. Other alloys such as palladium-germanium-gold, nickel-indium-germanium, palladium-germanium and aluminum-tin-nickel may be employed to advantage. Annealing causes an alloy to form among the metallic species and allows migration of metal into adjacent semiconductor material forming a metal semiconductor eutectic, thereby enhancing its low-resistance, ohmic property.

[0054] Turning now to FIG. 15, an electroplating process is thereafter performed to form a low-resistance source interconnect **365**. The source interconnect **365** is filled with plated platinum and gold. The wafer is dipped into a plating solution and is connected to an electrical current source. A metal material of the plating solution (e.g., either platinum or gold) becomes ionized and is deposited on a conductive surface. The creation of the source interconnect **365** enhances a metallic path between the highly conductive portions of the lateral channel **325** and the substrate **301**. In this manner, a lateral channel **325** between a source contact and a drain contact can be formed and a low-resistance contact to the source (coupled to the lateral channel **325**) can be configured on an opposing surface of the substrate driven FET from a contact for the drain (also coupled to the lateral channel **325**). Alternatively, an implant may be formed to create the source interconnect such as illustrated in U.S. Patent Application Publication No. 2006/0226477, entitled "Substrate Driven Field-Effect Transistor," to Brar, et al., published Oct. 12, 2006, which is incorporated herein by reference. Additionally, for examples of related semicon-

ductor devices, see U.S. Patent Application Publication No. 2006/0255360, entitled "Semiconductor Device Having Multiple Lateral Channels and Method of Forming the Same," to Brar, et al., published Nov. 16, 2006, U.S. patent application Ser. No. 11/211,964, entitled "Semiconductor Device Having Substrate-Driven Field-Effect Transistor and Schottky Diode and Method of Forming the Same," to Brar, et al., filed Aug. 25, 2005, and U.S. patent application Ser. No. 11/236,376, entitled "Semiconductor Device Having an Interconnect with Sloped Walls and Method of Forming the Same," to Brar, et al., filed Sep. 27, 2005, which are incorporated herein by reference.

[0055] Additionally, for examples of power supplies that provide an environment for the vertical FET, see U.S. Patent Application Publication No. 2005/0024179, entitled "Extended E Matrix Integrated Magnetics (MIM) Core," to Chandrasekaran, et al., published Feb. 3, 2005, U.S. Pat. No. 6,775,159, entitled "Switching Power Converter Circuits Providing Main and Auxiliary Output Voltages," to Webb, et al., issued Aug. 10, 2004, U.S. Pat. No. 6,549,436, entitled "Integrated Magnetic Converter Circuit and Method with Improved Filtering," to Sun, issued Apr. 15, 2003, U.S. Pat. No. 7,046,523, entitled "Core Structure and Interleaved DC-DC Converter Topology," to Sun, et al., issued May 16, 2006, U.S. Pat. No. 7,012,414, entitled "Vertically Packaged Switched-Mode Power Converter," to Mehrotra, et al., issued Mar. 14, 2006, U.S. Patent Application Publication No. 2006/0187684, entitled "Power Converter Employing Integrated Magnetics with a Current Multiplier Rectifier and Method of Operating the Same," to Chandrasekaran, et al., published Aug. 24, 2006, U.S. Pat. No. 7,176,662, entitled "Power Converter Employing a Tapped Inductor and Integrated Magnetics and Method of Operating the Same," to Chandrasekaran, issued Feb. 13, 2007, and U.S. Patent Application Publication No. 2006/0198173, entitled "Control Circuit for a Depletion Mode Switch and Method of Operating the Same," to Rozman, published Sep. 7, 2006, all of which are incorporated herein by reference.

[0056] Turning now to FIG. 16, a metal layer **370** is deposited in area associated with the drain, preferably by a vacuum evaporation and deposition process employing a patterned photoresist. The metal layer **370** provides a low-resistance ohmic contact for the drain. The metal layer **370** also provides a plating base for a process of constructing a drain post as set forth below. Additionally, the metal layer **360** described above and the present metal layer **370** may be deposited at the same time by a technique referred to as a metal lift off process. In such a case, a photoresist is spun on the surface and patterned such that an area where the metal is desired gets exposed and the other areas are covered by the photoresist. Metal evaporation is thereafter performed on the patterned wafer. When the wafer is dipped into solvents, the metal on the top of the patterned photoresist gets removed and only the metal on the exposed area remains. With this process, ohmic contacts may be created at the same time.

[0057] Turning now to FIG. 17, the first and second source/drain contact layers **345**, **350** are then patterned and selectively etched to form a wide recess area, to provide a gate-to-drain separation distance as described later herein-below with reference to FIGS. 18 and 19, down to the etch-stop layer **340**. The etch-stop layer **340** is etched by a selective wet etch process. A gate recess is thereafter formed

by patterning and selectively etching through the recess layer **339** down to the second barrier layer **336**. The unetched portion of the recess layer **339** between a gate and drain allows the substrate driven FET to sustain a higher voltage (e.g., 20 volts or more) by reducing a high internal electric field that would otherwise damage or destroy the device. An appropriate etchant or etchants are used for the selective removal of the respective layers as is well understood in the art.

[0058] Turning now to FIGS. **18** and **19**, a gate **375** is patterned and formed preferably by a self-aligned process in the gate recess. An enhanced gate-to-drain separation distance **377** between the gate **375** and drain formed in part by the first source/drain contact layer **345** is illustrated herein. An exemplary gate-to-drain separation distance is 0.2 μm for a lower voltage device and 1.5 μm for a higher voltage device. The drain is, therefore, offset from one side of the gate **375** by the gate-to-drain separation distance **377**. It should be understood that the first source/drain contact layer **345** forms at least a portion of the source and drain on opposite sides of the gate **375** of the substrate driven FET. The gate **375** forms a Schottky junction and is formed with multiple layers, preferably metallic multi-layer titanium-platinum-gold (“TiPtAu”), but other Schottky-junction forming layers such as titanium-tungsten (“TiW”), tantalum-nitrogen (“TaN”), and tungsten-silicon (“WSi”) can also be used within the scope of the present invention. Also, a thin layer providing dielectric surface passivation such as silicon nitride (“Si₃N₄,” not shown) may then be optionally deposited on an upper surface of the substrate driven FET. A dielectric layer **380** is then formed about the substrate driven FET, preferably with a low dielectric constant material (e.g., BCB, polyimide, Si glass, or other flowable oxide) to preserve a performance of the substrate driven FET. The dielectric layer **380** is typically spun on and cured as necessary for planarization and for further surface passivation. The thickness of the dielectric layer **380** can be controlled by a spinning speed and duration. The cured dielectric layer **380** is strong enough to provide mechanical and chemical support for subsequent processing steps.

[0059] Turning now to FIG. **20**, the dielectric layer **380** is then patterned and etched down to the metal layer **370** to form a drain via. An electroplating process is thereafter performed to form a drain post or finger **385**. Analogous to the process for creating the source interconnect **365**, the wafer is dipped into a gold plating solution and ionized gold elements are deposited on an electrical conductive surface. The drain post **385** is a metallic interconnect that forms a wide area, low-resistance interconnect to a top surface of the substrate driven FET. The alternative is to plate the drain post **385** first, apply the dielectric material **380** and etch the dielectric layer **380** down to the top of the drain post **385** using an etch back technique. In addition, this metal interconnect can be formed by metal evaporation and subsequent lift-off process.

[0060] Turning now to FIG. **21**, metallized top and bottom contacts (also referred to as drain and source contacts **390**, **395**, respectively) coupled to the drain post **385** and substrate **301**, respectively, are sequentially deposited and preferably patterned on opposing surfaces (i.e., the top and bottom surfaces, respectively) of the substrate driven FET, preferably using a metallic alloy such as titanium-platinum-gold for the top contact and gold-germanium-nickel-gold

(“AuGeNiAu”) for the bottom contact to form a wide-area, low-resistance, and ohmic junction with the heavily doped n-type GaAs substrate. Prior to creating the source contact **395**, the substrate **301** may be ground and polished down to reduce an electrical and thermal resistance. The deposition process may be performed by vacuum deposition, sputtering, plating processes or combinations thereof. The drain and source contacts **390**, **395** are typically a few microns in thickness to accommodate the packaging process including die attachment and bonding and cover a substantial portion of a top surface of the substrate driven FET and a bottom surface of the substrate **301** (and, thus, the substrate driven FET), respectively.

[0061] As previously mentioned, the isolation layer **307** forms a pair of back-to-back diodes with the buffer layer **304** and the n doped layers thereabove. For instance, an intrinsic body diode is formed with the isolation layer **307** acting as an anode and the first barrier layer **318** and other n-type layers above such as the first and second source/drain contact layers **345**, **350** acting as the cathode. The intrinsic body diode provides a conductive path between the source and drain contacts **390**, **395** of the substrate driven FET. While the back-to-back diodes are formed with an n-p-n structure in the illustrated embodiment, those skilled in the art should understand that other diode structures are well within the broad scope of the present invention.

[0062] Turning now to FIGS. **22** and **23**, illustrated are cross sectional and perspective views of another embodiment of a semiconductor device (e.g., substrate driven FET) constructed according to the principles of the present invention. The substrate driven FET includes a buffer layer **410** overlying a highly conductive gallium arsenide substrate **405**. Above the buffer layer **410** is a p-doped isolation layer **415** that is epitaxially grown and formed sufficiently thin to prevent substantial recombination of minority carriers that might be injected therein during certain modes of operation of the substrate driven FET.

[0063] The isolation layer **415** forms a pair of back-to-back diodes (generally designated **417** in FIG. **22**) at least in part with a region **420** formed thereabove and the buffer layer **410** (both of which include layers or portions thereof that are doped n-type) to substantially block current flow when the substrate driven FET is in a non-conducting state, particularly when a positive voltage is applied between the drain and source contacts thereof. The pair of back-to-back diodes differ from structures that dedicate active die area to build such a structure as illustrated in U.S. Pat. No. 5,956,578 entitled “Method of Fabricating Vertical FET with Schottky Diode,” by Weitzel, et al., issued on Sep. 21, 1999, and U.S. Pat. No. 6,097,046 entitled “Vertical Field Effect Transistor and Diode,” by Plumton, issued on Aug. 1, 2000, which are incorporated herein by reference. The aforementioned references employ structures that increase cost or resistance of the channel because active die area is taken away from the field-effect transistor for use by the diodes. In short, the principles of the present invention create the back-to-back diodes without a separate structure that takes up additional die area or additional footprint beyond the structure of the field-effect transistor. To accommodate the intrinsic body diodes, special attention as described herein should be given to the design of the isolation layer **415** and the layers thereabout. Above the region **420** is a thin, substantially undoped indium-gallium arsenide (“InGaAs”) layer.

layer that is epitaxially deposited with about 20% indium to form a lateral channel **425** with controllable conductivity.

[0064] Above the lateral channel **425** is another region **430** that is epitaxially deposited including sub-layers of AlGaAs (0.24 Å) to provide additional free carriers (electrons) for modulation doping of the lateral channel **425**, and to provide a barrier for the carriers in the lateral channel **425**. An etch-stop layer **435** embodied in a thin, doped AlAs epitaxial deposition is formed above the region **430**. Layers of GaAs are epitaxially deposited above the etch-stop layer **435** to form source and drain contact layers **440** for the substrate driven FET.

[0065] A source via (or trench) through the layers of the substrate driven FET down to the substrate **405** is provided to create a low-resistance contact between the lateral channel **425** and the substrate **405**. The walls of the source via are sufficiently sloped so that a thin metal layer (generally designated **445**) can be deposited on horizontal and semi-horizontal surfaces, preferably by a vacuum evaporation and deposition process. An electroplating process is thereafter performed to form a low-resistance source interconnect **450**. A metal layer **455** is also provided to form a low-resistance ohmic contact for the drain. A gate **460** is thereafter patterned and formed preferably by a self-aligned process in a gate recess in the substrate driven FET. An enhanced gate-to-drain separation distance **462** between the gate **460** and drain formed in part by the source/drain contact layers **440** is illustrated herein.

[0066] A dielectric layer **465** is then formed about the substrate driven FET, preferably with a low dielectric constant material (e.g., BCB, polyimide, Si glass, or other flowable oxide) to preserve a performance of the substrate driven FET and to provide mechanical support for a drain contact thereabove. The dielectric layer **465** is then patterned and etched down to the metal layer **455** to form a drain via. An electroplating process is thereafter performed to form a drain post **470**. Metallized top and bottom contacts (also referred to as drain and source contacts **475**, **480**, respectively) coupled to the drain post **470** and a bottom surface of the substrate **405**, respectively, are sequentially deposited and preferably patterned on the top and bottom surfaces, respectively, of the substrate driven FET. As described with respect to the embodiment of the substrate driven FET above, selected layers of the substrate driven FET may include multiple sub-layers therein to further delineate respective features of the device.

[0067] Turning now to FIG. 24, illustrated is a plan view of another embodiment of a semiconductor device (e.g., substrate driven FET) constructed according to the principles of the present invention. A drain contact **510** of the substrate driven FET provides a wide area surface covering a substantial portion of the die area, enabling a low-resistance contact to the drain. A gate contact **520** with gate extensions **530** contacts a gate of the substrate driven FET. The couplings (not shown) between the gate extensions **530** on a top surface of the die and the gate are made by plated vias through a dielectric layer using well understood masking, patterning, etching and deposition processes. For a more detailed explanation of an embodiment of the drain contact **510**, gate, and dielectric layer, see the description of the substrate driven FET as provided with respect to FIG. 3, et seq. A metallized source contact (not shown) preferably

covers an area of the opposing die surface. Thus, the substrate driven FET with reduced area and low on-resistance is enabled by the device structure and methods of the present invention.

[0068] Turning now to FIG. 25, illustrated is an equivalent circuit diagram of a semiconductor device (e.g., substrate driven FET) constructed according to the principles of the present invention. As described above, the substrate driven FET is formed on a conductive substrate and includes a drain contact D, gate contact G and a source contact S. An n-p-n bipolar transistor (i.e., back-to-back diodes) is formed within the structure of the substrate driven FET and includes an emitter E, a base B and a collector C. The base B and collector C of the n-p-n bipolar transistor are coupled to a source interconnect and source contact therefrom, which provides a short circuit across the base B and collector C. As a result, an intrinsic body diode is formed by the emitter-base junction of the n-p-n bipolar transistor in parallel with the source and drain of the substrate driven FET. Thus, an intrinsic body diode is formed within the substrate driven FET with a cathode coupled to the drain contact D, and an anode coupled to the source contact S. Of course, oppositely doped semiconductor processes can be used to form the substrate driven FET, with corresponding changes to the emitter, base, and collector of the bipolar transistor.

[0069] The substrate driven FET as described above is readily operable as a depletion-mode FET. In other words, the channel is enabled to conduct when substantially zero volts is applied between the gate and source contacts thereof (i.e., for “substantially zero gate voltage”). A depletion-mode device is ordinarily expected to be pinched off with negative gate voltage, relying on the current-blocking character of a gate for negative applied voltage. If the gate voltage is raised above about 0.8 volts positive to further enhance the channel conductivity, then gate current is expected to flow. A modest gate current is not harmful to the operation of the substrate driven FET, and thus the device is ordinarily capable of operation with gate voltage less than about 0.8 volts, or at higher gate voltage with suitable provision to limit the gate current. Exemplary circuits employing depletion mode devices are illustrated and described in U.S. Patent Application Publication No. 2006/0198173, entitled “Control Circuit for a Depletion Mode Switch and Method of Operating the Same,” to Rozman, published Sep. 7, 2006, which is incorporated herein by reference.

[0070] An enhancement-mode device can be produced or provided by several alternatives to the processing steps described hereinabove. For purposes of illustration, any modifications to the processing steps to attain an enhancement-mode device will be described with reference to the substrate driven FET illustrated and described with respect to FIGS. 3 to 21 above. One alternative is to reduce the top delta doping level to a selected level of about $1 \times 10^{12} \text{ cm}^{-2}$ instead of $4 \times 10^{12} \text{ cm}^{-2}$, which reduces the level of the free carriers in the lateral channel that can be used to increase channel resistance several orders of magnitude higher than a depletion-mode design with substantially zero gate voltage. It may not be necessary in practical circuit designs for the substrate driven FET to provide essentially an open circuit when the gate voltage is substantially zero. A careful engineering assessment of the proper doping levels for the layers should be made to determine the best trade-off of

channel resistance for substantially zero gate voltage and the resulting on-resistance of the device for a positive gate voltage. The reduction of free carriers in the portion of the lateral channel outside the region of the gate resulting from reduced pulse doping may raise the on-resistance of the substrate driven FET. This effect can be reduced by selectively implanting the lateral channel with an n-type dopant in regions away from the gate.

[0071] Another alternative to preserve low on-resistance of an enhancement-mode device is to recess the gate through the gate recess closer to or proximate the lateral channel and provide higher pulse doping levels. An etch-stop layer may be selectively formed under the gate to facilitate this option. This approach relies on the recessed gate metal forming a sufficiently deep depletion region in the lateral channel to provide the necessary device resistance for substantially zero gate voltage.

[0072] The substrate driven FET as described above includes an intrinsic body diode with its anode coupled to the source, and cathode to the drain. When the substrate driven FET is conducting, a positive current normally flows from source to drain through the lateral channel. When the lateral channel is not conducting and a negative potential is applied to the drain contact, an ohmic contact between the source interconnect and the buffer and isolation layers couples the respective layers together. The resistance of this ohmic contact can be adjusted by selecting a suitably high doping level for the isolation layer, thus providing an anode connection to the source for the intrinsic body diode. The n-doped layers above (such as the spacer layer above the lateral channel) provide the cathode, and are substantially coupled to the drain.

[0073] Another mechanism for conduction through an intrinsic body diode relies on the isolation layer being sufficiently thin that electrons can diffuse therethrough, enabling conduction through a parasitic n-p-n bipolar transistor formed by the substrate and the buffer layer (the collector), the isolation layer (the base), and overlying n-type layers such as the first second source/drain contact layers (the emitter). If the thickness of the isolation layer is increased to be greater than the 1000 Å as previously described (preferably in the range of 5000 Å), then electron recombination in the isolation layer will be a dominant effect, and electrons injected from the drain will not successfully diffuse to the substrate. Conduction will occur laterally through the isolation layer to the metallized source contact. Competition between these two mechanisms for operation of the intrinsic body diode can occur, with the dominant effect depending on the thickness and doping of the isolation layer. A forward voltage drop of approximately 1.5 volts is expected for this diode. Localized implant doping to increase the doping level of the isolation layer in a region about the metallized source interconnect can be used to enhance the diode performance.

[0074] Design enhancement of a semiconductor device to provide higher breakdown voltage between source and drain with minimal increase in device on-resistance, formed according to the principles of the present invention, will now be described. The device described hereinabove with reference to FIGS. 3 to 21 provides a baseline design with an on-resistance of about 1.27 Ω·mm and an exemplary reverse drain-to-source voltage up to 20 volts, employing a gate-to-

drain separation distance (see, e.g., gate-to-drain separation distance 377 of FIG. 18) of 1.5 μm. A preferable higher-voltage design will now be described providing an on-resistance of 2.19 Ω·mm and an exemplary reverse drain-to-source voltage up to 80 volts, employing a gate-to-drain separation distance of 2.5 μm. The results were obtained by simulation of fields and carrier flow on a scale of the device feature sizes using the commercially available simulation tool Silvaco®. Of course, the parameters described herein are for illustrative purposes only and the broad scope of the present invention is not so limited.

[0075] Ordinarily, for a field-effect transistor, on-resistance is expected to increase roughly as the 2.6 power of rated breakdown voltage. Thus, increasing the maximum reverse drain-to-source voltage from 20 volts to 80 volts should increase the on-resistance from 1.27 Ω·mm in the baseline case to approximately 47 Ω·mm for an 80 volts drain-to-source breakdown voltage rating. The on-resistance of 2.19 Ω·mm that was obtained by an exemplary enhancement for 80 volts is a significant reduction from ordinary expectation.

[0076] A key issue affecting maximum reverse drain-to-source breakdown voltage is the electric field in a region proximal the gate. One technique used in the industry to reduce a high electric field in a PHEMT or other semiconductor device is to introduce a “field plate” (i.e., a highly conductive structure preferably electrically coupled to the gate), such as a patterned metallic deposition, in a region of the device exhibiting such field. The advantage of field plates is to shift and reduce the peak electric field away from a region such as a gate edge (also spreading the electric field), resulting in a higher maximum reverse drain-to-source breakdown voltage. However, disadvantages of field plates are the extra mask layer and processing steps required for its deposition (such as by sputtering) and associated costs, as well as increased on-resistance resulting from higher channel depletion in an area under a field plate, requiring a larger active device area to provide a required on-resistance.

[0077] Another general technique to increase the maximum device breakdown voltage is to increase the gate-to-drain separation distance. This can be accomplished by increasing the recess width between the gate and drain, which can reduce the electric field at the drain-facing edge of the gate. However, a disadvantage of increasing the gate-to-drain separation distance is, again, an increase in device on-resistance and device cost due to the enlarged dimensions thereof.

[0078] Substantial improvement in gate-to-drain voltage can be obtained for a compound semiconductor device as described herein without significantly increasing device on-resistance. Such improvement can be obtained by jointly enhancing gate-to-drain separation distance (see, e.g., gate-to-drain separation distance 377 of FIG. 18), increasing the thickness and decreasing the doping concentration of the first spacer layer 313 as illustrated in FIG. 6 and discussed above, and reducing the delta doping concentration of the top and bottom delta-doped layers proximate the lateral channel (e.g., reducing the delta doping concentration of the barrier layer 318 and between the third spacer layer 333 and the second barriers layer 336 as illustrated in FIGS. 6-8 and discussed above).

[0079] Turning now to FIGS. 26A, 26B, and 26C, illustrated are graphical representations of a dependence of breakdown voltage and on resistance on a gate-to-drain separation distance (“gate-drain length”) of a semiconductor device constructed according to the principles of the present invention. The FIGURES illustrate the effect of changing the gate-to-drain separation distance on source-to-drain breakdown voltage (“Bdv”) and on-resistance (“Ron”). As observable in FIG. 26A, increasing the gate-to-drain separation distance from 1.5 μm to 2.0 μm provides an immediate increase in breakdown voltage, but further increases have only marginal effect. On-resistance, as illustrated in FIG. 26B, however, shows a consistent increase with increasing gate-to-drain separation distance. Plotting on-resistance against breakdown voltage, as illustrated in FIG. 26C, indicates that substantial increase in breakdown voltage can be obtained with little increase in on-resistance by increasing the gate-to-drain separation distance up to a corresponding breakdown voltage of roughly 70 to 80 volts.

[0080] Turning now to FIGS. 27A, 27B, and 27C, illustrated are graphical representations of a dependence of breakdown voltage and on resistance on a top layer delta doping density of a semiconductor device constructed according to the principles of the present invention. The FIGURES illustrate the effect on source-to-drain breakdown voltage and on-resistance of changing the delta doping of the top delta-doped layer (i.e., the delta doping applied between the third spacer layer 333 and second barrier layer 336 of the substrate drive FET described with respect to FIGS. 3-21 above). As illustrated in FIG. 27A, a small increase in delta doping concentration of the top delta-doped layer provides a modest increase in breakdown voltage, but a further increase has the opposite effect. In FIG. 27B, increasing the delta doping concentration of the top delta-doped layer provides continued improvement in on-resistance. The doping densities plotted on the horizontal axes of FIGS. 27A and 27B expressed in units of cm^{-3} can be converted to units of cm^{-2} as used herein by dividing by a factor $1.67 \times 10^6 \text{ cm}^{-1}$. Plotting on-resistance against breakdown voltage, as illustrated in FIG. 26C, indicates that substantial increase in breakdown voltage can be obtained with an increase up to a point in the delta doping concentration of the top delta-doped layer, but that a further increase is not beneficial.

[0081] Combining the results observable in FIGS. 26A, 26B, and 26C, in FIGS. 27A, 27B, and 27C, and with further results from varying the doping concentration of the first spacer layer 313 and its thickness provides a significant increase in breakdown voltage with limited increase in on-resistance compared to a baseline design as described previously hereinabove. The results are summarized in Table I below.

[0082] A substrate driven FET as described hereinabove with a breakdown voltage rating of 80 volts can be readily used as a synchronous rectifier in switch-mode power conversion applications requiring roughly a 12-volt dc output. The low gate charge of such a device accommodates a switching frequency in the power converter substantially higher than the few hundred kilohertz now obtainable with silicon devices. Practical switching frequencies for such higher voltage applications are expected to approach one megahertz or more, with a corresponding reduction in power converter size due to smaller magnetics and capacitors for filtering and power transformers.

[0083] Thus, a substrate driven FET configured with switched contacts on opposing surfaces, an intrinsic body diode and a lateral channel that may be modulation doped has been introduced. The substrate driven FET can be configured as a depletion-mode or as an enhancement-mode device. The resulting substrate driven FET can be designed and packaged to exhibit very low on-resistance and be operable with very fast switching speeds. While the illustrated embodiments introduce a source contact coupled to a bottom surface of a substrate and a drain contact on a top surface of the substrate driven FET, those skilled in the art understand that the contacts may be reversed and still fall within the broad scope of the present invention.

[0084] Those skilled in the art should understand that the previously described embodiments of the field-effect transistor and related methods of forming the same are submitted for illustrative purposes only. In addition, other embodiments capable of providing the advantages as described above are well within the broad scope of the present invention. While the field-effect transistor has been described as providing advantages in the environment of a power supply, other applications therefor are well within the broad scope of the present invention.

[0085] For a better understanding of power electronics, see “Principles of Power Electronics,” by J. G. Kassakian, M. F. Schlecht and G. C. Verghese, Addison-Wesley (1991). For a better understanding of semiconductor devices and processes, see “Fundamentals of III-V Devices,” by William Liu, John Wiley and Sons, (1999). For a better understanding of gallium arsenide processing, see “Modern GaAs Processing Methods,” by Ralph Williams, Artech House, Second Ed. (1990). The aforementioned references are incorporated herein by reference.

[0086] Also, although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For

TABLE I

Case	Top Delta Doping, cm^{-2}	Gate-Drain Length, μm	First Spacer Layer (313) concentration, cm^{-3}	First Spacer Layer (313) thickness, \AA	Bdv, V	Ron, $\Omega \cdot \text{mm}$
Baseline	3×10^{12}	1.5	1×10^{16}	8,000	20	1.27
Enhanced	1.2×10^{12}	2.5	1×10^{15}	23,000	80	2.19

example, many of the processes discussed above can be implemented in different methodologies and replaced by other processes, or a combination thereof, to form the devices providing reduced on-resistance, gate drive energy, and costs as described herein.

[0087] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. Additionally, the terms “above,” “formed over” or other similar terminology employed in reference to the semiconductor device or method of forming the same shall not be limited to “directly above” or “directly formed over” and, unless otherwise specified, the scope of the present invention contemplates that intervening layers may be present when characterizing a layer above, over, formed over, etc. another layer.

What is claimed is:

1. A semiconductor device, comprising:
 - a conductive substrate having a source contact covering a substantial portion of a bottom surface thereof;
 - an isolation layer oppositely doped from and above said conductive substrate;
 - a lateral channel above said isolation layer;
 - a drain contact above said lateral channel;
 - a gate located in a gate recess interposed between said lateral channel and said drain contact;
 - a drain formed by at least one source/drain contact layer interposed between said lateral channel and said drain contact, and offset from said gate by a gate-to-drain separation distance; and
 - an interconnect that connects said lateral channel to said conductive substrate operable to provide a coupling between said source contact and said lateral channel.
2. The semiconductor device as recited in claim 1 wherein said gate-to-drain separation distance is equal to or greater than 1.5 μm .
3. The semiconductor device as recited in claim 1 further comprising a buffer layer interposed between said conductive substrate and said isolation layer.
4. The semiconductor device as recited in claim 1, further comprising:
 - a spacer layer above said isolation layer;
 - a buffer layer above said spacer layer;
 - a modulation doped barrier layer above said spacer layer; and
 - another spacer layer above said barrier layer.

5. The semiconductor device as recited in claim 4 wherein said buffer layer is an alternating aluminum-gallium arsenide/gallium arsenide (“AlGaAs/GaAs”) super-lattice buffer.

6. The semiconductor device as recited in claim 1, further comprising:

- a spacer layer above said lateral channel;
- a barrier layer above said spacer layer;
- a recess layer above said barrier layer; and
- an etch stop layer above said recess layer.

7. The semiconductor device as recited in claim 6 wherein said spacer layer is modulation doped to a level of about $1.2 \times 10^{12} \text{ cm}^{-2}$ or less.

8. The semiconductor device as recited in claim 1 further comprising a metal layer and a drain post interposed between said at least one source/drain contact layer and said drain contact.

9. The semiconductor device as recited in claim 1 further comprising a dielectric layer interposed between said at least one source/drain contact layer and said drain contact.

10. The semiconductor device as recited in claim 1 wherein said lateral channel is pseudomorphic.

11. A method of forming a semiconductor device, comprising:

- providing a conductive substrate;
- forming a source contact on a bottom surface of said conductive substrate;
- forming an isolation layer oppositely doped from and above said conductive substrate;
- forming a lateral channel above said isolation layer;
- forming a drain contact above said lateral channel;
- forming a gate in a gate recess interposed between said lateral channel and said drain contact;
- forming a drain with at least one source/drain contact layer interposed between said lateral channel and said drain contact, and offset from said gate by a gate-to-drain separation distance; and
- forming an interconnect that connects said lateral channel to said conductive substrate operable to provide a coupling between said source contact and said lateral channel.

12. The method as recited in claim 11 wherein said gate-to-drain separation distance is equal to or greater than 1.5 μm .

13. The method as recited in claim 11 further comprising forming a buffer layer interposed between said conductive substrate and said isolation layer.

14. The method as recited in claim 11, further comprising:

- forming a spacer layer above said isolation layer;
- forming a buffer layer above said spacer layer;
- forming a modulation doped barrier layer above said spacer layer; and
- forming another spacer layer above said barrier layer.

15. The method as recited in claim 14 wherein said buffer layer is an alternating aluminum-gallium arsenide/gallium arsenide ("AlGaAs/GaAs") super-lattice buffer.

16. The method as recited in claim 11, further comprising:

forming a spacer layer above said lateral channel;

forming a barrier layer above said spacer layer;

forming a recess layer above said barrier layer; and

forming an etch stop layer above said recess layer.

17. The method as recited in claim 16 wherein said spacer layer is modulation doped to a level of about $1.2 \times 10^{12} \text{ cm}^{-2}$ or less.

18. The method as recited in claim 11 further comprising forming a metal layer and a drain post interposed between said at least one source/drain contact layer and said drain contact.

19. The method as recited in claim 11 further comprising forming a dielectric layer interposed between said at least one source/drain contact layer and said drain contact.

20. The method as recited in claim 11 wherein said lateral channel is pseudomorphic.

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