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(54) **DESIGN AND FABRICATION OF 6.1-A FAMILY SEMICONDUCTOR DEVICES USING SEMI-INSULATING ALSB SUBSTRATE**

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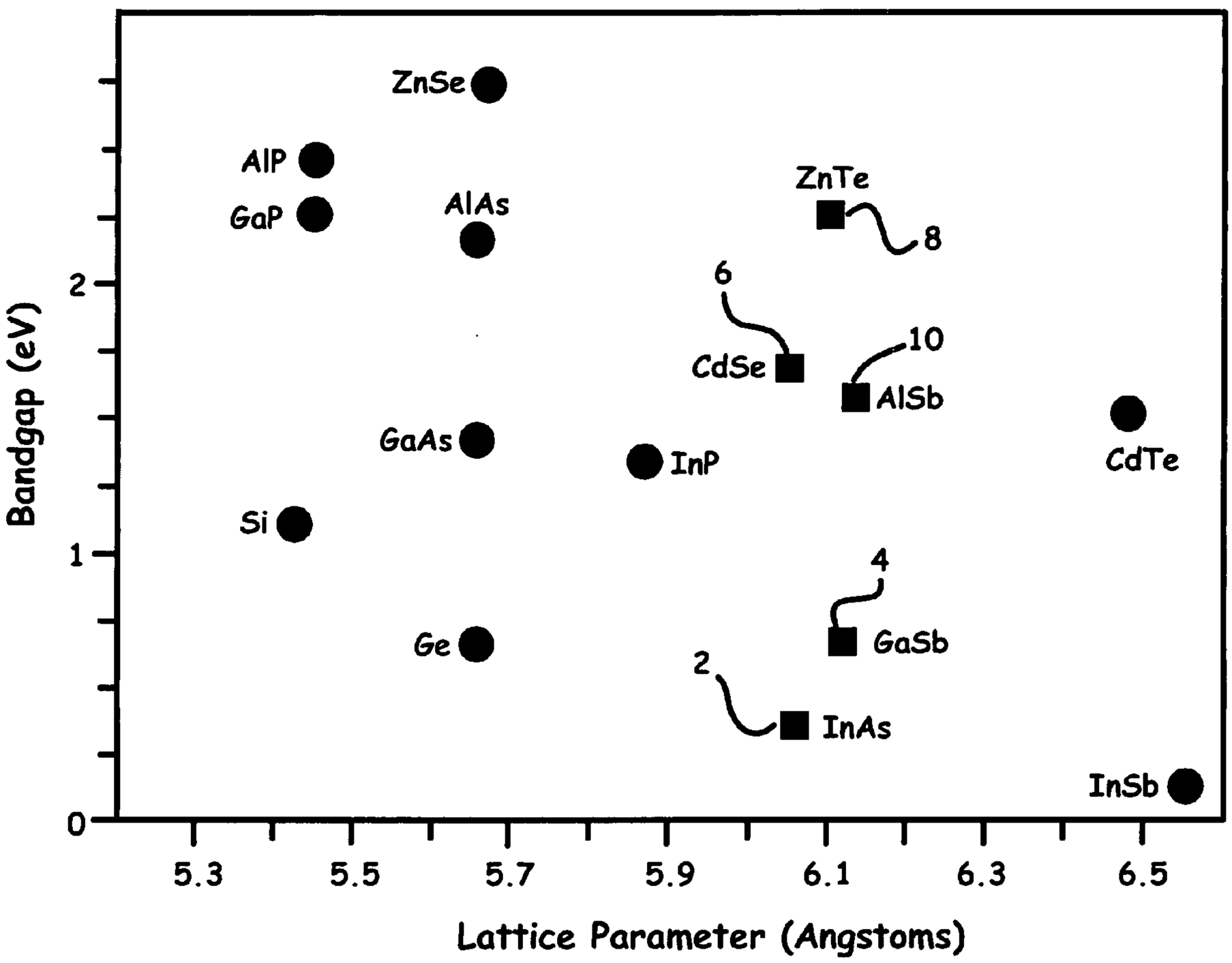
(57) **ABSTRACT**

For the first time, an aluminum antimonide (AlSb) single crystal substrate is utilized to lattice-match to overlying semiconductor layers. The AlSb substrate establishes a new design and fabrication approach to construct high-speed, low-power electronic devices while establishing inter-device isolation. Such lattice matching between the substrate and overlying semiconductor layers minimizes the formation of defects, such as threaded dislocations, which can decrease the production yield and operational life-time of 6.1-Å family heterostructure devices.



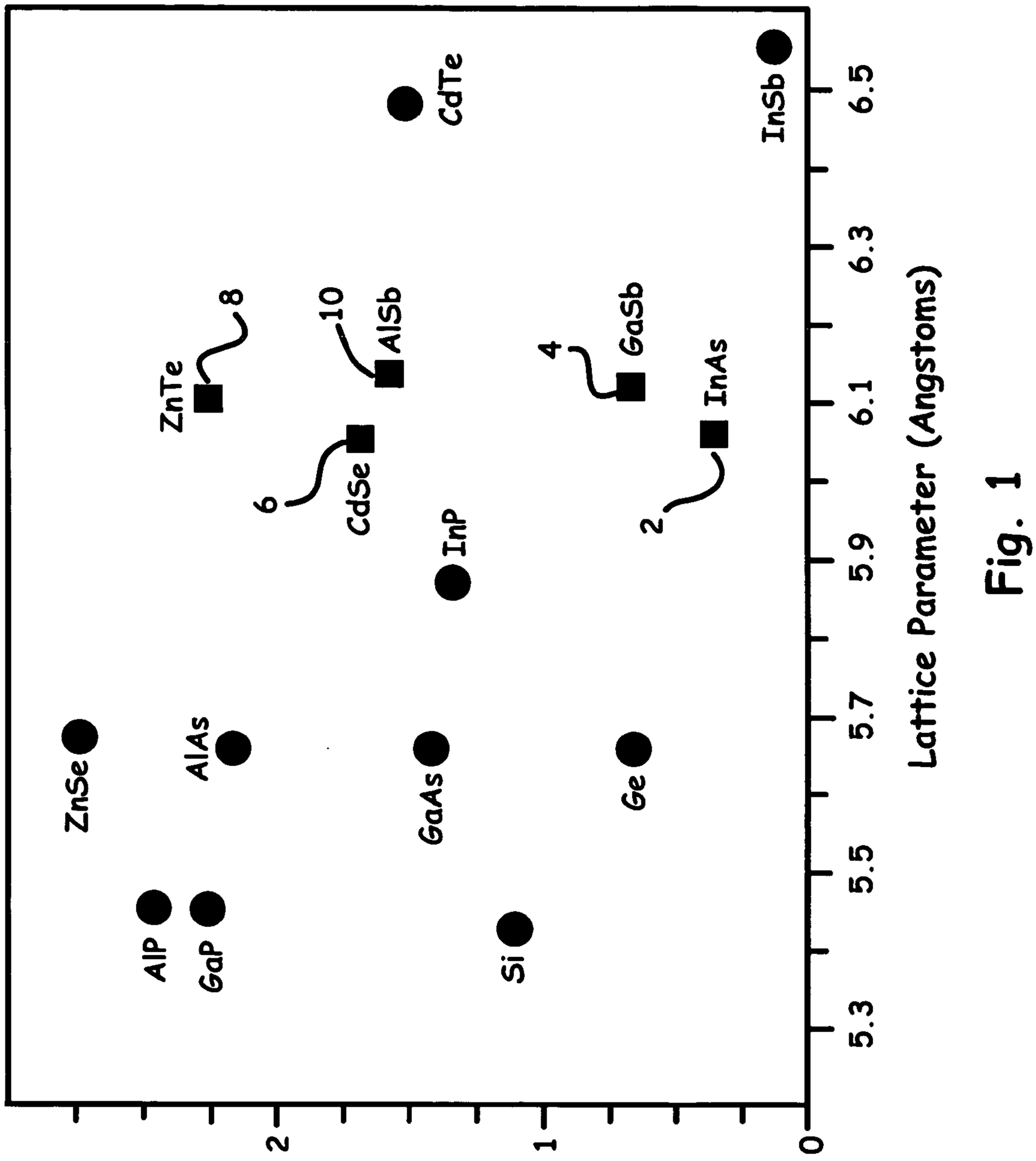

Bandgap (eV)
2
1
0
Lattice Parameter (Angstoms)
5.3
5.5
5.7
5.9
6.1
6.3
6.5
ZnSe
AlP
GaP
AlAs
Si
GaAs
InP
Ge
CdSe
InAs
GaSb
AlSb
CdTe
InSb
ZnTe
8
10
4
6
2

Fig. 1

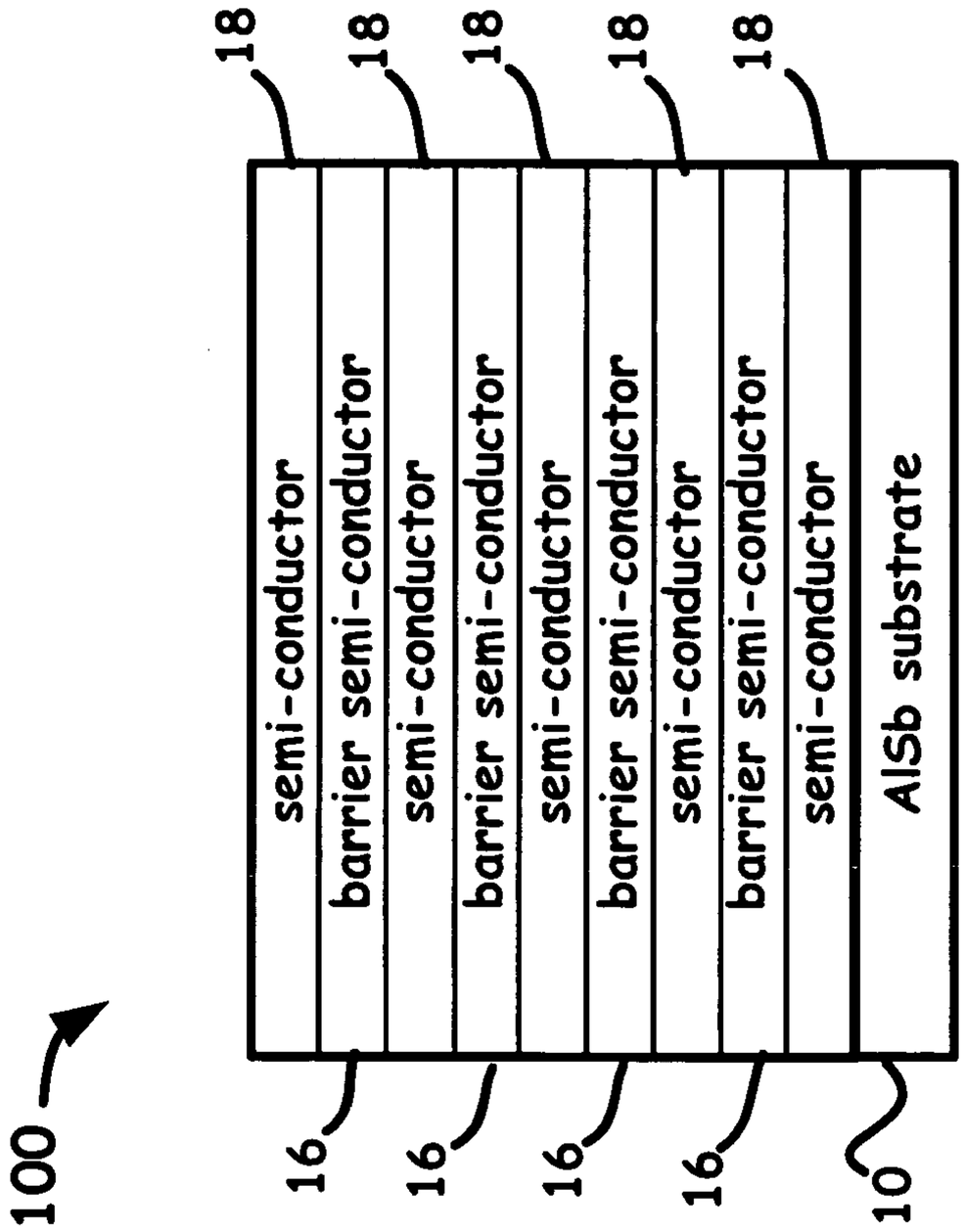

100
18
18
18
18
18
semi-conductor
barrier semi-conductor
semi-conductor
barrier semi-conductor
semi-conductor
barrier semi-conductor
semi-conductor
barrier semi-conductor
semi-conductor
AlSb substrate
16
16
16
16
10

Fig. 2(b)

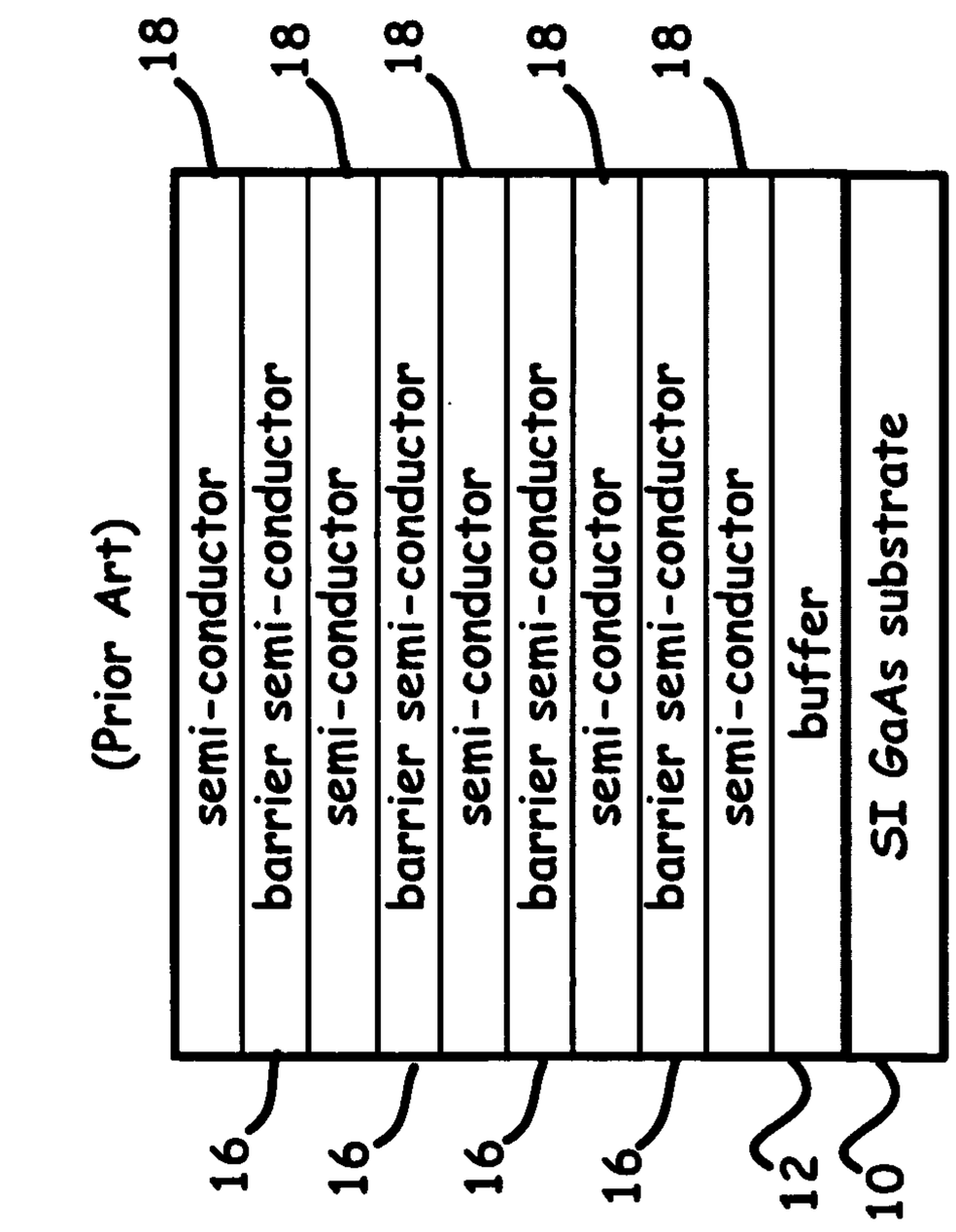

(Prior Art)
18
18
18
18
18
semi-conductor
barrier semi-conductor
semi-conductor
barrier semi-conductor
semi-conductor
barrier semi-conductor
semi-conductor
barrier semi-conductor
semi-conductor
buffer
SI GaAs substrate
16
16
16
16
12
10

Fig. 2(a)

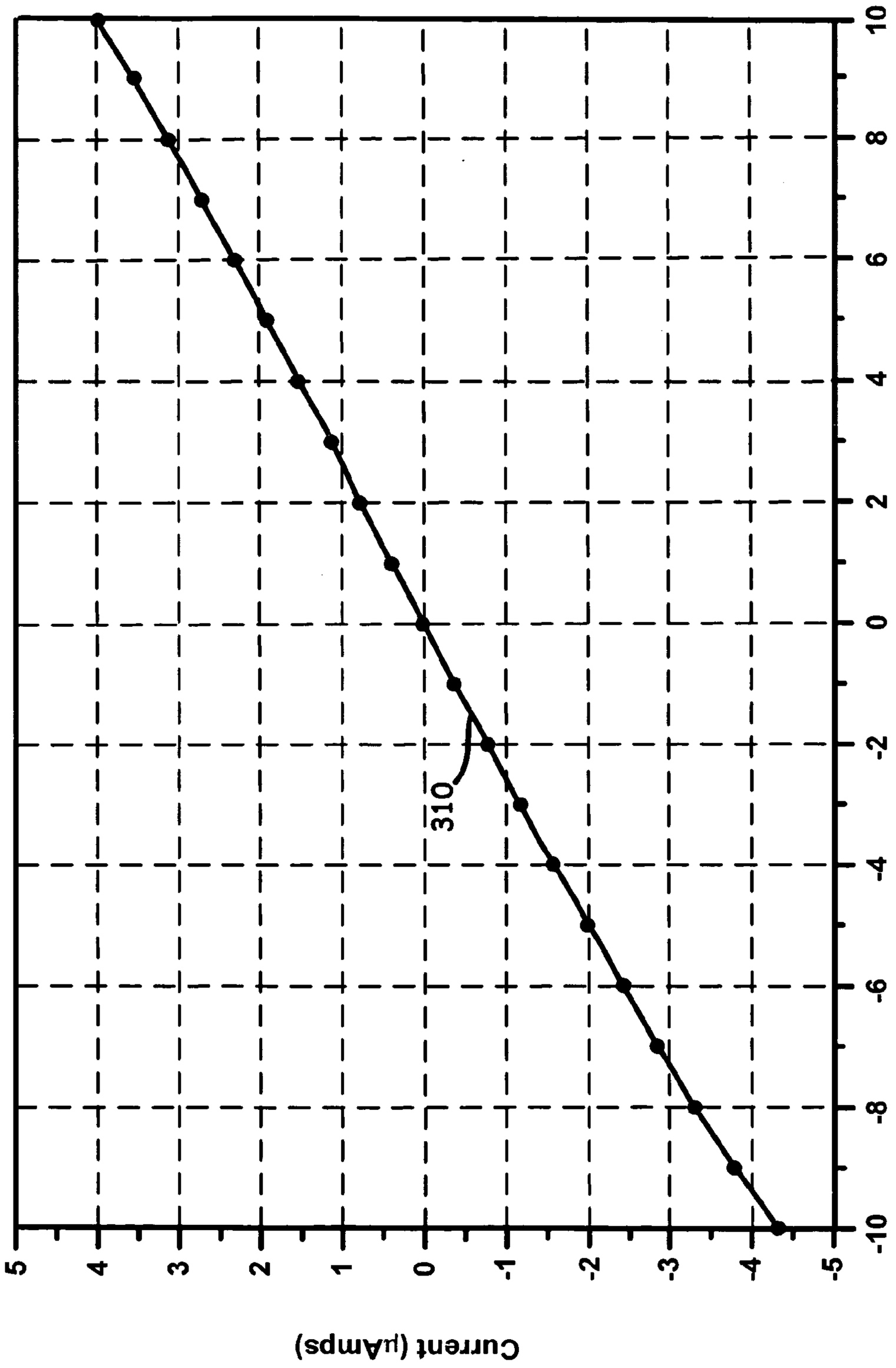

10
8
6
4
2
0
-2
-4
-6
-8
-10
Voltage (Volts)
5
4
3
2
1
0
-1
-2
-3
-4
-5
Current (μAmps)
310

Fig. 3

DESIGN AND FABRICATION OF 6.1-A FAMILY SEMICONDUCTOR DEVICES USING SEMI-INSULATING ALSB SUBSTRATE

RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Application No. 60/507,742, filed Sep. 30, 2003, and entitled, "Design and Fabrication of 6.1-Å Family III-V Semiconductor Devices Using Semi-Insulating AlSb Substrate," and U.S. Provisional Application No. 60/520,903, filed Nov. 17, 2003, entitled "Design and Fabrication of 6.1-Å Family III-V Semiconductor Devices Using Semi-Insulating AlSb Substrate" which are incorporated herein by this reference.

[0002] The United States Government has rights in this invention pursuant to Contract No. W-7405-ENG-48 between the United States Department of Energy and the University of California for the operation of Lawrence Livermore National Laboratory.

BACKGROUND OF THE INVENTION

[0003] 1. Field of the Invention

[0004] The present invention relates to semiconductors. More specifically, the present invention relates to bulk single crystal Aluminum Antimonide (AlSb) substrates incorporated with heterostructures from the 6.1-Å family of semiconductors.

[0005] 2. State of Technology

[0006] Antimonide/Arsenide heterostructures are recognized in the semiconductor industry as revolutionary low-noise, low-power, high-speed electronic devices. The composition of the Antimonide/Arsenide heterostructure is composed of multiple layers of Antimonide and Arsenide semiconductor compounds such as AlSb, GaSb, InAs, and related ternary and quaternary alloys from the elements of Al, As, Ga, In, and Sb. These Antimonide and Arsenide semiconductor compounds have a crystal structure dimension or lattice parameter that is nearly matched at 6.1 Å (Angstrom). Such compounds are identified as lattice-matched 6.1-Å family III-V semiconductors.

[0007] Recent research and development of the 6.1-Å family heterostructure devices, has lead to fabrication of state-of-the-art electronic devices, e.g., high electron mobility transistors (HEMTs), heterostructure field-effect transistors (HFETs), resonant interband tunneling diodes (RITDs), heterojunction bipolar transistors (HBTs), hybrid superconductor/semiconductor (HSS) devices, magneto-electronic devices (e.g., Hybrid Hall effect device), quantum cascade lasers (QCLs), infrared photodiodes, and infrared detectors. The development of Antimonide/Arsenide heterostructure devices has demonstrated that such devices can be used for high-speed analog and digital applications, high-speed logic applications, innovative multi-function radar and communication systems, and mid-infrared lasing and detection applications. Such applications strongly impact military and national security interest as well as commercialization interest.

[0008] However, fabrication of 6.1-Å family heterostructure devices is complicated because available semi-insulating (SI) substrates, i.e., substrates with very high resistivity (ρ) at room temperature (ρ_{300} greater than about 10^7 Ω·cm) do not have a suitable lattice parameter for lattice matching semiconductors from the 6.1-Å family III-V or the 6.1-Å family II-VI (e.g., Zinc Telluride (ZnTe)) semiconductors. For example, the room temperature lattice parameter of the desirable III-V SI GaAs substrate is 5.653 Å and the room temperature lattice parameter of the III-V SI InP substrate is 5.869 Å. In the case of GaAs, the lattice mismatch is about 8% when heterostructures from the 6.1-Å III-V family are used for desired devices, which can create about 10^8 cm^{-2} surface dislocations. Moreover, 6.1-Å family II-VI heterostructure devices (e.g. ZeTe) grown on such GaAs substrates, also results in a mismatch coefficient of about 7.4%, which induces compressed strain along the interface.

[0009] Because of such disparate lattice mismatches, device fabrication using such substrates requires a buffer layer material (often a relatively thick layer of up to a few microns of a semiconductor material, such as AlSb) arranged between a substrate and heterostructure to counter surface dislocation nucleation. The use of such buffer layers remains a fabrication issue because surface dislocations, known as threading dislocations, can still travel through the buffer layer material and severely degrade device performance by acting as radiative (photon) and non-radiative (phonon) recombination centers.

[0010] Background information on such a buffer layer requirement and remaining fabrication issues can be found in, "The 6.1 Å family (InAs, GaSb, AlSb) and its heterostructures: a selective review," by Herbert Kroemer, Physica E 20, pp. 196-203, 2004, including the following, "When the MBE growth is performed on lattice-mismatched GaAs substrates rather than on GaSb, the interposition of a proper buffer layer is essential for high quality growth . . . . Using GaSb for the initial nucleation leads to very rough initial morphology. Nucleating with AlSb leads to much less initial surface roughness, but the residual roughness persists with continued growth, and leads to InAs quantum wells with poor transport properties. Following the initial thin AlSb nucleation layer with a thick (≈1 μm) GaSb buffer layer smoothes out the surface morphology, and if the growth is then switched to AlSb or (Al, Ga)Sb, the smooth surface persist, leading to InAs quantum wells with much better transport properties."

[0011] Accordingly, a need exists for a high-speed low-power electronic heterostructure device that includes a single crystal, lattice-matched, semi-insulating substrate to replace the current use of lattice-mismatched substrates of SI GaAs or SI InP. Such a need has been jointly emphasized by several, such as Naval Research Laboratory (NRL) and TRW researchers at the August 2002 IEEE Lester Eastman Conference on High Performance Devices, "A semi-insulating substrate is required for complex circuits, and none exist with a lattice constant near 6.2 Å," IEEE Proceedings, pp. 288-296, 2002. The present invention is directed to such a need.

SUMMARY OF THE INVENTION

[0012] Accordingly, the present invention provides a method of forming a semiconductor device that includes: providing an AlSb substrate; and growing one or more semiconductor layers substantially lattice matched to the AlSb substrate.

[0013] Another aspect of the present invention is to provide a method of forming a semiconductor device that includes: providing an AlSb substrate; and growing a semiconductor heterostructure substantially lattice matched to the AlSb substrate, wherein the semiconductor device is capable of being arranged with one or more buffer layers intermediate the AlSb substrate and the semiconductor heterostructure.

[0014] A further aspect of the present invention is to provide a semiconductor device that includes an AlSb substrate and one or more semiconductor layers grown on the AlSb substrate, wherein the one or more semiconductor layers are substantially lattice matched to the AlSb substrate.

[0015] A final aspect of the present invention is to provide a semiconductor device that includes an AlSb substrate and a semiconductor heterostructure grown on the AlSb base substrate, wherein the heterostructure is substantially lattice matched to the AlSb substrate and wherein the one or more buffer layers are capable of being arranged intermediate the AlSb substrate and the heterostructure.

[0016] Accordingly, the present invention provides a semi-insulating (SI) Aluminum Antimonide (AlSb) single crystal substrate capable of having a resistivity (ρ) at room temperature (ρ_{300K°) of greater than about 10^3 Ω·cm, more often greater than about 10^7 Ω·cm to be utilized in the design and fabrication of 6.1-Å family Antimonide/Arsenide heterostructures devices. The use of SI AlSb of the present invention provides a substantially lattice-matched substrate to construct high-speed low-power Antimonide/Arsenide and/or Zinc/Telluride heterostructures electronic devices such as, but not limited to, HEMTs, HFETs, RITDs, HBTs, HSS structures, and magneto-electronic devices (e.g., the Hybrid Hall effect device). Such a high resistivity AlSb substrate also allows for inter-device isolation for other Antimonide/Arsenide and/or Zinc/Telluride heterostructures such as QCLs, photodiodes, infrared photodiodes, and infrared detectors. Fabrication of such heterostructures using SI Aluminum Antimonide (AlSb) single crystal substrates substantially minimizes the nucleation of threading dislocations. As a result, production yield and operational life-time of Antimonide/Arsenide and/or Zinc/Telluride heterostructure devices configured with such substrates are enhanced over similar devices, such as devices that incorporate SI GaAs or SI InP substrates.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The accompanying drawings, which are incorporated into and form a part of the disclosure, illustrate an embodiment of the invention and, together with the description, serve to explain the principles of the invention.

[0018] FIG. **1** shows lattice constants vs. band gaps for various pure and compound semiconductors.

[0019] FIG. **2**(*a*) illustrates a conventionally grown heterostructure device having a GaAs SI substrate.

[0020] FIG. **2**(*b*) illustrates heterostructure device of the present invention having an AlSb substrate.

[0021] FIG. **3** illustrates a current versus voltage (I-V) curve of the substrate material to be utilized in heterostructures.

DETAILED DESCRIPTION OF THE INVENTION

[0022] Referring now to the following detailed information, and to incorporated materials; a detailed description of the invention, including specific embodiments, is presented. The detailed description serves to explain the principles of the invention.

[0023] Unless otherwise indicated, all numbers expressing quantities of ingredients, constituents, reaction conditions and so forth used in the specification and claims are to be understood as being modified in all instances by the term "about". Accordingly, unless indicated to the contrary, the numerical parameters set forth in the specification and attached claims are approximations that may vary depending upon the desired properties sought to be obtained by the subject matter presented herein. At the very least, and not as an attempt to limit the application of the doctrine of equivalents to the scope of the claims, each numerical parameter should at least be construed in light of the number of reported significant digits and by applying ordinary rounding techniques. Notwithstanding that the numerical ranges and parameters setting forth the broad scope of the subject matter presented herein are approximations, the numerical values set forth in the specific examples are reported as precisely as possible. Any numerical value, however, inherently contain certain errors necessarily resulting from the standard deviation found in their respective testing measurements.

General Description

[0024] An Aluminum Antimonide (AlSb) semiconductor substrate material is a member of the III-V family of semiconductors including Gallium Arsenide (GaAs), Indium Antimonide (InSb), Gallium Phosphide (GaP), etc. Similar to Germanium (Ge), Silicon (Si) and GaAs, AlSb has a zinc-blend cubic crystal structure, similar to Ge and Si, but unlike GaAs, AlSb has an indirect energy band gap, and similar to GaAs, but unlike Ge and Si, the energy band gap (E_g) is relatively high, i.e., an E_g of about 1.62 eV. Such structure and band-gap features of AlSb provide a material that is beneficial as an electronic device quality semiconductor substrate when utilized with heterostructures from the 6.1 Å III-V family of semiconductors, such as AlSb, GaSb and Indium Arsenide (InAs).

[0025] Moreover, the AlSb substrate of the present invention can also be arranged with II-VI 6.1-Å family semiconductors, such as, for example, Zinc Telluride (ZnTe) and Cadmium Selenide (CdSe), to provide desired semiconductor heterostructure devices. Specifically, ZnTe is a compound that can be incorporated into the present invention because such a compound has a direct energy band gap of 2.26 eV and a zinc-blend structure with a lattice constant of 6.10037 Å. By virtue of such a band gap, ZnTe provides a substantially lattice matched material with the AlSb substrate of the present invention to construct heterostructure opto-electronic devices in the blue-green region, such as pure green light emitting diodes (LEDs) and laser diodes (LDs).

[0026] Heterostructures, as utilized in the present invention, can include one or more thin layers (between about 10 Å and up to about 2 μm) of binary compounds such as, but not limited to Aluminum Antimonide (AlSb), Gallium Anti-

monide (GaSb), Indium Arsenide (InAs), Zinc Telluride (ZnTe), and/or related ternary and quaternary alloys of such materials. For example, Antimonide (Sb) and Arsenide (As) semiconductor compounds are exemplary materials that can be utilized in the present invention due to an inherent crystal structure dimension or lattice parameter that is substantially lattice matched at 6.1 Angstroms, e.g., the room temperature lattice constant of AlSb is 6.135 Å, for GaSb it is 6.095 Å, and for InAs it is 6.058 Å.

[0027] FIG. **1** illustrates lattice constants vs. band gaps for various pure and compound semiconductors. The present invention incorporates the 6.1 Å family semiconductors, such as, for example, InAs **2**, GaSb **4**, CdSe **6**, ZnTe **8**, and AlSb **10** (also denoted by squares). Accordingly, compounds, such as AlSb, GaSb, InAs, ZnTe, CdSe and related ternary and quaternary alloys from the elements of Al, As, Ga, In, Sb, Cd, Se, Zn, and Te are herein identified as substantially lattice-matched 6.1-Å family semiconductors that can utilized in the present invention.

[0028] The present invention utilizes such 6.1-Å family semiconductors identified above, by growing such materials on a substrate material as disclosed herein with or without an intermediate buffer layer (i.e., a buffer layer, such as, for example, a layer of AlSb or layers containing Sb compounds, is herein defined as an intermediate material layer sandwiched between a substrate and a heterostructure). Such a buffer layer's functions can include crystal lattice matching, electrical isolation and/or surface smoothing.

[0029] The Aluminum Antimonide (AlSb) single crystal substrate utilized herein is capable of having a substantially uniform resistivity (ρ) as measured over the entire produced substrate at room temperature (300 K°) of often greater than about 10^3 Ω·cm, more often greater than about 10^7 Ω·cm. Such AlSb crystal substrates of the present invention can be produced by a Czochralski (CZ) growth technique. However, other growth methods such as, but not limited to, a Traveling Heating Method (THM), capable of producing quality crystals may also be employed. A detailed disclosure of example methods of producing such a single crystal substrate is disclosed in Incorporated by reference, Co-pending, U.S. application Ser. No. 10/260,141, titled "High Resistivity Aluminum Antimonide Radiation Detector" by Sherohman et al., assigned to the assignee of the present invention, the disclosure herein incorporated by reference in its entirety.

[0030] Such a crystal substrate is beneficial in the design and fabrication of heterostructure devices that utilize semiconductor materials from the 6.1-Å family semiconductors as described above, e.g., GaSb, InAs, AlSb, ZnTe, CdSe and various combinations of the elements Al, As, Ga, In, Sb, Zn, Te, Cd, and Se thereof. Being a member of the 6.1-Å family semiconductors, the use of AlSb provides a lattice-matched substrate to such overlying semiconductor materials so as to construct high-speed (e.g., quantum tunneling devices capable of oscillating at up to about 1 THz) low-power electronic devices such as, but not limited to, HEMTs, HFETs, RITDs, HBTs, HSS structures, and magneto-electronic devices (e.g., the Hybrid Hall effect device).

[0031] In addition, the present invention's high resistivity capability of greater than about 10^7 Ω·cm AlSb substrate allows for interdevice isolation for other heterostructures, such as, but not limited to, Antimonide/Arsenide QCLs, infrared photodiodes, and infrared detectors. Moreover, device fabrication using a lattice matched AlSb substrate as disclosed herein, minimizes the nucleation of threading dislocations. As a result, the production yield and operational life-time of 6.1-Å family heterostructure devices grown on an AlSb substrate are enhanced over similar devices that use SI GaAs or SI InP substrates.

Specific Description

[0032] FIG. **2**(*a*) shows an example of the basic concept that exemplifies conventionally grown heterostructure semiconductor devices, e.g., HEMTs, HFETs, RITDs, HBTs, etc., that incorporate semiconductor materials within the 6.1-Å family such as, for example, Aluminum Antimonide (AlSb), Gallium Antimonide (GaSb), Indium Arsenide (InAs), Zinc Telluride (ZnTe) and/or their related ternary and quaternary alloys as previously disclosed. Such devices utilize a semi-insulating substrate **10**, such as GaAs, and one or more overlying layers **12**, such as, but not limited to AlSb, or layers containing Sb compounds, to buffer and/or smooth lattice mismatches between substrate **10** and overlying semiconductor layers **16**, **18**, to prevent non-uniformities, such as threaded dislocations.

[0033] Semiconductor layers **16**, such as AlSb, and alternating semiconductor layers **18** such as semiconductor layers from the 6.1-Å family doped with materials such as, but not limited to, Silicon (Si), Tellerium (Te), Selenium (Se), Beryllium (Be), and Tin (Sn), can be grown according to methods known in the art, such as by molecular beam epitaxy (MBE), to create barrier layers, channels (current paths), caps, Schottky barriers, etc., so as to form what is know to those skilled in the art as semiconductor heterostructures. In addition, an oxidation barrier (not shown) can be grown so as to protect underlying layers of materials, e.g., **16**, **18**, and metalized ohmic contacts (not shown), can be applied to predetermined layers according to methods known in the art to provide such devices with a means for such devices to be integrated into a desired circuitry.

[0034] FIG. **2**(*b*) shows a basic example configuration of a heterostructure semiconductor device of the present invention, generally designated as reference numeral **100**, that utilizes similar semiconductor layers from the 6.1-Å family as discussed above. Such a device incorporates a substantially uniform high resistivity AlSb substrate **10** of often greater than about 10^3 Ω·cm, more often greater than about 10^7 Ω·cm, capable of semi-insulating one or more overlying heterostructure layers **16**, **18**. Device fabrication using such an AlSb substrate **10** as disclosed herein, in addition to providing a semi-insulating base substrate, minimizes the nucleation of threading dislocations as a result of the substantial lattice matching to overlying 6.1-Å family semiconductor layers, resulting in an increase in the operational life-time of 6.1-Å family heterostructure devices, such as HEMTs, HFETs, RITDs, HBTs, LEDs, HSS structures, and magneto-electronic devices (e.g., the Hybrid Hall effect device).

[0035] FIG. **3** shows an I-V curve **310** (current versus voltage) of a substrate material of the present invention illustrating current levels capable of being produced within such a substrate between about −4.5 μamps and about +4 μamps when subjected to respective voltages between about −10 volts and about +10 volts. Such a measurement involves measuring an electrical current flow across a sample mate-

rial, such as an AlSb bulk crystal utilized in the present invention, when a DC voltage is applied onto a given sample. I-V curve **310**, as shown in FIG. **3**, represents the basic electrical properties of a substrate AlSb material used in a device such as a heterostructure, fabricated from such a material as disclosed herein.

[**0036**] In making the measurements to produce such a curve as shown in FIG. **3**, a thin piece of AlSb sample measuring about 1 cm×1 cm×0.1 cm and mechanically polished to about ¼ micron finish is arranged with approximately 1000 Å thick and 6 mm diameter of gold sputtered onto the sample's surface to establish electrical contacts. An I-V measurement then is conducted at room temperature (300 K°) at a voltage range between about −10V and about +10V, which covers the operating voltage regime for most of the common electrical devices. Such an I-V characteristic is ohmic in nature and a resulting response current of about ±5 μA, as shown in FIG. **3**, is produced when an AlSb substrate sample of the present invention is subjected to the imposed measurement conditions. Previous reports as disclosed in, "Electrical Properties of Semiconducting AlSb", by R. K. Willardson, A. C. Beer and A. E. Middleton, *J. Electro. Chem. Soc.* 101, 354 (1954); and in "Some Properties of aluminium antimonide p-n junctions", by C. R. Bemrose, Solid-State Electronics, 7, 765 (1964), show AlSb I-V measurements response currents with similar measurement conditions in the hundreds of μA to mA ranges.

[**0037**] Accordingly, an AlSb substrate of the present invention that can produce such a surprising I-V curve as shown in FIG. **3**, illustrates the semi-insulating properties of such a substrate having a lattice constant of 6.1 Å that can fulfill a need in the industry to produce desired electronic devices. As discussed above, researchers at The Naval Research Laboratory (NRL) and TRW at the August 2002 IEEE Lester Eastman Conference on High Performance Devices stated such an industry need by stating, "A semi-insulating substrate is required for complex circuits, and none exist with a lattice constant near 6.2 Å," IEEE Proceedings, pp. 288-296, 2002.

[**0038**] Moreover, in addition to applications as discussed above, heterostructure devices, such as, but not limited to Antimonide/Arsenide heterostructures, which have previously been fabricated on a GaSb substrate for infrared laser and infrared detector applications, can also incorporate an AlSb substrate as disclosed herein. Although GaSb is substantially lattice matched, such a substrate material is a very low band gap semiconductor (bandgap at 300 ° K for GaSb is 0.725 eV) and is therefore quite conducting at room temperature (resistivity of about 0.01 Ω·cm, which is much lower than the resistivity capability of AlSb greater than about 10^7 Ω·cm), has a high carrier concentration, and low mechanical strength.

[**0039**] In addition to the above, as another example arrangement, for applications where GaSb has been used as a substrate, GaSb can be deposited on an AlSb substrate of the present invention to provide interdevice isolation and lattice matching properties as discussed above.

[**0040**] It is to be understood that the number of semiconductor layers and the variations disclosed herein are not limited to these numbers of layers and/or variations. While the example arrangements of the invention are described, various modifications may be made in such arrangements to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

1. A method of forming a semiconductor device, comprising:

providing a bulk single crystal semi-insulating AlSb substrate having a resistivity of greater than about 10^7 Ω·cm; and

growing one or more semiconductor layers substantially lattice matched to said bulk single crystal semi-insulating AlSb substrate.

2. The method of claim 1, wherein said AlSb substrate is arranged to have a uniform resistivity capable of a providing a current between about −4.5 μamps and about +4 μamps when subjected to respective voltages between about −10 volts and about +10 volts.

3. The method of claim 1, wherein said one or more semiconductor layers comprises a compound from the 6.1-Å family III-V semiconductor family.

4. The method of claim 1, wherein said one or more semiconductor layers comprises a compound from the 6.1-Å family II-VI semiconductor family.

5. (canceled)

6. The method of claim 1, wherein said one or more semiconductor layers further comprise alternating layers of doped and undoped semiconductor materials.

7. (canceled)

8. (canceled)

9. (canceled)

10. (canceled)

11. (canceled)

12. (canceled)

13. (canceled)

14. (canceled)

15. (canceled)

16. A method of forming a semiconductor device, comprising:

providing a bulk single crystal semi-insulating AlSb substrate having a resistivity of greater than about 10^7 Ω·cm; and

growing a semiconductor heterostructure substantially lattice matched to said bulk single crystal semi-insulating AlSb substrate, wherein said semiconductor device further comprises one or more buffer layers intermediate said bulk single crystal semi-insulating AlSb substrate and said semiconductor heterostructure.

17. The method of claim 16, wherein said AlSb substrate is arranged to have a uniform resistivity capable of a providing a current between about −4.5 μamps and about +4 μamps when subjected to respective voltages between about −10 volts and about +10 volts.

18. The method of claim 16, wherein said semiconductor heterostructure further comprises one or more binary, ternary, or quaternary, semiconductor layers comprising the 6.1-Å III-V family.

19. The method of claim 16, wherein said semiconductor heterostructure further comprises one or more binary, ternary, or quaternary, semiconductor layers comprising the 6.1-Å II-VI family.

20. The method of claim 16, wherein said one or more buffer layers are arranged so as to provide crystal lattice matching, electrical isolation and/or surface smoothing.

21. A semiconductor device, comprising:

a bulk single crystal semi-insulating AlSb substrate having a resistivity of greater than about 10^7 Ω·cm; and

one or more semiconductor layers grown on said bulk single crystal semi-insulating AlSb substrate, wherein said one or more semiconductor layers are substantially lattice matched to said bulk single crystal semi-insulating AlSb substrate.

22. The semiconductor device of claim 21, wherein said AlSb substrate is arranged to have a uniform resistivity capable of a providing a current between about −4.5 μamps and about +4 μamps when subjected to respective voltages between about −10 volts and about +10 volts.

23. The semiconductor device of claim 21, wherein said one or more semiconductor layers further comprise one or more binary, ternary, or quaternary, semiconductor layers comprising the 6.1-Å III-V family.

24. The semiconductor device of claim 21, wherein said one or more semiconductor layers further comprise one or more binary, ternary, or quaternary, semiconductor layers comprising the 6.1-Å II-VI family.

25. The semiconductor device of claim 21, wherein said semiconductor layers are formed by molecular beam epitaxy.

26. The semiconductor device of claim 21, wherein said one or more semiconductor layers further comprise alternating layers of doped and undoped semiconductor materials.

27. (canceled)

28. (canceled)

29. (canceled)

30. (canceled)

31. (canceled)

32. (canceled)

33. (canceled)

34. (canceled)

35. (canceled)

36. A semiconductor device, comprising:

a bulk single crystal semi-insulating AlSb substrate having a resistivity of greater than about 10^7 Ω·cm; and

a semiconductor heterostructure grown on said bulk single crystal semi-insulating AlSb base substrate, wherein said heterostructure comprises substantial lattice matching to said bulk single crystal semi-insulating AlS substrate and wherein said heterostructure further comprises one or more buffer layers intermediate said AlSb substrate and said heterostructure.

37. The semiconductor device of claim 36, wherein said AlSb substrate is arranged to have a uniform resistivity capable of a providing a current between about −4.5 μamps and about +4 μamps when subjected to respective voltages between about −10 volts and about +10 volts.

38. The semiconductor device of claim 36, wherein said semiconductor heterostructure further comprises one or more binary, ternary, or quaternary, semiconductor layers comprising the 6.1-Å III-V family.

39. The semiconductor device of claim 36, wherein said semiconductor heterostructure further comprises one or more binary, ternary, or quaternary, semiconductor layers comprising the 6.1-Å II-VI family.

40. The semiconductor device of claim 36, wherein said buffer layer is arranged so as to provide crystal lattice matching, electrical isolation and/or surface smoothing.

41. The semiconductor device of claim 36, wherein said semiconductor heterostructure is formed by molecular beam epitaxy.

42. The semiconductor device of claim 36, wherein said semiconductor heterostructure further comprises alternating layers of doped and undoped semiconductor materials.

43. (canceled)

44. (canceled)

45. (canceled)

46. (canceled)

47. (canceled)

48. (canceled)

49. (canceled)

50. (canceled)

51. (canceled)

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