US 20070069333A1

(19) **United States**

(12) **Patent Application Publication**

Crawford et al.

(10) **Pub. No.: US 2007/0069333 A1**

(43) **Pub. Date: Mar. 29, 2007**

(54) **INTEGRATED INDUCTOR STRUCTURE AND METHOD OF FABRICATION**

(76) Inventors: **Ankur Mohan Crawford**, New York, NY (US); **Henning Braunisch**, Chandler, AZ (US); **Rajendran Nair**, Gilbert, AZ (US); **Gilroy Vandentop**, Tempe, AZ (US); **Shan X. Wang**, Portola Valley, CA (US)

Correspondence Address:
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030 (US)

(21) Appl. No.: **11/554,567**

(22) Filed: **Oct. 30, 2006**

Related U.S. Application Data

(62) Division of application No. 10/975,552, filed on Oct. 27, 2004.

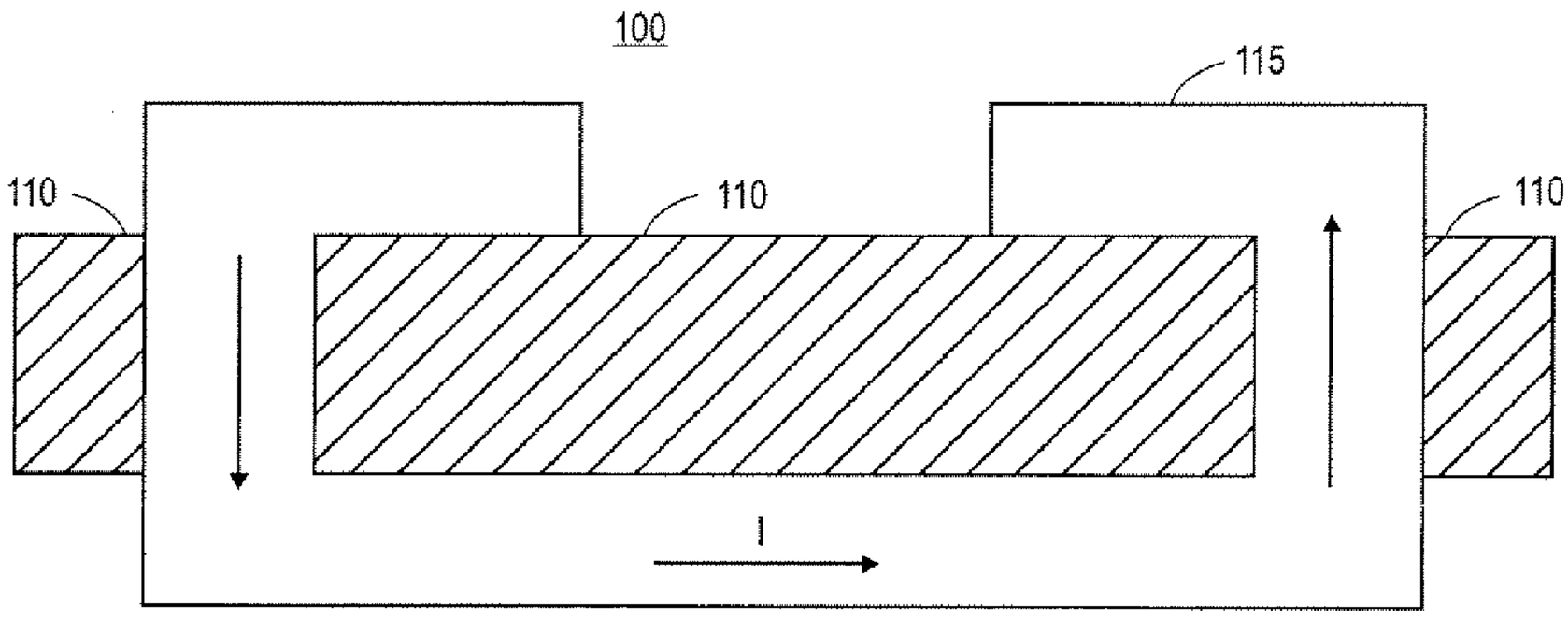
Publication Classification

(51) **Int. Cl.**
H01L 29/00 (2006.01)

(52) **U.S. Cl.** **257/531**

(57) **ABSTRACT**

An inductor structure comprised of a magnetic section and a single turn solenoid The single turn solenoid to contain within a portion of the magnetic section and circumscribed by the magnetic section.



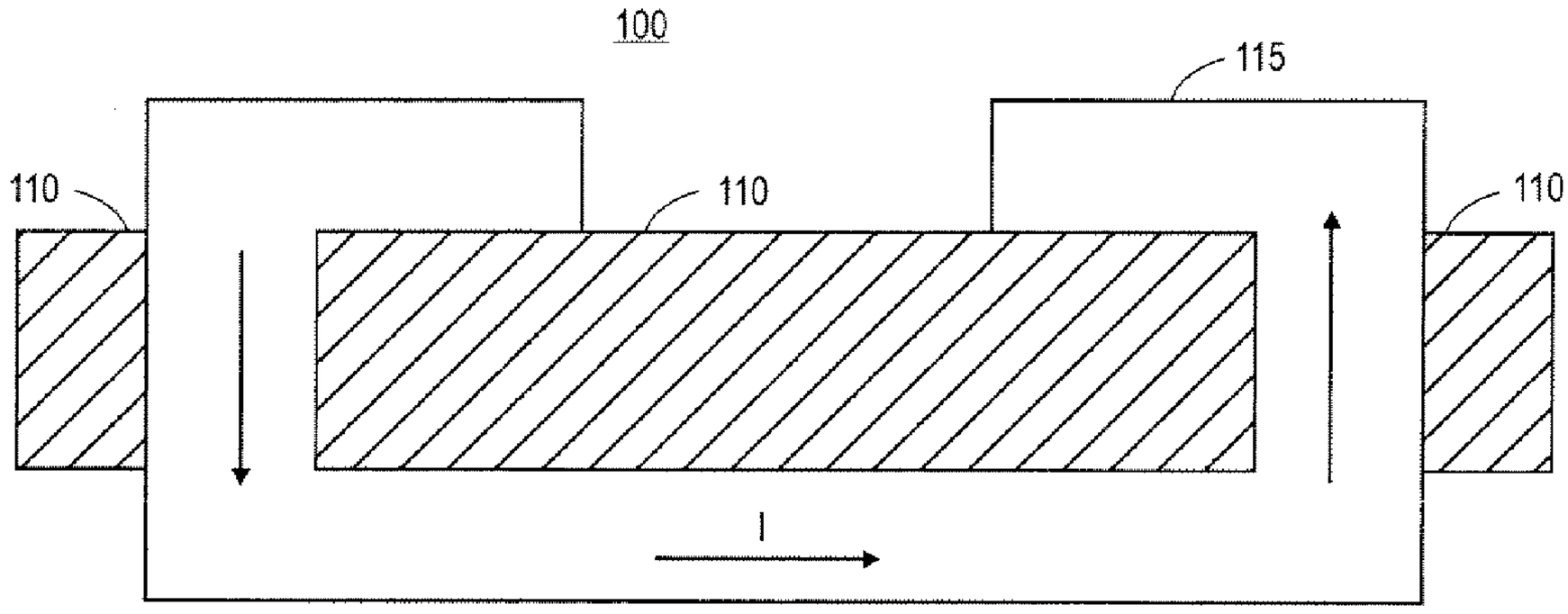


FIG. 1a

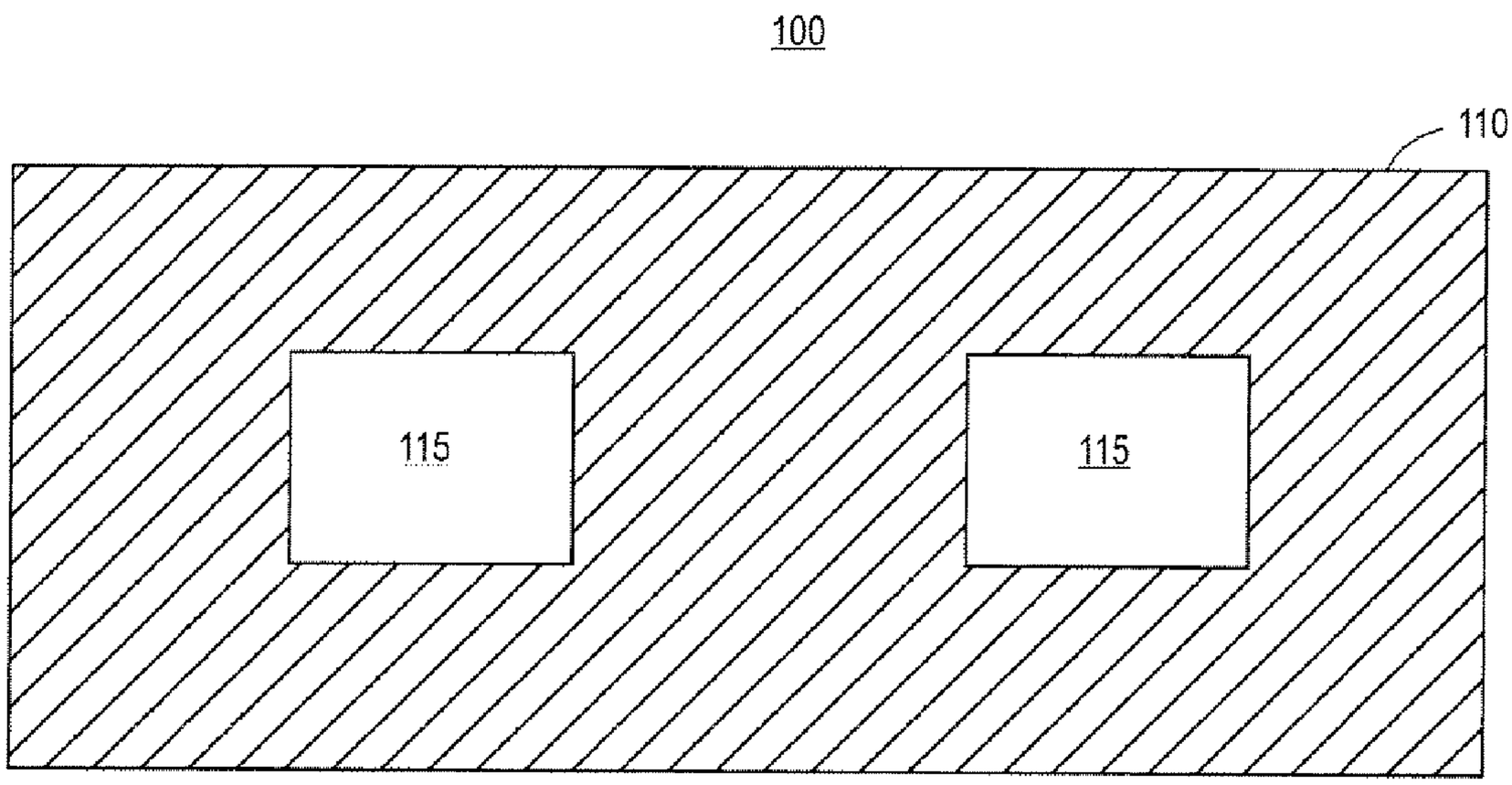


FIG. 1b

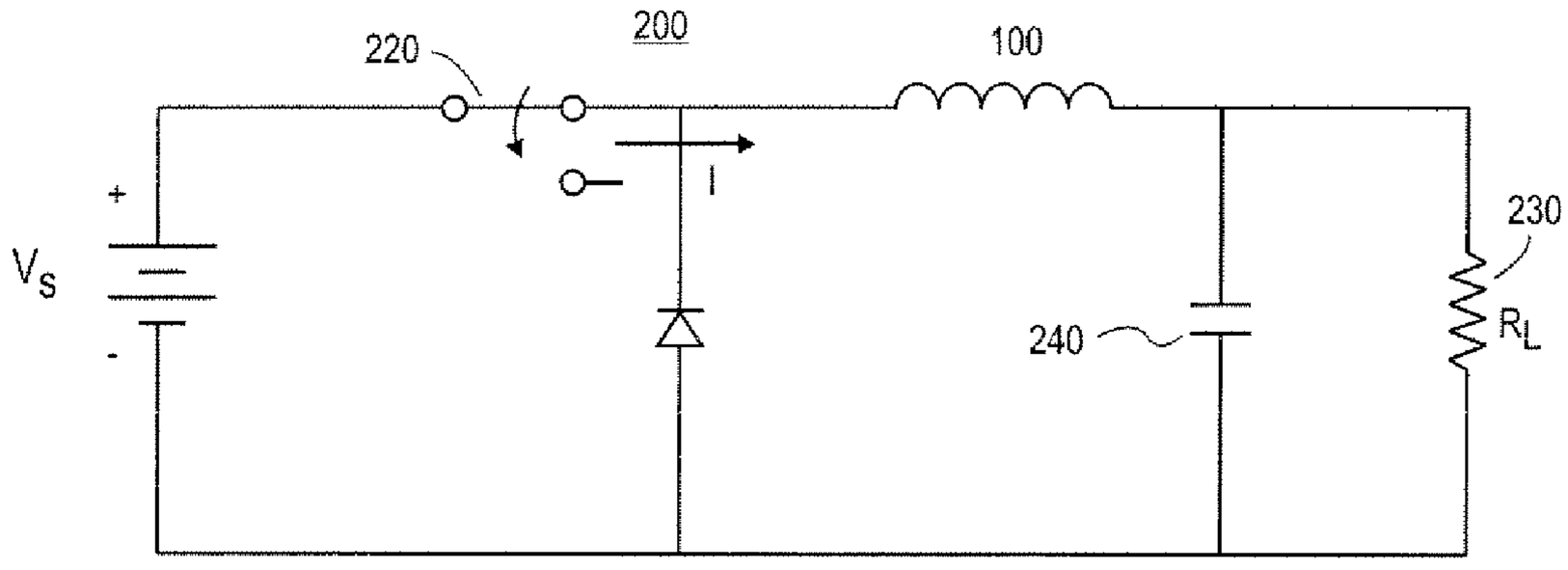


FIG. 2a

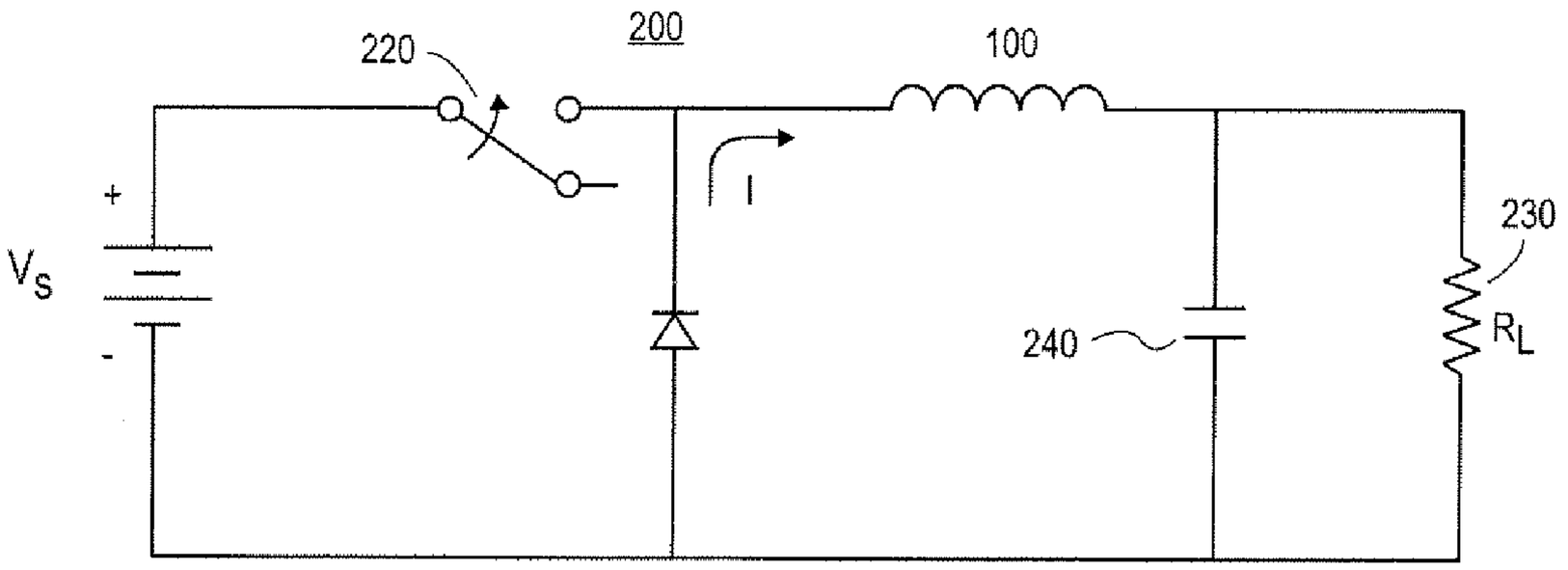


FIG. 2b

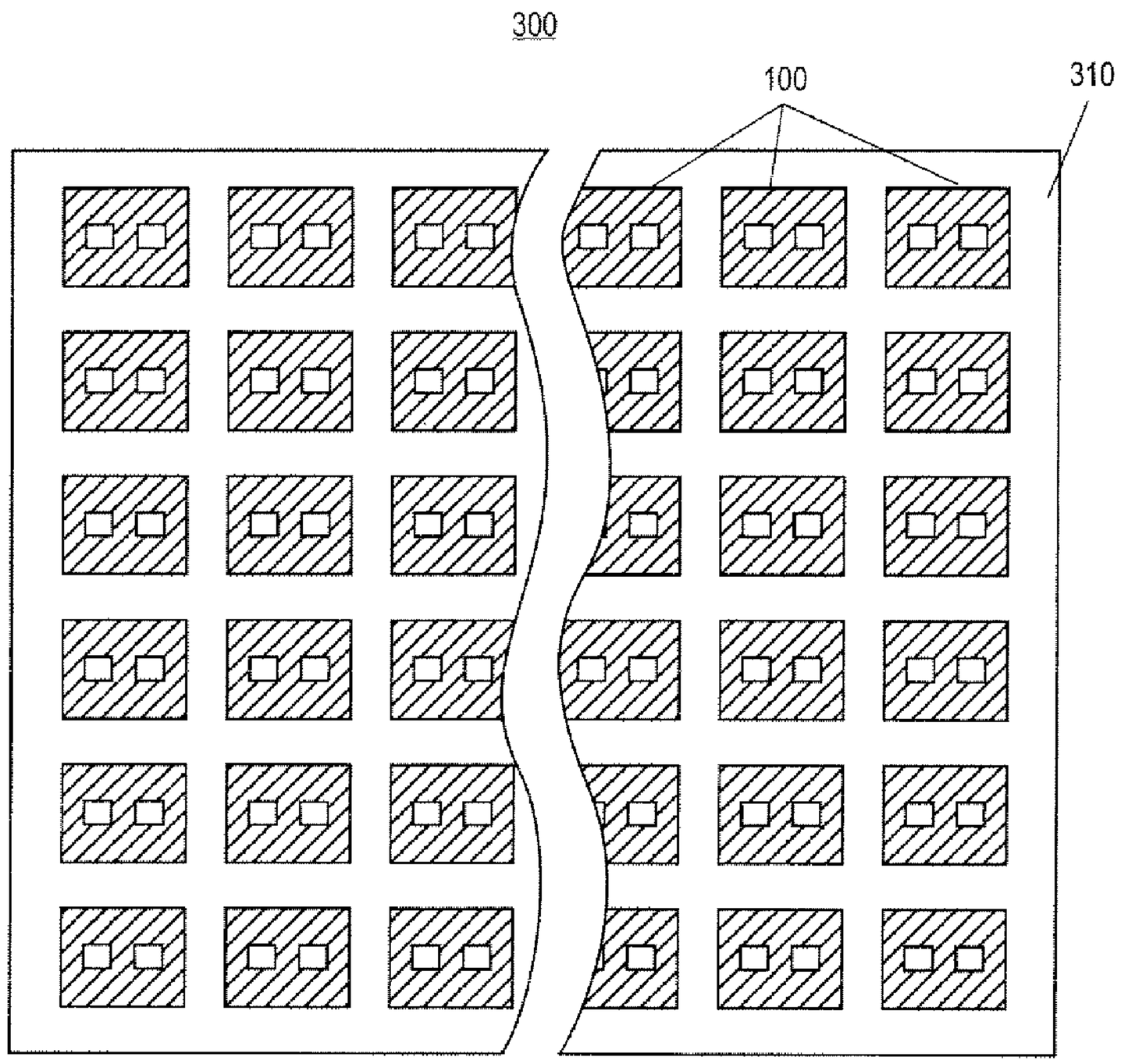


FIG. 3

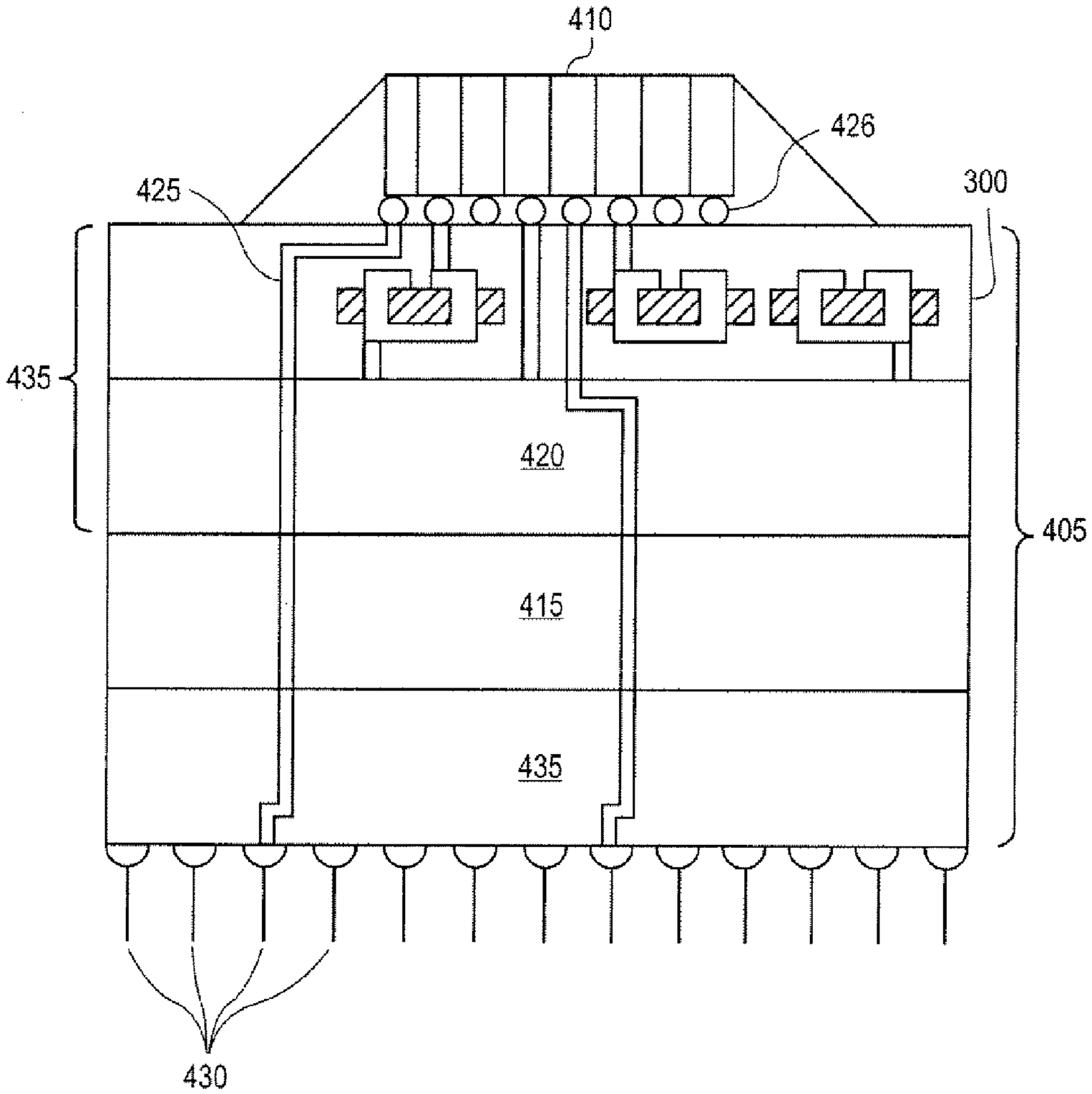


FIG. 4

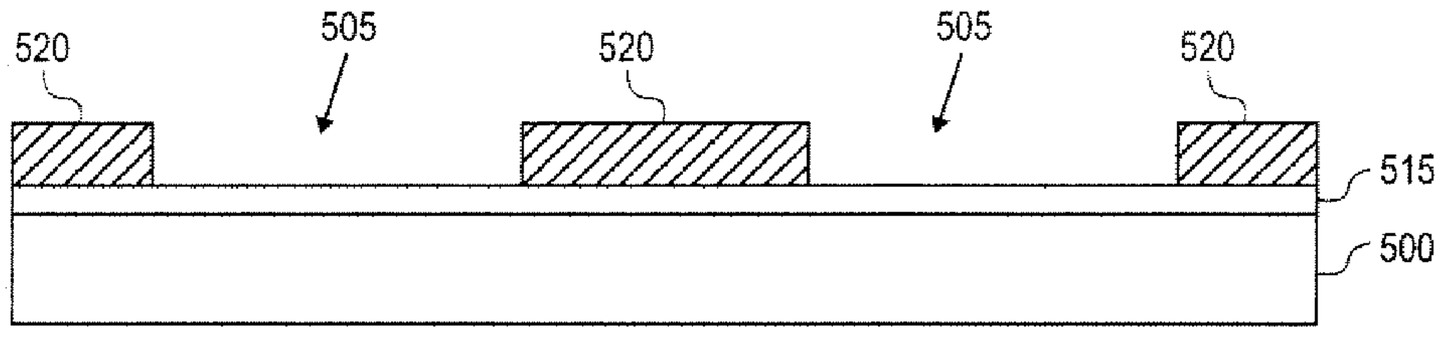


FIG. 5a

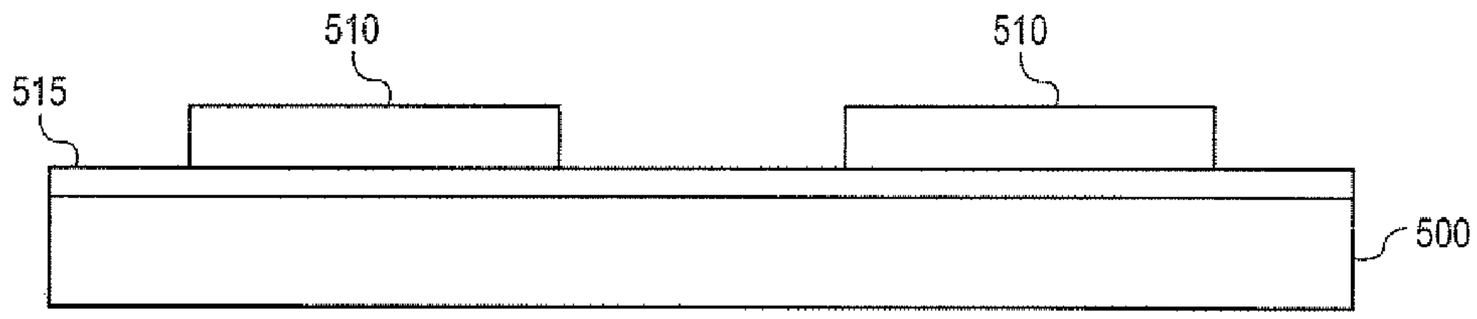


FIG. 5b

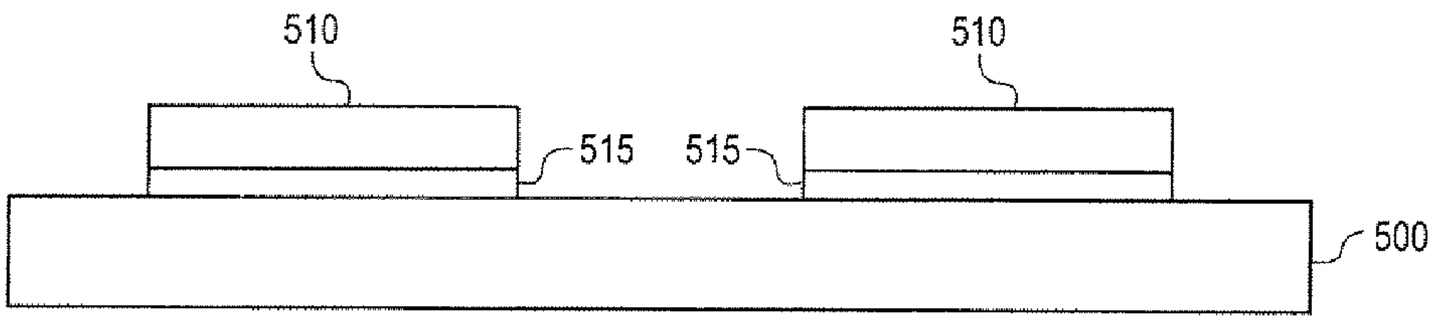


FIG. 5c

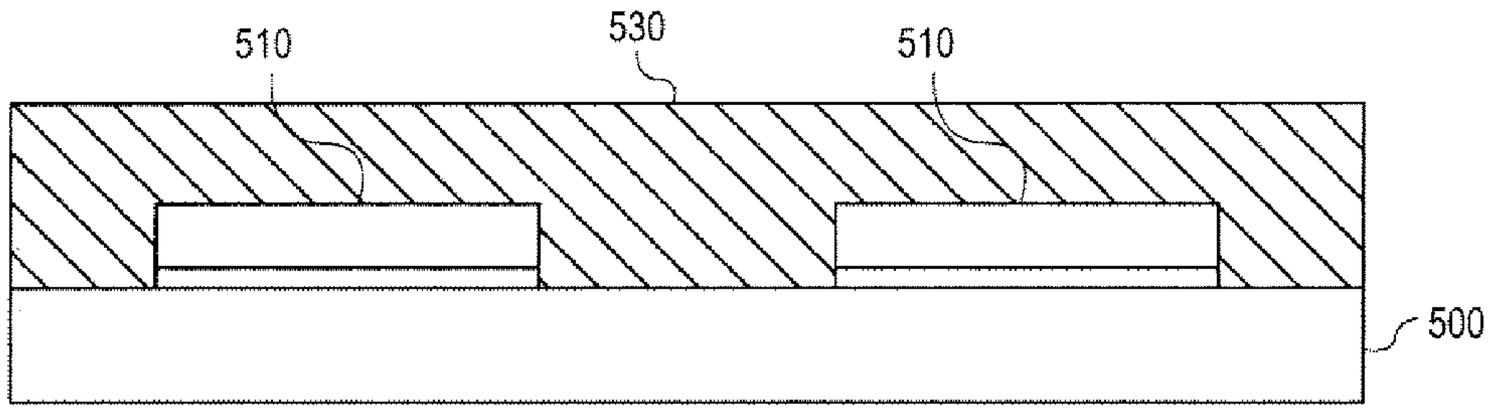


FIG. 5d

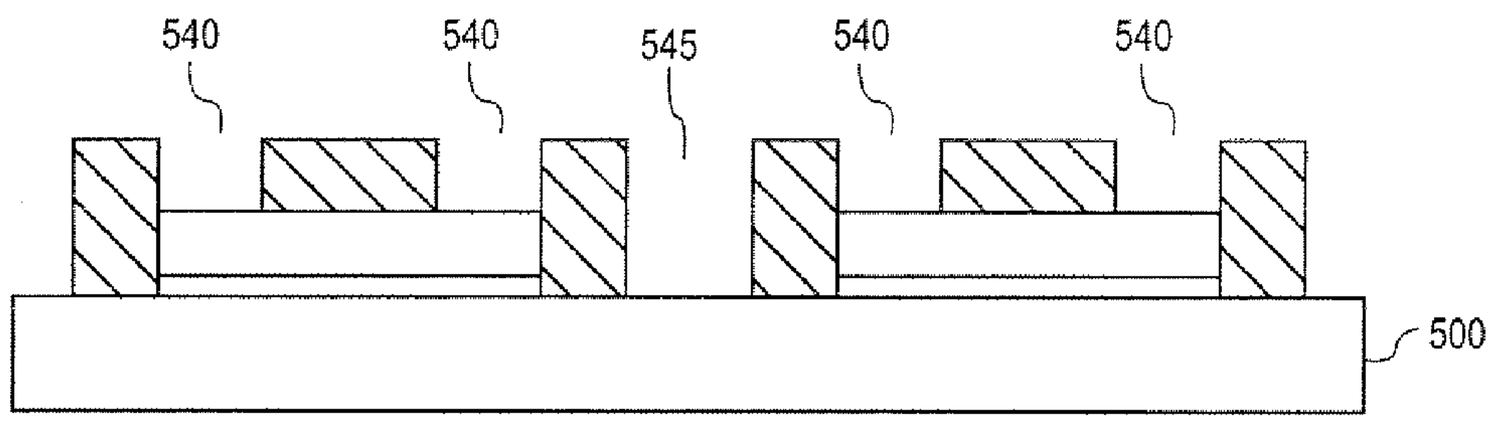


FIG. 5e

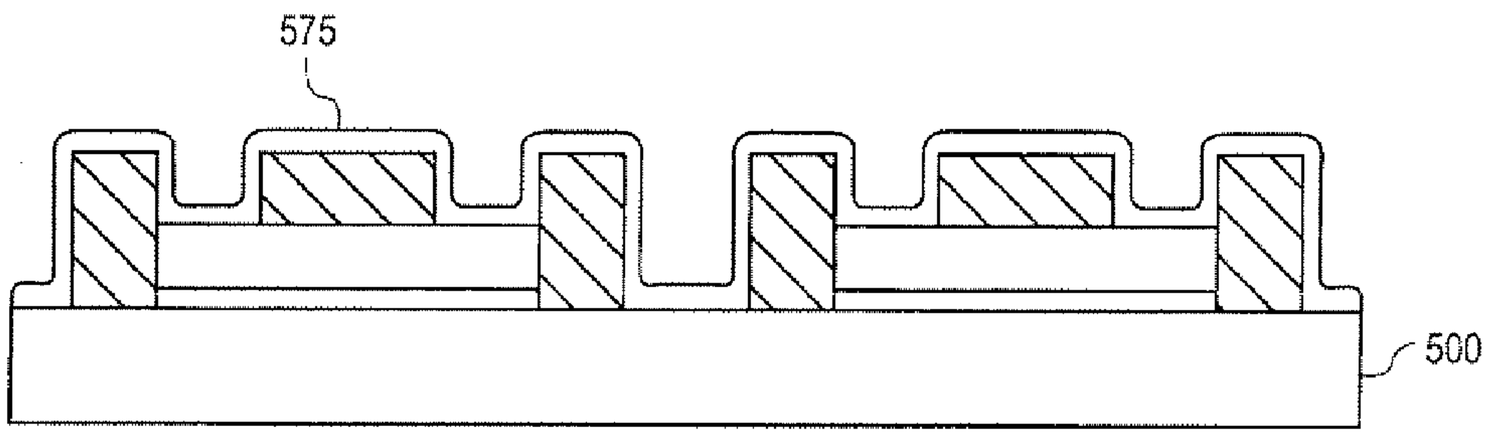


FIG. 5f

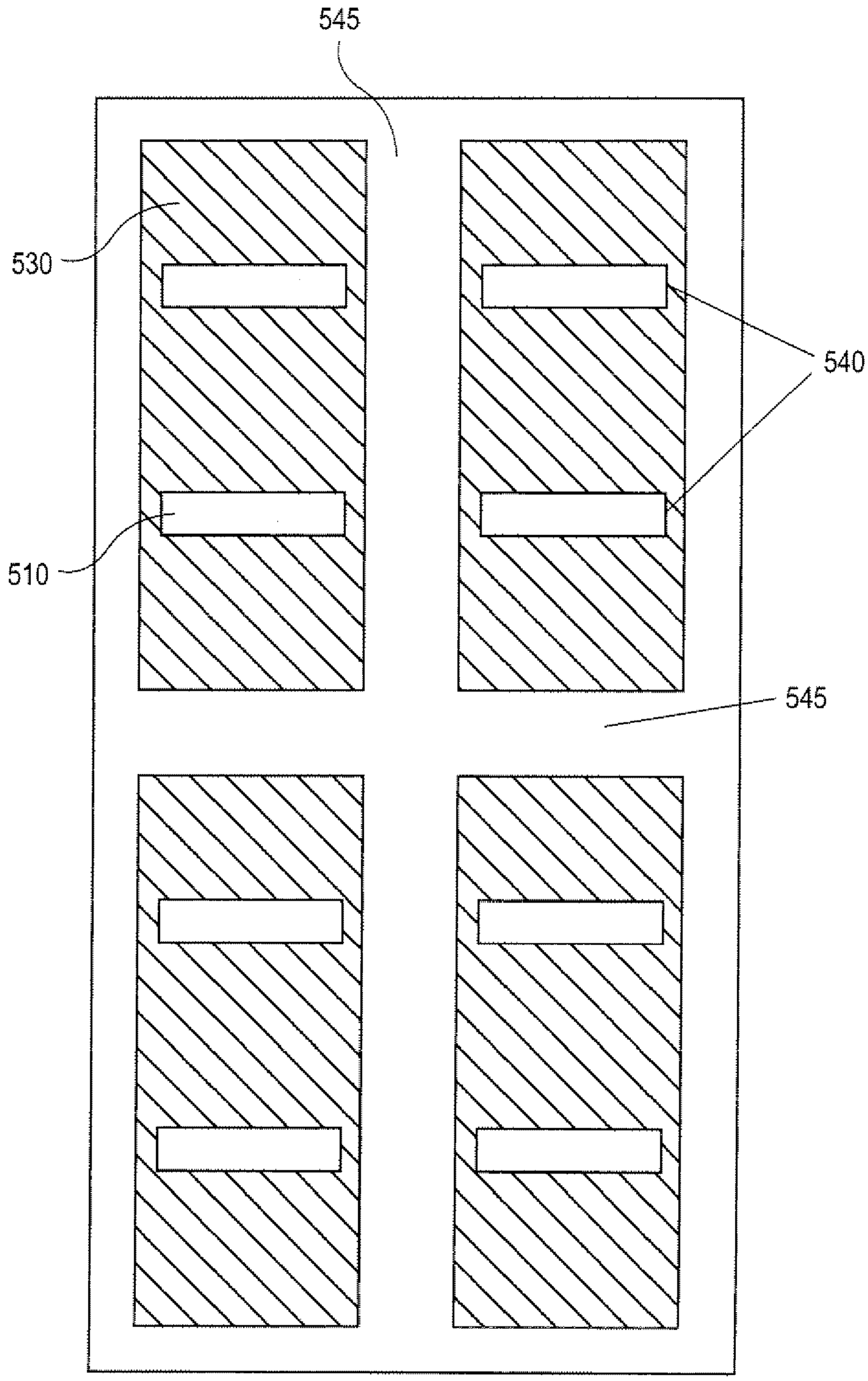


FIG. 5e'

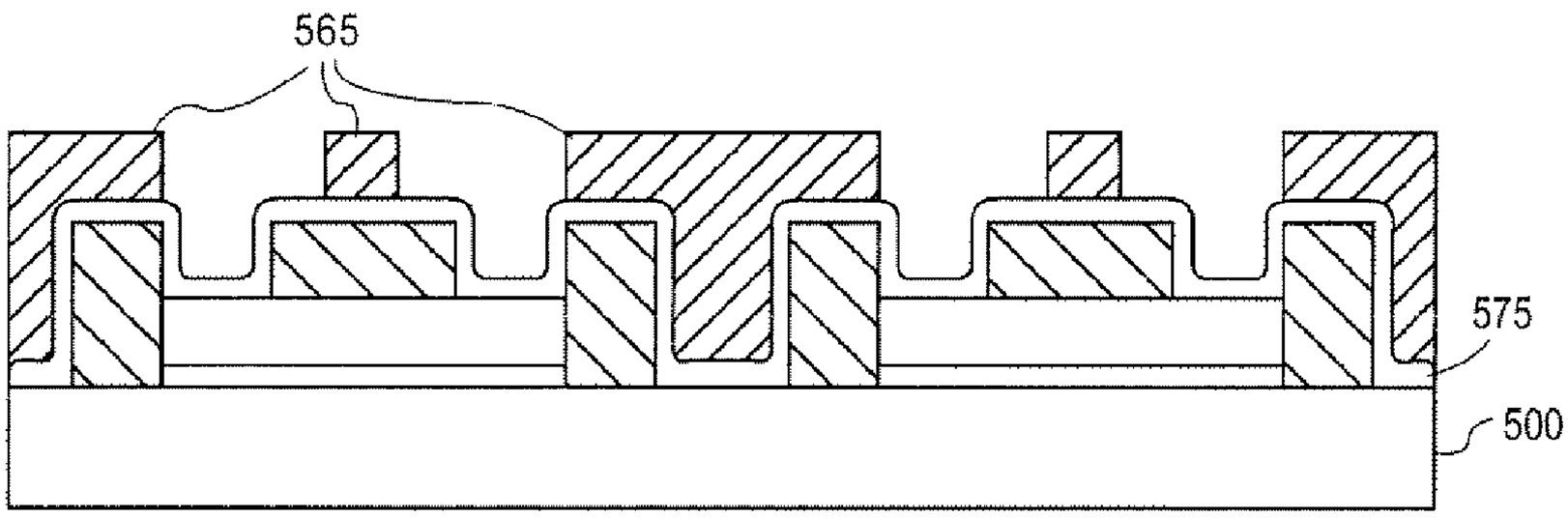


FIG. 5g

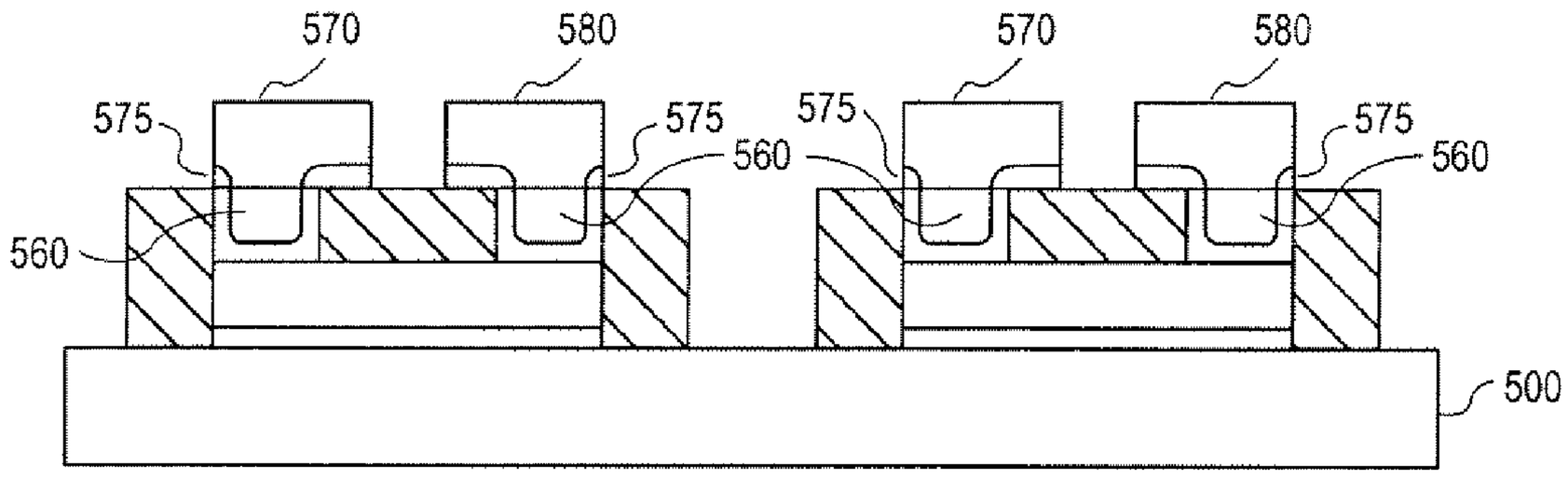


FIG. 5h

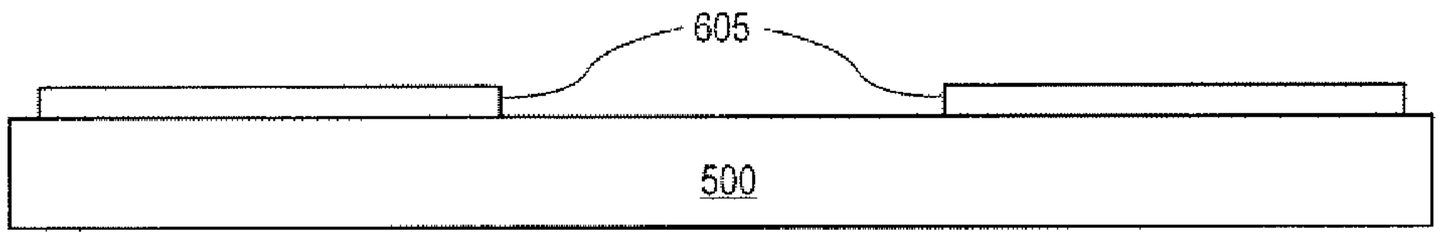


FIG. 6a

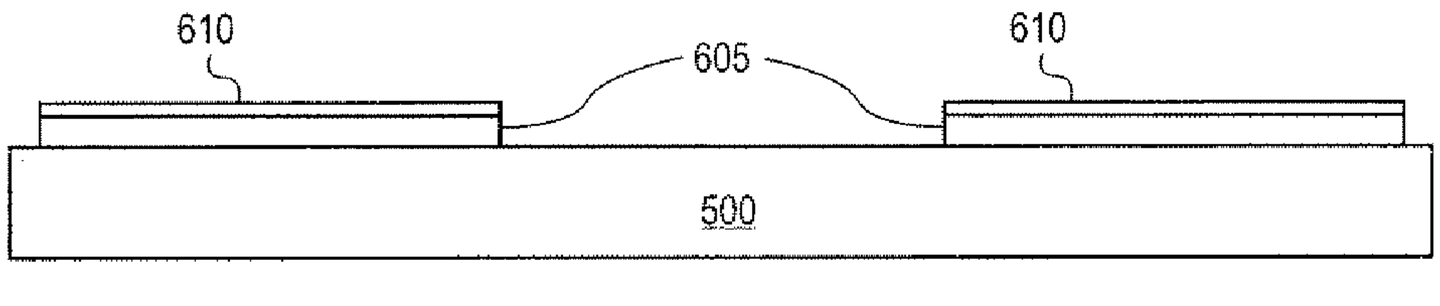


FIG. 6b

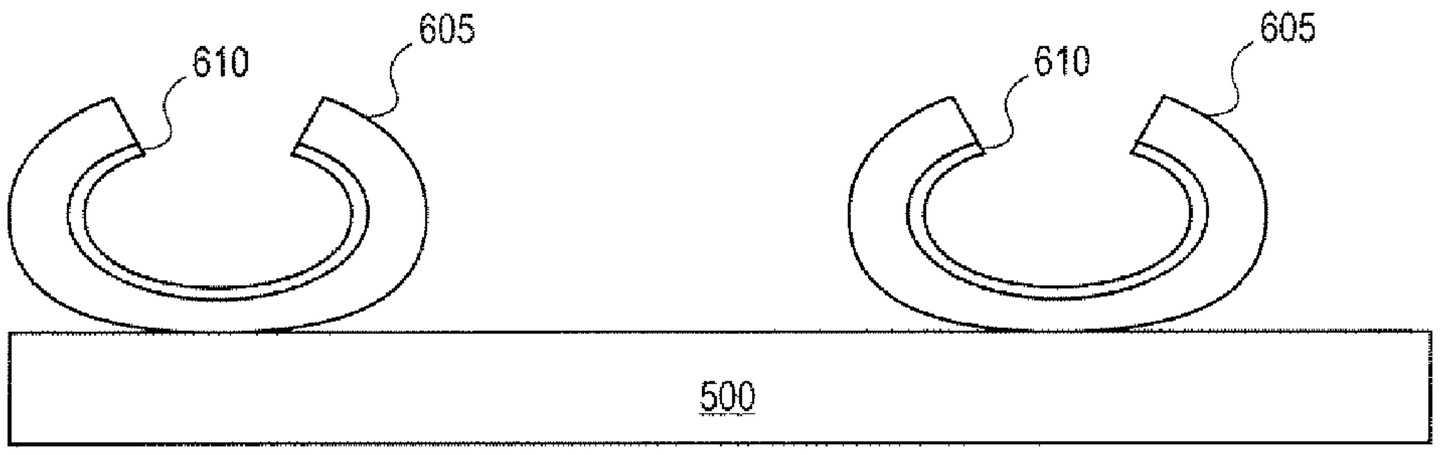


FIG. 6c

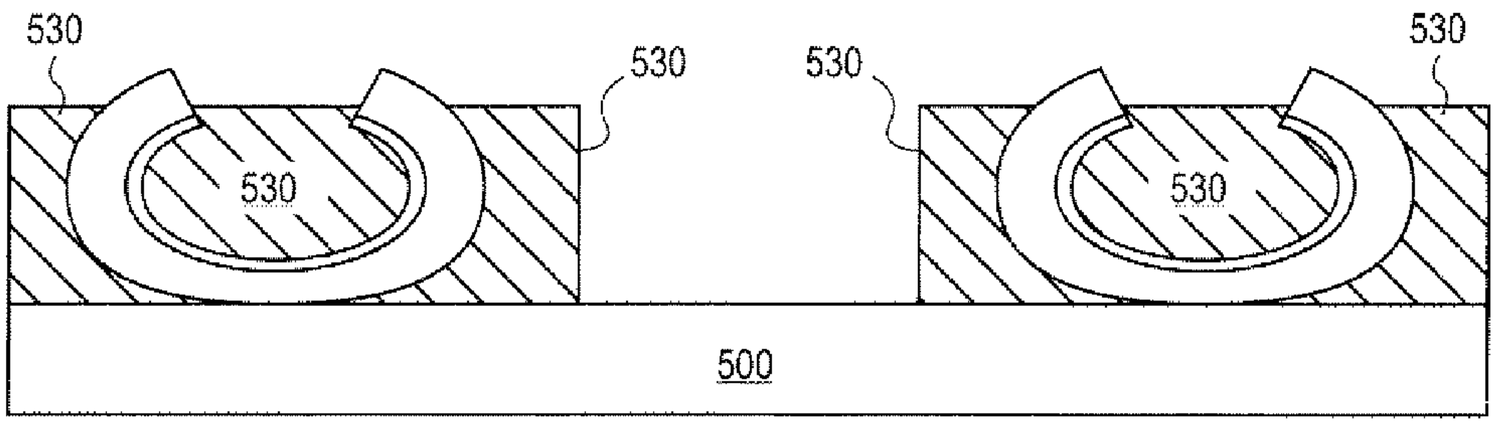


FIG. 6d

INTEGRATED INDUCTOR STRUCTURE AND METHOD OF FABRICATION

RELATED APPLICATIONS

[0001] This application is a divisional application of U.S. application Ser. No. 10/975,552, filed on Oct. 27, 2004, currently pending.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to the field of semiconductor devices and more specifically to an integrated inductor structure and its method of fabrication.

[0004] 2. Discussion of Related Art

[0005] The need for inductors in semiconductor design dictates the use of discrete inductors or spiral inductors. The discrete inductor is in an off-chip, off-package configuration and requires long interconnects to connect the inductor to the chip. These interconnects have high impedances and result in large ohmic losses. Also, discrete inductors require extra space outside the chip package, which is difficult to provide for in high-density circuit board fabrication.

[0006] Spiral inductors are created through windings of metal thin films, usually on a silicon substrate. The first drawback of spiral inductors includes the large area necessary to create large inductances, Another drawback of spiral inductors includes the tendency of the inductors to have high resistances. This high resistance deteriorates the quality factor of spiral inductors force the magnetic flux into the silicon substrate causing both eddy current losses and interference with devices.

SUMMARY

[0007] An inductor structure comprised of a magnetic section and a single turn solenoid. The single turn solenoid to contain within a portion of the magnetic section and circumscribed by the magnetic section.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. **1***a* is an illustration of a cross-sectional view of an embodiment of the inductor structure.

[0009] FIG. **1***b* is an illustration of an overhead view of an embodiment of the inductor structure.

[0010] FIG. **2***a* is a circuit diagram of an embodiment of a buck converter circuit with the switch in the on position.

[0011] FIG. **2***b* is a circuit diagram of an embodiment of a buck converter circuit with the switch in the off position

[0012] FIG. **3** is an illustration of an overhead view of an array of inductors.

[0013] FIG. **4** is an illustration of a cross-sectional view of an inductor structure incorporated into the build-up packaging layers of an integrated circuit package.

[0014] FIG. **5***a* is an illustration of a cross-sectional view of a seed layer and a photoresist mask formed on a package substrate for the formation of an inductor structure.

[0015] FIG. **5***b* is an illustration of a cross-sectional view of a package substrate and a conductive layer with a remaining seed layer for forming an inductor structure.

[0016] FIG. **5***c* is an illustration of a cross-sectional view of a package substrate and a conductive layer with a remaining exposed seed layer removed for forming, an inductor structure.

[0017] FIG. **5***d* is an illustration of a cross-sectional view showing a magnetic material formed over a conductive layer and a package substrate for forming of an inductor structure.

[0018] FIG. **5***e* is an illustration of a cross-sectional view of formed trench regions in a magnetic layer for forming an inductor structure.

[0019] FIG. **5***f* is an illustration of a cross-sectional view of a second seed layer formed over a magnetic layer and the trench formations for forming an inductor structure.

[0020] FIG. **5***g* is an illustration of a cross-sectional view of a second photoresist mask formed over the second seed layer for forming an inductor structure.

[0021] FIG. **5***h* is an illustration of a cross-sectional view of the formed sidewalls through a magnetic material with a second and third conductive layer formed over the magnetic material for forming an inductor structure.

[0022] FIG. **5***e* is an illustration of an overhead view of formed trench regions in a magnetic layer for forming an inductor structure.

[0023] FIG. **6***a* is an illustration of a cross-sectional view of formed conductive layers over a package substrate for forming an inductor structure.

[0024] FIG. **6***b* is an illustration of a cross-sectional view of metal-adhesion layers formed over conductive layers for forming an inductor structure.

[0025] FIG. **6***c* is an illustration of a cross-sectional view of a bowl shape formed by conductive layers after subjected to thermal stress for forming an inductor structure.

[0026] FIG. **6***d* is an illustration of a cross-sectional view of bowl shaped conductive layers with magnetic material formed within and around the conductive layers for forming an inductor structure.

DETAILED DESCRIPTION

[0027] In the following description numerous specific details are set forth in order to provide an understanding of the claims. One of ordinary skill in the art will appreciate that these specific details are not necessary in order to practice the disclosure. In other instances, well-known semiconductor fabrication processes and techniques have not been set forth in particular detail in order to not unnecessarily obscure the present invention.

[0028] The present invention is an integrated inductor structure **100** and its method of fabrication. In an embodiment, the integrated inductor structure **100**, as shown in FIG. **1***a* and FIG. **1***b*, is a solenoid structure **115** with a single turn that is filled with and is surrounded by magnetic material **110**. The magnetic material **110** enables a reduction of the inductor size because the magnetic material **110** has a relative magnetic permeability greater than one[HB1]. This results in a higher inductance per area than an inductor

without magnetic material. In an embodiment of the inductor structure **100**, the area can be about 0.01-9 mm^2 with an inductance in the nanohenry (nH) range. The dimensions of the structure of the inductor can be altered to meet specific inductance and area requirements.

[**0029**] Another benefit of the magnetic material **110** is the encapsulation of the magnetic flux within the plane of the inductor structure **100**, leading to a reduction of interference with surrounding components. In an embodiment, the single turn solenoid structure of the present invention enables an inductor with a low resistance. The low resistance and the capability of the inductor of the present invention to provide inductances in the nanohenry range permit the use of the inductor in applications such as power delivery for integrated circuits.

[**0030**] One such power application includes the use in a buck converter circuit **200** as shown in FIGS. **2***a* and **2***b*. In the buck converter circuit **200** the inductor structure **100** and the capacitor **240** act as energy storage devices when the switch **220** is in the on position as shown in FIG. **2***a*. Once the switch **220** is placed in the off position, as shown in FIG. **2***b*, the inductor structure **100** acts like a source and works to maintain the current through the load resistor **230**. Similarly, the capacitor **240** works to maintain the voltage across the load resistor **230**.

[**0031**] In the embodiment of FIG. **1***a*, the layer of magnetic material **110** is formed around and within a conductive material **115** in a single loop configuration. The conductive material **115** can be formed from such materials including copper, tungsten, or aluminum. FIG. **1***b* shows the overhead view of one embodiment where the magnetic material **110** surrounds the conductive material **115** in the longitudinal plane of the inductor structure **100**. In an embodiment the inductor structure **100** can be formed having an area of 0.11 mm^2 with a resistance less than **10** mΩ and an inductance of 10.1 nH. An embodiment of the inductor structure **100** can have a magnetic material **110** with the height of approximately 20-30 microns. This embodiment includes a conductive material **115** in the single loop configuration with a length of approximately 200-1000 microns, a width of approximately 350-450 microns, and a thickness of the conductive material **115** of approximately 20 microns.

[**0032**] In one embodiment the magnetic material **110** is composed of a soft magnetic material. Soft magnetic materials are easily magnetized and demagnetized. These properties make soft magnetic materials useful for enhancing or channeling flux produced by an electric current. One parameter used to distinguish soft magnetic materials is the relative permeability, The relative permeability indicates the amount of magnetic flux density in a material over that contained in a vacuum when in the presence of a magnetic force. In an embodiment of the inductor structure **100**, the relative permeability is approximately 95-900. Generally, the relative permeability of an embodiment of the inductor structure **100** is approximately 100-500 and typically approximately 300. As mentioned earlier, materials with magnetic properties are used because the high permeability creates an increased magnetic flux resulting in a higher inductance over inductors without material with magnetic properties. In some embodiments of the inductor structure **100**, the magnetic material **110** is a magneto-dielectric such as CoFHfO. The magneto-dielectric in another embodiment is formed from magnetic nanoparticles embedded into a dielectric material. In one embodiment nanoparticles can be distributed throughout a host material such as a polymer host.

[**0033**] As shown in FIG. **3**, an embodiment of the inductor structure **100** includes fabrication of an inductor array **300** formed from a predetermined number of the inductor structures of the present invention. In such an array, a dielectric material **310**, including an Ajinomoto buildup film (ABF); a ceramic; or a solder resist, can be used to separate an inductor structure **100** from one another within the inductor array **300**. One embodiment of an inductor array **300** can include approximately 9-10,000 inductor structures of the present invention.

[**0034**] In an inductor array **300** embodiment, the inductor structure **100** can be connected to another inductor structure **100** in series, in parallel, and/or to devices external to the array. Series connections of an inductor structure **100** can be used to create inductance values equal to the sum of the inductors connected in series. Also, the inductor structure **100** in the inductor array **300** can be connected to another inductor structure **100** in parallel to tune the effective inductance of the combined inductor structure **100** connected together to a certain predetermined inductance. An individual inductor structure **100** in the inductor array **300**, a combination of serially connected inductor structures **100**, a combination of inductor structures **100** connected in parallel, or a combination of inductor structures **100** connected in series and in parallel can be used to connect to devices external to the inductor array **300**. Examples of devices external to the inductor array **300** that could be connected to the inductor structure **100** include capacitors, voltage regulator modules, resistors, transistors and other devices useful in electronic design. Embodiments of the inductor array **300** can have the inductor structure **100** orientated on its side, upside down, or in other positions.

[**0035**] As shown in FIG. **4**[HB**2**], one embodiment of the inductor structure **100**, such as an inductor array **300**, can be fabricated into a build-up layer **435** of an integrated circuit package substrate **405**. This build-up layer **435** could contain passive components including parallel-plate capacitors to form part of a power converter, such as a buck converter circuit **200**. An embodiment of an inductor structure **100** in an inductor array **300** or a combination of connected inductors contained in an inductor array **300** contained within a build-up layer **435** can be used in conjunction with an array of voltage regulator modules (VRMs) **420** incorporated into a separate build-up layer **435**. Such an embodiment can be used as a part of a power conversion circuit, such as a buck converter circuit **200**, to power a die **410**. [HB**3**]One embodiment positions the inductor array **300** between a die **410** and an array of VRMs **420** as illustrated in FIG. **4**. The voltage regulator elements of a build-up layer **435**[HB**4**] convert a higher supply voltage to a lower voltage that is then coupled to the power grid of the die **410**. Since the voltage regulators within the build-up layer **435** are separated from the circuits on the die **410** by the distance covered by the connections, which can be on the order of a few tens of microns in length, the lowered-voltage supply can be distributed in a manner minimizing IR and Ldi/dt voltage drops.

[**0036**] In an embodiment, an inductor structure **100** or an inductor array **300** can be coupled to a die **410** by die

bonding techniques including flip-chip solder bumps **426**, bumpless build-up layer (BBUL), or wire bond. In a BBUL embodiment, the package is built up around the die **410**, so the die is contained within the packaging substrate core **415**. The die **410** is then connected to a build-up layer **435** and/or input/output (I/O) pins **430** using interconnections **425**. The two-dimensional interface and minimal separation distance between a build-up layer **435** and a die **410** helps ensure a further reduction of IR voltage drops and supply bottlenecks when compared to other die bonding techniques.

[**0037**] As illustrated in FIG. **4**, the die **410** can be connected directly to I/O pins **430** through interconnects **425** including copper I/O interconnects or thru-vias that transverse the package substrate **405**. The interconnects **425** within an integrated circuit package substrate **405** can connect an inductor structure **100**, inductor array **300**, a die **410** or other devices to external devices on a motherboard through the I/O pins **430**. These I/O pins **430** can include but are not limited to metal leads, solder bumps, or wire in formations such as a pin grid array, a ball grid array, a ceramic column grid array, a leadless grid array, or a land grid array.

[**0038**] Because the build-up layer **435** is positioned in between the I/O pins **430** and the die **410**, the build-up layer **435** can be made thin enough to allow a set of thru-vias to penetrate through the layer. The thru-vias are interconnections **425** that traverse the entire build-up layer **435** or packaging core **415**, while being insulated from the layer. In an embodiment, the thru-vias are situated around the perimeter of the build-up layer **435** and do not affect the devices contained within the build-up layer **435**. An alternative embodiment does not include thru-vias. Instead, the devices in the build-up layer **435** and I/O pins **430** and the die **410** are coupled via I/O interconnect wires that run beyond the edge of the build-up layer **435**.

[**0039**] One fabrication method of the inductor structure **100** can be achieved through a modified version of a conventional high-density interconnect process as illustrated in FIGS. **5***a*-**5***h*. FIG. **5***a* illustrates the formation of the first conductive layer **510** over a substrate **500** such as a printed circuit board by first forming a first seed layer **515** such as a copper seed layer. A technique to form the first conductive layer **510** includes forming a first photoresist mask **520** using well-known masking, exposing, and developing techniques over the substrate **500** to define the location **505** of the first conductive layer **510**. In an embodiment, the first conductive layer **510** can be formed of a material such as copper, tungsten, or aluminum. In an embodiment using copper, well-know techniques such as electroplating can be used. The first photoresist mask **520** is removed using well-known techniques to form the structure illustrated in FIG. **5***b*. The exposed first seed layer **515** is etched away to produce the formation as shown in FIG. **5***c*. A layer of magnetic material **530** is formed over the package substrate layer **500** and the first conductive layer **510** as illustrated in FIG. **5***d*.

[**0040**] One method for forming the magnetic material **530** includes laminating many layers of a magneto-dielectric sheet until the desired thickness is achieved. In an embodiment the thickness of the magnetic material can be approximately 30 microns. A second method used to form a magneto-dielectric sheet includes co-sputtering a polymer with a magnetic material. Another method of forming the magnetic material **530** includes alternating layers of magnetic material with insulating material. The combination of the layers helps mitigate the effects of eddy currents when the inductor structure **100** is used at high frequencies of operation. In yet another method, the magnetic material **530** can be formed by sputtering until the desired height of the material **530** is formed. One method of forming the magnetic material **530** includes a step to planarize the magnetic material **530** after the material is deposited.

[**0041**] Next, as shown in a cross-sectional view in FIG. **5***e* and the overhead view in FIG. **5***e'*, sidewall trenches **540** and isolation trenches **545** between each inductor structure **100** are formed by etching or typically by laser blazing[HB5] through the magnetic material **530** until the first conductive layer **510** is exposed. In one method the conductive sidewalls **560** can be formed using vias. These sidewall vias can be formed of copper using well-known plating techniques. One embodiment of the method can employ a series of vias stacked upon each other until the sidewalls **560** are formed through the magnetic layer, Another method employs vias spaced apart from one another at predetermined distances.

[**0042**] FIGS. **5***f* and **5***g* illustrate a step of one technique used to form the sidewalls **560**, the second conductive layer **570**, and the third conductive layer **580**. As FIG. **5***f* shows, the first step includes forming a second seed layer **575** over the formation shown in FIG. **5***e*. Once the second seed layer **575** is formed, a second photoresist mask **565** illustrated in FIG. **5***g* is formed to define the second conductive layer **570** and the third conductive layer **580** illustrated in FIG. **5***h*. The second photoresist mask **565** also prevents conductive material from filling the isolation trench **545**. The sidewall trenches **540** are then filled with a conductive material to form conductive sidewalls **560** coupled to the first conductive layer **510** as illustrated in FIG. **5***h*. A second conductive layer **570** is formed over one conductive sidewall **560** such that the second conductive layer **570** is coupled to a conductive sidewall **560**. The second conductive layer **570** overlays a portion of the magnetic material **530** toward the other conductive sidewall **560**. A third conductive layer **580** is formed to couple with the other conductive sidewall **560**. The third conductive layer **580** also covers part of the center portion of the magnetic material **530** as shown in FIG. **5***h*.

[**0043**] One method incorporates the creation of the second conductive layer **570**, third conductive layer **580**, and the sidewalls **560** into one step after the formation of a second photoresist mask **565**. After the second photoresist mask **565** defines the pattern for the second conductive layer **570** and third conductive layer **580**, a conductive material can be formed using well-known techniques such as electroplating. Once the second conductive layer **570**, the third conductive layer **580**, and the sidewalls **560** are formed, the second photoresist mask **565** can be removed by well-known techniques resulting in the structure shown in FIG. **5***h*.

[**0044**] In a method to form the inductor structure **100**, a dielectric layer is formed over the structure shown in FIG. **5***h* and within the isolation trench **545**. The dielectric layer can be an Ajinomoto buildup film (ABF), a ceramic, or a solder resist. In an embodiment using a solder resist for the dielectric layer, a further step of creating openings in the solder resist layer to expose circular areas of the conductive material of the second conductive layer **570** and the third

conductive layer **580** could be used. Once the openings are formed, the openings are then filled with a conductive material. This conductive material can be formed by electrolytic or electroless plating and creates a contact point for interconnecting with other devices.

[**0045**] In another method of fabrication, the conductive layer of the inductor structure **100** is formed in one step, as shown in FIGS. **6***a-d*. FIG. **6***a* shows the result of using standard electroplating methods to form a conductive layer **605** over a package substrate **500**. A metal-adhesion layer **610** is sputtered on the top of the conductive layer **605** to act as a mechanism to delaminate the conductive layer **605** from the package substrate **500** as shown in FIG. **6***b*. The metal-adhesion layer **610** is selected to have a greater adhesion with the conductive layer **605** than the adhesion between the conductive layer **605** and the package substrate **500**. Subjecting the conductive layer **605** to thermal stresses will delaminate the conductive layer **605** from the package substrate **500**. This process forms the conductive layer **605** into a bowl shaped structure as illustrated in **6***c*. As shown in FIG. **6***d*, a magnetic material **530** is then formed inside and around the conductive layer **605**.

We claim:

1. A method of forming an inductor structure comprising:

forming an open conductive loop; and

forming a magnetic material contained within said open conductive loop and to encompass said open conductive loop.

2. A method of forming an inductor structure of claim 1 used to form an inductor in a build-up packaging layer of an integrated circuit package.

3. A method of forming an inductor structure of claim 1 coupled to an integrated device.

4. A method of forming an inductor comprising:

forming a magnetic layer; and

forming a single turn solenoid to contain within a portion of said magnetic layer and circumscribed by said magnetic layer.

5. The method of claim 4 wherein said magnetic layer consists of CoFHfO.

6. The method of claim 4 wherein said single turn solenoid consists of copper.

7. The method of claim 6 used to form an inductor in a build-up packaging layer of an integrated circuit package.

8. The method of claim 4 wherein the magnetic layer is formed by a laminating technique.

9. A method of forming an inductor comprising:

forming a metal layer;

shaping said metal layer to form a bowl shape; and

forming a magnetic layer onto and around said metal layer.

10. The method of claim 9 wherein said metal layer consists of copper.

11. The method of claim 9 wherein said magnetic layer is formed by a sputtering technique.

12. The method of claim 9 wherein said magnetic layer has a permeability of about 300.

13. The method of claim 12 used to form an inductor in a build-up packaging layer of an integrated circuit package and coupled to an integrated device.

14. A method of forming an inductor structure comprising:

forming a first conductive layer;

forming a magnetic layer over said first conductive layer;

forming a first conductive sidewall and a second conductive sidewall through said magnetic layer and adjoined to said first conductive layer;

forming a first conductive portion adjoined to said first conductive sidewall, said first conductive portion formed opposite said magnetic layer from said first conductive layer; and

forming a second conductive portion adjoined to said second conductive sidewall, said second portion formed opposite said magnetic layer from said first conductive layer.

15. The method of forming an inductor structure of claim 14 further comprising planarizing said magnetic layer.

16. The method of forming an inductor structure of claim 14 wherein the first conductive layer is formed by an electroplating technique.

17. The method of forming an inductor structure of claim 14 wherein said first conductive sidewall and said second conductive sidewall are formed by vias.

18. A method of forming an inductor on a package substrate, said method comprising:

forming a first seed layer on the package substrate;

electroplating a first conductive layer on said substrate;

depositing a layer having magnetic properties over said first conductive layer;

laser drilling a via array in said layer having magnetic properties to form opposite first and second sidewalls coupled to said first conductive layer;

forming a second seed layer on said via array and said layer having magnetic properties;

forming a dry film resist over said second seed layer;

creating openings in said dry film resist in predetermined locations;

electroplating a second conductive layer in said openings; and

removing said dry film resist and said second seed layer.

19. The method of claim 18 used to form an inductor coupled to an integrated circuit die and a voltage regulator module.

20. The method of claim 19, wherein said layer having magnetic properties is a magneto-dielectric material with a relative permeability of approximately 300.

21. A method of forming an inductor structure into an array comprising:

forming a plurality of magnetic sections; and

forming a plurality of single turn solenoids, each one of said plurality of single turn solenoids to contain within a portion of one of said plurality of said magnetic sections and circumscribed by one of said plurality of magnetic sections.

22. The method of forming an inductor structure into an array of claim 21 further including the step of forming a dielectric material between said plurality of magnetic sections.

23. The method of forming an inductor structure into an array of claim 22 wherein said dielectric material is selected from a group consisting of an Ajinomoto buildup film (ABF), a ceramic, and a solder resist.

24. The method of forming an inductor structure into an array of claim 23 wherein said plurality of magnetic sections is formed from a magneto-dielectric.

25. The method of forming an inductor structure into an array of claim 21 used to form an inductor array used in conjunction with a voltage regulator module array.

26. A method of forming an inductor structure included in an inductor array comprising:

forming a plurality of first conductive layers;

forming a plurality of magnetic sections over said plurality of first conductive layers;

forming a plurality of first conductive sidewalls and a plurality of second conductive sidewalls through said magnetic sections, each one of said plurality of first and second conductive sidewalls adjoined to one of said plurality of first conductive layers;

forming a plurality of first conductive portions, each one of said plurality of first conductive portions adjoined to one of said plurality of first conductive sidewalls, each one of said plurality of first conductive portions formed opposite one of said plurality of magnetic sections from one of said plurality of first conductive layers; and

forming a plurality of second conductive portions, each one of said plurality of second conductive portions adjoined to one of said plurality of second conductive sidewalls, each one of said plurality of second conductive portions formed opposite one of said plurality of magnetic sections from one of said plurality of first conductive layers.

27. The method of claim 26 further including the step of forming a dielectric material between each of said plurality of magnetic sections and over said plurality of first and second conductive portions.

28. The method of claim 27 used to fabricate an inductor array between a voltage regulator module array and an integrated circuit die.

29. The method of claim 27 wherein said dielectric material is a solder resist.

30. The method of claim 29 further comprising forming openings in said dielectric material to expose a portion of said plurality of first and second conductive portions and filling said openings with conductive material.

31. The method of claim 30 wherein said openings are filled by electrolytic plating.

32. The method of claim 26 wherein said plurality of first conductive sidewalls and said plurality of second conductive sidewalls are formed by vias.

33. The method of claim 27 wherein said plurality of magnetic sections have a relative permeability about 300.

* * * * *