US 20060071304A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2006/0071304 A1**

(43) **Pub. Date: Apr. 6, 2006**

Jagannathan et al.

(54) **STRUCTURE AND LAYOUT OF A FET PRIME CELL**

(75) Inventors: **Basanth Jagannathan**, Beacon, NY (US); **John J. Pekarik**, Underhill, VT (US); **Christopher M. Schnabel**, Poughkeepsie, NY (US)

Correspondence Address:
GREENBLUM & BERNSTEIN, P.L.C.
1950 ROLAND CLARKE PLACE
RESTON, VA 20191 (US)

(73) Assignee: **INTERNATIONAL BUSINESS MACHINES CORPORATION**, Armonk, NY (US)

(21) Appl. No.: **10/711,640**

(22) Filed: **Sep. 29, 2004**

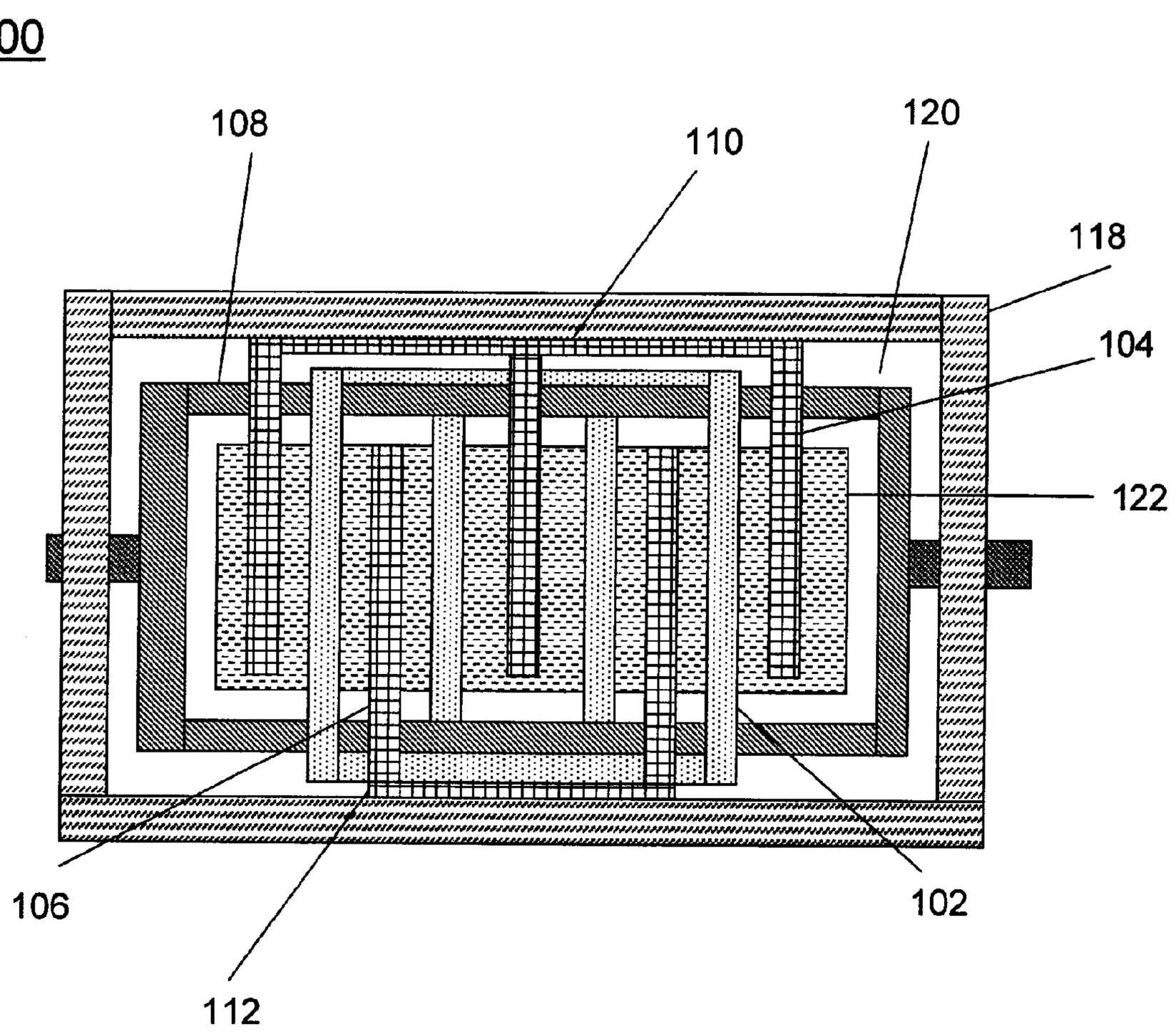
Publication Classification

(51) **Int. Cl.**
H01L 23/552 (2006.01)

(52) **U.S. Cl.** **257/659**

(57) **ABSTRACT**

A structure, apparatus and method for a FET prime cell surrounded by a conductor is provided. The surrounding conductor includes a substrate contact arranged proximate a source of the FET. The surrounding conductor may be a ring substrate contact arranged within the substrate of the FET in electrical communication with elongated sources of the FET. No external contacts are needed to the ring substrate contact because no current flows therethrough while the ring substrate contact may act as a collection source for noise such as stray currents.



100

FIG 1

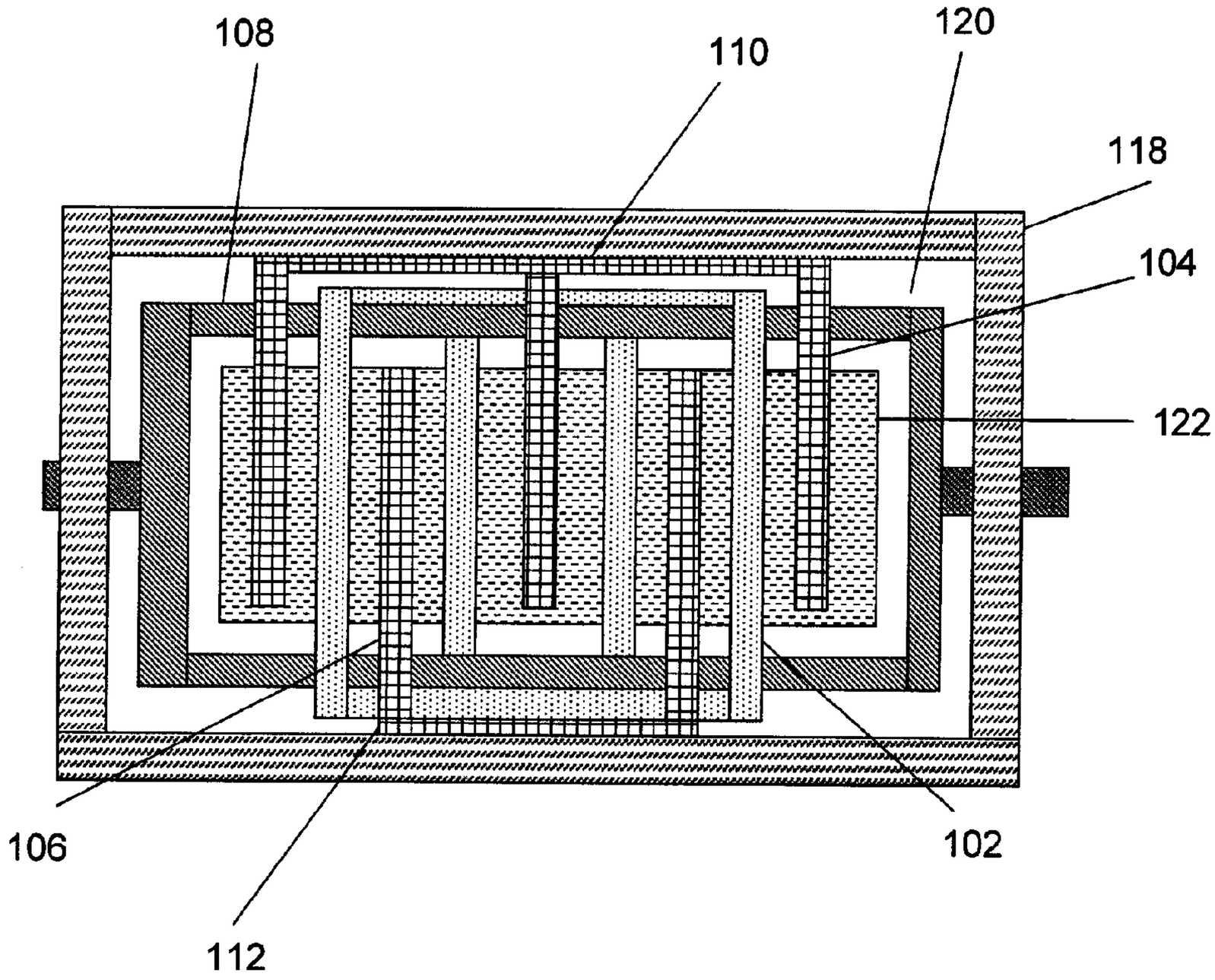


FIG 2

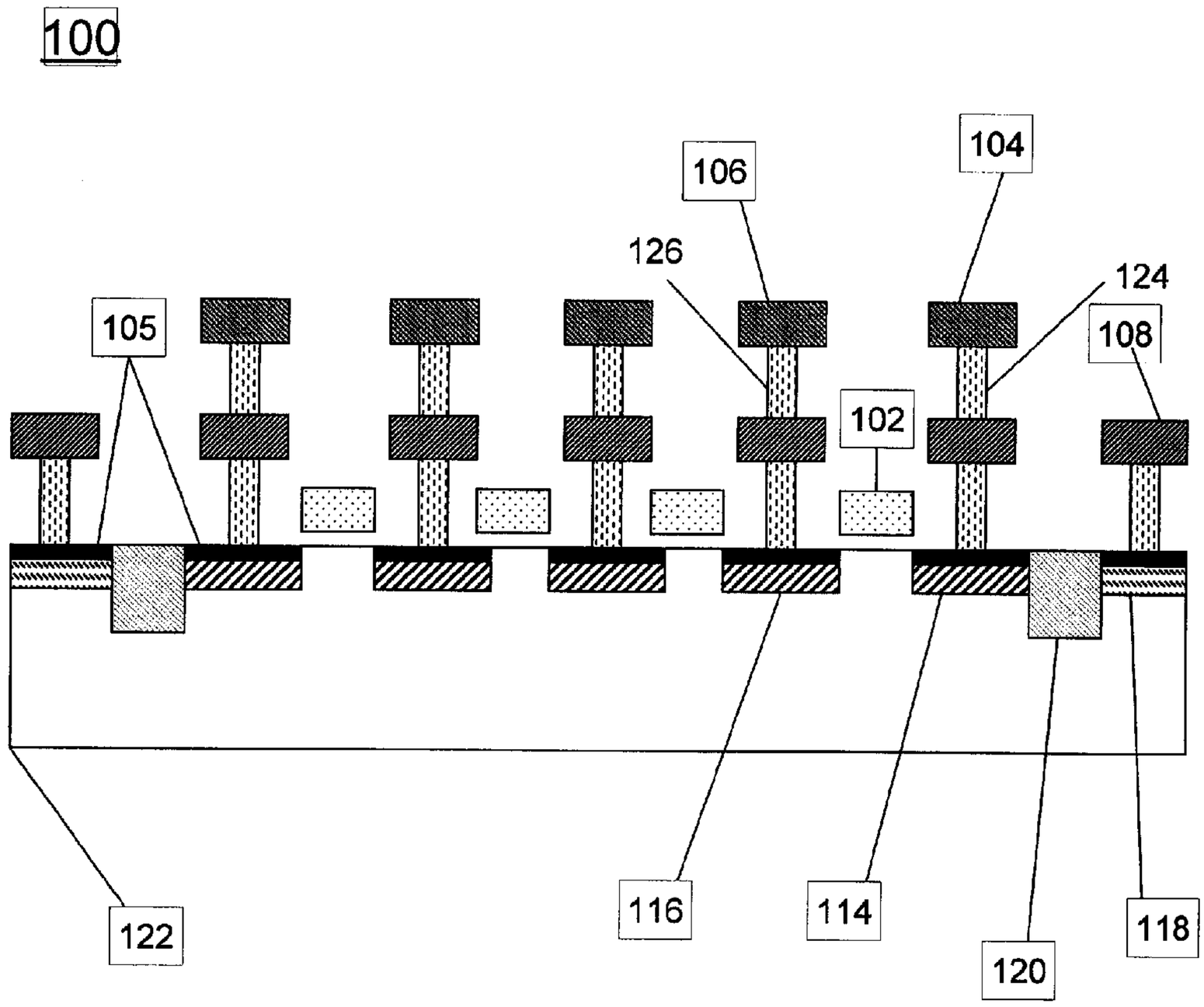


Fig. 3

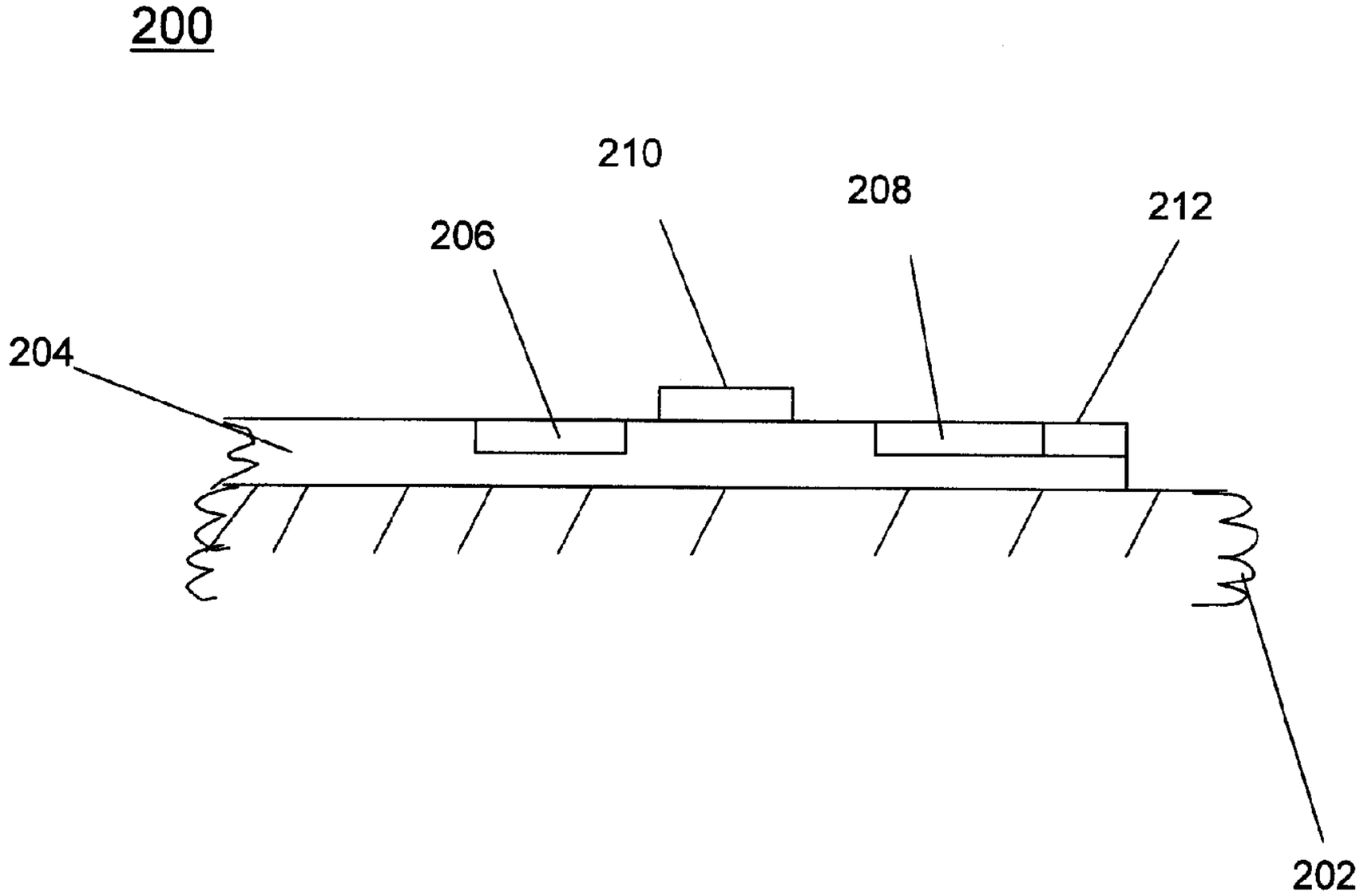


FIG 4

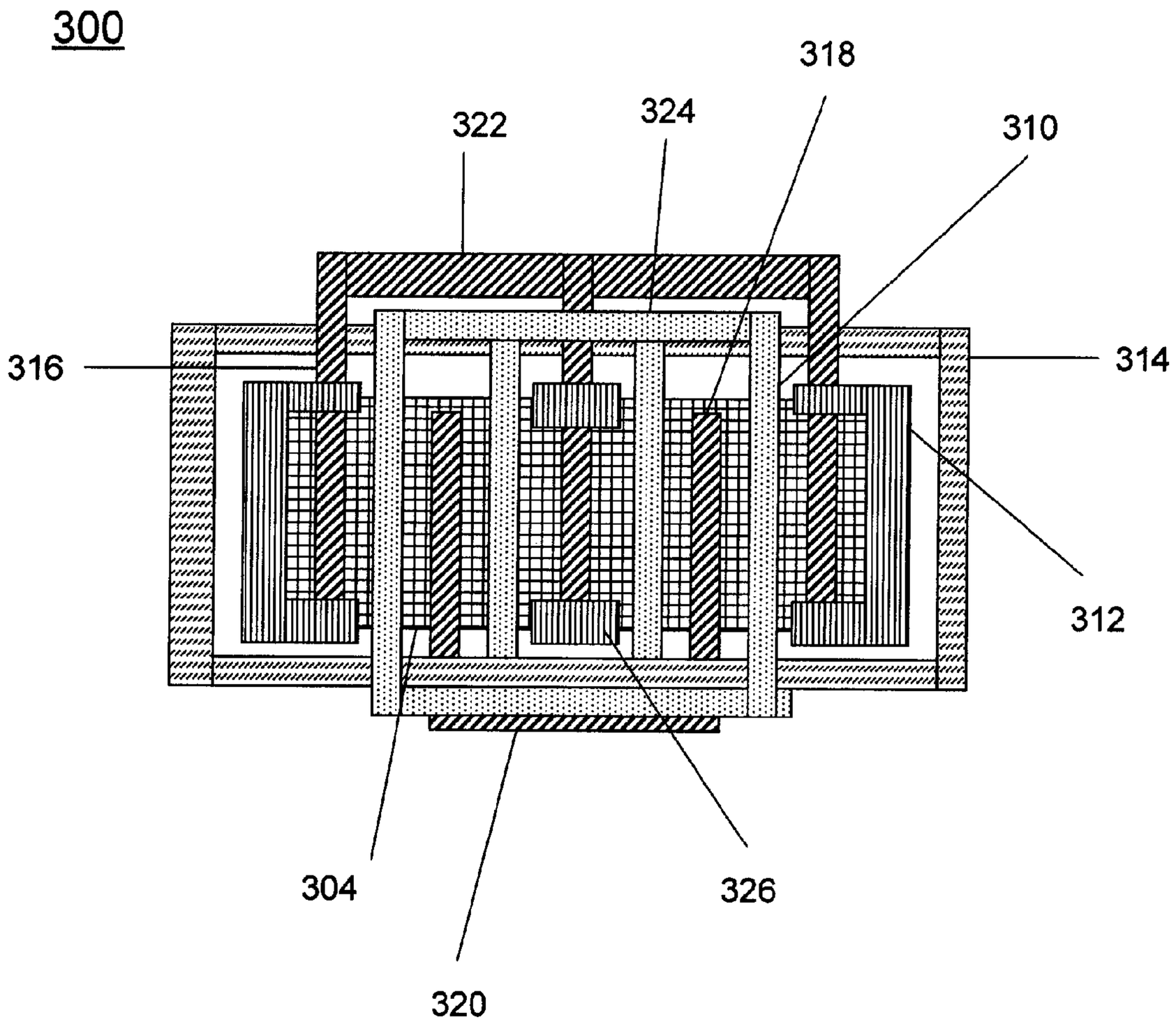


FIG 5

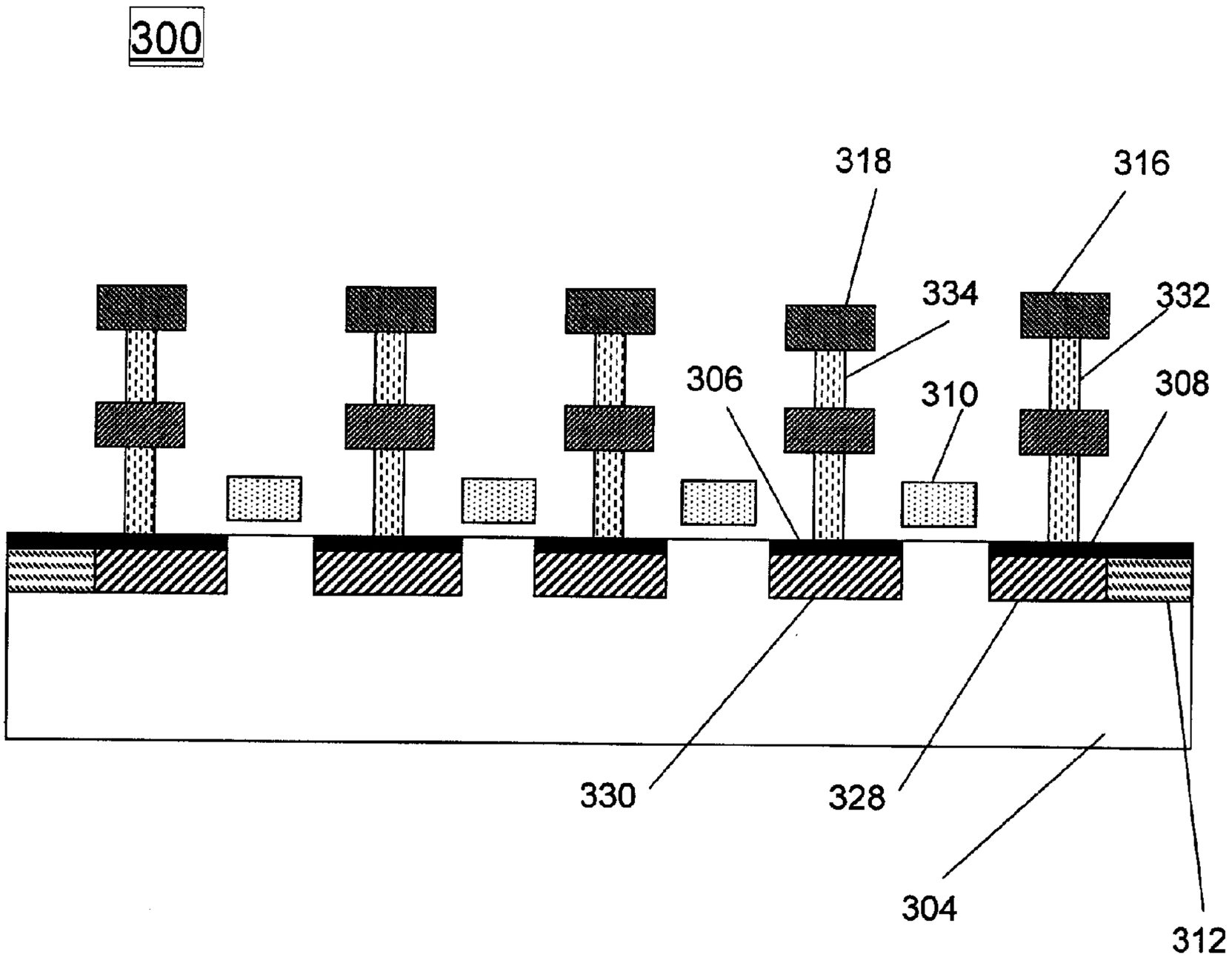


FIG 6

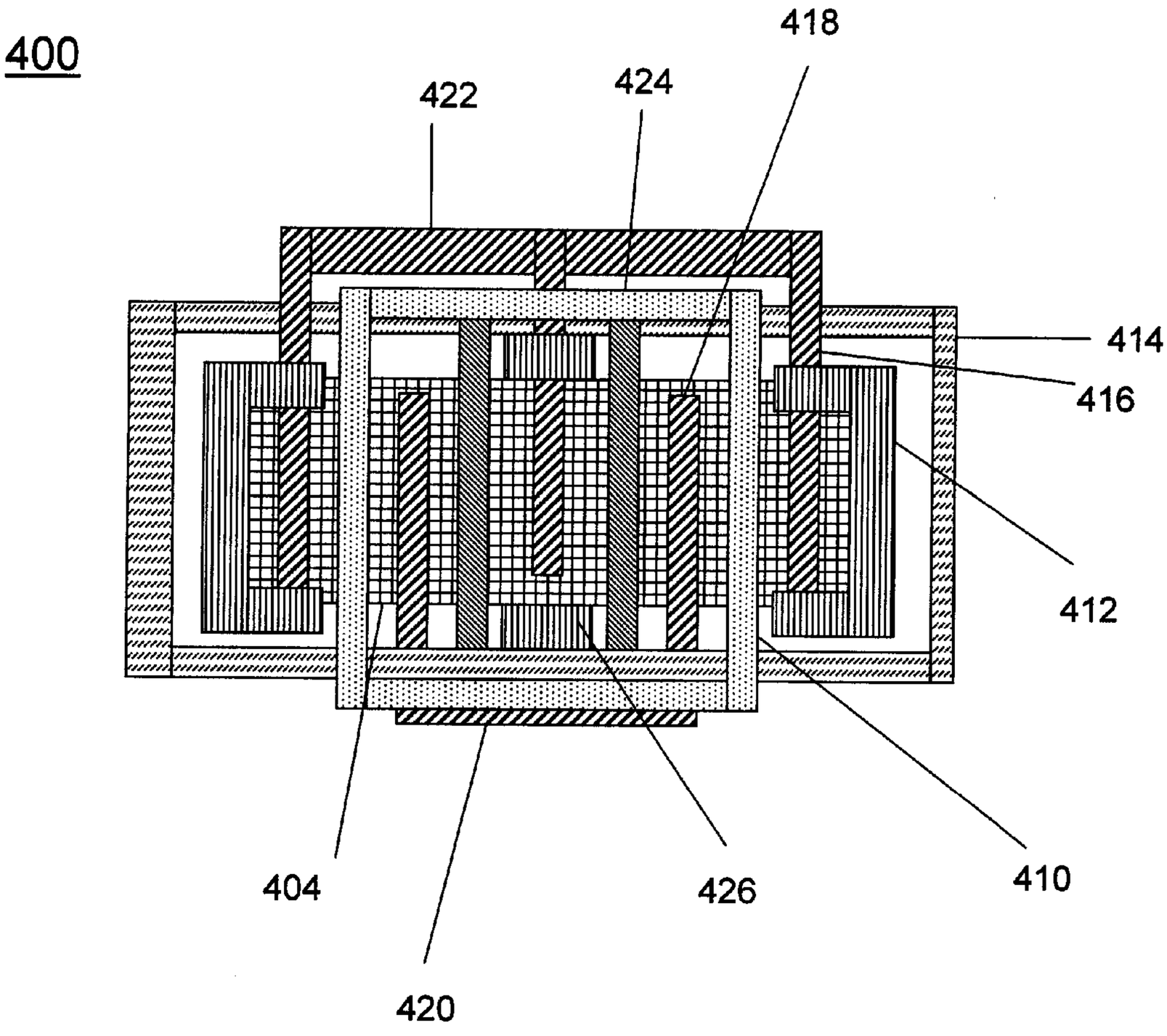
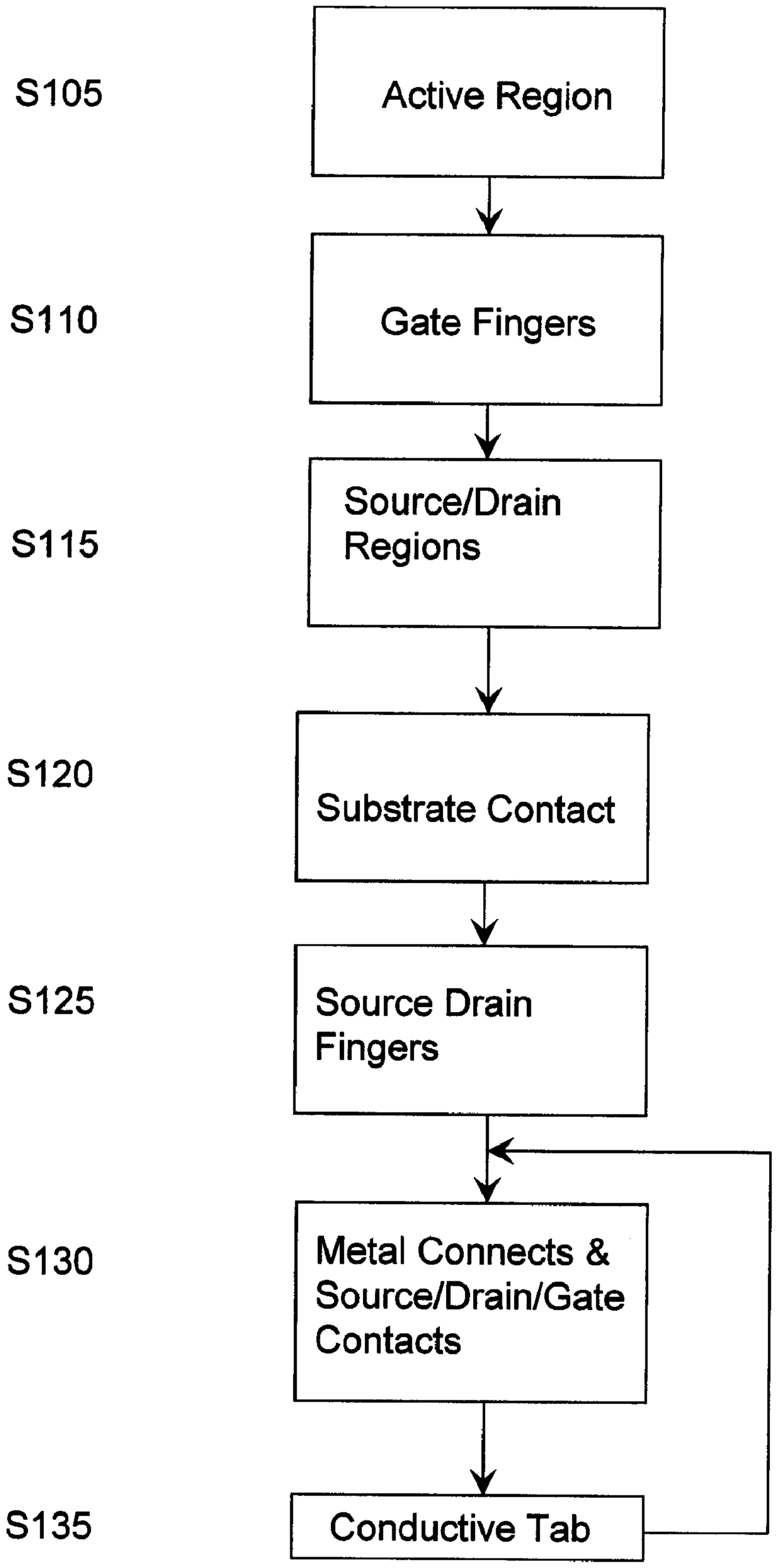


FIG 7


S105
Active Region
S110
Gate Fingers
S115
Source/Drain Regions
S120
Substrate Contact
S125
Source Drain Fingers
S130
Metal Connects & Source/Drain/Gate Contacts
S135
Conductive Tab

STRUCTURE AND LAYOUT OF A FET PRIME CELL

FIELD OF THE INVENTION

[0001] The invention relates to semiconductor circuits, and more particularly to FET (field effect transistor) circuits for microwave and RF (radio frequency) applications.

BACKGROUND OF THE INVENTION

[0002] In general, a FET is a three-terminal device which may find use in both microwave amplification and switching. The three terminals on the FET include a gate, source and drain. A basic FET includes a gallium arsenide (GaAs) substrate with an active layer arranged thereon. The active layer includes a source and a drain, with a gate arranged therebetween on top of the active layer. The FET may also include a backside metal on the bottom of the substrate. The backside metal may be configured to be in electrical communication with the source by a plated via hole through the substrate.

[0003] In operation, a voltage signal applied to the gate creates a depletion or inversion region in the active region between the source and the drain. This region allows current to flow between the source and the drain, respectively. In typical microwave and RF applications, the drain is the output of the device. FETs can be structured in the form of a FET prime cell which has better frequency and power properties then the basic FET design. The prime cell provides the gate, source, drain, substrate and wiring configuration to make an RF amplifier.

[0004] Although offering improved frequency and power characteristics, typical FET prime cell configurations include a relatively large footprint of the device due to the various features of the FET prime cell spread across the top region of the substrate. Additionally, typical FET designs include the wiring related capacitance between the gate fingers to the substrate. There is also wiring related capacitance between the source fingers and the substrate. Neither of these wiring related capacitances scale with shrinking device geometry, and thus become difficult to improve at ever smaller device sizes. These wiring related capacitances lead to a reduction in the maximum workable frequency of the device and thus imposes frequency limitation on the FET prime cell.

[0005] For example, **FIGS. 1 and 2** show a typical FET prime cell **100**. The FET prime cell **100** includes a substrate **122** with alternating or interleaved source contacts and drain contacts, **104** and **106**, respectively, arranged thereon. Also arranged on the substrate **122** are gate fingers **102** between the source contacts and drain contacts **104** and **106**. The gate fingers **102** are interconnected with one another by a metal ring **108**. The metal ring **108** forms a conductive ring around the region of the substrate **122** on which the gate fingers, source contacts, and drain contacts, **102**, **104** and **106**, are arranged.

[0006] Arranged in the substrate **122** surrounding the active region of the FET **100** is a shallow trench isolation **120** which is surrounded by a ring substrate contact **118** (e.g., the ring substrate contact **118** is arranged adjacent and outboard of the shallow trench isolation **120**). The ring substrate contact **118** provides electrical contact to substrate **122**. The outer-most sources **114** have the shallow trench isolation **120** arranged on either outboard side.

[0007] Accordingly, typical FET designs also include an explicit substrate contact which leads to requiring a unique wiring of the gate. The required wiring is not optimal for device operation and adds an undesirable design constraint for circuit designers. Also, typical related art designs cause wiring parasitics which may prevent the substrate from actually being at the same potential as the source. Additionally, the combination of the shallow trench isolation adjacent the ring substrate contact may make the typical FET more susceptible to stray currents and other electrical noise.

SUMMARY OF THE INVENTION

[0008] In a first aspect of the invention, a method of making a semiconductor device includes forming a source and a drain in a substrate. The method also includes forming a gate on the substrate between the source and drain, and forming a substrate contact in electrical contact with the source. The method additionally includes forming an electrical contact between the source, drain and gate, and the substrate.

[0009] In another aspect of the invention, a semiconductor device includes a substrate and a source and a drain arranged within the substrate. The device also includes a gate formed on the substrate between the source and drain, and a substrate contact formed within the substrate adjacent the source.

[0010] In yet another aspect of the invention, a semiconductor device includes a substrate, and at least two source fingers formed in the substrate substantially parallel to one another. The device also includes at least one drain finger formed in the substrate between the at least two source fingers. The device also includes at least two gate fingers formed on a top of the substrate, wherein each gate finger is arranged between the at least one drain finger and one source finger of the at least two source fingers. The device additionally includes a substrate contact formed within the substrate and adjacent two source fingers of the at lest two source fingers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] **FIG. 1** is an illustration of a top view of a typical FET prime cell for microwave and RF applications;

[0012] **FIG. 2** is an illustration of a cross-sectional view of a typical FET prime cell for microwave and RF applications;

[0013] **FIG. 3** is an illustration of a cross-sectional view of an embodiment of a FET prime cell in accordance with the invention;

[0014] **FIG. 4** is an illustration of a top view of an embodiment of a FET prime cell in accordance with the invention;

[0015] **FIG. 5** is an illustration of a cross-sectional view of an embodiment of a FET prime cell in accordance with the invention;

[0016] **FIG. 6** is an illustration of a top view of an embodiment of a FET prime cell in accordance with the invention; and

[0017] **FIG. 7** is a flow chart of a method of manufacturing a FET prime cell in accordance with the invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0018] In general, embodiments of the invention are directed to reducing the footprint of a FET prime cell as well as improving speed by reducing parasitic capacitance and allowing the circuit designer greater design freedom. An example of the invention includes eliminating a shallow trench isolation area from between the source and a ring substrate contact, and allowing the ring substrate contact to be arranged adjacent to or abutting the source without the need for a shallow trench isolation structure.

[0019] **FIG. 3** shows an embodiment 200 of the invention without a shallow isolation trench in the substrate, and includes a ring structure making contact with the source. The embodiment 200 includes a substrate **202** onto which is arranged an active region **204**. Arranged within the active region **204** are a drain **206** and a source **208**. The source **208** and the substrate **202** may be held at the same voltage potential. Arranged on the active region **204** is a gate **210** between the drain **206** and the source **208**. Also arranged within the active region **204** is a ring substrate contact **212** (e.g., ring structure). The ring substrate contact **212** is arranged within the active region **204** adjacent to the source **208**. Thus, the ring substrate contact **212** abuts or is adjacent to a side of the source **208** and is capable of being in electrical contact therewith without an intervening nonconductive structure such as a shallow trench isolation which would interfere with electrical contact between the ring structure and the source (e.g., separated by a conductive material).

[0020] In one embodiment of the invention, the ring substrate contact **212** is a p+ contact placed next to the source **208** of the FET **200**. Silicide then provides an electrical contact between the source **208** and the body or active region **204** of the FET **200**, such as, for example, forming a layer of silicide over a top surface of the source **208** and the body or active region **204**. It should be noted that by locating the ring substrate contact **212** next to the source **208**, in this fashion, it is not necessary to have a metal contact to the active region **204**.

[0021] Referring to **FIG. 4**, a top view of another embodiment of the invention includes a FET prime cell **300**. The FET prime cell **300** includes a p-well active region **304** with the elongated source contacts **316** and drain contacts **318** arranged across the surface of the active region **304** and alternating with one another. Arranged across the top of the active region **304** and between each source contact and drain contact, **316** and **318**, are gate fingers **310**. Accordingly, the source contacts **316**, drain contacts **318** and gate fingers **310** are interleaved with one another on the surface of the active region **304**. Each end of each gate finger **310** is connected to a gate bus **324**. An end of each source contact **316** is connected to a source bus **322**, and an end of each drain contact **318** is connected to a drain bus **320**. Surrounding the active region **304** of the FET prime cell **300** is a metal ring **314**.

[0022] Referring to **FIG. 5**, a cross-section of the FET prime cell **300** of **FIG. 4** is shown. As seen in the cross-section, the FET prime cell **300** includes a p-well active region **304** into which are arranged alternating elongated drain fingers **306** and source fingers **308**. Underneath each source contact **316** is the source finger **308**, and underneath each drain contact **318** is the drain finger **306**. Additionally, the source finger **308** and the drain finger **306** may each include metal tabs. The source contact **316** is connected to the source finger **308** with a metal connect **332**, and the drain contact **318** is connected to the drain finger **306** with a metal contact **334**. The drain fingers **306** and source fingers **308** include N+ wells, **330** and **328**, respectively.

[0023] On top of the active region **304** and between each drain finger and source finger, **306** and **308**, are the gate fingers **310**. Adjacent to each outer side of each outer-most source finger **308** is a ring substrate contact or substrate contact **312** (e.g., ring structure). The ring substrate contact **312** includes a p+ region formed in the p-well **304**. Also in contact with the source contact **316** in the center of the FET prime cell **300** is tab **326**. Accordingly, the source fingers **308** and the ring substrate contact **312** are in electrical contact with one another and can be held at the same voltage potential.

[0024] As can be seen in **FIG. 5**, the ring substrate contact **312** may be adjacent to or abutting against the outer-most source finger **308** in the body or active region **304** of the FET prime cell **300**. Accordingly, the ring substrate contact **312** may be placed in contact with the outer-most source finger **308**, or at least in close proximity thereto with substantially no intervening non-conductive material which would interfere with electrical contact between the ring structure and the source. As such, the ring substrate contact **312** helps to keep the body or active region **304** of the FET prime cell **300** at a known voltage potential. Additionally, such a configuration of the ring substrate contact **312** relative to the outer-most source finger **308** may also act as a collection source for stray currents. Such stray currents may be produced by electrical noise, which may be induced from a nearby current source, such as, for example, another device or circuit.

[0025] It should be noted that in the examples above, the ring substrate contact may be described as completely or almost completely encircling the body or active region of a FET prime cell. Accordingly, abutting the ring substrate contact against the outer-most source finger or adjacent thereto with substantially no intervening material such as a shallow trench isolation remains beneficial regardless of whether the structure completely or incompletely encircles the active area of the FET prime cell. Thus, the ring substrate contact may extend anywhere from completely around the active region of the FET prime cell to any portion thereof, such as, for example, three-quarters of the way or half-way around the FET prime cell.

[0026] Referring to **FIG. 6**, a top view of an alternate embodiment of the FET prime cell **400** is shown. The FET prime cell **400** includes a body or active region **404** which has drain contacts **418** and source contacts **416** arranged thereon. The drain contacts **418** and the source contacts **416** are elongated and alternate with one another across the surface of the active region **404**. Within the surface of the active region **404** underneath of the source contacts **416** are source fingers (not shown) and arranged under the drain contacts **418** in the surface of the action region **404** are drain fingers (not shown). Also arranged on the surface of the

active region **404** and between the source fingers and drain fingers are gate fingers **410**. The source contacts **416** are connected to one another with a source bus **422**, and the gate fingers **410** are connected to one another with gate busses **424** at either end of the gate fingers **410**. The drain contacts **418** are connected to one another with a drain bus **420**. Arranged within the active region **404** is a ring substrate contact **412**.

[**0027**] The ring substrate contact **412** is arranged in the active region **404** so that it is adjacent to and may abut the outer-most source fingers. Additionally, the ring substrate contact **412** may be arranged in the active region **404** of the FET prime cell **400** so that it is in close proximity to the outer-most source.

[**0028**] The FET prime cell **400** shown in **FIG. 6** also includes a silicon tab **426** which extends from the active region **404**. Accordingly, if proximity of a p+ diffusion area to the gate region and the drain region needs to be optimized, then the FET prime cell **400** incorporates the silicon tab **426** which is doped p-type for the source contact **416**. Note that a similar method may also be adopted for pFETs.

[**0029**] As shown in the embodiments, the ring substrate contact is arranged within the active region of the FET prime cell such that it is either in close proximity to the outer-most source fingers or abuts the source fingers. Additionally, because little or no current flows through the ring substrate contact, it is not necessary to have any metal contact at the ring substrate contact. Silicide provides the electrical contact between the source and the body.

[**0030**] A method of manufacturing a FET prime cell having a reduced footprint and improved speed, for example similar to the FET prime cell of **FIGS. 3-6**, may include the steps shown in **FIG. 7**. For example, referring to **FIG. 7** in conjunction with any of the embodiments of **FIGS. 3-6**, a P-well active region is formed in a substrate (S**105**). The P-well active regions may be formed by any of the suitable doping methods well known in the art.

[**0031**] Gate fingers are next formed on the substrate (S**110**). The gate fingers may be formed by any of the deposition, imaging and etching methods well known in the art for gate formation. The gates are used as a mask while source/drain regions are formed having N+ wells by any of the doping methods well know in the art for forming source/drain regions (S**115**). A substrate contact is formed around the active region (S**120**). The substrate contact may be formed from a conductor such as a metal and may formed using any of the methods well known in the art for forming such a conductor in the substrate.

[**0032**] Fingers are formed on each of the source/drain regions (S**125**). Metal connects are attached to the source/drain regions and source/drain contacts are formed in contact with the metal connects (S**130**). A conductive tab may be formed in electrical contact with the source contact near the center of the prime FET cell (S**135**) in one embodiment, having metal connects and source/drain contacts formed thereto, as well (repeat S**130**). Accordingly, an FET prime cell having a substrate contact is formed.

[**0033**] While the invention has been described in terms of exemplary embodiments, those skilled in the art will recognize that the invention can be practiced with the modifications and in the spirit and scope of the intended claims.

What is claimed is:

1. A method of making a semiconductor device, comprising the steps of:

forming a source and a drain in a substrate;

forming a gate on the substrate between the source and drain;

forming a substrate contact in electrical contact with the source; and

forming an electrical contact to the source, drain and gate, and the substrate.

2. The method of claim 1, further comprising arranging the source and the substrate at substantially the same voltage potential.

3. The method of claim 1, further comprising forming the substrate contact in electrical contact with the source.

4. The method of claim 3, further comprising forming the substrate contact in direct physical contact with the source.

5. The method of claim 1, wherein the substrate contact comprises a p+ region.

6. The method of claim 1, wherein the semiconductor device further comprises at least any of an additional source, drain, and gate.

7. The method of claim 1, further comprising forming a silicon tab in contact with the substrate contact and forming a silicide layer on a top of the substrate contact.

8. The method of claim 1, wherein the substrate contact is formed to partially surround the active region.

9. The method of claim 8, wherein the substrate contact is formed to completely surround an active region defined by the drain, source, and gate.

10. The method of claim 1, wherein the substrate contact is formed in electrical contact with the source without substantially any non-conductive material therebetween.

11. A method of fabricating a device, comprising the steps of:

forming an active region including a source, drain and gate region; and

forming a collection source configured for shielding electrical noise external to the active region.

12. The method of claim 11, further comprising forming the collection source in electrical contact with the source region.

13. The method of claim 11, further comprising forming the collection source in direct physical contact with the source region and either substantially or completely surrounding the active region.

14. A semiconductor device, comprising;

a substrate;

a source and a drain arranged within the substrate;

a gate formed on the substrate between the source and drain; and

a substrate contact formed within the substrate in electrical contact with the source.

15. The semiconductor device of claim 14, further comprising the substrate contact being configured to shield the semiconductor device from electrical noise.

16. The semiconductor device of claim 14, further comprising the substrate contact being in direct physical contact with the source of the semiconductor device.

17. The semiconductor device of claim 14, wherein the substrate contact comprises a p+ region.

18. The semiconductor device of claim 14, wherein the source comprises a source finger and the substrate contact abuts substantially all of one side of the source finger.

19. The semiconductor device of claim 18, comprising at least two source fingers arranged within the substrate, wherein the substrate contact abuts two of the at least two source fingers.

20. The semiconductor device of claim 14, wherein the substrate contact comprises a p-type doped silicon tab contacting the source and a silicide layer arranged on a top of the substrate contact.

21. A semiconductor device, comprising:

a substrate;

at least two source fingers in the substrate substantially parallel to one another;

at least one drain finger in the substrate between the at least two source fingers;

at least two gate fingers on a top of the substrate, wherein each gate finger is arranged between the at least one drain finger and one source finger of the at least two source fingers; and

a substrate contact within the substrate and adjacent two source fingers of the at least two source fingers configured to shield the semiconductor device from electrical noise.

22. The semiconductor device of claim 21, wherein the at least two gate fingers are connected to one another at at least one end with a gate finger bus.

23. The semiconductor device of claim 21, wherein the at least two source fingers are connected to one another at at least one end with a source finger bus.

24. The semiconductor device of claim 21, further comprising at least two drain fingers, wherein the at least two drain fingers are connected to one another at least at one end with a drain finger bus.

25. The semiconductor device of claim 21, wherein the substrate contact electrically contacts two source fingers of the at least two source fingers.

26. The semiconductor device of claim 21, further comprising a gate finger bus electrically connecting the at least two gate fingers, wherein:

the at least two source fingers comprise a source metal tab disposed on a top of the substrate and the at least one drain finger comprises a drain metal tab disposed on a top of the substrate,

the gate finger bus is electrically connected to the metal ring,

the only electrical connection to the substrate is through the source metal tab,

the substrate, the at least two source fingers, the at least one drain finger, and the at least two gate fingers are configured to amplify an RF signal.

27. The semiconductor region of claim 21, wherein the substrate contact is configured to physically contact all of a side of each of the two source fingers of the at least two source fingers.

28. The semiconductor device of claim 21, wherein the substrate contact comprises a p+ region.

29. The semiconductor device of claim 21, wherein the substrate contact comprises a p-type doped silicon tab.

30. The semiconductor device of claim 21, further comprising a silicide layer arranged on top of the substrate contact.

* * * * *