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(54) **SEMICONDUCTOR DEVICES WITH HIGH VOLTAGE TOLERANCE**

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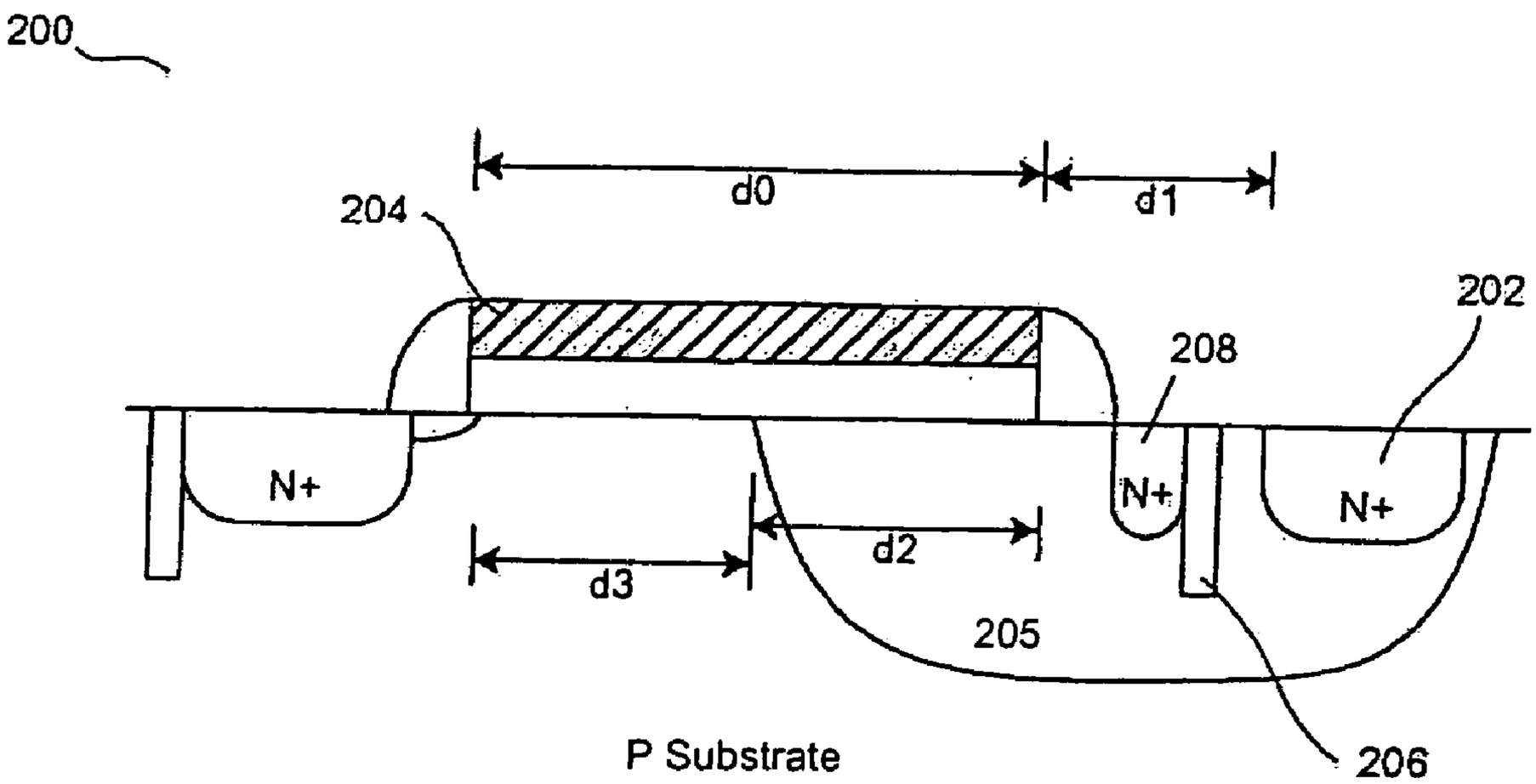
(52) **U.S. Cl.** **257/374**

(57) **ABSTRACT**

The present invention provides improve device designs for high voltage tolerance and methods for making the same. In one embodiment, a low doped drain extension (LDD) region is extended to sustain higher voltages with minimal extra space and processing. In another example, a trench isolation barrier is placed between the gate and an active region in a well. In another example, an additional trench isolation barrier is placed under the middle of the gate. The trench is filled with dielectric such as oxides, with a small upper portion replaced with recrystallized silicon. These disclosed transistor devices can have parameters controlled so that predetermined performances of the transistor devices can be achieved.



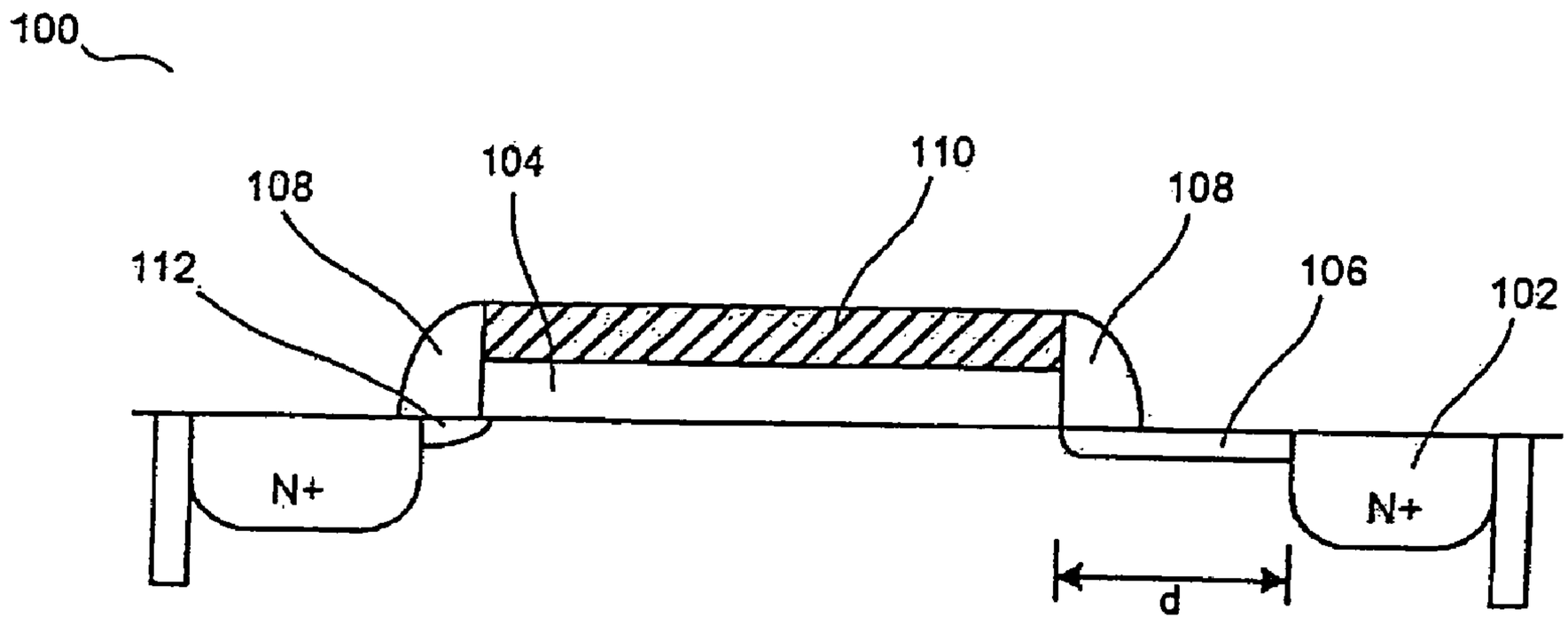

100
108
104
110
108
112
106
102
N+
N+
d

FIG. 1

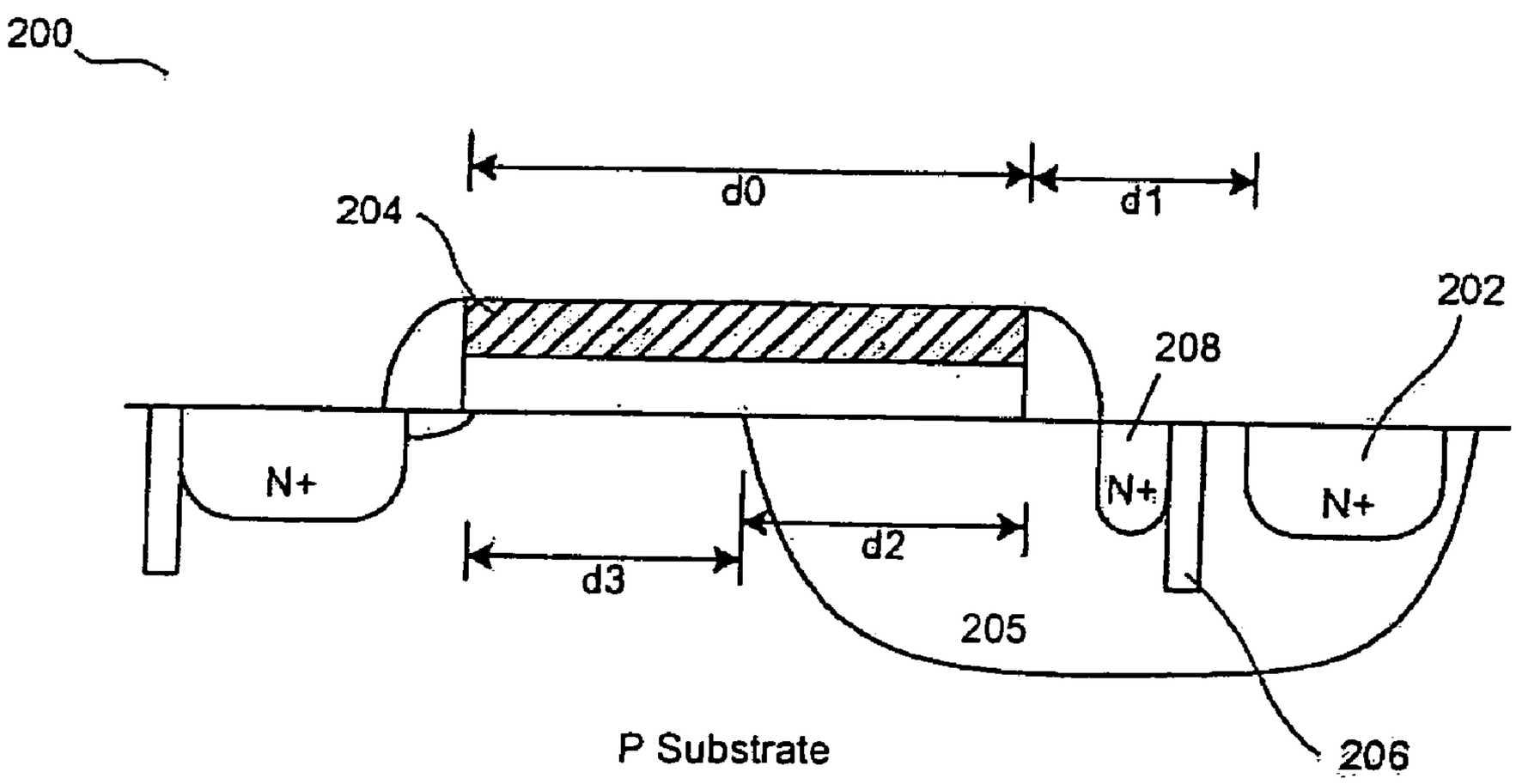

200
d0
d1
204
202
208
N+
N+
N+
d2
d3
205
206
P Substrate

FIG. 2

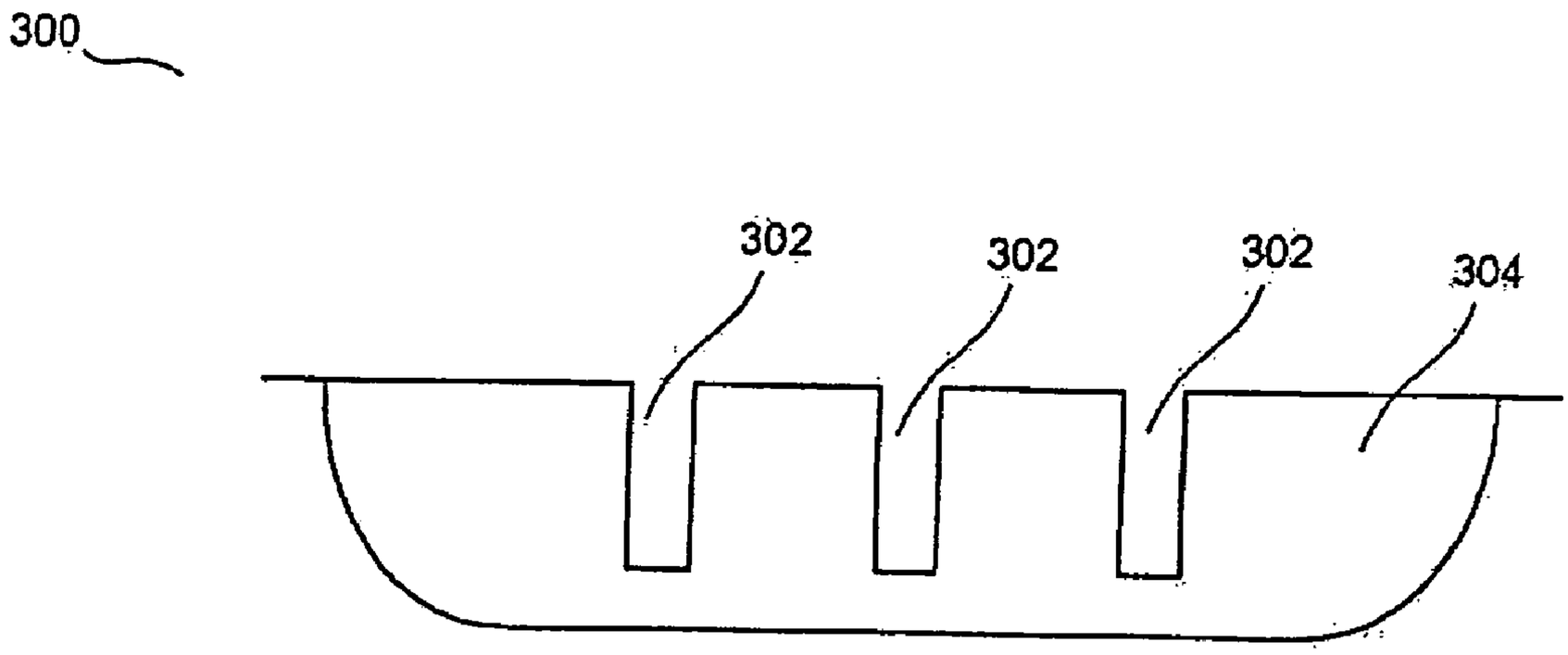


FIG. 3

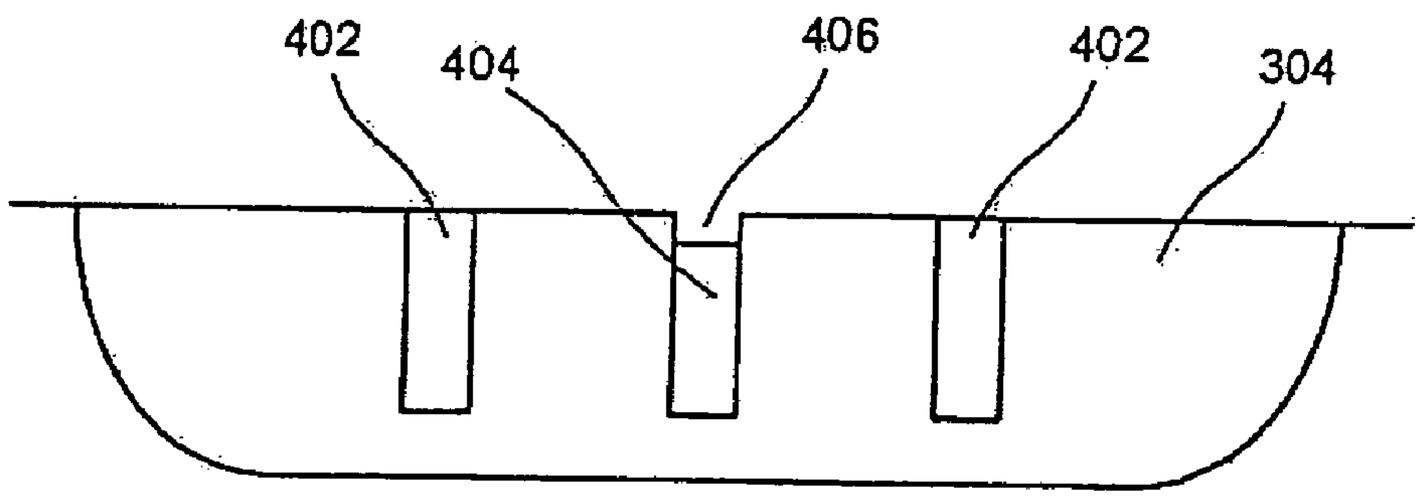


FIG. 4

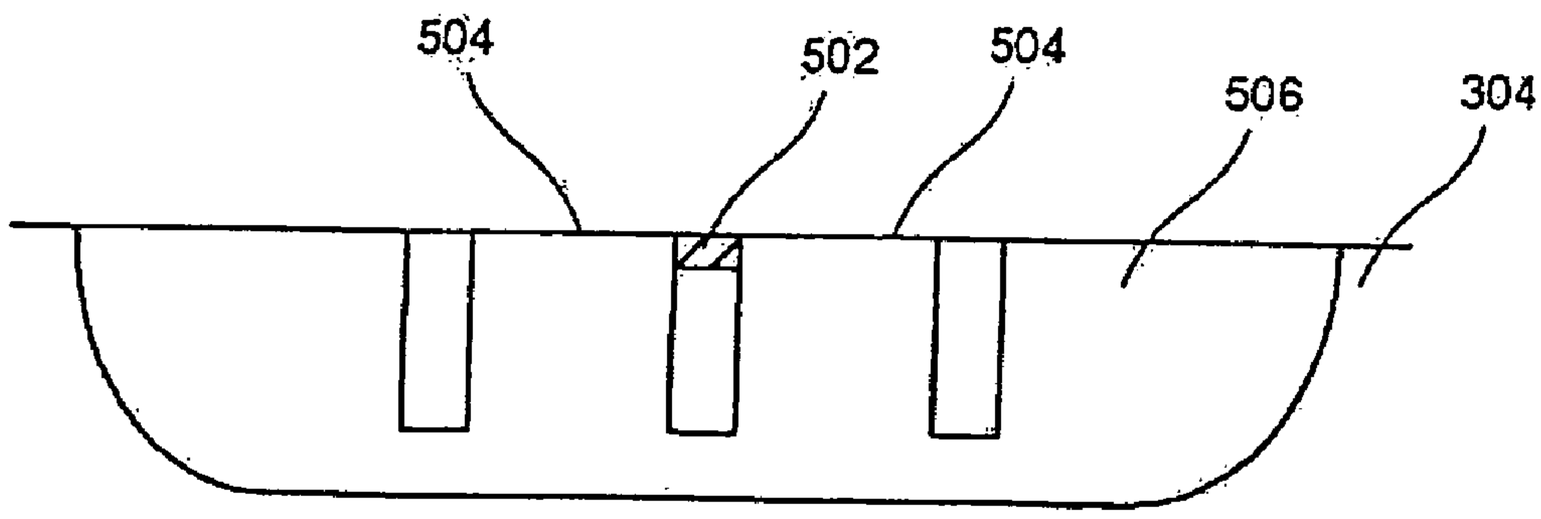


FIG. 5

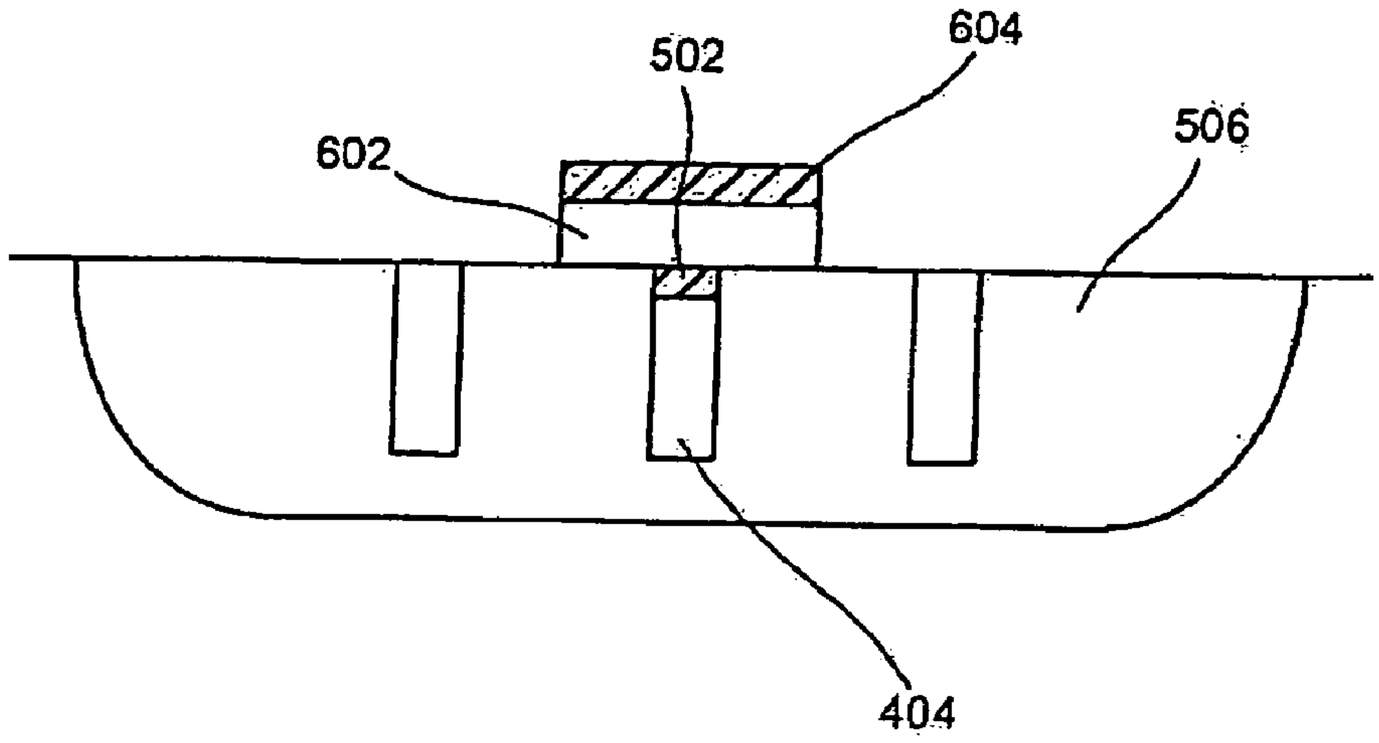


FIG. 6

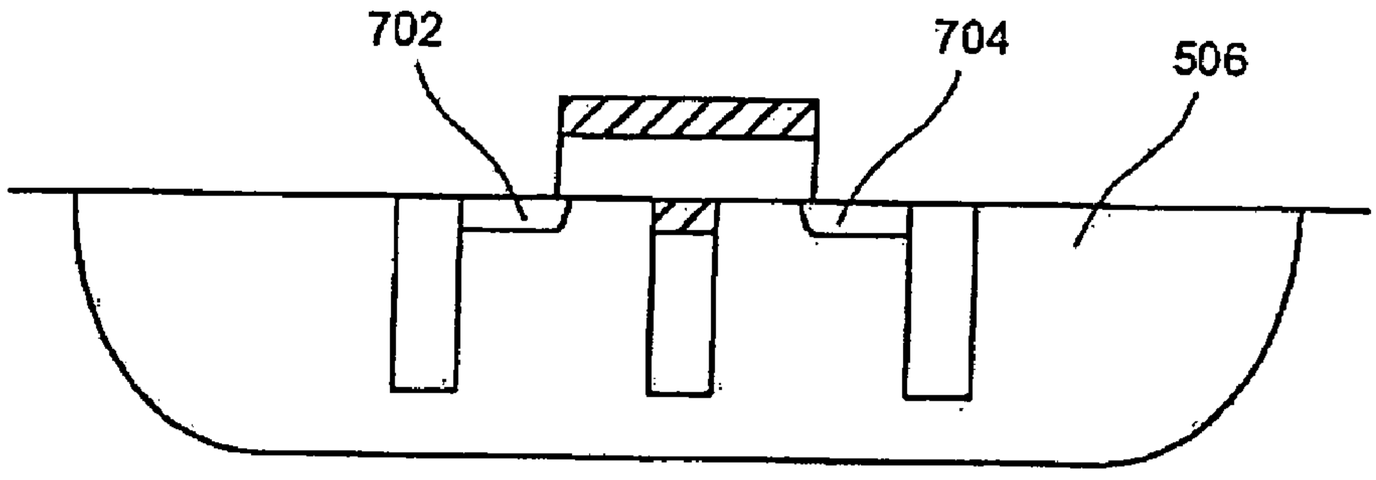


FIG. 7

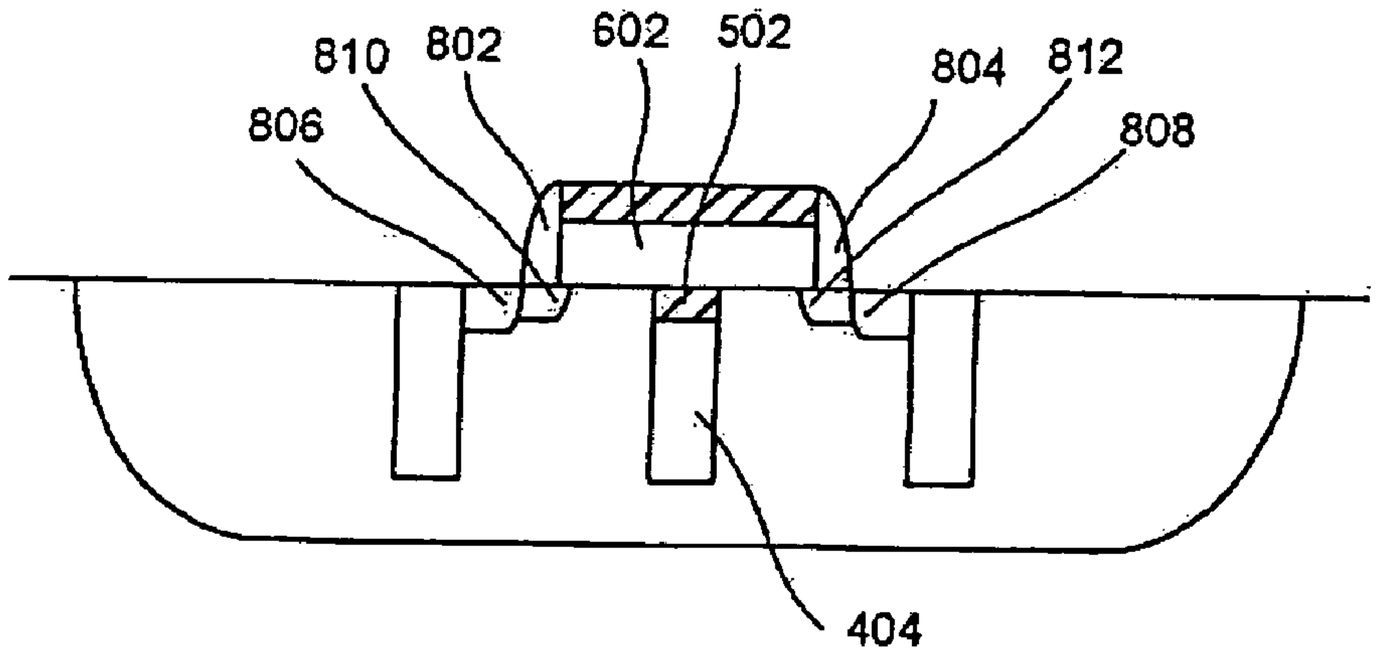


FIG. 8

SEMICONDUCTOR DEVICES WITH HIGH VOLTAGE TOLERANCE

CROSS REFERENCE

[0001] The present application claims the benefits of U.S. Provisional Application No. 60/579,044, which was filed on Jun. 12, 2004, and entitled "Edge-triggered flip-flop design and semiconductor devices with high voltage tolerance", the entirety of which is hereby incorporated by reference herein.

BACKGROUND

[0002] The present disclosure relates generally to semiconductor device designs, and more particularly to semiconductor devices with high voltage tolerance.

[0003] Semiconductor devices such as integrated circuits (IC) operate at a variety of voltages. Since a given IC may be subjected to two or more voltages, the manufacturer is faced with the challenge of economically producing ICs with parts that can withstand different voltages. High voltage typically requires extra space for extra structures and extra process steps. In addition, processing requirements may be incompatible with those of standard voltage devices.

[0004] One issue with respect to high voltage operation is that high voltage may change the performance and operational parameters of metal-oxide-semiconductor field-effect-transistors (MOSFETs) contained in the IC. Specifically, high voltage junctions have steep electric fields which can accelerate electrons to such energy levels that, as hot electrons, they may be injected into the gate oxide where they may cause damage directly, or they may reside and change the effective charge on the gate. The net effect is that the threshold voltage of the MOSFET may be changed, thereby changing the performance and operational parameters of the IC. Another issue in high voltage MOS devices is the drain junction that needs to sustain high voltage applied to the drain without breaking down the drain junction or punching through the channel.

[0005] One partial solution is to use drain extended transistors, which are specifically designed to withstand higher voltages. In such a device, the heavily doped region for drain contact is placed at a distance from the gate and within a well of the same type doping. The well distributes the high voltage over a greater distance. Another partial solution is to use thicker gate oxide, which are specifically designed to withstand higher voltages. However, extra and incompatible processing steps may be required to yield thicker gate oxide, thereby increasing processing complexity and cost. If a long channel is used, space and speed are sacrificed.

[0006] Desirable in the art of semiconductor designs are additional designs that yield a more space-efficient and more process-compatible high voltage tolerant MOS structure.

SUMMARY

[0007] In view of the foregoing, this disclosure provides circuits and methods to improve device designs for high voltage tolerance. In one embodiment, a low doped drain extension (LDD) region is extended to sustain higher voltages with minimal extra space and processing. In another example, the drain of an NMOS is placed inside an N-well and the drain contact is separated from the channel by a trench isolation. In yet another example, an additional trench isolation barrier is placed under the mid of the gate. The trench is filled with dielectric such as oxides, with a small upper portion replaced with recrystallized silicon. These disclosed transistor devices can have parameters controlled so that predetermined performances of the transistor devices can be achieved.

[0008] The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] **FIG. 1** illustrates a semiconductor transistor with a long LDD structure in accordance with an example of the present disclosure.

[0010] **FIG. 2** illustrates a semiconductor transistor with a trench isolation structure placed between a gate and an active region in accordance with another example of the present disclosure.

[0011] **FIGS. 3-8** illustrate a process for forming a semiconductor structure having at least one trench isolation with its top recrystalized between the source and drain regions in accordance with an example of the present disclosure.

DESCRIPTION

[0012] This present disclosure provides a detailed description of more space-efficient and more process-compatible MOS structures that may withstand a high operating voltage without a significant increase in processing or material cost. In one example, a low doped drain (LDD) region is extended to sustain higher voltages with minimal extra space and processing. In another example, the drain of a PMOS is placed inside an N-well and the drain contact is separated from the channel by a trench isolation. Some relationships between device parameters are needed to improve the performance of the device. In yet another example, an additional trench isolation barrier is placed under the middle of the gate. The trench is filled with dielectric such as oxides, with a small upper portion replaced with recrystallized silicon which acts as a pseudo silicon-on-insulator (SOI) structure. These disclosed transistor devices can have parameters controlled so that predetermined performances (such as with certain tolerance of high voltage) of the transistor devices can be achieved.

[0013] **FIG. 1** illustrates a typical N-channel metal-oxide-semiconductor field-effect-transistor (MOSFET) **100**, but with a modified drain structure. Such semiconductor transistors are constructed with a heavily doped N+ drain region **102**, for good electrical contact to the metallization of the integrated circuit wiring. However, if an N+-to-P-well junction is abrupt, it will have a steep electric field. That steep field could accelerate current carrier electrons to high energy so that some of them would be injected into a thin gate oxide **104**. Electron charges trapped in the gate oxide cause damage to it, reducing its reliability. Electron charges trapped in the gate oxide also change the threshold voltage and the conductivity of the channel of the MOS transistor. To reduce such effects, an extended low doped drain (LDD) **106**, in additional to regular LDD **112**, is employed. This extended low doped region is diffused before the formation

of the sidewall spacers **108**, so that it is partially placed under the sidewall spacers, joining the N+ drain region to the channel region directly under a gate electrode **110**. Since The LDD and N+ drain region has some resistance by being distributed over a longer distance, the electric field is less steep. Therefore, electrons are not accelerated to such high energies, and they are less likely to be injected into the thin gate oxide.

[**0014**] As shown in **FIG. 1**, the LDD region **106** is extended to a longer distance d before joining the N+ region **102**. This extended LDD **106** means that a high voltage may be distributed over a distance that is sufficiently long so that the electric field strength is low enough, thereby not accelerating current carrying electrons to damaging energies. Another LDD region **112** on the other side of the gate structure is of a typical length and under the sidewall spacer. The extended LDD **106** thus is substantially longer than the regular LDD region **112**, and is at least partially exposed between the gate (and the gate spacer) and the depletion region **102** while the regular LDD region **112** is substantially covered by the gate and the gate spacer **108**. The length of the LDD region can be controlled to determine the performance thereof such as the sustainable voltage of the transistor. One extra photomask operation may be required since the drain N+**102** is not self aligned, unlike the source side.

[**0015**] It is understood that the same configuration can be applied to a typical P-channel MOSFET with an uneven LLD for the source and drain structures. Similar to what is illustrated in **FIG. 1**, a P+ region (which is the source or drain region) of MOSFET is formed from a gate oxide with an extended LDD situated in between. When the typical sidewall spacers and a poly gate electrode are formed, the extended LDD region on the drain end is placed partially under the sidewall spacer, while the LDD region on the other side of the gate is placed under the corresponding spacer. The lateral length of regular LDD region **112** on source side is about 0.2-0.3 um, while the lateral length d of the extended LDD **106** on drain side may be 0.5-0.7 um, which is at least 0.2 um longer. It is further understood that N type substrates can also be used for making similar transistor devices. For example, a high voltage PMOS device canbe placed on an N-type substrate, and an NMOS device can be placed inside a P-well. Both devices have their LDD regions extended on the drain side.

[**0016**] **FIG. 2** illustrates an NMOS device **200** with one of its active regions, or in this case, its drain **202**, situated inside an N-well **205**, which is further formed in a P type substrate, according to one example of the present disclosure. The concentration of the N-well is sufficiently high and the vertical depth of the N-well is sufficiently large so that it can sustain the high voltage similar to what the LDD region can. The actual N+ drain is separated from the gate **204** by a trench isolation such as a Shallow Trench Isolation (STI) **206**. The low resistivity of the deep N-well allows the drain sustaining higher voltage. The N-well with the STI functions as the drain region for the transistor. It is further noted that there may be a residual N+ region **208** due to the self-aligned process used commercially as the implantation for the drain **202** may also implant the area between the STI and the gate. However, this residual N+ region is not significant and no contact will be made to this area. For the purpose of this application, it can be ignored. In fact, if a special process is designed, this residual N+ region can be eliminated.

[**0017**] Three parameters can be used to adjust voltage sustaining capability and other device performance. In this example, the gate width is referred to as d**0**. The distance between the gate edge to the N+ drain edge, d**1**, determines the extrinsic drain resistance. This resistance further depends on the N-well concentration and also on the STI depth. The length of the side diffusion of the N-well into the channel, d**2** (which is between the edge of the gate within the N-well to the edge of the channel outside of the N-well), affects the intrinsic drain resistance. This resistance also depends on the N-well concentration. The actual channel length, d**3**, determines the active channel region. It is noted that this device behaves like a drain with a junction as deep as the N-well. Therefore, the channel length d**3** may not be shorter than a necessary minimum length to induce punch through. As it is known in the art, such a minimum length can be determined through simulation. These three parameters can appropriately adjust the performance of the formed device. To ensure proper operation, the preferred relationship among three parameters are that d**1** is no shorter than 0, and d**3** is no shorter than d**2**.

[**0018**] Similar to what is illustrated in **FIG. 2**, a high voltage PMOS can be formed with a P-well replacing the N-well of **FIG. 2**. Instead of sitting in a P-type substrate directly, a deep N-well is formed in the P-type substrate to have the transistor built thereon.

[**0019**] A further enhancement of these devices may be realized with the addition of a third STI structure in the middle, in accordance with an example of the present disclosure. This oxide barrier will be constructed across the middle of the channel. The advantages in high voltage applications will become apparent in the following discussion.

[**0020**] **FIGS. 3-8** illustrate a process for forming a semiconductor structure **300** in accordance with an example of the present disclosure. **FIG. 3** illustrates three shallow trenches **302** etched in a P-type silicon substrate **304** in preparation for making a set of shallow-trench-isolation structures (STIs) after N-well formation. The structure **300** will later be processed into a P-channel MOSFET. The two outer or boundary STIs define the general area for forming the transistor while a gate will be formed over the substrate and centered around the center STI.

[**0021**] **FIG. 4** illustrates the semiconductor structure **300**, with oxide **402** filling up the outer two shallow trenches in the P-type silicon substrate **304**. In the center trench, the oxide has been partly etched after it is filled up along with the neighboring trenches to leave a shorter insulating STI **404**, thereby essentially creating a cavity **406**.

[**0022**] **FIG. 5** illustrates that a silicon material **502** is deposited for filling the cavity **406**, in the middle trench. Other areas may also be deposited by the silicon material initially, by the deposited silicon, in undesirable locations may be removed by etching or chemical-mechanical-polishing (CMP). This filled silicon is then recrystallized by high temperature processing to form single crystal silicon material that is coherent in structure with the single crystal P-type substrate **304**. This material may be implanted with appropriate doping for the desired MOS channel region **504** to be formed.

[**0023**] **FIG. 6** illustrates the formation of a gate structure. After a gate oxide **602** and a gate polycrystalline silicon **604**

are deposited and pattern etched sequentially, the silicon material **502** is now recrystallized and positioned beneath the gate oxide **602** and directly above the remaining portion of the insulating STI **404**. The N-well **506** still encloses all these structures.

[**0024**] In **FIG. 7**, a P-type low-doped-drain (LDD) regions **702** and **704** have been formed (e.g., through implant), both of which are within the N-well **506**. In **FIG. 8**, a source sidewall spacer **802** and a drain sidewall spacer **804** have been formed and the LDD regions **702** and **704** under the spacers **802** and **804** remain intact during source/drain implant while the rest portions of the LDD regions receive N+ implant and become the source **806** and drain **808**. The recrystallized silicon material **502** becomes a part of the channel beneath the gate oxide **602** and directly above the remaining portion of the insulating STI **404**.

[**0025**] This short section of the recrystallized silicon material **502** is part of the MOS channel. It functions as a pseudo SOI structure. The depletion region of the drain that is formed by the LDD **812** and the P+ drain **808**, when reverse biased, may be blocked from reaching the source **806** by the STI **404**. Thus, this device can sustain higher voltage. The containment of the depletion region means less junction surface area and therefore less electrical leakage. This structure allows shorter channel lengths to be formed with good control and with less chance of punch through.

[**0026**] The same structure may also be constructed as an N-channel MOSFET with certain changes. One option is to reverse all P-type and N-type labels, including changes from N-type well to P-type well, and from P-type substrate to N-type substrate. A preferred option would retain the P-type substrate. Also, the P-type LDD and P+ source and drain would change to N-type LDD and N+ source and drain. In addition, the N-well may no longer be necessary.

[**0027**] The above disclosure provides many different embodiments or examples for implementing different features of the disclosure. Specific examples of components and processes are described to help clarify the disclosure. These are, of course, merely examples and are not intended to limit the disclosure from that described in the claims.

[**0028**] Although the invention is illustrated and described herein as embodied in one or more specific examples, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the disclosure, as set forth in the following claims.

What is claimed is:

1. A high voltage transistor comprising:

a first active region on a first side of a gate in a substrate;

a second active region on a second side of the gate in the substrate;

a first low doped region formed between the gate and the first active region; and

a second low doped region formed between the gate and the second active region with a length substantially longer than that of the first low doped region.

2. The transistor of claim 1 the second active region is a drain of the transistor.

3. The transistor of claim 1 wherein the first low doped region is substantially under the gate and a spacer on the first side of the gate, while the second low doped region is partially under the gate and a spacer on the second side of the gate.

4. The transistor of claim 1 wherein the second low doped region is at least 0.2 um longer than the first low doped region.

5. The transistor of claim 1 wherein the first low doped region has a lateral length less than about 0.3 um.

6. The transistor of claim 1 wherein the second low doped region has a lateral length less than about 0.7 um.

7. A high voltage transistor comprising:

a first active region formed on a first side of a gate and in a well of a predetermined type within a substrate;

a second active region on a second side of the gate; and

a trench isolation (TI) of a predetermined depth formed within the well between the first active region and the gate,

wherein the well containing the first active region functions as a drain of the transistor.

8. The transistor of claim 7 wherein the well is an N well if the transistor is an NMOS transistor.

9. The transistor of claim 7 wherein the well is a P well if the transistor is a PMOS transistor.

10. The transistor of claim 7 wherein a performance of the transistor is determined by a distance (d**1**) between an edge of the gate to an edge of the first active region, which affects a drain resistance.

11. The transistor of claim 10 wherein the drain resistance is further affected by an electron or hole concentration of the well.

12. The transistor of claim 10 wherein the performance of the transistor is further affected by a distance (d**2**) between an edge of the gate in the well and the edge of the channel outside of the well.

13. The transistor of claim 12 wherein a channel length of the transistor is larger than d**2**.

14. A semiconductor transistor comprising:

a gate;

a source region formed in a substrate on a first side of the gate;

a drain region formed in the substrate on a second side of the gate; and

a trench isolation placed in the substrate between the source and drain regions underneath the gate with a predetermined top portion thereof forming a portion of a channel between the source and drain region.

15. The transistor of claim 14 wherein the top portion of the trench isolation includes a crystallized silicon material.

16. The transistor of claim 14 further comprising a first and second shallow trench isolations (STI) on the first and second sides of the gate respectively for defining a boundary of the transistor.

17. The transistor of claim 14 further comprising a first and second low doped drain extension regions overlapping at least a portion of the drain and source regions respectively.

18. A method for forming a transistor comprising:

forming at least three trenches in a substrate with a center trench surrounded by two boundary trenches;

filling the three trenches with a predetermined dielectric material;

placing a predetermined silicon material in a predetermined top portion of the center trench;

crystallizing the placed silicon material;

forming a gate over the substrate and substantially centered around the center trench; and

forming a source and a drain regions on both sides of the gate and next to the respective boundary trench.

19. The method of claim 18 wherein the placing further includes removing the dielectric material from the predetermined top portion of the center trench.

20. The method of claim 18 further comprising forming a first and second low doped drain extension regions overlapping at least a portion of the drain and source regions respectively.

21. The method of claim 18 further wherein forming the gate comprising forming two spacers on two sides of the gate.

22. The method of claim 18 further comprising forming a well around the three trenches.

* * * * *