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(54) **HIGH-TEMPERATURE SUPERCONDUCTOR DEVICES AND METHODS OF FORMING THE SAME**

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**Publication Classification**

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(57) **ABSTRACT**

An electronic device including a crystalline substrate, an electrode formed on and epitaxial to the substrate, the electrode including a first superconductive oxide, an insulator formed on and epitaxial to the electrode, a barrier that includes an ion-treated surface of the first superconductive oxide, and a counter-electrode formed on and epitaxial to the electrode and the barrier, the counter-electrode including a second superconductive oxide, whereby a Josephson junction is formed between the electrode and the counter-electrode. A superconductor device that includes an oxide superconductor having a surface exposed to ambient environment, and a passivation layer covering at least a portion of the surface of the oxide superconductor that is exposed to the ambient environment. Methods of forming the above devices are also included.

(21) Appl. No.: **10/751,091**

(22) Filed: **Jan. 2, 2004**

**Related U.S. Application Data**

(63) Continuation-in-part of application No. 10/704,215, filed on Nov. 6, 2003, which is a continuation of application No. 09/082,486, filed on May 20, 1998, now abandoned.

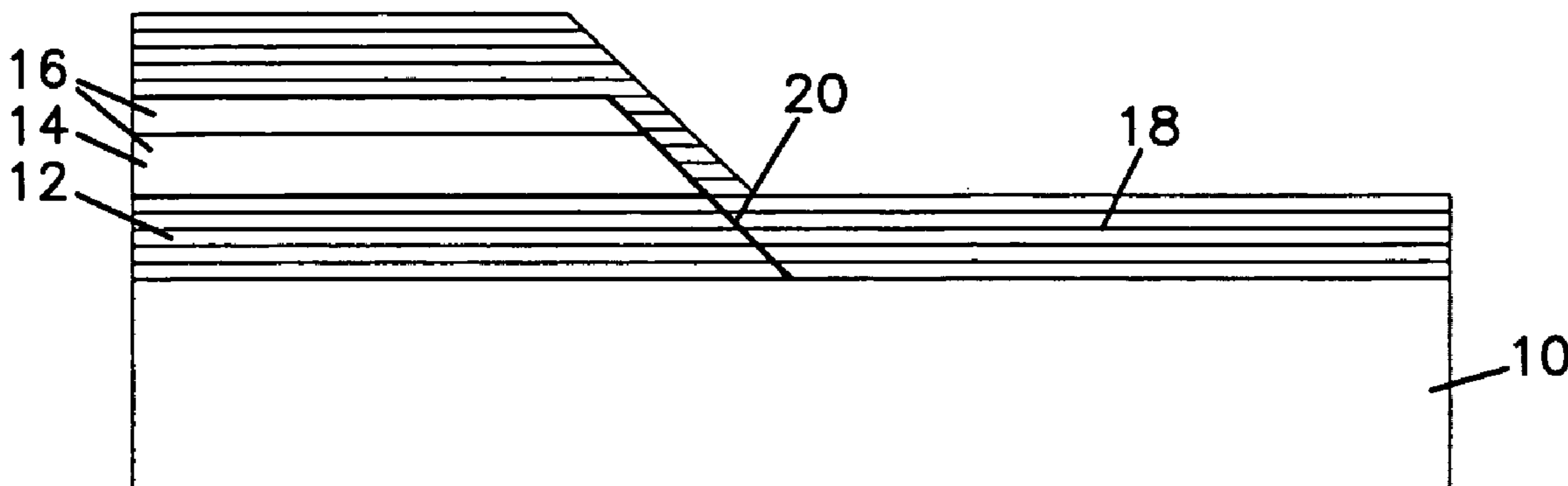


FIG. 1

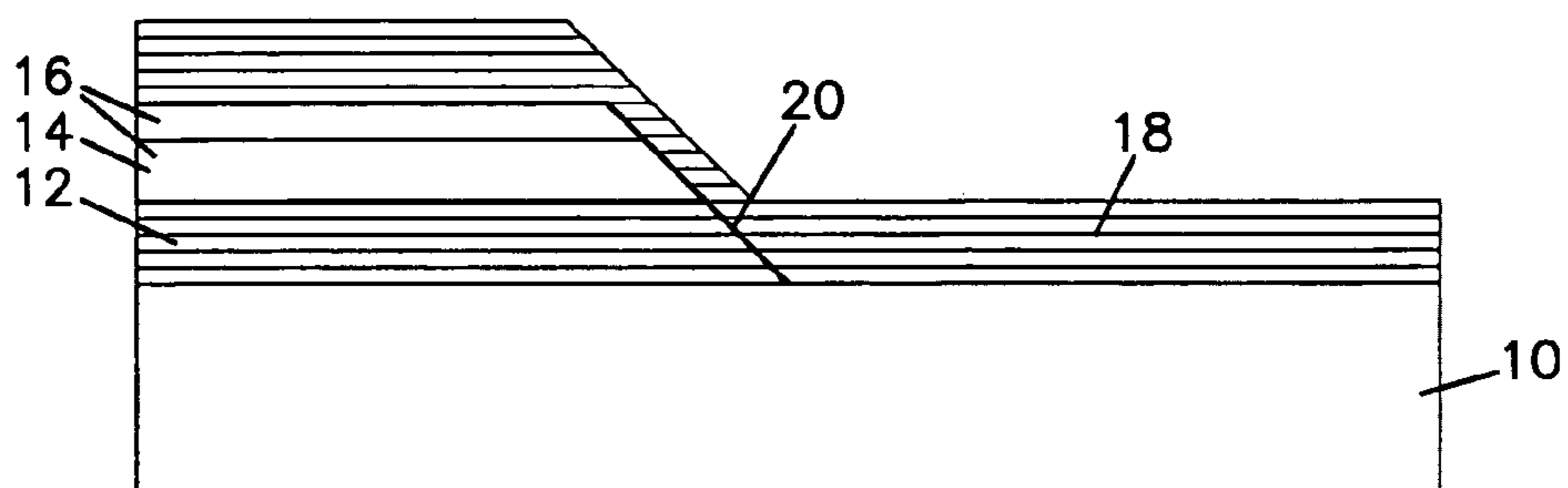


FIG. 2

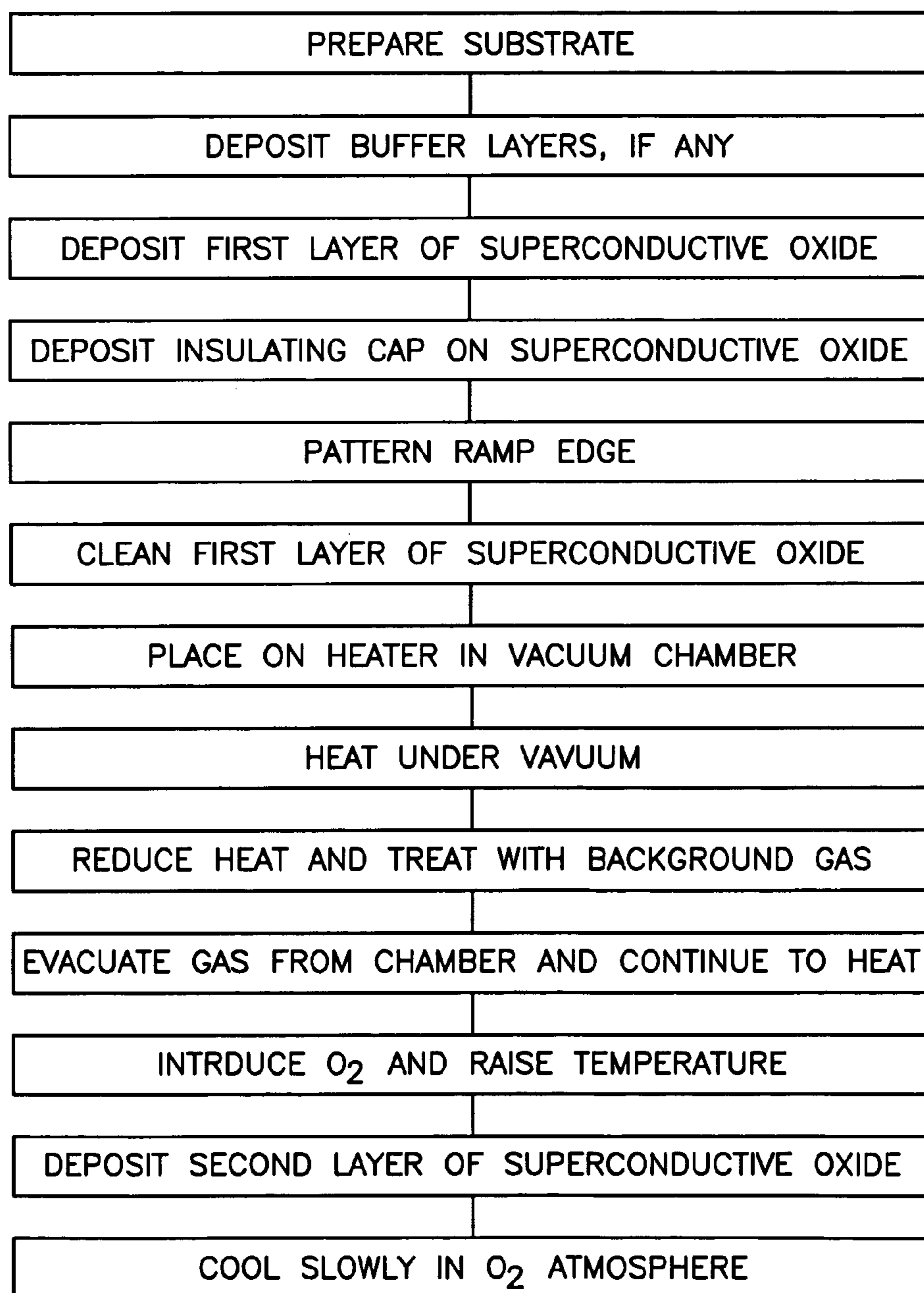


FIG.3

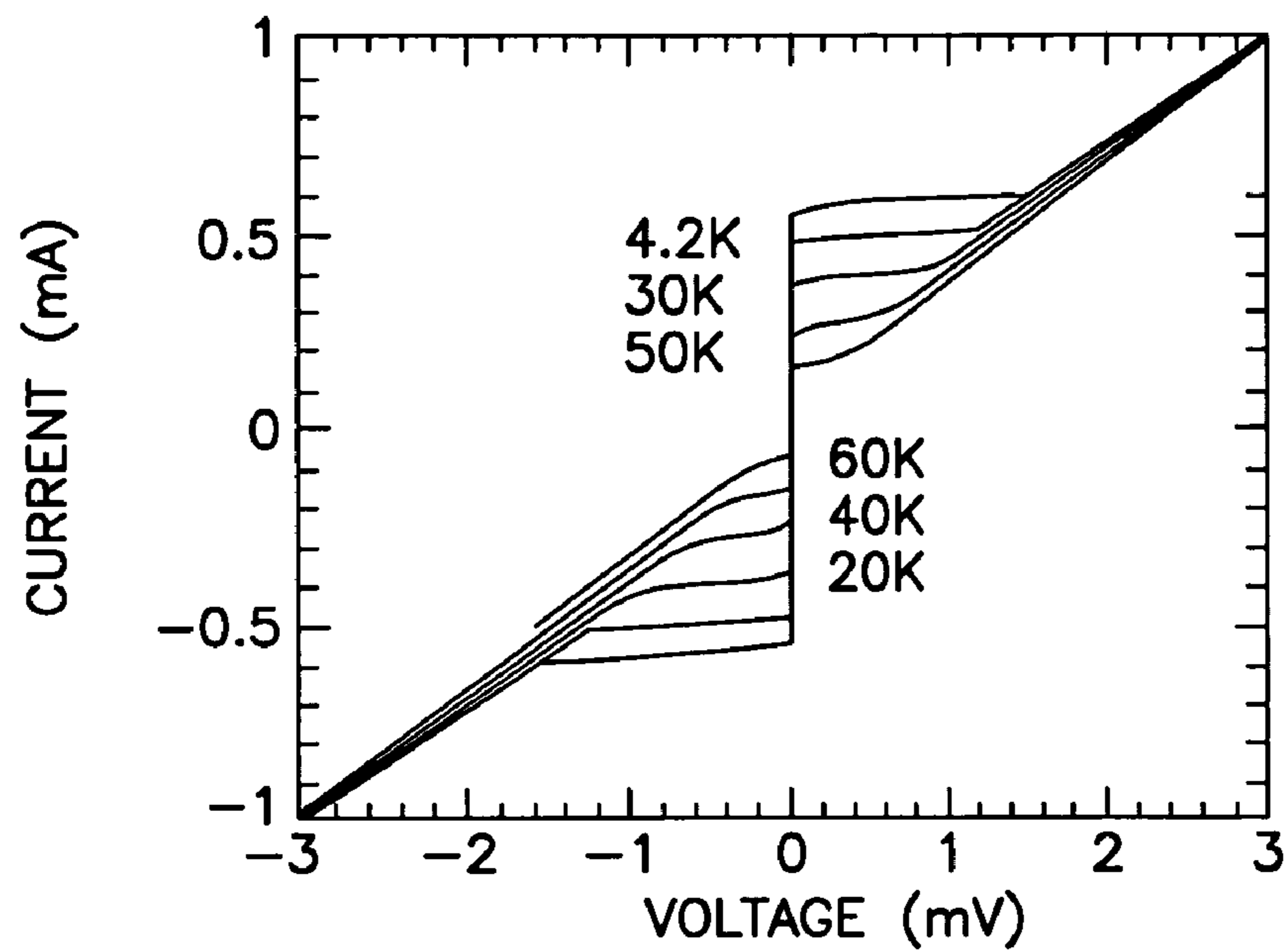


FIG.4

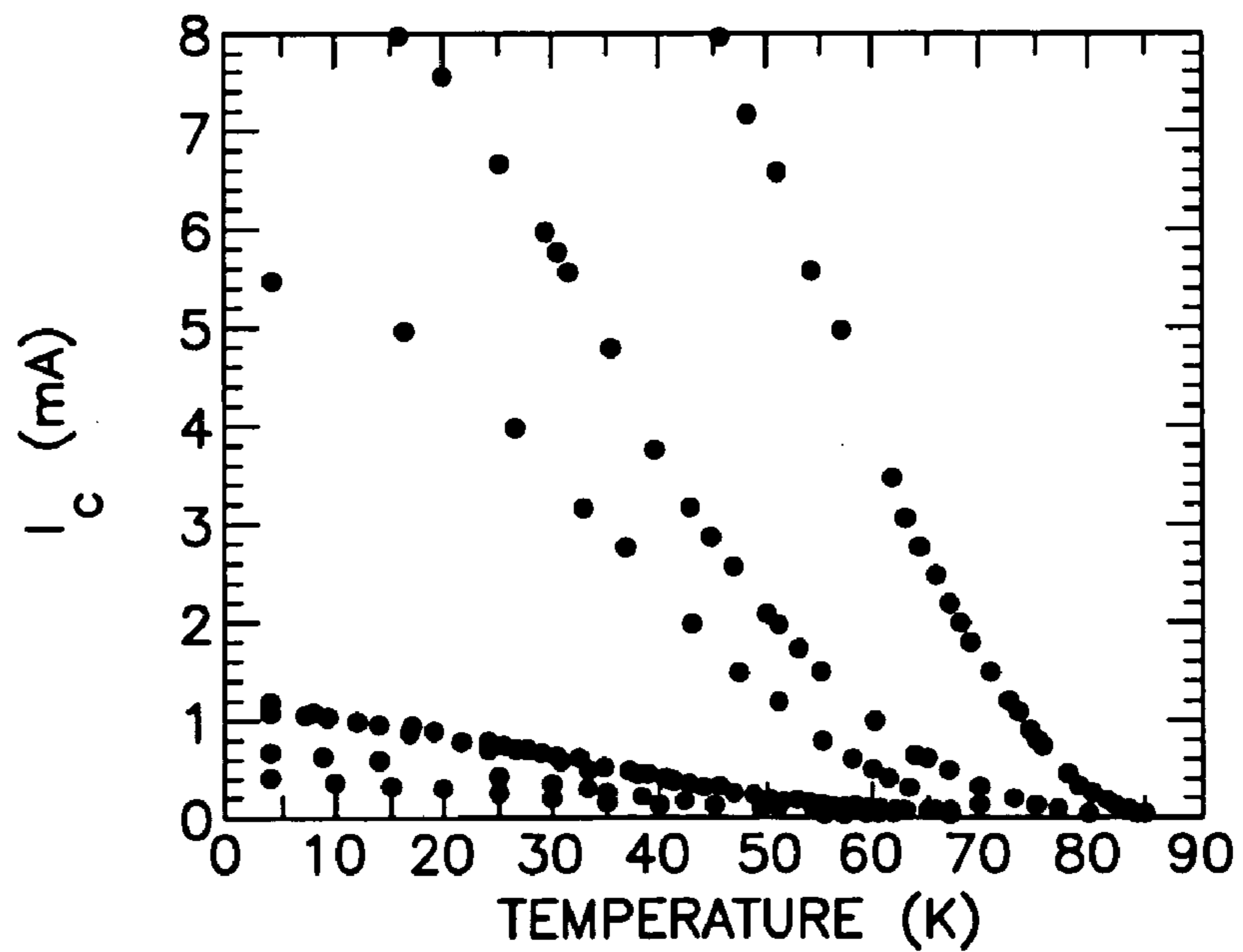


FIG.5

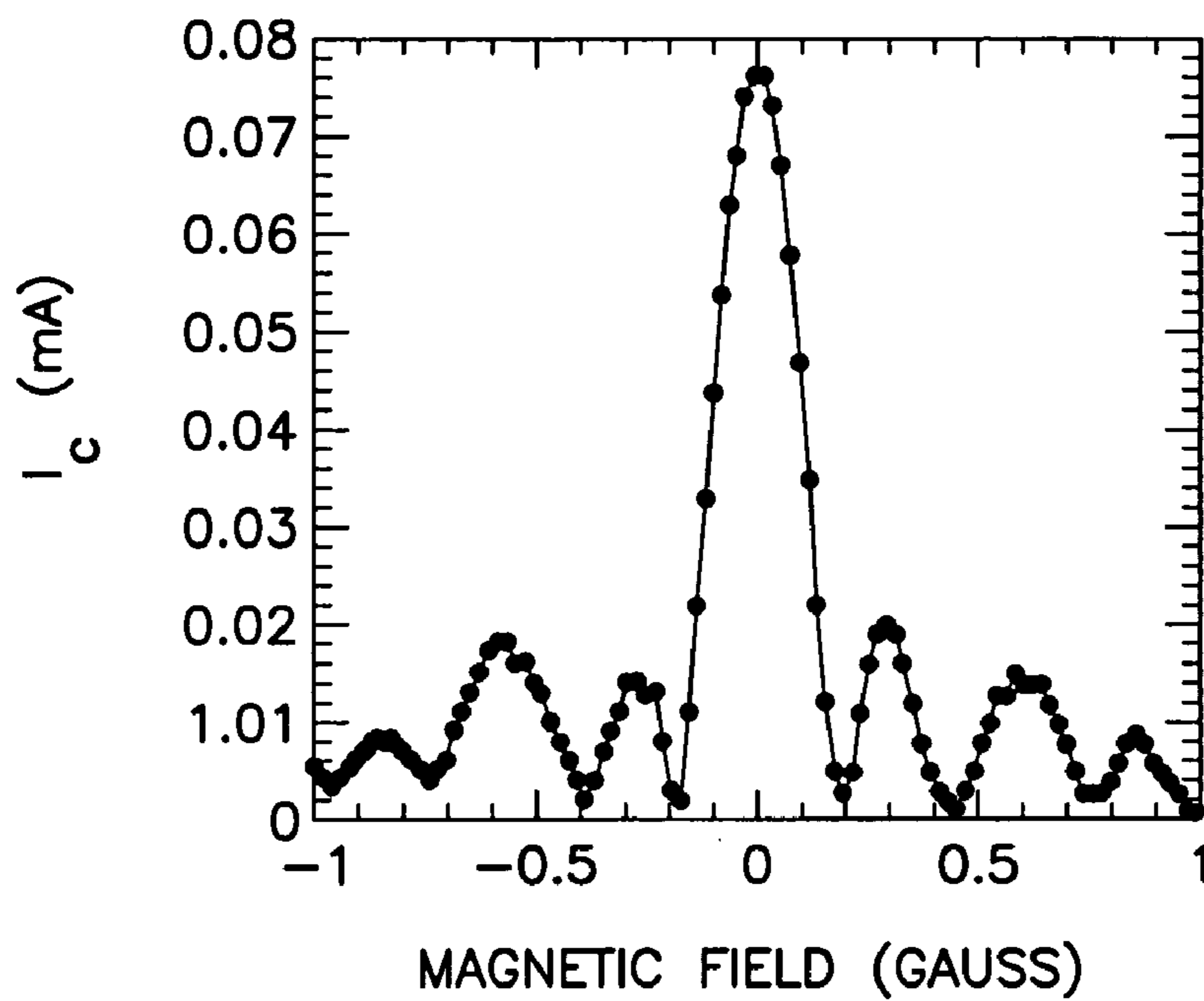


FIG.6

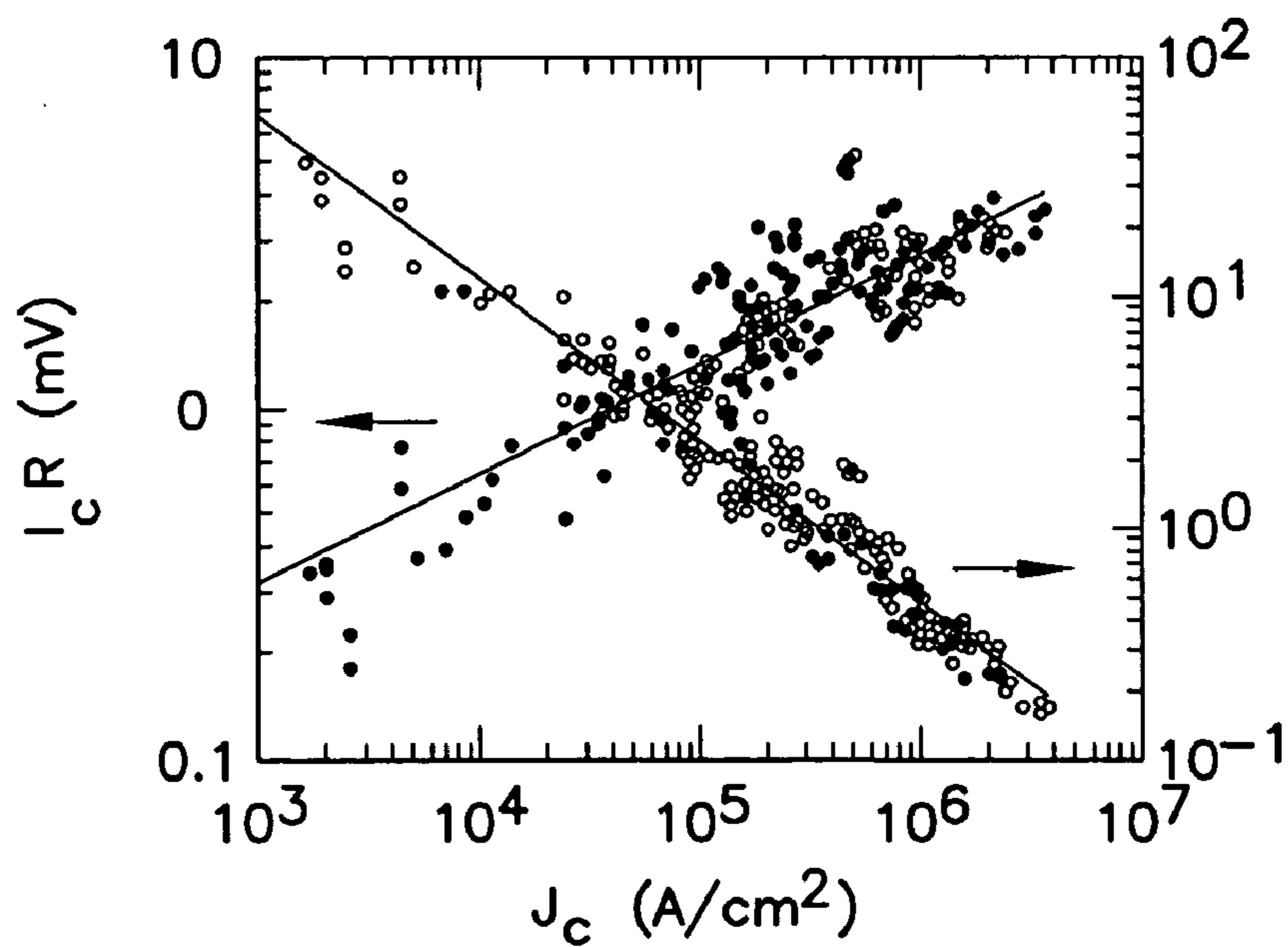


FIG.7

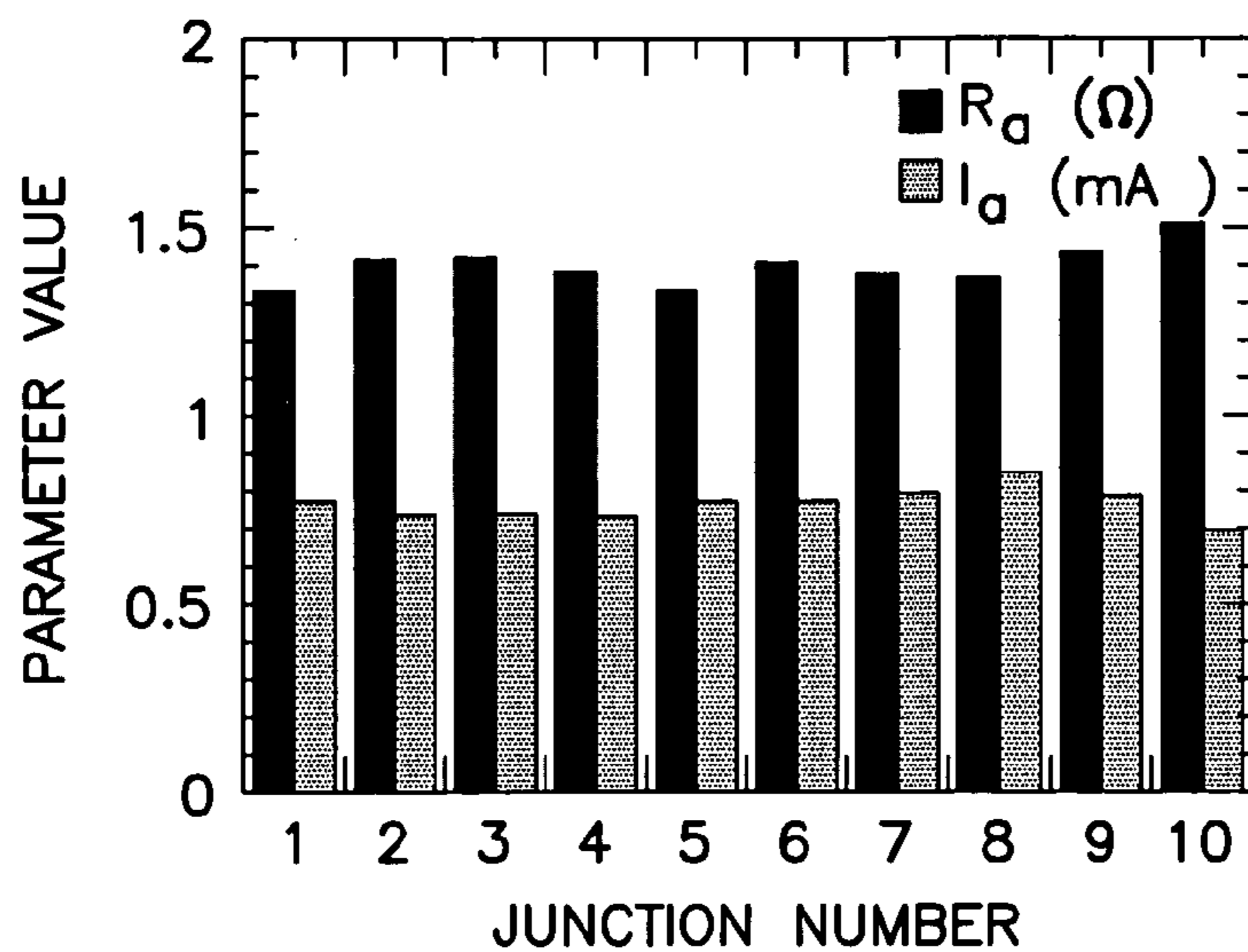


FIG.8

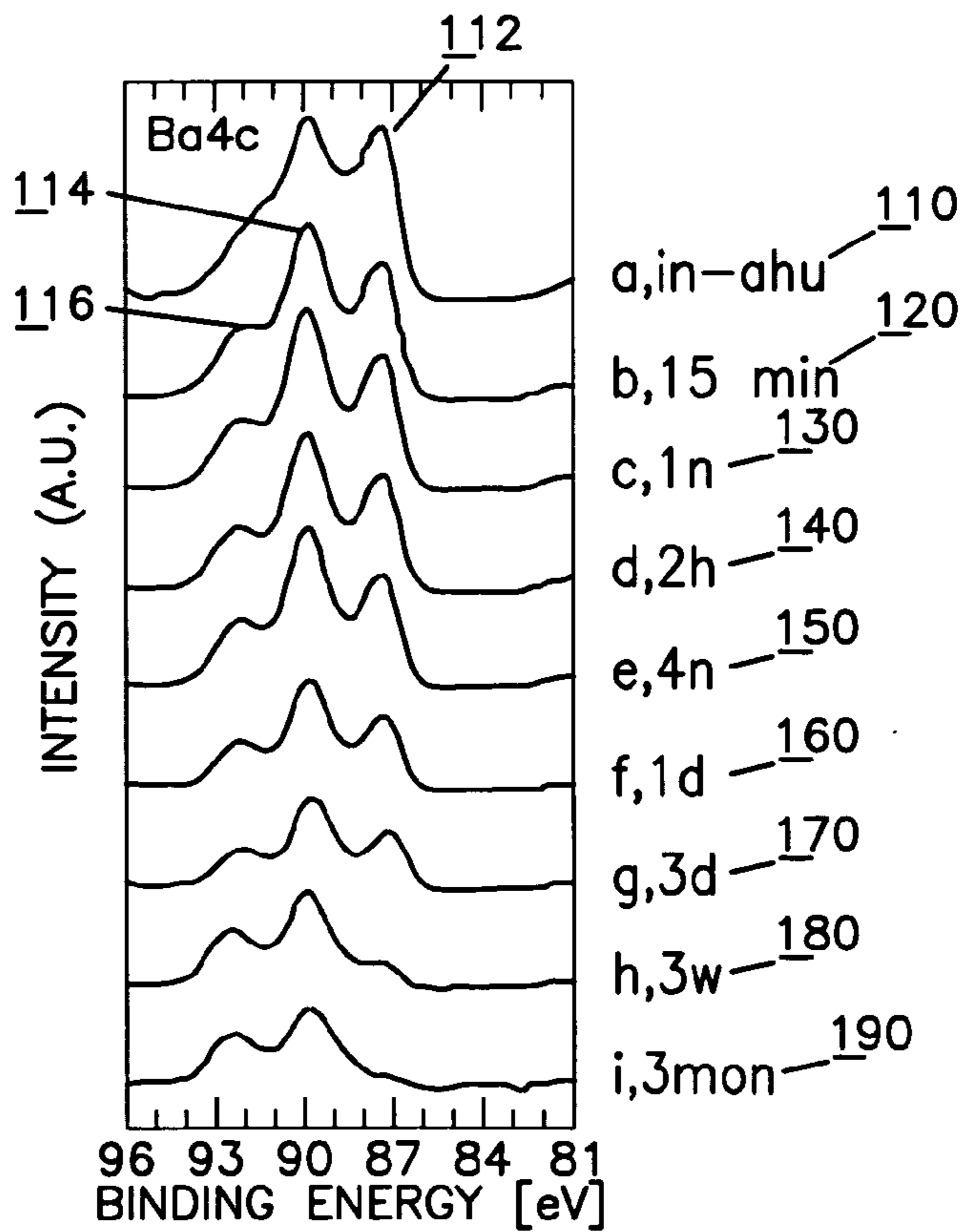


FIG.9

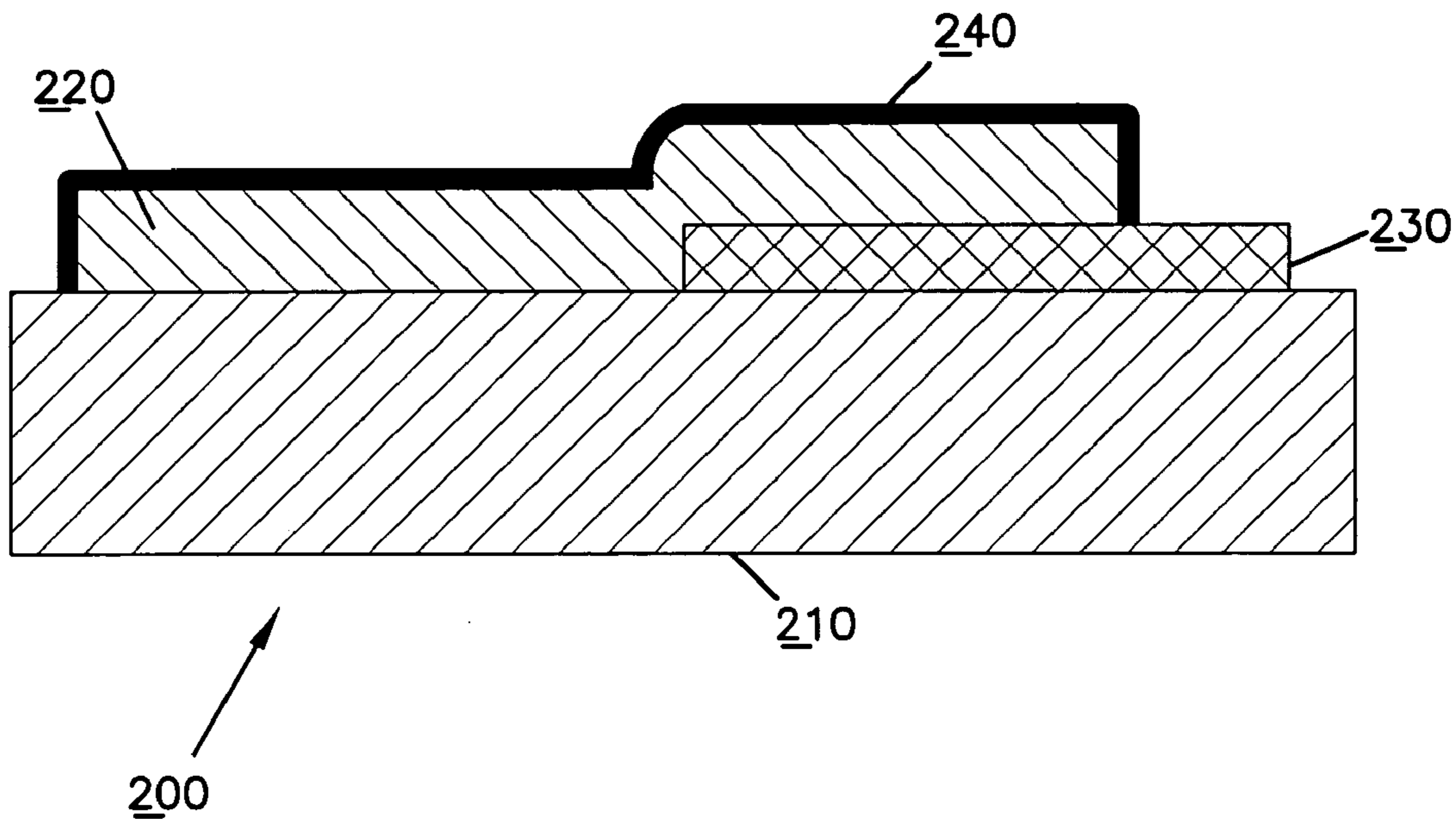


FIG.10

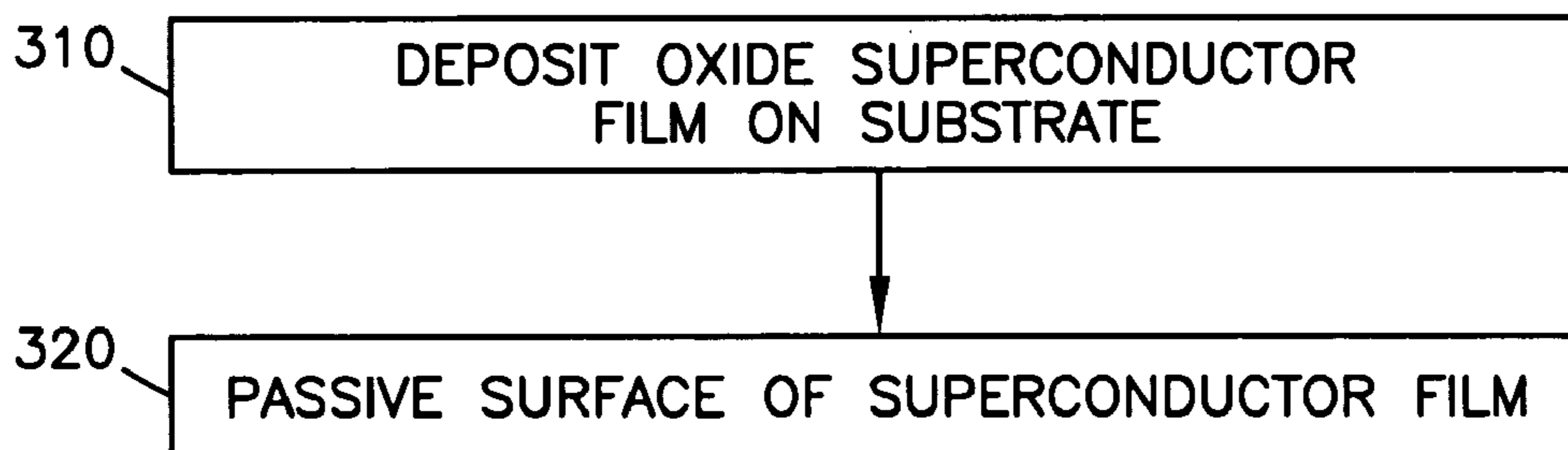


FIG. 11

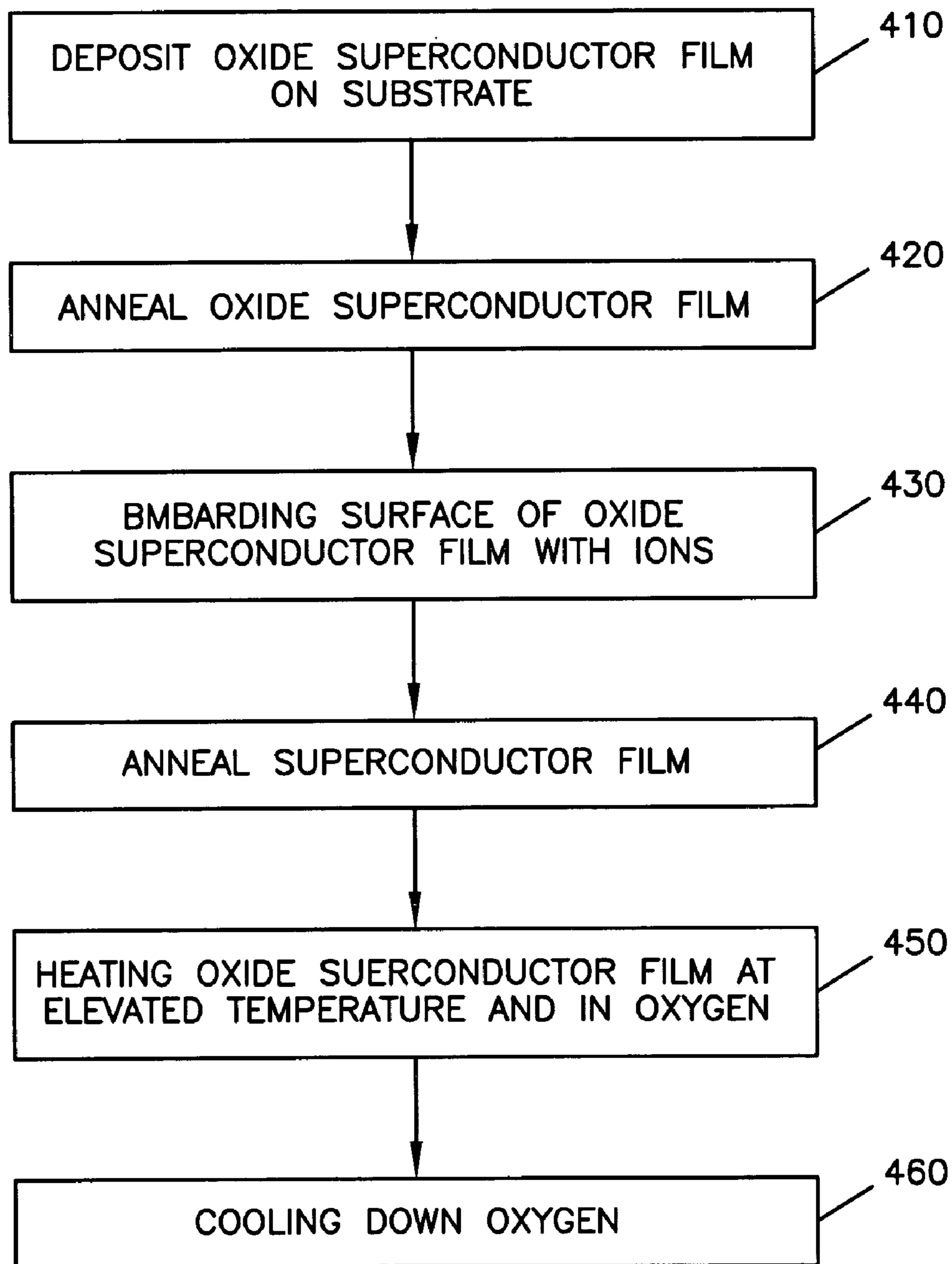


FIG. 12

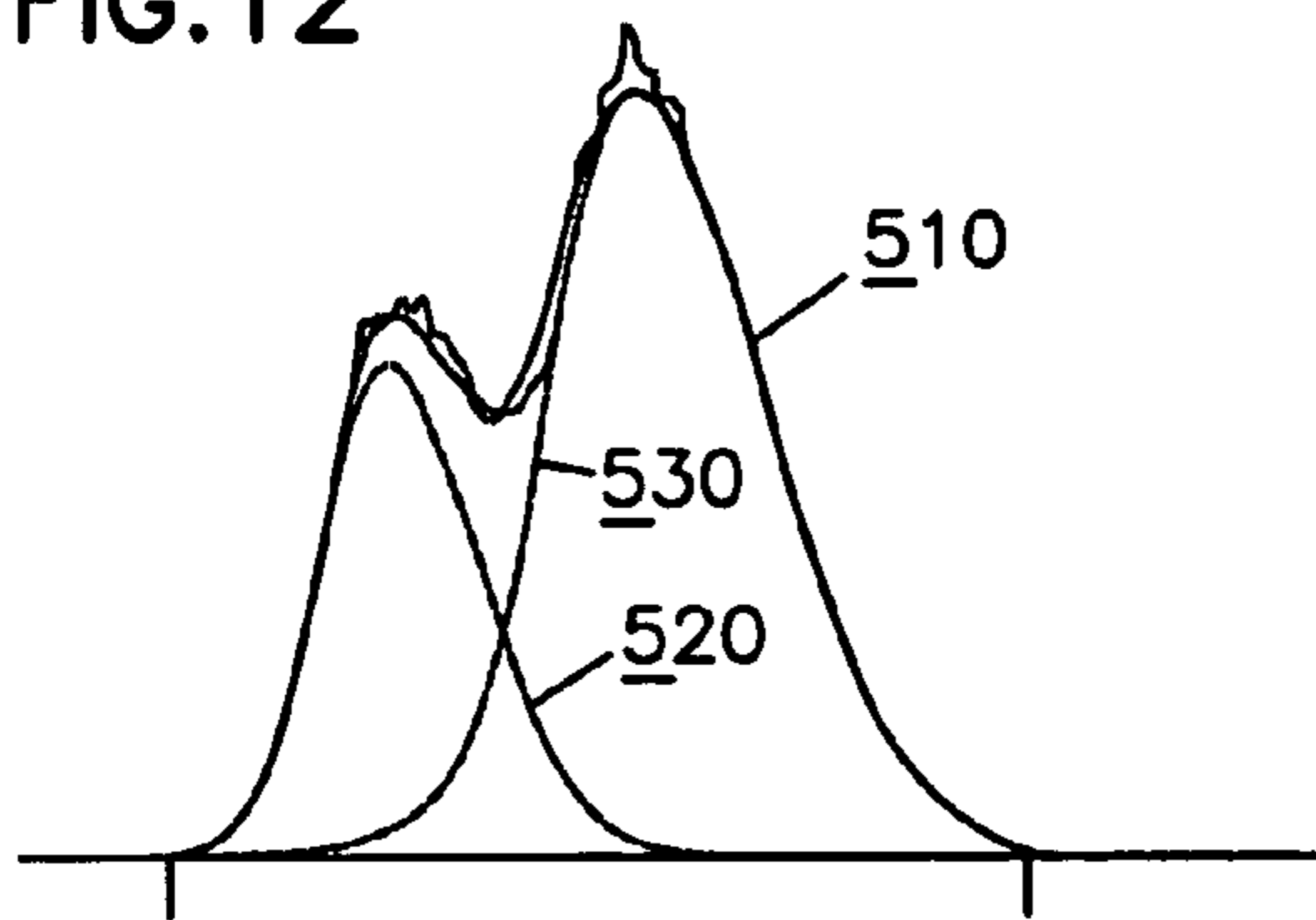


FIG. 13

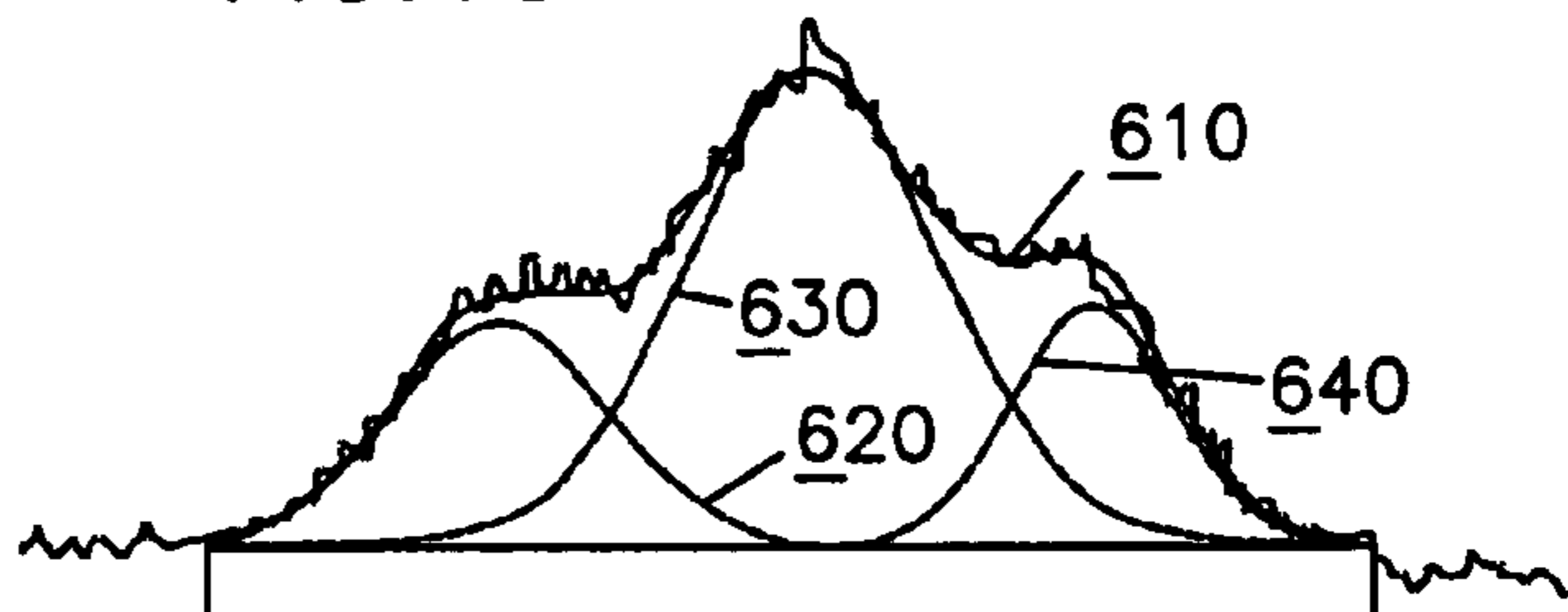


FIG. 14A

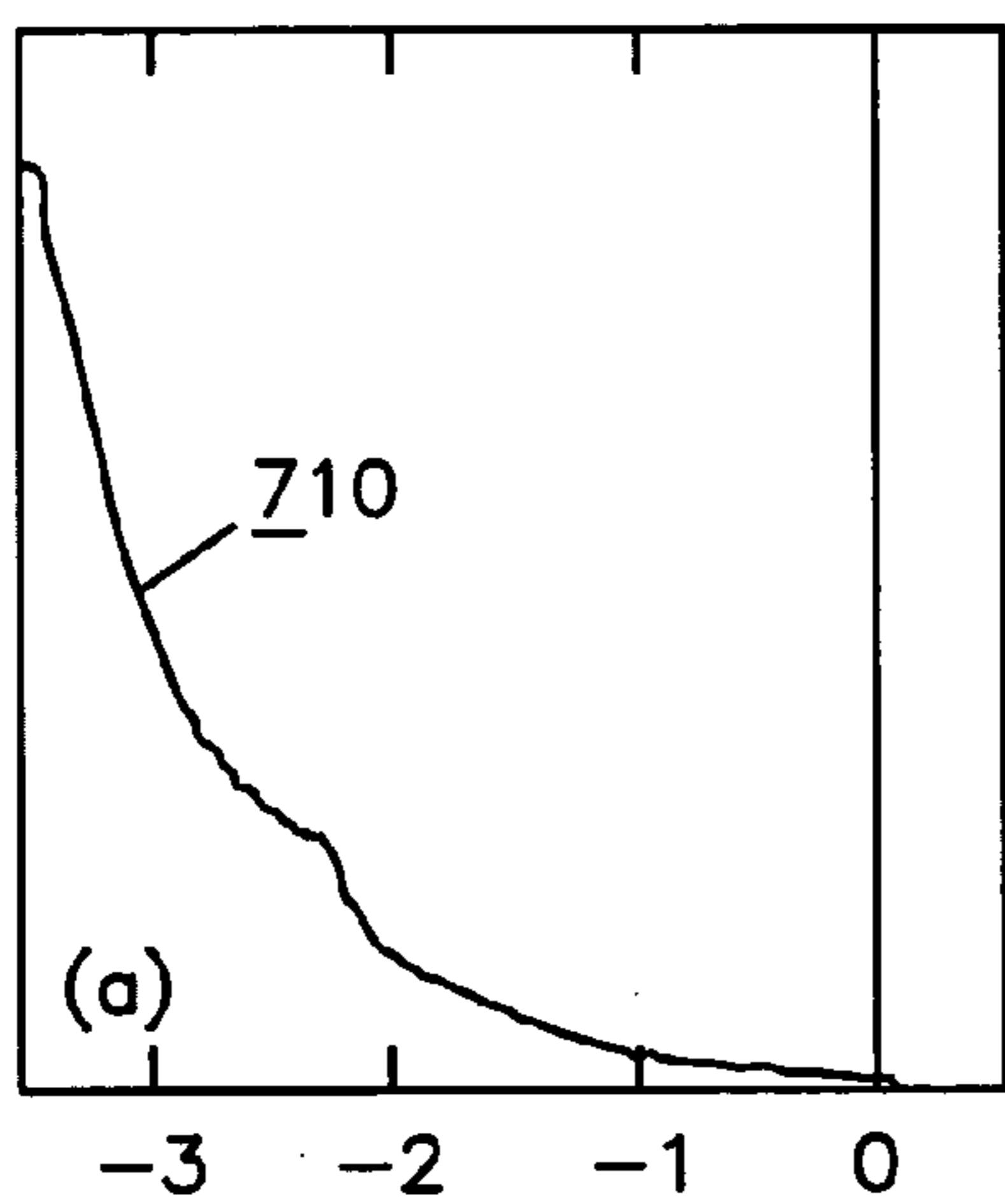
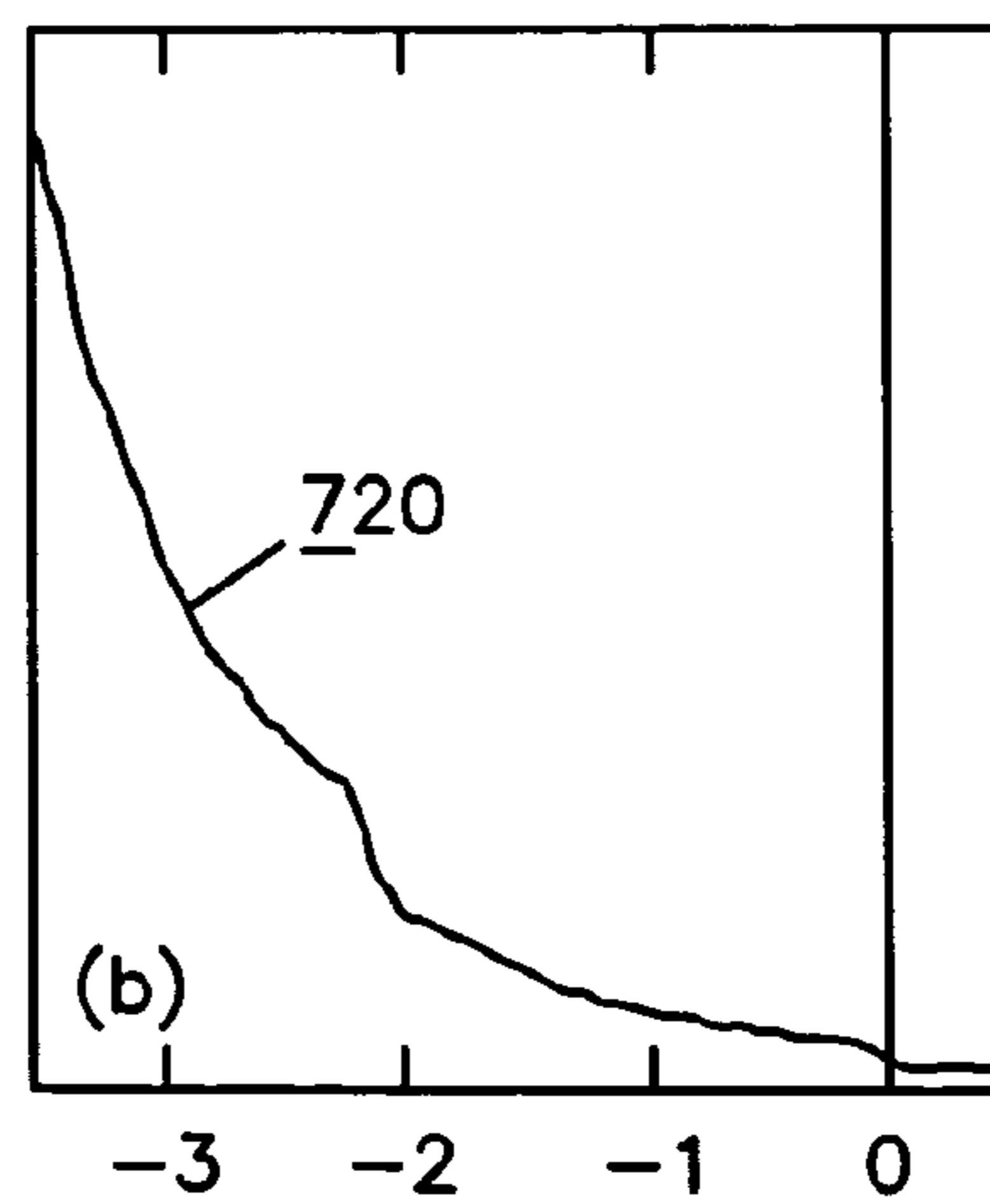


FIG. 14B





**HIGH-TEMPERATURE SUPERCONDUCTOR  
DEVICES AND METHODS OF FORMING THE  
SAME**

**CROSS-REFERENCE TO RELATED  
APPLICATIONS**

[0001] This is a continuation-in-part of U.S. patent application Ser. No. 10/704,215, filed Nov. 6, 2003, which is a continuation of U.S. patent application Ser. No. 09/082,486, filed May 20, 1998, which claims the benefit of U.S. Provisional Patent Application Ser. No. 60/047,555, filed May 22, 1997; and claims the benefit of U.S. Provisional Patent Application Ser. No. 60/437,781, which applications are hereby incorporated by reference in their entirety.

**STATEMENT OF GOVERNMENT INTEREST**

[0002] This invention was made with United States Government support under Contract No. N0014-96-C-2095 awarded by the Naval Research Laboratory. The United States Government has certain rights in the invention.

**FIELD OF THE INVENTION**

[0003] This invention relates generally to superconductor devices. More particularly, the invention relates to high-temperature superconductor devices, for example high-temperature superconductor ("HTS") Josephson junctions.

**BACKGROUND OF THE INVENTION**

[0004] Since the 1986 discovery of the new class of oxide superconductors, also known as high temperature superconductors (HTS), cuprate superconductors, and perovskite superconductors, many attempts have been made to fabricate useful junctions, devices, circuits, and systems. This discovery promised to bring the many benefits of superconductors to electronic circuits at practically attainable temperatures. Achieving these benefits, however, has been less than straightforward due to the nature of the materials, which is quite different from the metals and semiconductors normally used in electronics applications.

[0005] The first obstacle, now largely overcome, was the polycrystalline nature of these new ceramic superconductors. Traditional low temperature superconductors, having a superconducting transition temperature  $T_c < 23$  K, are metals, metal alloys, or intermetallic compounds. Metals are usually polycrystalline, but metallic bonding is so delocalized that the grain boundaries in these materials are not electrically active. Furthermore, coherence lengths in these superconductors are on the order of 100 nm, which is much larger than the size of a single grain, i.e., a single crystalline making up part of the polycrystalline body. This means that the superconducting electron pairs are affected by the average environment produced by many individual grains and are therefore not extremely sensitive to inhomogeneities at grain boundaries or other regions whose size is much less than a coherence length.

[0006] The cuprate superconductors are ceramic materials with ionic and covalent bonds that are more directional and localized than metallic bonds. Across grain boundaries atoms are displaced with respect to their normal positions in the ideal crystal. Chemical bonds between these displaced atoms are stretched, bent, broken, and sometimes vacant, depending on the atoms considered and their relative dis-

placements in distance and angle from their ideal positions. This sort of disruption of the electronic structure of the material, much more severe with directional bonding than with isotropic metallic bonding, can cause corresponding disruptions in the transport properties of the material. It is for this reason that bulk polycrystalline specimens of the cuprate superconductors typically have critical current densities, which are reduced by an order of magnitude or more when compared to well oriented epitaxial films of the same chemical composition.

[0007] Another exacerbating factor is the very small and anisotropic coherence length of the superconducting perovskites. The coherence length in these materials has been estimated at about 1.5 nm in the a-b plane and about ten times less (0.15 nm) in the c-direction. These distances are much smaller than the dimensions of a typical grain, and are of the order of the lattice constant in the c-direction in  $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$  ( $0 \leq \delta \leq 1$ ). The result is that the electrical properties of these superconductors are strongly influenced by the microstructure as well as the local environment of defects, including impurity atoms, vacancies, voids, dislocations, stacking faults, and grain boundaries.

[0008] With such a small coherence length, virtually any deviation from perfection can interrupt the flow of supercurrent enough to form a junction. Early thin films were so full of grain boundary junctions, due to their poor in-plane epitaxy, that the inherent properties of the material were masked by the behavior of thousands of weak-link junctions occurring naturally in the polycrystalline layers. By the early 1990s, however, the crystal growth technology had progressed to a state in which high-quality, well oriented epitaxial layers of high temperature superconductors could be grown by a variety of techniques and on a variety of substrates, so that well characterized junctions could be made in several ways. Most of these junctions, however, were deficient in one or more characteristics desirable for use in digital electronics or superconductive quantum interference devices ("SQUIDS").

[0009] The Josephson junction is one of the basic elements of superconductor electronic devices, and is well-developed in low temperature superconductors. For high-temperature superconductors, however, development of a technology for reproducible junctions has been difficult. The first reported, intentionally fabricated, junctions were of the weak-link type. They are characterized by a critical current density  $J_c$ , a critical current  $I_c$ , an effective device cross-sectional area  $A$ , junction resistance,  $R_n$ , and normalized junction resistance  $R_n A$ . Later, junctions with an interlayer of an insulating material (SIS junctions) or normal metal (SNS junctions) were developed. However, few of these approaches were commercially useful, and none met all of the requirements for a useful technology. To make good electronic devices and circuits from the oxide superconductors, a manufacturable junction technology must be developed.

[0010] A manufacturable technology is one that gives reproducible and predictable results when a defined series of processing steps is carried out. The devices perform as designed, and the processes are robust, that is, are sensitive to small changes in processing parameters. A particular requirement of the technology is that all necessary processing steps should be compatible, so that one step does not destroy the results of a step that must be performed earlier in the flow.

[0011] The junctions formed by this technology should meet design criteria as specified by the user. The junctions must perform reliably at a specified temperature. They must carry a current density of 100 to 100,000 A/cm<sup>2</sup>, at the designer's discretion, and must do so for the foreseeable lifetime of the device. Fluctuations in the critical current of each junction, as well as variations from junction to junction in a circuit, must be minimized. Noise must be reduced to a level at which random signals due to noise are much smaller and less common than the true signals the circuit is designed to detect.

[0012] For useful superconducting quantum interference devices (SQUIDs) it is necessary to fabricate matched pairs of junctions in a predetermined geometrical relationship. Not only must each junction have predictable qualities, but they must be easy to position at will. In practical terms, this implies that all of the materials used in a circuit should be patterned using similar techniques.

[0013] Development of a HTS circuit technology has remained elusive because of the difficulty of fabricating reproducible, uniform Josephson elements that possess suitable electrical properties for applications such as single flux quantum (SFQ) logic and SQUIDs. The state of the art is the ramp-edge process employing a Co-doped YBCO barrier layer. This process is described in Char, et al., U.S. Pat. No. 5,696,392 "Improved Barrier Layers for Oxide Superconductor Devices and Circuits," which is incorporated herein by reference. The devices disclosed by Char, et al. and further refined as disclosed in W. H. Mallison, S. J. Berkowitz, A. S. Hirahara, M. J. Neal, and K. Char, "A multilayer YBa<sub>2</sub>Cu<sub>3</sub>O<sub>x</sub> Josephson junction process for digital circuit applications," Appl. Phys. Lett., vol. 68, pp. 3808, 1996, have spreads in junction parameters approaching that which is needed to make multi-junction circuits. However, these junctions appear to operate as true proximity-effect elements—their values of  $R_n$  are quite low due to the low resistivity of the barrier material in their SNS configuration. Therefore, most of their usefully high  $I_c R_n$  product derives from a relatively high  $I_c$ , outside the range that is useful for SFQ devices. SFQ technology holds promise in high speed switching. Moreover, difficulty with the deposition of reproducible Co-YBCO films has limited the exploitation of those junctions.

[0014] Other types of high- $T_c$  SNS geometry junctions have clearly been plagued by an excess resistance that does not correlate with that of the barrier material. This resistance has been shown to exist at the YBCO/barrier interface, most likely arising from oxygen disorder due to mismatches in lattice and thermal expansion coefficients. Unfortunately, although the  $R_n$  of these devices is in a useful range, their uncontrollable excess resistance makes them unsuitable for a reproducible junction technology. Indeed, we speculate that the primary weak-link effect in many of these devices arises specifically because of the weakened superconductivity at the interface, not due to the intended proximity effect.

[0015] Successful manufacture of Co-YBCO junctions has required great care in order to insure elimination of an excess interface resistance. If we are to increase the  $R_n$  of these devices, two obvious options become apparent: (1) add an excess interface resistance, or (2) increase  $R_n$  of the barrier layer, while preserving a negligible interface resistance. Unfortunately, we don't know how to perform the first

item uniformly, and the second task requires the deposition of a high-resistivity, lattice-matched, pinhole-free barrier on the scale of a few nm. Such material expertise is presently beyond our capability, and thus, ideal junctions using Co-YBCO are not yet commercially practicable. Furthermore, it is not at all clear that  $I_c R_n$  remains high for high-resistivity barriers.

[0016] Josephson junctions have also been reported using surface-treated YBCO as the barrier. For example, R. B. Laibowitz, R. H. Koch, A. Gupta, G. Koren, W. J. Gallagher, V. Foglietti, B. Oh, and J. M. Viggiano, Appl. Phys. Lett. 56, 686 (1990) used ion milling to damage the interface followed by ex-situ, low-temperature plasma oxyfluorination to repair the damage. K. Harada, H. Myoren, and Y. Osaka, "Fabrication of all-high- $T_c$  Josephson junction using as-grown YBa<sub>2</sub>Cu<sub>3</sub>O<sub>x</sub> thin films," Jap. J. Appl. Phys., vol. 30, pp. L1387, 1991, report ion plasma treated YBCO surfaces exhibiting Josephson behavior. C. L. Gia, M. I. Faley, U. Poppe, and K. Urban, "Effect of chemical and ion-beam etching on the atomic structure of interfaces in YBa<sub>2</sub>Cu<sub>3</sub>O<sub>7</sub>/PrBa<sub>2</sub>Cu<sub>3</sub>O<sub>7</sub> Josephson junctions," Appl. Phys. Lett., vol. 67, pp. 3635, 1995, report that ion milling produces a surface phase of PBCO consistent with a cubic structure. However, these surface methods fail to achieve a sufficiently reproducible modified-surface barrier high- $T_c$  junction technology.

[0017] Moreover, many oxide superconductors have crystal structures and compositions that accommodate an appreciable range of oxygen content. For example, in the well-known "1-2-3" oxide superconductor, YBa<sub>2</sub>Cu<sub>3</sub>O<sub>7- $\delta$</sub>  ("YBCO"), the oxygen content may deviate from stoichiometry (i.e., where  $\delta=0$ ) by a significant amount. Oxygen deficiency,  $\delta$ , may be as high as 1. Experience has shown that both normal and superconducting properties, such as transition temperature, depend strongly on oxygen content and atomic arrangement. Generally,  $T_c$  decreases as oxygen deficiency increases.

[0018] Unfortunately, oxide superconductors have a tendency to lose their oxygen content to the surrounding atmosphere, even at normal storage conditions. The change in oxygen content results in changes in the electronic structure of the oxide material. As an example, **FIG. 8** shows a series of X-ray photoelectron spectra (XPS) taken at the surface of a YBCO film after the film was formed. Initially, and for a few days after the film was made, the XPS of the Ba 4d emission shows three peaks. See, for example, spectra **110**, **120**, **130**, **140**, **150**, **160** and **170**, taken immediately, 15 minutes, 1 hour, 2 hours, 4 hours, 1 day and 3 days, respectively, after the film was made. At three weeks (spectrum **180**), the low-energy peak **112**, which is associated with Ba in the bulk, superconducting phase, had begun to disappear. At three months (spectrum **190**), the low-energy peak **112** has entirely disappeared. The higher-energy peaks, **114** and **116**, which are associated with Ba in a non-conducting surface phase, remained. This change in XPS indicates that the superconducting YBCO phase has disappeared over time, at least from the near-surface regions. It is believed that this is due to oxygen loss and from corrosion resulting from, for example, Ba reacting with carbon to form barium carbonates.

[0019] The loss of oxygen and the associated structural changes lead to change, and often degradation, of certain

properties in the superconductor. This variation or degradation is highly undesirable. In telecommunication applications, for example, oxide superconductors have been used in thin-film devices such as high-performance, high-precision filters. These filters are often placed inside sealed vacuum chambers and are difficult to tune once sealed. Oxygen loss over time or as a result of bake-out and other procedures at elevated temperatures can produce shifts and degradation of filter characteristics.

[0020] Additionally, the performance of oxide superconductor devices may also suffer as a result of corrosion due to chemical reactions between the superconductor and its environment.

#### SUMMARY OF THE INVENTION

[0021] One embodiment of the invention provides a Josephson junction having reproducible properties with a high  $R_n$ . Another embodiment of the invention provides a method of fabricating a Josephson junction having a high, reproducible, and controllable  $I_c R_n$  product.

[0022] An electronic device is provided that includes a crystalline substrate; a first superconductive element formed on and epitaxial to the substrate, the superconductive element including a superconductive oxide having a surface including a barrier means, a second superconductive element formed on and epitaxial to the first superconductive element, whereby a Josephson junction is formed between the first superconductive element and the second superconductive element. In contrast to prior art Josephson junctions which relied on grain boundaries at which crystalline lattice changed direction or on metallic or insulating barrier layers, the edge-junction of the present invention can be formed without deposition of any barrier at all.

[0023] The invention takes advantage of a property of the notoriously complex YBCO material; that its electrical properties are tunable over a wide range, from an insulator to a superconductor, by altering its oxygen content and order, changing its crystal structure, or by adding dopants. The invention uses this property to create a thin layer of high-resistivity material on, for example, the junction edge of a Josephson junction, by altering the structure or chemistry of YBCO only at the surface. In the case of a Josephson junction, if this is done prior to deposition of the YBCO counterelectrode, a high  $R_n$  device is formed.

[0024] In the invention, the surface of a first layer of YBCO is modified by using a combination of vacuum annealing and plasma treatment. Unlike previous attempts in which a junction was formed ex situ via ion milling or etching, the current invention does not lead to weakened superconductivity in the second layer due to lattice mismatch at the interface.

[0025] The invention also provides an oxide superconductor that has a protective layer on the surface thereof. In one embodiment the protective layer is a passivation layer. The passivation layer can prevent deterioration or degradation of structural and physical properties of the oxide superconductor due to oxygen migration or corrosion.

[0026] In one embodiment, the passivation layer covers at least a portion of the surface of the superconductor. In another embodiment, the passivation layer covers all por-

tions of the surface of the superconductor that would otherwise be exposed to the ambient environment.

[0027] The passivation layer can be formed by modifying the surface of the superconductor so that the passivation layer is formed at least partially by material originating from the oxide superconductor. In another embodiment, the passivation layer is an ion-modified layer of the oxide superconductor.

[0028] The oxide superconductor, which can be YBCO, can be deposited onto a suitable substrate and at least a portion of the surface of the superconductor is then passivated. Optionally, a buffer layer can be deposited onto the substrate prior to deposition of the oxide superconductor. After the oxide superconductor is deposited, it is then annealed in some embodiments of the invention. Following annealing, the surface of the oxide superconductor is treated by ion bombardment, followed by a further optional annealing, heating at elevated temperature in an oxygen-rich environment, and cooling in an oxygen-rich environment.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0029] FIG. 1 is a schematic representation of a side view of a junction of the invention;

[0030] FIG. 2 shows the processing steps used to form the interface-engineered junction;

[0031] FIG. 3 illustrates an I-V curve for an interface-engineered junction over the temperature range 4.2 K to 60 K.  $R_n$  of this  $4 \mu\text{m} \times 0.15 \mu\text{m}$  device is  $3 \Omega$ ;

[0032] FIG. 4 illustrates examples of the dependence of  $I_c$  on temperature for several junctions of the invention;

[0033] FIG. 5 illustrates the dependence of  $I_c$  on applied magnetic field at 40 K for a junction with  $R_n$  of  $2.9 \Omega$ ;

[0034] FIG. 6 shows the range of  $I_c R_n$  and  $R_n$  which is presently attainable at 4.2 K for the junction process. The data are plotted as a function of  $J_c$ , and the lines represent least-square fits to the data. The junction area is  $4 \mu\text{m} \times 0.15 \mu\text{m}$ ;

[0035] FIG. 7 shows values of  $I_c$  and  $R_n$  at 4.2 K for a O-junction test chip. The  $1\sigma$  values are 7.8% for  $I_c$  and 3.5% for  $R_n$ .

[0036] FIG. 8 is a graphic depiction of a series of X-ray photoelectron spectra (XPS), taken over a period of time, of a prior art YBCO film without the benefit of a passivation layer of the invention;

[0037] FIG. 9 is a schematic cross-sectional view of a device having a superconductor with a passivation layer in accordance with the invention;

[0038] FIG. 10 lists the steps in a process for making a superconductor with a passivation layer according to the invention;

[0039] FIG. 11 lists the more detailed steps of the process illustrated in FIG. 10;

[0040] FIG. 12 shows the XPS of the surface of a YBCO film without the benefit of a passivation layer;

[0041] FIG. 13 shows the XPS of the surface of a YBCO film with a passivation layer; the films studied in FIGS. 12

**and 13** were made on the same day, and both spectra were taken after the same number of days after the films were made; and

[0042] **FIG. 14** shows a comparison between the XPS of the passivated surface of a YBCO film and  $\text{YBa}_2\text{Cu}_3\text{O}_6$  single crystal.

#### DETAILED DESCRIPTION OF THE INVENTION

[0043] Formation of the Junctions of the Invention

[0044] **FIG. 1** is a schematic cross-sectional representation of a junction in accordance with one embodiment of the invention. The drawing is not necessarily to scale. **FIG. 2** is a flow schematic of the preferred process for forming the superconducting device of the invention.

[0045] A suitable crystalline substrate **10** for the structure is selected. Any substrate suitable for supporting epitaxial growth of an oxide superconductor, either alone or with an intermediate buffer layer may be used. Suitable substrates include  $\text{MgO}$ ,  $\text{LaAlO}_3$ , sapphire, yttrium-stabilized zirconia, strontium titanite and the like. In one embodiment, the substrate is  $\text{LaAlO}_3$ . In another embodiment, the substrate is (001)  $\text{LaAlO}_3$ . As used herein, the term crystalline substrate refers to a support material having major crystallographic axes and having a lattice structure suitable for the growth of a superconducting oxide.

[0046] A buffer layer (not depicted in **FIG. 2**) may optionally be deposited on the substrate prior to deposition of the superconductive oxide. Buffer layers are generally used to provide chemical isolation from the substrate or to provide an improved lattice match between the substrate and the superconductive oxide. Suitable buffer layers include  $\text{CeO}_2$ ,  $\text{SrTiO}_3$  and  $\text{CaTiO}_3$ . The buffer layer and the superconductive oxide may be deposited using any of several known methods for achieving epitaxial growth of the oxide, including laser ablation, and reactive coevaporation. In the embodiment depicted in **FIG. 1**, a buffer layer of  $\text{CeO}_2$  (not depicted in **FIG. 1**) and a first superconducting layer **12** of  $\text{YBa}_2\text{Cu}_3\text{O}_{7.8}$  (YBCO), about 150 nm thick in this case, were deposited on the substrate. However, the invention should not be viewed as limited to YBCO. Other oxide superconductors may also be used.

[0047] Any suitable methods known to those of skill in the art, having read this specification, for depositing these layers can be utilized. In one embodiment, deposition conditions for these materials, when deposited by laser ablation, are: substrate temperatures about  $780^\circ\text{C} \pm 20^\circ\text{C}$ ., oxygen pressure 100-600 mT. In another embodiment, about 300-400 mT, laser energy about  $1\text{-}5\text{ J/cm}^2$  at the target. More detailed process conditions for epitaxial film growth are described in many publications.

[0048] Next an insulator **14**, in this case a layer of PBCO capped with a layer of epitaxial  $\text{SrTiO}_3$  **16**, is deposited to prevent contact between the first superconducting layer **12** and the second superconducting layer **18**. Other insulators having good insulating properties, suitable lattice structures and chemical compatibility with the superconductor may also be used.

[0049] The first superconducting layer **12** and the overlying insulators **14**, **16** are then patterned as desired. For the

devices whose test results are shown, patterning was accomplished with standard photolithography and inert ion etching.

[0050] Prior to insertion into the laser ablation vacuum chamber, the edge is prepared via an Ar ion mill clean at 200 V for about one minute. Other voltages and times of Argon milling are within the scope of the invention. The sample is then heated under vacuum. In one embodiment, it is heated to about a range of  $10^{-5}$  to  $10^{-7}$  Torr to between  $400$  and  $500^\circ\text{C}$ . In another embodiment, it is heated to about  $450^\circ\text{C}$ ., for a period up to about one hour. In yet another embodiment, it is heated for about 30 minutes. At temperatures above about  $500^\circ\text{C}$ . in vacuum, bulk orthorhombic YBCO films may be completely converted to a quasi-cubic phase.

[0051] Following this anneal, the pre-device is treated, in situ, to uniformly convert only the exposed YBCO surface **20** to a slightly different phase, structure, or chemical configuration. This is generally referred to as ion treating the surface of the superconductor. This can be accomplished, for example, by using a background gas of Ar and/or  $\text{O}_2$  plasma generated by biasing the substrate heater with an rf source. In one embodiment, the background gas is Ar. Any mixture is suitable, but in one embodiment, a 1:1 mixture of Ar/ $\text{O}_2$  is utilized. In one embodiment, a plasma treatment with a forward power of about 100-400 watts in a background total pressure of about 10 to 100 mTorr is sufficient to form an interface material whose properties allow fabrication of Josephson devices. In another embodiment, the background total pressure of about 20-50 mTorr is utilized. The typical reflected rf power is less than about 10 W and the dc self-bias on the heater is typically about 600-900 V. Specific conditions of the plasma can be adjusted to achieve junctions with the desired parameters. The ion treatment, of which a plasma treatment is one example, is generally done for several minutes to an hour. In one embodiment the plasma treatment is done for about 20 minutes, followed by a further optional vacuum anneal, for about 30 minutes at about  $400^\circ\text{C}$ ., in one embodiment. Other gasses may be used as the background gas, including noble gasses such as Xe and halogens, such as  $\text{F}_2$  for example. If other gasses are used, the conditions may need to be adjusted to achieve the desired parameters. Persons skilled in the art would be able to make such adjustments, having read this specification.

[0052] In one embodiment, following the vacuum anneal, about 300-400 mTorr of  $\text{O}_2$  is introduced and the temperature is increased to about  $785^\circ\text{C}$ . Immediately thereafter, the YBCO counter-electrode is deposited under standard conditions. The bottom YBCO is re-oxygenated before and/or during the deposition, as its  $T_c$  remains quite high. In one embodiment, chips are patterned to form **5** junctions with widths of about  $4\text{ }\mu\text{m}$  each.

[0053] Junction Properties

[0054] Devices of the invention display RSJ-type I-V characteristics over the entire temperature range of operation; examples are shown in **FIG. 3**. This behavior may be contrasted with Co-YBCO edge junctions, whose temperature range of operation is limited due to their exponential  $I_c(T)$  dependence and the eventual onset of superconductivity in the barrier layer.

[0055] **FIG. 4** displays the  $I_c(T)$  dependence for a few junctions of the invention. Note that the behavior is quasi-

linear in accord with many types of high- $T_c$  devices. Also, note that the temperature at which a critical current decrease is begun to be seen with decreasing  $I_c$ . This behavior is not due to thermal noise rounding alone, however, but also depends on the value of  $R_n$  of the device.

[0056] These junctions can respond quite strongly to an applied magnetic field. The critical current can modulate to zero in a few gauss at high temperatures, and  $I_c(H)$  displays a Fraunhofer-like pattern, as shown in FIG. 5. The periodicity is consistent with the physical width of the device if flux focusing is taken into account. Even at 4.2 K where excess current is notable, these junctions continue to modulate by 80 to 90% in the best cases.

[0057] In FIG. 6, the ranges of  $I_c R_n$  and  $R_n$  that are attainable at 4.2 K are displayed. Note that  $I_c R_n$  products from 0.3 to 5 mV are possible, with corresponding  $R_n A$  values of  $3 \times 10^{-7}$  to  $1 \times 10^9 \Omega \text{cm}^2$ . A clear scaling relation exists between  $I_c R_n$  and  $J_c$  similar to that observed for grain boundary weak links, although the dependence is somewhat different for these interface-engineered junctions.

[0058] Even at higher temperatures, the parameters of these junctions may make them quite attractive for applications. For example, at 40 K,  $I_c R_n$  values between 0.1 and 2 mV can be obtained. Thus embodiments of the invention may include junctions with  $I_c R_n$  products of 500  $\mu\text{V}$  and corresponding  $I_c$  and  $R_n$  values of 500  $\mu\text{A}$  and 1  $\Omega$  for a size of  $4 \mu\text{m} \times 0.15 \mu\text{m}$ .

[0059] Of course, these junctions may not be useful for multi-junction circuits unless they can be made uniformly. The spread of these junctions on 10- and 20-junction test chips have been preliminary studied. A result from one of these tests is displayed in FIG. 7. This 10-junction chip displayed a  $I_c$  spread in  $I_c$  of 7.8% and a spread in  $R_n$  of 3.5%. The spreads over 20 junctions have been as low as 12% in  $I_c$  thus far.

[0060] The junctions of the invention may find uses in a variety of applications. Josephson junctions are an essential feature of Superconducting Quantum Interference Devices ("SQUID(s)"), which are useful in magnetic sensing applications and as amplifiers. The junctions are also useful in digital logic devices, such as in high-speed switching and clock recovery circuits.

[0061] The invention provides methods of fabricating all-YBCO Josephson junctions that can avoid the deposition of a barrier layer. These devices are uniform and reproducible. The tested devices have worked as a resistively shunted junction. Their electrical characteristics are easily adjustable within a range suitable for electronics circuit technology. For example, an  $I_c$  of several hundred  $\mu\text{A}$  and an  $R_n$  of 2  $\Omega$  at 40K is ideally suited for RSFQ technology. The junctions are also well suited to making 1  $\Omega$  SQUIDS with an  $I_c$  of 1 mA at 40K.

[0062] It would be apparent to one skilled in the art, having read this specification, that variations of the process are also within the scope of the invention. Examples of such variations include the use of other superconductive oxides, variation of the background gas (and could include other noble gasses or halogens, alone or in combination), and variations in time and temperature for various steps, for example.

[0063] Formation of a Passivation Layer of the Invention

[0064] The invention also provides an oxide superconductor having a protective surface layer that substantially prevents deterioration of structural and physical properties of the superconductor due to oxygen migration or corrosion. The protective surface layer is referred to herein as a passivation layer.

[0065] Referring to FIG. 9, a superconductor device 200 includes an oxide superconductor layer 220, which is typically formed on a substrate 210. For example, the oxide superconductor layer 220 can be epitaxially grown on the substrate 210. An example of a suitable oxide superconductor is YBCO. However, it is to be realized that the invention could be implemented using other oxide superconductors.

[0066] Any substrate suitable for supporting growth of an oxide superconductor can be used. For example, materials such as MgO, LaAlO<sub>3</sub>, sapphire, yttrium-stabilized zirconia (YSZ), and SrTiO<sub>3</sub> can be used as the substrate 210. The substrate 210 typically has a chosen crystallographic orientation for epitaxial growth of the oxide superconductor layer 220. For example, an (001) LaAlO<sub>3</sub> substrate can be used.

[0067] The substrate can also be a noncrystalline or polycrystalline substrate with a suitably aligned crystalline buffer layer deposited on top by various methods known to those of ordinary skill in the art, having read this specification, such that an epitaxial superconductor thin film may be deposited.

[0068] The device can also include an intermediate layer 230, which can be a buffer layer that provides chemical isolation or improved lattice match between the rest of the substrate 210 and the oxide superconductor 220. Examples of suitable buffering materials include, but are not limited to, CeO<sub>2</sub>, SrTiO<sub>3</sub>, and CaTiO<sub>3</sub>. The intermediate layer 230 can also include other layers in a multi-layer circuit. As illustrated in FIG. 9, the intermediate layer 230 is between only a portion of the substrate 210 and the superconductor 220. However, the intermediate layer 230 can be between the entire substrate 210 and the superconductor 220.

[0069] The oxide superconductor layer 220 also includes a passivation surface layer 240. A passivation surface layer can function to substantially reduce or prevent oxygen out diffusion (i.e. oxygen diffusing out of the layer 220) and/or corrosion. That is, the passivation layer can be characterized by a substantially lower oxygen mobility as compared to that of the oxide superconductor. A passivation layer can also be characterized as isolating the portion(s) of the superconductor covered thereby from the ambient atmosphere or other non-conducting surroundings. The passivation layer 240 can additionally be an electrical insulator, as well as being corrosion resistant (i.e. the layer 240 prevents reaction of the constituent atoms with other elements).

[0070] The passivation layer 240 need not cover the entire portion of the superconductor surface. In another embodiment, the passivation layer 240 covers all surfaces of the superconductor 220 that would otherwise be exposed to the ambient, as illustrated in FIG. 9.

[0071] The passivation layer 240 can be a native layer to the oxide superconductor 220, that is, a layer formed at least partially by the material originating from the oxide superconductor 220. Native passivation layers may provide a

number of advantages over externally applied coatings. For example, because the native passivation layer is grown from the superconductor it covers, the bonding between the two can be more intimate than that between a superconductor and an externally applied coating. It is believed that the native passivation layer is thus mechanically more robust than externally applied coatings. In addition, the native passivation layer may also have a more uniform thickness and construction, i.e. be free of holes. The lack of holes can be an advantage because holes can provide spots for corrosion to occur. Uniformity in thickness can also be important if an additional layer(s) is to be grown on top of the passivation layer **240**.

[0072] Specifically, the passivation layer **240** can be an ion-modified layer of the oxide superconductor **220**. For example, the passivation layer **240** can be a plasma-treated surface layer of the oxide superconductor **220**. The passivation layer **240** can be of any suitable thickness. For example, the layer **240** can be as thin as between about 1-5 nm. In another embodiment, the passivation layer **240** can be as thin as between about 2-3 mm.

[0073] The passivation layer **240** can be covered by one or more additional layers of material if desired. For example, one or more protective layers could be disposed on the passivation layer **240** to protect against scratches and other damage to the passivation layer. In addition, because the passivation layer **240** is epitaxial and crystalline, one or more epitaxial layers can be grown on top of the layer **240**. For example, a Josephson junction having a junction layer produced by ion-bombardment of an oxide superconductor film could be produced as discussed above.

[0074] A method for passivating the surface of an oxide superconductor includes modifying the surface. The modification can be accomplished by bombarding the surface with ions, including argon and oxygen ions. Ion bombardment can be accomplished by treating the surface of the oxide superconductor with a plasma of ions, for example argon or oxygen or a mixture of both. Ion bombardment can also be accomplished by using any other type of ion source known to one of skill in the art, having read this specification, including ion beam sources. The ion bombardment can be performed at elevated temperatures, with vacuum annealing at elevated temperature, along with a high temperature oxygen anneal as described further below.

[0075] Referring to **FIG. 10**, a method of making a superconductor device includes depositing (step **310**) an oxide superconductor film on a substrate and passivating the surface of the superconductor film (step **320**). Another embodiment of a method in accordance with the invention can be seen in **FIG. 11**, this method includes first depositing (step **410**) an oxide superconductor film on a substrate. A buffer layer is optionally deposited on the substrate prior to deposition of the oxide superconductor. The oxide superconductor film and buffer layer can be deposited using any of several known methods, including but not limited to laser ablation, sputtering, and reactive coevaporation. For example, for epitaxial deposition by laser ablation, the substrate temperatures can be about 780° C.±20° C., the oxygen pressure between about 100-600 mTorr. In another embodiment, the oxygen pressure is between about 300-400 mTorr, and laser energy about 1-5 J/cm<sup>2</sup> at the target. Further details regarding process conditions for epitaxial film

growth are known in the art. See, for example K. Char and V. Matijasevic, "HTS film growth," in *Engineering Superconductivity*, ed. by P. J. Lee (Wiley, New York), **2001**, which is incorporated herein by reference.

[0076] Next, the oxide superconductor film can be annealed (step **420**), either in the same deposition chamber or after being transferred to another vacuum chamber. For a YBCO film, for example, the background pressure can range from about 10<sup>-7</sup> to about 10<sup>-5</sup> Torr. Inert gas annealing could also be used. The annealing temperature can be between about 400 and 500° C. In another embodiment, it is between about 450° C. Annealing time can vary from about 15 minutes to about one hour. In another embodiment, the anneal time is about 30 minutes. Choices of alternative and other annealing parameters are well within the capabilities of persons skilled in the art, having read this specification.

[0077] Following the annealing, the device is treated to convert the exposed YBCO surface to a different phase, structure, or chemical configuration. This can be accomplished by ion bombardment (step **430**) followed by annealing (step **440**) of the surface. The ion bombardment (step **430**) can be performed by treating the surface with a plasma of Ar or an Ar—O<sub>2</sub> mixture, for example, a 1:1 mixture of Ar and O<sub>2</sub>. For example, the Ar background pressure can range from about 10 to about 100 mTorr. In one embodiment, the background pressure ranges between about 20-50 mTorr. In another embodiment, the background pressure is about 20 mTorr. Noble gasses such as Xe and halogens such as F<sub>2</sub> could also be used in place of Ar and O<sub>2</sub>.

[0078] The plasma can be generated by an RF source in a manner known to those of skill in the art, having read this specification. The forward RF power that is used can be between about 100 and about 400 watts. In another embodiment, it is about 300 watts. The typical reflected RF power is less than about 10 W and the DC self-bias on the heater can be set at between about -600 to about -1000 V. In one embodiment, the DC self-bias on the heater is set at about -800 V.

[0079] The device can be heated by a substrate heater, which can be electrically biased by being electrically connected to a suitable source. The temperature of the device can be held at a temperature between about 300° C. to about 650° C. In one embodiment, the temperature is held at about 400° C., while the surface of the oxide superconductor is subjected to the plasma treatment. The plasma treatment can last between two minutes and an hour. In one embodiment, it lasts between about five and twenty minutes. In yet another embodiment, it lasts about ten minutes. Specific plasma treatment parameters can be adjusted by one of skill in the art, having read this specification, to achieve the desired characteristics of the passivation layer.

[0080] The ion bombardment can be followed by a further vacuum annealing (step **440**). The annealing conditions can be similar to the first annealing (step **420**). For example, the annealing step **440** can last about 30 minutes at temperatures between about 300° C. to about 600° C. In another embodiment, the temperature is about 400° C., at a pressure of from about 10<sup>-7</sup> to about 10<sup>-5</sup> Torr. Other annealing conditions can also be used, as would be apparent to persons skilled in the art, having read this specification.

[0081] Following the vacuum annealing step **440**, the oxide superconductor film is heated in an oxygen-rich

environment (step **450**). It is thought, but not relied upon, that this heating step results in a passivation layer that has a different phase, or crystal structure, than the oxide superconductor film. It has been found that the passivation layer is quasi-cubic and its composition is probably not "1-2-3". It is thought that the heating may anneal and remove atomic defects from the passivation layer already partially formed during ion bombardment to "perfect" the final passivation layer, or cause the new phase to form by allowing the atoms in the ion-bombarded regions to rearrange. The oxygen pressure can be set at between about 100 to about 600 mTorr. In one embodiment between about 300 to about 400 mTorr, and in another embodiment at about 350 mTorr. The temperature can be set at between about 700° C. to about 800° C., and in another embodiment at about 785° C. The heating step **450** lasts about 10 minutes in one embodiment.

[**0082**] The device is then cooled down to room temperature in an oxygen-rich environment in step **460**. For example, the oxygen pressure can be increased to about 600 Torr after the heating step **450**.

[**0083**] The process discussed above can be varied in other ways to produce a variety of devices without departing from the spirit and scope of the invention. For example, the surface layer **240** can be doped with various elements to achieve device properties depending on the specific applications in which the device is to be used. In addition, it is contemplated that the first annealing step could be left out.

## WORKING EXAMPLES

### Example 1

[**0084**] Two YBCO films were grown under substantially the same conditions on the same day. The first film did not undergo surface treatment, whereas the second film was plasma-treated as described above.

[**0085**] The first film was grown by pulsed laser ablation using a KrF excimer laser operating at a repetition frequency of 10 Hz; fluence on the YBCO target was about 1 J/cm<sup>2</sup>. The single-crystal LaAlO<sub>3</sub> substrate was attached to the heater with silver paste and was located about 5 cm from the target. A 20-nm-thick CeO<sub>2</sub> buffer layer was first deposited at a substrate temperature of 785° C. and a background oxygen pressure of 100 mTorr. A 200-nm-thick YBCO film was deposited immediately thereafter at a substrate temperature of 785° C. in a background oxygen pressure of 350 mTorr. Following deposition, the vacuum chamber was backfilled to an oxygen pressure of 600 Torr, and the substrate temperature was decreased to room temperature at a rate of 30° C./min. This fabrication procedure is standard. Similar deposition procedures by pulsed laser deposition are well-known to those skilled in the art. The YBCO thin films may be deposited by any technique, however, and the surface treatment discussed here does not depend on the thin film deposition method.

[**0086**] The second YBCO thin film was deposited in a manner identical to that outlined above, except that immediately following deposition, the surface treatment procedure of Applicant's invention was employed. Following growth of the YBCO film, the deposition chamber was backfilled to 600 Torr of oxygen and the substrate temperature was reduced to 450° C. The chamber was then pumped to vacuum (<10<sup>-5</sup> Torr) and held at this temperature and

pressure for 30 minutes. The substrate temperature was then decreased to 400° C. Argon gas was introduced to a pressure of 20 mTorr, and a plasma was generated by biasing the heater with an RF source. The forward power of the RF source varied from 300 to 342 W, the reflected power varied 8 to 9 W, and the DC self-bias was fixed at -900 V. This plasma treatment was performed for 10 minutes. The RF source was then turned off, the deposition chamber was pumped to vacuum, and the sample was annealed at 400° C. for 31 minutes. Oxygen was then introduced into the chamber to a pressure of 350 mTorr, and the substrate was heated to 785° C. at 30° C./min, and was held at this temperature for 10 minutes. The oxygen pressure was then increased to 600 Torr, and the substrate temperature was decreased to room temperature at a rate of 30° C./minute.

[**0087**] Both films were then stored in a desiccator. As shown in **FIG. 12**, without the surface treatment of the invention, after four months, the Ba 4*d* XPS (**510**) of the film surface contains only two peaks **520** and **530** of higher binding energies; the lower energy peak (peak **112** in **FIG. 8**) has disappeared, indicating that the superconducting YBCO phase had deteriorated, at least near the surface.

[**0088**] In contrast, as shown in **FIG. 13**, with the surface treatment according to the invention, the XPS (**610**) taken at substantially the same time as that shown in **FIG. 12** still includes all three peaks **620**, **630** and **640**, indicating that the superconducting YBCO has been preserved. Thus, the plasma-modified surface phase of the YBCO superconductor film has been shown to be stable over time, structurally robust and substantially impervious to oxygen migration.

### Example 2

[**0089**] The photoemission spectra of the surface of an YBCO film treated with plasma were compared with those of an YBa<sub>2</sub>Cu<sub>3</sub>O<sub>6</sub> single crystal.

[**0090**] The plasma treated YBCO film was prepared as follows. A CeO<sub>2</sub> buffer layer was deposited onto a (**100**) LaAlO<sub>3</sub> single-crystal substrate by pulsed laser ablation to a thickness of approximately 200 nm. The substrate temperature was 785° C., and the background oxygen pressure was 100 mTorr. The excimer laser conditions were identical to those mentioned previously. The YBCO thin film was deposited immediately thereafter at a substrate temperature of 785° C., oxygen pressure of 350 mTorr, and to a thickness of approximately 200 nm. Following deposition, the deposition vacuum chamber was backfilled with O<sub>2</sub> to a pressure of 600 Torr, and the substrate temperature was decreased to 450° C. at a rate of 30° C./min. The chamber was then pumped to a vacuum pressure of 9×10<sup>-7</sup> Torr and held at this pressure and substrate temperature of 450° C. for 30 minutes. The substrate temperature was then decreased to 400° C., and Ar gas was subsequently introduced into the chamber to a pressure of 20 mTorr. A plasma was struck and the YBCO surface was treated for 10 minutes. The forward power of the RF source used to generate the Ar plasma was 302 W at the beginning of this period, and increased to 350 W by the end of the 10 minute treatment time. The reflected power varied from 7 to 8 W, and the DC bias on the heater was fixed at -900 V. Following the plasma treatment, the chamber was pumped to a vacuum pressure of 5×10<sup>-7</sup> Torr, and the sample was held at this pressure and a temperature of 400° C. for 31 minutes. O<sub>2</sub> gas was subsequently intro-

duced into the system to a pressure of 350 mTorr, and the substrate temperature was increased to 785° C. at a rate of 30° C./min. The sample was held at this pressure and temperature for 8 minutes. The chamber was then backfilled with O<sub>2</sub> gas to a pressure of 600 Torr, and the substrate temperature was decreased to room temperature at a rate of 30° C./min.

[0091] Plot (a) in **FIG. 14** shows a spectrum from the plasma-treated YBCO film for energies around -2 eV relative to the Fermi energy, E<sub>F</sub>. The spectrum exhibits a kink **710** near -2.2 eV. This kink feature is similarly shown in the spectrum from the YBa<sub>2</sub>Cu<sub>3</sub>O<sub>6</sub> single crystal, as illustrated in plot (b), which also exhibits a kink **720** at about -2.2 eV. This feature is not present in untreated YBCO films, whether the films were annealed in oxygen (ozone) or vacuum.

[0092] Because YBa<sub>2</sub>Cu<sub>3</sub>O<sub>6</sub> is an insulator, the similarities in the photoemission spectra in **FIG. 14** suggests that the plasma-treated YBCO superconductor surface according to the invention also has insulating properties.

[0093] The device and process disclosed above are particularly applicable to oxide superconductors such as YBCO in which oxygen migration is significant and detrimental. However, the device and process can also be used for other superconductors to produce passivated surfaces to prevent or reduce atomic migration or corrosion.

[0094] While the foregoing disclosure contains many specificities, it should be understood that these are given by way of example only. The scope of the invention should not be limited by the specific examples given above, but only by the appended claims and their legal equivalents.

What is claimed is:

1. An electronic device comprising:
  - (a) a crystalline substrate;
  - (b) an electrode formed on and epitaxial to the substrate, the electrode comprising a first superconductive oxide;
  - (c) an insulator formed on and epitaxial to the electrode;
  - (d) a barrier comprising an ion-treated surface of the first superconductive oxide; and
  - (e) a counter-electrode formed on and epitaxial to the electrode and the barrier, the counter-electrode comprising a second superconductive oxide, whereby a Josephson junction is formed between the electrode and the counter-electrode.
2. The device of claim 1, wherein the barrier is a surface formed by treating the first superconductive oxide with a plasma comprising a gas selected from the group consisting of argon, xenon, oxygen, and halogen.
3. The device of claim 2, wherein the gas is argon gas.
4. The device of claim 2, wherein the gas is a 1:1 mixture of argon and oxygen.
5. The device of claim 1 wherein the first superconductive oxide has an a-b plane and a step-edge junction is formed in the a-b plane of the first superconductive oxide.
6. The device of claim 1 wherein the first superconductive oxide has an a-b plane, the a-b plane is epitaxial to the substrate, and the second superconductive oxide is on and epitaxial to the first superconductive element, whereby a junction is formed perpendicular to the a-b plane of the first superconductive oxide.

7. The device of any one of claims 1-6, wherein the first and second superconductive oxide is YBCO.

8. The device of claim 1, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.3 mV at a temperature of 4.2 K.

9. The device of claim 2, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.3 mV at a temperature of 4.2 K.

10. The device of claim 3, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.3 mV at a temperature of 4.2 K.

11. The device of claim 4, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.3 mV at a temperature of 4.2 K.

12. The device of claim 5, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.3 mV at a temperature of 4.2 K.

13. The device of claim 6, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.3 mV at a temperature of 4.2 K.

14. The device of claim 7, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.3 mV at a temperature of 4.2 K.

15. The device of claim 1, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.5 mV at a temperature of 40 K.

16. The device of claim 2, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.5 mV at a temperature of 40 K.

17. The device of claim 3, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.5 mV at a temperature of 40 K.

18. The device of claim 4, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.5 mV at a temperature of 40 K.

19. The device of claim 5, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.5 mV at a temperature of 40 K.

20. The device of claim 6, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.5 mV at a temperature of 40 K.

21. The device of claim 7, the device having an I<sub>c</sub>R<sub>n</sub> value of at least about 0.5 mV at a temperature of 40 K.

22. A process for making a Josephson junction device comprising the steps of:

- (a) preparing a substrate;
- (b) depositing an electrode comprising a first layer of a superconductive oxide on the substrate;
- (c) depositing an insulating layer on the first layer of superconductive oxide;
- (d) patterning to form a pre-device having an exposed surface of the first superconductive oxide;
- (e) placing the pre-device into a deposition chamber;
- (f) forming a barrier on the exposed surface of the first layer of superconductive oxide by treating the exposed surface with ions; and
- (g) depositing a second layer of a superconductive oxide on the pre-device, whereby a Josephson junction is formed between the first and the second superconductive oxides at the barrier.

23. The process of claim 22, wherein the treating with ions is accomplished with a plasma of Ar gas at a pressure of between 10 and 100 mTorr.

24. The process of claim 22, wherein the treating with ions is with a mixture of Ar and O<sub>2</sub> gas at a pressure of between 10 and 100 mTorr.

25. The process of any one of claims 22-24, further comprising the step of vacuum annealing the pre-device prior to depositing the second superconductive oxide.

26. A superconductor device, comprising:

- a) an oxide superconductor having a surface exposed to ambient environment; and



- b) a passivation layer covering at least a portion of the surface of the oxide superconductor that is exposed to the ambient environment.
- 27.** The device claim 26, further comprising a buffer layer at least partially between the passivation layer and the oxide superconductor.
- 28.** The device of claim 26, wherein the passivation layer originates from the superconductor.
- 29.** The device of claim 28, wherein the passivation layer is an ion-modified layer of the superconductor.
- 30.** The device of claim 26, wherein the oxide superconductor comprises  $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ , wherein  $\delta \geq 0$ .
- 31.** The device of claim 26, wherein the passivation layer is an electrical insulator.
- 32.** The device of claim 26, wherein the passivation layer is epitaxial and crystalline.
- 33.** The device of claim 26, wherein the passivation layer covers the entire surface of the oxide superconductor that is exposed to the ambient environment.
- 34.** The device of claim 26, further comprising a layer of a superconductive oxide on the passivation layer, whereby a Josephson junction is formed between the superconductive oxides.
- 35.** A method of providing a passivation layer on the surface of an oxide superconductor, the method comprising vacuum annealing and ion treating at least a portion of the surface of the oxide superconductor that is exposed to ambient environment.
- 36.** The method of claim 35, further comprising additional vacuum annealing after the ion treatment.
- 37.** The method of claim 35, further comprising heating in an oxygen-rich environment after the ion treatment.
- 38.** The method of claim 35, comprising vacuum annealing and ion treating the entire surface of the oxide superconductor that is exposed to ambient environment.
- 39.** A method of making a superconductor device, the method comprising:
- a) forming a layer of oxide superconductor on a substrate, the layer of oxide superconductor having a surface that is exposed to ambient environment; and
  - b) passivating at least a portion of the surface of the oxide superconductor that is exposed to ambient environment.
- 40.** The method of claim 39, comprising passivating the entire exposed surface of the oxide superconductor.
- 41.** The method of claim 39, wherein the passivating step comprises bombarding the exposed surface portion with ions.
- 42.** The method of claim 41, further comprising annealing the layer of oxide superconductor between steps (a) and (b).
- 43.** The method of claim 42, further comprising annealing the layer of oxide superconductor after step (b).
- 44.** The method of claim 42, wherein the bombarding step comprises treating the exposed surface portion with plasma.
- 45.** The method of claim 39, wherein step (a) comprises forming a layer of  $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ , wherein  $\delta \geq 0$ .
- 46.** The method of claim 42, further comprising heating the oxide superconductor in oxygen after step (b).
- 47.** The method of claim 46, further comprising cooling the oxide superconductor to room temperature in oxygen after heating the oxide superconductor in oxygen.
- 48.** The method of claim 41, further comprising maintaining the layer of oxide superconductor at a temperature of between about  $300^\circ\text{C}$ . and about  $650^\circ\text{C}$ . while bombarding the exposed surface portion with ions.
- 49.** The method of claim 46, wherein the heating step comprises maintaining the layer of oxide superconductor at a temperature of between about  $700^\circ\text{C}$ . and about  $800^\circ\text{C}$ . after treating the exposed surface portion with plasma.
- 50.** The method of claim 39, wherein the passivation step comprises changing a surface layer of the oxide superconductor to a material different from the oxide superconductor.
- 51.** The method of claim 50, wherein the changing step comprises changing the surface layer of the oxide superconductor to a material having an oxygen mobility that is lower than the oxygen mobility in the oxide superconductor.
- 52.** The method of claim 39, further comprising forming a layer of oxide superconductor on at least a portion of the passivated surface portion, whereby a Josephson junction is formed between the oxide superconductors.
- 53.** A passivation layer comprising an ion-modified layer on an oxide superconductor, the ion-modified layer covering at least a portion of the surface of the oxide superconductor that would otherwise be exposed to ambient environment, and the ion-modified layer having an oxygen mobility that is lower than an oxygen mobility of the oxide superconductor.
- 54.** The passivation layer of claim 53, wherein the ion-modified layer is formed by material originating from the oxide superconductor.
- 55.** The passivation layer of claim 53, wherein the ion-modified layer is an externally applied layer that is bonded to the oxide superconductor.
- 56.** The passivation layer of claim 55, wherein the ion-modified layer is quasi-cubic and is not  $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ , wherein  $\delta \geq 0$ .
- 57.** The passivation layer of claim 53, wherein the ion-modified layer is epitaxial and crystalline.
- 58.** The passivation layer of claim 53, the ion-modified layer covering the entire surface of the oxide superconductor that would otherwise be exposed to ambient environment

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