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**Ono et al.**

# (54) SEMICONDUCTOR DEVICE

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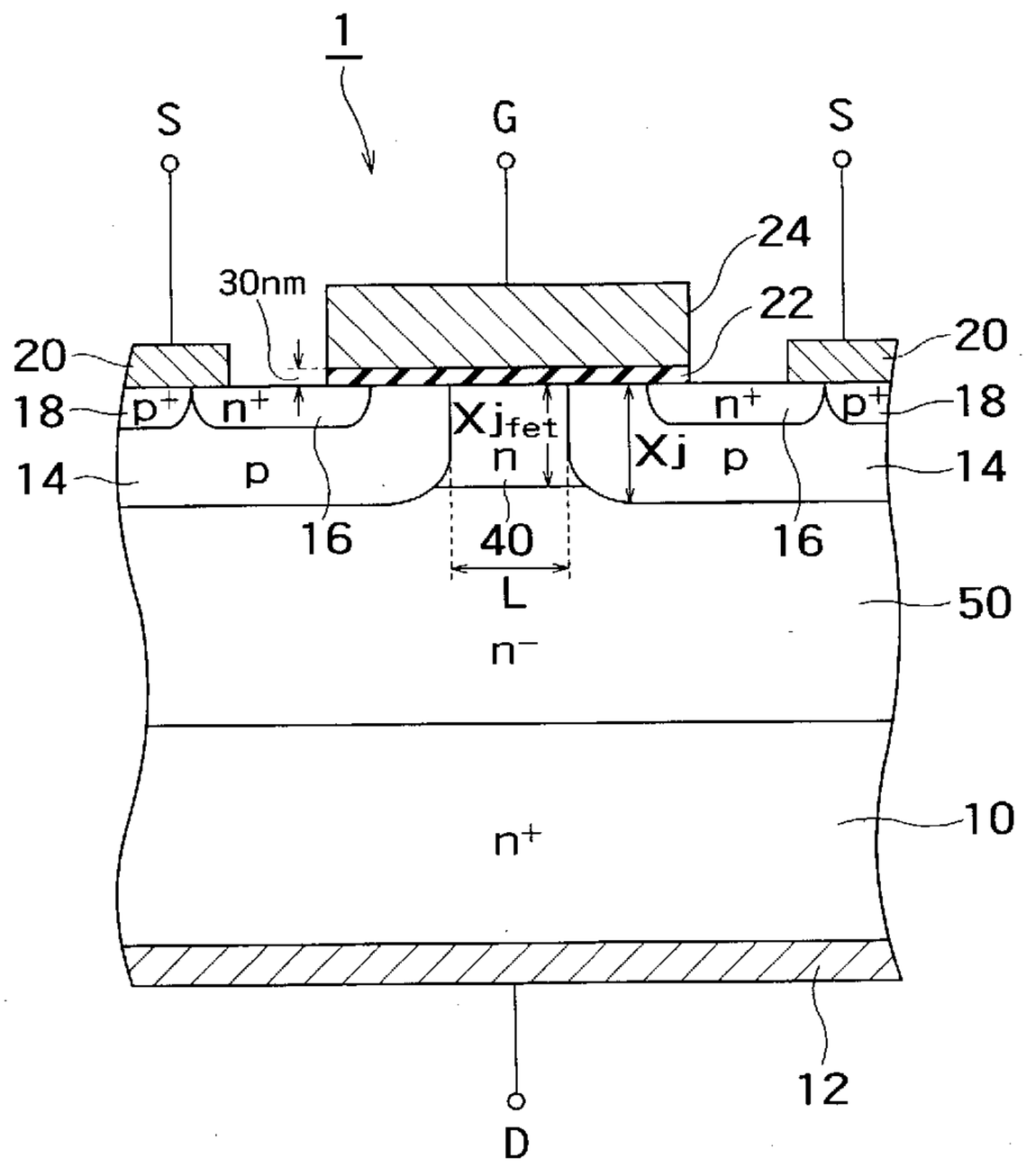
## (57) ABSTRACT

A semiconductor device includes: a semiconductor substrate, at least a surface portion thereof serving as a low-resistance drain layer of a first conductivity type; a first main electrode connected to the low-resistance drain layer; a high-resistance epitaxial layer of a second-conductivity type formed on the low-resistance drain layer; a second-conductivity type base layer selectively formed on the high-resistance epitaxial layer; a first-conductivity type source layer selectively formed in a surface portion of the second-conductivity type base layer; a trench formed in a region sandwiched by the second-conductivity type base layers with a depth extending from the surface of the high-resistance epitaxial layer to the semiconductor substrate; a jfet layer of the first conductivity type formed on side walls of the trench; an insulating layer formed in the trench; an LDD layer of the first-conductivity type formed in a surface portion of the second-conductivity type base layer so as to be connected to the first-conductivity type jfet layer around a top face of the trench; a control electrode formed above the semiconductor substrate so as to be divided into a plurality of parts, and formed on a gate insulating film formed on a part of the surface of the LDD layer, on surfaces of end parts of the first-conductivity type source layer facing each other across the trench, and on a region of the surface of the second-conductivity type base layer sandwiched by the LDD layer and the first-conductivity type source layer; and a second main electrode in ohmic contact with the first-conductivity type source layer and the second-conductivity type base layer so as to sandwich the control electrode.



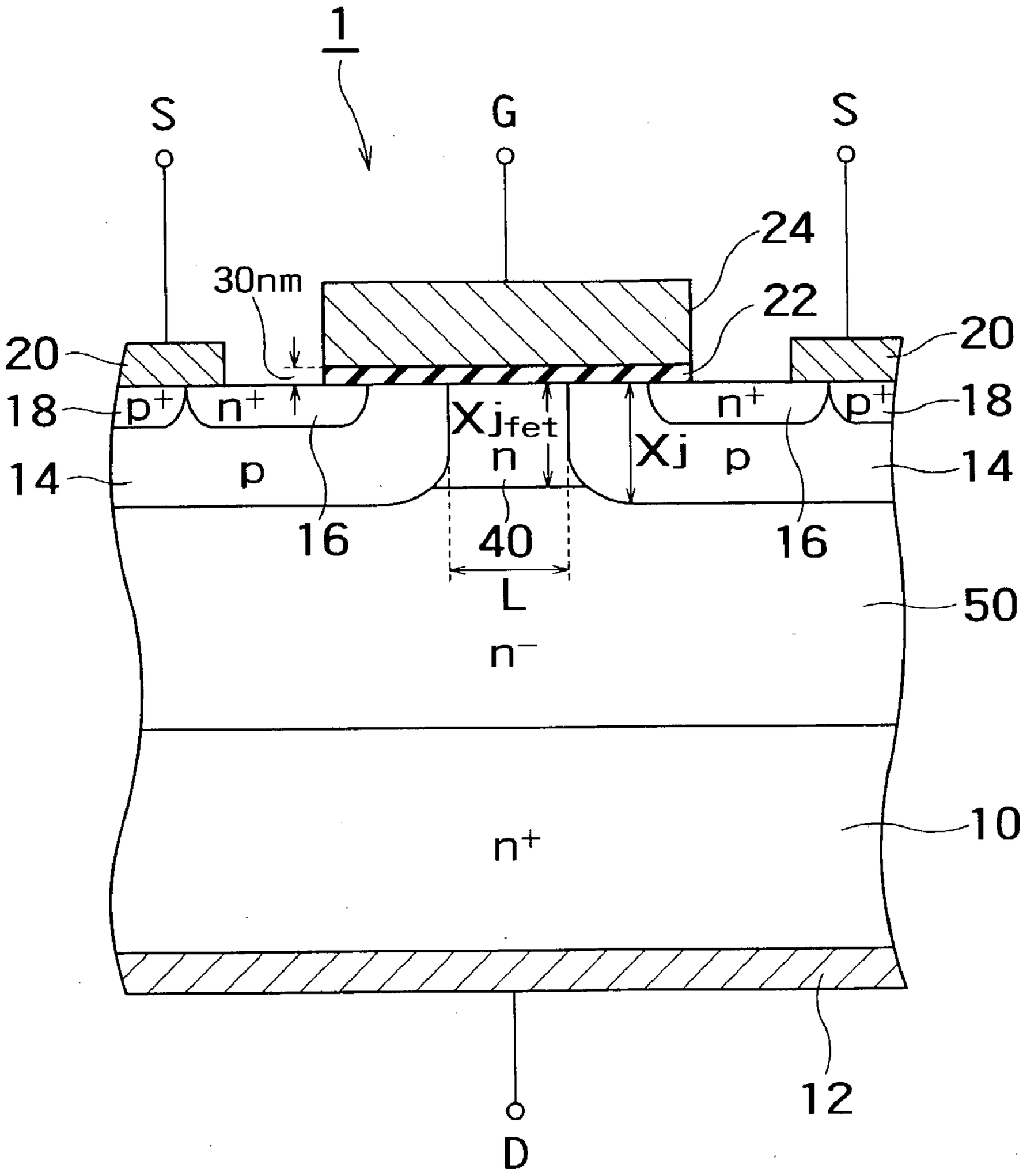

1
S
G
S
24
30nm
22
20
20
18
p+
n+
Xjfet
n+
p+
18
Xj
14
p
n
p
14
16
40
16
L
50
n−
10
n+
12
D

FIG. 1

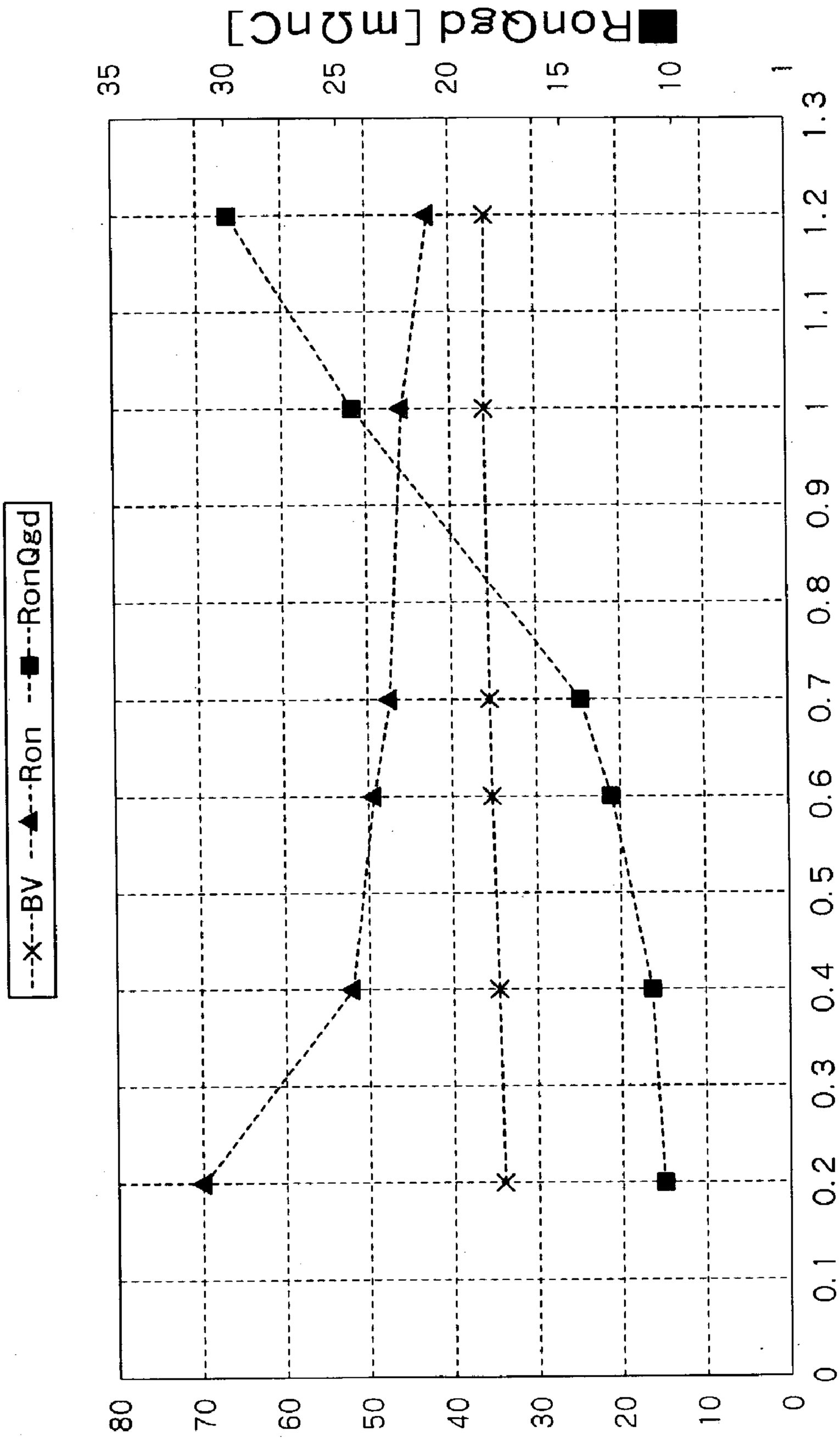

RonQgd [mΩnC]
35
30
25
20
15
10
1
1.3
1.2
1.1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
L [μm]
Xj=1 μm
BV
Ron
RonQgd
×BV [V], ▲Ron [mΩ]
80
70
60
50
40
30
20
10
0

FIG. 2

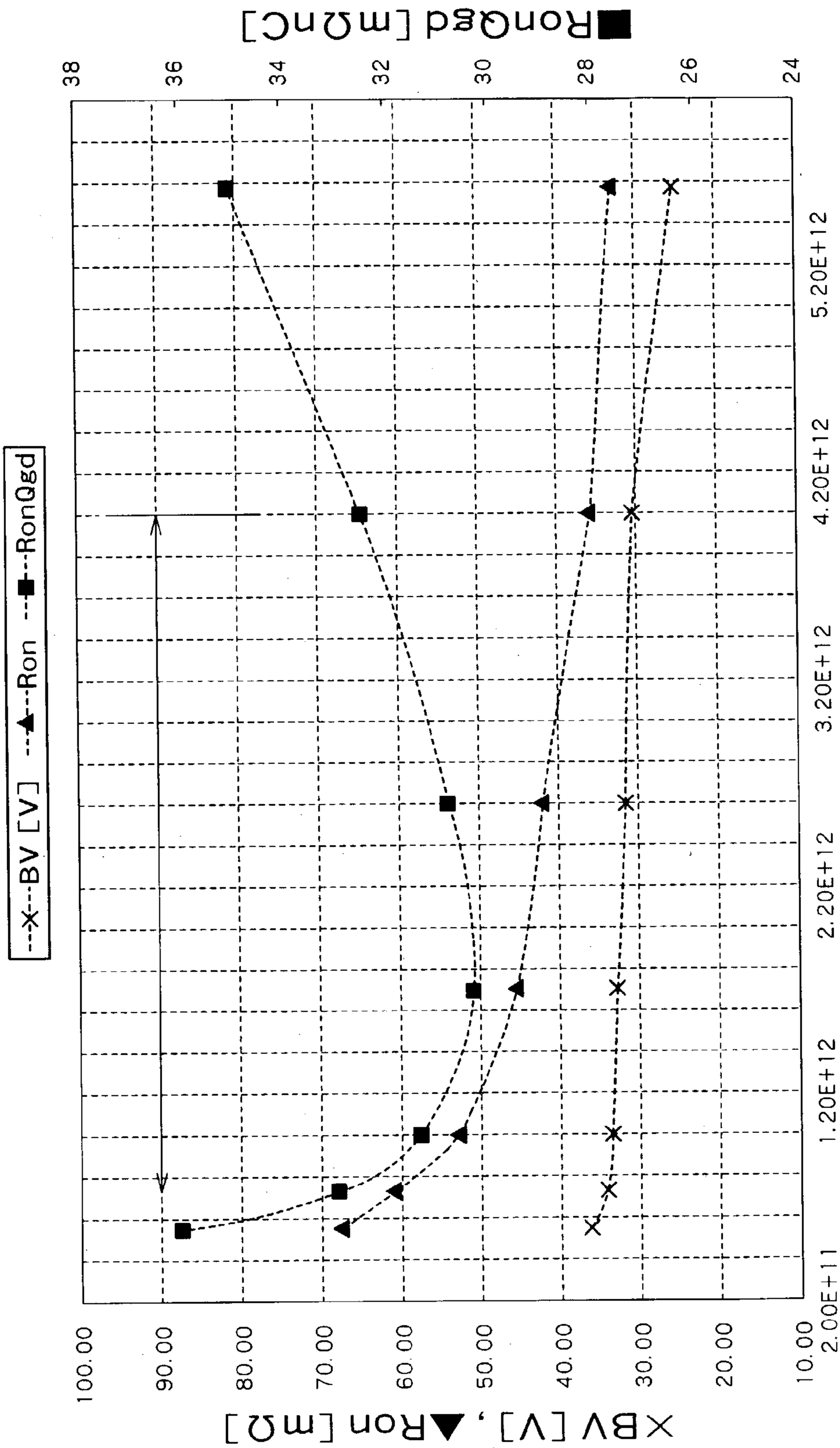

■RonQgd [mΩnC]
38
36
34
32
30
28
26
24
5.20E+12
4.20E+12
3.20E+12
2.20E+12
1.20E+12
OE+11
JFET REGION SURFACE DOSE AMOUNT
L=1.0μm
--▲--Ron --■--RonQgd
--×--BV [V]
100.00
90.00
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
2.0
×BV [V], ▲Ron [mΩ]

FIG. 3

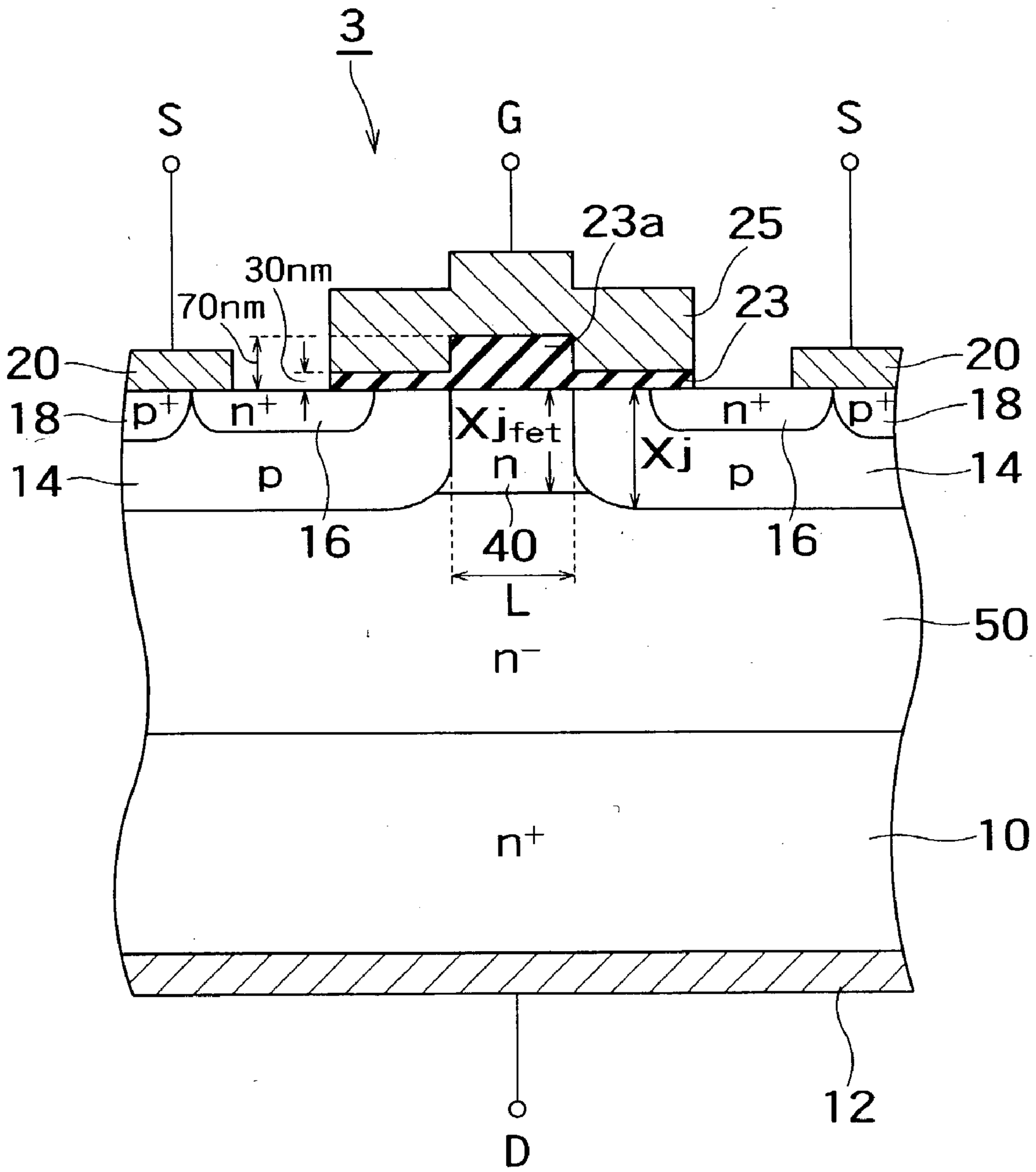

3
S
G
S
23a
25
30nm
70nm
23
20
20
18
p+
n+
Xjfet
Xj
n+
p+
18
14
p
n
p
14
16
40
16
L
50
n−
n+
10
12
D

FIG. 4

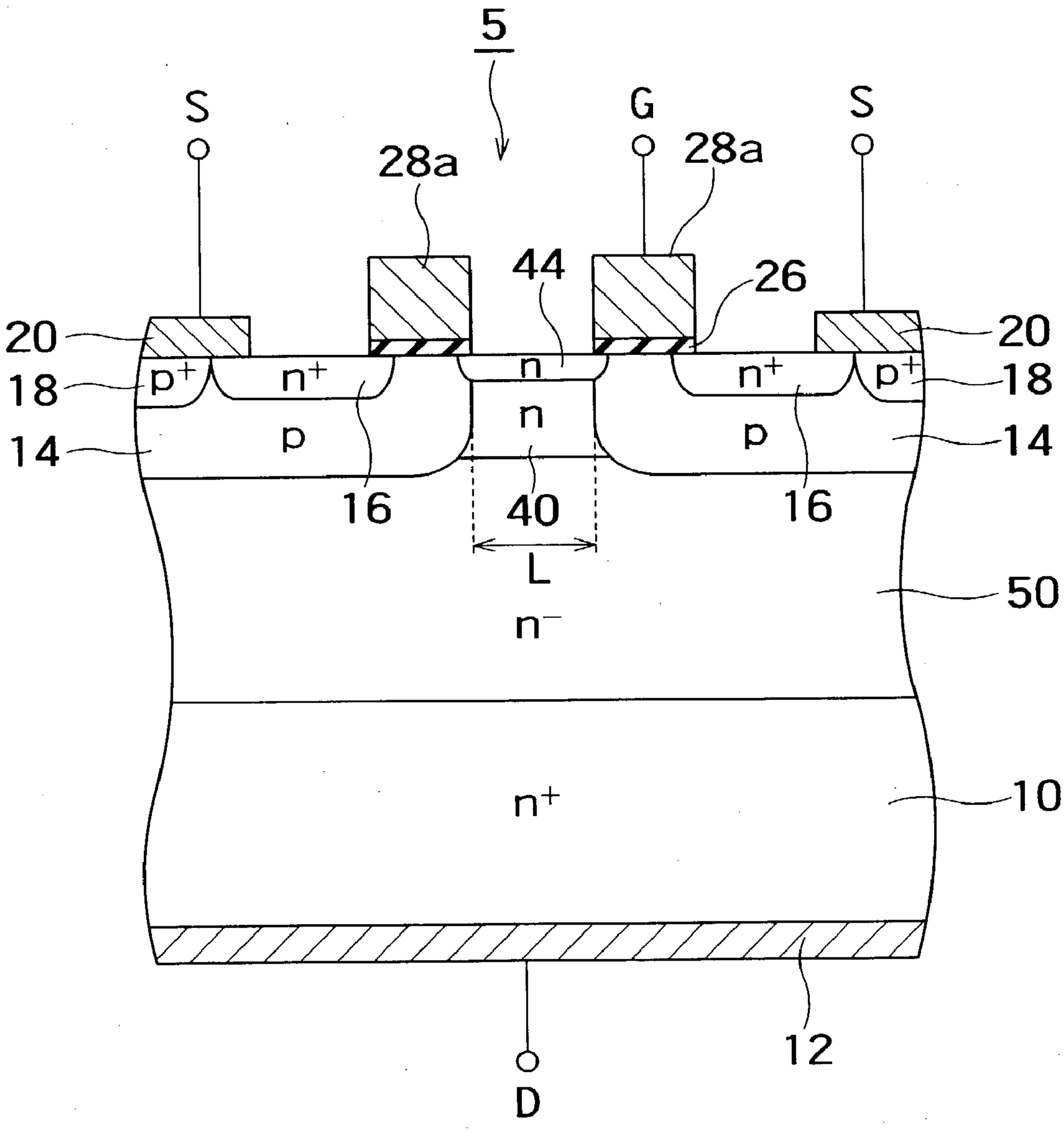

5
S
G
S
28a
28a
44
26
20
20
18
18
$p^+$
$n^+$
n
$n^+$
$p^+$
n
p
p
14
14
16
16
40
L
50
$n^-$
$n^+$
10
12
D

FIG. 5

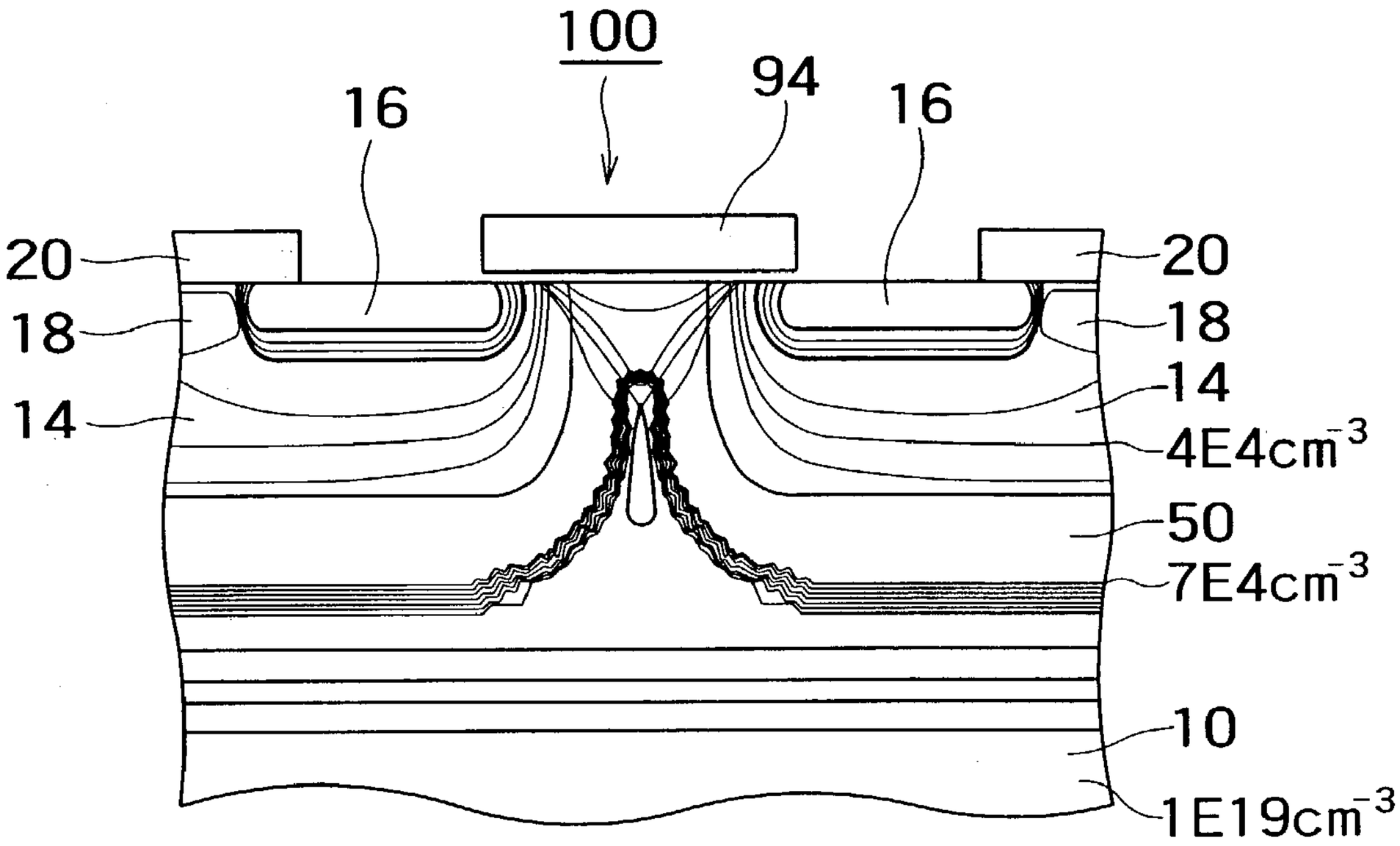

100
94
16
16
20
20
18
18
14
14
4E4cm-3
50
7E4cm-3
10
1E19cm-3

FIG. 6

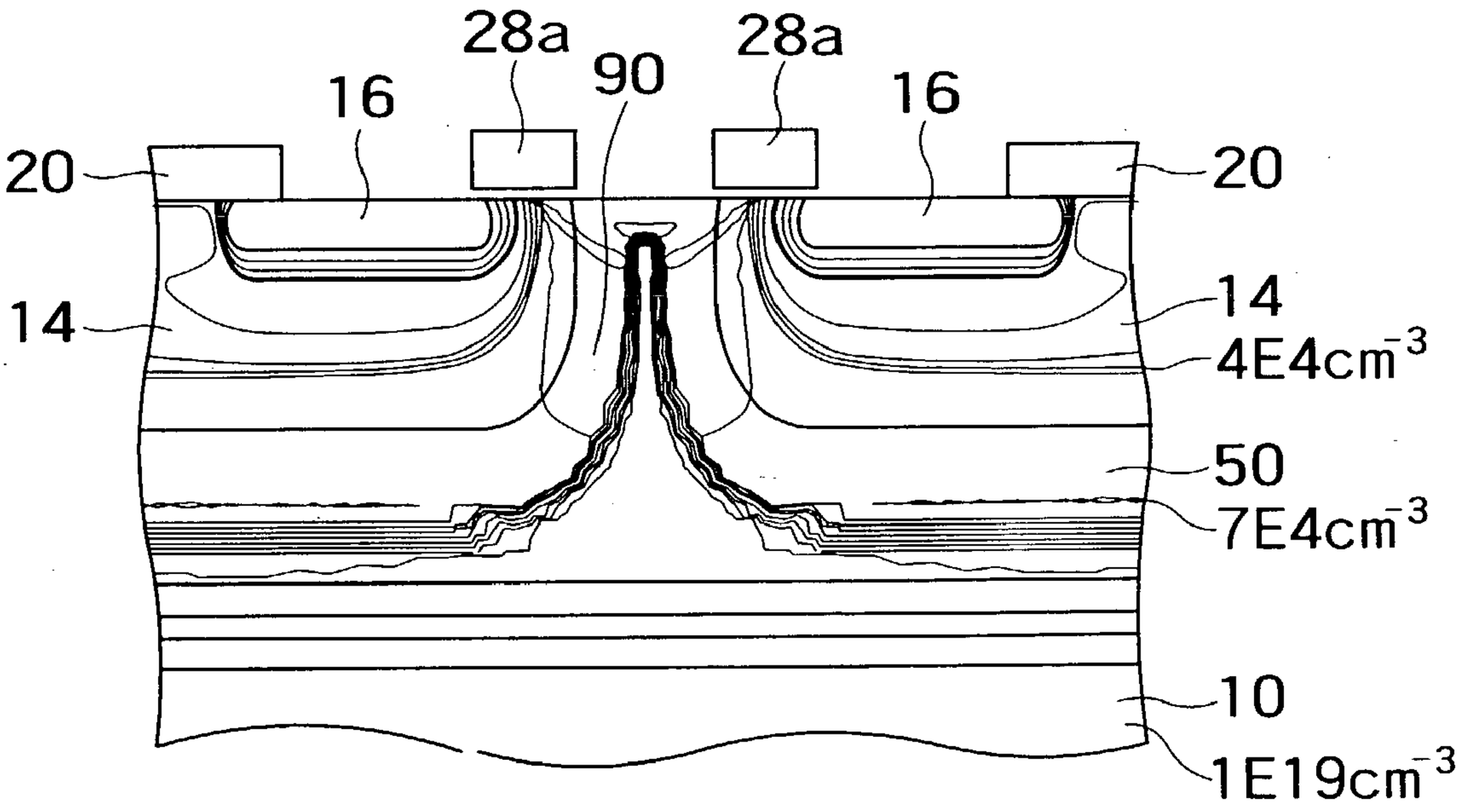

28a
28a
90
16
16
20
20
14
14
4E4cm-3
50
7E4cm-3
10
1E19cm-3

FIG. 7

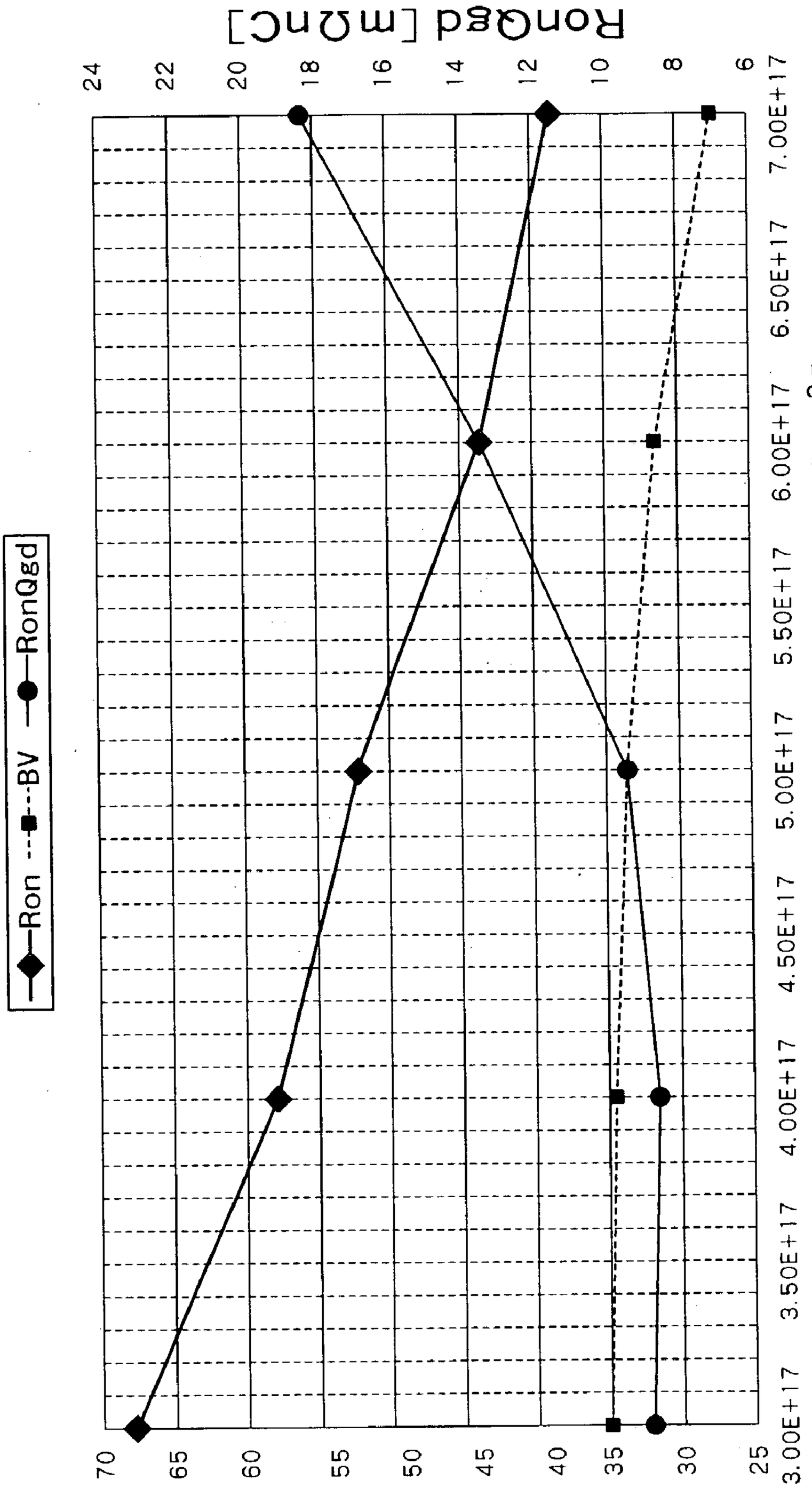

RonQgd [mΩnC]
24
22
20
18
16
14
12
10
8
6
7.00E+17
6.50E+17
6.00E+17
5.50E+17
5.00E+17
4.50E+17
4.00E+17
3.50E+17
3.00E+17
NJFET SURFACE CONCENTRATION [cm⁻³]
Xj=0.8μm
L=0.4μm
RonQgd
Ron
BV
70
65
60
55
50
45
40
35
30
25
BREAKDOWN VOLTAGE [V], Ron[mΩ]

FIG. 8

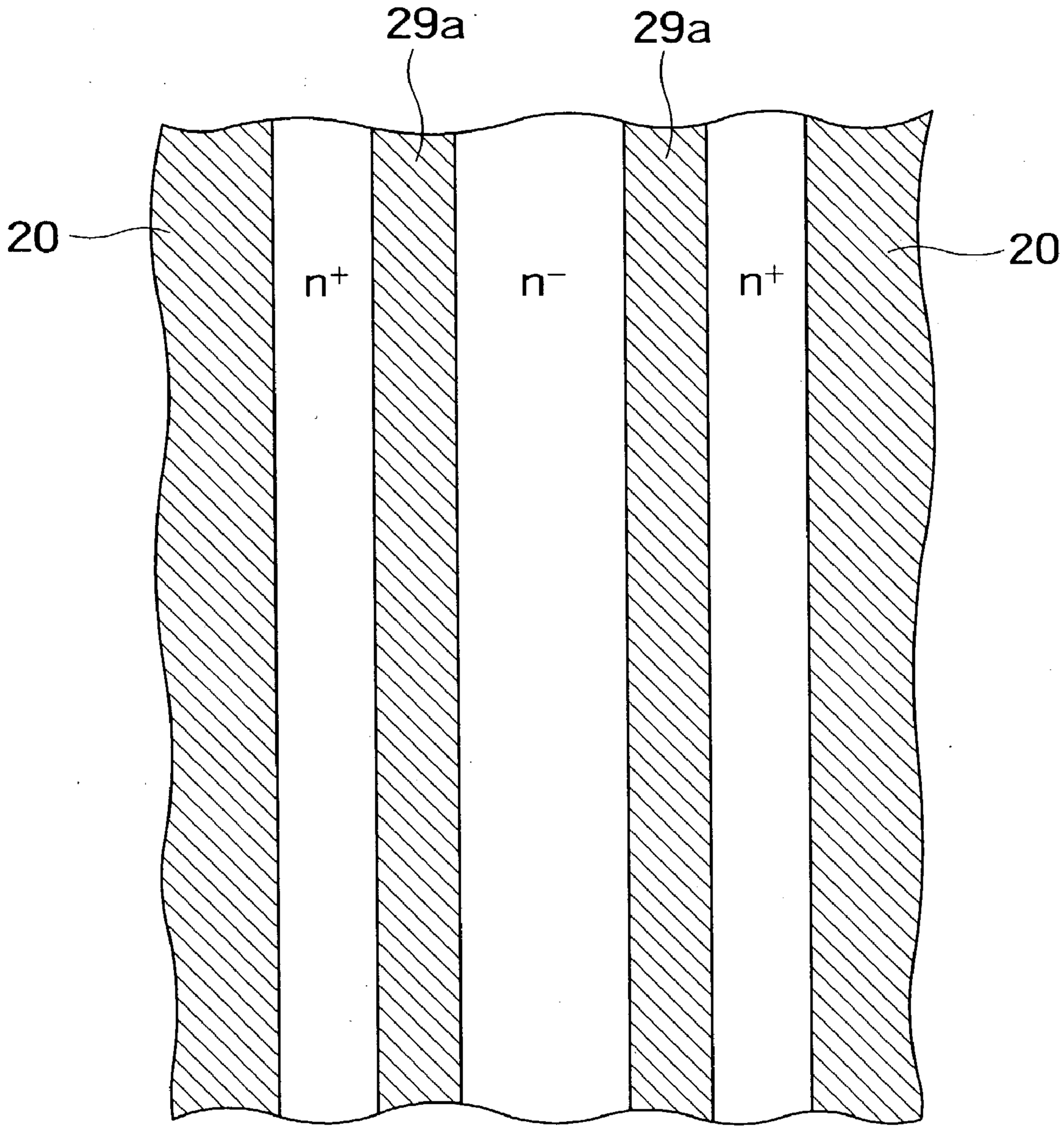



FIG. 9

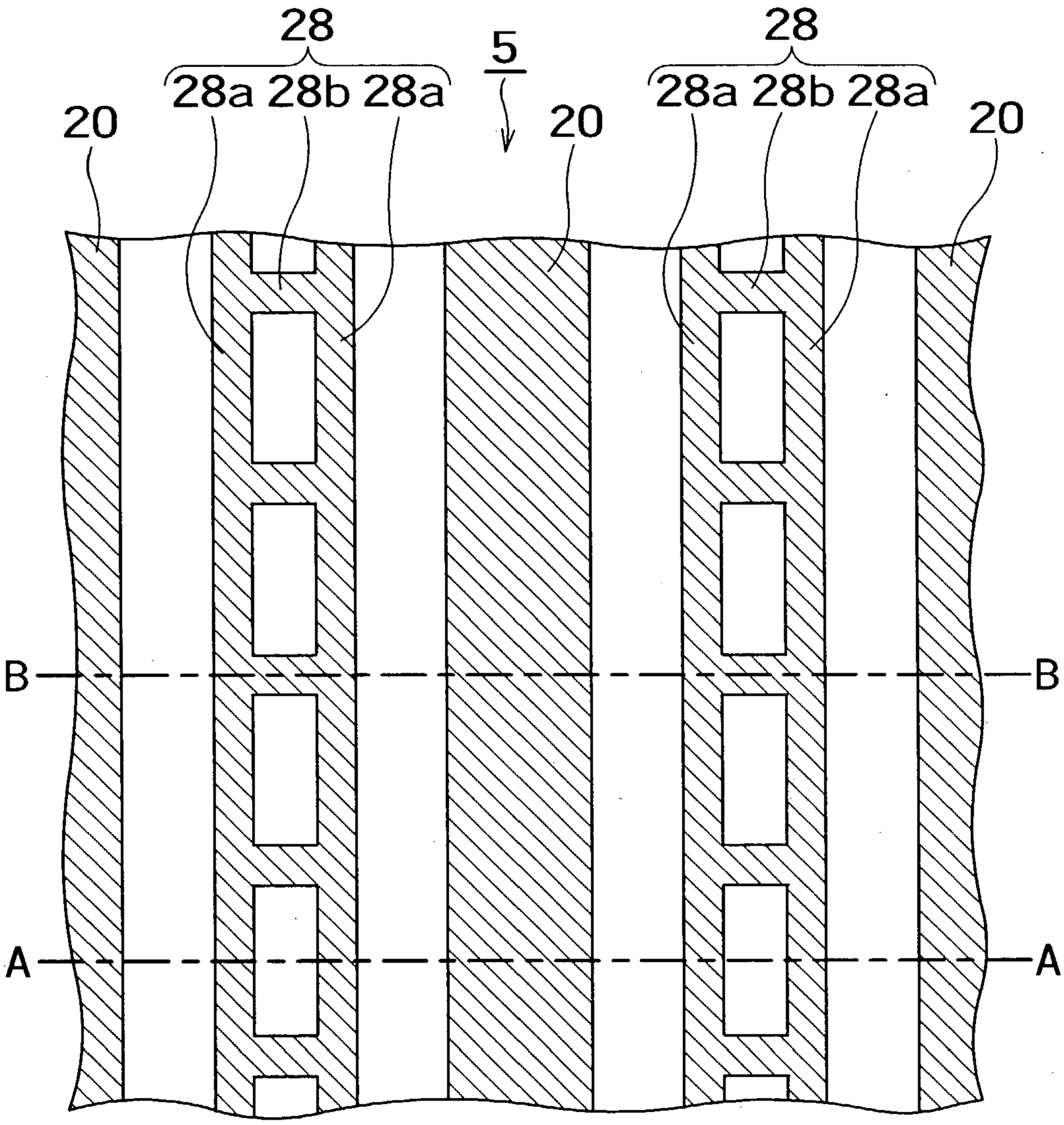



FIG. 10

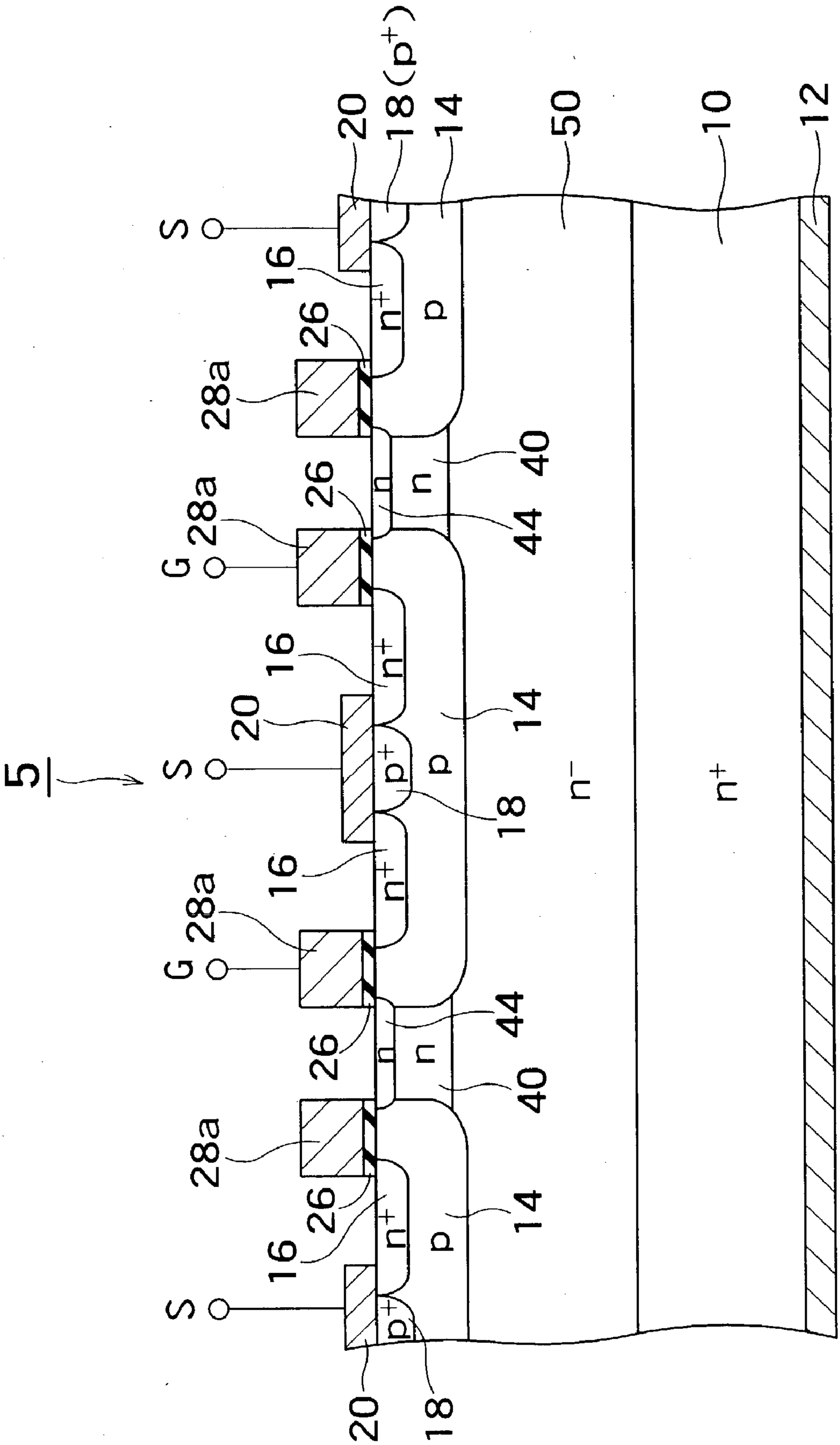



FIG. 11

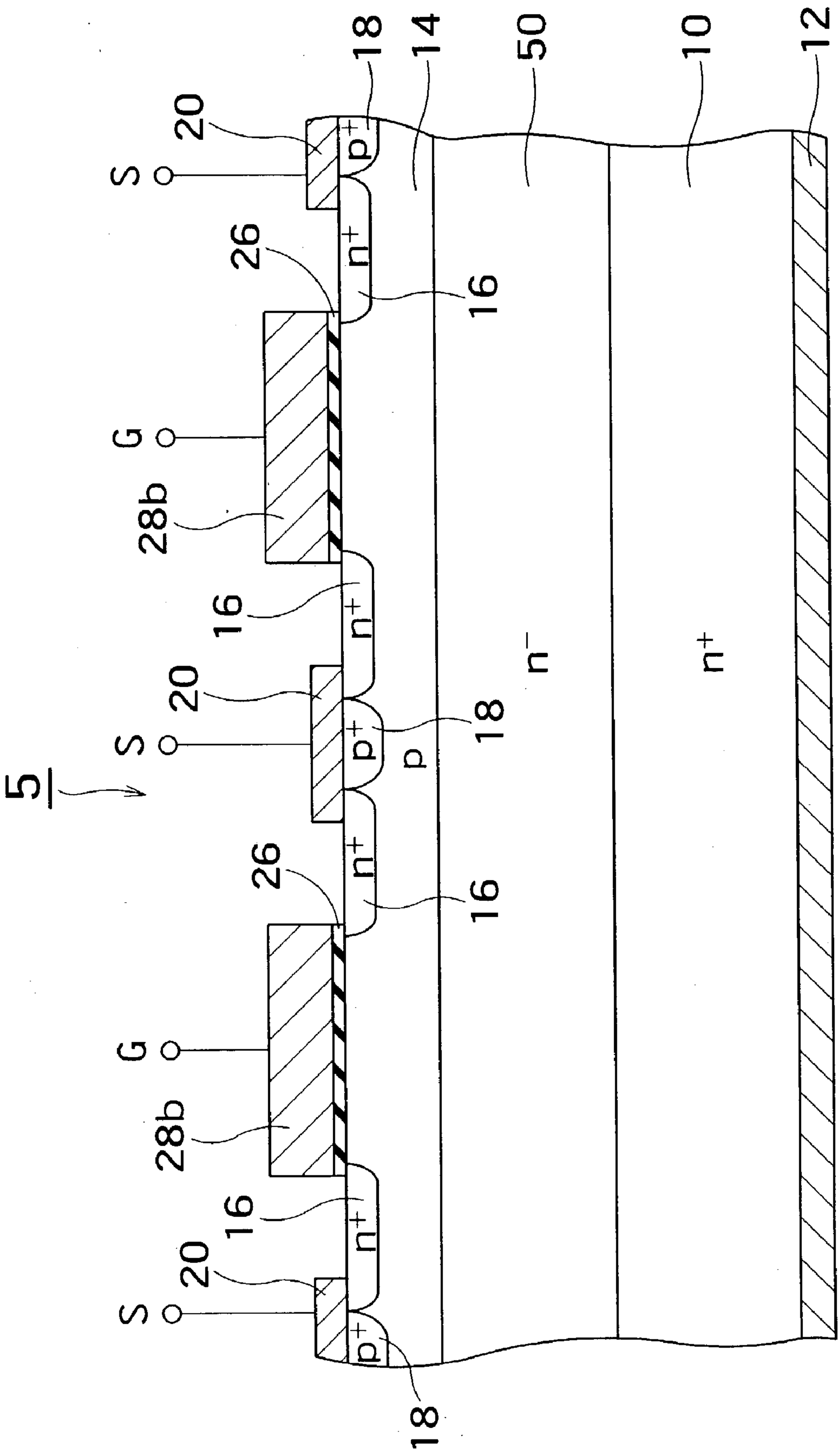

18
14
50
10
12
20
S
$p^+$
26
$n^+$
16
G
28b
16
$n^+$
20
S
$p^+$
18
p
$n^-$
$n^+$
5
26
$n^+$
16
G
28b
16
$n^+$
20
S
$p^+$
18

FIG. 1

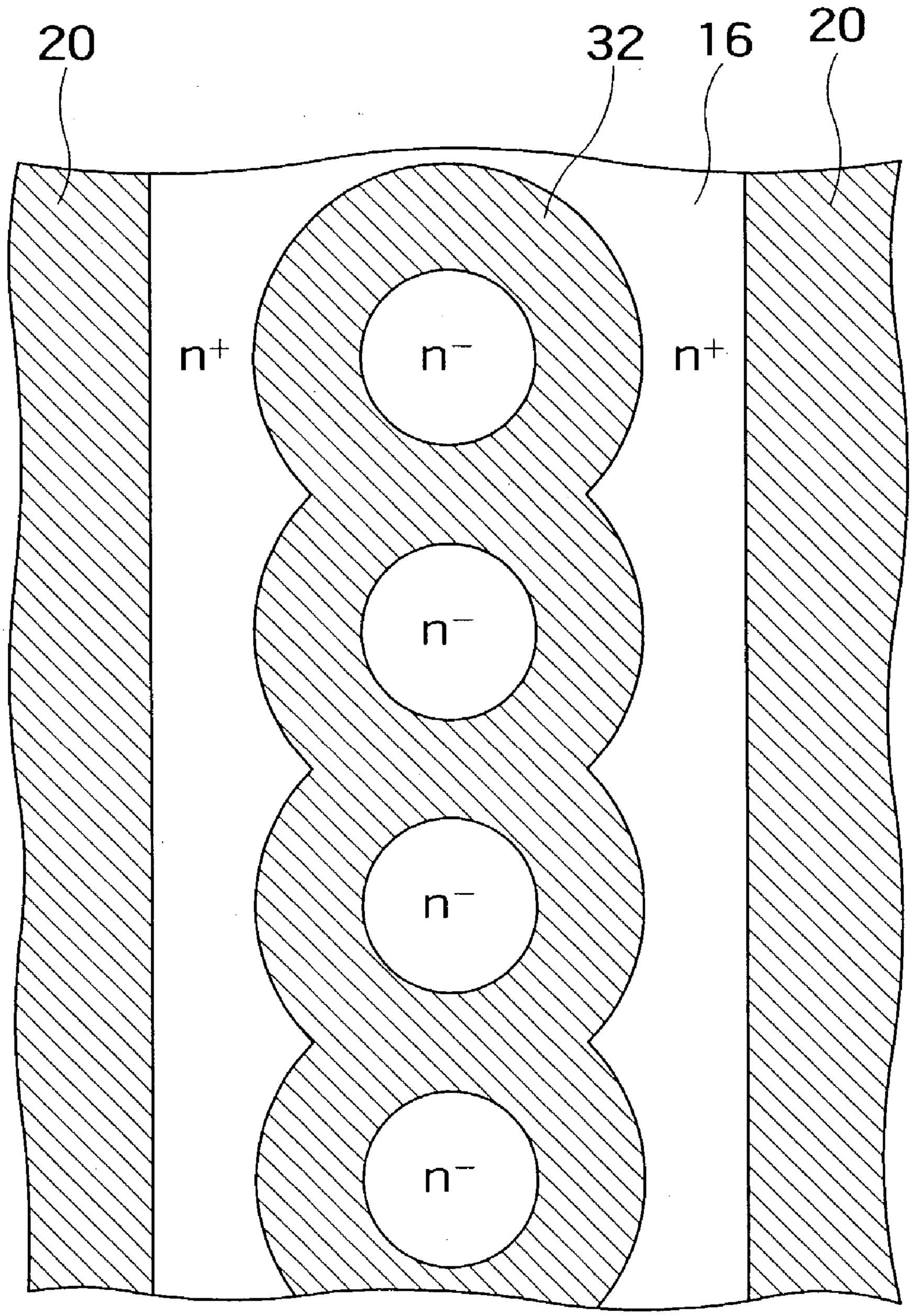



FIG. 13

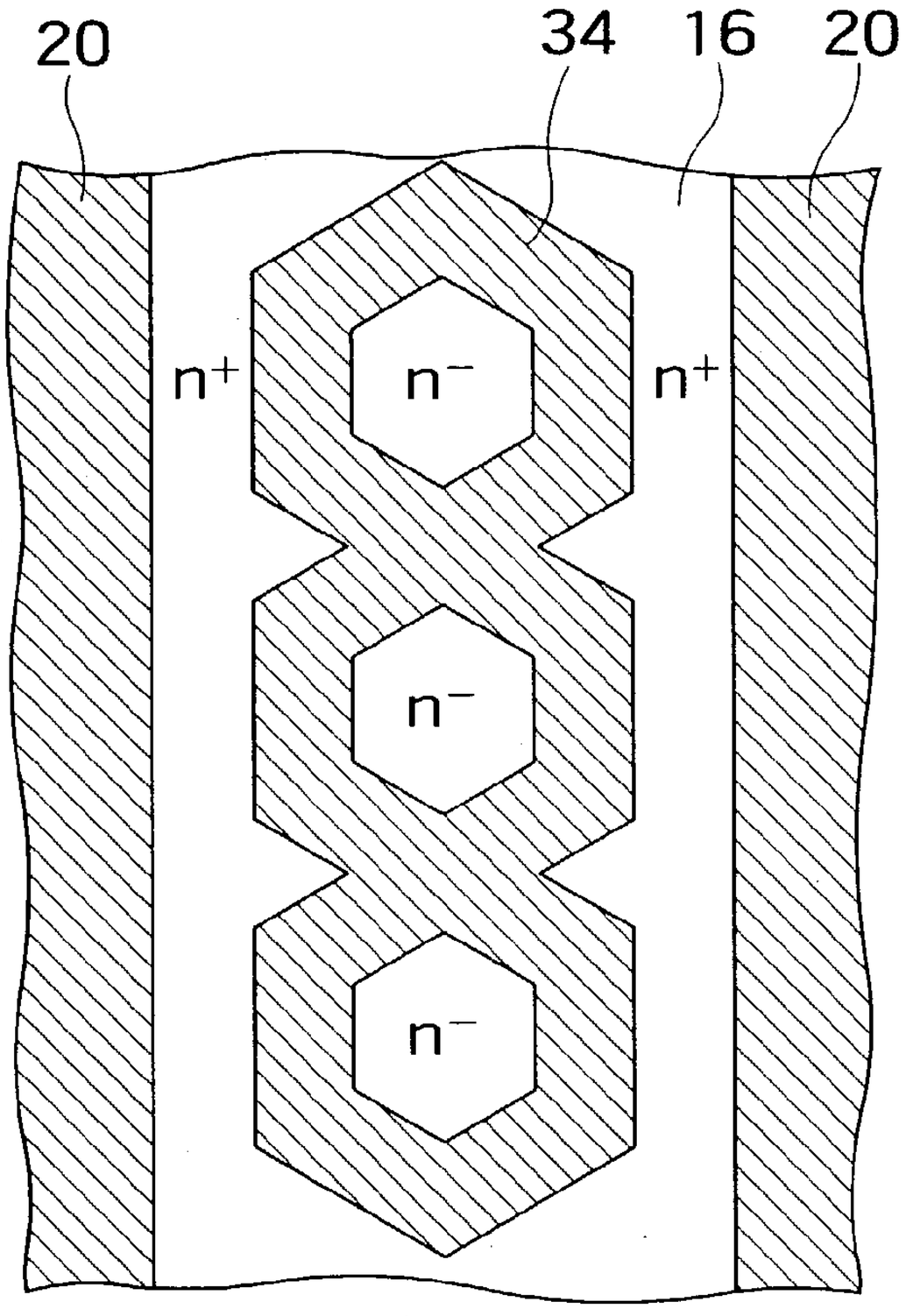

20
34
16
20
n+
n−
n+
n−
n−

FIG. 14

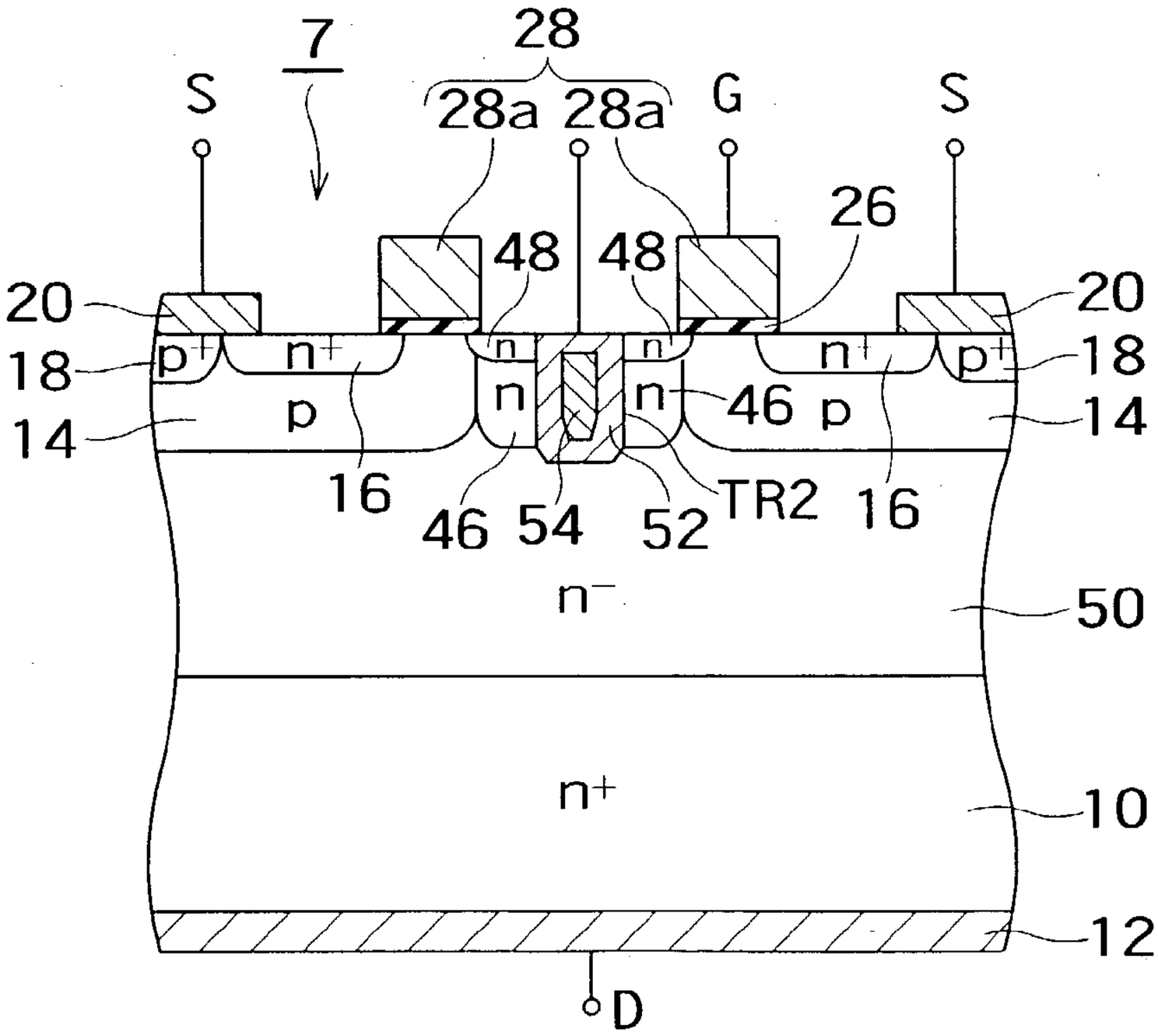

7
28
28a
28a
S
G
S
26
48
48
20
20
18
18
14
14
p+
n+
n
n
n+
p+
p
n
n
46
p
16
46
54
52
TR2
16
n−
50
n+
10
12
D

FIG. 16

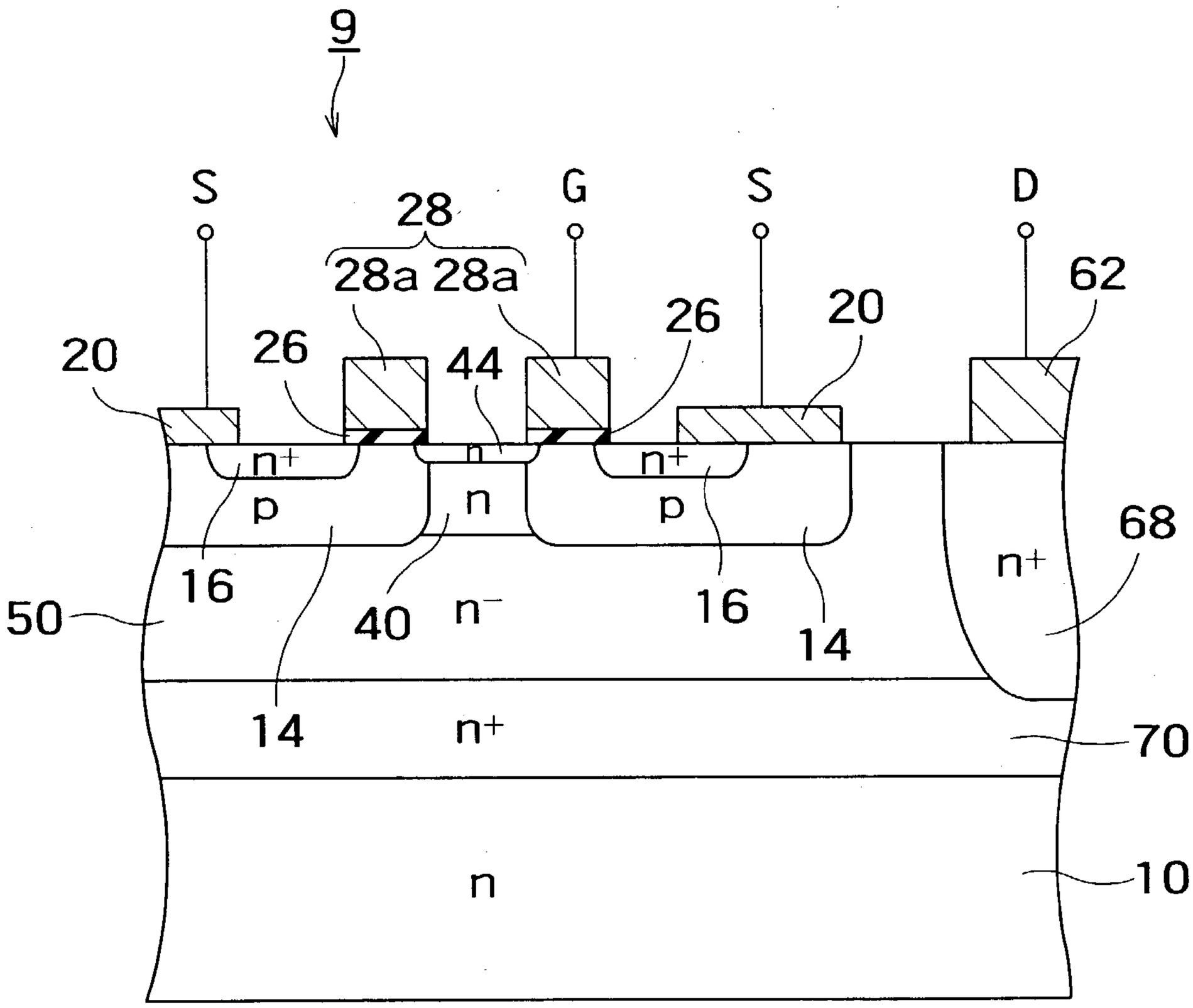

9
S
G
S
D
28
28a
28a
62
20
26
44
26
20
n+
n
n+
p
n
p
68
16
n+
50
40
n−
16
14
14
n+
70
n
10

FIG. 15

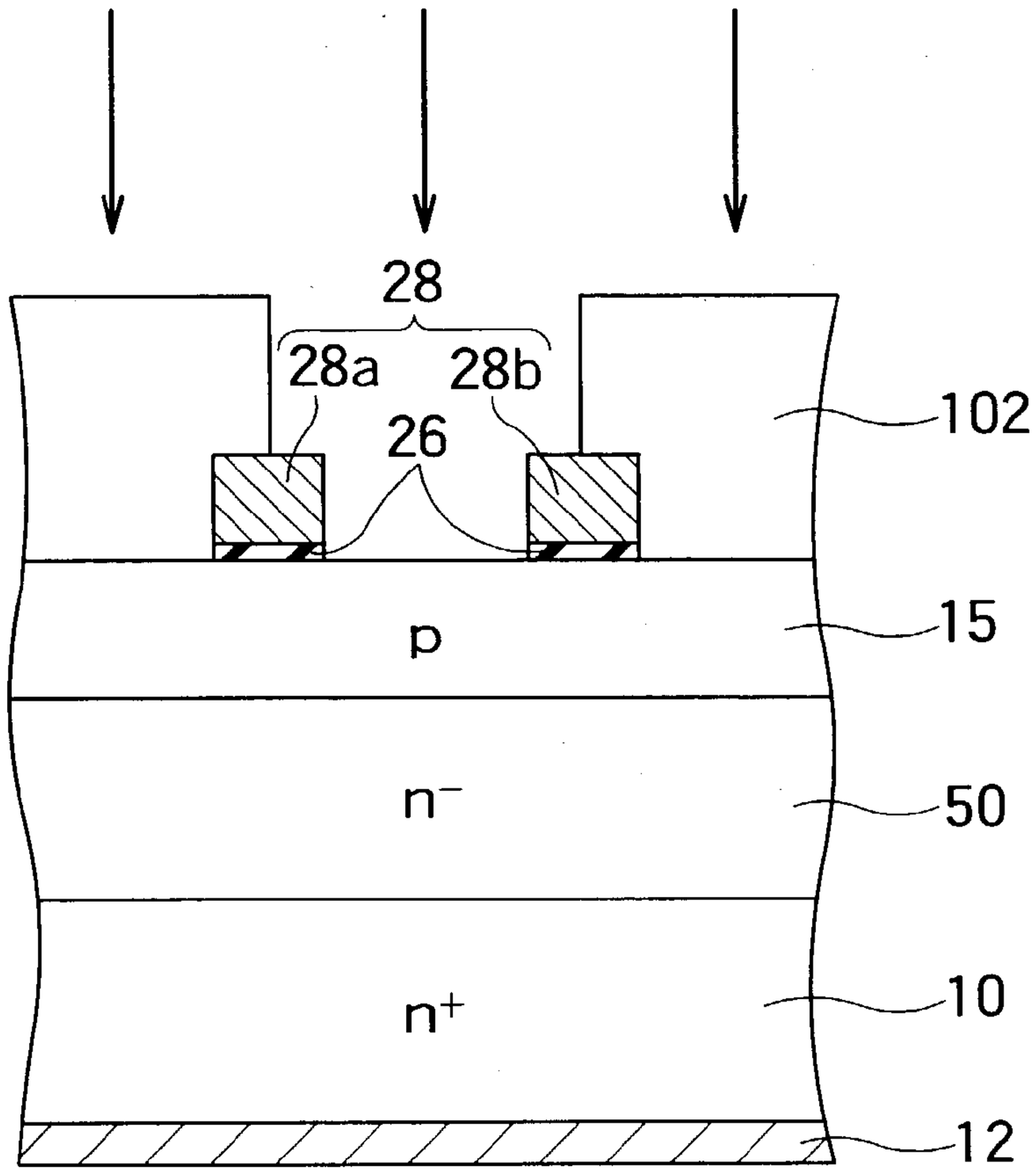

28
28a
28b
26
102
p
15
n⁻
50
n⁺
10
12

FIG. 17

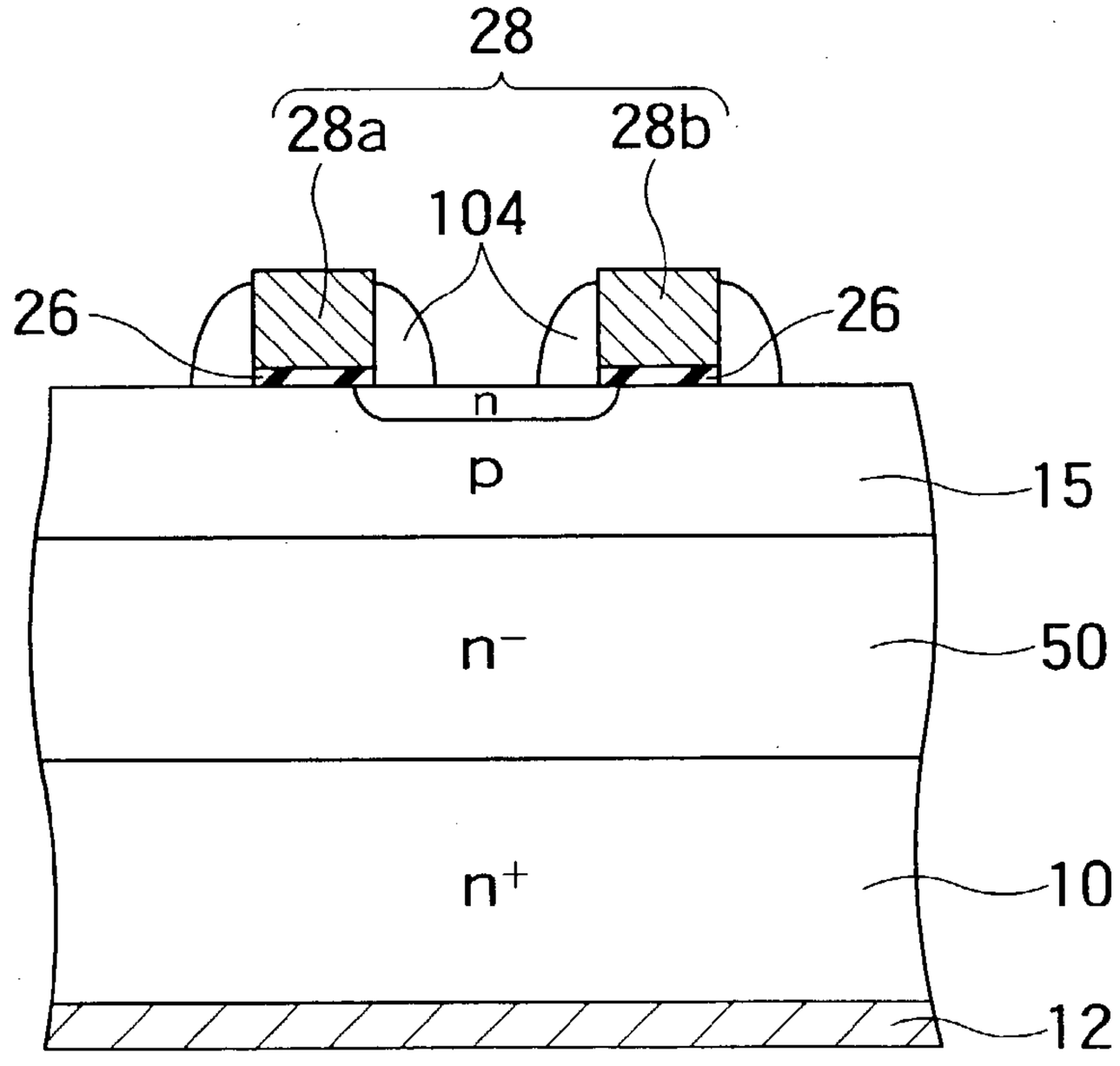

28
28a
28b
104
26
26
n
p
15
n⁻
50
n⁺
10
12

FIG. 18

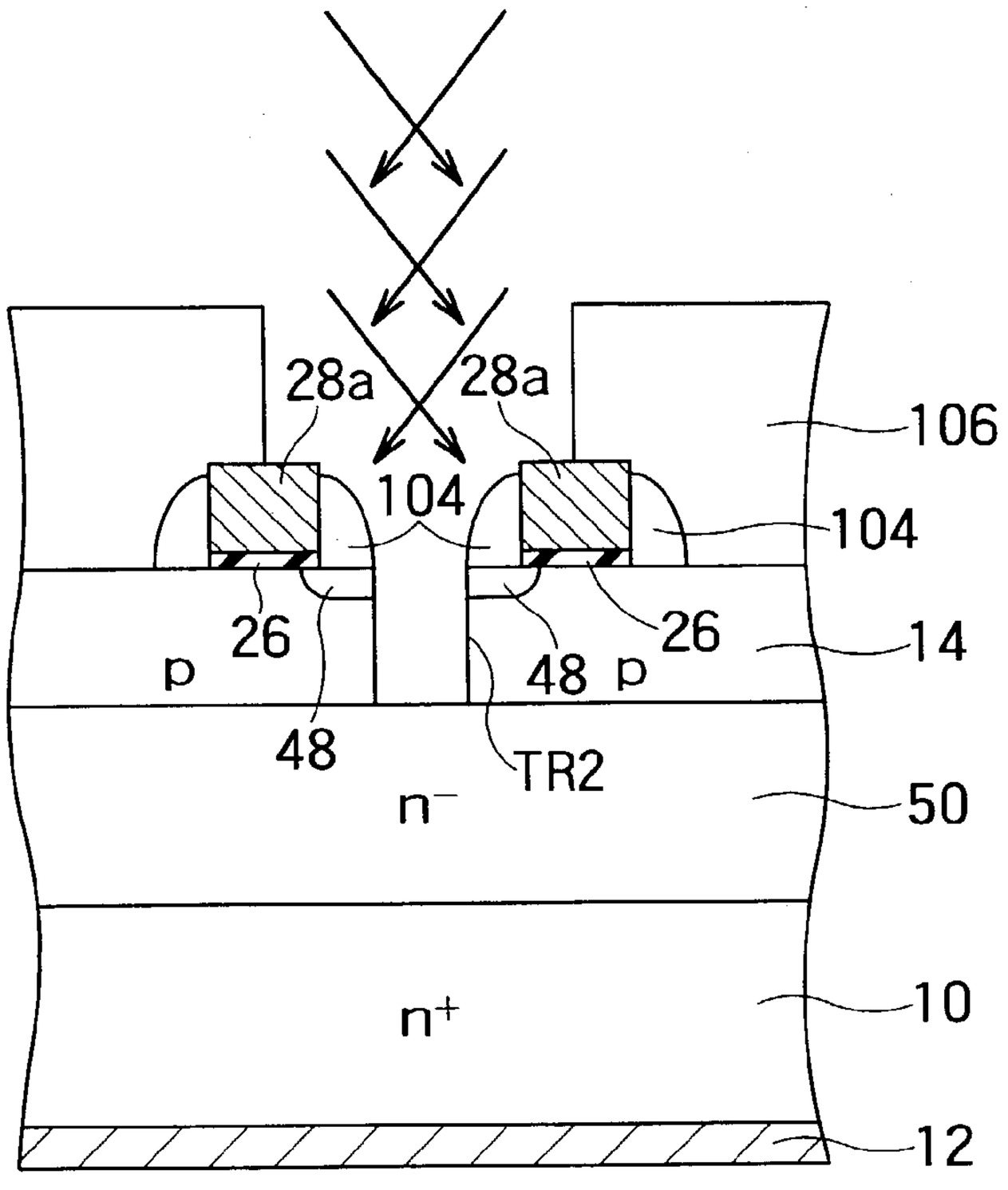

28a
28a
106
104
104
26
26
p
48
p
14
48
TR2
n⁻
50
n⁺
10
12

FIG. 19

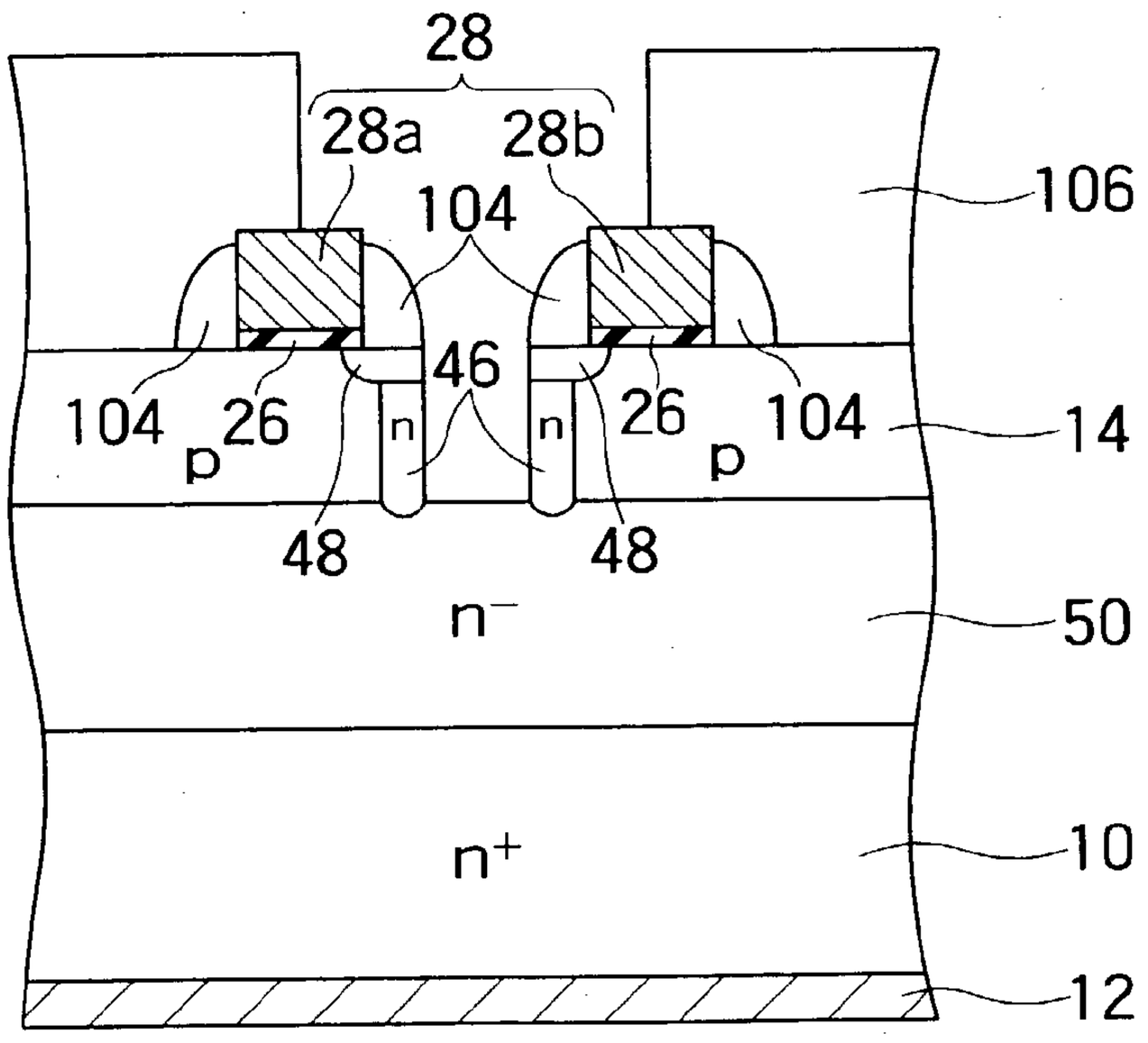

28
28a
28b
104
106
46
104
26
n
n
26
104
p
p
14
48
48
n⁻
50
n⁺
10
12

FIG. 20

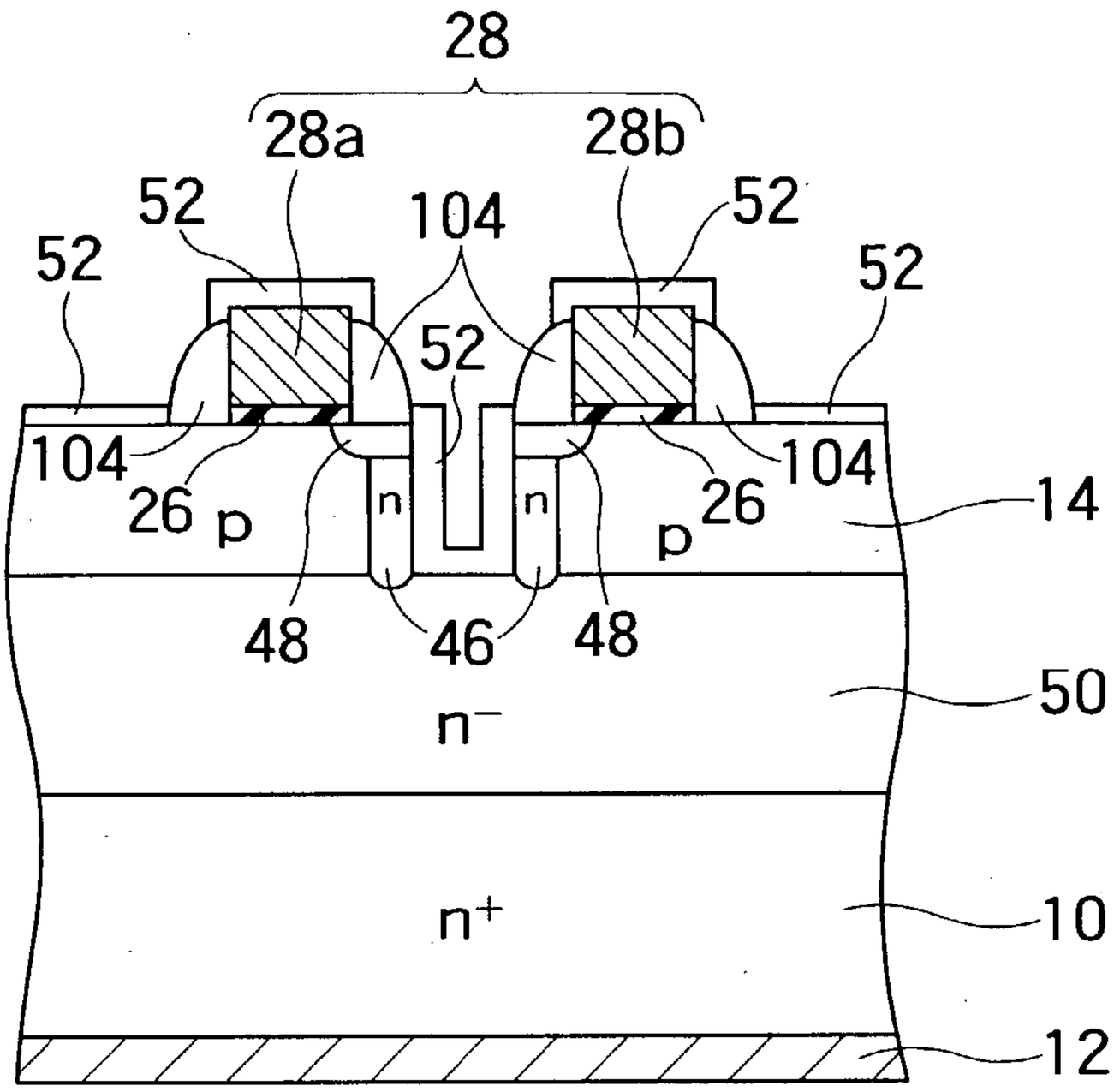

28
28a
28b
52
52
104
52
52
52
104
26
p
n
n
p
26
104
14
48
46
48
n⁻
50
n⁺
10
12

FIG. 21

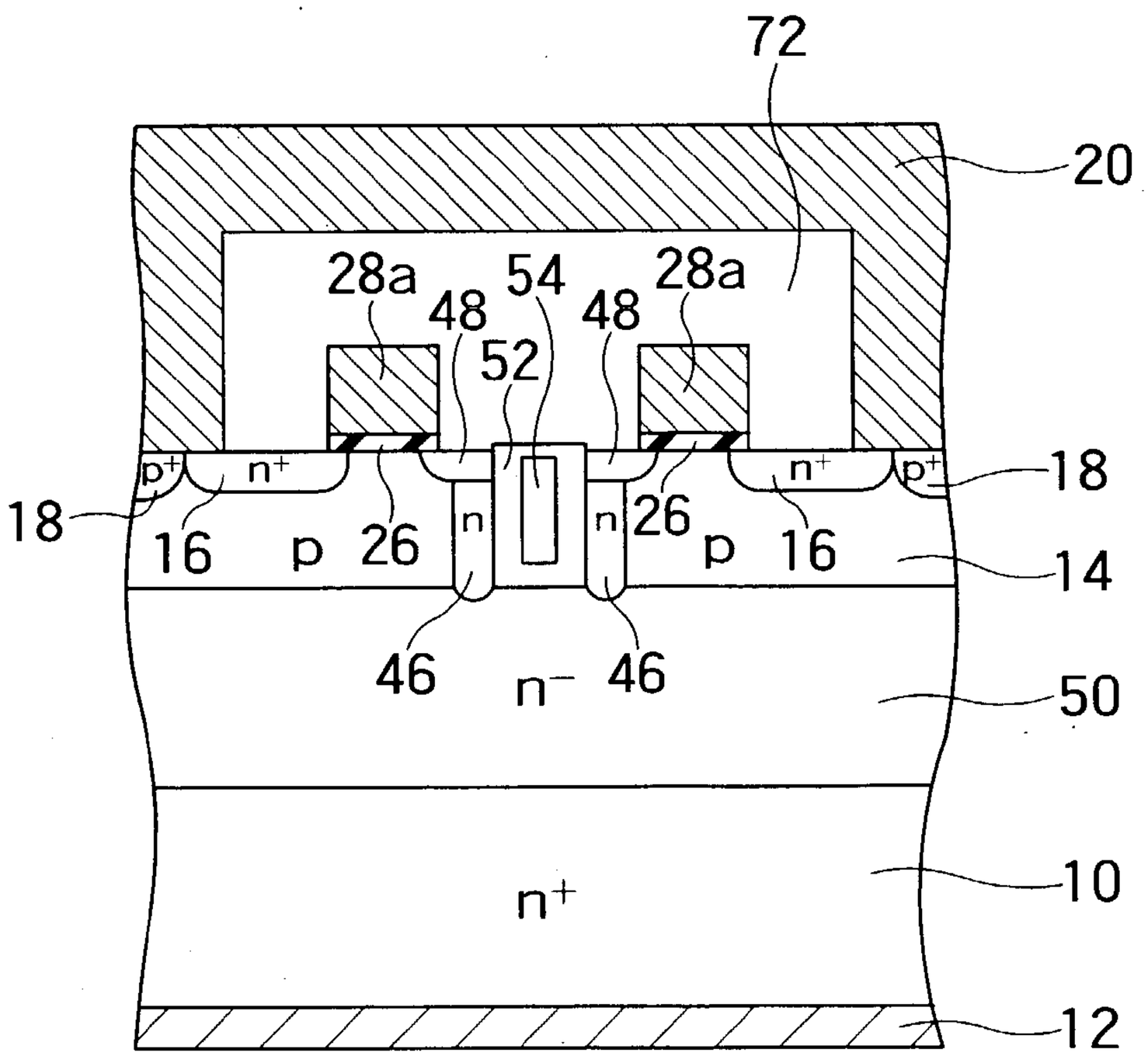

72
20
28a
48
54
48
28a
52
p⁺
n⁺
n⁺
p⁺
18
18
16
p
26
n
n
26
p
16
14
46
n⁻
46
50
n⁺
10
12

FIG. 22

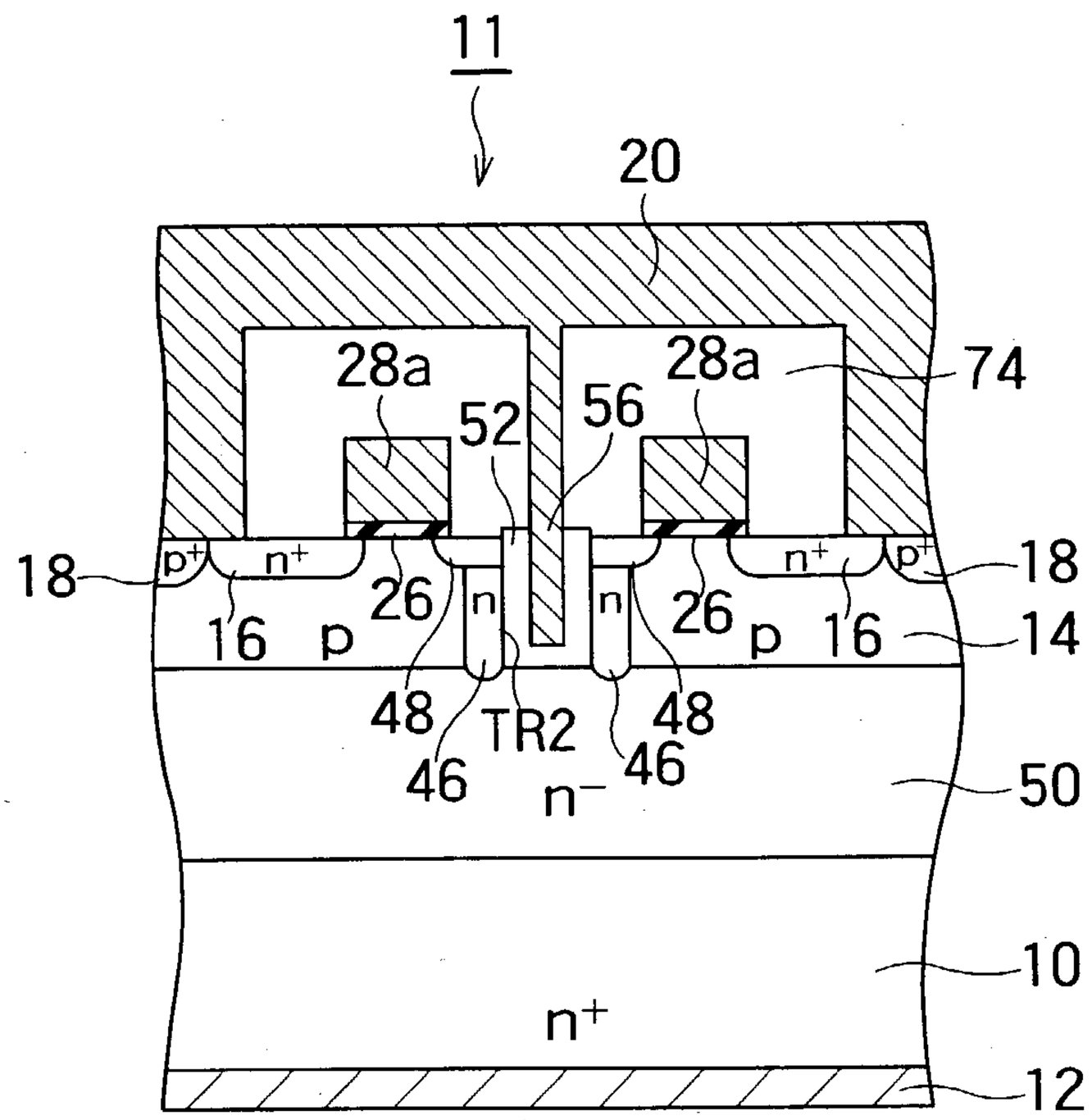

11
20
28a
28a
74
52
56
18
p+
n+
n+
p+
18
26
n
n
26
16
p
p
16
14
48
TR2
48
46
46
n−
50
10
n+
12

FIG. 23

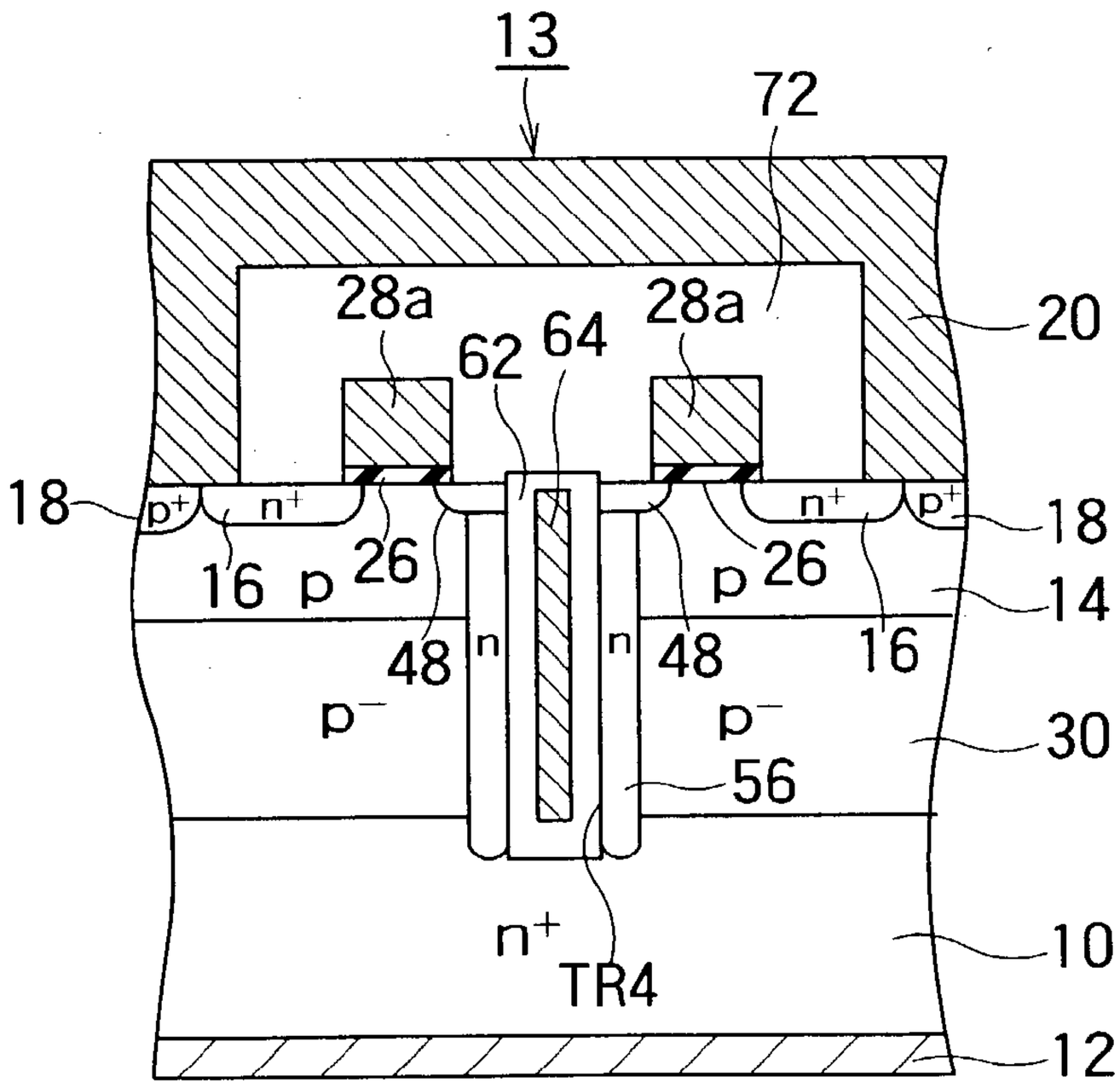

13
72
28a
28a
20
62
64
18
p+
n+
n+
p+
18
16
p
26
p
26
14
48
n
n
48
16
p−
p−
30
56
n+
TR4
10
12

FIG. 24

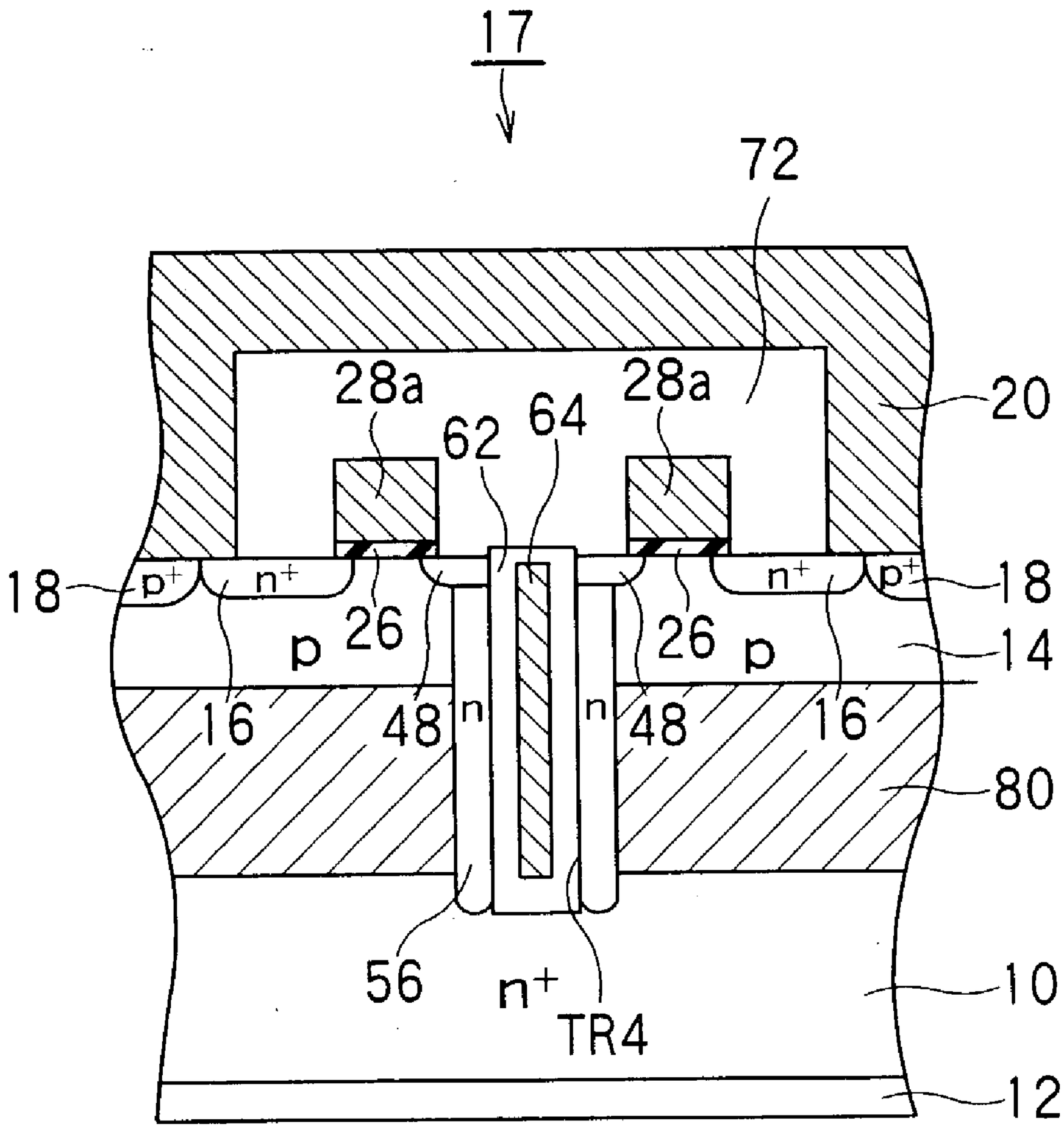
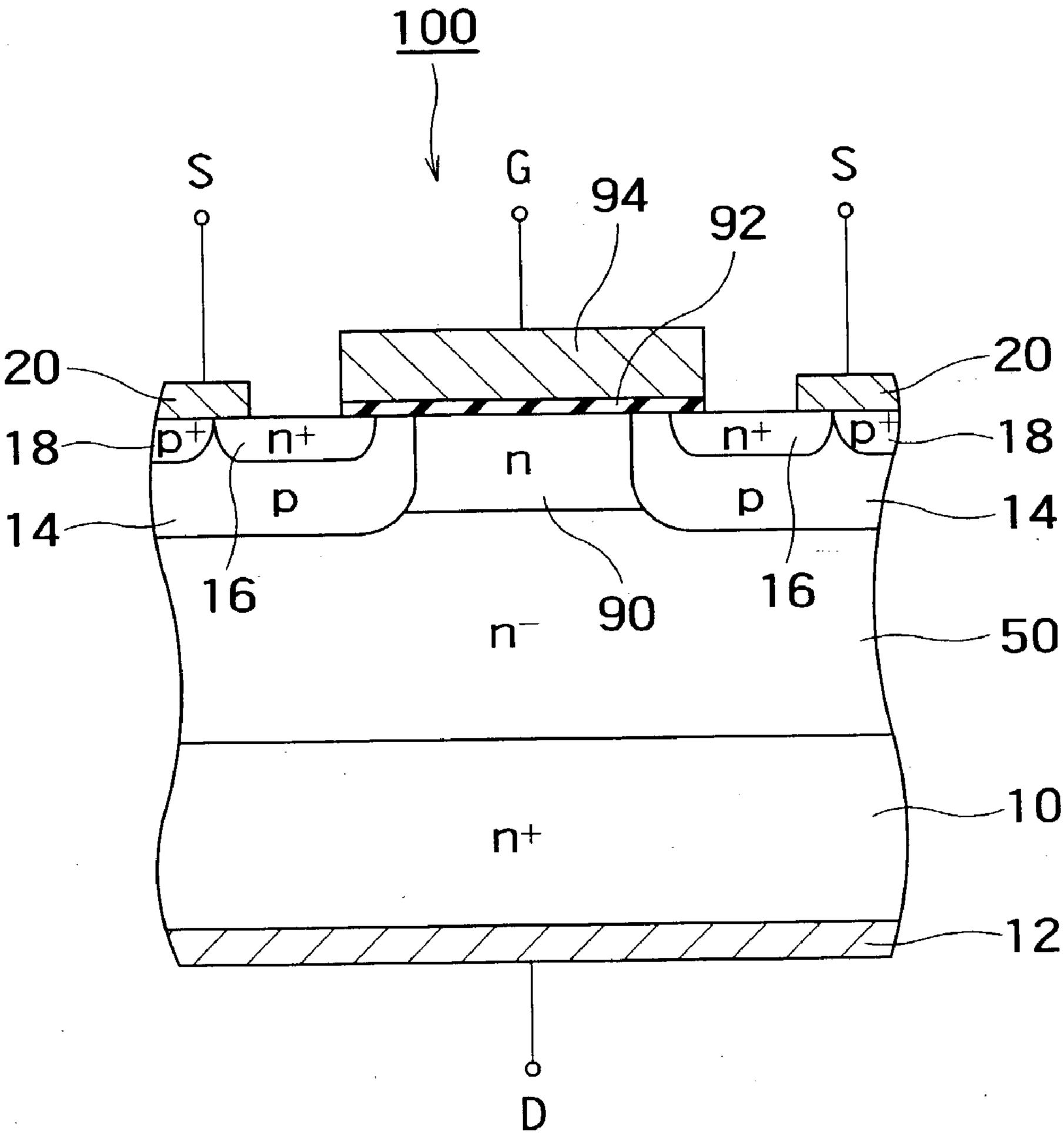

17
72
28a
28a
62
64
20
18
p+
n+
n+
p+
18
26
26
p
p
14
16
48
n
n
48
16
80
56
n+
TR4
10
12

FIG. 25




RELATED ART

FIG. 26

# SEMICONDUCTOR DEVICE

## CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims benefit of priority under 35USC §119 to Japanese patent application No. 2002-94361, filed on Mar. 29, 2002, the contents of which are incorporated by reference herein.

## BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor device and, more particularly, to a semiconductor device having a power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) structure.

[0004] 2. Related Background Art

[0005] In recent years, demand for a power MOSFET has been rapidly increasing in the field of a switching power source of heavy current and high breakdown voltage and, in addition, in the field of switching elements for energy saving of mobile communication devices such as a notebook-sized PC (Personal Computer). Since the power MOSFET is often used for a power management circuit, a safety circuit of a lithium ion battery, and the like in these fields, driving with a lower voltage so that the device can be directly driven with a battery voltage, lower ON-state resistance, reduction in capacitance $Q_{gd}$ between a gate and a drain for reducing a switching loss, and the like are strongly demanded.

[0006] A conventional vertical-type power MOSFET will be described with reference to a schematic cross section of **FIG. 26**. In the following diagrams, like parts are designated by like reference numerals and repetitive descriptions thereof will be appropriately omitted.

[0007] In a power MOSFET **100** shown in **FIG. 26, a** drain electrode **12** is provided on the under face of an $n^+$ type low-resistance semiconductor substrate **10**, and an $n^-$ type high-resistance epitaxial layer **50** is formed on the top face of the low-resistance semiconductor substrate **10**. In a surface portion of the high-resistance epitaxial layer **50**, a p type base layer **14** is selectively formed. In a surface portion of the p type base layer **14**, an $n^+$ type source layer **16** is selectively formed. In a surface portion of the p type base layer **14**, a highly-doped p type region **18** is selectively formed so as to be adjacent to the $n^+$ type source layer **16**. In the surface portion of the high-resistance epitaxial layer **50**, in a region sandwiched by the p-type base layers **14**, an Njfet region **90** is selectively formed, into which an n-type impurity is doped at a higher concentration as compared with the high-resistance epitaxial layer **50**. On the surface of the Njfet region **90**, the surfaces of the p-type base layers **14** sandwiching the Njfet region **90**, and the surfaces of end portions of the $n^+$ type source layers **16** facing each other so as to sandwich the Njfet region **90**, a gate electrode **94** is provided via a gate insulating film **92**. On the surfaces of the $n^+$ type source layers **16** and the surfaces of the highly-doped p type regions **18**, source electrodes **20** are provided so as to sandwich the gate electrode **94**.

[0008] For the power MOSFET **100** having such a structure, it is necessary to make the Njfet region **90** easily depleted in order to reduce the gate-drain capacitance $Q_{gd}$.

[0009] However, when the impurity concentration of the Njfet region **90** is lowered to make the Njfet region **90** easily depleted, a problem occurs such that an ON-state resistance Ron of the device increases and, as a result, a breakdown voltage of the device decreases.

## BRIEF SUMMARY OF THE INVENTION

[0010] According to a first aspect of the invention, there is provided a semiconductor device comprising: a semiconductor substrate, at least a surface portion thereof serving as a low-resistance drain layer of a first conductivity type; a first main electrode connected to the low-resistance drain layer; a high-resistance epitaxial layer of the first conductivity type formed on the low-resistance drain layer; a second-conductivity type base layer selectively formed in a surface portion of the high-resistance epitaxial layer; a first-conductivity type source layer selectively formed in a surface portion of the second-conductivity type base layer; a jfet layer of the first conductivity type selectively formed in a region sandwiched by the second-conductivity type base layers in a surface portion of the high-resistance epitaxial layer and having impurity concentration higher than that of the high-resistance epitaxial layer; a gate insulating film formed on at least a part of the surface of the first-conductivity type jfet layer, on the surfaces of the second-conductivity type base layers facing each other across the first-conductivity type jfet layer, and on the surfaces of end portions of the first-conductivity type source layers facing each other across the first-conductivity type jfet layer; a control electrode formed on the gate insulating film; and a second main electrode in ohmic contact with the first-conductivity type source layer and the second-conductivity type base layer so as to sandwich the control electrode, wherein assuming that depth of the second-conductivity type base layer is Xj, width L of the first-conductivity type jfet layer in the direction orthogonal to the longitudinal direction of the control electrode is substantially equal to or less than that of an interval between neighboring control electrodes and satisfies the following expression.

$$L \leq Xj \times 0.7$$

[0011] According to a second aspect of the invention, there is provided a semiconductor device comprising: a semiconductor substrate, at least a surface portion thereof serving as a low-resistance drain layer of a first conductivity type; a first main electrode connected to the low-resistance drain layer; a high-resistance epitaxial layer of the first conductivity type formed on the low-resistance drain layer; a second-conductivity type base layer selectively formed in a surface portion of the high-resistance epitaxial layer; a first-conductivity type source layer selectively formed in a surface portion of the second-conductivity type base layer; a jfet layer of the first conductivity type selectively formed in a region sandwiched by the second-conductivity type base layer in the surface portion of the high-resistance epitaxial layer and having impurity concentration higher than that of the high-resistance epitaxial layer; a gate insulating film formed on at least a part of the surface of the first-conductivity type jfet layer, on the surfaces of the second-conductivity type base layers facing each other across the first-conductivity type jfet layer, and on the surfaces of end portions of the first-conductivity type source layers facing each other across the first-conductivity type jfet layer; a control electrode formed on the gate insulating film; and; a

second main electrode in ohmic contact with the first-conductivity type source layer and the second-conductivity type base layer so as to sandwich the control electrode, wherein the, second-conductivity type base layers sandwiching the first-conductivity type jfet layer are disposed close to each other so that depletion from the second-conductivity type base layer becomes dominant, and the gate insulating film and the control electrode are formed by selectively removing a part of a region facing the first-conductivity type jfet layer.

[0012] According to a third aspect of the invention, there is provided a semiconductor device comprising: a semiconductor substrate, at least a surface portion thereof serving as a low-resistance drain layer of a first conductivity type; a first main electrode connected to the low-resistance drain layer; a high-resistance epitaxial layer of a second-conductivity type formed on the low-resistance drain layer; a second-conductivity type base layer selectively formed on the high-resistance epitaxial layer; a first-conductivity type source layer selectively formed in a surface portion of the second-conductivity type base layer; a trench formed in a region sandwiched by the second-conductivity type base layers with a depth extending from the surface of the high-resistance epitaxial layer to the semiconductor substrate; a jfet layer of the first conductivity type formed on side walls of the trench; an insulating layer formed in the trench; an LDD layer of the first-conductivity type formed in a surface portion of the second-conductivity type base layer so as to be connected to the first-conductivity type jfet layer around a top face of the trench; a control electrode formed above the semiconductor substrate so as to be divided into a plurality of parts, and formed on a gate insulating film formed on a part of the surface of the LDD layer, on surfaces of end parts of the first-conductivity type source layer facing each other across the trench, and on a region of the surface of the second-conductivity type base layer sandwiched by the LDD layer and the first-conductivity type source layer; and a second main electrode in ohmic contact with the first-conductivity type source layer and the second-conductivity type base layer so as to sandwich the control electrode.

[0013] According to a fourth aspect of the invention, there is provided a semiconductor device comprising: a semiconductor substrate, at least a surface portion thereof serving as a low-resistance drain layer of a first conductivity type; a first main electrode connected to the low-resistance drain layer; a first insulating layer formed on the low-resistance drain layer; a second-conductivity type base layer formed on the first insulating layer; a first-conductivity type source layer selectively formed in a surface portion of the second-conductivity type base layer; a trench formed so as to extend from the surface of the second-conductivity type base layer to the semiconductor substrate; a jfet layer of the first conductivity type formed on side walls of the trench; a second insulating layer formed in the trench; an LDD layer of the first conductivity type formed in a surface portion of the second-conductivity type base layer so as to be connected to the jfet layer of the first conductivity type around a top face of the trench; a control electrode formed so as to be divided into a plurality of parts above the semiconductor substrate, and formed on a gate insulating film formed on a part of the surface of the LDD layer, on surfaces of end portions of the first-conductivity type source layer facing each other across the trench, and on a region of the second-conductivity type base layer sandwiched by the LDD layer and the first-conductivity type source layer; and a second main electrode in ohmic contact with the first-conductivity type source layer and the second-conductivity type base layer so as to sandwich the control electrode.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0014] **FIG. 1** is a schematic cross section showing a first embodiment of a semiconductor device according to the invention.

[0015] **FIG. 2** is a graph showing a simulation result of width L of an Njfet region in the semiconductor device illustrated in **FIG. 1**.

[0016] **FIG. 3** is a graph showing a simulation result of the amount of a dose in the surface of the Njfet region in the semiconductor device illustrated in **FIG. 1**.

[0017] **FIG. 4** is a schematic cross section showing a second embodiment of the semiconductor device according to the invention.

[0018] **FIG. 5** is a schematic cross section showing a third embodiment of the semiconductor device according to the invention.

[0019] **FIG. 6** is a diagram showing electron density in a conventional power MOSFET **100** illustrated in **FIG. 26**.

[0020] **FIG. 7** is a diagram for explaining reduction in gate-drain capacitance $Q_{gd}$ by the semiconductor device illustrated in **FIG. 5**.

[0021] **FIG. 8** is a graph showing a simulation result of a proper range of impurity concentration in an LDD region in the semiconductor device illustrated in **FIG. 5**.

[0022] **FIG. 9** is a plan view showing a first example of a plane shape of a gate electrode of the semiconductor device illustrated in **FIG. 5**.

[0023] **FIG. 10** is a plan view showing a second example of a plane shape of the gate electrode of the semiconductor device illustrated in **FIG. 5**.

[0024] **FIG. 11** is a schematic cross section taken along line A-A of **FIG. 10**.

[0025] **FIG. 12** is a schematic cross section taken along line B-B of **FIG. 10**.

[0026] **FIG. 13** is a plan view showing a third example of a plane shape of the gate electrode of the semiconductor device illustrated in **FIG. 5**.

[0027] **FIG. 14** is a plan view showing a fourth example of a plane shape of the gate electrode of the semiconductor device illustrated in **FIG. 5**.

[0028] **FIG. 15** is a schematic cross section showing a fourth embodiment of the semiconductor device according to the invention.

[0029] **FIG. 16** is a schematic cross section showing a fifth embodiment of the semiconductor device according to the invention.

[0030] **FIGS. 17 through 22** are schematic cross sections for explaining a method of manufacturing the semiconductor device shown in **FIG. 16**.

[0031] **FIG. 23** is a schematic cross section showing a sixth embodiment of the semiconductor device according to the invention.

[0032] **FIG. 24** is a schematic cross section showing a seventh embodiment of the semiconductor device according to the invention.

[0033] **FIG. 25** is a schematic cross section showing a modification of the semiconductor device illustrated in **FIG. 24**.

[0034] **FIG. 26** is a schematic cross section showing an example of a conventional vertical-type power MOSFET.

## DETAILED DESCRIPON OF THE INVENTION

[0035] Embodiments of the invention will be described in detail hereinbelow with reference to the drawings.

[0036] (1) First Embodiment

[0037] **FIG. 1** is a schematic cross section showing a first embodiment of a semiconductor device according to the invention. The semiconductor device of the present embodiment is characterized in that an Njfet region **40** is formed in a narrow width at a high concentration. The structure of the semiconductor device of the embodiment will be described in more detail hereinbelow.

[0038] A power MOSFET **1** shown in **FIG. 1** is a power MOSFET of a vertical type to which the invention is applied, and includes an $n^+$ type low-resistance semiconductor substrate **10**, a drain electrode **12**, an $n^-$ type high-resistance epitaxial layer **50**, a p type base layer **14**, an $n^+$ type source layer **16**, the Njfet region **40**, a gate electrode **24**, and a source electrode **20**.

[0039] The drain electrode **12** is provided on one of the surfaces (under face in **FIG. 1**) of the $n^+$ type low-resistance semiconductor substrate **10**, and the $n^-$ type high-resistance epitaxial layer **50** is formed on the other face (top face in **FIG. 1**) of the $n^+$ type low-resistance semiconductor substrate **10**. The p type base layer **14** is selectively formed in a surface portion of the $n^-$ type high-resistance epitaxial layer **50**, and the $n^+$ type source layer **16** is selectively formed in a surface portion of the p type base layer **14**. In the surface portion of the p type base layer **14**, the highly-doped p type region **18** is formed. The Njfet region **40** is selectively formed in a region sandwiched by the p type base layers **14** in the surface portion of the $n^-$ type high-resistance epitaxial layer **50**. A gate electrode **24** is provided via a gate insulating film **22** on the surface of the Njfet region **40**, on the surfaces of the regions of the p type base layer **14** sandwiching the Njfet region **40**, and on the surfaces of end portions of the $n^+$ type source layers **16** facing each other across the Njfet region **40**. The source electrodes **20** are provided on the surfaces of the $n^+$ type source layers **16** and the surfaces of the highly-doped p type regions **18** so as to sandwich the gate electrode **24**.

[0040] The Njfet region **40** is a characteristic part in the embodiment and, as obviously understood by comparison with **FIG. 26**, the Njfet region **40** is formed so as to be narrower than the Njfet region **90** of the conventional power MOSFET. The width L of the Njfet region **40** is substantially equal to or narrower than the spacing between two neighboring gate electrodes **24**. By forming the Njfet region **40** so as to have such a narrow width L, a structure is obtained with which an amount contributed to the gate-drain capacitance $Q_{gd}$ by the gate electrode **24** decreases and depletion from the neighboring p type base layers **14** becomes dominant in depletion of the Njfet region **40**. More specifically, a simulation shows that the width L of the Njfet region **40** satisfies the relation of $L \leqq 1.0\ \mu m$ when depth Xj of the p type base layer **14** is 1.0 $\mu$m.

[0041] **FIG. 2** is a graph showing a result of the simulation of the width L of the Njfet region **40**. When the gate insulating film **22** is formed in almost uniform thickness of about 30 nm, $R_{on}Q_{gd}$ is about 24 [m$\Omega$nC] or less in the region satisfying the relation of $L \leqq 1.0\ \mu m$ as shown in **FIG. 2**. It is understood that particularly in the region satisfying the relation of Xj×0.7 or less, conspicuous effects appear on both $R_{on}Q_{gd}$ and a breakdown voltage BV.

[0042] Referring again to **FIG. 1**, the Njfet region **40** is formed with a depth almost equal to the depth Xj of the p type base layer **14**. The Njfet region **40** is also formed so that the junction interface thereof with the p-type base layer **14** becomes perpendicular to the surface of the Njfet region **40** as it approaches the surface.

[0043] By narrowing the width L of the Njfet region **40** as described above, the surface density of the Njfet region **40** can be increased to the range from about 1E16 to about 3E17 [$cm^{-3}$], so that on-state resistance $R_{on}$ can be also reduced.

[0044] **FIG. 3** is a graph showing a simulation result of the amount of a dose in the surface of the Njfet region **40**. As shown in **FIG. 3**, the simulation teaches that, when the width L of the Njfet region **40** is 1 $\mu$m, the breakdown voltage BV of 30V or higher is obtained and the value of $R_{on}Q_{gd}$ is also low, over a range in which the amount N of the surface dose of the Njfet region **40** satisfies the relation of $N \leqq 4E \times 12$.

[0045] (2) Second Embodiment

[0046] **FIG. 4** is a schematic cross section showing a second embodiment of a semiconductor device according to the invention. As obviously understood from comparison with **FIG. 1, a** power MOSFET **3** of the second embodiment is characterized in that a gate insulating film **23** is formed so as to be thicker in a region facing the Njfet region **40** as well as in that the Njfet region **40** is formed in narrow width and at high concentration. More specifically, a portion **23***a* of the gate insulating film **23** facing the Njfet region **40** has a thickness of about 90 nm whereas the other portion of the gate insulating film **23** is formed to have a thickness of about 30 nm. By the configuration, in the region facing the Njfet region **40**, a gate electrode **25** can be further isolated from the Njfet region **40**.

[0047] Since the Njfet region **40** is formed in narrow width and at high concentration, at the time of depleting the Njfet region **40**, depletion from the p type base layer **14** becomes dominant. Thus, it is possible to employ such structures of the gate insulating film **23** and the gate electrode **25**.

[0048] In the power MOSFET **3** of the embodiment, the gate electrode **25** is provided via the gate insulating film **23** which is formed so that the region facing the Njfet region **40** is thicker than the other region. Thus, the amount of contribution to the gate-drain capacitance $Q_{gd}$ of the gate electrode can be further reduced.

[0049] (3) Third Embodiment

[0050] **FIG. 5** is a schematic cross section showing a third embodiment of a semiconductor device according to the invention. As obviously understood by comparison with **FIG. 1, a** power MOSFET **5** of the third embodiment is characterized in that a portion facing the Njfet region **40** in the gate electrode **28** is selectively removed.

[0051] By employing the structure in which the gate electrode **28** is divided as described above, the width L of the Njfet region **40** can be further narrowed, so that the gate-drain capacitance $Q_{gd}$ is further reduced and operation speed of the device is further increased. By implanting n-type impurities using the gate electrode **28** in the divisional structure as a mask, the Njfet region **40** can be formed in a self-aligned manner.

[0052] **FIGS. 6 and 7** are diagrams for explaining reduction in the gate-drain capacitance $Q_{gd}$ according to the third embodiment. **FIG. 6** shows electron density in the conventional power MOSFET **100** illustrated in **FIG. 26**, and **FIG. 7** shows electron density in the case where the gate electrode of the power MOSFET **100** of **FIG. 26** is simply divided without reducing the width L of the Njfet region. Each of **FIGS. 6 and 7** shows electron density when 20V is applied as Vds.

[0053] As understood from comparison between **FIG. 6** and **FIG. 7**, when the gate electrode **94** of the conventional power MOSFET **100** is simply divided, the ratio of depletion by the gate remains high due to the wide region between neighboring p type base layers **14**. As a result, depletion from the gate does not occur, a breakdown voltage decreases.

[0054] Referring again to **FIG. 5**, the power MOSFET **5** of the embodiment further includes an LDD (Lightly Doped Drain) region **44** formed in the surface portion of the Nifet region **40**. The LDD region **44** is formed in a self-aligned manner by shallowly implanting n-type impurity ions into the Njfet region **40** by using the divided gate electrode **28** as a mask and, after that, performing thermal diffusion.

[0055] **FIG. 8** is a graph showing an appropriate range of impurity concentration in the LDD region **44** of the power MOSFET **5** obtained by a simulation. It is understood from the graph that, when Xj=0.8 $\mu$m and L=0.4 $\mu$m, the value of $R_{on}Q_{gd}$ can be set to **10**[mΩnC] or less by setting the upper limit of the impurity concentration Cs of the LDD region **44** to about 5E17 [$cm^{-3}$].

[0056] Referring to **FIGS. 9 through 14**, some plane shapes of the gate electrode of the power MOSFET **5** of the embodiment will be described.

[0057] **FIG. 9** shows a plane shape of a gate electrode **29** as a first example. The gate electrode **29** of the example is divided into two parts and each part is formed so as to have a stripe pattern similar to the plane shape of the gate electrode of a conventional power MOSFET. Such an electrode shape has a drawback such that resistance of the gate electrode itself might become high and it might disturb increase in the processing speed of the device.

[0058] As a solution to such drawback, the Njfet region **40** of the power MOSFET **5** is not formed in stripes in the longitudinal direction of the gate electrode **28** in the surface portion of the $n^-$ type high-resistance epitaxial layer **50**. For example, as shown in a second example of **FIG. 10**, divided gate electrodes each having a hollow rectangular plane shape are disposed at regular intervals in the longitudinal direction, each Njfet region **40** just bellow the hollow rectangular is surrounded by the p type base layer **14**, and divided gate electrodes are connected to each other at regular intervals so as to form a plane shape like a ladder in a region where the Njfet region **40** does not exist in the lower layer. Since the gate electrodes **28** are formed so as to surround the Njfet regions **40** disposed at regular intervals from the top view, resistance of the gate electrodes can be largely reduced. Further, depletion of the Njfet region **40** develops only in the horizontal direction of the drawing sheet in the example shown in **FIG. 9**. By disposing the Njfet regions **40** at regular intervals as shown in **FIG. 10**, depletion develops omnidirectionally. Consequently, operation speed of the device is further improved. **FIG. 11** shows a schematic cross section taken along line A-A of **FIG. 10**, and **FIG. 12** shows a schematic cross section taken along line B-B of **FIG. 10**.

[0059] In the example shown in **FIG. 10**, the shape of the Njfet region **40** surrounded by the p type base layer **14** is a rectangular shape. However, the shape of the Njfet region **40** is not limited to the rectangular shape but may be, for example, a circular shape **32** as a third example shown in **FIG. 13** or a polygonal shape **34** as a fourth example show in **FIG. 14**.

[0060] (4) Fourth Embodiment

[0061] **FIG. 15** is a schematic cross section showing a fourth embodiment of the semiconductor device according to the invention. A power MOSFET **9** shown in **FIG. 15** is obtained by applying the foregoing third embodiment to a lateral-type power MOSFET. Specifically, in a region outside of the p type base layer **14**, an $n^+$ type low-resistance drain layer **68** is formed so as to extend from the surface of the $n^-$ type high-resistance epitaxial layer **50** to an $n^+$ low-resistance semiconductor layer **70** just below the layer **50**. A drain electrode **62** is provided on the surface of the $n^+$ type low-resistance drain layer **68**, thereby constructing a vertical-type power MOSFET. The power MOSFET **9** is substantially the same as the power MOSFET **5** shown in **FIG. 5** in that the Njfet region **40** sandwiched (or surrounded) by the p type base layer **14** is formed so that its width L is narrow, in that the Njfet region **40** is formed at high concentration, in that the gate electrode **28** is provided in a divided form, and in that the LDD region **44** is formed in the surface portion of the Njfet region **40**.

[0062] (5) Fifth Embodiment

[0063] **FIG. 16** is a schematic cross section showing a fifth embodiment of a semiconductor device according to the invention. A power MOSFET **7** shown in **FIG. 16** is characterized in that it further includes an insulating film **52** formed in a trench TR2 provided with a depth which is approximately the same as diffusion depth of the p type base layer **14** in an almost center portion in the Njfet region **46** and it further includes an electrode **54** of a fixed potential provided in the insulating film **52**.

[0064] By providing the trench TR2 in the Njfet region **46** sandwiched (or surrounded) by the p type base layer **14** as described above, ions can be implanted obliquely to the surface of the wafer. Consequently, the highly-doped Njfet

region **46** can be formed in a fine structure on the side walls of the trench TR**2**. By providing the electrode **54** via the insulating film **52** in the trench TR**2** and fixing the potential of the electrode **54**, the breakdown voltage can be further increased by about 5V and the gate-drain capacitance $Q_{gd}$ can be further reduced by about 20%.

[**0065**] A method of manufacturing the power MOSFET **7** shown in **FIG. 16** will be briefly described with reference to **FIGS. 17 through 22**.

[**0066**] First, as shown in **FIG. 17**, an $n^-$ type high-resistance epitaxial layer **50** is formed on the top face of the $n^+$ type low-resistance semiconductor substrate **10** having the drain electrode **12** on its under face, and a p type base layer **15** is formed on the top face of the $n^-$ type epitaxial layer **50**. Subsequently, a gate insulating film **26** and the gate electrode **28** are formed on the surface of the p type base layer **15**. After that, the gate electrode **28** is divided into at least two parts. Subsequently, a photoresist **102** is formed, and n type impurities are selectively implanted between the divided gate electrodes **28***a*, thereby forming a shallow n-type lightly doped drain (LDD) region **48** so that its both ends face the divided gate electrodes **28***a* via the gate insulating film **26** (refer to **FIG. 18**). By making the ends of the LDD region **48** overlapped with the gate electrode **28** as described above, the gate-drain capacitance $Q_{gd}$ can be suppressed.

[**0067**] After removing the photoresist **102**, an insulating film is deposited on the whole wafer and RIE (Reactive Ion Etching) is executed. By the operation, as shown in **FIG. 18**, the deposited insulating film can be left only on the side walls of the gate insulating film **26** and the gate electrodes **28***a* (side walls **104**). As a material of the side walls **104**, a conductive material such as polysilicon can be used in place of the insulating film. In this case, the gate electrode **28***a* has to be oxidized so as to be insulated from the conductive material by post-oxidation or the like.

[**0068**] Next, as shown in **FIG. 19, a** photoresist **106** is formed. By using the photoresist **106** and the side walls **104** as a mask, the p type base layer **15** is selectively removed by RIE, thereby forming the trench TR**2** with the ends of the LDD region **48** being retained by widths each of which corresponds to that of the side wall **104**. Subsequently, n-type impurities are implanted at oblique angles to the wafer as shown by arrows in **FIG. 19**. Thus, the n type region **46** serving as an Njfet region is selectively formed only on the side walls of the trench TR**2** (**FIG. 20**).

[**0069**] Subsequently, as shown in **FIG. 21**, the oxide film **52** is formed on the silicon on the surface of the wafer with an oxidizing process. If ions implanted in the side walls of the trench TR**2** are, for example, of arsenic, the extent of thermal diffusion is less than in a case of phosphorus and, by speed-increased oxidization, the oxide film in the surface portion of arsenic can be formed thicker than that of the other silicon surface portion.

[**0070**] Further, as shown in **FIG. 22**, the trench TR**2** is buried with the insulating film **52**, or the insulating film **52** and a conductive material. Finally, an interlayer insulating film **72** and the source electrode **20** are formed.

[**0071**] By the processes, the size of the gate-drain overlap region below the gate electrode is minimized by the LDD region **48**, and the highly-doped Njfet region **46** can be formed on the side walls of the trench TR**2**. By filling the trench TR**2** with the insulating film or the conductive material via the insulating film **52** and connecting and fixing the electrode **54** made of the conductive material to the source potential or other potential, a field plate effect can be expected in the Njfet region **46** of the side walls of the trench TR**2**. As a result, depletion is promoted. The concentration of the Njfet region **46** of the side walls of the trench TR**2** can thus be made higher than that of the drift layer necessary to obtain a breakdown voltage for an ordinary purpose. With the structures, remarkable reduction in the gate-drain capacitance $Q_{gd}$ and the on-state resistance $R_{on}$ can be realized.

[**0072**] The manufacturing method of the power MOSFET according to the embodiment is not limited to the above described method. For example, in place of the method of preliminarily forming the p type base layer **15** before dividing the gate electrode **28**, p type impurities may be diffused only from the source region after division of the gate electrode **28**. Also with respect to the shallow n-type LDD region **48**, in place of the method of implanting n type impurities in the self-alignment process so that both ends of the LDD region **48** face the gate electrode **28***a* via the gate oxide film **26**, the LDD region **48** may be formed by implanting after forming the trench TR or after forming the oxide film **52**. In this case, the number of processes of thermal diffusion can be reduced, and the overlap of the gate and drain can be adjusted to the minimum amount.

[**0073**] (6) Sixth Embodiment

[**0074**] **FIG. 23** is a schematic cross section showing a sixth embodiment of a semiconductor device according to the invention. A power MOSFET **11** shown in **FIG. 23** is characterized in that the electrode **56** formed in the insulating film **52** in the trench TR**2** is electrically connected to an upper part of the source electrode **20**. With such a structure, the potential of the electrode **56** in the trench TR**2** can be fixed to the potential of the source electrode **20**.

[**0075**] (7) Seventh Embodiment

[**0076**] **FIG. 24** is a schematic cross section showing a seventh embodiment of a semiconductor device according to the invention. A power MOSFET **13** shown in the diagram is characterized in that a trench TR**4** is formed so deep as to reach the $n^+$ type semiconductor substrate **10** so that the n-type highly-doped region **56** of the side walls of the trench TR**4** is directly connected to the $n^+$ type semiconductor substrate **10** and in that the n type highly doped region **56** is sandwiched by the insulating film **62** in the trench TR**4** and the $p^-$ type region **30** on the outside of the trench TR**4**.

[**0077**] In the foregoing fifth and sixth embodiments, since the trench TR**2** is formed with approximate same depth as that of the p-type base layer **14**, the Njfet region **46** on the side walls of the trench also has to be formed with approximate same depth as the depth of the p-type base layer **14** for the following reason. If the trench is too shallow, a current path between the source and the drain is interrupted. On the other hand, if the trench is too deep, the impurity concentration of the $n^-$ type drain layer increases. In this case, it is concerned that a depletion layer does not extend and the breakdown voltage decreases.

[**0078**] Since the power MOSFET **13** of the seventh embodiment employs the structure in which the n type highly-doped region **56** serving as the Njfet region is sand-

wiched by the insulating film **62** in the trench TR**4** and the $p^-$type region **30** on the outside of the trench TR**4**, a current can directly pass to the $n^+$ type low-resistance semiconductor substrate **10** via no $n^-$type drift layers, so that ON-state resistance can be decreased. With the configuration, the n-type highly-doped region **56** is therefore easily depleted and the depletion layer extends also to the $p^-$type region **30**. As a result, a desired breakdown voltage can be obtained.

[**0079**] **FIG. 25** is a schematic cross section showing a modification of the seventh embodiment. A power MOSFET **17** shown in the diagram has an insulating layer **80** formed on the outside of the trench TR**4** in place of the $p^-$type region **30** formed on the outside of the trench TR**4** in the power MOSFET **13** shown in **FIG. 24**. Even with such an insulating layer **80**, the n type highly-doped region **56** on the side walls of the trench is depleted.

[**0080**] Since the third through seventh embodiments employ the structure in which the gate electrode is divided into two or more parts, there may occur a concern about increase in gate resistance. Examples of methods of eliminating such a concern include a method of metallizing the surface of a gate polysilicon electrode with a silicide process and a method of re-connecting the divided parts of the gate electrode in a terrace state in a wiring process to be performed after forming element regions.

[**0081**] Although the embodiments of the invention have been described above, it is obvious that the invention is not limited to the embodiments but can be variously modified within the scope and the spirit of the invention. For example, the case of selecting the n type as a first conductivity type has been described in the foregoing embodiments. Also when the invention is applied to a p-type channel device in which n and p are opposite to those of the embodiments, similar effects can be obtained.

What is claimed is:

**1**. A semiconductor device comprising:

a semiconductor substrate, at least a surface portion thereof serving as a low-resistance drain layer of a first conductivity type;

a first main electrode connected to the low-resistance drain layer;

a high-resistance epitaxial layer of the first conductivity type formed on the low-resistance drain layer;

a second-conductivity type base layer selectively formed in a surface portion of the high-resistance epitaxial layer;

a first-conductivity type source layer selectively formed in a surface portion of the second-conductivity type base layer;

a jfet layer of the first conductivity type selectively formed in a region sandwiched by the second-conductivity type base layers in a surface portion of the high-resistance epitaxial layer and having impurity concentration higher than that of the high-resistance epitaxial layer;

a gate insulating film formed on at least a part of the surface of said first-conductivity type jfet layer, on the surfaces of the second-conductivity type base layers facing each other across said first-conductivity type jfet layer, and on the surfaces of end portions of the first-conductivity type source layers facing each other across said first-conductivity type jfet layer;

a control electrode formed on the gate insulating film; and

a second main electrode in ohmic contact with the first-conductivity type source layer and the second-conductivity type base layer so as to sandwich the control electrode,

wherein assuming that depth of the second-conductivity type base layer is Xj, width L of said first-conductivity type jfet layer in the direction orthogonal to the longitudinal direction of the control electrode is substantially equal to or less than that of an interval between neighboring control electrodes and satisfies the following expression.

$$L \leqq Xj \times 0.7$$

**2**. The semiconductor device according to claim 1, wherein depth of said first-conductivity type jfet layer is substantially same as that of the second-conductivity type base layer.

**3**. The semiconductor device according to claim 1, wherein impurity concentration N of said first-conductivity type jfet layer satisfies the following expression.

$$N \leqq 4E12/L \ [\mathrm{cm}^{-3}]$$

**4**. The semiconductor device according to claim 1, wherein a junction interface between the second-conductivity type base layer and said first-conductivity type jfet layer becomes perpendicular to the surface of the device as it comes close to the surface of the device.

**5**. The semiconductor device according to claim 1, wherein at least a part of a region of the gate insulating film facing said first-conductivity type jfet layer is thicker than the other region of the gate insulating film.

**6**. The semiconductor device according to claim 1, wherein the gate insulating film and the control electrode are formed by selectively removing a part of a region facing said first-conductivity type jfet layer.

**7**. The semiconductor device according to claim 6, wherein said first-conductivity type jfet layer is formed in a self-aligned manner by using the control electrode as a mask.

**8**. The semiconductor device according to claim 6, which further comprises a first-conductivity type LDD layer which is formed in a surface portion of said first-conductivity type jfet layer and impurity concentration of which is higher than that of the high-resistance epitaxial layer and is lower than that of said first-conductivity type jfet layer.

**9**. The semiconductor device according to claim 8, wherein said first-conductivity type LDD layer is formed in a self-aligned manner by using the control electrode as a mask.

**10**. The semiconductor device according to claim 6, wherein surface peak concentration of said first-conductivity type jfet layer is 5E17 [$\mathrm{cm}^{-3}$ ] or less.

**11**. The semiconductor device according to claim 6, wherein said first-conductivity type jfet layers each having a rectangular plane shape are disposed at regular intervals in the longitudinal direction of the control electrode, and the second-conductivity type base layer is formed so as to surround each of said first-conductivity type jfet layers.

**12**. The semiconductor device according to claim 6, wherein said first-conductivity type jfet layers each having a circular plane shape are disposed at regular intervals in the longitudinal direction of the control electrode, and the second-conductivity type base layer is formed so as to surround each of said first-conductivity type jfet layers.

**13**. The semiconductor device according to claim 6, wherein said first-conductivity type jfet layers each having a polygonal plane shape are disposed at regular intervals in the longitudinal direction of the control electrode, and the second-conductivity type base layer is formed so as to surround each of said first-conductivity type jfet layers.

**14**. A semiconductor device comprising:

a semiconductor substrate, at least a surface portion thereof serving as a low-resistance drain layer of a first conductivity type;

a first main electrode connected to the low-resistance drain layer;

a high-resistance epitaxial layer of the first conductivity type formed on the low-resistance drain layer;

a second-conductivity type base layer selectively formed in a surface portion of the high-resistance epitaxial layer;

a first-conductivity type source layer selectively formed in a surface portion of the second-conductivity type base layer;

a jfet layer of the first conductivity type selectively formed in a region sandwiched by the second-conductivity type base layer in the surface portion of the high-resistance epitaxial layer and having impurity concentration higher than that of the high-resistance epitaxial layer;

a gate insulating film formed on at least a part of the surface of said first-conductivity type jfet layer, on the surfaces of the second-conductivity type base layers facing each other across said first-conductivity type jfet layer, and on the surfaces of end portions of the first-conductivity type source layers facing each other across said first-conductivity type jfet layer;

a control electrode formed on the gate insulating film; and;

a second main electrode in ohmic contact with the first-conductivity type source layer and the second-conductivity type base layer so as to sandwich the control electrode,

wherein the second-conductivity type base layers sandwiching said first-conductivity type jfet layer are disposed close to each other so that depletion from the second-conductivity type base layer becomes dominant, and

the gate insulating film and the control electrode are formed by selectively removing a part of a region facing said first-conductivity type jfet layer.

**15**. The semiconductor device according to claim 14, which further comprises an insulating layer formed in said first-conductivity type jfet layer.

**16**. The semiconductor device according to claim 15, which further comprises an electrode which is formed in the insulating layer so as to be covered with the insulating layer and to which a potential is fixed.

**17**. The semiconductor device according to claim 16, wherein an electrode in said first-conductivity type jfet layer is connected to the second main electrode.

**18**. A semiconductor device comprising:

a semiconductor substrate, at least a surface portion thereof serving as a low-resistance drain layer of a first conductivity type;

a first main electrode connected to the low-resistance drain layer;

a high-resistance epitaxial layer of a second-conductivity type formed on the low-resistance drain layer;

a second-conductivity type base layer selectively formed on the high-resistance epitaxial layer;

a first-conductivity type source layer selectively formed in a surface portion of the second-conductivity type base layer;

a trench formed in a region sandwiched by the second-conductivity type base layers with a depth extending from the surface of the high-resistance epitaxial layer to the semiconductor substrate;

a jfet layer of the first conductivity type formed on side walls of said trench;

an insulating layer formed in said trench;

an LDD layer of the first-conductivity type formed in a surface portion of the second-conductivity type base layer so as to be connected to said first-conductivity type jfet layer around a top face of said trench;

a control electrode formed above the semiconductor substrate so as to be divided into a plurality of parts, and formed on a gate insulating film formed on a part of the surface of said LDD layer, on surfaces of end parts of the first-conductivity type source layer facing each other across said trench, and on a region of the surface of the second-conductivity type base layer sandwiched by said LDD layer and the first-conductivity type source layer; and

a second main electrode in ohmic contact with the first-conductivity type source layer and the second-conductivity type base layer so as to sandwich the control electrode.

**19**. The semiconductor device according to claim 18, which further comprises an electrode which is formed in said trench so as to be covered with the insulating layer and to which a potential is fixed.

**20**. A semiconductor device comprising:

a semiconductor substrate, at least a surface portion thereof serving as a low-resistance drain layer of a first conductivity type;

a first main electrode connected to the low-resistance drain layer;

a first insulating layer formed on the low-resistance drain layer;

a second-conductivity type base layer formed on the first insulating layer;

a first-conductivity type source layer selectively formed in a surface portion of the second-conductivity type base layer;

a trench formed so as to extend from the surface of the second-conductivity type base layer to the semiconductor substrate;

a jfet layer of the first conductivity type formed on side walls of said trench;

a second insulating layer formed in said trench;

an LDD layer of the first conductivity type formed in a surface portion of the second-conductivity type base layer so as to be connected to said jfet layer of the first conductivity type around a top face of said trench;

a control electrode formed so as to be divided into a plurality of parts above the semiconductor substrate, and formed on a gate insulating film formed on a part of the surface of said LDD layer, on surfaces of end portions of the first-conductivity type source layer facing each other across said trench, and on a region of the second-conductivity type base layer sandwiched by said LDD layer and the first-conductivity type source layer; and

a second main electrode in ohmic contact with the first-conductivity type source layer and the second-conductivity type base layer so as to sandwich the control electrode.

**21**. The semiconductor device according to claim 20, which further comprises an electrode which is formed in the second insulating layer so as to be covered with the second insulating layer and to which a potential is fixed.

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