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(54) **MULTI-CHIP MODULE AND FABRICATING METHOD THEREOF**

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(57) **ABSTRACT**

A multi-chip module and a fabricating method thereof are proposed, in which two or more chips are simultaneously integrated in a package unit and then connected to a printed circuit board for providing a manifold level of functionality and data storage capacity. The multi-chip module includes at least a first chip and a second chip, wherein the second chip is connected to the first chip through chip-on-chip technology. Further, the first chip is mounted on a substrate through flip-chip technology. Then, the substrate is attached to a printed circuit board through surface-mount technology (SMT) Finally, at least one passive component is bonded to the printed circuit board at a position beside the substrate and directly beneath the second chip. This arrangement allows the use of a PCB having a smaller layout area for implementing the multi-chip module, making the resulted multi-chip module more compact in profile.

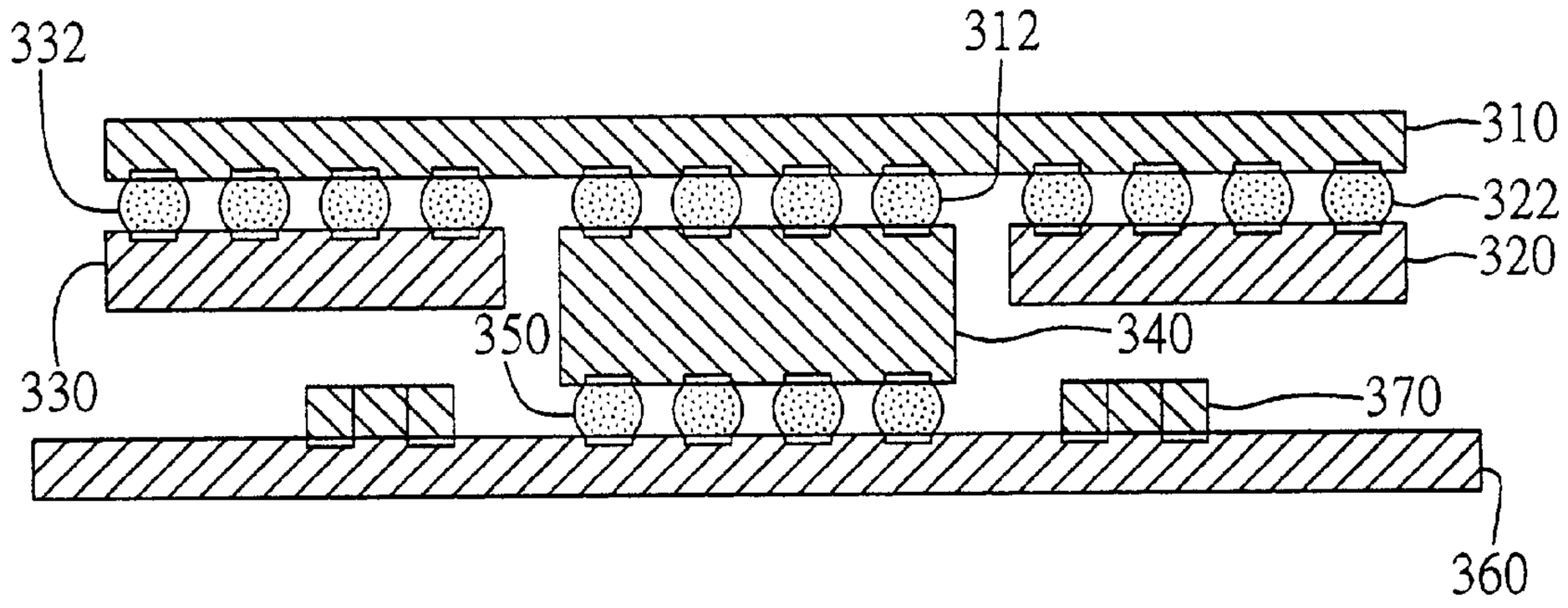


FIG. 1 (PRIOR ART)

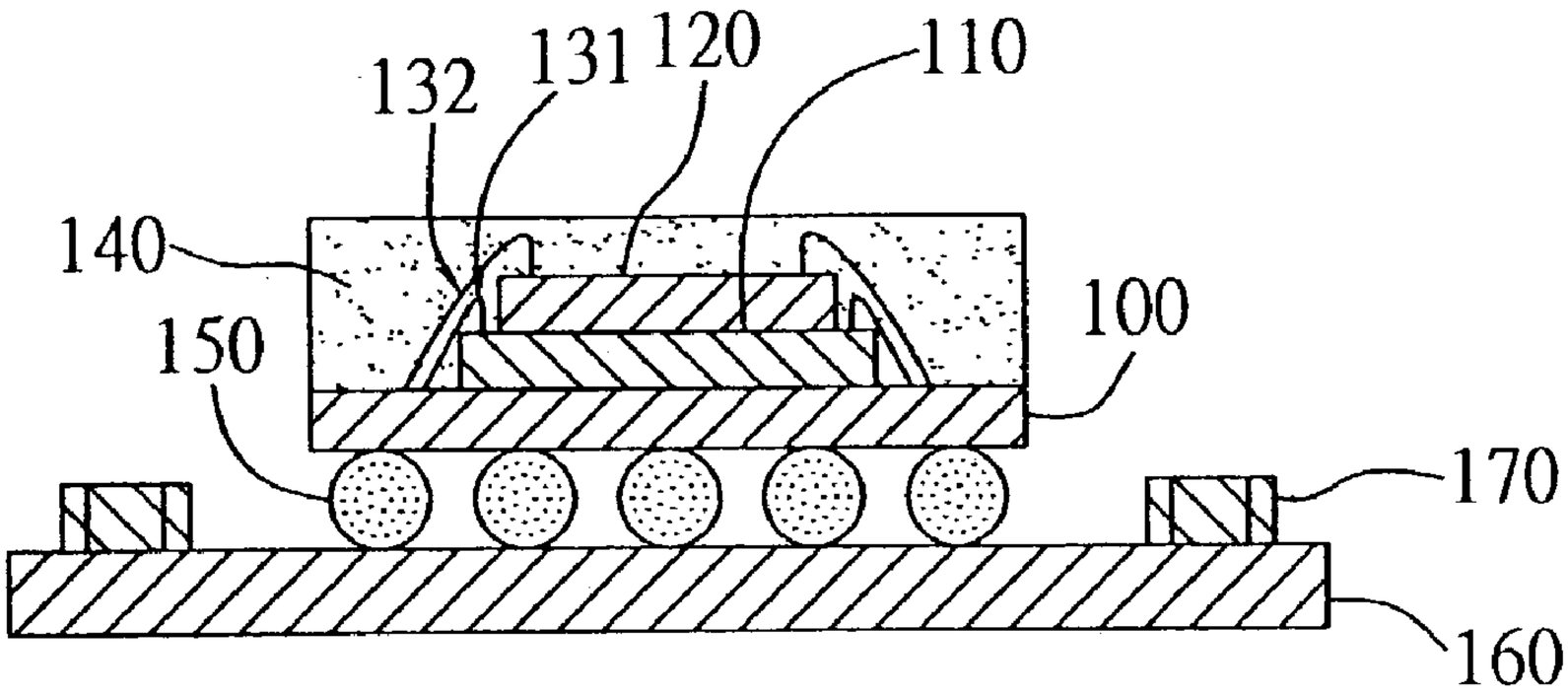


FIG. 2 (PRIOR ART)

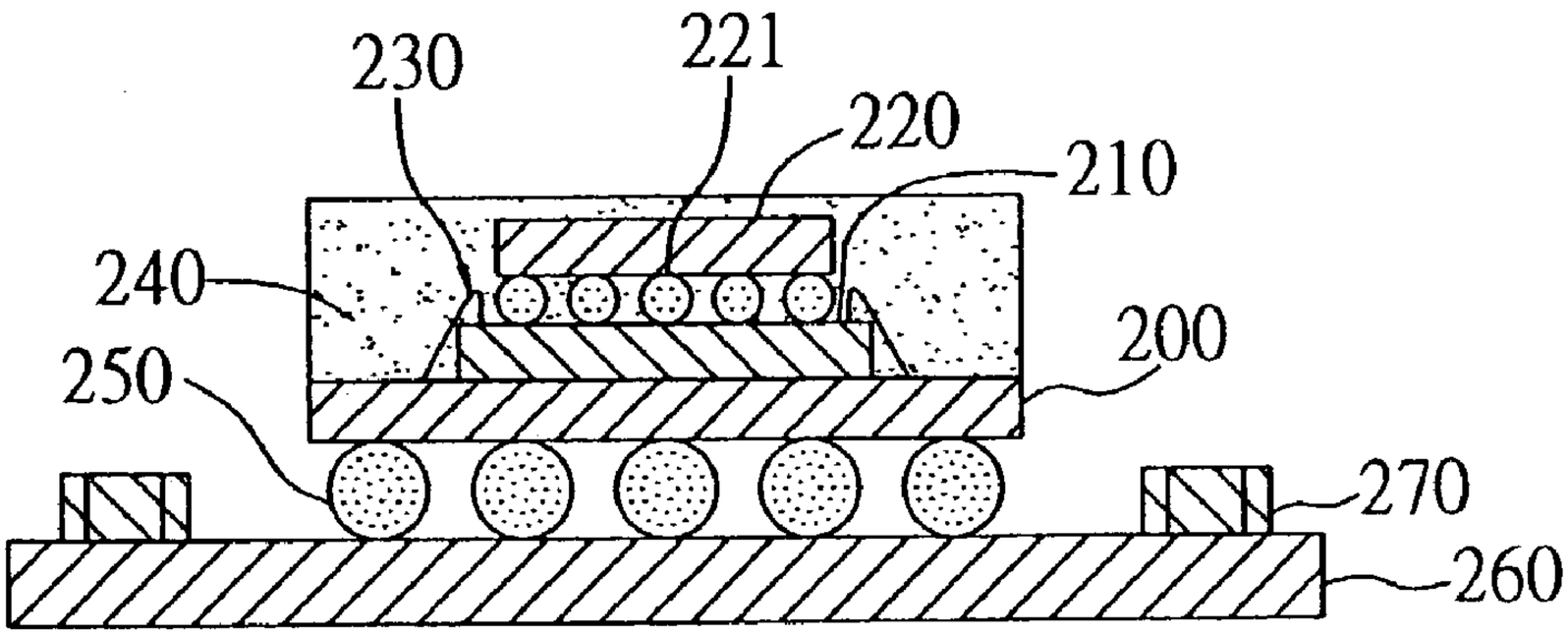
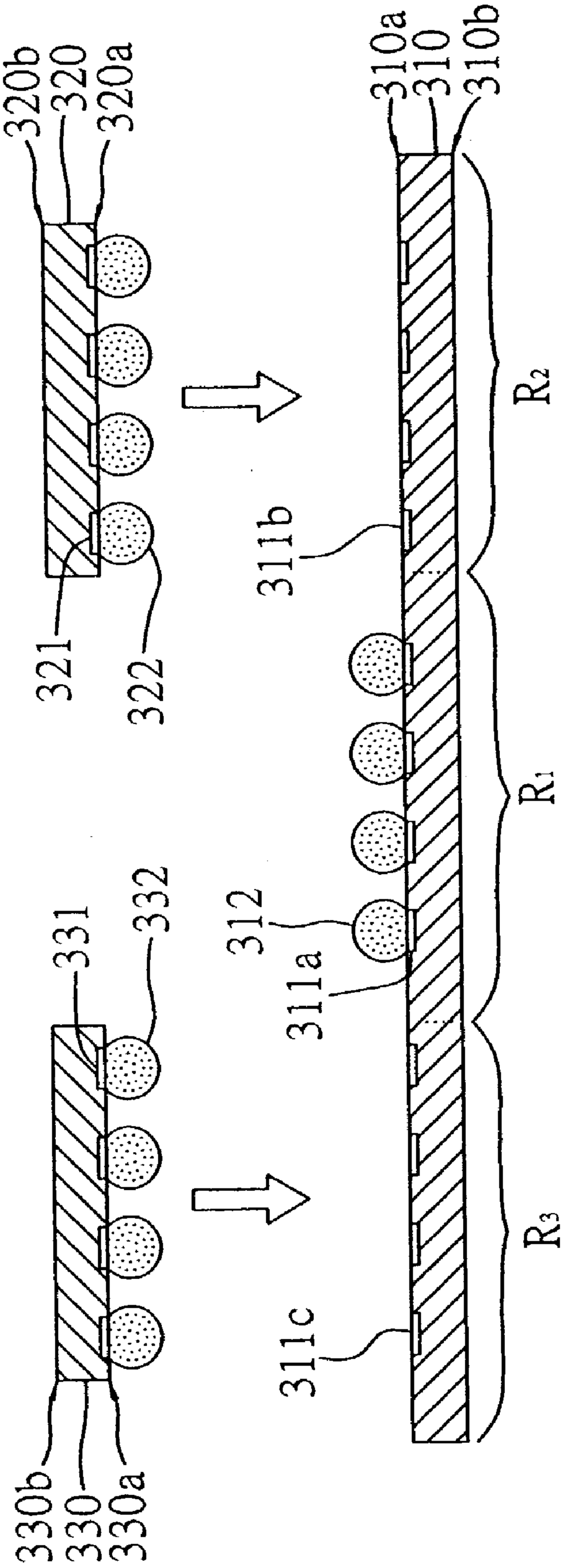


FIG. 3A


320b
320
320a
321
322
310a
310
310b
311b
R2
R1
331
332
312
311a
R3
330b
330
330a
311c

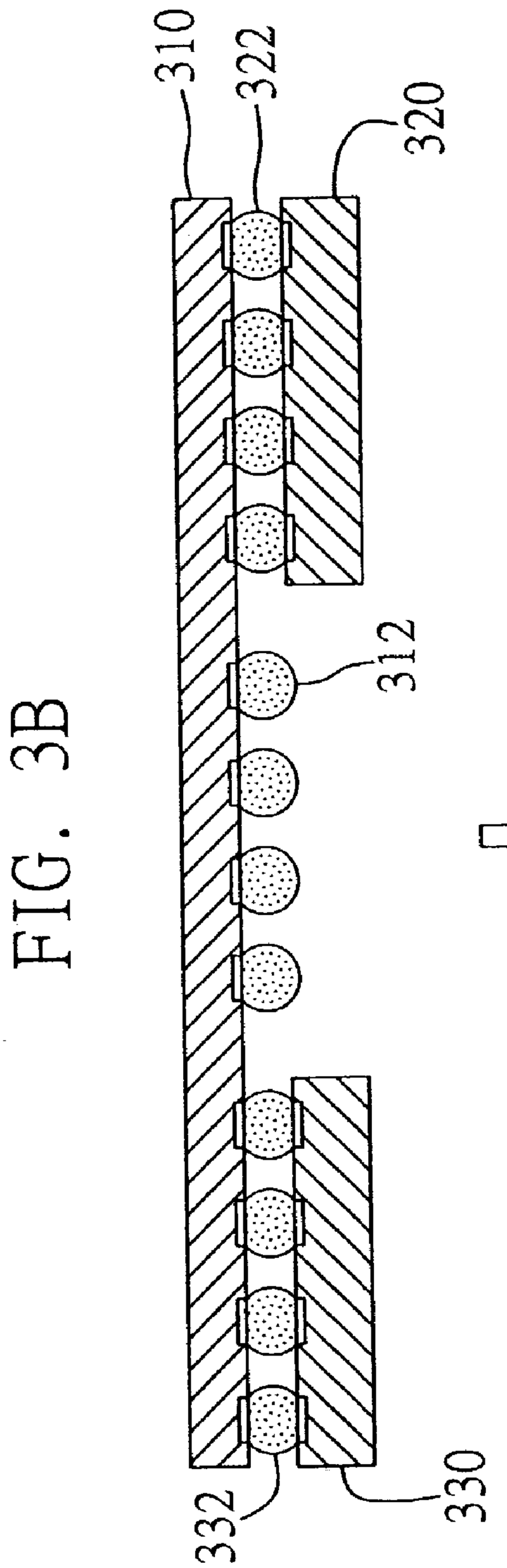
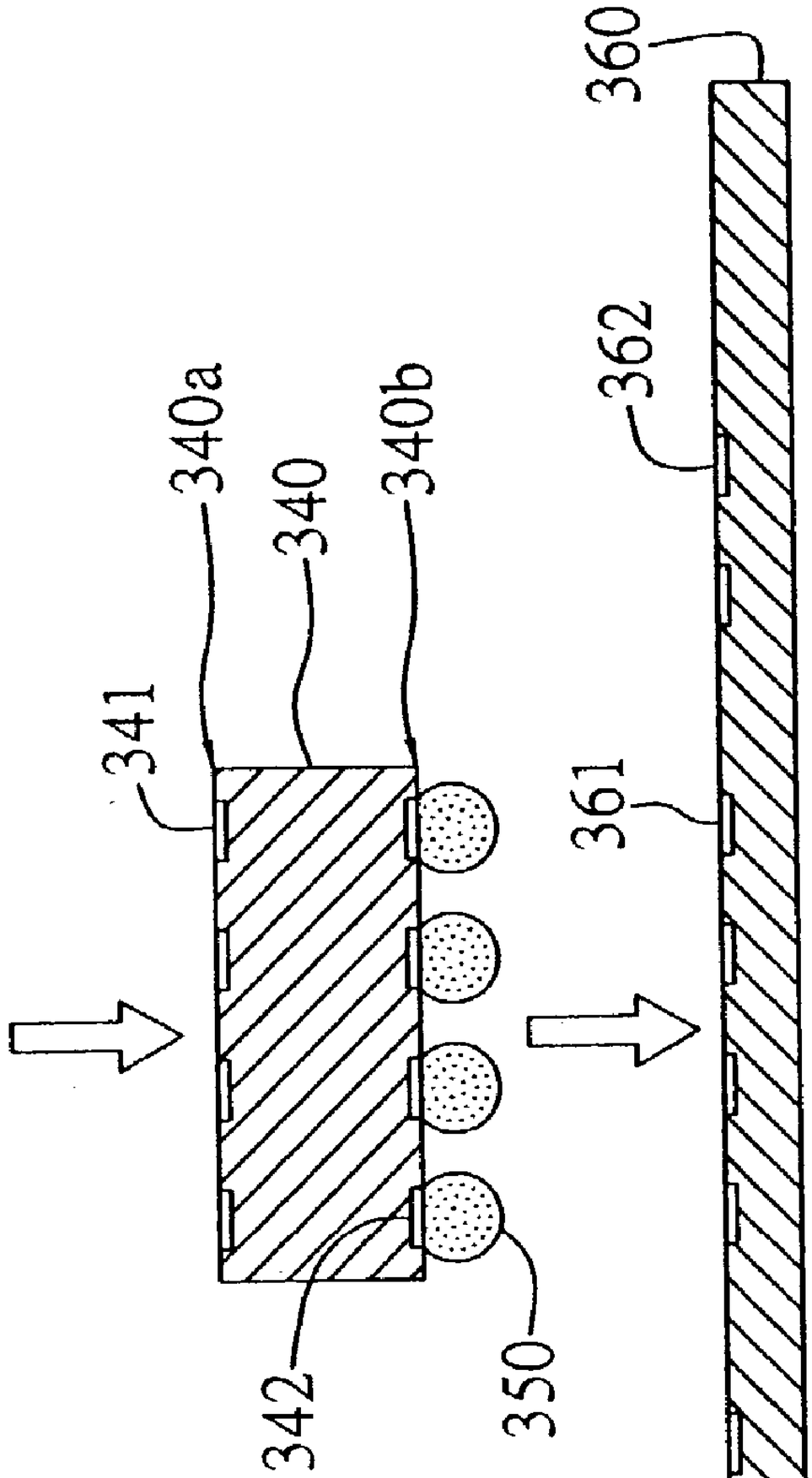


FIG. 3B



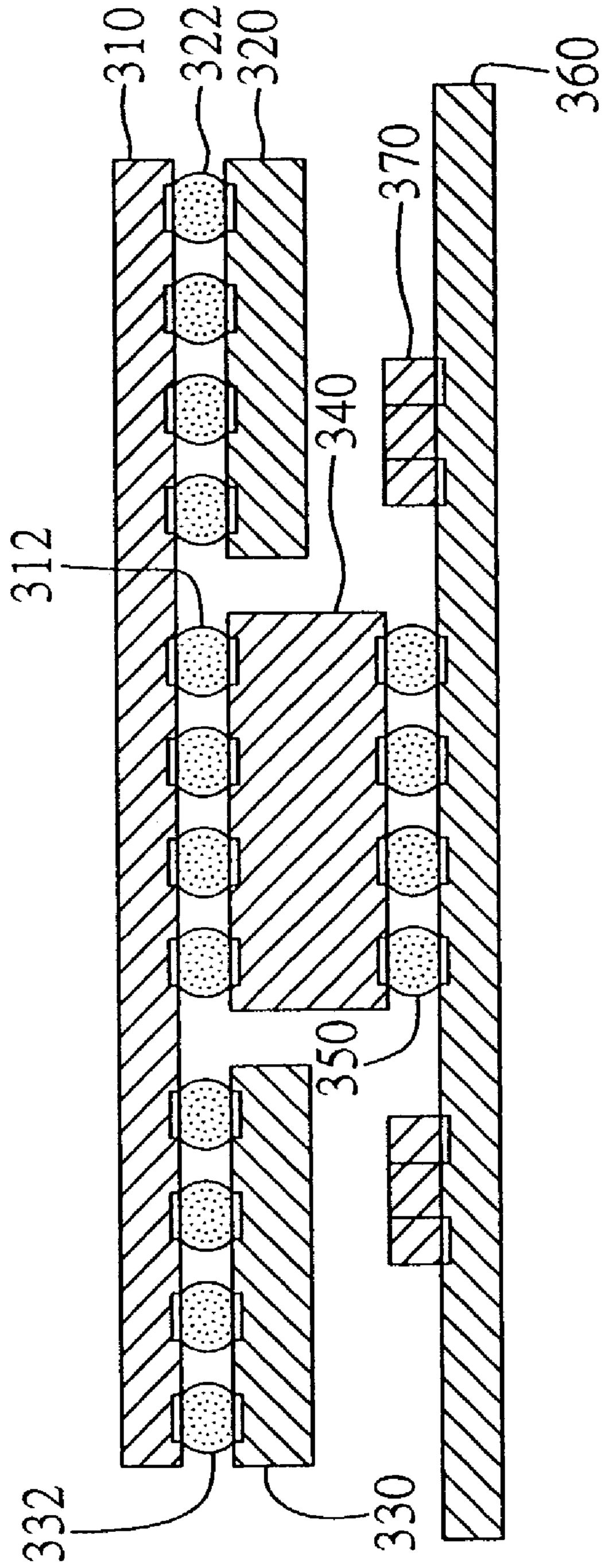


FIG. 3C

MULTI-CHIP MODULE AND FABRICATING METHOD THEREOF

FIELD OF THE INVENTION

[0001] The present invention relates to multi-chip modules and fabricating methods thereof, and more particularly, to a multi-chip module and a fabricating method thereof, in which two or more semiconductor chips are integrated in one single package unit for offering manifold increase in functionality or data storage capacity.

BACKGROUND OF THE INVENTION

[0002] Multi-chip module technology allows two or more semiconductor chips to be integrated in one single package unit and then connected to a printed circuit board for forming a multi-chip module, which is capable of offering a manifold level of functionality or data storage capacity. Similarly, a general memory module, such as a flash memory module, typically has two or more memory chips integrated in one single memory module for providing significant increase in data storage capacity.

[0003] Illustrated in **FIG. 1** and **FIG. 2** are two conventional multi-chip modules Referring to **FIG. 1, a** conventional multi-chip module is constructed based on a stacked dual-chip BGA (Ball Grid Array) semiconductor package, including: (a) a substrate **100**; (b) a first semiconductor chip **110** mounted on the substrate **100**; (c) a second semiconductor chip **120** stacked on the first semiconductor chip **110**, (d) a set of first bonding wires **131** for electrically connecting the first semiconductor chip **110** to the substrate **100**; (e) a set of second bonding wires **132** for electrically connecting the second semiconductor chip **120** to the substrate **100**; (f) an encapsulant **140** for encapsulating the two semiconductor chips **110**, **120**; and (g) ball grid array **150** implanted on a back side of the substrate **100** for mechanically bonding and electrically connecting the BGA package to a printed circuit board (PCB) **160**. After the BGA package is mounted on the PCB **160**, a plurality of passive components **170** are further bonded to predetermined positions on the PCB **160** beside the BGA package. This results in a dual-chip module.

[0004] **FIG. 2** shows another conventional multi-chip module constructed based on a dual-chip COC (Chip-On-Chip) BGA semiconductor package, including: (a) a substrate **200**; (b) a first semiconductor chip **210** mounted on the substrate **200**; (c) a second semiconductor chip **220** mounted on the first semiconductor chip **210** through a plurality of solder bumps **221** by using chip-on-chip (COC) technology; (d) a set of bonding wires **230** for electrically connecting the first semiconductor chip **210** to the substrate **200**; (e) an encapsulant **240** for encapsulating the two semiconductor chips **210**, **220**; and (g) ball grid array **250** implanted on a back side of the substrate **200** for mechanically bonding and electrically connecting the semiconductor package to a PCB **260**. After the semiconductor package is mounted on the PCB **260**, a plurality of passive components **270** are further bonded to predetermined positions on the PCB **260** beside the semiconductor package. This also results in a dual-chip module.

[0005] One common drawback to the foregoing two dual-chip modules, however, is that a relatively larger PCB is required for disposing the semiconductor package together with the associated passive components thereon, which undesirably makes the resulted dual-chip modules less compact in size.

[0006] Related patents include, for example, U.S. Pat. No. 5,646,828 entitled "THIN PACKAGING OF MULTI-CHIP MODULES WITH ENHANCED THERMAL/POWER MANAGEMENT", U.S. Pat. No. 5,477,082 entitled "BI-PLANAR MULTI-CUP MODULE"; and U.S. Pat. No. 5,784,261 entitled "MICROCHIP MODULE ASSEMBLIES", to name just a few.

[0007] The above patents, however, still have the foregoing drawback of making the resulted multi-chip module less compact in size Therefore, it is desired to construct a multi-chip module more miniaturized in profile.

SUMMARY OF THE INVENTION

[0008] A primary objective of the present invention is to provide multi-chip module and a fabricating method thereof, in which the multi-chip module can be made more compact in size while allowing high density of integration.

[0009] In accordance with the foregoing and other objectives, the invention proposes a new multi-chip module and a fabricating method thereof

[0010] The fabricating method of the invention is firstly to prepare a first semiconductor chip and at least one second semiconductor chip, wherein the first semiconductor chip is larger in area size than the second semiconductor chip and is partitioned at least into a first connecting region and a second connecting region. The multi-chip module constructed according to the invention can contain two, three, four or more chips, depending on the area size of the first semiconductor chip.

[0011] With the use of chip-on-chip (COC) technology, the second chip is mounted on the second connecting region of the first semiconductor chip. Subsequently, the first connecting region of the first semiconductor chip is disposed on an upper surface of a substrate by using flip-chip technology. Then, the substrate has a lower surface attached to a printed circuit board through surface-mount technology (SMT). Moreover, at least one passive component is bonded to the printed circuit board (PCB) at a predetermined position beside the substrate and directly beneath the second semiconductor chip. This arrangement allows a PCB having a smaller layout area to be used in the invention, making the resulted multi-chip module more compact in size than the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The invention can be more fully understood by reading the following detailed description of the preferred embodiments, with reference made to the accompanying drawings, wherein:

[0013] **FIG. 1** (PRIOR ART) is schematic sectional diagram of a conventional multi-chip module, **FIG. 2** (PRIOR ART) is a schematic sectional diagram of another conventional multi-chip module; and

[0014] FIGS. **3**A-**3**C are schematic sectional diagrams used to depict the steps involved in the fabricating method of the multi-chip module of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0015] Illustrated in FIGS. **3**A-**3**B are the steps involved in the fabricating method of the multi-chip module of one preferred embodiment according to the invention. In this embodiment, fabrication of a triple-chip module of the invention is demonstrated; however, it is to be noted that the invention can also be used to fabricate a dual-chip module or a multi-chip module having four or more semiconductor chips.

[0016] Referring first to **FIG. 3**A, as fabrication of a triple-chip module is illustrated in this embodiment, the first step of the fabricating method is to prepare three semiconductor chips, including a first semiconductor chip **310**, a second semiconductor chip **320**, and a third semiconductor chip **330**.

[0017] The first semiconductor chip **310** has an active surface **310***a* and an inactive surface **310***b*, while the active surface **310***a* is partitioned into three regions. a first connecting region R**1**, a second connecting region R**2**, and a third connecting region R**3**. Further, on the active surface **310***a* there are formed a plurality of input/output (I/O) pads, including a first set of I/O pads **311***a* disposed in the first connecting region R**1**, a second set of I/O pads **311***b* disposed in the second connecting region R**2**, and a third set of I/O pads **311***c* disposed in the third connecting region R**3** Moreover, on the first set of I/O pads **311***a* there are mounted a plurality of solder bumps **312** used for subsequent flip-chip application. It is to be noted that the three connecting areas R**1**, R**2**, R**3** are defined on the active surface **310***a* of the first semiconductor chip **310** in correspondence with the triple-chip module being fabricated in this embodiment. However, the invention can further be applied to a multi-chip module containing two, four or more chips, depending on the area size of the first semiconductor chip **310**.

[0018] The second semiconductor chip **320** has an active surface **320***a* and an inactive surface **320***b*, while the active surface **320***a* is formed with a set of I/O pads **321** thereon. Further, on the I/O pads **321** there are mounted a plurality of solder bumps **322** used for subsequent COC application. The second semiconductor chip **320** is necessarily smaller in area size than the first semiconductor chip **310** and approximately equal in dimension to the second connecting region R**2** on the active surface **310***a* of the first semiconductor chip **310**.

[0019] The third semiconductor chip **330** has an active surface **330***a* and an inactive surface **330***b*, while the active surface **330***a* is formed with a set of I/O pads **331** thereon. Further, on the I/O pads **331** there are mounted a plurality of solder bumps **332** used for subsequent COC application. The third semiconductor chip **330** is necessarily smaller in area size than the first semiconductor chip **310** and approximately equal in dimension to the third connecting region R**3** on the active surface **310***a* of the first semiconductor chip **310**.

[0020] Referring further to **FIG. 3**B, with the use of COC technology, the second semiconductor chip **320** is integrated with the first semiconductor chip **310** by bonding the I/O pads **321** on the active surface **320***a* of the second semiconductor chip **320** through the solder bumps **322** to the second set of I/O pads **311***b* in the second connecting region R**2** on the active surface **310***a* of the first semiconductor chip **310**. Furthermore, the third semiconductor chip **330** can be similarly integrated with the first semiconductor chip **310** by bonding the I/O pads **331** on the active surface **330***a* of the third semiconductor chip **330** through the solder bumps **332** to the third set of I/O pads **311** c in the third connecting region R**3** on the active surface **310***a* of the first semiconductor chip **310**.

[0021] After completing the above COC process, the next step is to integrate the first semiconductor chip **310** with a substrate **340** through flip-chip technology. The substrate **340** can be a silicon substrate, an organic substrate or a ceramic substrate, which has an upper surface **340***a* and a lower surface **340***b*. The upper surface **340***a* is formed with a set of top contact pads **341**, while on the lower surface **340***b* there are formed a set of bottom contact pads **342**, which are electrically connected through a plurality of conductive traces and vias (not shown) to the top contact pads **341**. Further, the substrate **340** need to be approximately equal in area size to the first connecting region R**1** on the active surface **310***a* of the first semiconductor chip **310**, while the height of the substrate **340** should be greater than the total height of the second semiconductor chip **320** or the third semiconductor chip **330** plus subsequently-used passive components (shown in **FIG. 3C** by the reference numeral **370**).

[0022] With the use of flip-chip technology, the first semiconductor chip **310** is mounted on the substrate **340** in such a manner that the first set of I/O pads **311***a* in the first connecting region R**1** on the active surface **310***a* of the first semiconductor chip **310** are bonded through the solder bumps **312** to the top contact pads **341** on the upper surface **340***a* of the substrate **340**.

[0023] The next step is to connect the substrate **340** to a printed circuit board (PCB) **360** having a set of contact pads **361** and a plurality of passive-component bond pads **362** through surface-mount technology (SMT).

[0024] Referring further to **FIG. 3**C, with the use of the SMT process, the substrate **340** is mounted on the PCB **360** in such a manner that the bottom contact pads **342** on the lower surface **340***b* of the substrate **340** are bonded through ball grid array **350** to the contact pads **361** on the PCB **360**. Finally, a plurality of passive components **370** are bonded to the passive-component bond pads **362** on the PCB **360**. This completes the fabrication of the multi-chip module of the invention.

[0025] As comparing **FIG. 3C** with **FIG. 1** and **FIG. 2**, the invention is characterized by mounting the passive components **370** on the PCB **360** at positions beside the substrate **340** and directly beneath the second semiconductor chip **320** and the third semiconductor chip **330**, which allows the multi-chip module to be implemented with the use of a PCB having a smaller layout area, and thus the resulted multi-chip module can be made more compact in size. The invention is therefore more advantageous to use than the prior art.

[0026] The invention has been described using exemplary preferred embodiments. However, it is to be understood that the scope of the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements. The scope of the claims, therefore, should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. A multi-chip module, comprising:

(a) a first semiconductor chip having an active surface and an inactive surface, wherein the active surface is partitioned at least into a first connecting region and a second connecting region;

(b) a second semiconductor chip having an active surface and an inactive surface, and mounted on the second connecting region of the first semiconductor chip through chip-on-chip technology;

(c) a substrate having an upper side and a lower side, wherein the upper side is used for mounting the first connecting region of the first semiconductor chip thereon through flip-chip technology, and the substrate has a predetermined height larger than the thickness of the second semiconductor chip; and

(d) a printed circuit board for mounting the substrate thereon through surface-mount technology.

2. The multi-chip module of claim 1, further comprising:

at least one passive component bonded to the printed circuit board at a predetermined position beside the substrate and beneath the second semiconductor chip.

3. The multi-chip module of claim 1, wherein the first and second semiconductor chips are memory chips.

4. The multi-chip module of claim 1, wherein the substrate is a silicon-made substrate.

5. The multi-chip module of claim 1, wherein the substrate is an organic substrate.

6. The multi-chip module of claim 1, wherein the substrate is a ceramic substrate.

7. A multi-chip module, comprising:

(a) a first semiconductor chip having an active surface and an inactive surface, wherein the active surface is partitioned into a first connecting region, a second connecting region, and a third connecting region;

(b) a second semiconductor chip having an active surface and an inactive surface, wherein the active surface is mounted on the second connecting region of the first semiconductor chip through chip-on-chip technology;

(c) a third semiconductor chip having an active surface and an inactive surface, wherein the active surface is mounted on the third connecting region of the first semiconductor chip through chip-on-chip technology;

(d) a substrate having an upper side and a lower side, wherein the upper side is used for mounting the first connecting region of the first semiconductor chip thereon through flip-chip technology, and the substrate has a predetermined height larger than the overall thickness of the second semiconductor chip or the third semiconductor chip; and

(e) a printed circuit board for mounting the substrate thereon through surface-mount technology

8. The multi-chip module of claim 7, further comprising:

at least one passive component bonded to the printed circuit board at a predetermined position beside the substrate and beneath the second semiconductor chip or the third semiconductor chip.

9. The multi-chip module of claim 7, wherein the first, second, and third semiconductor chips are memory chips.

10. The multi-chip module of claim 7, wherein the substrate is a silicon-made substrate

11. The multi-chip module of claim 7, wherein the substrate is an organic substrate.

12. The multi-chip module of claim 7, wherein the substrate is a ceramic substrate.

13. A fabricating method of a multi-chip module, comprising the steps of:

(1) preparing a first semiconductor chip, a second semiconductor chip, and a third semiconductor chip;

wherein the first semiconductor chip has an active surface and an inactive surface, with the active surface being partitioned into a first connecting region, a second connecting region, and a third connecting region; the second semiconductor chip has an active surface and an inactive surface; and the third semiconductor chip has an active surface and an inactive surface;

(2) mounting the active surface of the second semiconductor chip and the active surface of the third semiconductor chip respectively on the second connecting region and the third connecting region of the first semiconductor chip through chip-on-chip technology;

(3) mounting the first connecting region of the first semiconductor chip on a substrate through flip-chip technology; and

(4) mounting the substrate on a printed circuit board through surface-mount technology.

14. The fabricating method of claim 13, further comprising the step of:

bonding at least one passive component to the printed circuit board at a predetermined position beside the substrate and beneath the second semiconductor chip or the third semiconductor chip.

15. The fabricating method of claim 13, wherein in the step **(1)**, the first, second, and third semiconductor chips are memory chips.

16. The fabricating method of claim 13, wherein in the step **(1)**, the substrate is a silicon-made substrate.

17. The fabricating method of claim 13, wherein in the step **(1)**, the substrate is an organic substrate.

18. The fabricating method of claim 13, wherein in the step **(1)**, the substrate is a ceramic substrate.

* * * * *