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Sim et al.

(54) **NEGATIVE VOLTAGE GENERATOR FOR A SEMICONDUCTOR MEMORY DEVICE**

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(57) **ABSTRACT**

A negative voltage generator is controlled responsive to a word line precharge signal. Voltage fluctuations in a negatively biased word line scheme are reduced by using a kicker circuit to provide a predetermined amount of negative charge to shut off a word line during a precharge operation. The negative voltage generator includes first and second negative charge pumps. The second charge pump is activated responsive to the word line precharge signal. A negative voltage regulator can be used to regulate a negative voltage signal. A level shifter uses two voltage dividers and a differential amplifier to reduce response time, output ripple, and sensitivity to process and temperature variations. A negative voltage regulator cancels ripple from a charge pump to provide a stable negative bias voltage and reduce the amount of charge needed to precharge a word line.

30

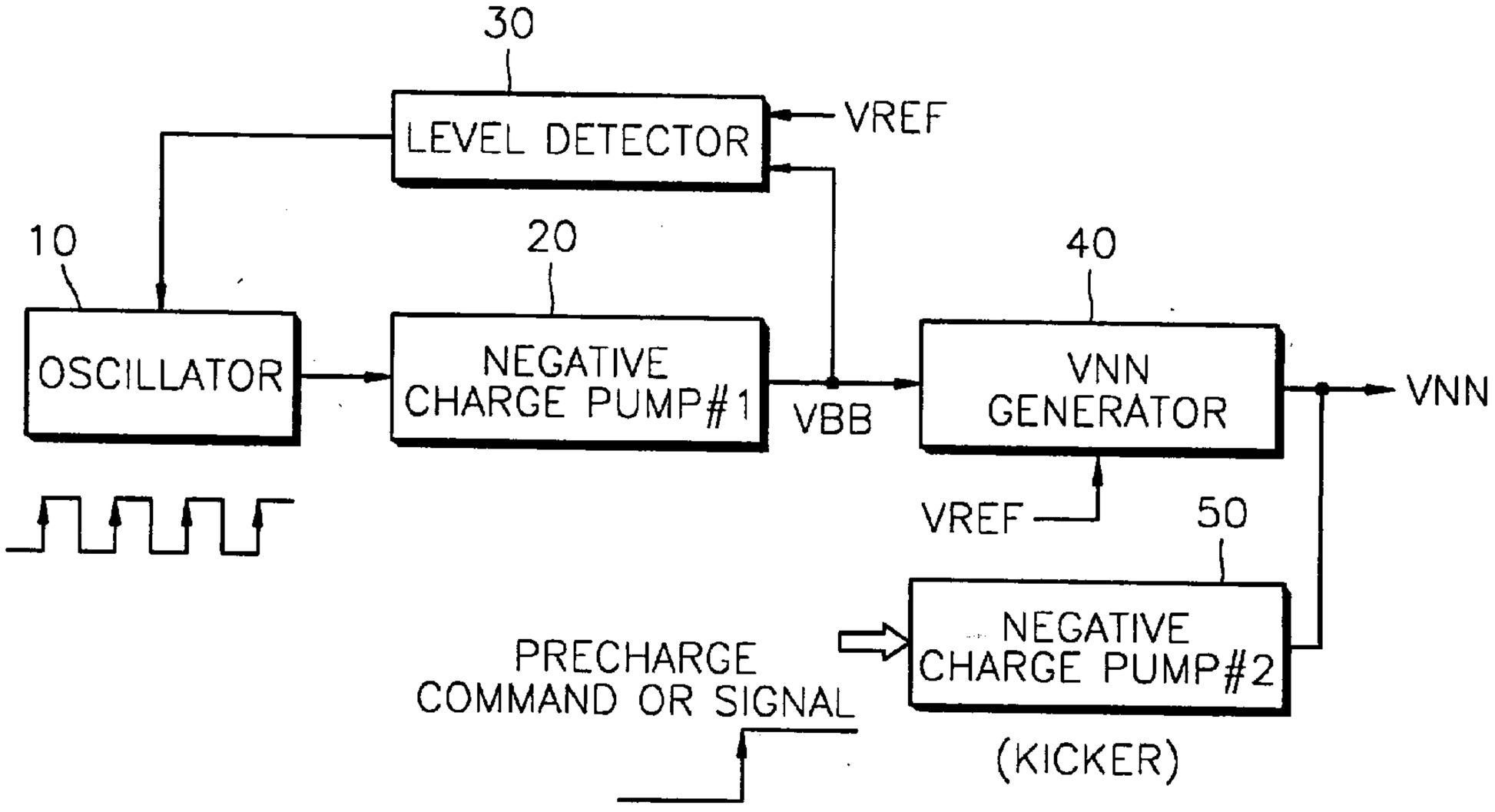


FIG. 1 (PRIOR ART)

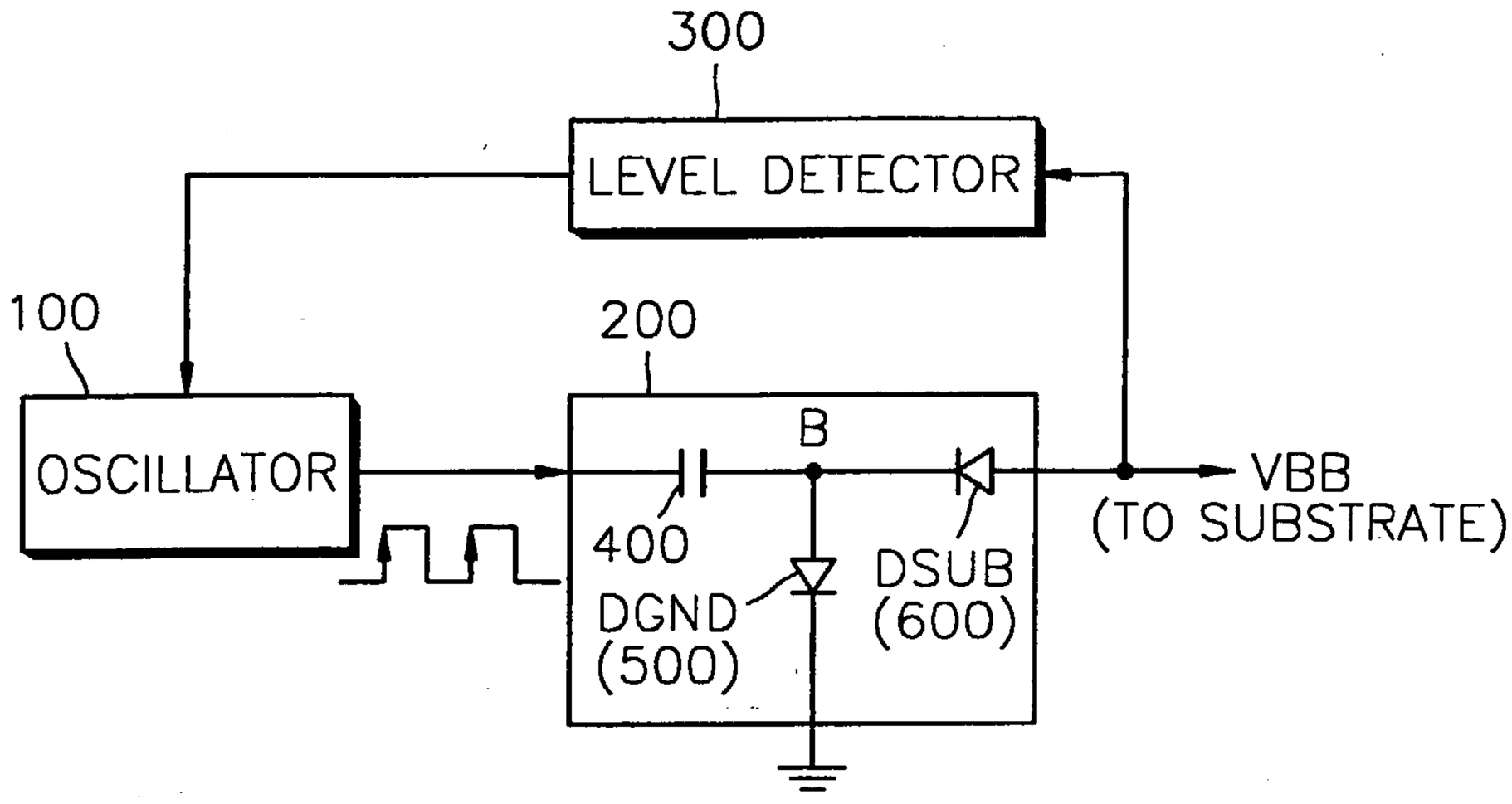
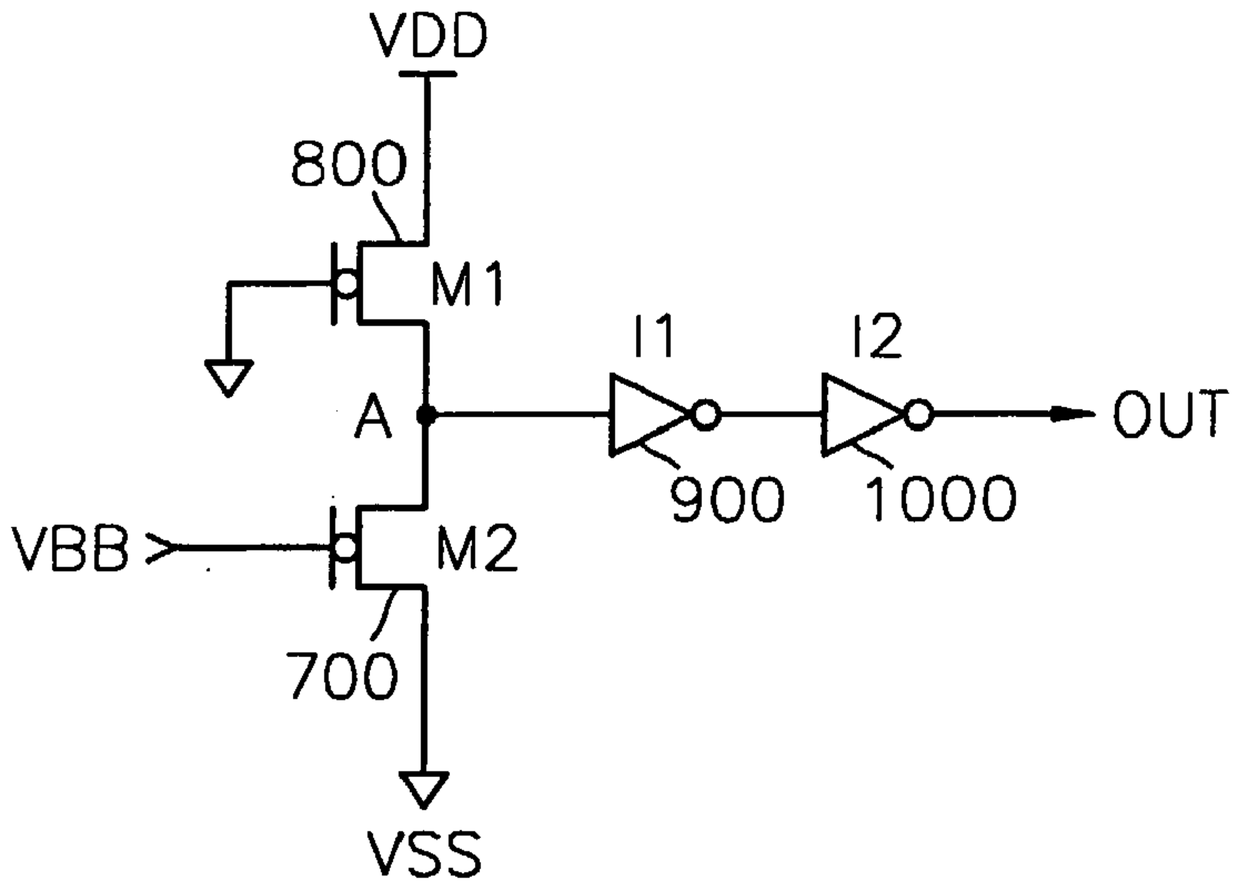


FIG. 2 (PRIOR ART)



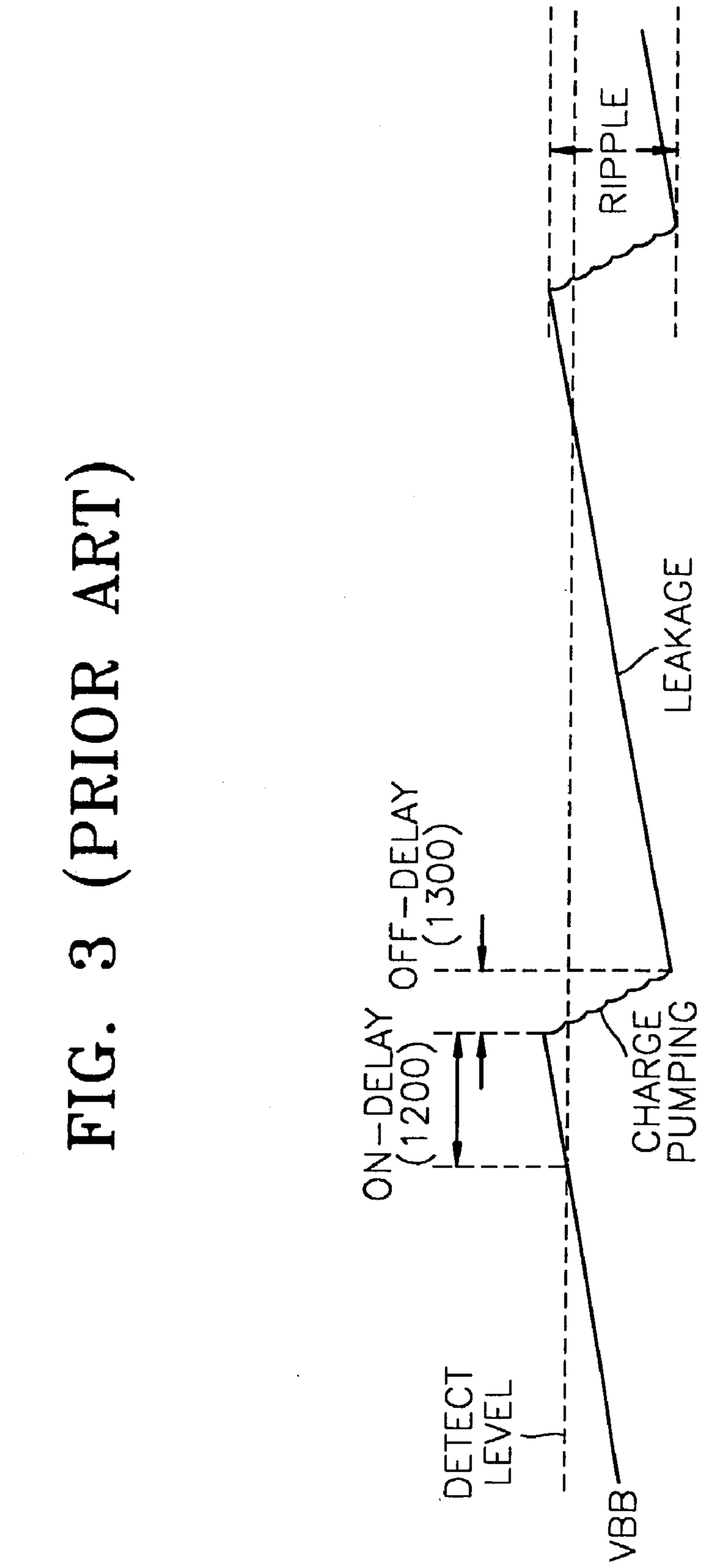


FIG. 3 (PRIOR ART)

FIG. 4

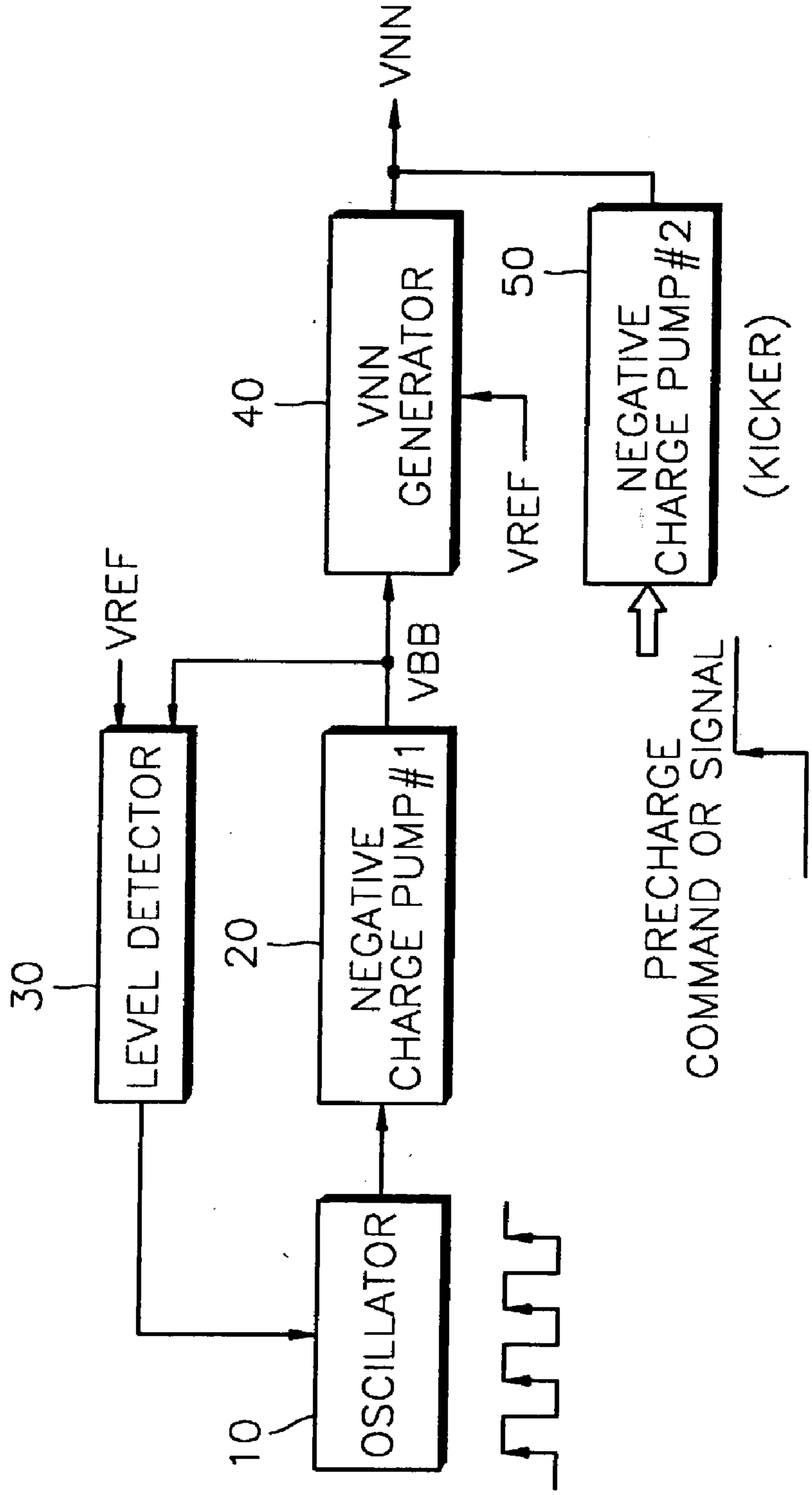

VNN
40
VNN GENERATOR
VREF
50
NEGATIVE CHARGE PUMP#2
(KICKER)
VREF
VBB
30
LEVEL DETECTOR
20
NEGATIVE CHARGE PUMP#1
10
OSCILLATOR
PRECHARGE COMMAND OR SIGNAL

FIG. 5

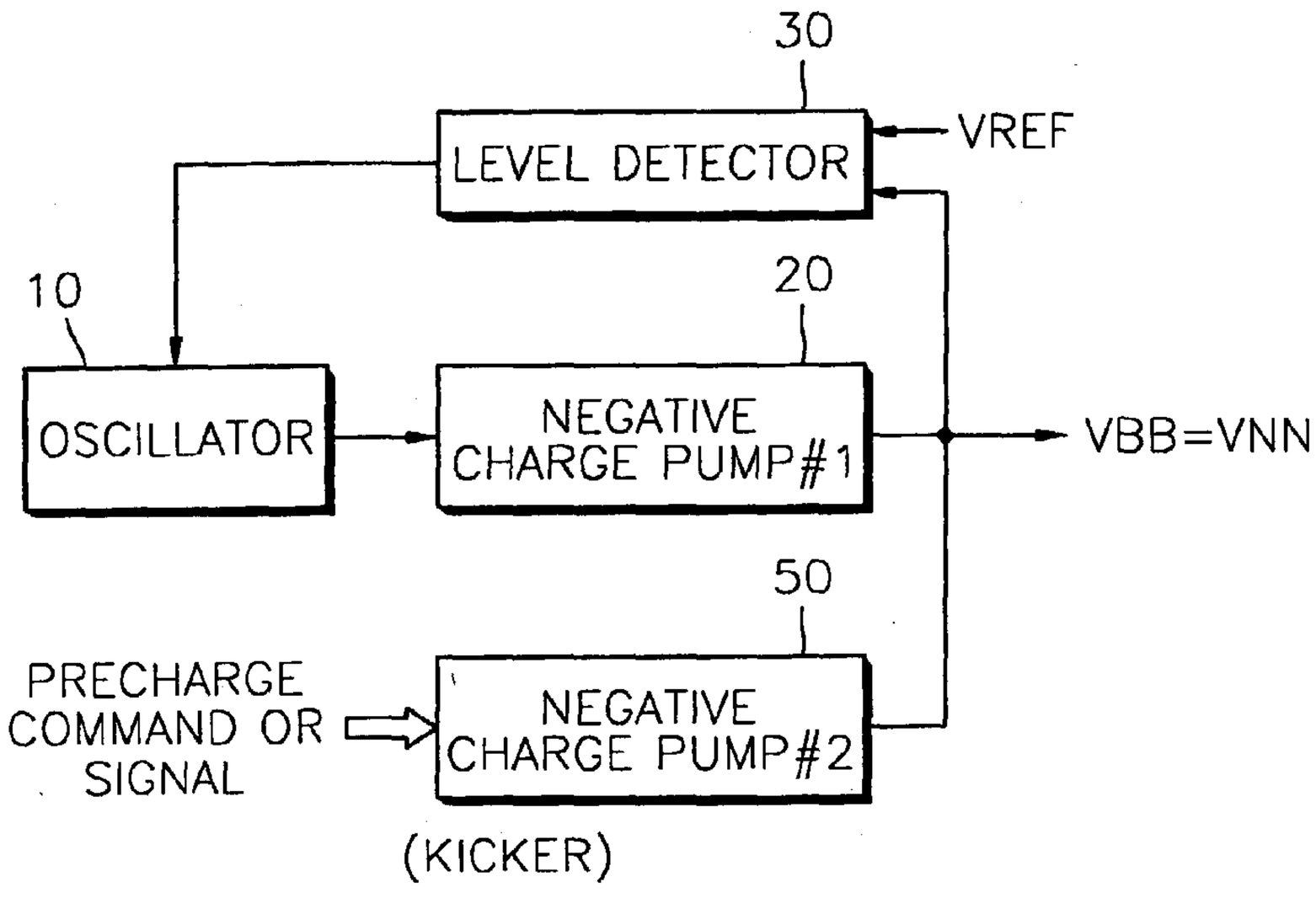

30
LEVEL DETECTOR
VREF
10
OSCILLATOR
20
NEGATIVE CHARGE PUMP#1
VBB=VNN
50
PRECHARGE COMMAND OR SIGNAL
NEGATIVE CHARGE PUMP#2
(KICKER)

FIG. 6

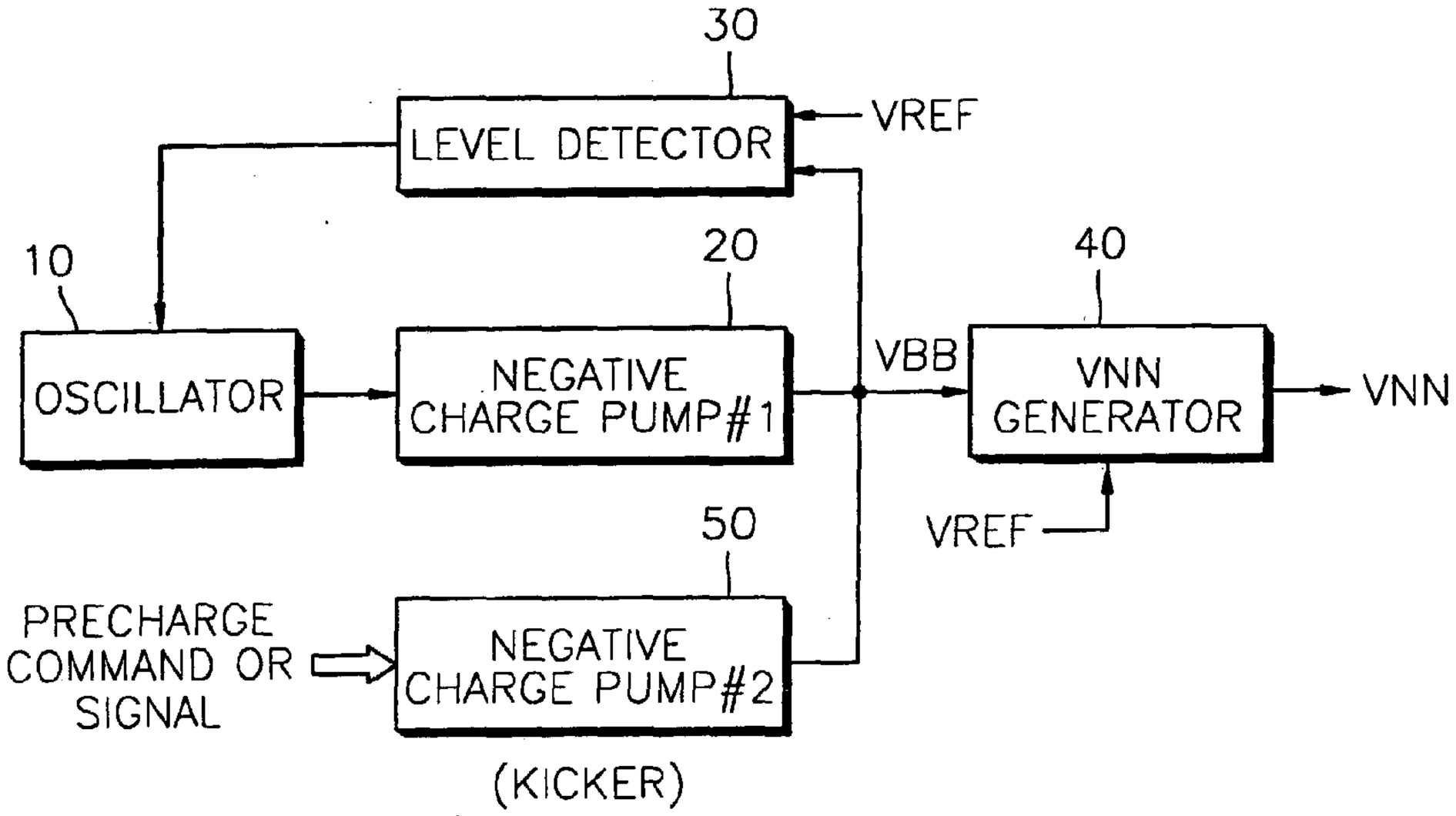

30
LEVEL DETECTOR
VREF
10
OSCILLATOR
20
NEGATIVE CHARGE PUMP#1
VBB
40
VNN GENERATOR
VNN
VREF
50
PRECHARGE COMMAND OR SIGNAL
NEGATIVE CHARGE PUMP#2
(KICKER)

FIG. 7

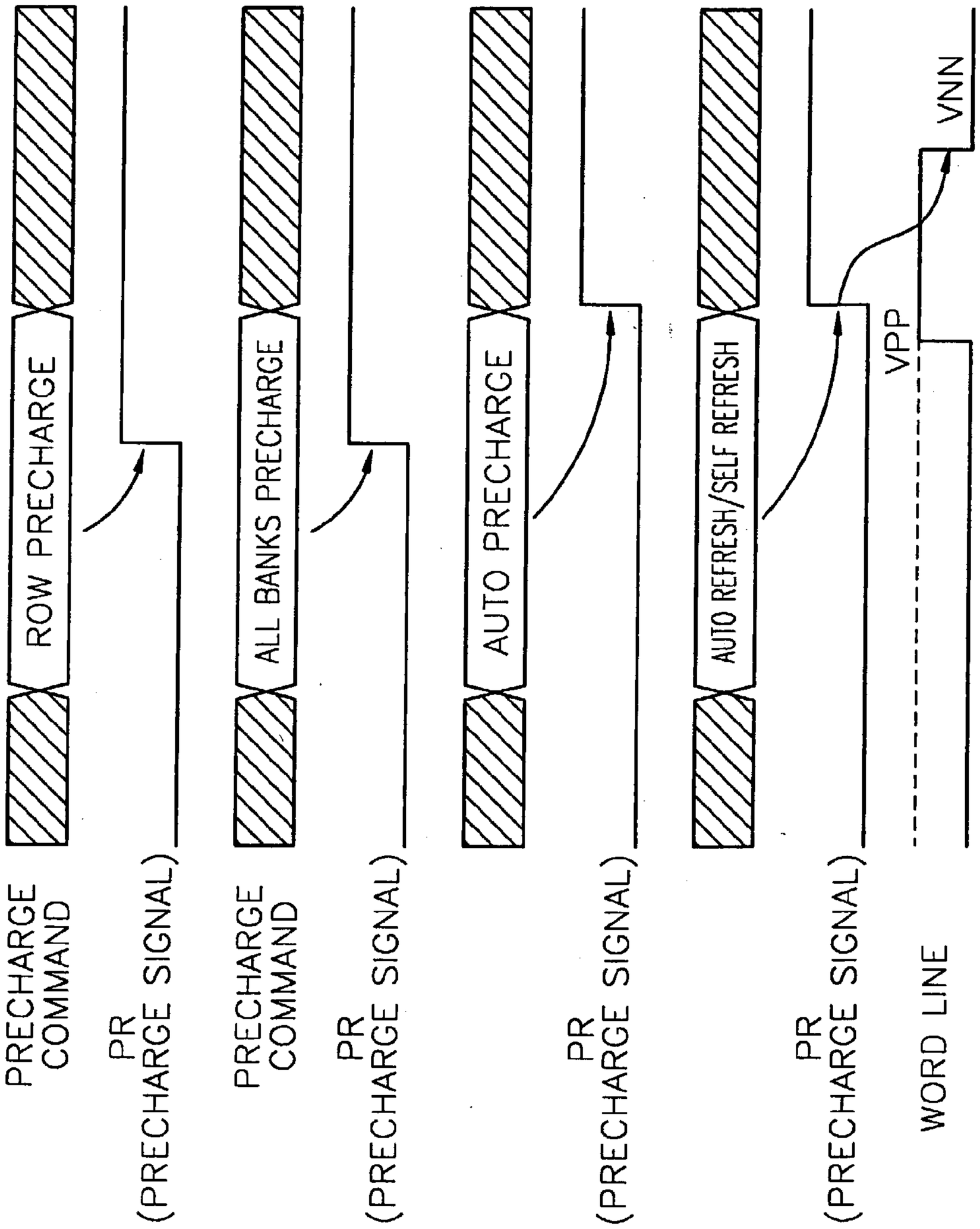

ROW PRECHARGE
ALL BANKS PRECHARGE
AUTO PRECHARGE
AUTO REFRESH/SELF REFRESH
VNN
VPP
PRECHARGE COMMAND
PR (PRECHARGE SIGNAL)
PRECHARGE COMMAND
PR (PRECHARGE SIGNAL)
PR (PRECHARGE SIGNAL)
PR (PRECHARGE SIGNAL)
WORD LINE

FIG. 8

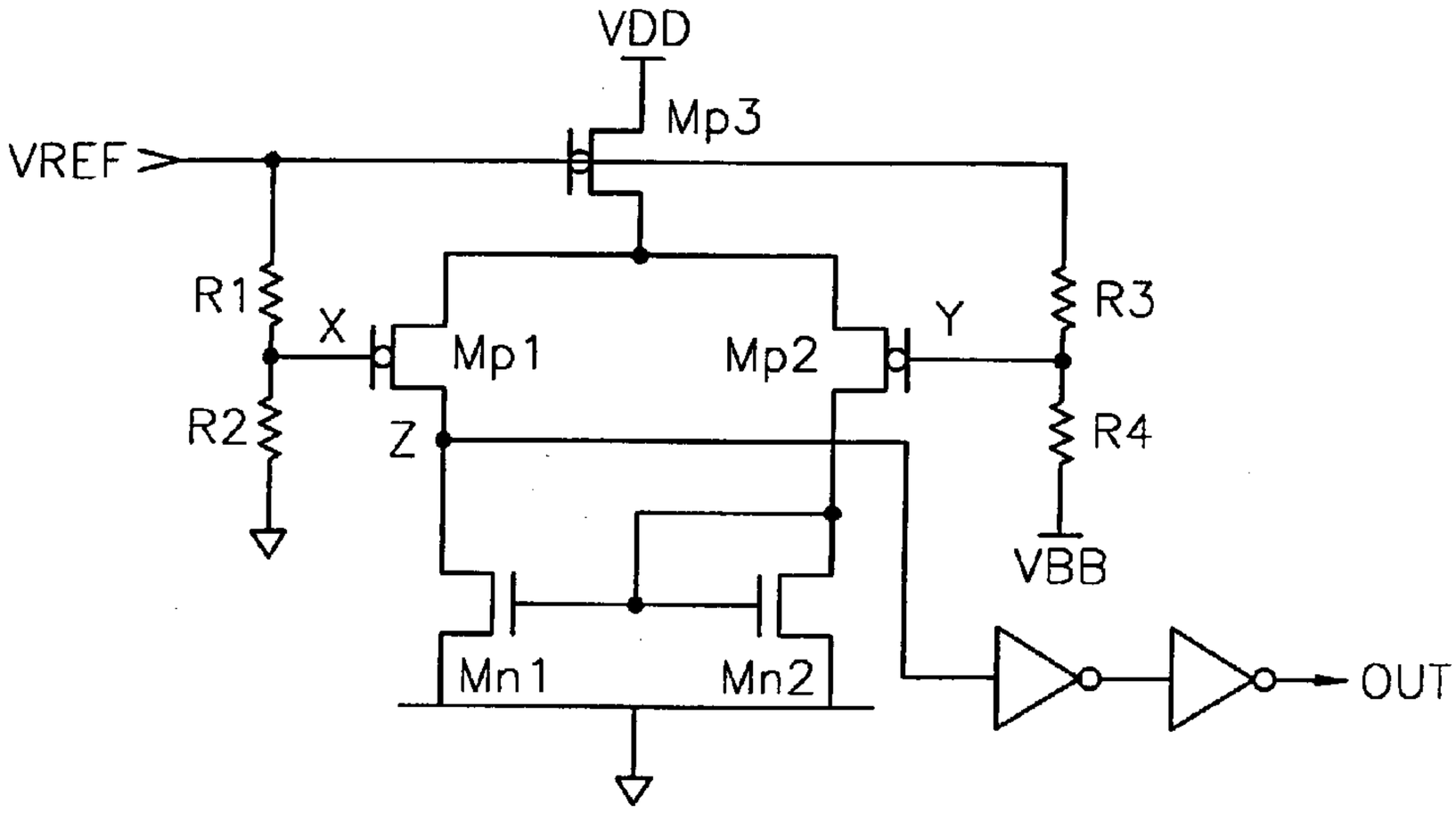

VDD
Mp3
VREF
R1
X
Mp1
Mp2
Y
R3
R2
Z
R4
VBB
Mn1
Mn2
OUT

FIG. 9

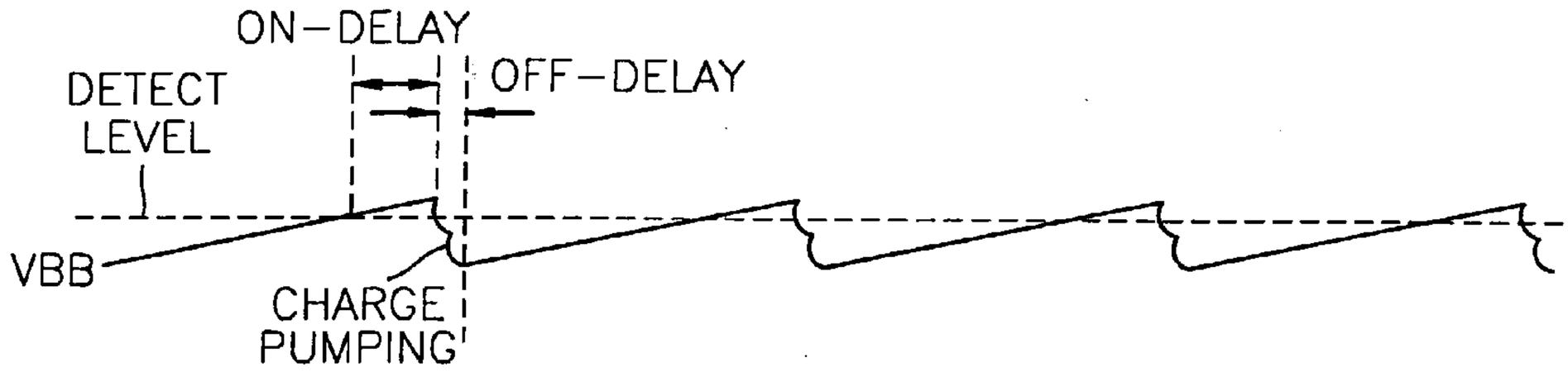

ON-DELAY
OFF-DELAY
DETECT
LEVEL
VBB
CHARGE
PUMPING

FIG. 10

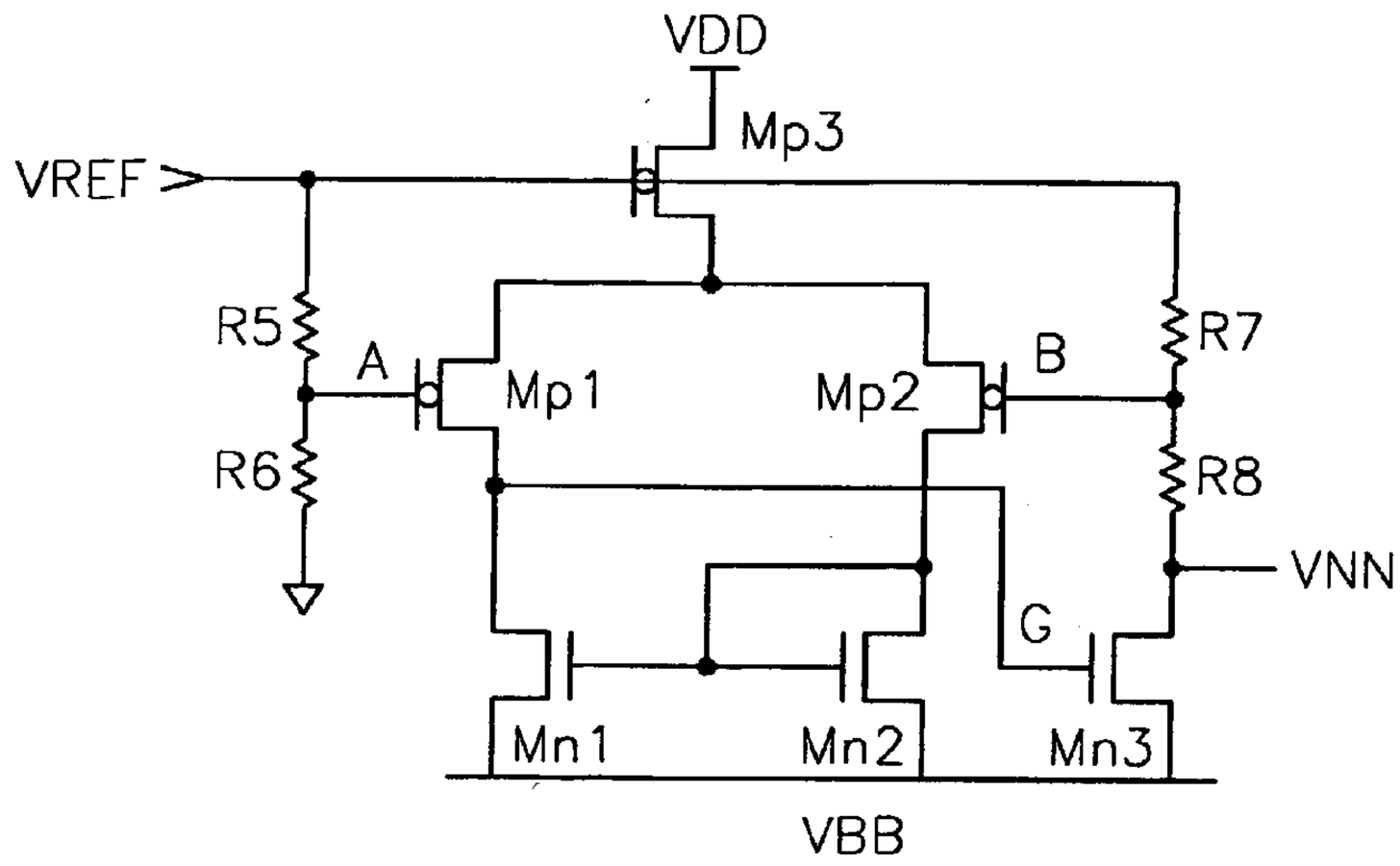
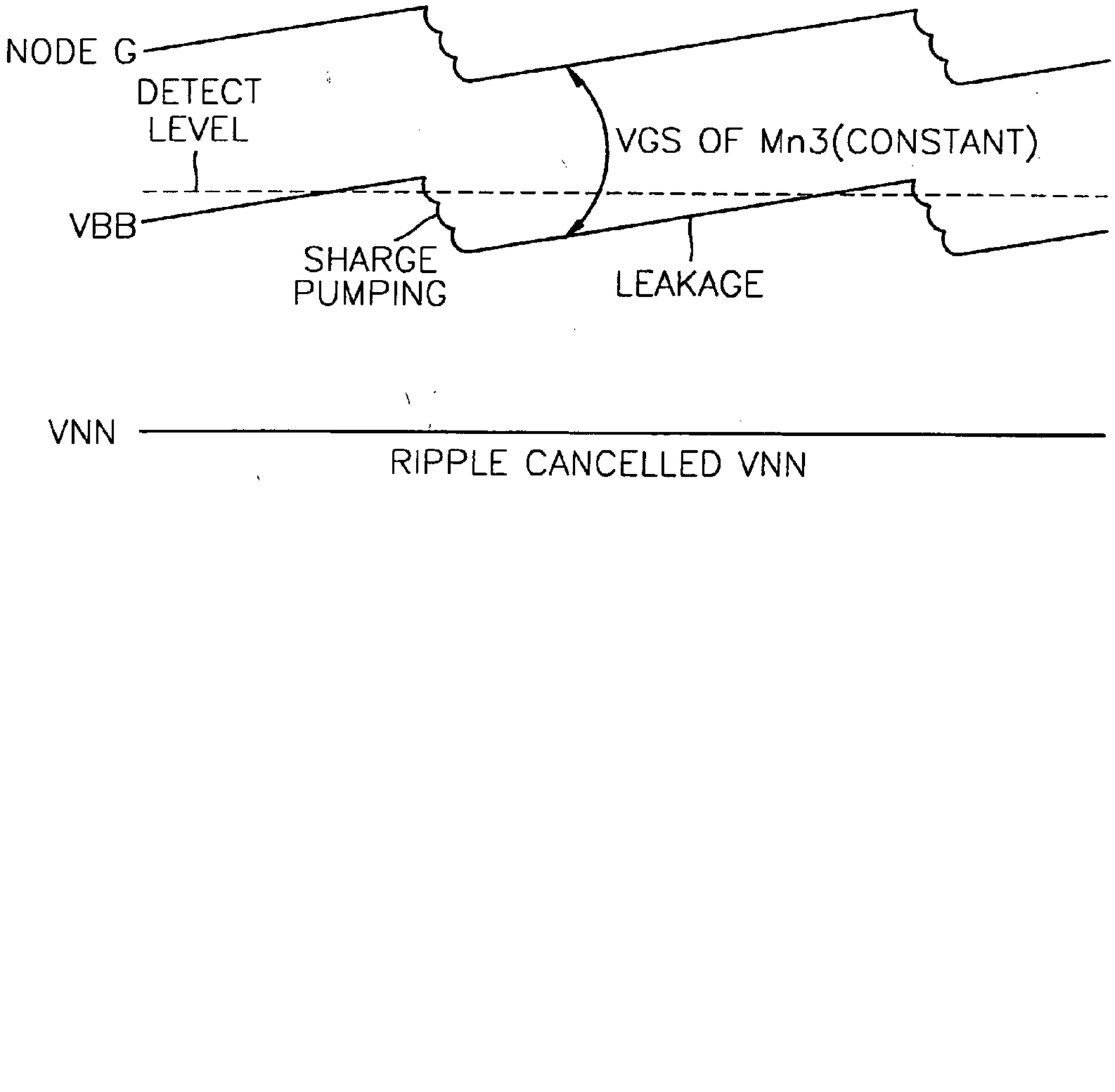

VDD
Mp3
VREF
R5
A
Mp1
Mp2
B
R7
R6
R8
VNN
G
Mn1
Mn2
Mn3
VBB

FIG. 11


NODE G
DETECT
LEVEL
VGS OF Mn3(CONSTANT)
VBB
SHARGE
PUMPING
LEAKAGE
VNN
RIPPLE CANCELLED VNN

NEGATIVE VOLTAGE GENERATOR FOR A SEMICONDUCTOR MEMORY DEVICE

[0001] This application is a divisional of U.S. patent application Ser. No. 09/901,930 filed on Jul. 9, 2001, now pending, which is herein incorporated by references in it's entirety.

BACKGROUND

[0002] 1. Field of the Invention

[0003] The present invention relates generally to semiconductor memory devices, and more particularly, to a negative voltage generator for a semiconductor memory device.

[0004] 2. Description of the Related Art

[0005] A typical semiconductor memory devices utilizes an access transistor in each memory cell to store, read and refresh data in the cell. The refresh time of a memory cell is degraded by the leakage current of the access transistor. A negatively biased word line scheme has been devised to reduce this leakage current. A memory device employing a negative word line scheme applies a negative voltage Vbb or Vnn to the word lines of non-selected memory cells. This is also referred to as back biasing the word line.

[0006] **FIG. 1** illustrates a prior art negative voltage generator which includes an oscillator **100**, a negative charge pump **200** and a level detector **300**. The generator of **FIG. 1** has commonly been used to generate a negative voltage (Vbb) for reverse biasing the substrate of a semiconductor device, thereby reducing leakage current. Thus, it is often referred to as a substrate voltage generator. It generates a regulated negative voltage supply using a negative feedback operation. When Vbb increases due to substrate leakage current, the detector **300** enables the oscillator **100** which then drives the charge pump **200**. The voltage of Vbb is driven more negative by the charge pump until the detector disables the oscillator.

[0007] **FIG. 2** illustrates a typical prior art Vbb level detector **300**. When Vbb increases due to substrate leakage current, the source-drain equivalent resistance of M2 **(700)** increases, thereby causing the voltage of Node A to rise. When node A reaches the trip point of inverter **900**, the output signal OUT goes high and enables the oscillator **100** which then drives the negative charge pump **200** with a rectangular wave signal. The negative charge pump includes a capacitor **400** and two diodes DGND **(500)** and DSUB **(600)** which are arranged in a typical negative charge pumping configuration. When the rectangular signal is high, node B is clamped at one threshold voltage (Vth) above ground by DGND, while the other end of the capacitor **400** is charged to the positive supply voltage Vdd. Then, when the rectangular signal goes low, the capacitor pumps negative charge to Vbb through DSUB.

[0008] To implement a negatively biased word line scheme, the prior art negative voltage generator described above with reference to **FIGS. 1 and 2** has also been utilized to provide the negative bias for the word lines. However, this prior art generator is not very well suited for driving negative word lines. The regulator shown in **FIGS. 1 and 2** was originally intended to provide a small amount of current for reverse or back biasing a semiconductor substrate. A negative word line scheme, however, requires large current drive capability to discharge a word line from a boosted voltage of Vpp to the negative voltage of Vbb or Vnn during a word line precharge operation. These large discharge currents cause fluctuations in the negative voltage supply. The drive circuitry for a negative word line scheme places additional demands on the negative voltage generator because it consumes additional operating current from the negative voltage supply.

[0009] Another problem with the prior art negative voltage generator is that the voltage gain of the detector **300** is very low (~0.1), so the response time is slow. This causes a long on/off delay time (~1 us) which results in a large ripple component in the negative voltage Vbb as shown in **FIG. 3**. A further problem with the detector is that it is highly sensitive to process and temperature variations.

SUMMARY

[0010] A negative voltage generator in accordance with the present invention is controlled responsive to a word line precharge signal.

[0011] One aspect of the present invention is a negative voltage generator for a semiconductor memory device comprising: a first charge pump having an output; and a second charge pump having an output coupled to the output of the first charge pump, wherein the second charge pump is adapted to be controlled by a word-line precharge signal. Another aspect is a method for operating a semiconductor memory device comprising controlling a negative voltage generator responsive to a word line precharge signal.

[0012] Another aspect of the present invention is a level detector for a semiconductor device comprising: a differential amplifier having a first input and a second input; a first voltage divider coupled to the first input of the differential amplifier; and a second voltage divider coupled to the second input of the differential amplifier, and adapted to drive the second input of the differential amplifier responsive to an output signal. Another aspect is a method for detecting a voltage in a semiconductor device comprising: dividing a reference signal, thereby generating a first divided signal; dividing the voltage, thereby generating a second divided signal; and amplifying the difference between the first and second divided signals.

[0013] A further aspect of the present invention is a negative voltage regulator for a semiconductor device comprising: a differential amplifier having a first input, a second input, and an output; an output transistor coupled to the output of the differential amplifier; a first voltage divider coupled to the first input of the differential amplifier; and a second voltage divider coupled to the second input of the differential amplifier, and adapted to drive the second input of the differential amplifier responsive to an output signal from the output transistor. Another aspect is a method for generating a first negative voltage in a semiconductor device comprising: generating a second negative voltage; dividing a reference signal, thereby generating a first divided signal; dividing the first negative voltage, thereby generating a second divided signal; amplifying the difference between the first and second divided signals, thereby generating a drive signal; and driving an output transistor coupled between the first negative voltage and the second negative voltage responsive to the drive signal.

[0014] Yet another aspect of the present invention is a semiconductor memory device having a negative word line scheme comprising a negative voltage generator comprising: a charge pump adapted to generate a first negative voltage, and a negative voltage regulator coupled to the negative charge pump and adapted to generate a second negative voltage by regulating the first negative voltage. Another aspect is a method for driving a word line in a semiconductor memory device having a negative word line scheme comprising: generating a first negative voltage; generating a second negative voltage by regulating the first negative voltage; and driving the word line with the second negative voltage.

[0015] These and other aspects of the present invention are disclosed and claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] **FIG. 1** is a diagram of a prior art negative voltage generator.

[0017] **FIG. 2** is a schematic diagram of a prior art level detector.

[0018] **FIG. 3** illustrates the operation of a prior art negative voltage generator and level detector.

[0019] **FIG. 4** is a diagram of an embodiment of a negative voltage generator in accordance with the present invention.

[0020] **FIG. 5** is a diagram of a second embodiment of a negative voltage generator in accordance with the present invention.

[0021] **FIG. 6** is a diagram of a third embodiment of a negative voltage generator in accordance with the present invention.

[0022] **FIG. 7** is a timing diagram of some example word line precharge commands and signals suitable for use with the present invention.

[0023] **FIG. 8** is a schematic diagram of an embodiment of a level detector in accordance with the present invention.

[0024] **FIG. 9** illustrates the operation of an embodiment of a level detector in accordance with the present invention.

[0025] **FIG. 10** is a schematic diagram of an embodiment of a negative voltage regulator in accordance with the present invention.

[0026] **FIG. 11** illustrates the operation of an embodiment of a negative voltage regulator in accordance with the present invention.

DETAILED DESCRIPTION

Negative Voltage Generator

[0027] **FIG. 4** is a diagram of an embodiment of a negative voltage generator in accordance with the present invention. The embodiment of **FIG. 4** includes an oscillator **10**, a first negative charge pump **20** having an output Vbb, and a level detector **30** arranged as in the prior art. However, the embodiment of **FIG. 4** further includes a second negative charge pump **50** having an output coupled to the output of the first negative charge pump **20**, either through a Vnn generator **40** as shown in **FIG. 4**, or through a direct connection as shown in **FIGS. 5 and 6**, or through any other suitable arrangement. The second negative charge pump **50** (also referred to as a "kicker") is activated and supplies additional negative charge for shutting off a word line responsive to a precharge command or signal. The second negative charge pump is preferably designed to provide an accurately pre-determined amount of negative charge. Thus, by providing most of the precharge current required to shut off a word line, the second charge pump dramatically reduces voltage fluctuations on the negative voltage supply.

[0028] In a preferred embodiment, the second charge pump is constructed essentially the same as the first charge pump, but it is activated responsive to a precharge command or signal. The capacitor in the second charge pump is preferably sized to discharge just the right amount of charge from a word line during a precharge operation.

[0029] Since most semiconductor memory devices operate from positive power supplies that are referenced to a power supply ground, a back bias scheme is described in terms of a negative voltage. However, as used herein, negative is understood to mean simply the reverse polarity from that applied to a word line during an access operation.

[0030] The level detector **30** performs the same function as the level detector **300** in **FIG. 1**, but in a preferred embodiment, it is replaced with a detector having faster response time and greater immunity to process and temperature variations in accordance with the present invention such as that shown in **FIG. 8** below.

[0031] The embodiment shown in **FIG. 4** further includes an optional Vnn generator **40** which is a voltage regulator that generates Vnn by canceling ripple in Vbb. Thus, a more stable negative word line bias can be obtained using the Vnn supply. A preferred embodiment of a negative voltage regulator is described below with respect to **FIGS. 10 and 11**. An advantage of using a negative voltage regulator in accordance with the present invention is that it cancels ripple in Vbb. Thus, it provides a more stable negative word line bias. Another advantage is that, since Vnn (typically about –0.5 Volts) is less negative than Vbb (typically about –1.0 Volts), it reduces the total amount of charge that must be removed from a word line during a precharge operation. A further advantage of using a negative voltage regulator to reduce the negative word line bias voltage is that the drive circuitry for the negative word line driving scheme dissipates less power.

[0032] Examples of precharge commands and signals suitable for triggering the second negative charge pump are shown in **FIG. 7** which is a timing diagram of commands and signals for a Synchronous Dynamic Random Access Memory (SDRAM) device. Precharge commands are typically external commands such as Row Precharge, Auto Precharge, All Banks Precharge, etc. Signals are typically internal signals such as PR in **FIG. 7**. The present invention, however, is not limited use with these commands and signals, or to SDRAM devices. The present invention can be adapted to work with any other suitable commands and/or signals that anticipate or correspond to a precharge operation for a word line. Pprecharge command and signal will be used interchangeably. Thus, precharge command or signal is understood to refer to any suitable command and/or signal that anticipates or corresponds to a precharge operation for a word line. Moreover, the present invention is not limited

to use with word lines, but can also be used with any other type of memory access line the operates with a negative precharge voltage.

[0033] **FIG. 5** is a diagram of another embodiment of a negative voltage generator in accordance with the present invention. In the embodiment of **FIG. 5**, there is no negative voltage regulator, and the output of the second negative charge pump **50** is connected directly to the output of the first negative charge pump **20**. In this configuration, Vbb and Vnn are the same signal, and the second charge pump is designed to deliver the predetermined negative charge directly to the word line control circuit in response to a word line precharge command or signal.

[0034] **FIG. 6** is a diagram of a third embodiment of a negative voltage generator in accordance with the present invention. The embodiment of **FIG. 6** is the same as the embodiment of **FIG. 5** except that it includes a negative voltage regulator **40** which has an input coupled to the outputs of the first and second charge pumps, and an output that generates the regulated Vnn signal.

Level Detector

[0035] **FIG. 8** is a schematic diagram of an embodiment of a level detector in accordance with the present invention. The level detector of **FIG. 8** includes a first voltage divider formed from resistors R1 and R2, a second voltage divider formed from resistors R3 and R4, a differential amplifier formed from transistors MP2, Mp2, Mp3, Mn1, and Mn2, and one or more inverters INV1, INV2. The first divider is connected between an internal reference voltage Vref and a power supply ground. The second divider is connected between the internal reference voltage Vref and the negative power supply, in this case Vbb. The voltage dividers divide the voltage between Vref and ground and between Vref and Vbb, thereby generating two divided signals X and Y which operate as comparison signals in response to Vref and Vbb according to the following equations:

$$X = Vref \cdot \frac{R2}{R1 + R2} \quad \text{and} \quad Y = (Vref - Vbb) \cdot \frac{R4}{R3 + R4}$$

[0036] Vref is a stable reference voltage, so X has a constant value, and the output Z will depend on whether Y is higher or lower than X. The target level for Vbb is given by:

$$Vbb = Vref \cdot \frac{R2R3 - R1R4}{R1R3 + R2R3}$$

[0037] Transistors Mp1, Mp2, Mp3, Mn1, and Mn2 are arranged as a differential amplifier with Mp3 forming a current source that biases Mp1 and Mp2 which are arranged as a differential pair of input transistors. Transistors Mn1 and Mn2 are arranged as a current mirror load referenced to the power supply ground. The output Z is taken from the connection between the drains of Mp1 and Mn1 and applied to the input of inverter INV1.

[0038] Since the differential amplifier has a high voltage gain (typically about 50), the output Z will swing quickly past the switching point of inverter INV1 as Y swings above and below X. The high gain characteristic of the differential amplifier reduces the on/off delay of the detector as shown in **FIG. 9**. This, in turn, reduces fluctuations in the negative voltage supply.

[0039] Another advantage of the level detector shown in **FIG. 8** is that the resistor divided voltage levels X and Y are insensitive to process and temperature variations, so the detector is also insensitive to these variations.

[0040] A further advantage is that, by connecting the voltage dividers to Vref instead of a positive power supply such as Vdd or a boosted voltage source such as Vpp, the level detector can be made insensitive to variations in the supply voltage, as happens, for example when Vdd is increased during a testing operation.

[0041] Yet another advantage of the level detector shown in **FIG. 8** is that the current mirror load is referenced to the power supply ground terminal rather than the Vbb terminal. This reduces the current draw from Vbb.

[0042] An additional advantage is that the comparison signals X and Y are biased by the voltage dividers at a quiescent voltage that is well above Vbb. This simplifies the design of the differential amplifier. In essence, the voltage dividers level shift the Vbb signal to a convenient voltage level.

[0043] A level detector in accordance with the present invention can be substituted anywhere for the conventional level detector shown in **FIG. 2** and is not limited to applications using a negative word line scheme.

Negative Voltage Regulator

[0044] **FIG. 10** is a schematic diagram of an embodiment of a negative voltage regulator (Vnn generator) in accordance with the present invention. The regulator of **FIG. 10** includes a first voltage divider formed from resistors R5 and R6, a second voltage divider formed from resistors R7 and R8, a differential amplifier formed from transistors Mp1, Mp2, Mp3, Mn1, and Mn2, and an output transistor Mn3.

[0045] The first divider is connected between an internal reference voltage Vref and a power supply ground. The second divider is connected between the internal reference voltage Vref and the drain of transistor Mn3. The source of Mn3 is connected to the negative power supply Vbb, and the gate of Mn3 is connected to the output of the differential amplifier at node G between the drains of Mn1 and Mp1.

[0046] Transistors Mp1, Mp2, Mp3, Mn1, and Mn2 are arranged as a differential amplifier with Mp3 forming a current source that biases Mp1 and Mp2 which are arranged as a differential pair of input transistors. Transistors Mn1 and Mn2 are arranged as a current mirror load referenced to the negative power supply Vbb.

[0047] The voltage dividers divide the voltage between Vref and ground and between Vref and Vnn, thereby generating two divided signals A and B which operate as comparison signals in response to Vref and Vnn. Since the regulator is connected in a negative feedback arrangement, the voltages on nodes A and B are forced to the same value. Thus, Vnn is given by the following equation:

$$Vnn = Vref \cdot \frac{R6R7 - R5R8}{R5R8 + R6R8}$$

[0048] As the voltage of Vbb varies, the voltage at node G tracks in the same phase as Vbb so that the gate-to-source voltage of Mn3 remains constant and the Vbb ripple caused by the detector on/off time is cancelled at Vnn as shown in FIG. 11.

[0049] An advantage of the negative voltage regulator of FIG. 10 is that the voltage dividers bias the comparison signals A and B at a quiescent voltage that is well above Vnn. This greatly simplifies the regulator circuit as compared to other regulators which typically have comparison signals that are biased at about the same voltage level as Vnn. In essence, the voltage dividers level shift the signals to a convenient voltage level.

[0050] Having described and illustrated the principles of the invention in some preferred embodiments thereof, it should be apparent that the invention can be modified in arrangement and detail without departing from such principles. We claim all modifications and variations coming within the spirit and scope of the following claims.

1. A negative voltage level detector for a semiconductor device comprising:

a differential amplifier having a first input and a second input;

a first voltage divider coupled to the first input of the differential amplifier; and

a second voltage divider coupled to the second input of the differential amplifier, and adapted to drive the second input of the differential amplifier responsive to a negative voltage.

2. A negative voltage level detector according to claim 1 wherein the first voltage divider is adapted to drive the first input of the differential amplifier responsive to a reference voltage.

3. A negative voltage level detector according to claim 2 wherein the first voltage divider comprises:

a first resistor coupled between the reference voltage and the first input of the differential amplifier; and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal.

4. A negative voltage level detector according to claim 2 wherein the second voltage divider comprises:

a first resistor coupled between a reference voltage and the second input of the differential amplifier; and

a second resistor coupled between the second input of the differential amplifier and the negative voltage.

5. A negative voltage level detector according to claim 1 further comprising an inverter having an input coupled to an output of the differential amplifier.

6. A negative voltage level detector according to claim 1:

wherein the first voltage divider comprises:

a first resistor coupled between a reference voltage and the first input of the differential amplifier, and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal;

wherein the second voltage divider comprises:

a third resistor coupled between the reference voltage and the second input of the differential amplifier, and

a fourth resistor coupled between the second input of the differential amplifier and the negative voltage;

wherein the differential amplifier comprises:

a differential pair of input transistors coupled to the first and second input terminals,

a current source coupled to the differential pair of transistors, and

a load coupled to the differential pair of transistors; and

further comprising an inverter having an input coupled to an output of the differential amplifier.

7. A negative voltage level detector according to claim 1 wherein the differential amplifier comprises a current mirror load coupled to a power supply terminal.

8. A negative voltage level detector according to claim 1 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the negative voltage is a negative voltage source for negatively biasing a word line.

9. A negative voltage level detector for a semiconductor device comprising:

means for dividing a reference voltage, thereby generating a first divided signal;

means for dividing a negative voltage, thereby generating a second divided signal; and

means for amplifying the difference between the first and second divided signals.

10. A negative voltage level detector according to claim 9 wherein the means for dividing a reference voltage comprises:

a first resistor coupled between the reference voltage and a first input of the means for amplifying; and

a second resistor coupled between the first input of the means for amplifying and a power supply terminal.

11. A negative voltage level detector according to claim 9 wherein the means for dividing a negative voltage comprises:

a first resistor coupled between a reference voltage and a second input of the means for amplifying; and

a second resistor coupled between the second input of the means for amplifying and the negative voltage.

12. A negative voltage level detector according to claim 9 wherein the means for amplifying comprises a differential amplifier referenced to a power supply voltage.

13. A negative voltage level detector according to claim 9 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the negative voltage is a negative voltage for biasing a word line.

14. A negative voltage level detector for a semiconductor device comprising:

a differential amplifier having a first input and a second input;

a first voltage divider coupled to the first input of the differential amplifier and adapted to drive the first input of the differential amplifier responsive to a reference voltage, wherein the first voltage divider is adapted to maintain the first input of the differential amplifier at a positive voltage; and

a second voltage divider coupled to the second input of the differential amplifier and adapted to drive the second input of the differential amplifier responsive to a negative voltage, wherein the second voltage divider is adapted to maintain the second input of the differential amplifier at a positive voltage.

15. A negative voltage level detector according to claim 14 wherein the first voltage divider comprises:

a first resistor coupled between the reference voltage and the first input of the differential amplifier; and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal.

16. A negative voltage level detector according to claim 14 wherein the second voltage divider comprises:

a first resistor coupled between a reference voltage and the second input of the differential amplifier; and

a second resistor coupled between the second input of the differential amplifier and the negative voltage.

17. A method for detecting a negative voltage in a semiconductor device comprising:

dividing a reference-voltage, thereby generating a first divided signal;

dividing the negative voltage, thereby generating a second divided signal; and

amplifying the difference between the first and second divided signals.

18. A method according to claim 17 wherein dividing the reference voltage comprises level shifting the reference voltage.

19. A method according to claim 17 wherein dividing the negative voltage comprises level shifting the negative voltage.

20. A method according to claim 17 wherein amplifying the difference between the first and second divided signals comprises referencing a differential amplifier to a power supply voltage.

21. A method according to claim 17 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the negative voltage is a negative voltage for biasing a word line.

22. A negative voltage regulator for a semiconductor device comprising:

a differential amplifier having a first input, a second input, and an output;

an output transistor coupled to the output of the differential amplifier and arranged to generate a second negative voltage from a first negative voltage;

a first voltage divider coupled to the first input of the differential amplifier; and

a second voltage divider coupled to the second input of the differential amplifier, and adapted to drive the second input of the differential amplifier responsive to the second negative voltage.

23. A negative voltage regulator according to claim 22 wherein the first voltage divider is adapted to drive the first input of the differential amplifier responsive to a reference voltage.

24. A negative voltage regulator according to claim 23 wherein the first voltage divider comprises:

a first resistor coupled between the reference voltage and the first input of the differential amplifier; and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal.

25. A negative voltage regulator according to claim 22 wherein the second voltage divider comprises:

a first resistor coupled between a reference voltage and the second input of the differential amplifier; and

a second resistor coupled between the second input of the differential amplifier and the second negative voltage.

26. A negative voltage regulator according to claim 32:

wherein the first voltage divider comprises:

a first resistor coupled between a reference voltage and the first input of the differential amplifier, and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal;

wherein the second voltage divider comprises:

a third resistor coupled between the reference voltage and the second input of the differential amplifier, and

a fourth resistor coupled between the second input of the differential amplifier and a the second negative voltage;

wherein the differential amplifier comprises:

a differential pair of input transistors coupled to the first and second input terminals,

a current source coupled to the differential pair of transistors, and

a load coupled to the differential pair of transistors; and

wherein the output transistor has a second terminal coupled to an output terminal of the differential amplifier.

27. A negative voltage regulator according to claim 22 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the second negative voltage is a negative voltage source for negatively biasing a word line.

28. A negative voltage regulator for a semiconductor device comprising:

means for generating a second negative voltage from a first negative voltage responsive to a drive signal;

means for dividing a reference voltage, thereby generating a first divided signal;

means for dividing the second negative voltage, thereby generating a second divided signal;

means for amplifying the difference between the first and second divided signals, thereby generating the drive signal.

29. A negative voltage regulator according to claim 28 wherein the means for dividing the reference voltage comprises:

a first resistor coupled between the reference voltage and a first input of the means for amplifying; and

a second resistor coupled between the first input of the means for amplifying and a power supply terminal.

30. A negative voltage regulator according to claim 28 wherein the means for dividing the second negative voltage comprises:

a first resistor coupled between a reference voltage and the second input of the means for amplifying; and

a second resistor coupled between the second input of the means for amplifying and the second negative voltage.

31. A negative voltage regulator according to claim 28 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the first negative voltage is a negative voltage for biasing a word line.

32. A negative voltage regulator for a semiconductor device comprising:

a differential amplifier having a first input, a second input, and an output;

an output transistor coupled to the output of the differential amplifier and arranged to generate a second negative voltage from a first negative voltage;

a first voltage divider coupled to the first input of the differential amplifier and adapted to drive the first input of the differential amplifier responsive to a reference voltage, wherein the first voltage divider is adapted to maintain the first input of the differential amplifier at a positive voltage; and

a second voltage divider coupled to the second input of the differential amplifier and adapted to drive the second input of the differential amplifier responsive to the second negative voltage, wherein the second voltage divider is adapted to maintain the second input of the differential amplifier at a positive voltage.

33. A negative voltage level detector according to claim 32 wherein the first voltage divider comprises:

a first resistor coupled between the reference voltage and the first input of the differential amplifier; and

a second resistor coupled between the first input of the differential amplifier and a power supply terminal.

34. A negative voltage level detector according to claim 32 wherein the second voltage divider comprises:

a first resistor coupled between a reference voltage and the second input of the differential amplifier; and

a second resistor coupled between the second input of the differential amplifier and the second negative voltage.

35. A method for generating a first negative voltage in a semiconductor device comprising:

generating a second negative voltage;

dividing a reference voltage, thereby generating a first divided signal;

dividing the first negative voltage, thereby generating a second divided signal;

amplifying the difference between the first and second divided signals, thereby generating a drive signal; and

driving an output transistor coupled between the first negative voltage and the second negative voltage responsive to the drive signal.

36. A method according to claim 35 wherein dividing the reference voltage comprises level shifting the reference voltage.

37. A method according to claim 35 wherein dividing the first negative voltage comprises level shifting the first negative voltage.

38. A method according to claim 35 wherein amplifying the difference between the first and second divided signals comprises referencing a differential amplifier to the second negative voltage.

39. A method according to claim 35 wherein:

the semiconductor device is a memory device utilizing a negative word line scheme; and

the first negative voltage is a negative voltage for biasing a word line.

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