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(54) **SELECTIVE & DAMAGE FREE CU CLEANING PROCESS FOR PRE-DEP, POST ETCH/CMP**

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(73) Assignee: **CHARTERED SEMICONDUCTOR MANUFACTURING LTD.**

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(63) Continuation of application No. 09/356,872, filed on Jul. 19, 1999.

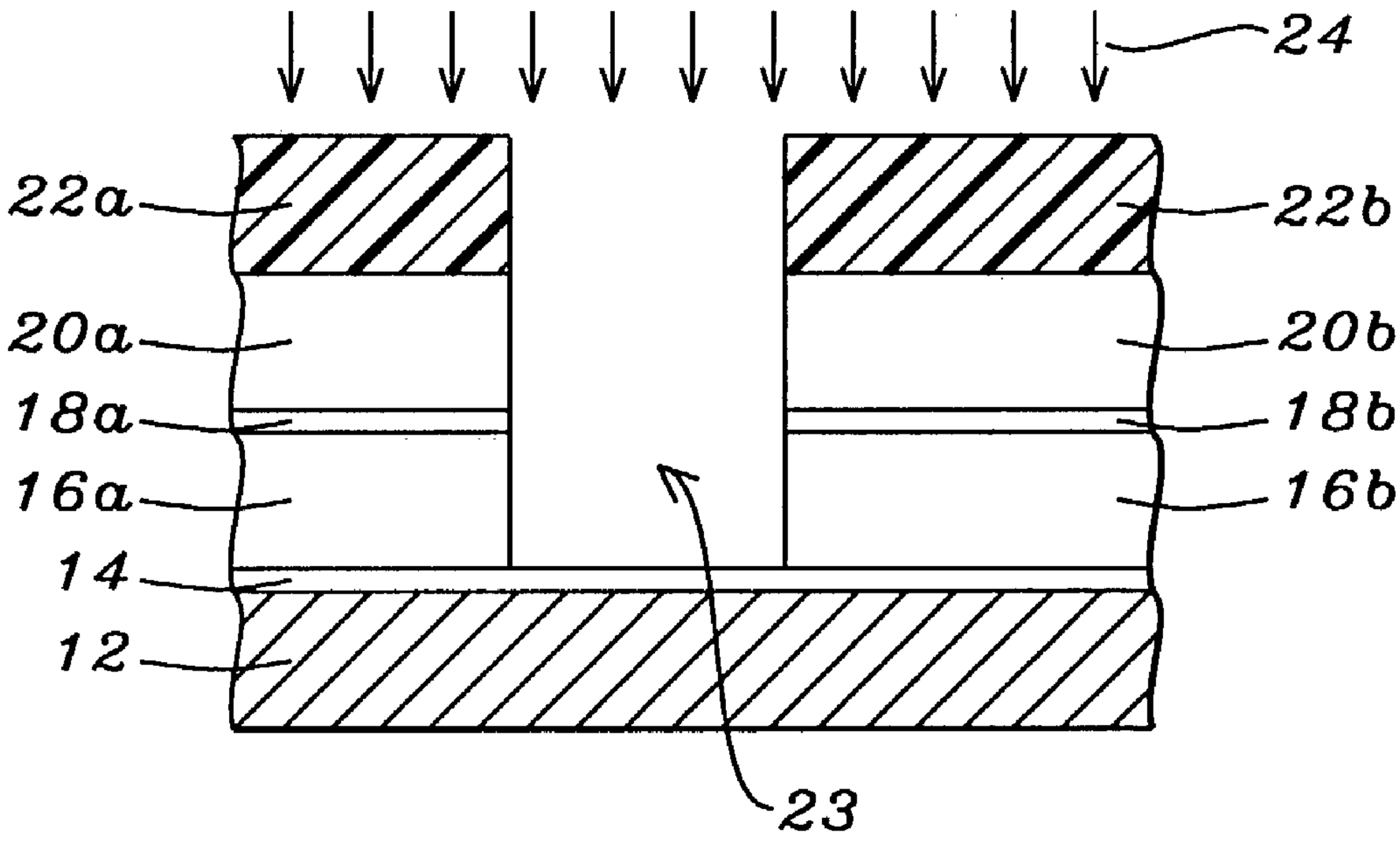
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(57) **ABSTRACT**

A method for forming a copper containing microelectronic structure. There is first provided a substrate. There is then formed over the substrate a copper containing microelectronic structure comprising a copper containing layer and a non-copper containing layer, where the non-copper containing layer has formed thereupon a copper containing residue. Finally, there is then stripped from the non-copper containing layer the copper containing residue while employing a stripper composition comprising a non-aqueous coordinating solvent and a halogen radical producing specie. Additionally, the copper so dissolved may be recovered from a non-aqueously solvated copper halide compound dissolved within the non-aqueous solvent.



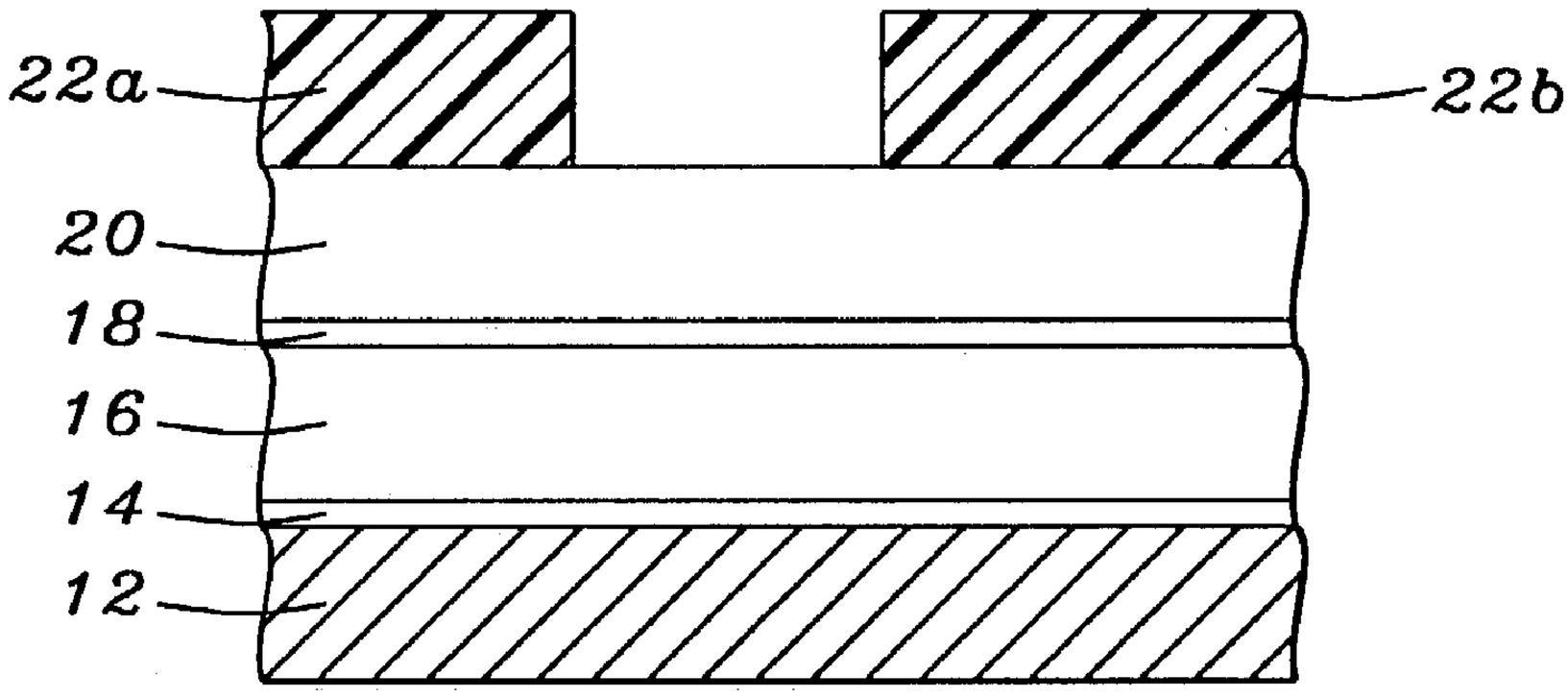


FIG. 1

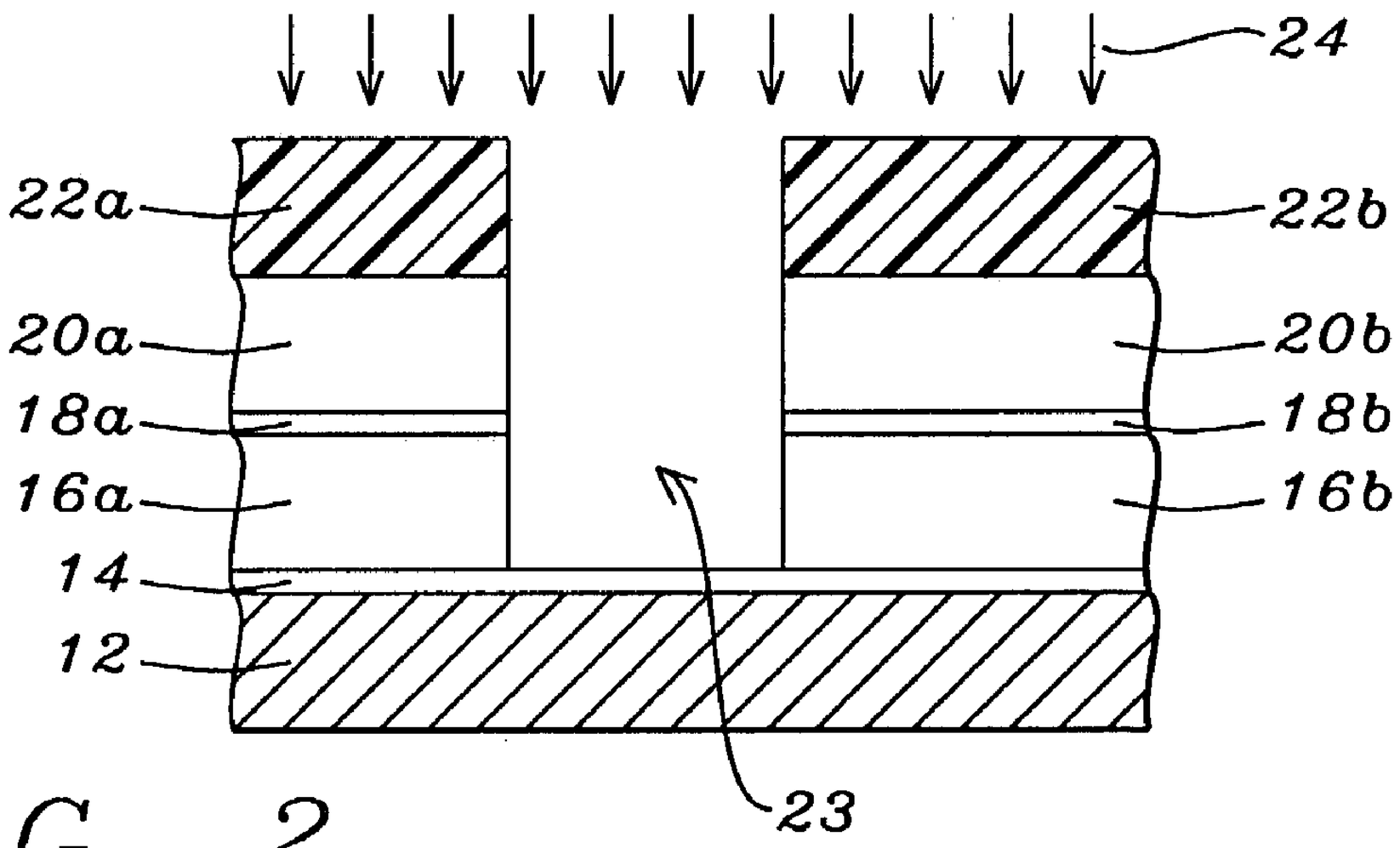


FIG. 2

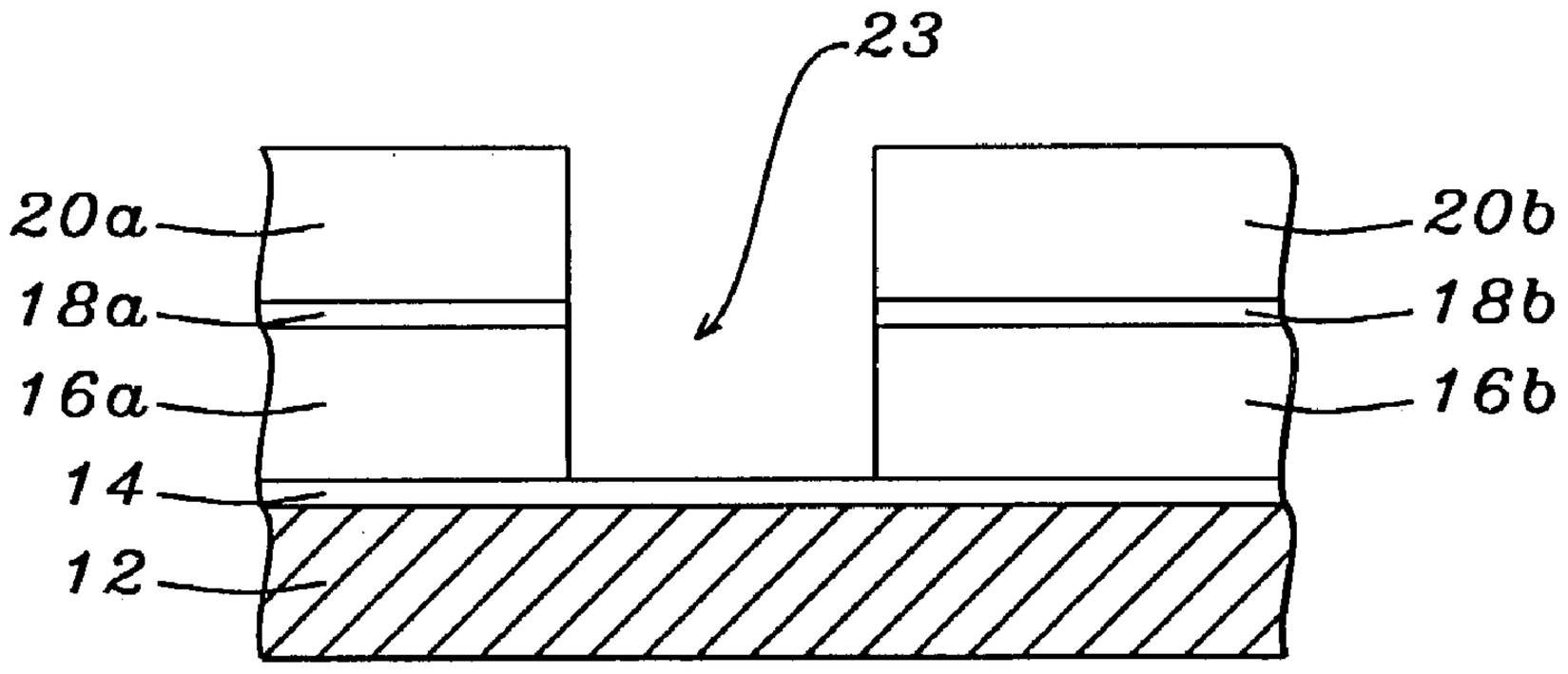


FIG. 3

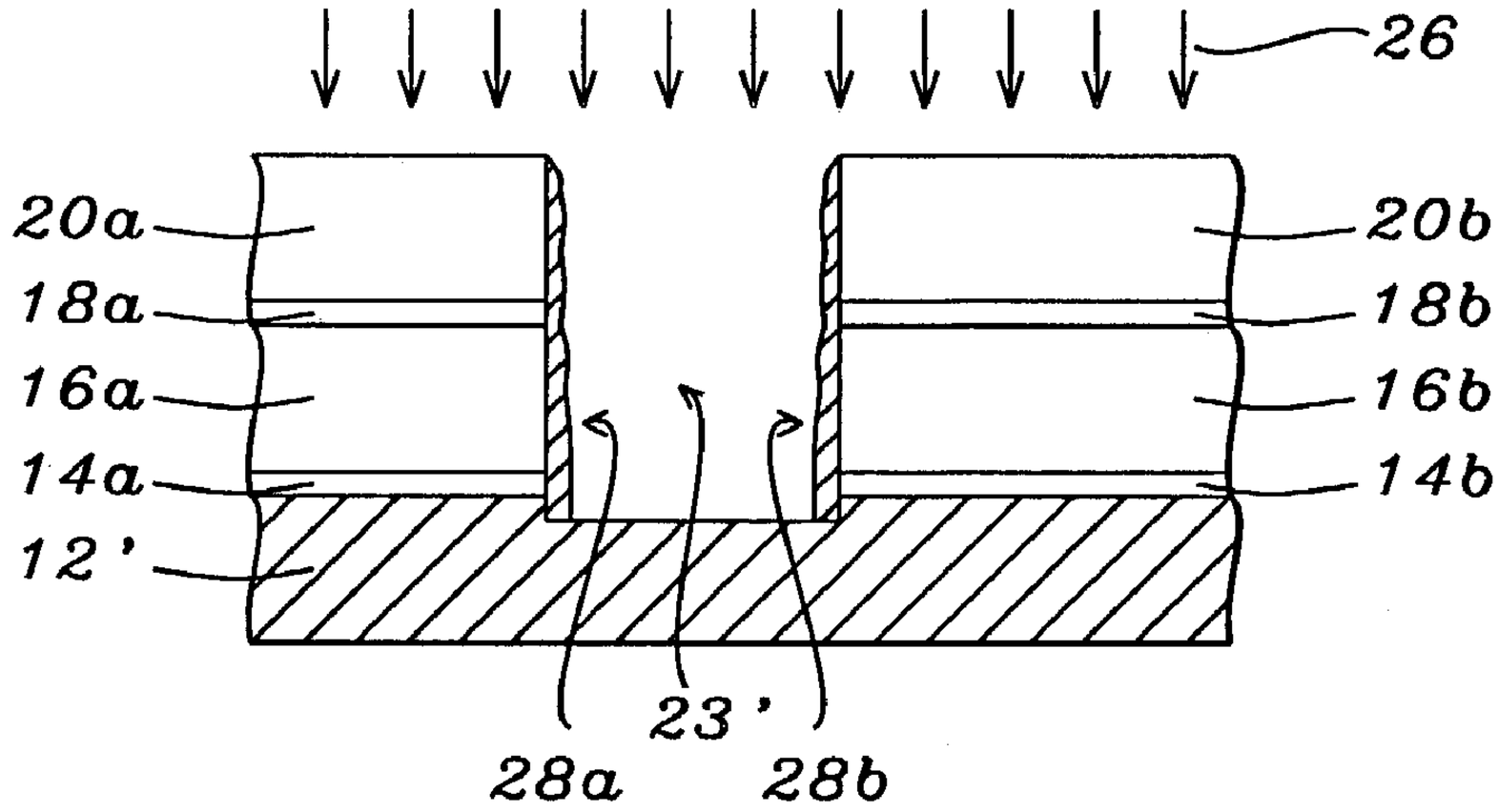


FIG. 4

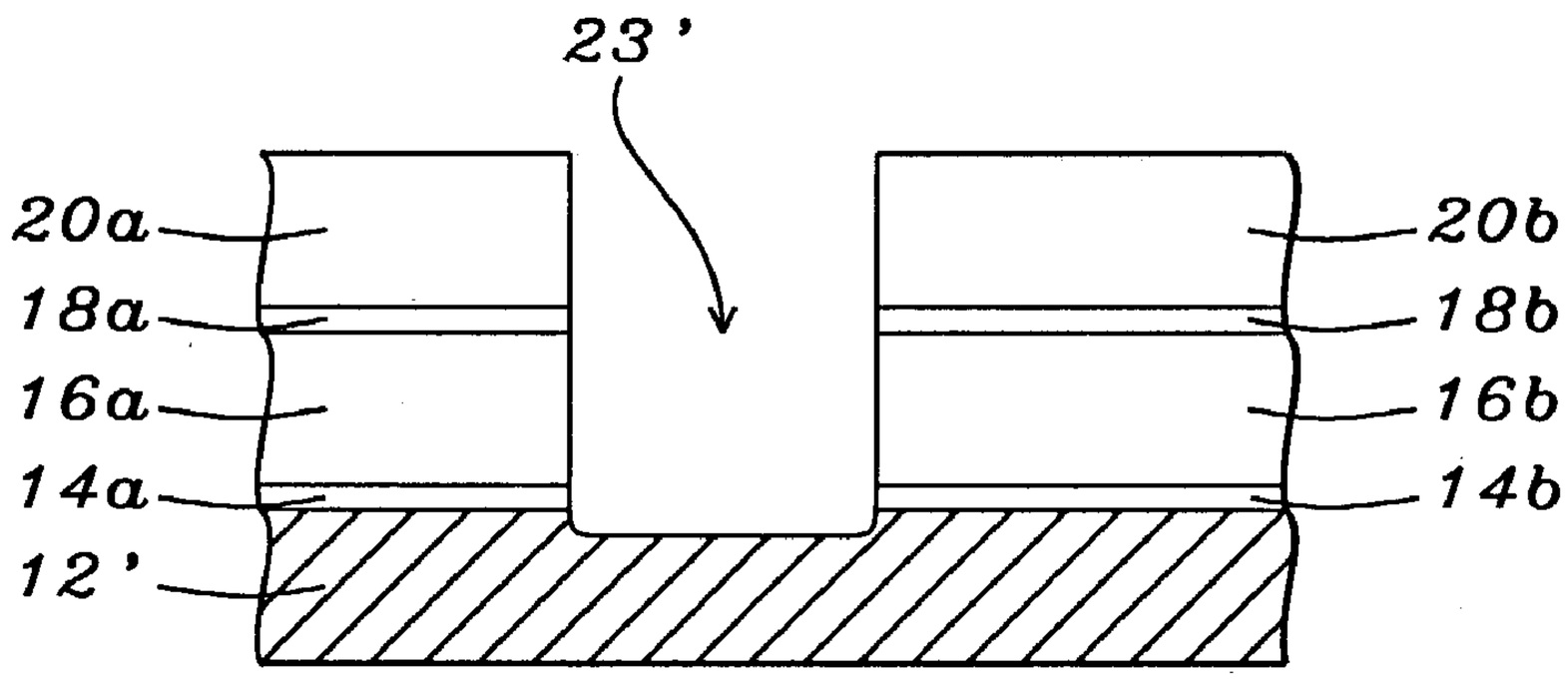


FIG. 5

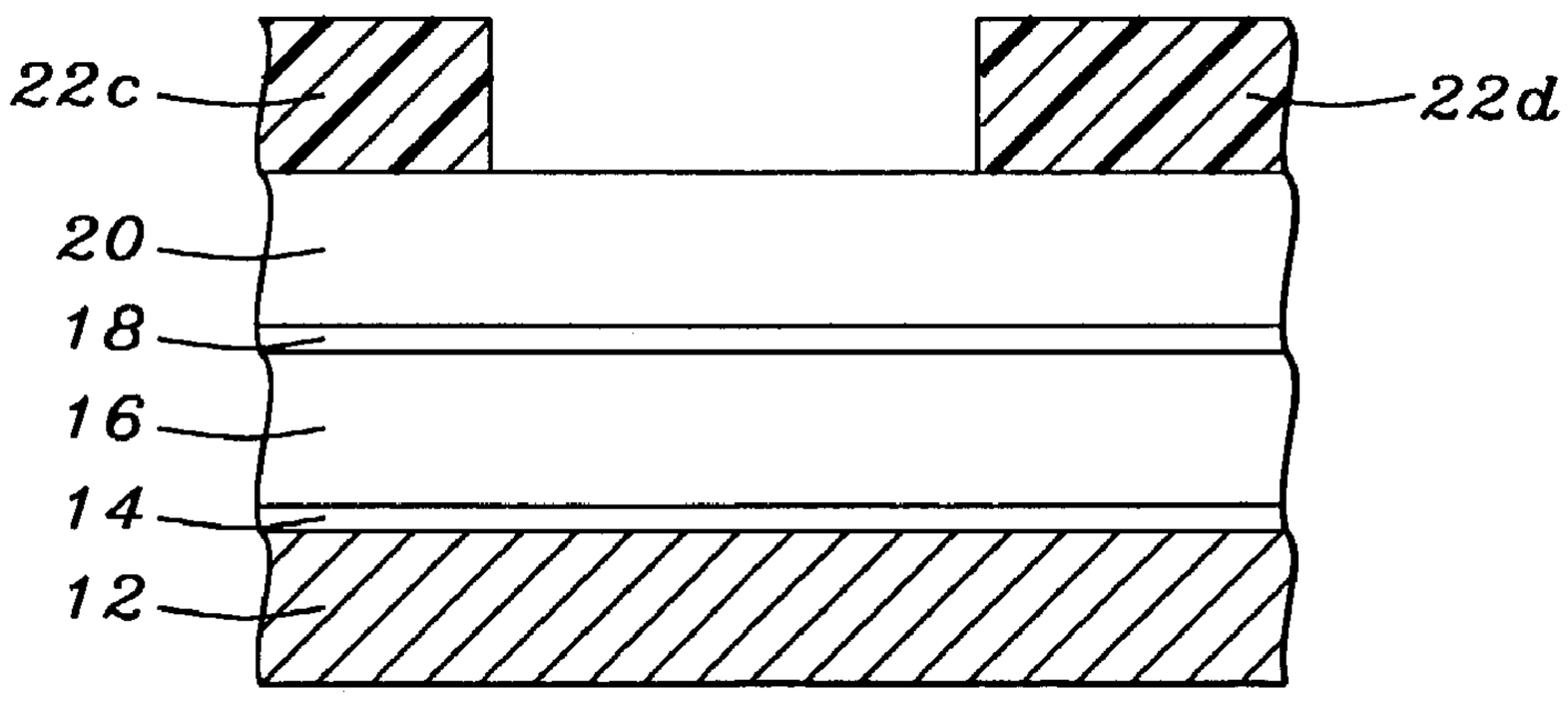


FIG. 6

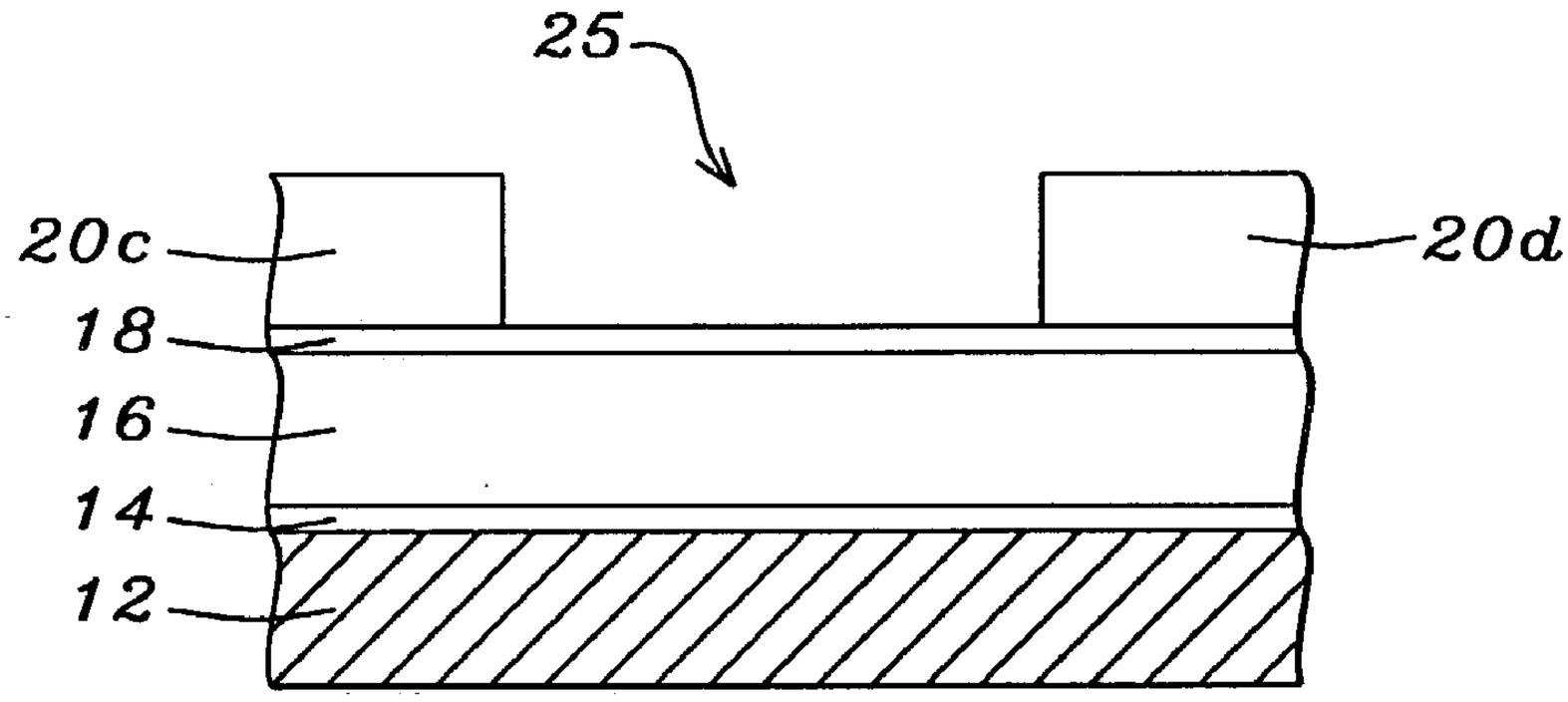


FIG. 7

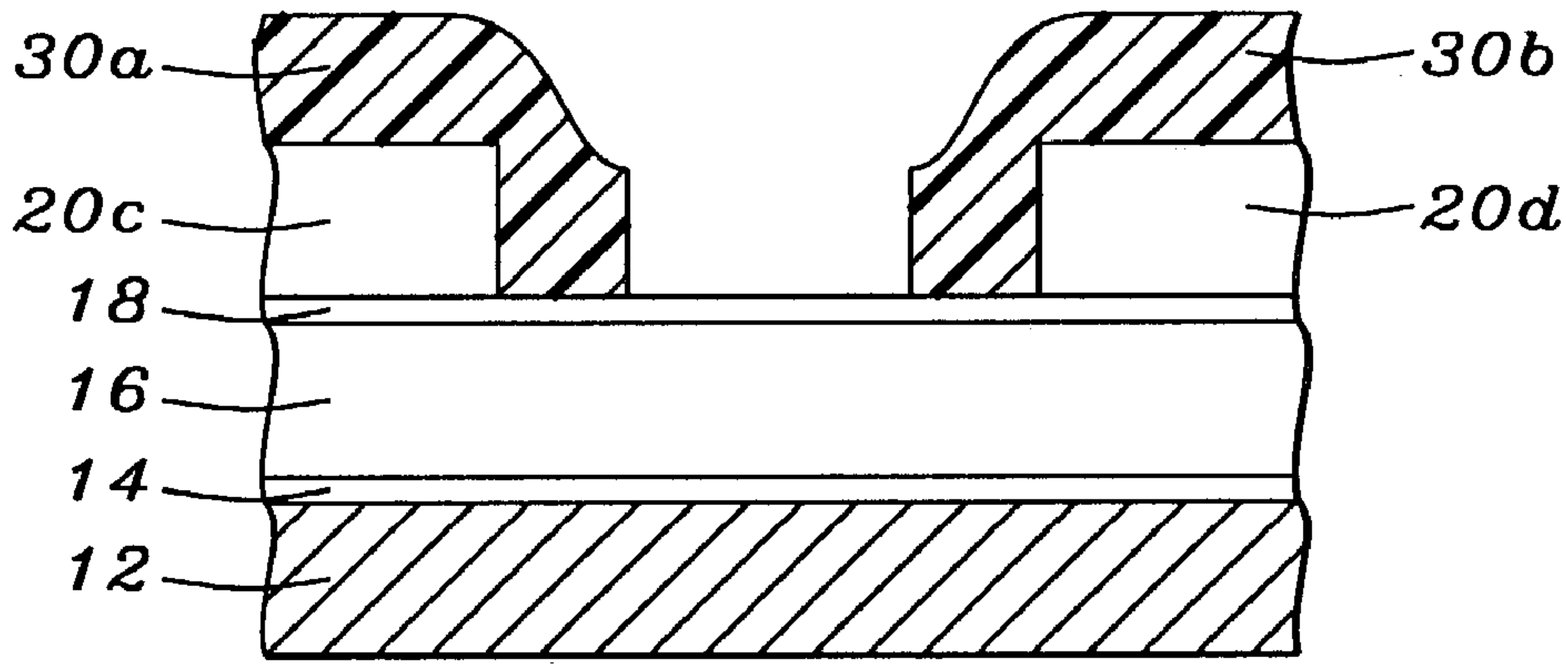


FIG. 8

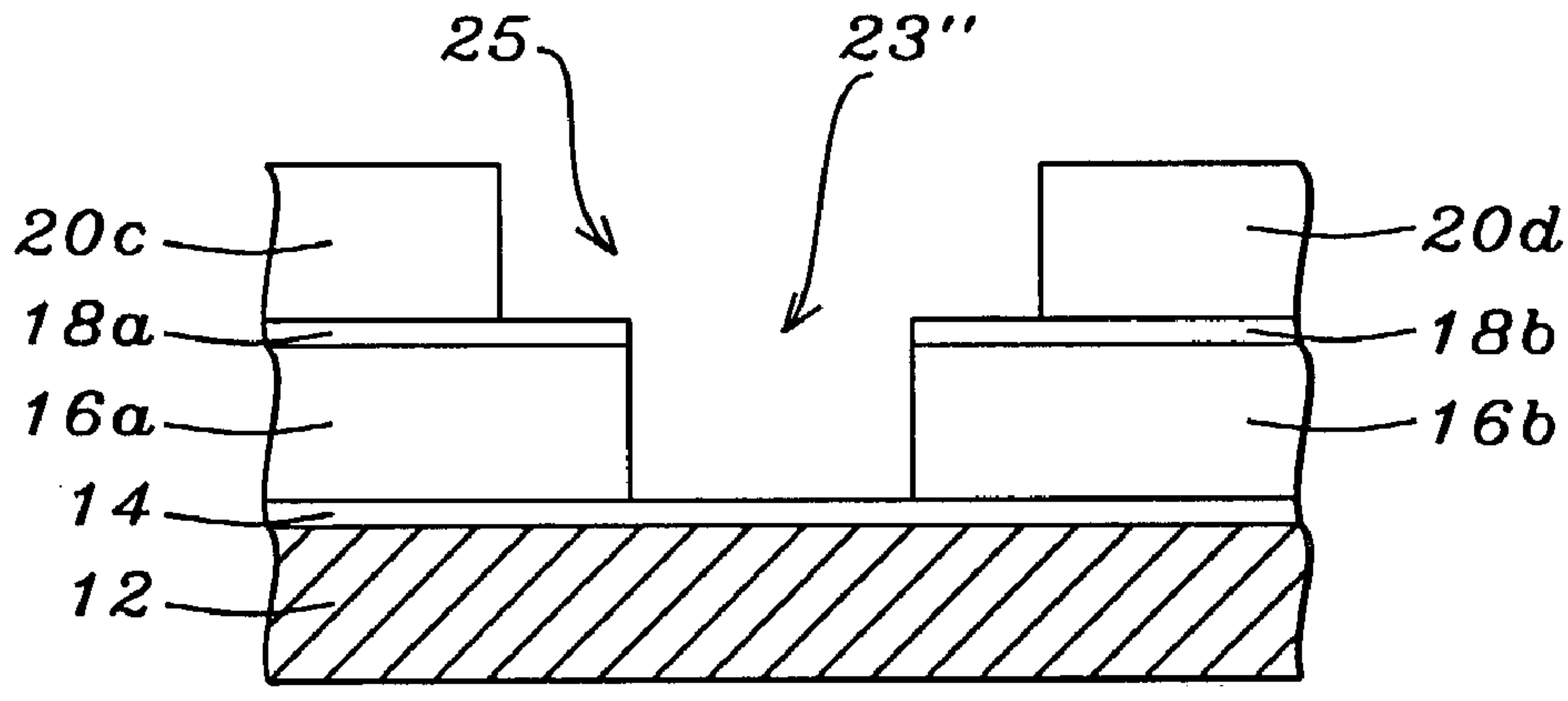


FIG. 9

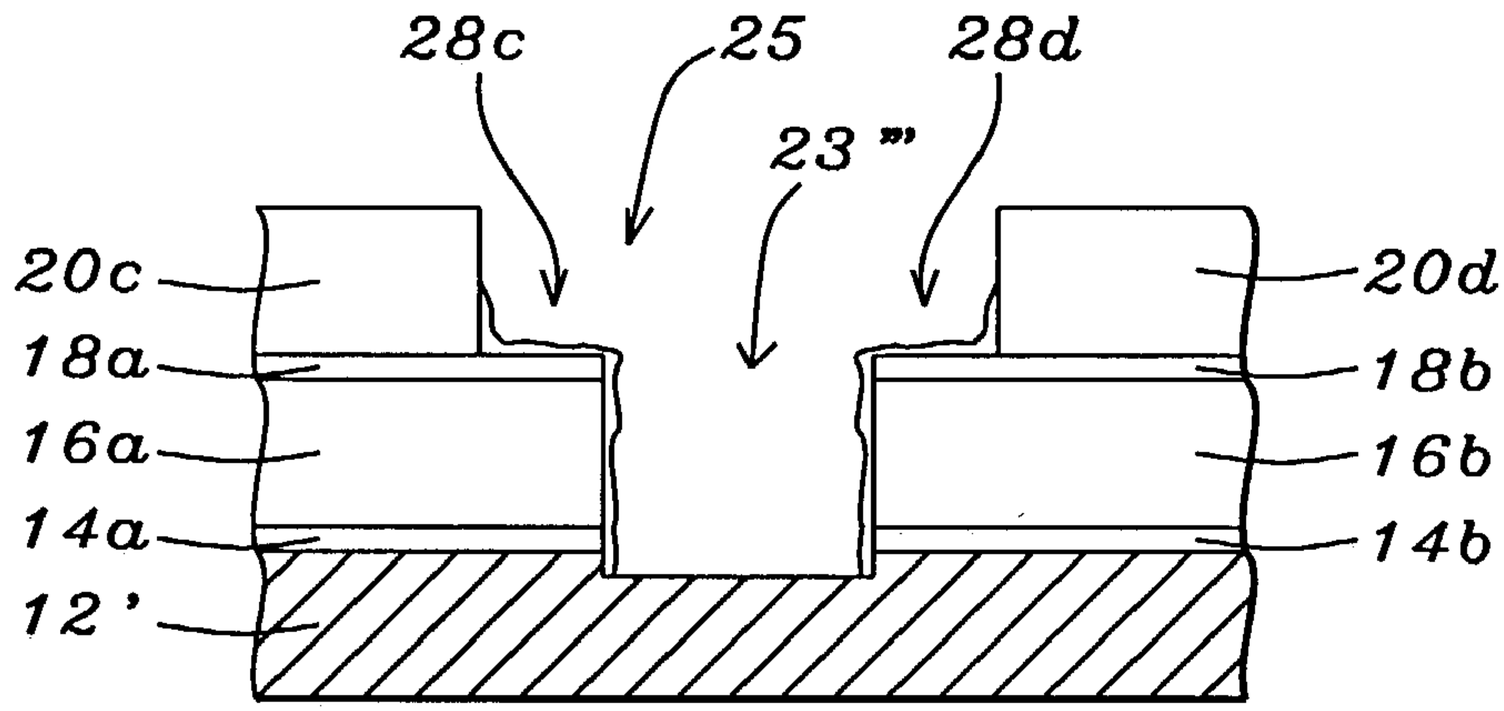


FIG. 10

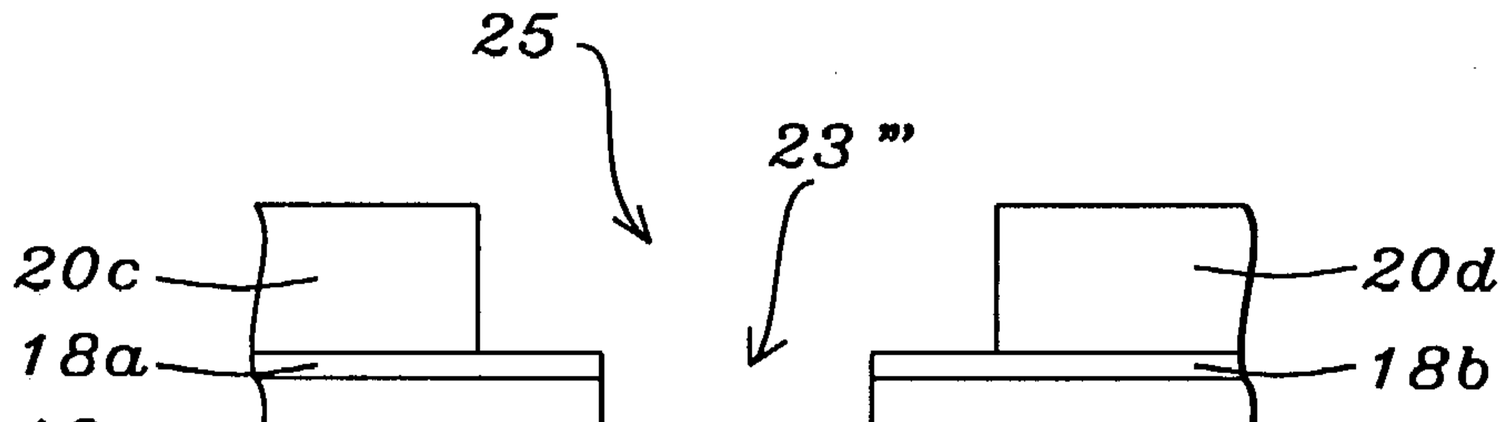


FIG. 11

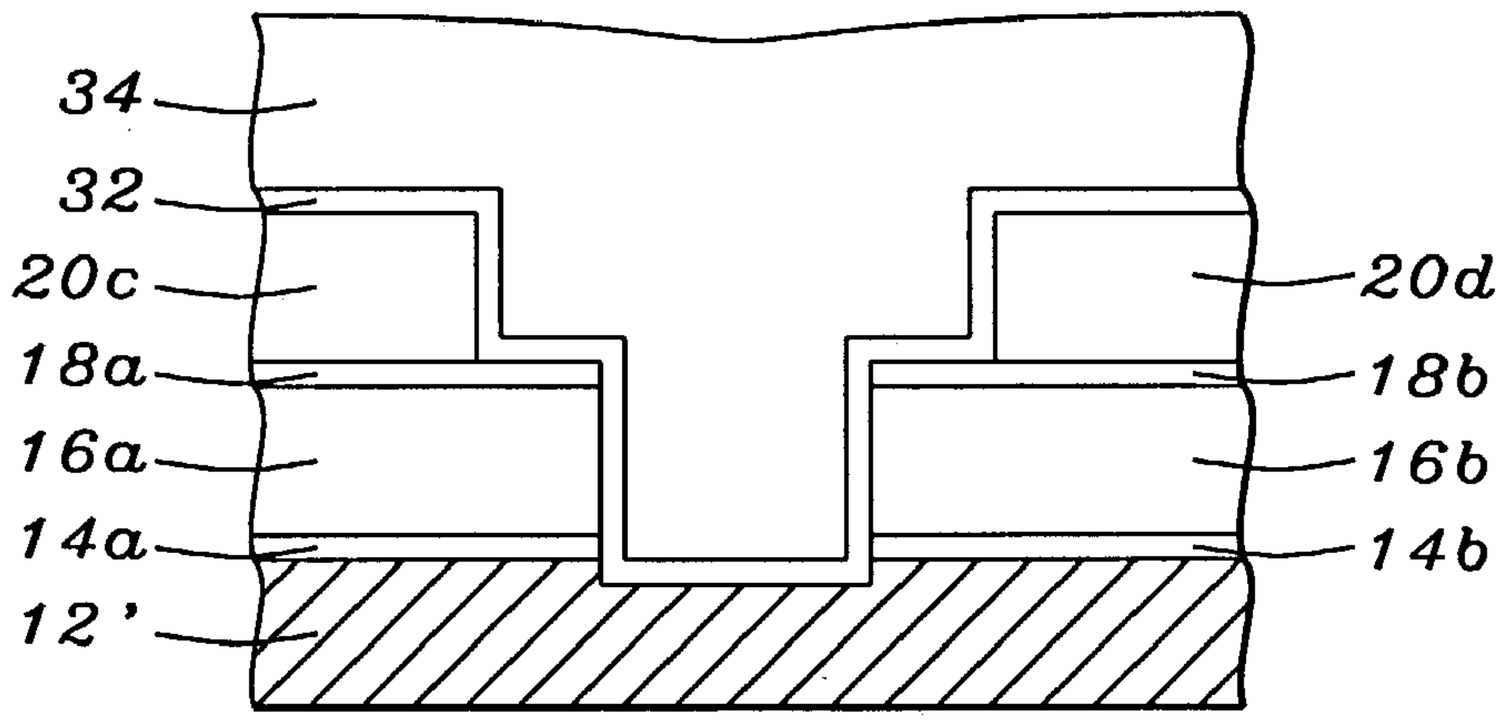


FIG. 12

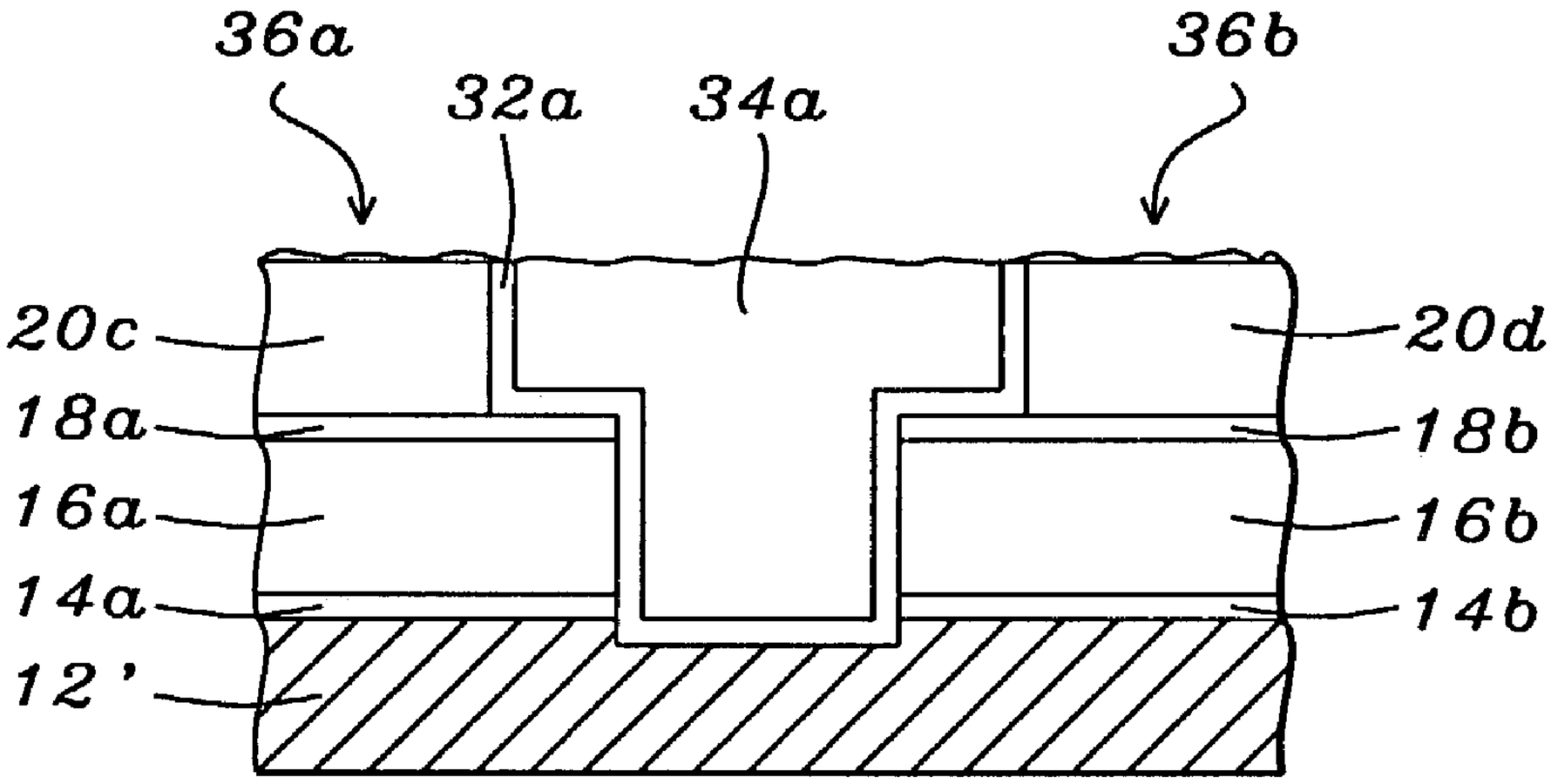

36a
32a
34a
36b
20c
20d
18a
18b
16a
16b
14a
14b
12'

FIG. 13

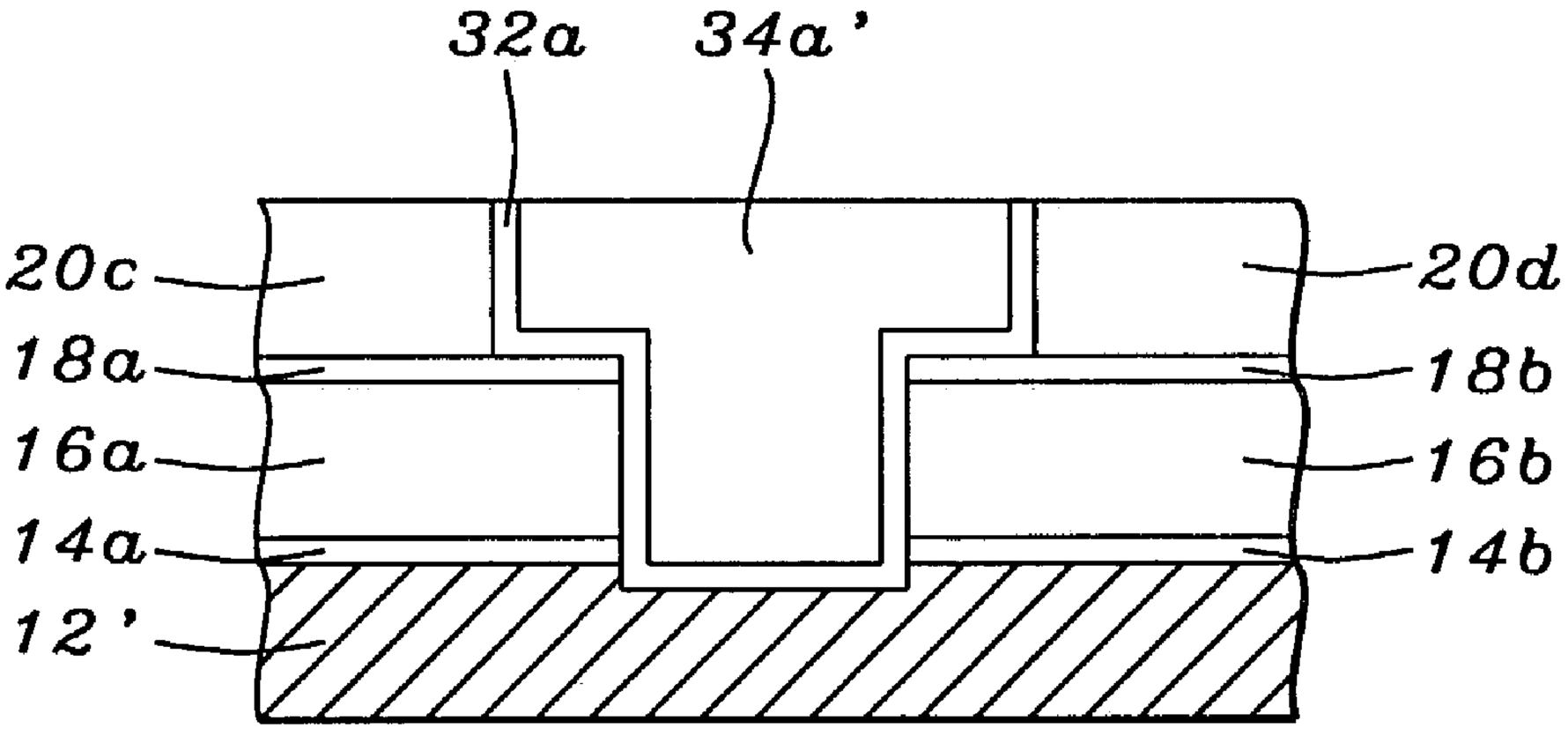

32a
34a'
20c
20d
18a
18b
16a
16b
14a
14b
12'

FIG. 14

SELECTIVE & DAMAGE FREE CU CLEANING PROCESS FOR PRE-DEP, POST ETCH/CMP

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates generally to methods for fabricating microelectronic layers within microelectronic fabrications. More particularly, the present invention relates to methods for fabricating residue free microelectronic structures comprising copper containing microelectronic layers within microelectronic fabrications.

[0003] 2. Description of the Related Art

[0004] As dimensions of microelectronic devices within advanced microelectronic fabrications have continued to decrease, so also have the dimensions of conductor layers and interconnect layers which connect and interconnect those microelectronic devices. In particular, dimensions of conductor layers and interconnect layers which directly contact microelectronic devices have typically decreased the greatest, thus becoming the smallest in dimension of conductor layers and interconnect layers within advanced-microelectronic fabrications.

[0005] These most narrow conductor layers and interconnect layers typically comprise the first conductor layer or interconnect layer which contacts a microelectronic device. Most commonly, first conductor layers have been traditionally been formed from aluminum metal or aluminum metal alloys. Most commonly, first interconnect layers (i.e.: first conductive contact stud layers) are formed of tungsten.

[0006] As microelectronic device dimensions have decreased while simultaneously maintaining or increasing demands for performance of microelectronic devices, it has become increasingly important for conductor layers and interconnect layers within microelectronic fabrications to exhibit a high level of conductivity while simultaneously showing limited susceptibility to degradative phenomenon such as electromigration. Electromigration is the physical movement of portions of conductor layers and interconnect layers which occurs under conditions of high current density. Under extremely high current densities, electromigration may yield the complete separation of a portion of a conductor layer or an interconnect layer, resulting in an electrical open. Electromigration is most common in aluminum metal and aluminum metal alloy conductor layers and interconnect layers. Although electromigration is not typically observed in interconnect layers formed of tungsten, the conductivity of tungsten interconnect layers is unfortunately typically substantially lower than the conductivity of aluminum metal or aluminum metal alloy interconnect layers.

[0007] In order to simultaneously provide the desired high electrical conductivity and low electromigration susceptibility of conductor layers and interconnect layers within advanced microelectronic fabrications, there has recently evolved for use within advanced microelectronic fabrications conductor layers and interconnect layers formed of copper metal or copper metal alloys. While copper metal and copper metal alloys possess the high electrical conductivity and low electromigration susceptibility desired for conductor layers and interconnect layers within advanced microelectronic fabrications, methods through which copper metal and copper metal alloys may be formed into conductor layers and interconnect layers within advanced microelectronic fabrications are unfortunately not entirely without problems in the art of microelectronic fabrication. In particular, it is known in the art of microelectronic fabrication that copper residues formed incident to fabricating copper containing conductor layers and copper containing interconnect layers are particularly undesirable insofar as copper residues efficiently interdiffuse with adjacent silicon oxide dielectric materials as are common within the art of microelectronic fabrication to significantly compromise microelectronic fabrication performance within microelectronic fabrications within which are formed those copper residues.

[0008] It is thus towards the goal of forming microelectronic fabrications which employ copper containing conductor layers or copper containing interconnect layers, without forming within those microelectronic fabrications copper containing residue layers, that the present invention is directed.

[0009] Various methods and materials have been disclosed within the art of microelectronic fabrication for forming microelectronic layers, preferably residue free microelectronic layers, within microelectronic fabrications.

[0010] For example, Ward et al., in U.S. Pat. No. 5,709,756, discloses a basic stripping and cleaning composition which may be employed for removing from various microelectronic fabrication structures and microelectronic fabrication layers within microelectronic fabrications various types of residue layers, including both inorganic residue layers and organic residue layers. The basic stripping and cleaning composition comprises an aqueous solution of hydroxylamine and ammonium fluoride, with optional added dimethylsulfoxide.

[0011] In addition, Zhou et al., in U.S. Pat. No. 5,780,358 and U.S. Pat. No. 5,863,307 disclose a chemical mechanical polish (CMP) planarizing method and a chemical mechanical polish (CMP) slurry composition for chemical mechanical polish (CMP) planarizing copper containing conductor layers within microelectronic fabrications. The chemical mechanical polish (CMP) planarizing method and the chemical mechanical polish (CMP) slurry composition employ a non-aqueous coordinating solvent and a halogen radical producing specie.

[0012] Finally, Givens et al., in U.S. Pat. No. 5,807,467, discloses an in-situ method for cleaning a substrate employed within a microelectronic fabrication prior to depositing threreupon a conductor layer. The in-situ method comprises an in-situ sputter etch method employing a physical vapor deposition (PVD) reactor chamber having formed therein a collimator, and wherein the collimator is held at a higher bias voltage than the substrate while sputter etch cleaning the substrate with an ionized inert sputter gas.

[0013] Desirable in the art of microelectronic fabrication are additional methods and materials which may be employed for fabricating microelectronic fabrications having formed therein copper containing layers with attenuated copper containing residue layer formation.

[0014] It is towards the foregoing object that the present invention is directed.

SUMMARY OF THE INVENTION

[0015] A first object of the present invention is to provide a method for forming within a microelectronic fabrication a microelectronic. structure comprising a copper containing layer.

[0016] A second object of the present invention is to provide a method in accord with the first object of the present invention, wherein the microelectronic structure is formed absent a copper containing residue formed upon a portion of the microelectronic structure other than the copper containing layer.

[0017] A third object of the present invention is to provide a method in accord with the first object of the present invention and the second object of the present invention, which method is readily commercially implemented.

[0018] In accord with the objects of the present invention, there is provided by the present invention a method for forming a copper containing microelectronic structure. To practice the method of the present invention, there is first provided a substrate. There is then formed over the substrate a copper containing microelectronic structure comprising a copper containing layer and a non-copper containing layer, where the non-copper containing layer has formed thereupon a copper containing residue. Finally, there is then stripped from the non-copper containing layer the copper containing residue while employing a stripper composition comprising a non-aqueous coordinating solvent and a halogen radical producing specie.

[0019] The present invention provides a method for forming within a microelectronic fabrication a microelectronic structure comprising a copper containing layer, where the microelectronic structure is formed absent a copper containing residue formed upon a portion of the microelectronic structure other than the copper containing layer. The present invention realizes the foregoing object by stripping from a non-copper containing layer within the microelectronic structure a copper containing residue while employing a stripper composition comprising a non-aqueous coordinating solvent and a halogen radical producing specie.

[0020] The present invention is readily commercially implemented. The present invention employs materials as are generally known, but not necessarily routinely employed in combination, in the art of microelectronic fabrication. Since it is a particular composition of materials and their use within microelectronic fabrication, rather than the existence of individual materials, which at least in part provides the present invention, rather than the existence of materials which provides the present invention, the present invention is readily commercially implemented.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The objects, features and advantages of the present invention are understood within the context of the Description of the Preferred Embodiments, as set forth below. The Description of the Preferred Embodiments is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

[0022] **FIG. 1**, **FIG. 2**, **FIG. 3**, **FIG. 4** and **FIG. 5** show a series of schematic cross-sectional diagrams illustrating the results of progressive stages in forming a microelectronic fabrication having formed therein a microelectronic structure having formed therein a copper containing conductor layer in accord with a preferred embodiment of the present invention.

[0023] **FIG. 6**, **FIG. 7**, **FIG. 8**, **FIG. 9**, **FIG. 10**, **FIG. 11**, **FIG. 12**, **FIG. 13** and **FIG. 14** show a series of schematic cross-sectional diagrams illustrating the results of forming a microelectronic fabrication having formed therein a microelectronic structure having formed therein a pair of copper containing conductor layers in accord with an alternate preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0024] The present invention provides a method for forming within a microelectronic fabrication a microelectronic structure comprising a copper containing layer, where the microelectronic structure is formed absent a copper containing residue layer formed upon a portion of the microelectronic structure other than the copper containing layer. The present invention realizes the foregoing object by stripping from a non-copper containing layer within the microelectronic structure a copper containing residue layer while employing a stripper composition comprising a non-aqueous coordinating solvent and a halogen radical producing specie.

[0025] The present invention may be employed in forming a microelectronic structure comprising a copper containing layer, where the microelectronic structure is formed absent a copper containing residue formed upon a portion of the microelectronic structure other than the copper containing layer within a microelectronic fabrication selected from the group including but not limited to integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

[0026] Although the preferred embodiment of the present invention illustrates the present invention within the context of stripping copper containing residue layers at least in part from passivation dielectric layers within microelectronic fabrications, the present invention may be employed for stripping from microelectronic layers including but not limited to microelectronic conductor layers, microelectronic semiconductor layers and microelectronic dielectric layers copper containing residue layers.

[0027] Referring now to **FIG. 1** to **FIG. 5**, there is shown a series of schematic cross-sectional diagrams illustrating the results of forming within a microelectronic fabrication in accord with a preferred embodiment of the present invention a microelectronic structure comprising a copper containing conductor layer. Shown in **FIG. 1** is a schematic cross-sectional diagram of the microelectronic fabrication at an early stage in its fabrication in accord with the preferred embodiment of the present invention.

[0028] Shown in **FIG. 1** is a first copper containing conductor layer **12**, where the first copper containing conductor layer **12** has formed thereupon a blanket first barrier layer **14**, which in turn has formed thereupon a blanket first passivation dielectric layer **16**, which in turn has formed thereupon a blanket etch stop layer **18**, which in turn has

formed thereupon a blanket second passivation dielectric layer **20**, which in turn finally has formed thereupon a pair of patterned photoresist layers **22***a* and **22***b*. Within the preferred embodiment of the present invention, each of the foregoing first copper containing conductor layer **12**, blanket first barrier layer **14**, blanket first passivation dielectric layer **16**, blanket etch stop layer **18**, blanket second passivation dielectric layer **20** and pair of patterned photoresist layers **22***a* and **22***b* may be formed employing methods and materials as are conventional in the art of microelectronic fabrication.

[**0029**] Similarly, although not specifically illustrated within the schematic cross-sectional diagram of **FIG. 1**, the series of foregoing layers is typically and preferably formed upon or over a substrate, where the substrate may be employed within a microelectronic fabrication selected from the group including but not limited to integrated circuit microelectonic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectonic fabrications and display image array optoelectronic fabrications.

[**0030**] Yet similarly, although also not specifically illustrated within the schematic cross-sectional diagram of **FIG. 1**, such a substrate may comprise a substrate alone as employed within a microelectronic fabrication, or in the alternative, the substrate may comprise the substrate as employed within the microelectronic fabrication, where the substrate has formed thereupon and/or thereover, and thus incorporated therein, any of several additional microelectronic layers as are commonly employed within the microelectronic fabrication within which is employed the substrate. Similarly with the substrate itself, such additional microelectronic layers may independently be formed of microelectronic materials including but not limited to microelectronic conductor materials, microelectronic semiconductor materials and microelectronic dielectric materials.

[**0031**] Still yet similarly, although also not specifically illustrated within the schematic cross-sectional diagram of **FIG. 1**, the substrate, particularly but not exclusively when the substrate comprises a semiconductor substrate employed within a semiconductor integrated circuit microelectronic fabrication, has formed therein and/or thereupon, and thus incorporated therein, any of several microelectronic devices as are conventional within the microelectronic fabrication within which is employed the substrate. Such microelectronic devices may include, but are not limited to, resistors transistors, diodes and capacitors.

[**0032**] Within the preferred embodiment of the present invention with respect to the first copper containing conductor layer **12**, although the first copper containing conductor layer **12** may be formed employing methods including but not limited to chemical vapor deposition (CVD) methods, physical vapor deposition (PVD) methods and electrochemical plating methods, the first copper containing conductor layer **12** is typically and preferably formed employing a physical vapor deposition (PVD) sputtering method as is conventional in the art of microelectronic fabrication. Typically and preferably, the first copper containing conductor layer **12** is formed to a thickness of from about 2000 to about 20000 angstroms and, if the first copper containing conductor layer is a patterned copper containing conductor layer, a linewidth of from about 0.1 to about 100 microns. Typically and preferably, the first copper containing conductor layer **12** is formed of 100 percent copper.

[**0033**] Within the preferred embodiment of the present invention with respect to the blanket first barrier layer **14** and the blanket etch stop layer **18**, although it is known in the art of microelectronic fabrication that barrier layers and etch stop layers may be formed employing methods including but not limited to chemical vapor deposition (CVD) methods, plasma enhanced chemical vapor deposition (PECVD) methods and physical vapor deposition (PVD) sputtering methods to form barrier layers of barrier materials including but not limited to conductor barrier materials, semiconductor barrier materials and dielectric barrier materials and etch stop layers of etch. stop materials including but not limited to conductor etch stop materials, semiconductor etch stop materials and dielectric etch stop materials, for the preferred embodiment of the present invention, the blanket first barrier layer **14** and the blanket etch stop layer **18** are typically and preferably formed of a silicon nitride dielectric barrier material and a silicon nitride dielectric etch stop material deposited employing a plasma enhanced chemical vapor deposition (PECVD) method, where: (1) the blanket first barrier layer **14** so formed impedes interdiffusion of the first copper containing conductor layer **12** with the blanket first passivation dielectric layer **16** when the blanket first passivation dielectric layer **16** is formed of dielectric materials such as but not limited to undoped silicon oxide dielectric materials, fluorine doped silicon oxide dielectric materials and generally both inorganic and organic low dielectric constant dielectric materials formed upon the blanket first barrier layer **14**; and (2) the blanket etch stop layer **18**, which is optional within the preferred embodiment of the present invention, serves as an etch stop layer under circumstances when selectively etching the blanket second passivation dielectric layer **20** with respect to the blanket first passivation dielectric layer **16**. Typically and preferably, each of the blanket first barrier layer **14** and the blanket etch stop layer **18** is formed to a thickness of from about 500 to about 5000 angstroms.

[**0034**] Within the preferred embodiment of the present invention with respect to the blanket first passivation dielectric layer **16** and the blanket second passivation dielectric layer **20**, the blanket first passivation dielectric layer **16** and the blanket second passivation dielectric layer **20** are, as suggested above, typically and preferably formed of a dielectric material selected from the group including but not limited to undoped silicon oxide dielectric materials, fluorine doped silicon oxide dielectric materials, and generally other inorganic and organic low dielectric constant dielectric materials which may be deposited employing a method selected from the group including but not limited to chemical vapor deposition (CVD) methods, plasma enhanced chemical vapor deposition (PECVD) methods, physical vapor deposition (PVD) sputtering methods and spin-on methods. Typically and preferably, each of the blanket first passivation dielectric layer **16** and the blanket second passivation dielectric layer **20** is formed to a thickness of from about 2000 to about 20000 angstroms from a silicon oxide dielectric material deposited employing a plasma enhanced chemical vapor deposition (PECVD) method.

[**0035**] Finally, within the preferred embodiment of the present invention with respect to the pair of patterned

photoresist layers **22***a* and **22***b*, the pair of patterned photoresist layers **22***a* and **22***b* may be formed employing photoresist materials as are conventional in the art of microelectronic fabrication, including but not limited to photoresist materials selected from the general groups of photoresist materials including but not limited to positive photoreist materials and negative photoresist materials. Typically and preferably, each photoresist layer **22***a* or **22***b* within the pair of patterned photoresist layers **22***a* and **22***b* is formed to a thickness of from about 4000 to about 20000 angstroms.

[**0036**] Referring now to **FIG. 2**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 1**.

[**0037**] Shown in **FIG. 2** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated within **FIG. 1**, but wherein the blanket second passivation dielectric layer **20**, the blanket etch stop layer **18** and the blanket first passivation dielectric layer **16** have been sequentially patterned, while employing the patterned photoresist layers **22***a* and **22***b* as a photoresist etch mask layer and in conjunction with a first etching plasma **24**, to form a corresponding pair of patterned second passivation dielectric layers **20***a* and **20***b*, a corresponding pair of patterned etch stop layers **18***a* and **18***b* and a corresponding pair of patterned first passivation dielectric layers **16***a* and **16***b* which in the aggregate define a via **23**. Typically and preferably, the blanket second passivation dielectric layer **20**, the blanket etch stop layer **18** and the blanket first passivation dielectric layer **16** are sequentially etched to form the corresponding patterned second passivation dielectric layers **20***a* and **20***b*, the corresponding patterned etch stop layers **18***a* and **18***b* and the corresponding patterned first passivation dielectric layers **16***a* and **16***b* while employing the first etching plasma **24** which employs an etchant gas composition appropriate to the materials from which is formed the blanket second passivation dielectric layer **20**, the blanket etch stop layer **18** and the blanket first passivation dielectric layer **16**. Within the preferred embodiment of the present invention where: **(1)** the blanket first passivation dielectric layer **16** and the blanket second passivation dielectric layer **20** are typically and preferably formed of a dielectric material selected from the group including but not limited to undoped silicon oxide dielectric materials, fluorine doped silicon oxide dielectric materials, and generally inorganic and organic low dielectric constant dielectric materials; and (2) the blanket first barrier layer **14** and the blanket etch stop layer **18** are each formed of a silicon nitride dielectric material, the first etching plasma **24** typically and preferably employs an etchant gas composition which upon plasma activation forms an active fluorine containing etchant species. More typically and preferably, the etchant gas composition which upon plasma activation forms the active fluorine containing etchant species comprises at least one of a perfluorocarbon of up to about 6 carbon atoms and a hydrofluorocarbon of up to about 4 carbon atoms, in conjunction. with an optional sputter gas component and an optional diluent gas as may be desirable to provide a stabilized first etching plasma **24**. Most typically and preferably within the preferred embodiment of the present invention, the first etching plasma **24** employs an etchant gas composition comprising carbon tetrafluoride, trifluoromethane and argon.

[**0038**] When etching the blanket second passivation dielectric layer **20**, the blanket etch stop layer **18** and the blanket first passivation dielectric layer **16** to form the corresponding patterned second passivation dielectric layers **20***a* and **20***b*, the corresponding patterned etch stop layers **18***a* and **18***b* and the corresponding patterned first passivation dielectric layers **16***a* and **16***b* over an eight inch diameter substrate, the first etching plasma **24** also typically and preferably also employs: (1) a reactor chamber pressure of from about 0.1 to about 1000 mtorr; (2) a source radio frequency power of from about 500 to about 3000 watts at a source radio frequency of 13.56 MHZ; (3) a substrate temperature of from about 50 to about 300 degrees centigrade; (4) a carbon tetrafluoride flow rate of from about 1 to about 200 standard cubic centimeters per minute (sccm); (5) a trifluoromethane flow rate of from about 1 to about **200** standard cubic centimeters per minute (sccm); and (6) an argon flow rate of from about 100 to about 1000 standard cubic centimeters per minute (sccm).

[**0039**] Referring now to **FIG. 3**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 2**.

[**0040**] Shown in **FIG. 3** is a schematic cross-sectional diagram of a microelectronic. fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 2**, but wherein there is stripped from the pair of patterned second passivation dielectric layers **20***a* and **20***b* the corresponding pair of patterned photoresist layers **22***a* and **22***b*. Within the preferred embodiment of the present invention, the pair of patterned photoresist layers **22***a* and **22***b* may be stripped from the pair of patterned second dielectric passivation layers **20***a* and **20***b* to form from the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 2** the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 3** while employing photoresist stripping methods as are both conventional in the art of microelectronic fabrication and appropriate to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 2**, such photoresist stripping methods including but not limited to wet chemical photoresist stripping methods, dry plasma photoresist stripping methods and aggregate photoresist stripping methods employing wet chemical photoresist stripping methods and dry plasma photoresist stripping methods.

[**0041**] Referring now to **FIG. 4**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 3**.

[**0042**] Shown in **FIG. 4** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 3**, but wherein the blanket first barrier layer **14** has been patterned to form a pair of patterned first barrier layers **14***a* and **14***b* through etching within a second etching plasma **26** to thus also form from the via **23** a via **23'**. Typically and preferably, the second etching plasma **26** employs methods and materials analogous or equivalent to the methods and materials employed within the first etching plasma **24**, under circum-

stances when the blanket first barrier layer **14** and the blanket etch stop layer **18** are formed of an analogous or equivalent material.

[**0043**] Shown also within **FIG. 4** formed upon the sidewalls of the pair of patterned second passivation dielectric layers **20***a* and **20***b*, the pair of patterned etch stop layers **18***a* and **18***b*, the pair of patterned first passivation dielectric layers **16***a* and **16***b* and the pair of patterned first barrier layers **14***a* and **14***b* which define the via **23**' is a pair of first copper containing residue layers **28***a* and **28***b*. The pair of first copper containing residue layers **28***a* and **28***b* is typically formed incident to complete etching within the second etching plasma **26** of the blanket first barrier layer **14**, in absence of the patterned photoresist layers **22***a* and **22***b*, to form the patterned first barrier layers **14***a* and **14***b* while simultaneously over-etching into the first copper containing conductor layer **12** to form a plasma etched first copper containing conductor layer **12**', as is also illustrated within the schematic cross-sectional diagram of **FIG. 4**. Typically, the first copper containing residue layers **28***a* and **28***b* are comprised of a copper fluoride and/or copper oxide and/or copper type material which may have a substantial weight percent copper.

[**0044**] Referring now to **FIG. 5**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 4**. Shown in **FIG. 5** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 4**, but wherein the pair of first copper containing residue layers **28***a* and **28***b* has been stripped from the microelectronic fabrication.

[**0045**] Within the preferred embodiment of the present invention with respect to stripping the pair of first copper containing residue layers **28***a* and **28***b*, the pair of first copper containing residue layers **28***a* and **28***b* is stripped employing a stripper composition comprising a non-aqueous coordinating solvent and a halogen radical producing specie. This combination of components has been shown to assist in the rapid dissolution of copper metal under mild conditions. See, for example, Hui-Qing et al., "Copper Metal Oxidation by a Dimethylsulfoxide-Carbon Tetrachloride Mixture," Proceedings, Science Research Congress 1992, Singapore, pp. 81-86, the teachings of which are incorporated herein fully by reference, as originally cited within Zhou et al., U.S. Pat. No. 5,780,358 and U.S. Pat. No. 5,863,307, as cited within the Description of the Related Art, the teachings of all of which related art are also incorporated herein by reference.

[**0046**] There are several options for non-aqueous coordinating solvents which may be employed within the stripper composition of the present invention. Non-aqueous coordinating solvents may be mono-coordinate or poly-coordinate. In addition, the coordinating atoms within the non-aqueous coordinating solvent may include, but are not limited to, oxygen coordinating atoms, nitrogen coordinating atoms and sulfur coordinating atoms. Preferably, the non-aqueous coordinating solvent within the stripper composition of the present invention is chosen from the group of non-aqueous coordinating solvents consisting of acetonitrile (CH3CN), tetrahydrofuran (THF) and dimethylsulfoxide (DMSO). Most preferably, the non-aqueous coordinating solvent within the stripper composition of the present invention is dimethylsulfoxide (DMSO).

[**0047**] Various halogen containing species which may produce halogen radicals within the non-aqueous coordinating solvent of the stripper composition of the present invention are known in the art. Typical halogen containing species which may produce halogen radicals within the non-aqueous coordinating solvent include but are not limited to C1-C2 perchloro, hydrochloro, perbromo and hydrobromo compounds. Preferably the halogen radical producing specie of the present invention is a chlorine radical producing specie chosen from the group of chlorine radical producing species consisting of C1-C2 perchloro and hydrochloro compounds. Most preferably, the halogen radical producing specie is the chlorine radical producing specie carbon tetrachloride (CCl4). Most preferably, the stripper composition of the present invention is formed with dimethylsulfoxide (DMSO) as the non-aqueous coordinating solvent and carbon tetrachloride (CCl4) as the halogen radical producing specie, at a DMSO:CCl4 volume ratio of from about 100:1 to about 0.01:1.

[**0048**] Within the preferred embodiment of the present invention, the pair of first copper containing residue layers **28***a* and **28***b* is stripped by immersion in, or spraying with, the stripper composition comprising the non-aqueous coordinating solvent and the halogen radical producing specie for a time period of from about **0.1** to about **60** minutes, without a specific need for additional abrasion or activation to effect stripping of the pair of first copper containing residue layers **28***a* and **28***b*, although abrasion or activation may under certain circumstances be desirable.

[**0049**] Referring now to **FIG. 6** to **FIG. 14**, there is shown a series of schematic cross-sectional diagrams illustrating the results of progressive stages in forming a microelectronic fabrication having formed therein a microelectronic structure having formed therein a pair of copper containing conductor layers in accord with an alternate preferred embodiment of the present invention. Shown in **FIG. 6** is a schematic cross-sectional diagram of the microelectronic fabrication at an early stage in its fabrication in accord with the alternate preferred embodiment of the present invention.

[**0050**] Shown in **FIG. 6** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 1**, but wherein: (1) the blanket etch stop layer **18** is no longer optional but is required in the alternate preferred embodiment of the present invention; and (2) there is employed in place of the patterned first photoresist layers **22***a* and **22***b* as illustrated within the schematic cross-sectional diagram of **FIG. 1 a** pair of patterned first photoresist layers **22***c* and **22***d*, where the patterned first photoresist layers **22***c* and **22***d* as illustrated within the schematic cross-sectional diagram of **FIG. 6** have a greater separation distance (i.e. aperture width) than the patterned first photoresist layers **22***a* and **22***b* as illustrated within the schematic cross-sectional diagram of **FIG. 1**. Otherwise, within the alternate preferred embodiment of the present invention as illustrated in **FIG. 6**, each of the layers as illustrated therein is formed employing methods, materials and dimensions analogous or equivalent to the methods, materials and dimensions as employed for forming

the corresponding layers within the microelectronic fabrication of the preferred embodiment of the present invention whose schematic cross-sectional diagram is illustrated in **FIG. 1**.

[**0051**] Referring now to **FIG. 7**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 6**.

[**0052**] Shown in **FIG. 7** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 6**, but wherein in a first instance the blanket second passivation dielectric layer **20** has been patterned to form a pair of patterned second passivation dielectric layers **20***c* and **20***d* which defines a trench **25**. The blanket second passivation dielectric layer **20** as illustrated within the schematic cross-sectional diagram of **FIG. 6** may be patterned to form the pair of patterned second dielectric passivation dielectric layers **20***a* and **20***b* which defines the trench **25** as illustrated within the schematic cross-sectional diagram of **FIG. 7** while employing a plasma etch method such as the first plasma etch method employing the first etching plasma **24** as illustrated within the schematic cross-sectional diagram of **FIG. 2**.

[**0053**] Also shown within the schematic cross-sectional diagram of **FIG. 7** in comparison with the schematic cross-sectional diagram of **FIG. 6** is the absence of the pair of patterned first photoresist layers **22***c* and **22***d* which are employed as an etch mask layer for forming the pair of patterned second passivation dielectric layers **20***c* and **20***d* from the blanket second passivation dielectric layer **20**. The patterned first photoresist layers **22***c* and **22***d* may be stripped from the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 6** to provide in part the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 7** while employing photoresist stripping methods as are conventional in the art of microelectronic fabrication, as disclosed above.

[**0054**] Referring now to **FIG. 8**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 7**.

[**0055**] Shown in **FIG. 8** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 7**, but wherein there is formed encapsulating the pair of patterned second passivation dielectric layers **20***c* and **20***d* a pair of patterned second photoresist layers **30***a* and **30***b* which define the location of a via to be formed through the blanket etch stop layer **18**, the blanket first passivation dielectric layer **16** and the blanket first barrier layer **14**. The pair of patterned second photoresist layers **30***a* and **30***b* may otherwise be formed employing methods and materials analogous or equivalent to the methods and materials employed for forming the pair of patterned first photoresist layers **20***c* and **20***d* as illustrated within the schematic cross-sectional diagram of **FIG. 6** or the pair of patterned first photoresist layers **20***a* and **20***b* as illustrated within the schematic cross-sectional diagram of **FIG. 1**. Similarly, the pair of patterned second photoresist layers **30***a* and **30***b* is formed with a separation distance analogous or equivalent to the separation distance employed for forming the pair of patterned first photoresist layers **22***a* and **22***b* as illustrated within the schematic cross-sectional diagram of **FIG. 1**.

[**0056**] Referring now to **FIG. 9**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 8**.

[**0057**] Shown in **FIG. 9** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 8**, but wherein in a first instance there is formed through the blanket etch stop layer **18** and the blanket first passivation dielectric layer **16** a via **23**" contiguous with the trench **25** while simultaneously forming a pair of patterned etch stop layers **18***a* and **18***b* and a pair of patterned first passivation dielectric layers **16***a* and **16***b*. The blanket etch stop layer **18** and the blanket first passivation dielectric layer **16** as illustrated within the schematic cross-sectional diagram of **FIG. 8** may be patterned to form the patterned etch stop layers **18***a* and **18***b* and the patterned first passivation dielectric layers **16***a* and. **16***b* as illustrated within the schematic cross-sectional diagram of **FIG. 9** while employing a plasma etch method analogous or equivalent to the plasma etch method employed for forming the via **23** within the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 2**.

[**0058**] Also shown within the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 9** in comparison with the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 8** is the absence of the pair of patterned second photoresist layers **30***a* and **30***b*. The pair of patterned second photoresist layers **30***a* and **30***b* may be stripped from the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 8** to provide in part the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 9** while employing photoresist stripping methods as are conventional in the art of microelectronic fabrication.

[**0059**] Referring now to **FIG. 10**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 9**.

[**0060**] Shown in **FIG. 10** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 9**, but wherein the blanket first barrier layer **14** has been etched to form a pair of patterned first barrier layers **14***a* and **14***b* while simultaneously forming a pair of first copper containing residue layers **28***c* and **28***d* upon various portions of the patterned first barrier layers **14***a* and **14***b*, the patterned first passivation dielectric layers **16***a* and **16***b*, the patterned etch stop layers **18***a* and **18***b* and the patterned second passivation dielectric layers **20***a* and **20***b* which in part define a via **23**'" which is formed from the via **23**" which is contiguous with the trench **25**. Within the alternate preferred embodiment of the present invention, the pair of patterned first barrier layers **14***a* and **14***b*, as well as the pair of first copper containing

residue layers **28***c* and **28***d* may be formed employing methods and materials analogous or equivalent to the methods and materials employed for forming the pair of patterned first barrier layers **14***a* and **14***b* and the pair of first copper containing residue layers **28***a* and **28***b* within the preferred embodiment of the present invention as illustrated within the schematic cross-sectional diagram of **FIG. 4**.

[**0061**] As is understood by a person skilled in the art, a microelectronic fabrication analogous or equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 10** may be formed within the preferred embodiment of the present invention incident to further patterning of the patterned second passivation dielectric layers **20***a* and **20***b* as illustrated within the schematic cross-sectional diagram of **FIG. 4** while employing a pair of patterned second photoresist layers of separation distance (i.e. aperture width) equivalent to the separation distance of the pair of patterned first photoresist layers **22***c* and **22***d* as illustrated within the schematic cross-sectional diagram of **FIG. 6**.

[**0062**] Referring now to **FIG. 11**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 10**.

[**0063**] Shown in **FIG. 11** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 10**, but wherein there is stripped from the microelectronic fabrication the pair of first copper containing residue layers **28***c* and **28***d*. The pair of first copper containing residue layers **28***c* and **28***d* may be stripped from the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 10** to provide the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 11** while employing the method and material employed for stripping the first copper containing residue layers **28***a* and **28***b* from the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 4** to form the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 5**. In particular, the pair of first copper containing residue layers **28***c* and **28***d* is stripped from the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 10** to provide the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 11** while employing a stripper composition comprising a non aqueous coordinating solvent and a halogen radical producing specie.

[**0064**] Although not specifically illustrated within the schematic cross-sectional diagram of **FIG. 11** or **FIG. 5**; in order to completely remove the first copper containing residue layers **28***c* and **28***d* or the first copper containing residue layers **28***a* and **28***b*, it may be desirable to provide multiple non-aqueous coordinating solvent rinses prior to further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 11** or **FIG. 5**, with additional volatile solvent drying which may be effected, for instance, by employing an isopropyl alcohol solvent drying method.

[**0065**] Referring now to **FIG. 12**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 11**.

[**0066**] Shown in **FIG. 12** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 11**, but wherein there has been formed over the substrate and into trench **25** defined by the pair of patterned second passivation dielectric layers **20***c* and **20***d* the via **23**''' defined by the pair of patterned etch stop layers **18***a* and **18***b*, the pair of patterned first passivation dielectric layers **16***a* and **16***b* and the pair of patterned first barrier layers **14***a* and **14***b* a blanket second barrier layer **32** having formed thereupon a blanket second copper containing conductor layer **34**, and where the blanket second barrier layer **32** contacts the plasma etched first copper containing conductor layer **12**'.

[**0067**] Within the preferred embodiment of the present invention with respect to the blanket second barrier layer **32**, in contrast with the blanket first barrier layer **14** as illustrated within the schematic cross-sectional diagram. of **FIG. 1** and the schematic cross-sectional diagram of **FIG. 6**, the blanket second barrier layer **32** is typically and preferably formed of a conductor barrier material which provides a barrier for interdiffusion between the blanket second copper containing conductor layer **34** and the patterned second passivation dielectric layers **20***c* and **20***d*. Such conductor barrier materials may be selected from the group of conductor barrier materials including but not limited to titanium nitride conductor barrier materials, tantalum nitride conductor barrier materials and composites thereof More preferably, the blanket second barrier layer **32** is formed of a tantalum nitride conductor barrier material while employing a deposition method selected from the group consisting of chemical vapor deposition (CVD) methods, plasma enhanced chemical vapor deposition (PECVD) methods and physical vapor deposition (PVD) deposition methods.

[**0068**] Within the preferred embodiment of the present invention with respect to the blanket second copper containing conductor layer **34**, the blanket second copper containing conductor layer **34** is typically and preferably formed employing copper containing conductor materials and deposition methods analogous or equivalent to the copper containing conductor materials and deposition methods employed for forming the first copper containing conductor layer **12** as illustrated within the schematic cross-sectional diagram of **FIG. 1** and the schematic cross-sectional diagram of **FIG. 6**. Typically and preferably, the blanket second copper containing conductor layer **34** is formed to a thickness which more than completely fills the via **23**''' and the trench **25**, as illustrated within the schematic cross-sectional diagram of **FIG. 12**.

[**0069**] Referring now to **FIG. 13**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 12**.

[**0070**] Shown in **FIG. 13** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 12**, but wherein the blanket second copper containing conductor layer **34** and the blanket second barrier layer **32** have been planarized to form a corresponding patterned second barrier layer **32***a* having formed thereupon a patterned second copper containing conductor layer **34***a*. Although it is known

in the art of microelectronic fabrication that blanket layers may in general be planarized to form patterned layers while employing planarizing methods including but not limited to reactive ion etch (RIE) etchback planarizing methods and chemical mechanical polish (CMP) planarizing methods, for the preferred embodiment of the present invention, the blanket second copper containing conductor layer **34** and the blanket second barrier layer **32** are preferably planarized to form the corresponding patterned second copper containing conductor layer **34***a* formed upon the patterned second barrier layer **32***a* while employing a chemical mechanical polish (CMP) planarizing method as is conventional in the art of microelectronic fabrication.

[**0071**] As is illustrated within the schematic cross-sectional diagram of **FIG. 13**, there is also formed incident to chemical mechanical polish (CMP) planarizing the blanket second copper containing conductor layer **34** and the blanket second barrier layer **32** to form the corresponding patterned second copper containing conductor layer **34***a* formed upon the patterned second barrier layer **32***a* a pair of second copper containing residue layers **36***a* and **36***b* formed upon the corresponding patterned second passivation dielectric layers **20***c* and **20***d*. The pair of second copper containing residue layers **36***a* and **36***b* typically results from smearing of the blanket second copper containing conductor layer **34** and the blanket second barrier layer **32** into inhomogeneous depressions within the corresponding pair of patterned second passivation dielectric layers **20***c* and **20***d* while chemical mechanical polish (CMP) planarizing the blanket second copper containing conductor layer **34** and the blanket second barrier layer **32** to form the corresponding patterned second copper containing conductor layer **34***a* and the patterned second barrier layer **32***a*. Thus, although the pair of second copper containing residue layers **36***a* and **36***b* is formed, analogously with either the pair of first copper containing residue layers **28***a* and **28***b* or the pair of first copper containing residue layers **28***c* and **28***d*, also upon patterned portions of the blanket second passivation dielectric layer **20**, the chemical composition of the pair of second copper containing residue layers **36***a* and **36***b* is unlikely to be equivalent to the chemical composition of either the pair of first copper containing residue layers **28***a* and **28***b* or the pair of first copper containing residue layers **28***c* and **28***d*.

[**0072**] Referring now to **FIG. 14**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 13**.

[**0073**] Shown in **FIG. 14** is a schematic cross-sectional diagram of a microelectronic fabrication otherwise equivalent to the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 13**, but wherein the pair of second copper containing residue layers **36***a* and **36***b* is stripped from the pair of patterned second passivation dielectric layers **20***c* and **20***d*. Within the preferred embodiment of the present invention, the pair of second copper containing residue layers **36***a* and **36***b* is stripped from the corresponding pair of patterned passivation dielectric layers **20***c* and **20***d* while employing methods and materials analogous or equivalent to the methods and materials employed for stripping from the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 4** the pair of first copper containing residue layers **28***a* and **28***b* to form the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 5** or stripping from the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 10** the pair of first copper containing residue layers **28***c* and **28***d* to form the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 11**. More particularly, the pair of second copper containing residue layers **36***a* and **36***b* as illustrated within the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 13** is stripped to provide the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 14** while employing a stripper composition comprising a non-aqueous coordinating solvent and a halogen radical producing specie, optionally and preferably followed by additional non-aqueous coordinating solvent rinsing and volatile solvent drying.

[**0074**] Upon forming the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 14** or the microelectronic fabrication whose schematic cross-sectional diagram is illustrated in **FIG. 5**, there is formed a microelectronic fabrication having formed therein a microelectronic structure comprising at least one copper containing conductor layer and a plurality of non-copper containing layers, where there is formed the microelectronic structure absent a copper containing residue layer formed upon any of the plurality of non-copper containing layers. The copper containing residue layer is absent incident to stripping within a stripper composition comprising a non-aqueous coordinating solvent and a halogen radical producing specie.

[**0075**] As is understood by a person skilled in the art, by employing the stripper composition comprising the non-aqueous coordinating solvent and the halogen radical producing specie for removing copper containing residue layers in accord with the preferred embodiments of the present invention, there may also be avoided when forming contacts to copper containing conductor layers within microelectronic fabrications, such as contacts to the first copper containing conductor layer **12** within the preferred embodiment of the present invention and the alternative preferred embodiment of the present invention, a pre-sputtering of the copper containing conductor layers. Such a pre-sputtering may typically be employed for removing copper oxide surface layers from those copper containing conductor layers. Such a pre-sputtering may be avoided since in addition to removing copper containing residue layers within microelectronic fabrications, copper oxide surface layers will also be removed employing the stripper composition of the present invention comprising the non-aqueous coordinating solvent and the halogen radical producing specie. As is similarly understood by a person skilled in the art, such pre-sputtering of copper containing conductor layers within microelectronic fabrications is undesirable insofar as there is often realized incident to such pre-sputtering: (1) insufficient copper oxide surface layer removal; (2) copper containing conductor layer sputtering within a via on the via sidewalls; and/or (3) reduced pre-sputtering tooling lifetime.

[**0076**] In addition to providing a method for forming a microelectronic fabrication comprising a copper containing layer and a non-copper containing layer absent a copper containing residue layer upon the non-copper containing layer, the present invention also provides an efficient method for recovery of copper, whether from copper containing

residue layers or from copper containing conductor layers, which are etched from a microelectronic fabrication in accord with the present invention. In that regard, there is illustrated within equation 1, as follows, a chemical equation which is believed to govern dissolution of copper within a dimethylsulfoxide (DMSO) non-aqueous coordinating solvent and a carbon tetrachloride halogen radical producing specie. Analogous chemical equations are contemplated for non-aqueous coordinating solvents other than dimethylsulfoxide (DMSO) and halogen radical producing species other than carbon tetrachloride.

$$Cu+CCl_4+(CH_3)_2SO \rightarrow CuCl_2((CH_3)_2SO)_x+CO+CO_2+CH_3Cl+(CH_3)_2S \quad (1)$$

[0077] Within equation 1, which is not intended as a balanced equation, but rather as an equation directed towards identifying reactants and reaction products, it is noted that all reaction products other than the dimethylsulfoxide (DMSO) solvated cupric chloride compound are volatile reaction products which are readily exhausted from a carbon tetrachloride/dimethylsulfoxide (DMSO) solvent mixture. Upon concentration of the carbon tetrachloride/dimethylsulfoxide (DMSO) solvent mixture, the dimethylsulfoxide (DMSO) solvated cupric chloride compound reaction product $CuCl_2((CH_3)_2SO)_x$ may be recrystallized, and thus recovered, possibly as a disolvated adduct.

[0078] In the alternative, the carbon tetrachloride/dimethylsulfoxide (DMSO) solvent mixture may be extracted with water which extracts the cupric chloride portion of the dimethylsulfoxide (DMSO) solvated cupric chloride complex into an aqueous phase from which it may subsequently, for example and without limitation, be electroplated and recovered as a metallic copper deposit.

[0079] As is understood by a person skilled in the art, the preferred embodiments of the present invention are illustrative of the present invention rather than limiting of the present invention. Revisions and modifications may be made to methods, materials structures and dimensions through which is provided a microelectronic fabrication in accord with the preferred embodiments of the present invention, while still providing microelectronic fabrications in accord with the present invention, in accord with the appended claims.

What is claimed is:

1. A method for forming a copper containing microelectronic structure comprising:

providing a substrate,

forming over the substrate a copper containing microelectronic structure comprising a copper containing layer and a non-copper containing layer, where the non-copper containing layer has formed thereupon a copper containing residue; and

stripping from the non-copper containing layer the copper containing residue while employing a stripper composition comprising a non-aqueous coordinating solvent and a halogen radical producing specie.

2. The method of claim 1 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

3. The method of claim 1 wherein the copper containing layer contains about 100 weight percent copper.

4. The method of claim 1 wherein the non-copper containing layer is selected from the group of non-copper containing layers consisting of non-copper containing conductor layers, non-copper containing semiconductor layers and non-copper containing dielectric layers.

5. The method of claim 1 wherein the halogen radical producing specie is a chlorine radical producing specie.

6. The method of claim 5 wherein the chlorine radical producing specie is chosen from the group of chlorine radical producing species consisting of C1-C2 perchloro and hydrochloro chlorine radical producing species.

7. The method of claim 5 wherein the chlorine radical producing specie is carbon tetrachloride (CCl4).

8. The method of claim 1 wherein the non-aqueous coordinating solvent is chosen from the group of non-aqueous coordinating solvents consisting of acetonitrile (CH3CN), tetrahydrofuran (THF) and dimethylsulfoxide (DMSO).

9. The method of claim 1 wherein the non-aqueous coordinating solvent is dimethylsulfoxide (DMSO).

10. A method for forming a copper containing microelectronic structure comprising:

providing a substrate;

forming over the substrate a copper containing microelectronic structure comprising a non-copper containing layer in conjunction with at least one of a copper containing layer and a copper containing residue; and

etching at least one of the copper containing layer and the copper containing residue while employing a stripper composition comprising a non-aqueous coordinating solvent and a halogen radical producing specie to form an etched microelectronic structure and a non-aqueous solvated copper halide compound dissolved within the non-aqueous coordinating solvent.

11. The method of claim 10 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications. solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

12. The method of claim 10 wherein the copper containing layer contains about 100 weight percent copper.

13. The method of claim 10 wherein the non-copper containing layer is selected from the group of non-copper containing layers consisting of non-copper containing conductor layers, non-copper containing semiconductor layers and non-copper containing dielectric layers.

14. The method of claim 10 wherein the halogen radical producing specie is a chlorine radical producing specie.

15. The method of claim 14 wherein the chlorine radical producing specie is chosen from the group of chlorine radical producing species consisting of C1-C2 perchloro and hydrochloro chlorine radical producing species.

16. The method of claim 14 wherein the chlorine radical producing specie is carbon tetrachloride (CCl4).

17. The method of claim 10 wherein the non-aqueous coordinating solvent is chosen from the group of non-aqueous coordinating solvents consisting of acetonitrile (CH3CN), tetrahydrofuran (THF) and dimethylsulfoxide (DMSO).

18. The method of claim 10 wherein the non-aqueous coordinating solvent is dimethylsulfoxide (DMSO).

19. The method of claim 10 further comprising recovering the copper from the copper halide compound.

20. The method of claim 19 wherein the copper is recovered by crystallizing a non-aqueous solvated copper halide compound from the non-aqueous solvent.

21. The method of claim 19 wherein the copper is recovered by extracting at least a portion of the copper halide compound into an aqueous solvent and electrodepositing therefrom a copper deposit.

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