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(54) **METHOD OF REDUCING WATER SPOTTING AND OXIDE GROWTH ON A SEMICONDUCTOR STRUCTURE**

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Publication Classification

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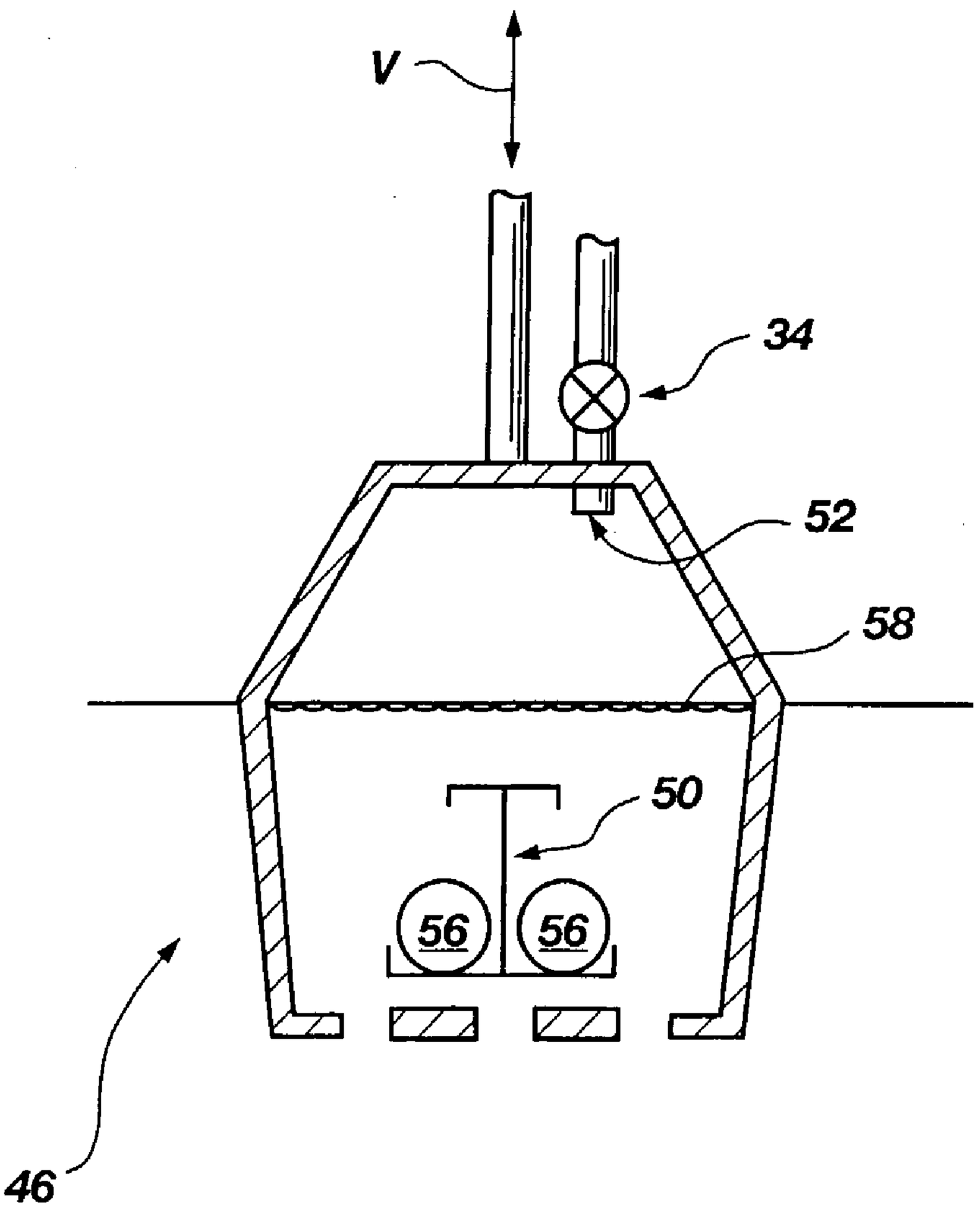
(57) **ABSTRACT**

The present invention relates to a method of cleaning and drying a semiconductor structure in a modified conventional gas etch/rinse or dryer.



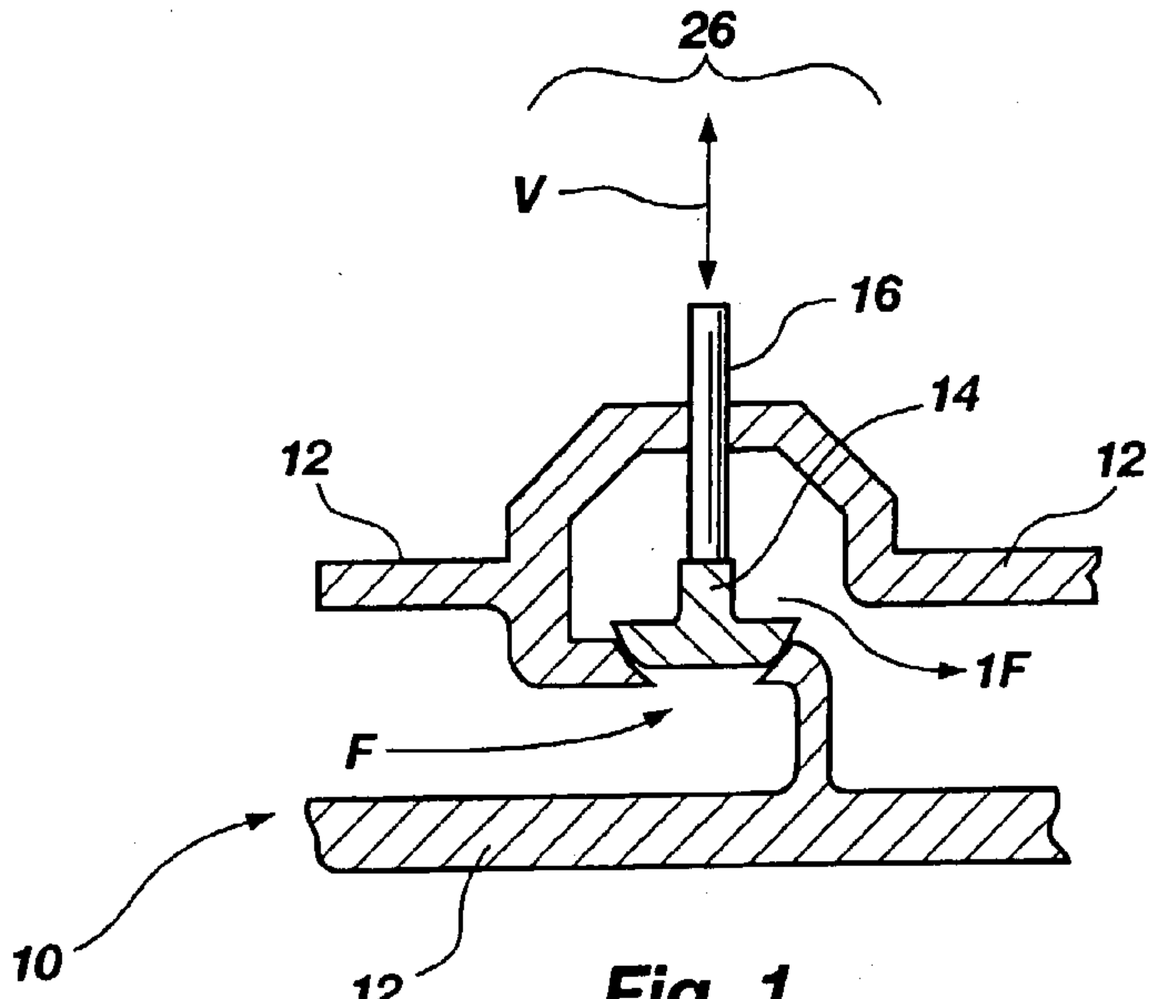


Fig. 1

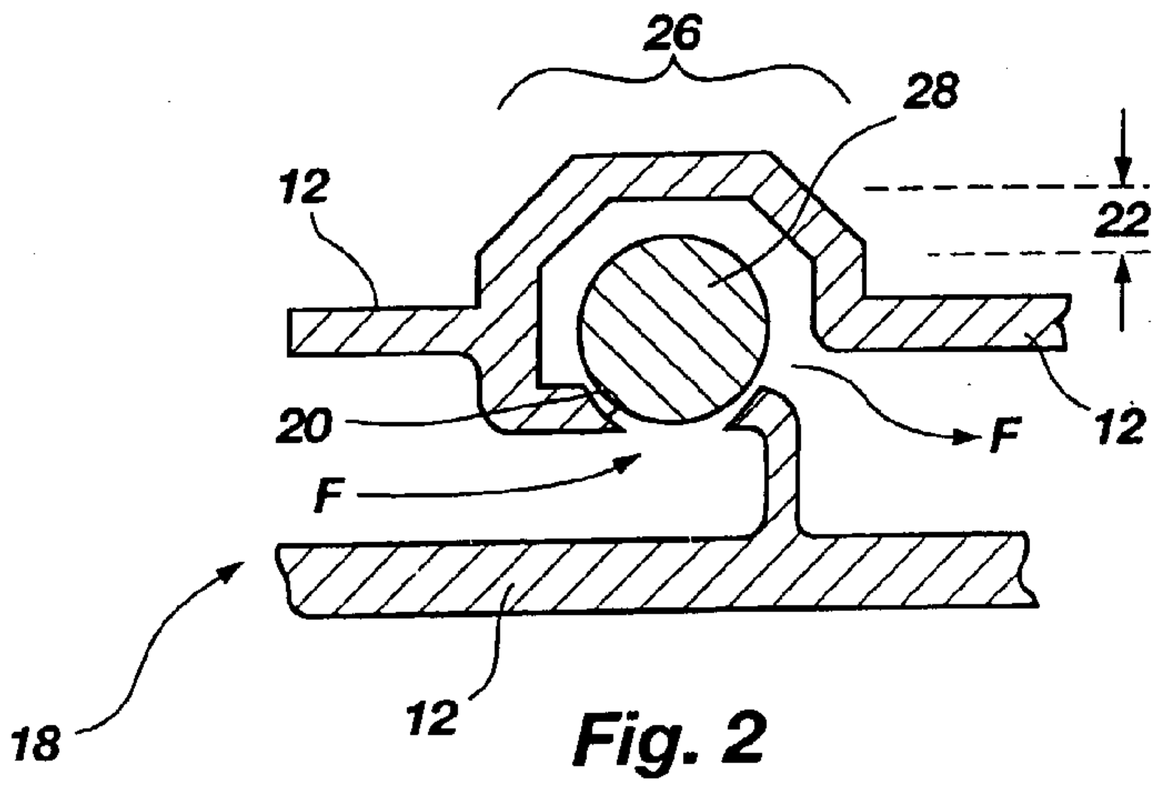


Fig. 2

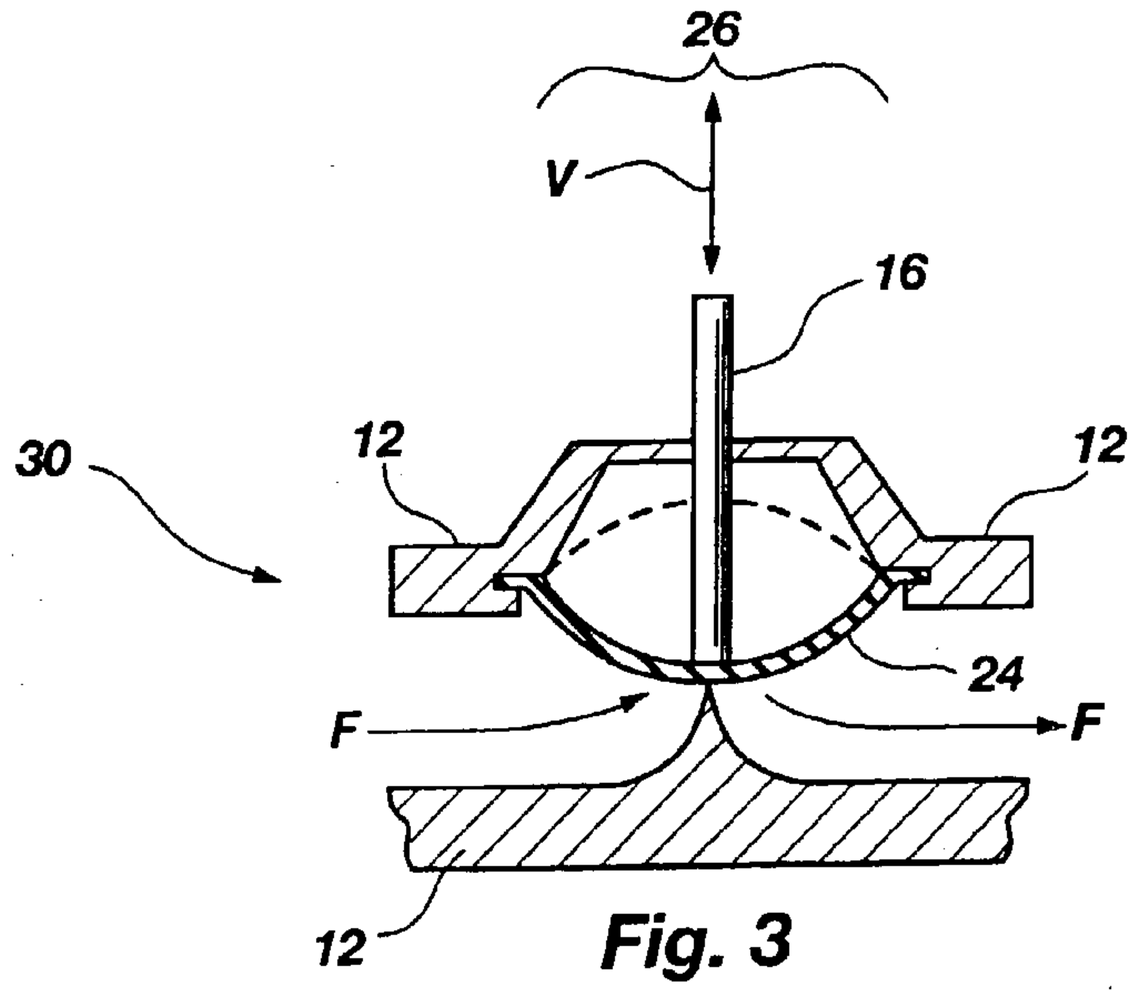


Fig. 3

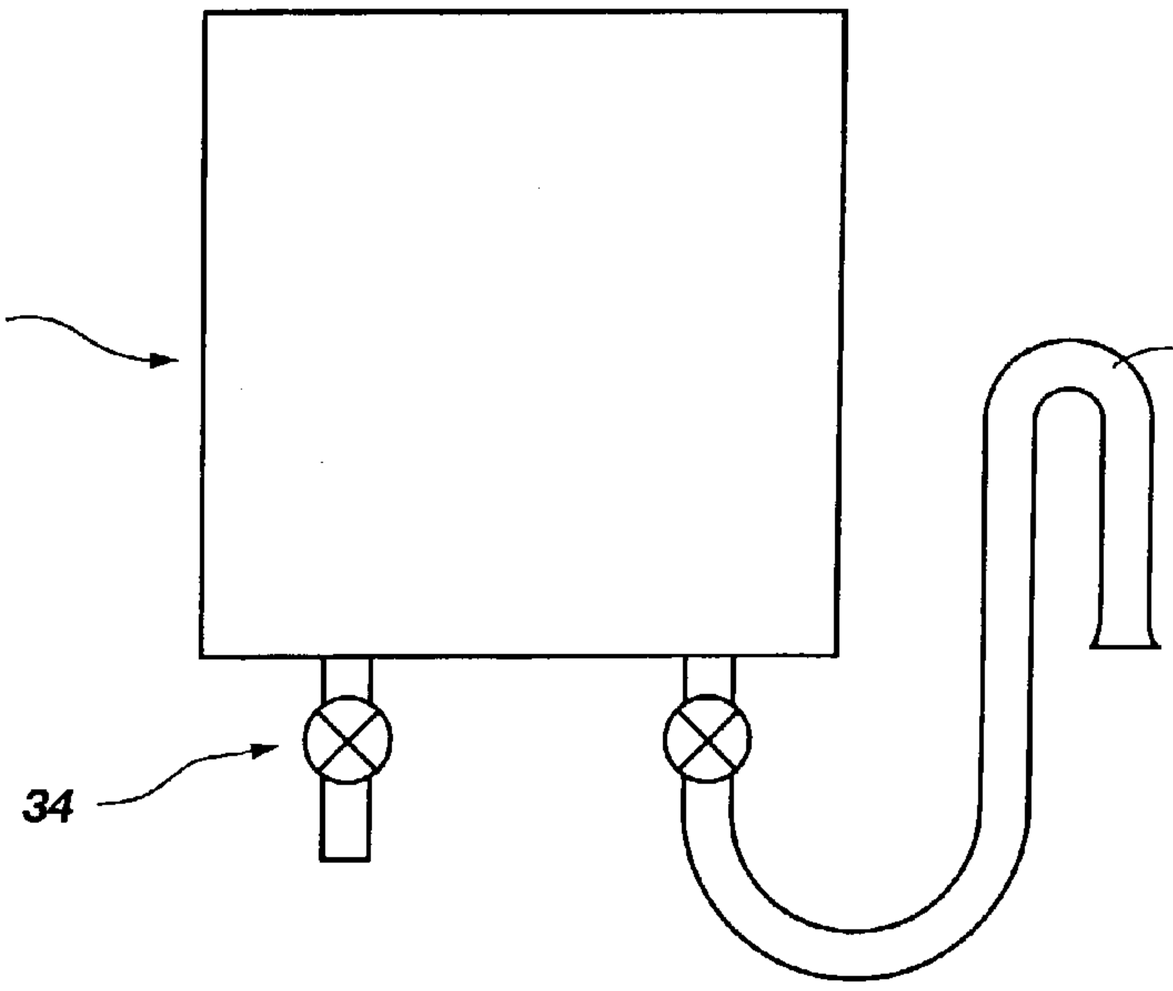


Fig. 4

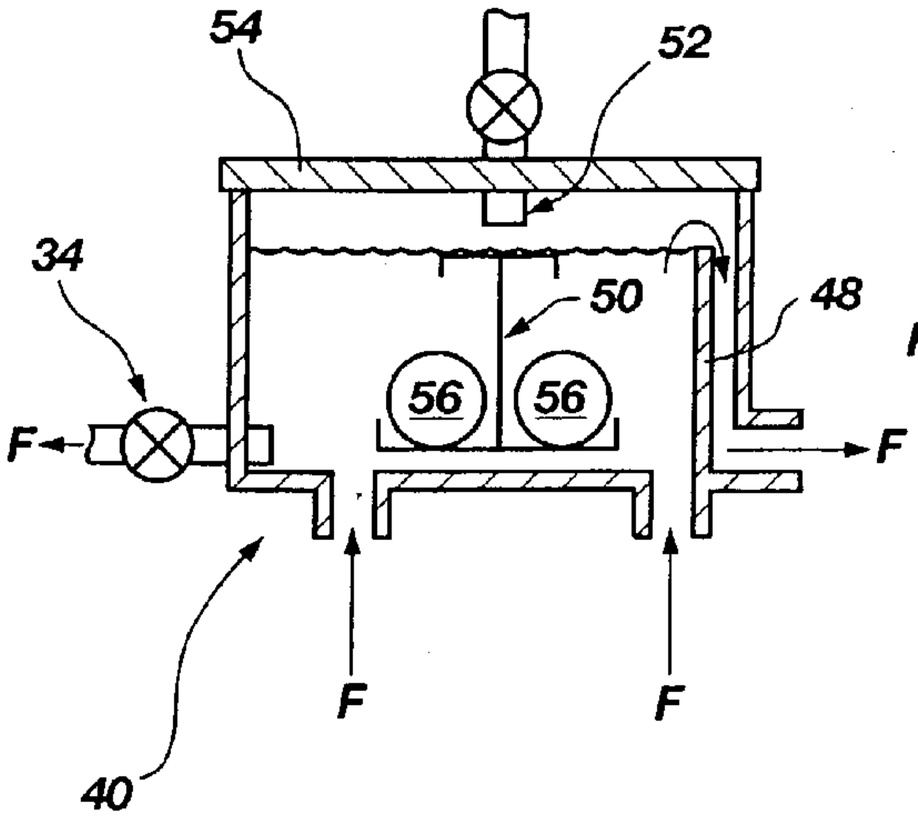


Fig. 5

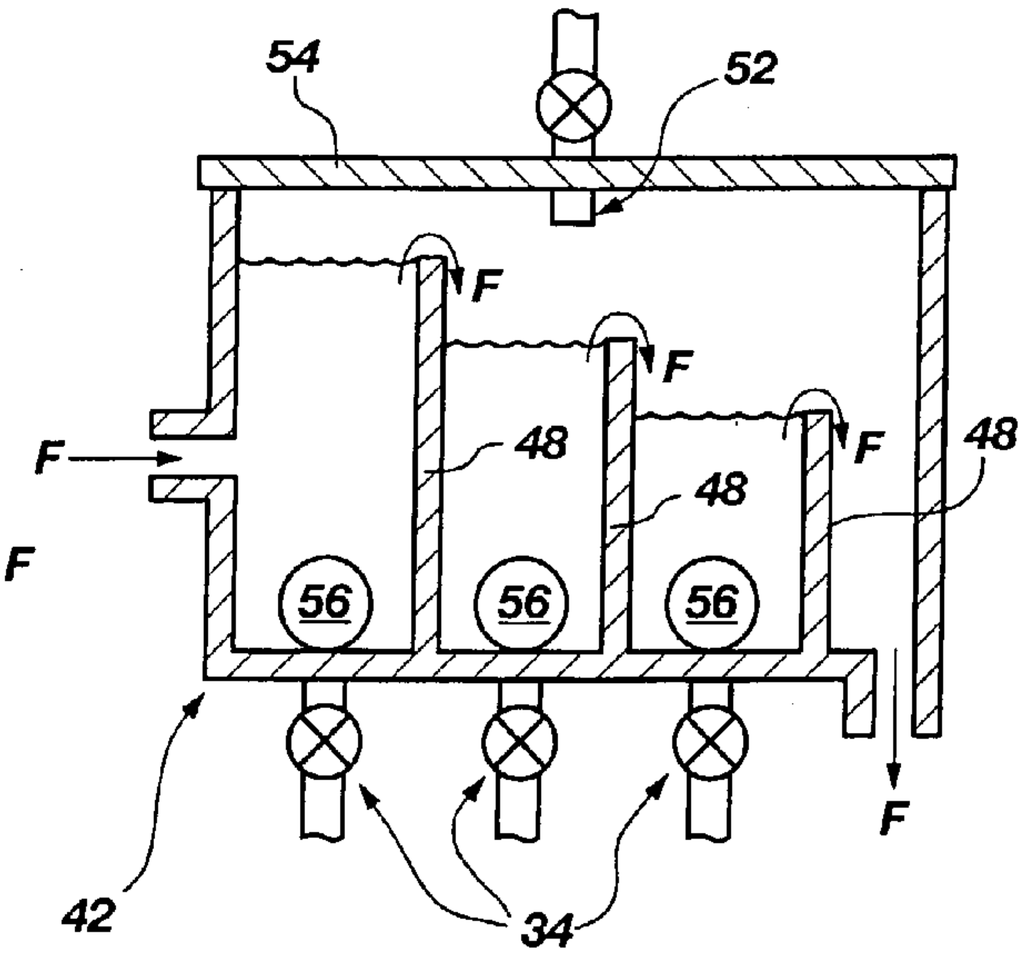


Fig. 6

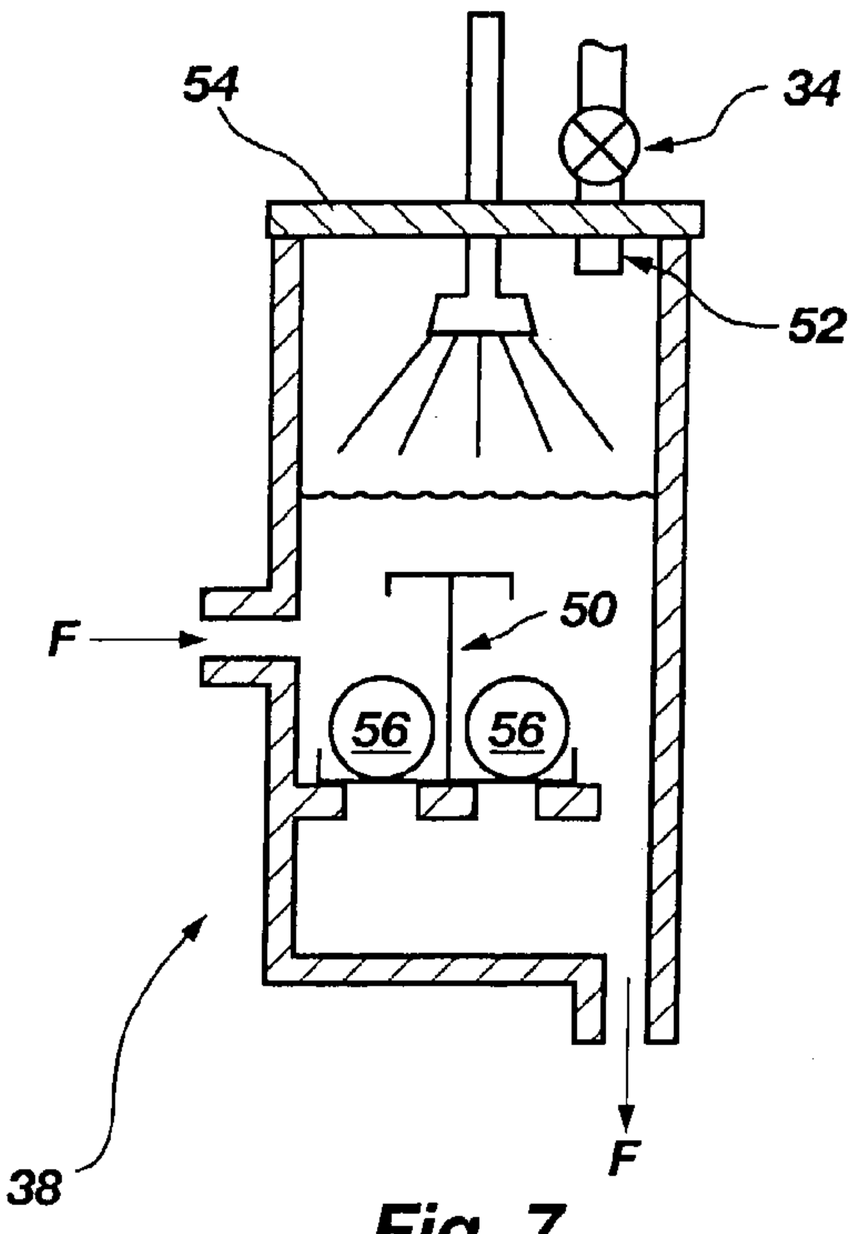


Fig. 7

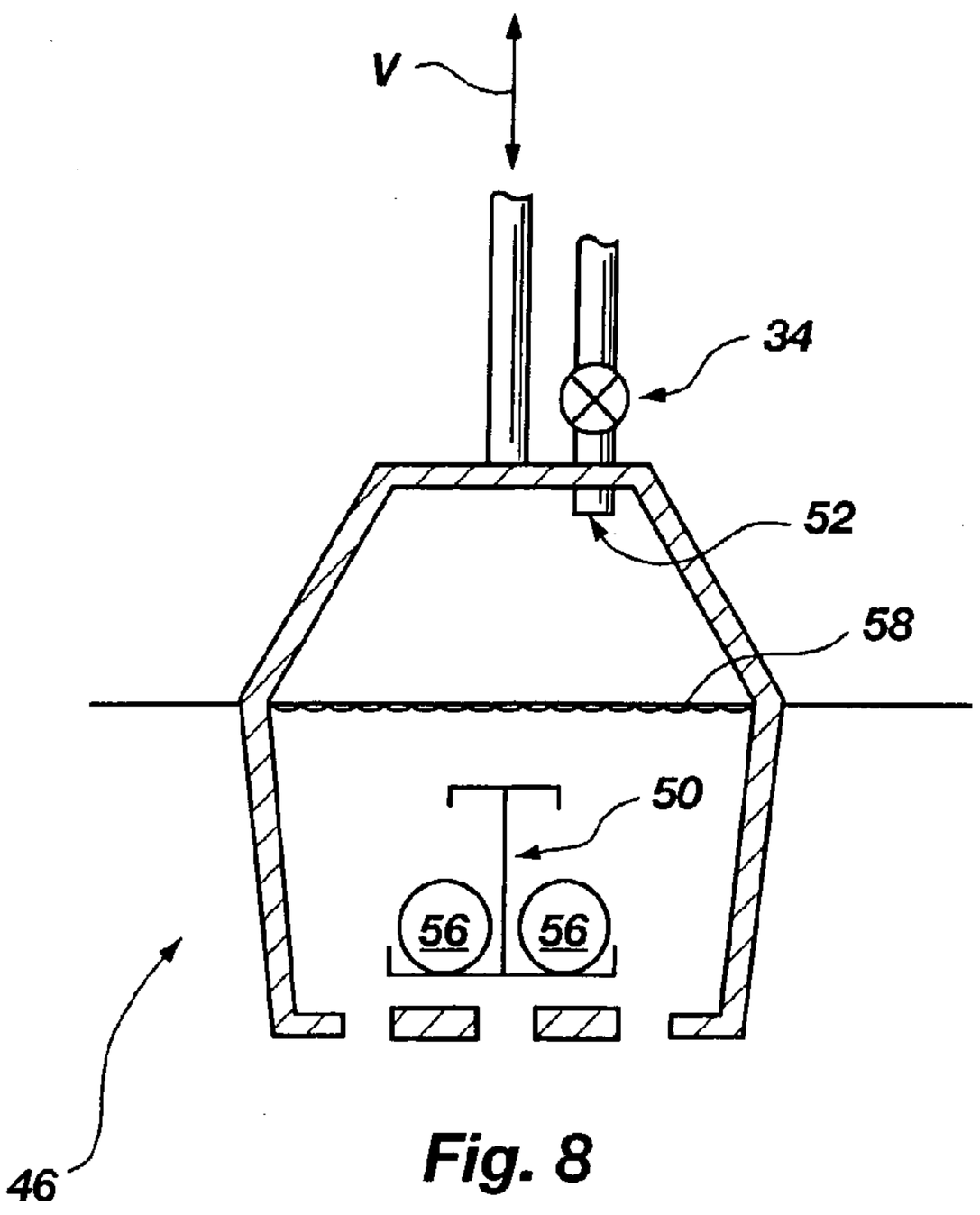


Fig. 8

METHOD OF REDUCING WATER SPOTTING AND OXIDE GROWTH ON A SEMICONDUCTOR STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of application Ser. No. 09/845,692, filed Apr. 30, 2001, pending, which is a divisional of application Ser. No. 09/427,920, filed Oct. 27, 1999, pending, which is a divisional of application Ser. No. 08/814,900, filed Mar. 12, 1997, now U.S. Pat. No. 6,350,322, issued Feb. 26, 2002.

BACKGROUND OF THE INVENTION

[0002] Field of the Invention: The present invention relates to drying semiconductor structures. More particularly, the present invention relates to the minimization of water spotting and of oxide growth that are experienced on semiconductor structures during chemical treatment steps, deionized (DI) water rinse steps, and drying steps. Examples of minimization of water spotting and of oxide growth are given for an HF rinse process in which the steps of DI water rinsing and drying are combined.

[0003] State of the Art: Producing a substantially impurity-free semiconductor structure is an ongoing challenge during fabrication of operable integrated circuits and other microelectronic devices. During fabrication, several operations are completed with a chemical treatment such as a polysilicon etching, a photoresist stripping, an RCA cleaning, or a buffered oxide etching (BOE). Following a chemical treatment, rinsing the structure to remove treatment chemicals is required.

[0004] Following a chemical treatment such as an HF rinse cleaning, a semiconductor structure is typically transferred to a vessel for a DI water rinse and then to a dryer to be dried. With each transfer of the semiconductor structure during fabrication between processing vessels, the possibility of contamination increases and, with that, also the likelihood of lower process yield. In chemical treatments of semiconductor structures that result in exposed hydrophobic surfaces, the possibility of oxidation and particle contamination is high.

[0005] During an HF-last rinse of a semiconductor structure with exposed silicon, for example, a significant number of $(Si)_2$=O bonds are changed to Si—H bonds. About ten to twenty percent of the changed bonds, however, are Si—F instead of the preferred Si—H. During the industry standard DI water rinse that follows most chemical treatments, the Si—F bonds in this example are easily washed off, and oxidation of semiconductor materials, such as silicon, occurs while transferring the semiconductor structure from a rinsing vessel to a drying vessel. Oxidation can occur both during the transfer to the drying vessel and while the semiconductor structure resides in the drying vessel prior to drying.

[0006] Before the semiconductor device is moved to the next fabrication phase, substantially complete drying must be accomplished because any water that remains on the surface of a semiconductor structure has the potential of interfering with subsequent processing. Drying can be accomplished in spin-rinse dryers (SRDs), Marangoni dryers, axial dryers and others used in the art.

[0007] Various drying techniques such as spin drying also cause water spotting. During spin drying, water spotting droplet tracks are left on the hydrophobic faces of the semiconductor structures. These water spotting tracks are formed from slight impurities contained in the DI water droplets. Water spotting is caused due to the hydrophobic nature of the cleaned silicon and other surfaces such as metallization lines.

[0008] As DI water is spun off from the hydrophobic face of a semiconductor structure, water droplet size decreases. Any portion of the DI water droplet that is not pure water is attracted to the hydrophobic surfaces of the semiconductor structure, while the water portion is repelled. Because the water droplets become exceedingly small, dissolved impurities are more strongly attracted to the hydrophobic surfaces of the semiconductor structure than they are to remaining in solution within the water droplet.

[0009] The Marangoni drying technique reduces water spotting that is incident to spin drying. In the Marangoni drying technique, a chemically treated semiconductor structure is DI water rinsed, transferred to the Marangoni dryer, immersed in a DI water bath, and drawn through an isopropyl alcohol (IPA) layer that rests on the surface of the DI water bath. In the Marangoni technique, the forces that attract impurities to exposed hydrophobic semiconductor structure surfaces are balanced by the bulk of the water in the relatively pure DI water bath that tends to keep the impurities in solution. When employing the Marangoni drying technique, the DI water and its impurities are entrained beneath the water-IPA interface while the semiconductor structure is drawn through the interface.

[0010] Marangoni drying reduces water spotting, but it does not ameliorate oxidative contamination that occurs upon a semiconductor structure during transfer of the semiconductor structure from the DI water rinsing vessel to the dryer. Thus, elimination of the deleterious effects of water spotting may be overshadowed by contamination of the semiconductor structure experienced simply during transfer from one vessel to another.

[0011] Because a Marangoni dryer may have moving parts, the function of which is to draw a wafer boat out of a DI water bath, the possibility of particulate contamination arises, which contamination is caused by abrasion of surfaces on the moving parts.

[0012] What is needed is a method of rinsing and drying semiconductor structures, particularly hydrophobic semiconductor structures, in such a way as to substantially eliminate oxide contamination incident to semiconductor structure transfer from vessel to vessel and by water spotting incident to spin drying. What is also needed is a device that will accomplish the inventive method while simplifying the Marangoni technique and equipment.

BRIEF SUMMARY OF THE INVENTION

[0013] The present invention relates to a method of cleaning and drying semiconductor structures. The present invention also relates to a method of using a conventional gas etch/rinse vessel, or a conventional dryer vessel. The present invention also relates to an apparatus that accomplishes the inventive method. The present invention reduces the likelihood of oxide contamination and the like, as well as the incidence of water spotting.

[0014] In a first embodiment of the present invention, a semiconductor structure is placed into a first treatment vessel for a chemical treatment. Following the chemical treatment, the semiconductor structure is transferred directly from the first treatment vessel to a second treatment vessel. The semiconductor structure is rinsed with DI water in the second treatment vessel. Next, the second treatment vessel is flooded with DI water to form a DI water bath. The second treatment vessel may also be optionally flooded with a gas that is inert to the ambient, such as nitrogen, to form an inert atmosphere in the second treatment vessel. The inert gas forming the inert atmosphere is intended herein to mean a gas that does not substantially react with or otherwise contaminate the semiconductor structure or the vessel in which the inert atmosphere is formed under the processing conditions set forth herein. The inert atmosphere is maintained during rinsing. Following rinsing, a gaseous stream, such as nitrogen, that is laden with IPA vapor is fed into the second treatment vessel.

[0015] After a selected period of time, a layer of IPA has formed upon the surface of the DI water bath to form an IPA-DI water interface. The semiconductor structure is drawn out of the DI water bath at a preferred rate that causes substantially all the DI water, and contaminants therein, to be entrained beneath the IPA-DI water interface.

[0016] In a second embodiment of the present invention, a dry etch is performed. The process of the second embodiment comprises first placing a semiconductor structure into a gas etch chamber. After placing a semiconductor structure into a gas etch chamber, the gas etch chamber is sealed and gas etching of the semiconductor structure commences. Following gas etching, the semiconductor structure is rinsed with DI water. After rinsing and an optional washing of the semiconductor structure in the gas etch chamber, the gas etch chamber is purged of any gas that is not inert to the semiconductor structure or to the gas etch chamber. The semiconductor structure is then submerged in DI water by flooding the gas etch chamber, wherein a surface of DI water forms above the semiconductor structure. Nitrogen gas laden with IPA vapor is introduced into the gas etch chamber to form an IPA-DI water interface upon the surface of the DI water. Finally, the gas etch chamber is drained by displacing the DI water bath with more IPA-laden nitrogen. As the gas etch chamber is drained at a preferred rate, the IPA-DI water interface functions as a dynamic barrier to the DI water and substantially "wipes down" the semiconductor structure by substantially entraining the DI water, and contaminants therein, beneath the IPA.

[0017] In a third embodiment of the present invention, a rinser is retrofitted with a lid and a fail-shut valve. In the third embodiment, the process of chemical treatment is carried out conventionally, but DI water rinsing and drying both occur within the rinser. Following sufficient rinse cycles, IPA-laden nitrogen is fed into the rinser in a manner similar to the method of the second embodiment. Entrainment of substantially all DI water, and contaminants therein, beneath the IPA layer is accomplished by displacement of the last spray/dump DI water volume with an IPA-DI water interface as set forth above. In this embodiment, retrofitted rinsers include spray/dump rinsers, overflow rinsers, cascade rinsers, and Marangoni dryers that have been retrofitted with rinsing capabilities.

[0018] These and other features of the present invention will become more fully apparent from the following description and appended claims, or may be learned by the practice of the invention as set forth hereinafter.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0019] In order to obtain the above-recited and other advantages of the invention, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are not, therefore, to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[0020] **FIG. 1** is a cross-sectional elevational view of a glove valve that can be installed in a Marangoni dryer, a spray/dump rinser, and other wet processing vessels in order to practice the method of the present invention;

[0021] **FIG. 2** is a cross-sectional elevational view of a check valve that can be installed in a Marangoni dryer, a spray/dump rinser, and other wet processing vessels in order to practice the method of the present invention;

[0022] **FIG. 3** is a cross-sectional elevational view of a diaphragm valve that can be installed in a Marangoni dryer, a spray/dump rinser, and other wet processing vessels in order to practice the method of the present invention;

[0023] **FIG. 4** is an elevational side view of a treatment vessel used in the method of the present invention in which fail-shut valves or simple gate valves are used to allow draining of the treatment vessel according to the method of the present invention;

[0024] **FIG. 5** is an elevational side view of a sealed overflow rinse vessel used in the present invention in which a vessel wall is illustrated as transparent;

[0025] **FIG. 6** is an elevational side view of a sealed spray/dump rinse vessel used in the present invention in which a vessel wall is illustrated as transparent;

[0026] **FIG. 7** is an elevational side view of a sealed cascade rinse vessel used in the present invention in which a vessel wall is illustrated as transparent; and

[0027] **FIG. 8** is an elevational side view of a sealed Marangoni dryer type rinse/dry vessel used in the present invention in which a vessel wall is illustrated as transparent.

DETAILED DESCRIPTION OF THE INVENTION

[0028] The present invention relates to a method of cleaning and drying semiconductor structures. The present invention also relates to a method of using a conventional gas etch/rinse vessel, or a conventional dryer, or a conventional rinser in conjunction with the inventive method. The present invention also relates to an apparatus that accomplishes the inventive method. The present invention reduces the likelihood of oxide contamination or the like, as well as the incidence of water spotting.

[0029] Rinsing by the method of the present invention is usually carried out with DI water. Other rinsing solutions may be used such as aqueous hydrogen peroxide. Drying by the method of the present invention comprises forming a substantially continuous layer of a drying liquid upon the upper surface of a DI water bath in which the semiconductor structure is submerged. Following formation of the substantially continuous layer of the drying liquid, the semiconductor structure is drawn through the substantially continuous layer of the drying liquid. Both the DI water and contaminants therein are entrained beneath the substantially continuous layer of the drying liquid in the DI water bath and are, therefore, substantially removed from the semiconductor structure.

[0030] The drying liquid comprises a volatile liquid such as IPA. Other drying liquids are contemplated to be, but need not be, derived from an anhydrous organic vapor, such as acetone, chloroform, methanol, carbon tetrachloride, benzene, ethanol, ethyl acetate, hexane, 1-propanol, and 2-propanol, and equivalents. By reading the disclosure of the present invention and by practicing the present invention, one of ordinary skill in the art will recognize that anhydrous organic liquids or the like may be used in the method of the present invention. The skilled practitioner will recognize that, although a water-miscible drying liquid such as IPA may be used, such liquids are preferred to be more volatile than the DI water used for rinsing, and such liquids are preferred in that they are not prone to cause deleterious chemical effects upon the semiconductor structure.

[0031] In order to avoid unwanted oxidation or other contamination incident to ambient air exposure that may occur during and after rinsing, the method of the present invention comprises filling the rinsing vessel with a gas that will not react detrimentally with the semiconductor structure. The gas preferably will be inert to both the semiconductor structure and to the rinsing vessel, such as nitrogen. Other gases that may be used include all the noble gases, methane, ethane, and the like. Other gases may include the drying liquid in vapor form. The preferred gas, if a gas is used, is nitrogen.

[0032] In a first embodiment of the present invention, a semiconductor structure is placed into a first treatment vessel and chemically treated. Chemical treatment may be any number of treatments such as rinsing the semiconductor structure in an aqueous HF solution, performing an HF dry etch on the semiconductor structure, performing a buffered oxide etch on the semiconductor structure, performing a polysilicon etch on the semiconductor structure, other wet or dry etching processes, photoresist stripping, or RCA cleaning. In an example of the first embodiment, an HF rinse is carried out in which aqueous HF contacts the semiconductor structure and is optionally filtered and recirculated. The aqueous HF is discarded after a number of uses, depending upon the specific application.

[0033] Following the chemical treatment step, a rinsing step is carried out usually by transferring the semiconductor structure to a second treatment vessel and performing a DI water rinse. DI water rinsing vessels are known in the art such as a cascade rinser, an overflow rinser, a spray/dump rinser, a spin/rinse dryer, an etcher/rinser, and others. In the first embodiment of the present invention, the rinsing vessel is omitted. The semiconductor structure is transferred directly from the first treatment vessel to a second treatment vessel, rinsed in the second treatment vessel, and then dried. In this first embodiment of the present invention, the semiconductor structure is transferred from an HF-last cleaning vessel to a Marangoni dryer that has been retrofitted with means for contacting the semiconductor structure with DI water, such as with spray nozzles for rinsing the semiconductor structure.

[0034] In the first example of the first embodiment of the present invention, most of the hydrophobic surfaces of the semiconductor structure are hydrogen terminated, e.g. M-H, where M represents Si, Al, Al alloys, and other metals. About ten to twenty percent of the bonds, however, are M-F instead of the preferred M-H. Because significant oxidation occurs only after the rinsing, and because significant water spotting occurs only during spin drying or post-rinse (pre-dry) atmospheric exposure, exposing the semiconductor structure to the ambient by transferring it from an HF rinsing treatment vessel to a rinse/dry treatment vessel under conventional clean room conditions results in some contamination of the semiconductor structure. The inventive method, therefore, does not expose the semiconductor structure to ambient air after rinsing.

[0035] The second treatment vessel is flooded with an inert gas such as nitrogen to create an inert atmosphere, and the inert atmosphere is maintained during rinsing. Maintaining an inert atmosphere prevents unwanted oxidation caused by oxygen contact with freshly broken M-F bonds that occur during rinsing. Alternatively, no inert gas per se is used, but rather the second treatment vessel is flooded with an anhydrous organic vapor such as with IPA vapor. Rinsing is carried out in such a way that the IPA vapor is not substantially flushed from the second treatment vessel.

[0036] Rinsing is commenced within the second treatment vessel. Following appropriate rinsing, the second treatment vessel is optionally cleaned and a DI water bath is formed in the second treatment vessel. A nitrogen stream that is laden with IPA vapor is fed into the second treatment vessel. Alternatively, an IPA stream with no nitrogen or other inert gas acting as a carrier is fed to the second treatment vessel. After a preferred period of time, a layer of IPA has formed upon the surface of the DI water bath to form an IPA-DI water interface. When a sufficient layer of IPA vapor has formed upon the surface of the DI water bath, the semiconductor structure is drawn out of the DI water bath at a rate that allows substantially all DI water, and contaminants therein, on the semiconductor structure to be entrained beneath the IPA-DI water interface. Impurities in the DI water bath are substantially all retained in the DI water bath as the semiconductor structure is drawn through the IPA-DI water interface. By this method, unwanted oxidation incident to ambient exposure of the semiconductor structure is minimized, and unwanted water spotting incident to spin drying and to post-rinse atmospheric exposure is eliminated.

[0037] In a second embodiment of the present invention, the chemical treatment is an HF gas etch, by way of non-limiting example. Other etching may be carried out, such as wet or dry etching. Following the chemical treatment, a DI water rinse followed by drying is carried out. Single-chamber HF gas etching may be done, or multiple-chamber etching may be done by using an apparatus such as

that described in U.S. Pat. No. 5,089,084 issued to Chhabra et al., the disclosure of which is incorporated herein by specific reference.

[**0038**] The process of the second embodiment comprises first placing a semiconductor structure into a gas etch chamber. The gas etch chamber is sealed and gas etching of the semiconductor structure commences. Following gas etching, the semiconductor structure is rinsed with DI water in an inert atmosphere and optionally washed in the gas etch chamber. The semiconductor structure is then submerged in DI water by flooding the gas etch chamber with DI water, wherein a surface of DI water forms above the semiconductor structure. An inert carrier gas, such as nitrogen gas laden with IPA vapor, is introduced into the gas etch chamber to form an IPA-DI water interface upon the surface of the DI water. Alternatively, an IPA vapor without an inert carrier gas is introduced into the gas etch chamber to form an IPA-DI water interface upon the surface of the DI water. Finally, the gas etch chamber is drained by displacing the DI water bath with more IPA-laden nitrogen, by more IPA alone, or by nitrogen alone, whereby the IPA layer entrains the DI water, and contaminants therein, beneath itself while the DI water is draining or being displaced.

[**0039**] The method of draining the gas etch chamber by displacing the DI water bath with a gas or a vapor, or both, can be accomplished by installing an effluent valve, as seen in FIGS. **1-3**, in the gas etch chamber at a level below the lowest portion of the semiconductor structure. A preferred valve is one that is fail-shut, but that opens by sufficient positive pressure on the gas etch chamber side of the valve. In **FIG. 1, a** glove valve **10** is installed within an effluent pipe **12** that can be installed in a gas etch chamber according to the second embodiment of the present invention. Glove valve **10** comprises a stopper **14** that is part of a valve housing **26** that is part of effluent pipe **12**. Stopper **14** is attached to a valve shaft **16** that moves in directions V. Valve shaft **16** may be attached to a spring or some other device that provides stopper **14** with a selected resistance against allowing an effluent flow F therethrough. The selected resistance can be chosen depending upon the specific application.

[**0040**] In an example of the second embodiment of the present invention, a preferred IPA-DI water interface thickness is selected to optimize entrainment beneath the IPA-DI water interface of all dissolved impurities contained within the DI water bath. A selected resistance is set to resist movement of valve shaft **16** caused by pressure against the gas etch chamber side of stopper **14**. The selected resistance allows a specific pressure within the gas etch chamber, such that the IPA-DI water interface will have a preferred thickness, and such that displacement of the DI water bath is accomplished only by further feeding of the gases, such as IPA-laden nitrogen, IPA alone, or nitrogen alone, to the gas etch chamber.

[**0041**] Another valve scheme, seen in **FIG. 2**, includes a check valve **18** that comprises a ball **28** that rests in a fail-shut mode against a sphere-contoured valve seat **20**. One advantage of check valve **18** is that no moving part must breach valve housing **26**, such as is seen in **FIG. 1** where valve shaft **16** is required for a glove valve or a diaphragm valve. With no breach of valve housing **26**, the possibility of abraded parts caused by dynamic frictional contact of valve shaft **16** against valve housing **26** is eliminated.

[**0042**] Check valve **18** can be configured within valve housing **26** such that a selected clearance **22** limits how high ball **28** of check valve **18** may rise and, therefore, how large an effluent opening allows effluent flow F to pass through. It can be seen in **FIG. 2** that clearance **22** could be configured to allow ball **28** of check valve **18** to move less than one diameter thereof, or to move greater than one diameter thereof. It will be appreciated by one of ordinary skill in the art that using the present disclosure as a guide, clearance **22** may be adjusted within a single valve housing by placing a screw or piston above ball **28** of check valve **18** to adjustably limit its upward motion.

[**0043**] Thus, for a process that merits well-defined process parameters and that is part of a high-volume fabrication, clearance **22** of valve housing **26** for check valve **18** may be unadjustable. On the other hand, for an apparatus that is used for various processes that require selected dissimilar conditions, valve housing **26** for check valve **18** may have an adjustable clearance **22**.

[**0044**] Another valve scheme is a diaphragm valve **30** illustrated in **FIG. 3**. Diaphragm valve **30** comprises a flexible diaphragm **24** that is connected to valve shaft **16** similarly to glove valve **10**. It can be appreciated by one of ordinary skill in the art that the function of the valves illustrated in FIGS. **1-3** can also be accomplished by a simple goose neck, wherein the height of the goose neck may be selected to allow pressures that optimize the IPA-DI water interface or other processing parameters as the gas etch chamber is drained.

[**0045**] The process of entraining DI water and thereby substantially removing DI water, and contaminants therein, from the semiconductor structure by the method of the present invention may be accomplished in the second embodiment by a rapid displacement of the DI water bath such that the IPA layer "wipes down" the semiconductor structure in a substantially continuous stroke. A rapid displacement may be accomplished, for example, by pushing IPA-laden nitrogen from a piston that displaces a volume approximately equal to the volume of the gas etch chamber.

[**0046**] Where a rapid displacement of the DI water bath from the gas etch chamber is not a preferred variation of draining the gas etch chamber, IPA-laden nitrogen may be fed to the gas etch chamber by conventionally used equipment and methods such as those used in a STEAG® Marangoni dryer.

[**0047**] A third embodiment of the present invention comprises a retrofitted spray/dump rinser with a rinser-sealable lid **54** and a valve **34** such as those depicted in FIGS. **4-6**. In the third embodiment, the process of chemical treatment is carried out conventionally, but DI water rinsing and drying both occur within the rinser. Following sufficient spray/dump cycles, IPA-laden nitrogen or the like is fed into the rinser in a manner similar to the method of the second invention. Removal of DI water from the semiconductor structure comprises displacement of the last spray/dump DI water volume by forming an IPA-DI water interface as set forth above.

[**0048**] The artisan will appreciate that other rinsers may be retrofitted to practice the method of the present invention. For example, an overflow rinser or a cascade rinser may be retrofitted, as well as spinner rinser/dryers. **FIG. 5** illustrates

an elevational side view of an overflow rinser **40** that has been retrofitted with a lid **54**, a vapor-gas inlet **52**, a semiconductor structure holder **50**, and at least one, fail-shut valve **34** or a goose neck. During the process of passing an IPA-DI water interface across a semiconductor structure **56**, IPA-laden nitrogen gas or the like is fed through vapor-gas inlet **52** while influent DI water that normally enters from below overflow rinser **40** is shut off.

[**0049**] **FIG. 6** illustrates an elevational side view of a retrofitted cascade rinser **42** in which semiconductor structure **56** is substantially batch treated instead of counter-current treated. Influent DI water flows in the direction F and spills over weirs **48**. After sufficient rinsing, such that semiconductor structure **56** contacted with the DI water that is about to exit cascade rinser **42** is substantially as thoroughly rinsed as semiconductor structure **56** contacted with the first influent DI water, influent DI water is shut off and IPA-laden nitrogen gas or the like is fed through vapor-gas inlet **52**. Fail-shut valves **34** are opened and the pressure of influent IPA-laden nitrogen gas that is fed through vapor-gas inlet **52** displaces all DI water contained within cascade rinser **42**.

[**0050**] Draining each stage in cascade rinser **42** may require that fail-shut valve **34** in the deepest stage be opened first. DI water then drains from the deepest stage until the DI water depth in the deepest stage matches that of the next deepest stage, at which point fail-shut valve **34** in that stage opens, and so forth for each stage.

[**0051**] Another method of assuring uniform draining of each stage relative to semiconductor structures **56** is to set semiconductor structures **56** upon racks (not shown). By placing semiconductor structures **56** upon racks, the semiconductor structure **56** in the deepest stage will have completely surfaced before all DI water has exited from the shallowest stage.

[**0052**] **FIG. 7** illustrates an elevational side view of a spray/dump rinser **38** that has been retrofitted with sealable lid **54** and vapor-gas inlet **52**. In the method of the present invention, the normal spray/dump cycle is carried out in an inert atmosphere that may be supplied through vapor-gas inlet **52**. The final flooding of spray/dump rinser **38** comprises forming an IPA layer upon the DI water bath and either drawing semiconductor structure **56** through the IPA surface or draining the DI water bath as set forth above such that the IPA surface passes across semiconductor structure **56**.

[**0053**] **FIG. 8** illustrates an elevational side view of a Marangoni type dryer **46** in which semiconductor structures **56** are held in semiconductor structure holder **50**. In the method of the present invention, rinsing is carried out within Marangoni type dryer **46** in an inert atmosphere. The method concludes by drawing semiconductor structure **56** through an IPA layer **58**, or by draining the DI water bath such that IPA layer **58** passes across semiconductor structure **56**. As semiconductor structure **56** and IPA layer **58** pass each other, the DI water bath, and contaminants therein, are entrained beneath IPA layer **58** such that substantially all DI water is removed from semiconductor structure **56**.

[**0054**] The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims and their combination in whole or in part rather than by the foregoing description. All changes that come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed is:

1. A method of treating a semiconductor structure in a single treatment vessel, comprising:

providing a treatment vessel;

performing a first treatment upon said semiconductor structure in a first portion of the treatment vessel;

rinsing said semiconductor structure in a second portion of the treatment vessel; and

drying said semiconductor structure in the second portion of the treatment vessel.

2. The method of claim 1, wherein the first treatment comprises a chemical treatment.

3. The method of claim 1, wherein the first treatment comprises a chemical process treatment selected from the group consisting of rinsing said semiconductor structure in an aqueous HF solution, performing an HF dry etch on said semiconductor structure, performing a buffered oxide etch on said semiconductor structure, and performing a polysilicon etch on said semiconductor structure.

4. The method of claim 1, further comprising:

injecting a first gas that is inert to said semiconductor structure into the second portion of the treatment vessel.

5. The method of claim 4, wherein the step of rinsing said semiconductor structure includes:

rinsing said semiconductor structure with deionized water in the presence of the first gas.

6. The method of claim 5, further comprising:

submerging said semiconductor structure in a deionized water bath in the second portion of the treatment vessel.

7. The method of claim 4, wherein the first gas includes nitrogen.

8. The method of claim 5, further comprising:

forming a liquid layer on a surface of the deionized water bath in the second portion of the treatment vessel.

9. The method of claim 5, wherein the first gas includes isopropyl alcohol.

10. The method of claim 5, wherein the first gas includes isopropyl alcohol in a nitrogen carrier.

11. The method of claim 6, further comprising:

separating said semiconductor structure from the deionized water bath.

12. The method of claim 11, wherein the step of separating said semiconductor structure from the deionized water bath comprises drawing said semiconductor structure from the deionized water bath.

13. The method of claim 11, wherein the step of separating said semiconductor structure from the deionized water bath comprises draining the deionized water bath from the treatment vessel.

14. The method of claim 13, wherein the draining of the deionized water bath from the treatment vessel includes

purging the second portion of the treatment vessel with an anhydrous organic liquid in an inert gas carrier.

15. A method of treating a semiconductor structure in a first portion and a second portion of a single treatment vessel, comprising:

performing a first treatment upon said semiconductor structure in a first portion of the treatment vessel;

rinsing said semiconductor structure in a second portion of the treatment vessel; and

drying said semiconductor structure in the second portion of the treatment vessel.

16. The method of claim 15, wherein the first treatment comprises a chemical treatment.

17. The method of claim 15, wherein the first treatment comprises a chemical process treatment selected from the group consisting of rinsing said semiconductor structure in an aqueous HF solution, performing an HF dry etch on said semiconductor structure, performing a buffered oxide etch on said semiconductor structure, and performing a polysilicon etch on said semiconductor structure.

18. The method of claim 15, further comprising:

injecting a first gas that is inert to said semiconductor structure into the second portion of the treatment vessel.

19. The method of claim 18, wherein the step of rinsing said semiconductor structure includes: rinsing

said semiconductor structure with deionized water in the presence of the first gas.

20. The method of claim 15, further comprising:

submerging said semiconductor structure in a deionized water bath in the second portion of the treatment vessel.

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