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(54) METHOD OF FORMING PREDOMINANTLY POLYCRYSTALLINE SILICON THIN FILM TRANSISTORS

(76) Inventor: **Apostolos Voutsas**, Vancouver, WA (US)

Correspondence Address:
Matthew D. Rabdau
Patent Attorney
Sharp Laboratories of America, Inc.
5750 NW Pacific Rim Boulevard
Camas, WA 98607 (US)

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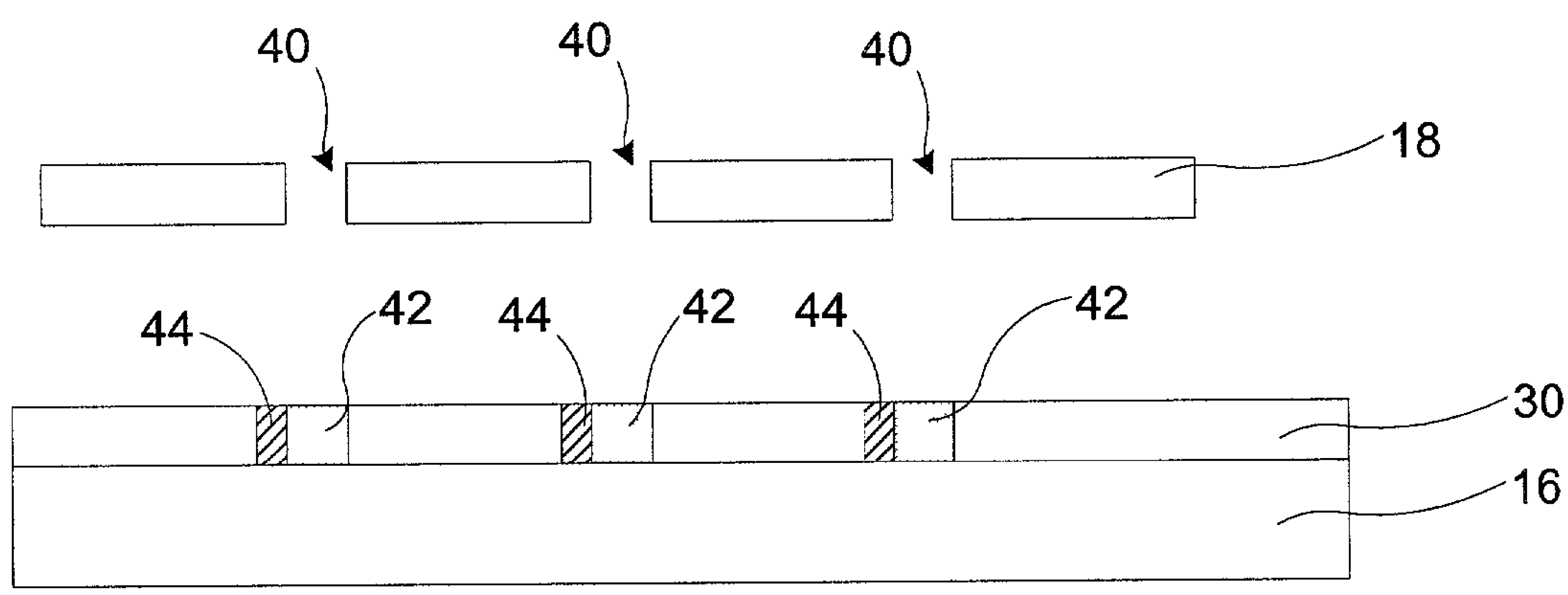
(57) **ABSTRACT**

A method is provided to produce thin film transistors (TFTs) on polycrystalline films having a single predominant crystal orientation. A layer of amorphous silicon is deposited over a substrate to a thickness suitable for producing a desired crystal orientation. Lateral-seeded excimer laser annealing (LS-ELA) is used to crystallize the amorphous silicon to form a film with a preferred crystal orientation. A gate is formed overlying the polycrystalline film. The polycrystalline film is doped to produce source and drain regions.



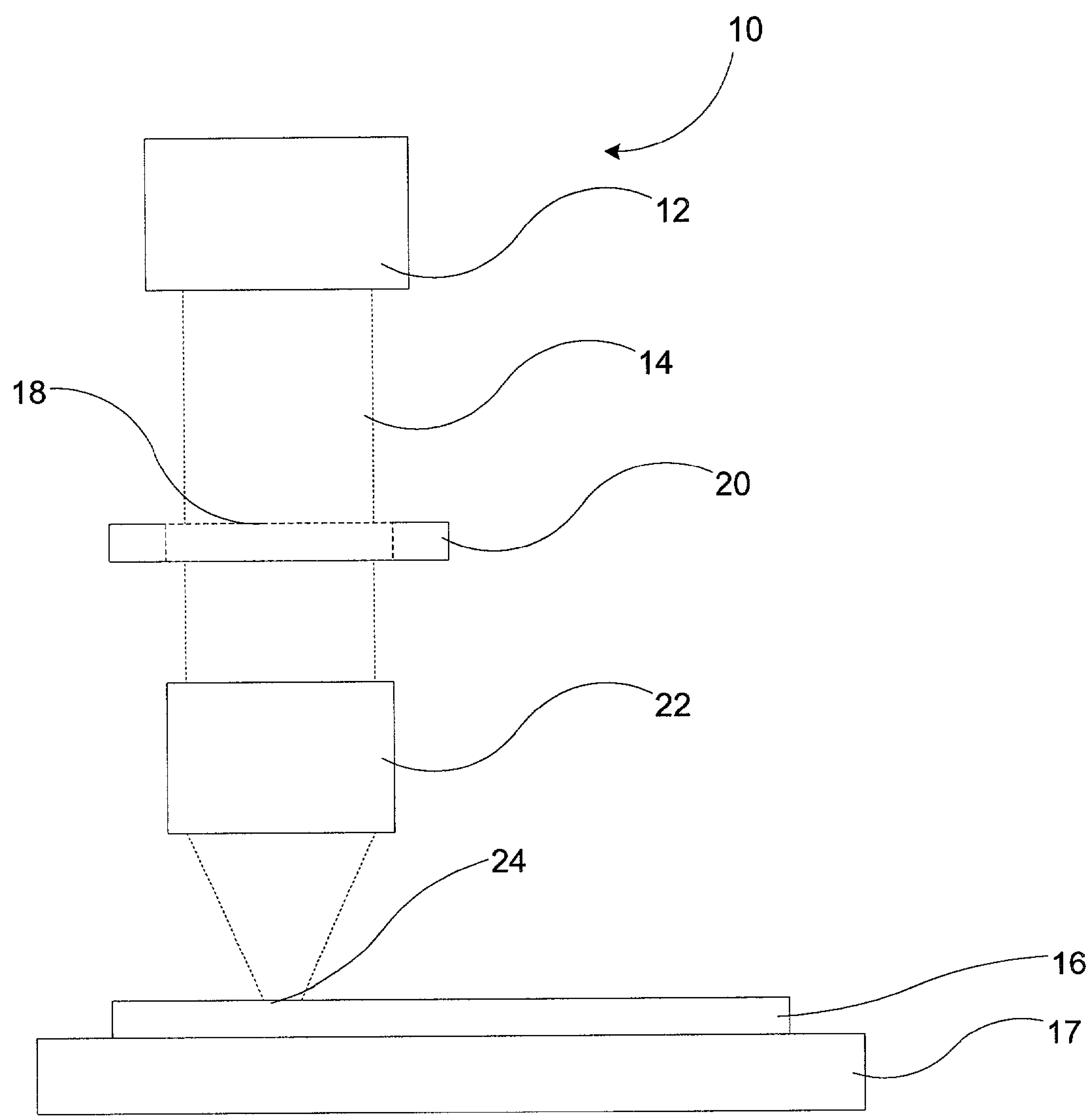


FIG. 1

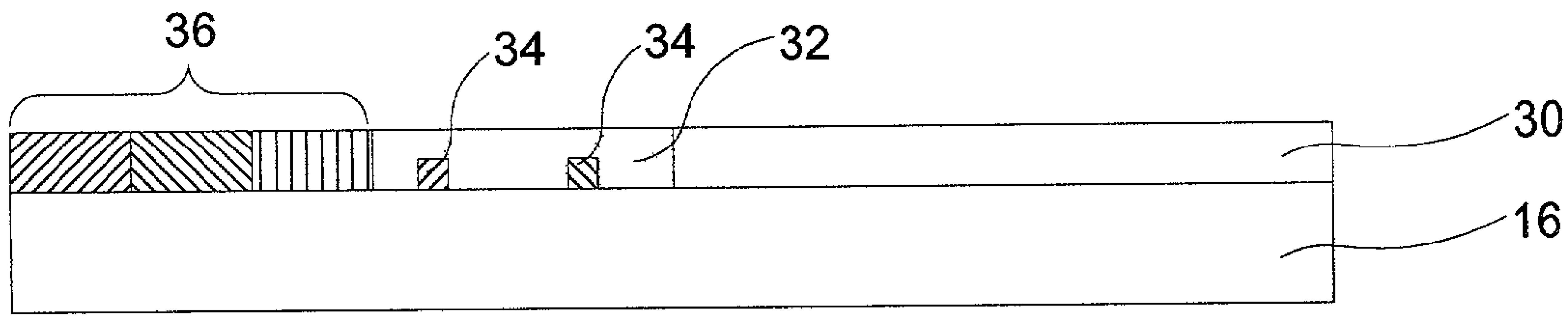


FIG. 2 (prior art)

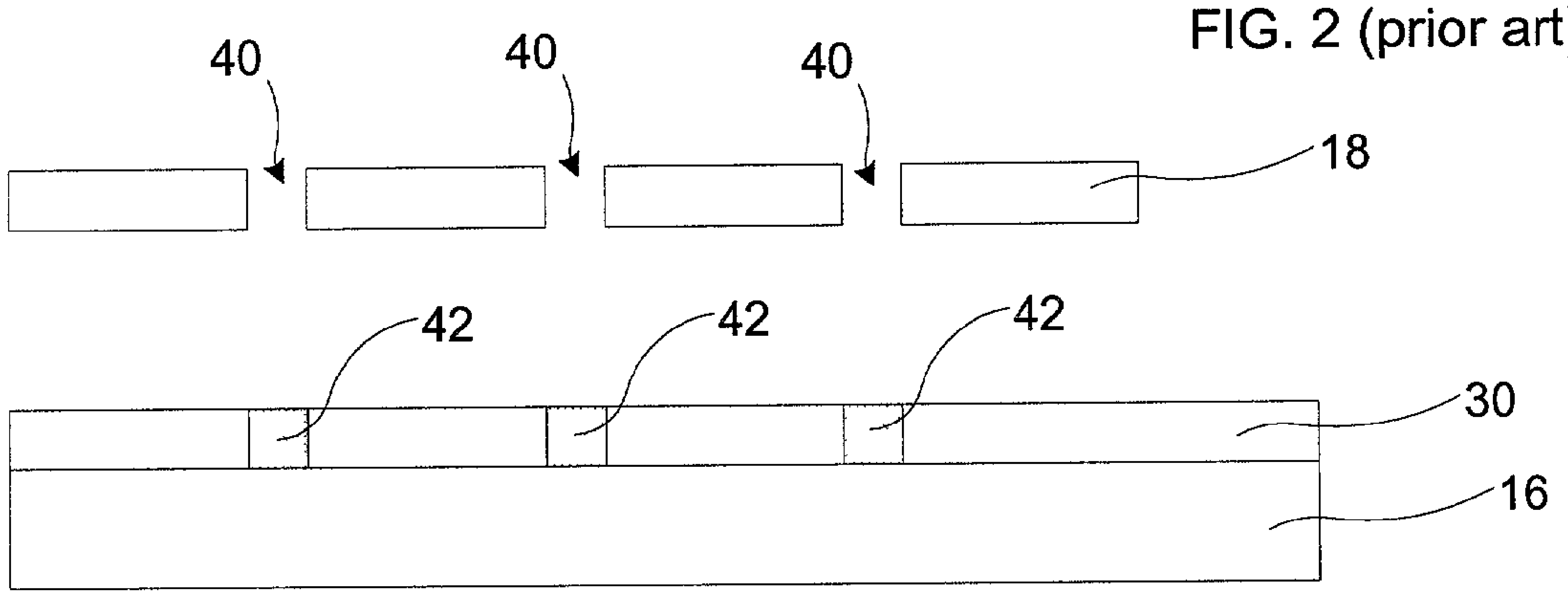


FIG. 3

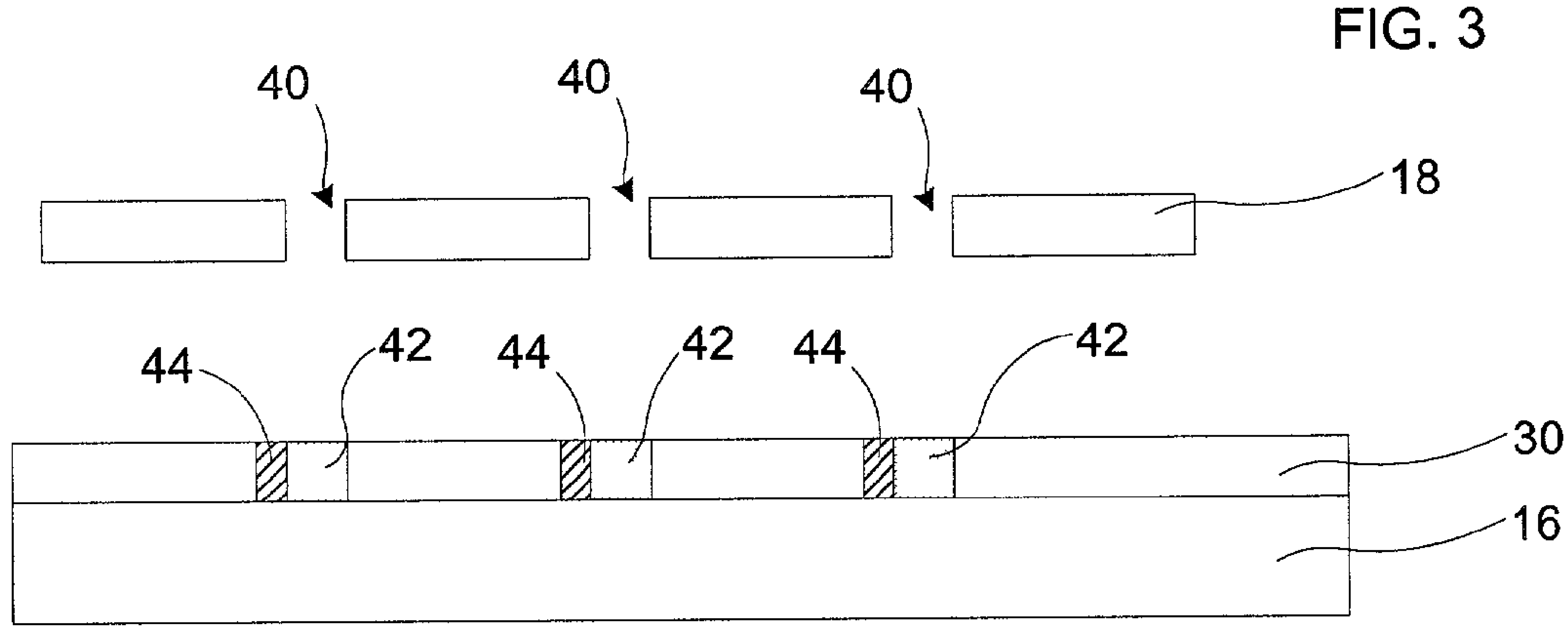


FIG. 4

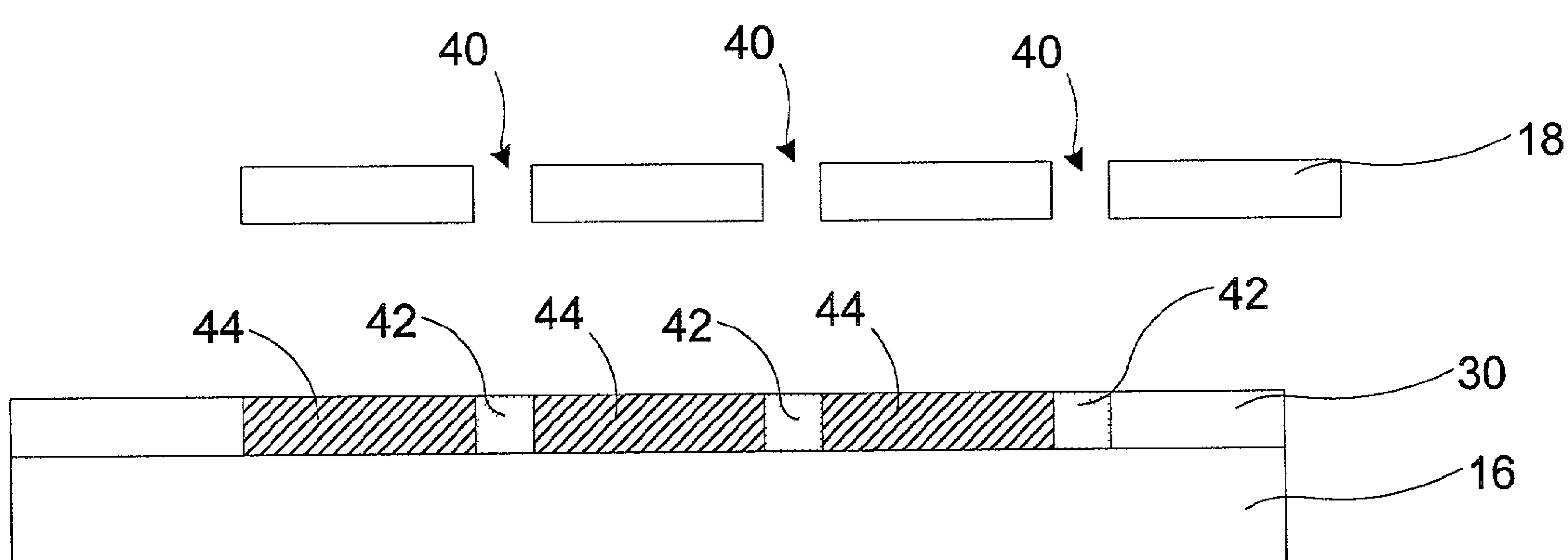


FIG. 5

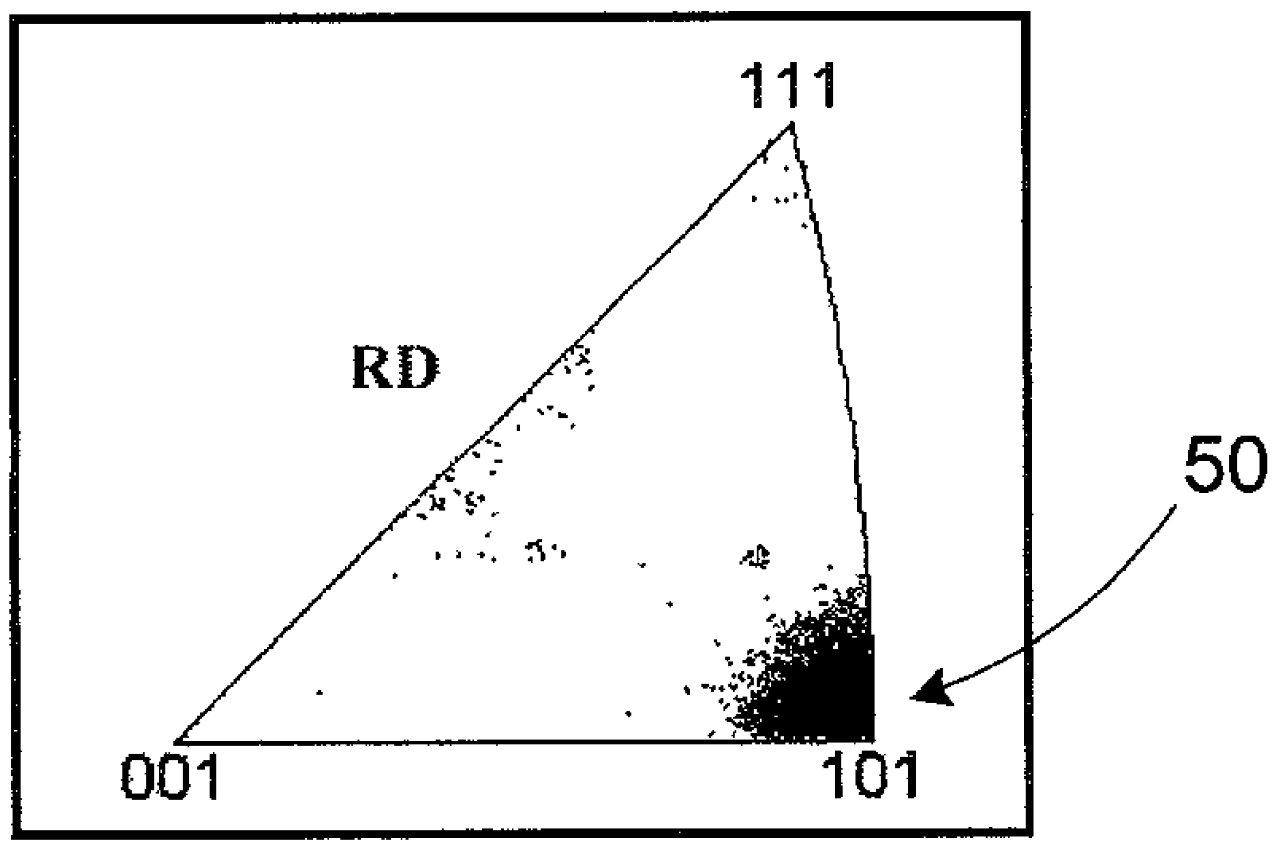


FIG. 6

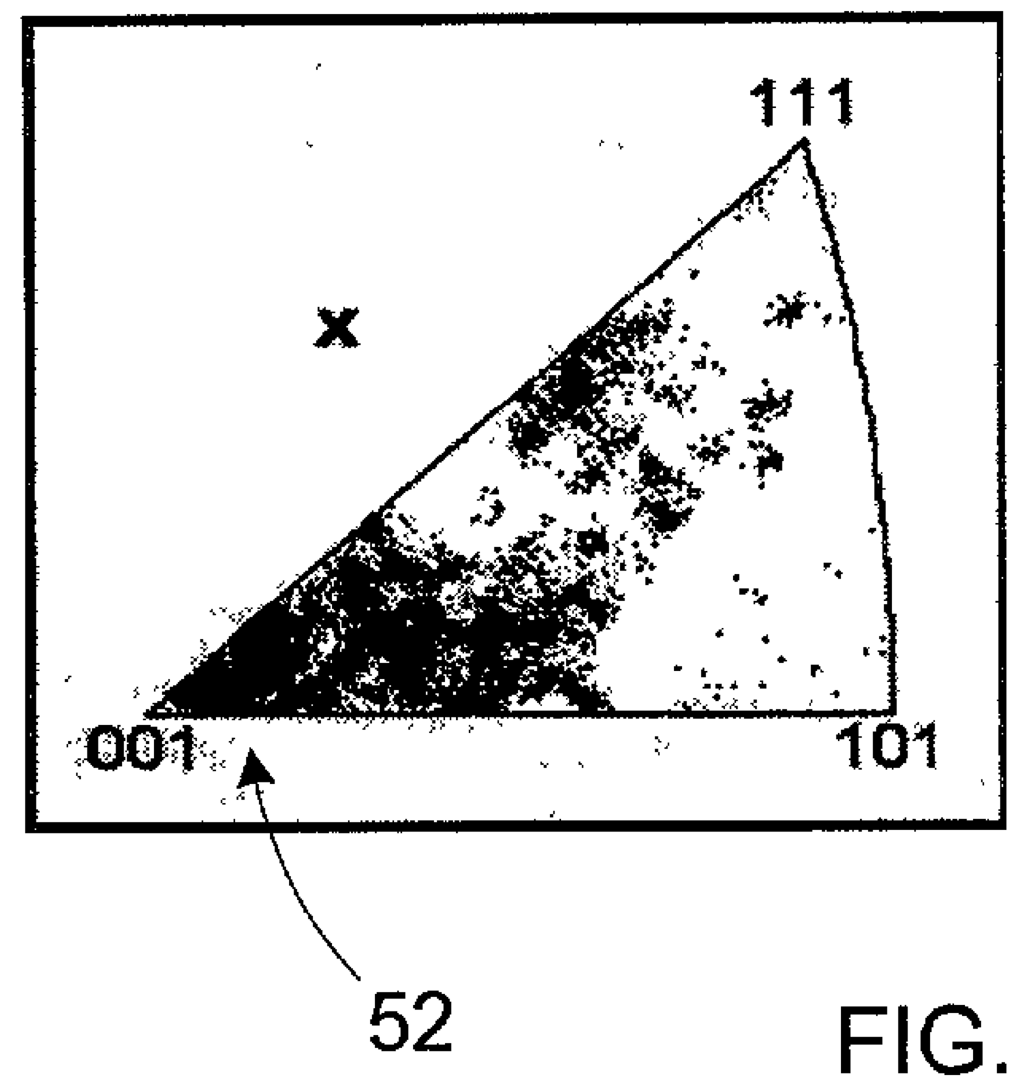


FIG. 7

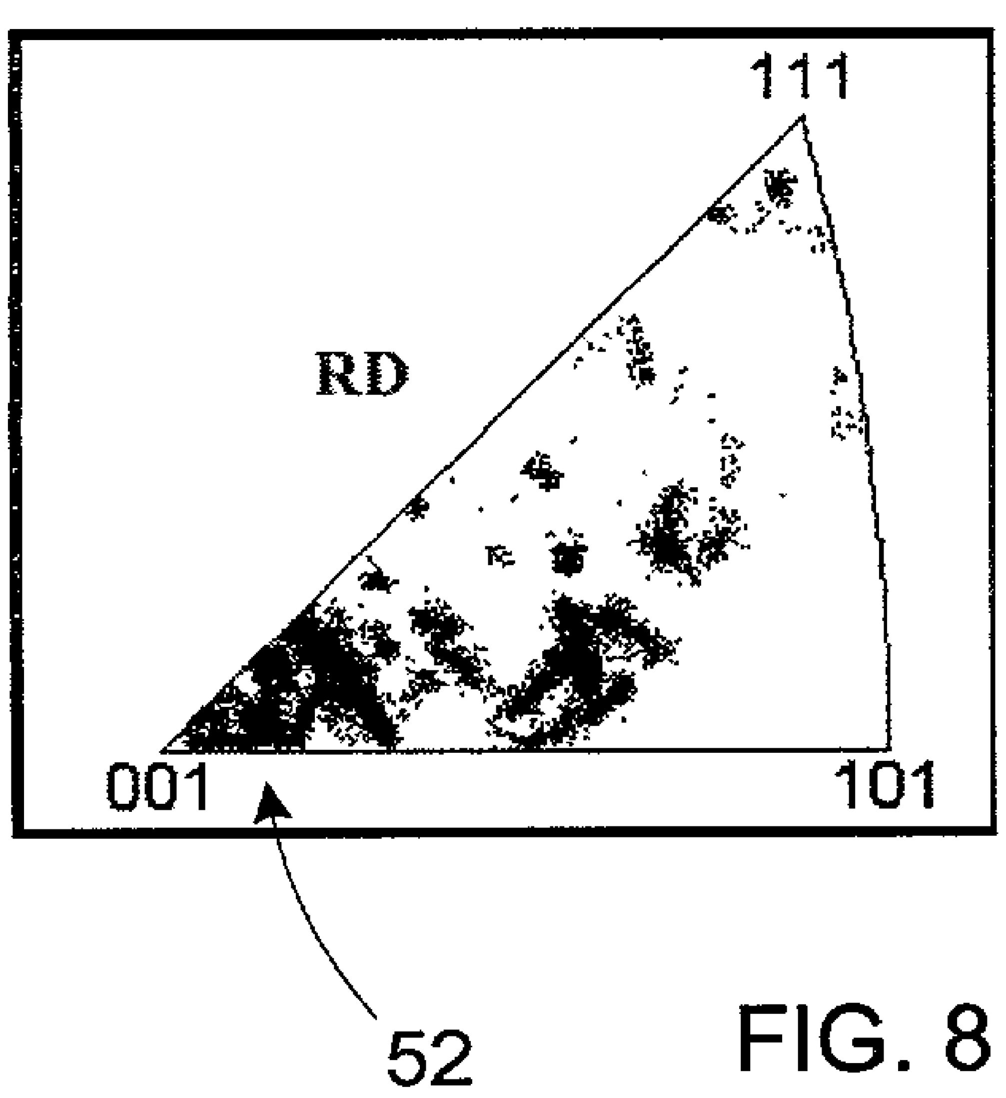


FIG. 8

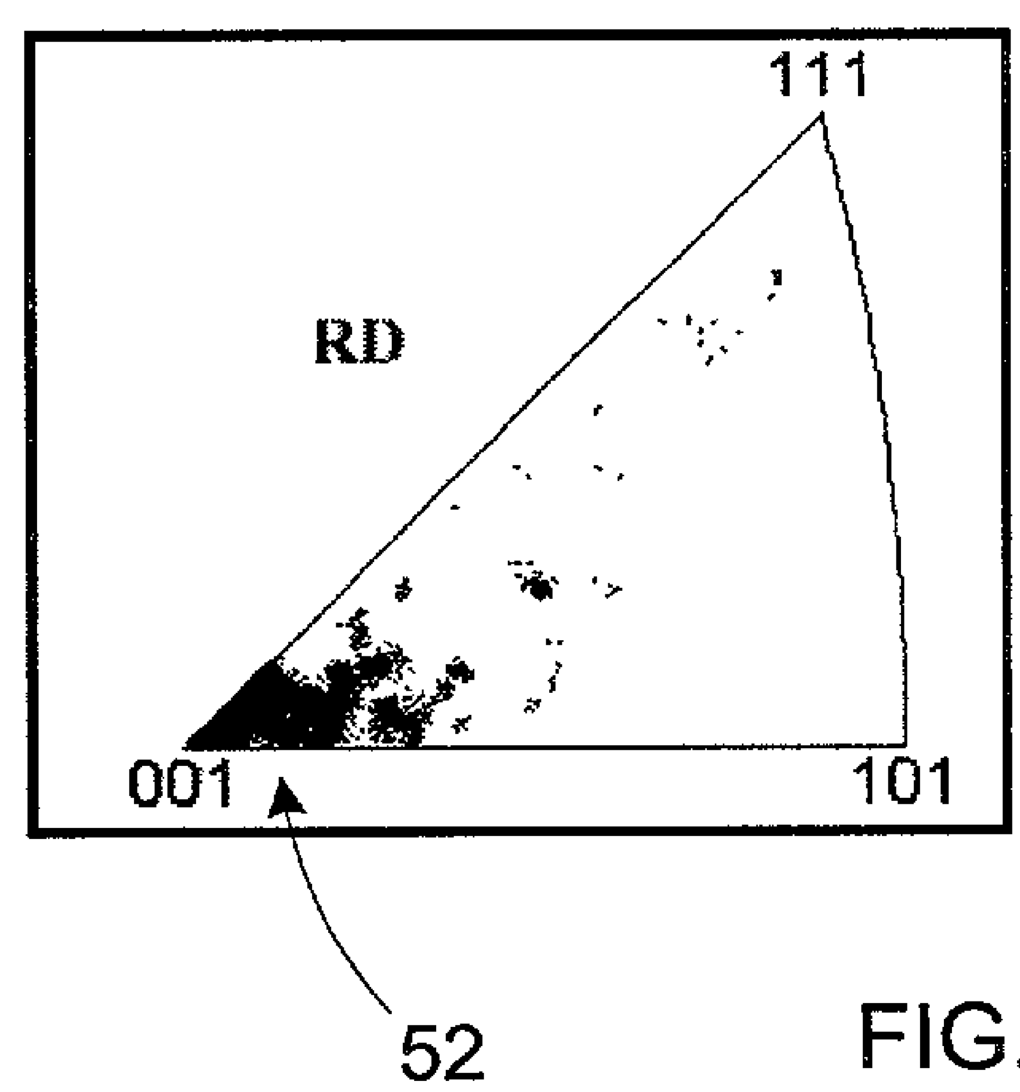


FIG. 9

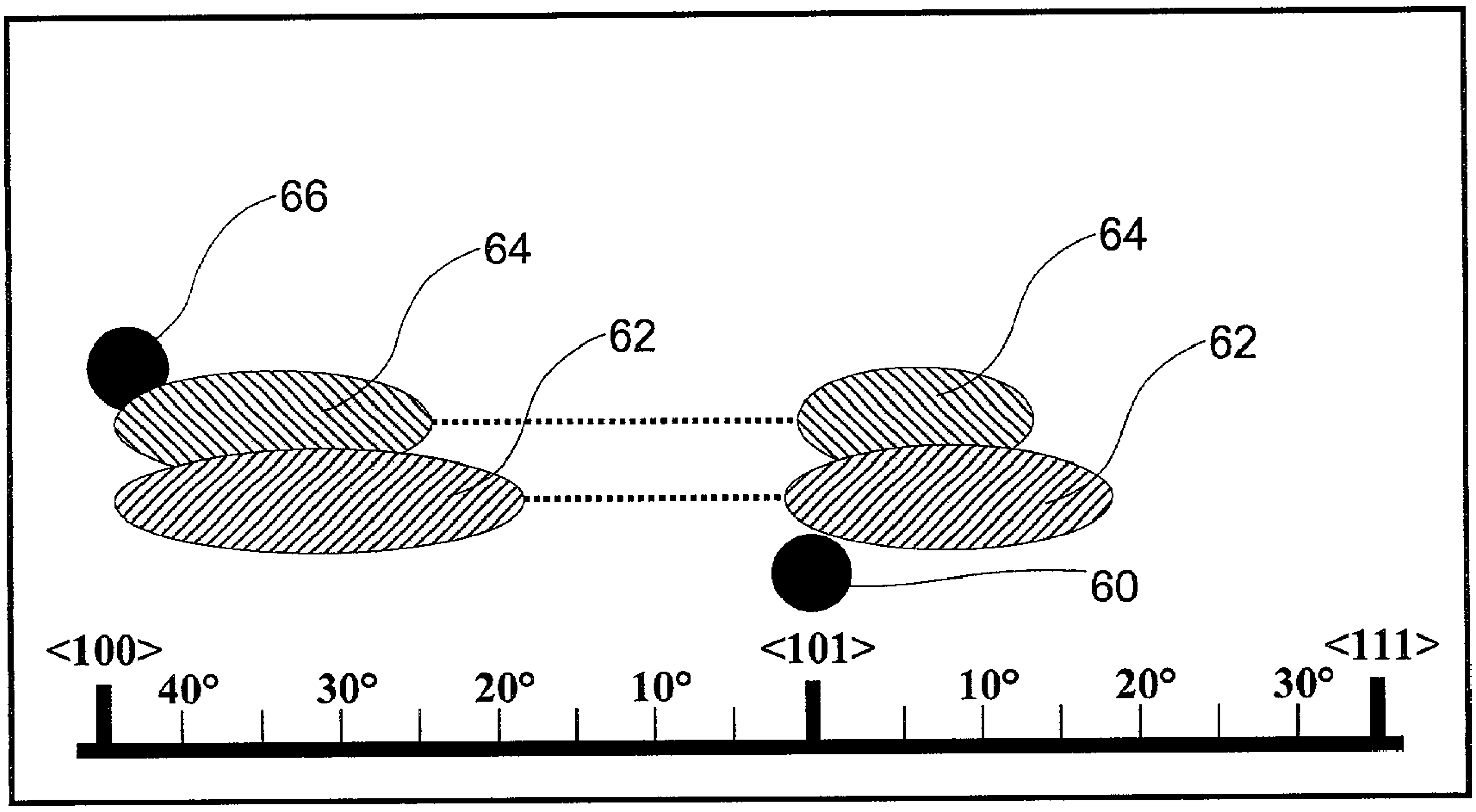


FIG. 10

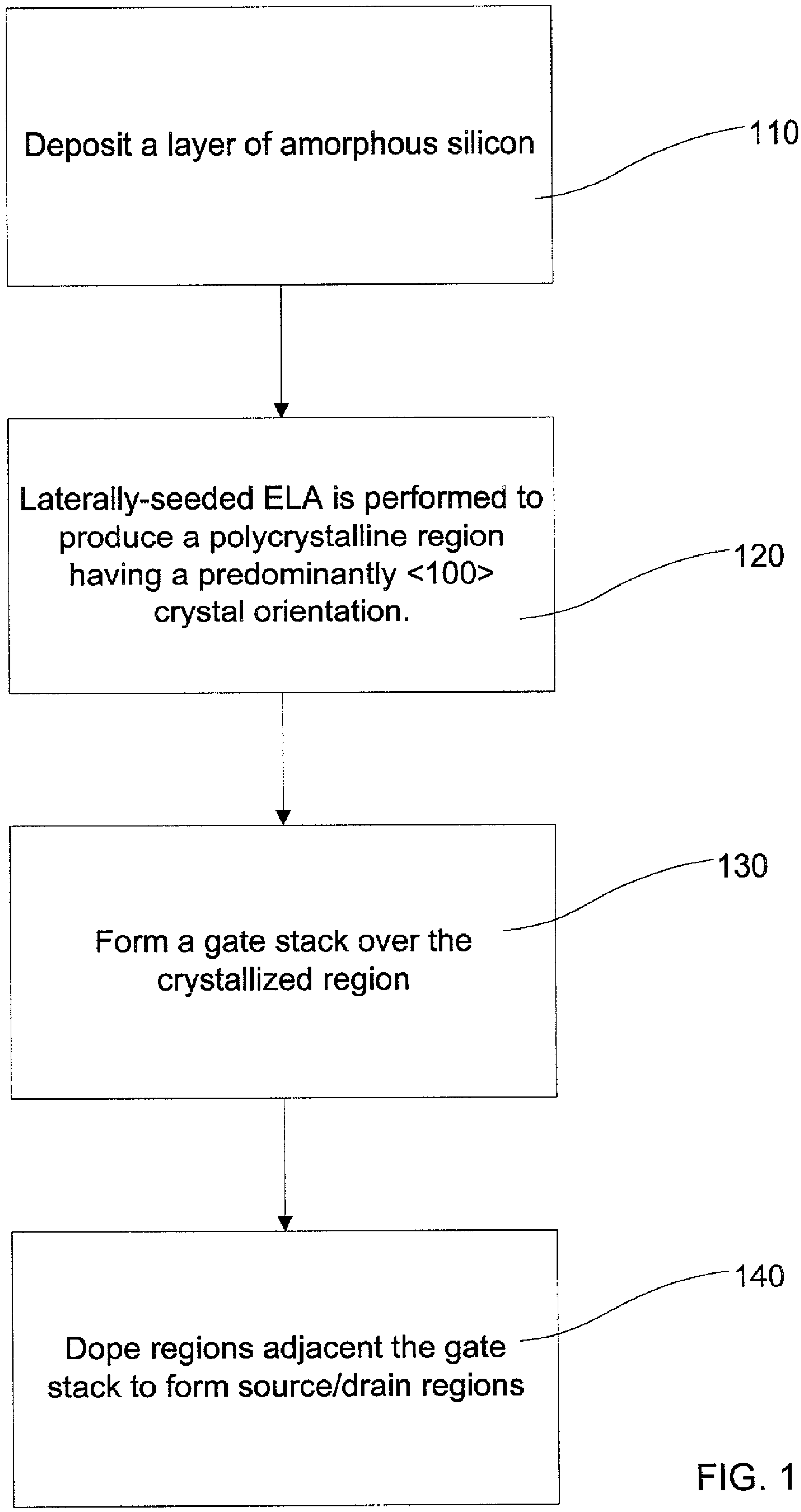

Deposit a layer of amorphous silicon
110
Laterally-seeded ELA is performed to produce a polycrystalline region having a predominantly <100> crystal orientation.
120
Form a gate stack over the crystallized region
130
Dope regions adjacent the gate stack to form source/drain regions
140

FIG. 11

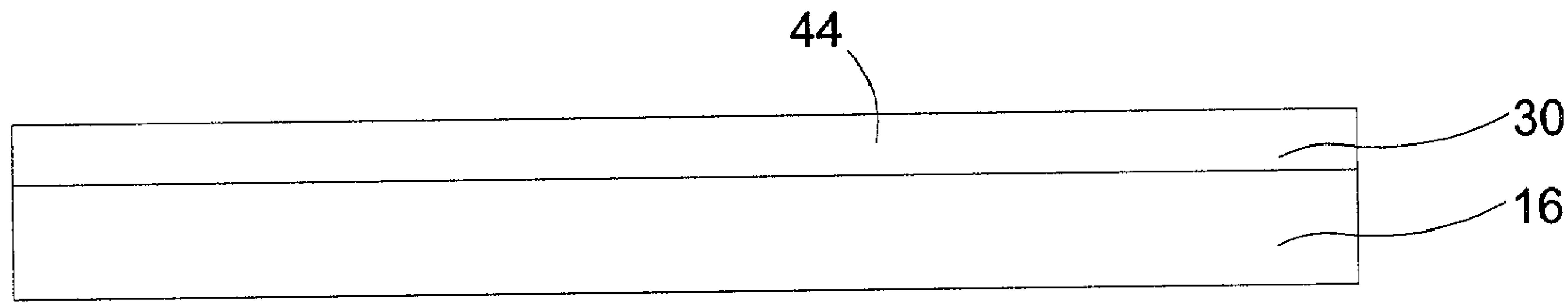


FIG. 12

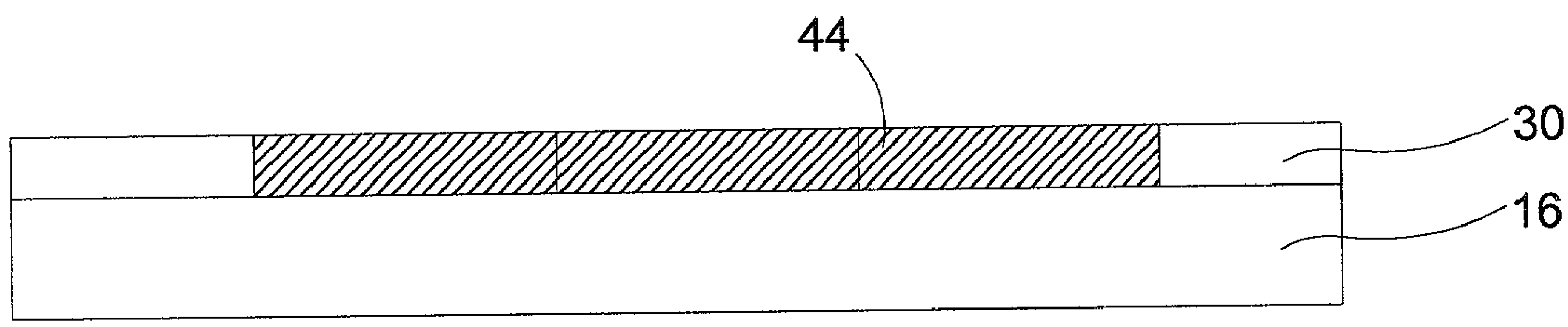


FIG. 13

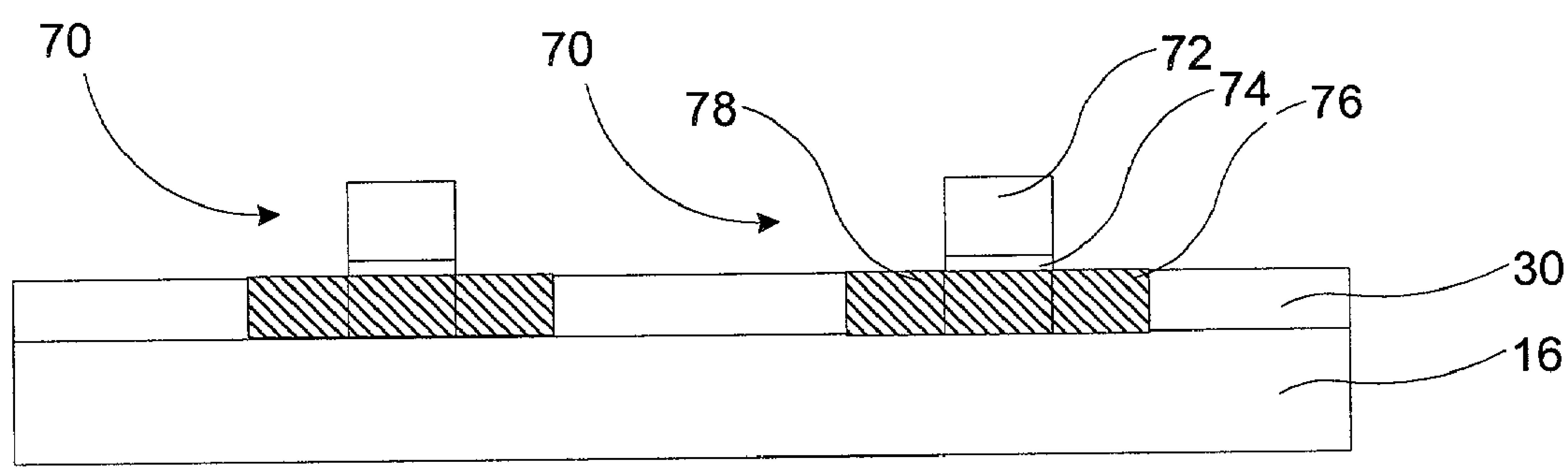


FIG. 14

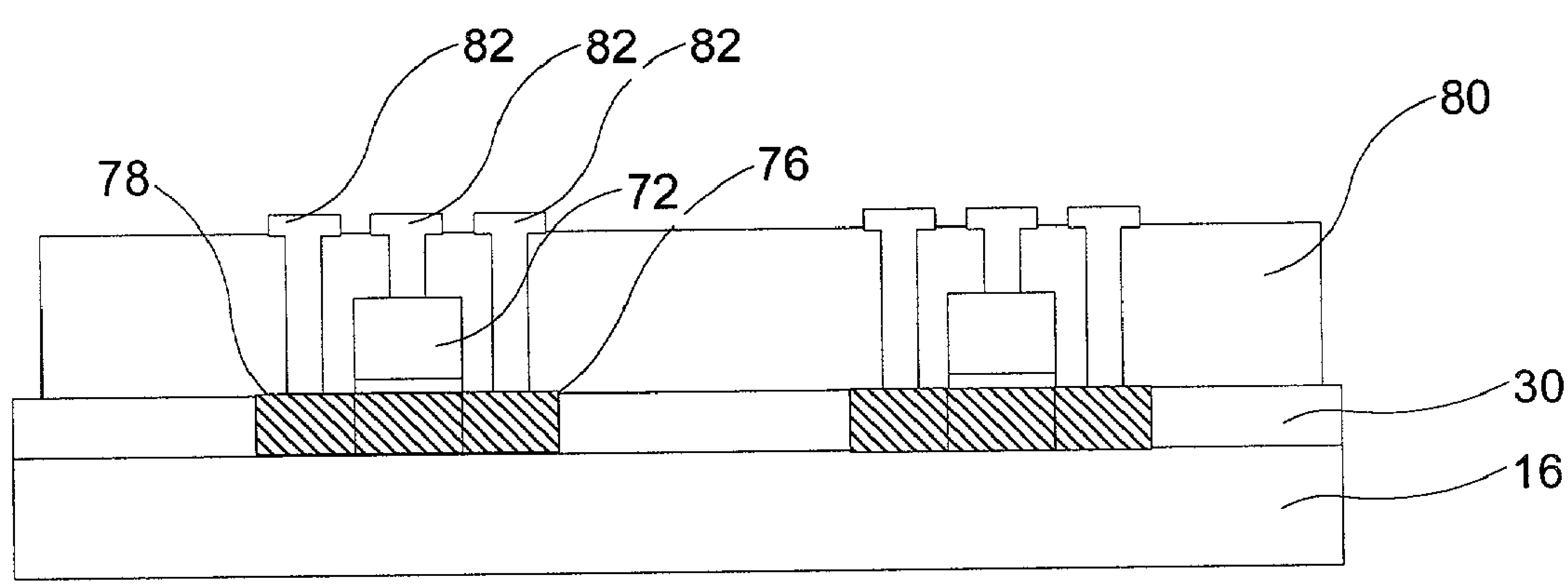


FIG. 15

METHOD OF FORMING PREDOMINANTLY POLYCRYSTALLINE SILICON THIN FILM TRANSISTORS

BACKGROUND OF THE INVENTION

[0001] This invention relates generally to semiconductor technology and more particularly to the method of forming thin film transistors (TFTs) on polycrystalline silicon regions within an amorphous silicon film.

[0002] Polycrystalline silicon is formed by crystallizing amorphous silicon films. One method of crystallizing amorphous silicon films is excimer laser annealing (ELA). Conventional ELA processes form polycrystalline films having a random polycrystalline structure. Random, as used here, means that no single crystal orientation is dominant and that polycrystalline structures consist of a mixture of crystallographic orientations in silicon. These crystallographic orientations in silicon are commonly denoted as **<111>**, **<110>**, and **<100>**, along with their respective corollaries, as is well known in the art. Control of crystallographic orientation is generally desirable because the electrical characteristics of a polycrystalline silicon film depend upon the crystallographic orientation of the film. In addition, the uniformity of the electrical characteristics will improve if the majority of the film has a controllable texture.

[0003] ELA, as well as many other annealing methods, has not provided a means to control these microstructural characteristics and achieve a predictable and repeatable preferential crystal orientation and film texture within an annealed film. It would be desirable to have a method of producing TFTs using a polycrystalline silicon film with a more uniform crystallographic orientation. It would also be desirable to be able to produce TFTs using predominantly **<100>** polycrystalline silicon.

SUMMARY OF THE INVENTION

[0004] Accordingly, a method of forming thin film transistor (TFT) structures on a substrate, which has a polycrystalline silicon film with a desired predominant crystal orientation, is provided. The method of forming the TFTs comprises the steps of: providing a substrate, depositing an amorphous silicon film on the substrate, annealing the substrate to produce a polycrystalline film with the desired predominant crystal orientation, preferably a **<100>** crystal orientation, forming a gate structure over the polycrystalline film; and doping the polycrystalline film to produce source regions and drain regions.

[0005] The substrate can be any material that is compatible with the deposition of amorphous silicon and excimer laser annealing. For display applications, the substrate is preferably a transparent substrate such as quartz, glass or plastic.

[0006] To achieve a good quality film that is predominantly **<100>** crystal orientation, the step of depositing the amorphous film should deposit to a thickness of at least approximately 100 nm.

[0007] The step of annealing preferably uses a laterally seeded excimer laser annealing process.

[0008] The method of the present invention, produces a thin film transistor structure comprising a polycrystalline film, which has a predominantly **<100>** crystal orientation, overlying a substrate. The final film is at least 100 nm thick. A gate structure overlies the polycrystalline silicon film and source/drain regions are formed by doping the polycrystalline silicon film.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] **FIG. 1** is a schematic cross-sectional view showing an excimer laser anneal (ELA) apparatus used in connection with the present method.

[0010] **FIG. 2** (prior art) is a cross-sectional view showing polycrystalline film crystallized using an interface-seeded ELA (IS-ELA) process

[0011] **FIG. 3** illustrates a step in the process of lateral-seeded ELA (LS-ELA).

[0012] **FIG. 4** illustrates a step in the process of lateral-seeded ELA (LS-ELA).

[0013] **FIG. 5** illustrates a step in the process of lateral-seeded ELA (LS-ELA).

[0014] **FIG. 6** is a scatter plot of crystal orientations for a 35 nm thick film.

[0015] **FIG. 7** is a scatter plot of crystal orientations for a 45 nm thick film.

[0016] **FIG. 8** is a scatter plot of crystal orientations for a 75 nm thick film.

[0017] **FIG. 9** is a scatter plot of crystal orientations for a 100 nm thick film.

[0018] **FIG. 10** is a diagram illustrating variation in crystal orientation for various film thicknesses.

[0019] **FIG. 11** is a flowchart of a process of performing the method of the present invention.

[0020] **FIG. 12** is a cross-sectional view of a substrate during processing.

[0021] **FIG. 13** is a cross-sectional view of a substrate during processing.

[0022] **FIG. 14** is a cross-sectional view of transistor structures formed on the substrate during processing.

[0023] **FIG. 15** is a cross-sectional view of transistor structures formed on the substrate during processing.

DETAILED DESCRIPTION OF THE INVENTION

[0024] Referring to **FIG. 1 a** lateral-seeded excimer laser annealing (LS-ELA) apparatus **10** is shown. LS-ELA apparatus **10** has a laser source **12**. Laser source **12** includes a laser (not shown) along with optics, including mirrors and lens, which shape a laser beam **14** (shown by dotted lines) and direct it toward a substrate **16**, which is supported by a stage **17**. The laser beam **14** passes through a mask **18** supported by a mask holder **20**. The laser beam **14** preferably has an output energy in the range of 0.8 to 1 Joule when the mask **18** is 50 mm×50 mm. Currently available commercial lasers such as Lambda Steel 1000 can achieve this output. As the power of available lasers increases, the energy of the laser beam **14** will be able to be higher, and the mask size will be able to increase as well. After passing through the mask **18**, the laser beam **14** passes through demagnification optics **22** (shown schematically). The demagnification optics **22** reduce the size of the laser beam reducing the size of any image produced after passing through the mask **18**, and simultaneously increasing the intensity of the optical energy striking the substrate **16** at a desired location **24**. The demagnification is typically on the order of between 3x and 7x reduction, preferably a 5x reduction, in image size. For a 5x reduction the image of the mask **18** striking the surface at the location **24** has 25 times less total area than the mask, correspondingly increasing the energy density of the laser beam **14** at the location **24**.

[**0025**] The stage **17** is preferably a precision x-y stage that can accurately position the substrate **16** under the beam **14**. The stage **17** is preferably capable of motion along the z-axis, enabling it to move up and down to assist in focusing or defocusing the image of the mask **18** produced by the laser beam **14** at the location **24**. The mask holder **20** is also capable of x-y movement.

[**0026**] **FIG. 2** illustrates aspects of a prior art ELA process. This process is sometimes referred to as Interface-Seeded ELA (IS-ELA). An amorphous silicon film **30** has been deposited over the substrate **16**. A laser pulse is directed at the amorphous silicon film **30**, which melts and crystallizes a region **32**. The laser pulse melts a region on the order of 0.5 mm. Small microcrystalline seeds **34** remain, or form, at the interface. As the surrounding amorphous silicon crystallizes these seeds affect the crystal orientation. Since the seeds **34** have a variety of crystal orientations, the resulting films will accordingly have a wide mix of crystal orientations. This is illustrated by previously crystallized region **36**. In actuality, since a large number of seeds would be present at the interface, a large number of crystal orientations would form.

[**0027**] **FIGS. 3 through 5** illustrate the steps of Lateral-Seeded ELA (LS-ELA), which is also referred to as Lateral-Growth ELA (LG-ELA) or Lateral Crystallization ELA (LC-ELA). Starting with **FIG. 3**, the amorphous silicon film **30** has been deposited over the substrate **16**. A laser beam pulse has been passed through openings **40** in the mask **18** to form beamlets, which irradiate regions **42** of the amorphous silicon film **30**. Each beamlet is on the order of 5 microns wide. This is approximately 100 times narrower than the 0.5 mm used in the prior art IS-ELA process. The small regions **42** are melted and crystallized by the beamlets produced by the laser pulse passing through the mask.

[**0028**] After each pulse the mask **18** is advanced by an amount not greater than half the lateral crystal growth distance. A subsequent pulse is then directed at the new area. By advancing the image of the openings **40** a small distance, the crystals produced by preceding steps act as seed crystals for subsequent crystallization of adjacent material. Referring now to **FIG. 4**, the irradiated regions **42** have moved slightly. The previously crystallized regions **44** act as the seed crystal for the crystallization of the irradiated regions **42**. By repeating the process of advancing the mask laterally and firing short pulses the crystal is effectively pulled in the direction of the advancing laser pulses.

[**0029**] **FIG. 5** shows the amorphous silicon film **30** after several additional pulses following **FIG. 4**. The crystals have continued to grow in the direction of the masks' movement to form a polycrystalline region. The mask will preferably advance until each opening **40** reaches the edge of a polycrystalline region formed by the opening immediately preceding it. To crystallize larger regions, the stage **17**, which was described in reference to **FIG. 1**, can be moved, and the mask **18** repositioned, to continue crystallizing the amorphous silicon film **30** until a region of the desired size has been crystallized.

[**0030**] This LS-ELA process produces crystallized regions that are more uniform, due to the propagation of a first crystallized region by subsequent laser pulses, as opposed to crystallized regions formed using multiple seed crystals at the interface. **FIGS. 6 through 9** are plots that illustrate the affect of amorphous silicon film thickness on the resulting predominant crystal orientation.

[**0031**] **FIG. 6** is a plot of the distribution of crystal orientation for a 30 nm thick deposited amorphous silicon film after LS-ELA processing. **FIG. 6** shows that a majority of the crystals are in a **101** region **50**. The **101** region **50** corresponds to a **<110>** crystal orientation.

[**0032**] **FIG. 7** is a plot of the distribution of crystal orientation for a 45 nm thick deposited amorphous silicon film after LS-ELA processing. **FIG. 7** shows that the crystal orientations are spread throughout the orientation plot. This is a less ideal condition for the resulting film. It should be noted that the predominant crystal orientation has shifted away from the **<110>** orientation toward the **<100>** orientation region **52**, which corresponds to 001 on the plot.

[**0033**] **FIG. 8** is a plot of the distribution of crystal orientation for a 75 nm thick deposited amorphous silicon film after LS-ELA processing. **FIG. 8** shows that the crystal orientation has moved closer to the **<100>** orientation. However, the crystal orientation is still spread over a relatively wide range of crystal orientations.

[**0034**] **FIG. 9** is a plot of the distribution of crystal orientation for a 100 nm thick deposited amorphous silicon film after LS-ELA processing. **FIG. 9** shows that the crystal orientation is now predominantly **<100>** as shown by the **<100>** region **52**.

[**0035**] **FIG. 10** is a diagram illustrating variation in crystal orientation for various film thicknesses. A first thickness **60**, which corresponds to an approximately 35 nm thick film, has a **<110>** orientation to within less than 10 degrees. A second film thickness **62**, which corresponds to an approximately 45 nm thick film, has a mix of **<100>** orientation to within 25 degrees and **<101>** orientation to within approximately 20 degrees. A third film thickness **64**, which corresponds to an approximately 75 nm thick film, has a mix of **<100>** orientation to within approximately 20 degrees and **<101>** orientation to within approximately 15 degrees. A forth film thickness **66**, which corresponds to an approximately 100 nm thick film, has a **<100>** orientation to within approximately 10 degrees. As used herein, the term predominant crystal orientation, or any similar phrase, refers to a material that is within less than 15 degrees of a desired crystal orientation. Looking at **FIG. 10**, it is apparent that it is possible to produce films with predominantly **<110>** orientation, or **<100>** orientation. **<100>** orientation is generally preferred for semiconductor processes because of its electrical properties. Unfortunately, to produce predominantly **<100>** orientation requires the formation of thicker films than those that generally are considered desirable for the formation of thin film transistors. Thicker films tend to have greater leakage currents than thinner films. In the method of this invention, the compromise is made between leakage current and the desirable electrical properties associated with having predominantly **<100>** polycrystalline films. While it may be possible to polish the films to produce thinner films, this may not be practical for all applications.

[**0036**] Referring now to **FIG. 11, a** flow chart of the steps of the method of the present invention is shown. Step **110** deposits a layer of amorphous silicon over the substrate. The layer of amorphous silicon should be thick enough to produce predominantly **<100>** polycrystalline silicon following subsequent processing according to the method of the present invention. The necessary thickness to produce a predominantly **<100>** polycrystalline material can be determined without undue experimentation. Preferably, the layer of amorphous silicon will be at least approximately 100 nm thick.

[**0037**] Step **120** performs lateral crystallization using LS-ELA to produce a polycrystalline region having a predominantly **<100>** crystal orientation. A laser beam is used to project an image of the mask onto the substrate. The laser beam energy is sufficient to cause amorphous silicon to crystallize. A sequence of laser pulses can be used to crystallize a region, as described above. The resulting polycrystalline film is predominantly **<100>** crystal orientation, meaning within 15 degrees of **<100>** crystal orientation. Preferably, the crystal orientation is within 10 degrees of **<100>** crystal orientation.

[**0038**] Step **130** forms a gate stack overlying the polycrystalline film. The gate stack includes a dielectric layer, preferably silicon dioxide, and a gate, preferably composed of polysilicon.

[**0039**] Step **140** dopes regions adjacent the gate stack to form n-type and p-type regions on either side of the gate stack. These doped regions are referred to as source and drain regions. The doping is accomplished by appropriately masking the area, implanting the desired dopants, and annealing. In TFT structures, the dopants preferably extend through the thickness of the polycrystalline film.

[**0040**] **FIGS. 12 through 15** show the film at various stages of processing. **FIG. 12** shows the substrate **16** with an overlying amorphous silicon film **30**. For display applications, the substrate is preferably transparent. Available transparent substrate materials include quartz, glass, and plastic. Although it is not shown, a barrier coat may be used between the substrate and the amorphous silicon as is well known to one of ordinary skill in the art. The amorphous silicon film is preferably thick enough to form a predominantly **<100>** crystal orientation following LS-ELA processing. Amorphous silicon films on the order of at least approximately 100 nm will produce predominantly **<100>** crystal orientation. Slightly thinner films may also produce the desired result, without undue experimentation.

[**0041**] **FIG. 13** shows a polycrystalline region **44** following the LS-ELA process, which was discussed above. The polycrystalline region **44** is predominantly **<100>**. By predominantly **<100>**, it is meant that the orientation is within 15 degrees of **<100>** as described above with reference to **FIG. 10**.

[**0042**] **FIG. 14** shows TFT structures **70** formed using the polycrystalline film. A gate **72** has been formed overlying the polycrystalline film, with a dielectric layer **74** interposed between the gate and the polycrystalline film. Source region **76** and drain region **78** have been formed within the polycrystalline film by doping the polycrystalline film with n-type and p-type dopants, respectively.

[**0043**] The gate is preferably a polysilicon gate. The interposed dielectric layer is silicon dioxide, or other suitable dielectric material. The source and drain regions are formed by implanting, or other suitable doping method.

[**0044**] The polycrystalline film is removed from the substrate over areas that are not used to produce TFTs or other device elements. Elimination of the polycrystalline film from these open spaces provides isolation of device components.

[**0045**] Referring now to **FIG. 15**, an isolation material **80** is provided to isolate the device components as well as the metal connections **82**.

[**0046**] Although a simple TFT structure has been shown, many different transistor structures are known to those of ordinary skill in the art and could be used in connection with the present method. Lightly-doped drain and source regions could be used. A variety of gate structures could be used as well, including substitute gates, and new high-k dielectric materials. The invention is not limited to the specific embodiments described above, but is defined by the claims.

What is claimed is:

1. A method of forming thin film transistor (TFT) structures on a substrate comprising the steps of;

a) providing the substrate;

b) depositing an amorphous silicon film at least 100 nm thick over the substrate;

c) annealing the amorphous silicon film using a lateral crystallization process to produce a polycrystalline film having a predominantly **<100>** crystallographic orientation;

d) forming a gate structures over the polycrystalline film; and

e) doping the polycrystalline film having a predominantly **<100>** crystallographic orientation to produce source regions and drain regions.

2. The method of claim 1; wherein the substrate is transparent.

3. The method of claim 2, wherein the substrate is quartz, glass or plastic.

4. The method of claim 1, wherein the amorphous silicon film is in the range of between approximately 100 and 250 nm thick.

5. The method of claim 1, wherein the polycrystalline film has a crystallographic orientation within 15 degrees of **<100>**.

6. The method of claim 1, wherein the polycrystalline film has a crystallographic orientation within 10 degrees of **<100>**.

7. The method of claim 1, wherein the lateral crystallization process comprises a sequence of laser pulses projected through a mask having a narrow slit to project a beamlet onto the surface of the amorphous silicon film to crystallize the amorphous silicon film as the beamlet is advanced over the surface of the amorphous silicon film between successive laser pulses.

8. A thin film transistor (TFT) structure comprising:

a) a substrate;

b) a polycrystalline silicon film having a predominantly <**100**> crystallographic orientation overlying the substrate;

c) a gate structure formed over the polycrystalline silicon film; and

d) source and drain regions formed by doping the polycrystalline silicon film.

9. The thin film transistor structure of claim 8, wherein the substrate is transparent.

10. The thin film transistor structure of claim 9, wherein the substrate is quartz, glass, or plastic.

11. The thin film transistor structure of claim 8, wherein the polycrystalline silicon film is at least 100 nm thick.

12. The thin film transistor structure of claim 8, wherein the polycrystalline silicon film is in the range of between approximately 100 and 250 nm thick.

13. The thin film transistor structure of claim 8, wherein the source and drain regions extend only partially through the polycrystalline silicon film.

* * * * *