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(54) **METHOD FOR LIFT-OFF OF EPITAXIALLY GROWN SEMICONDUCTORS BY ELECTROCHEMICAL ANODIC ETCHING**

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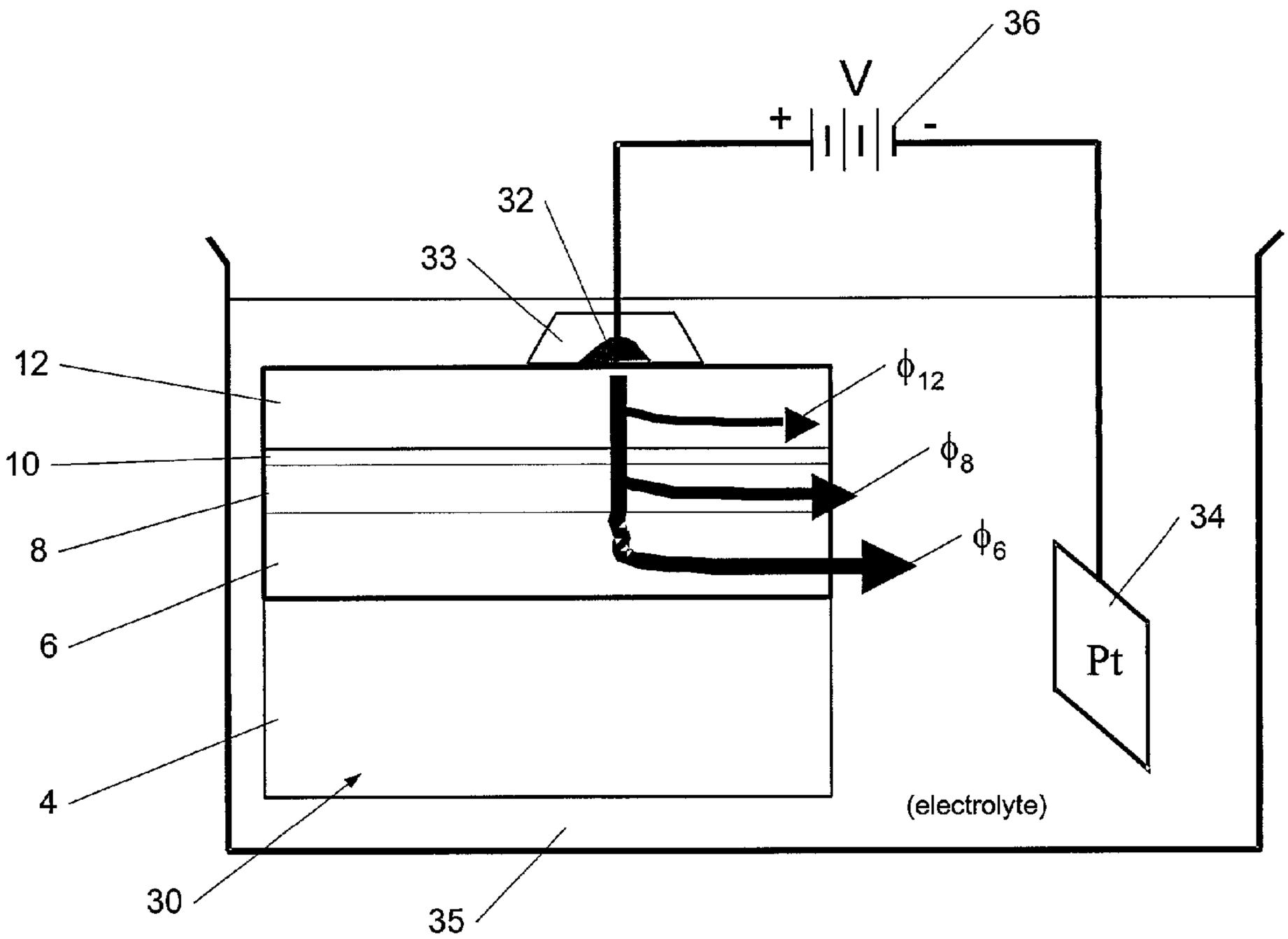
(57) **ABSTRACT**

A method is disclosed for separating a semiconductor epitaxial structure from an insulating growth substrate. The method utilizes electrochemical anodic reactions to remove a thin etch layer disposed near the growth interface. The thin etch layer can be an intentional layer made of a material different from the epitaxial structure and/or can include a material with a high defect density. The method can be applied in the fabrication of optoelectronic and electronic devices from III-V materials, in particular gallium-nitride based materials.



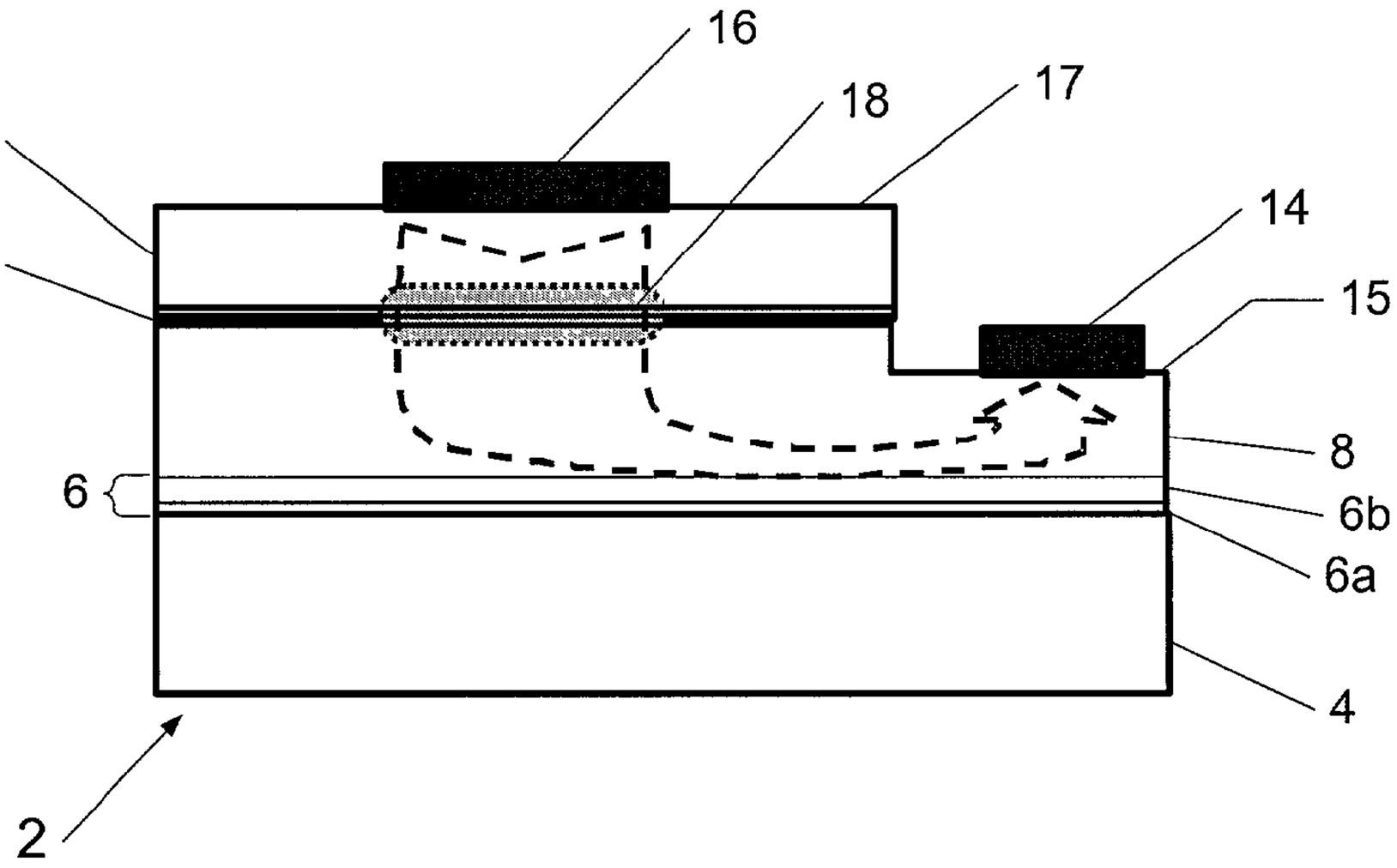


Fig. 1

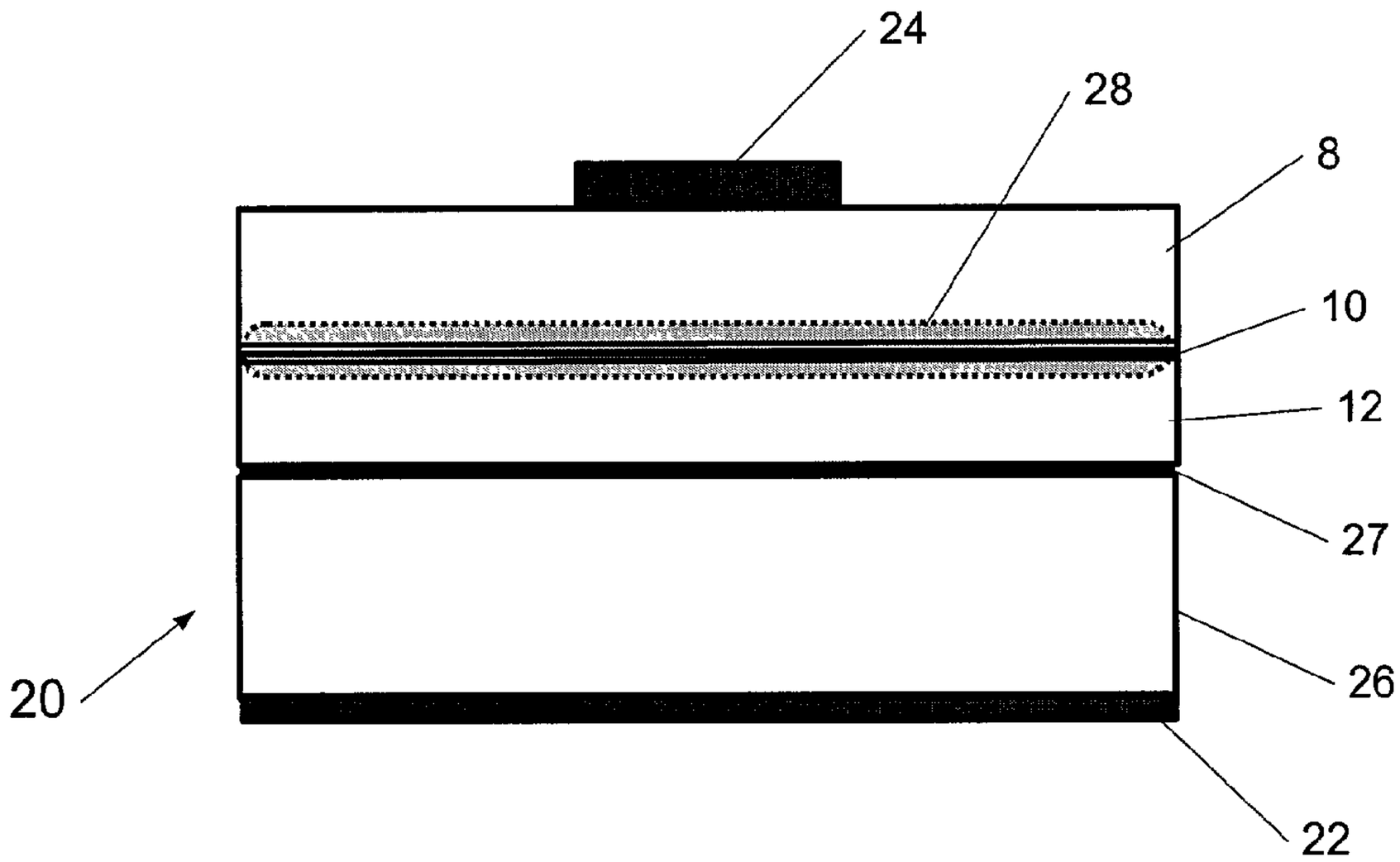


Fig. 2

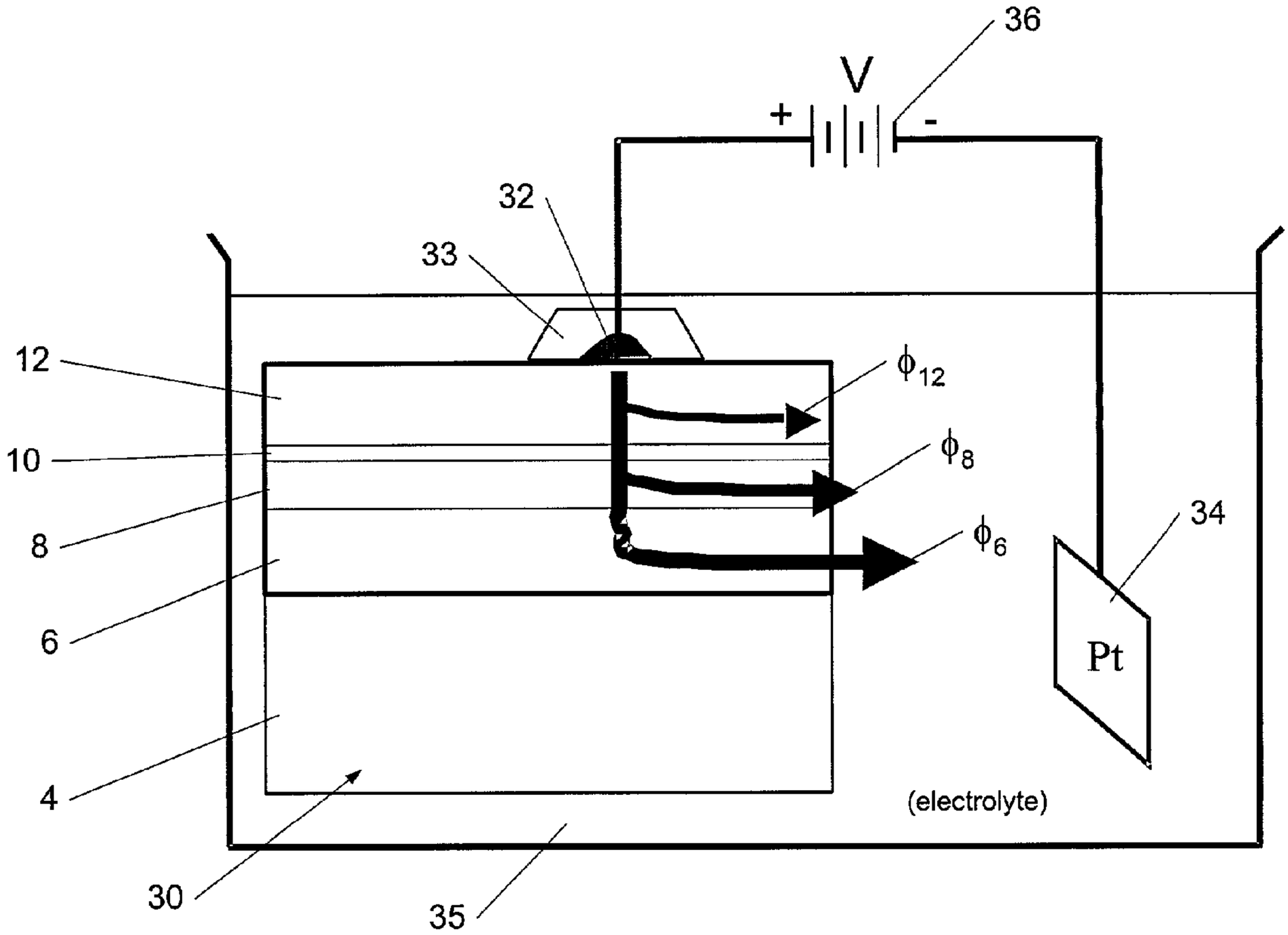


Fig. 3

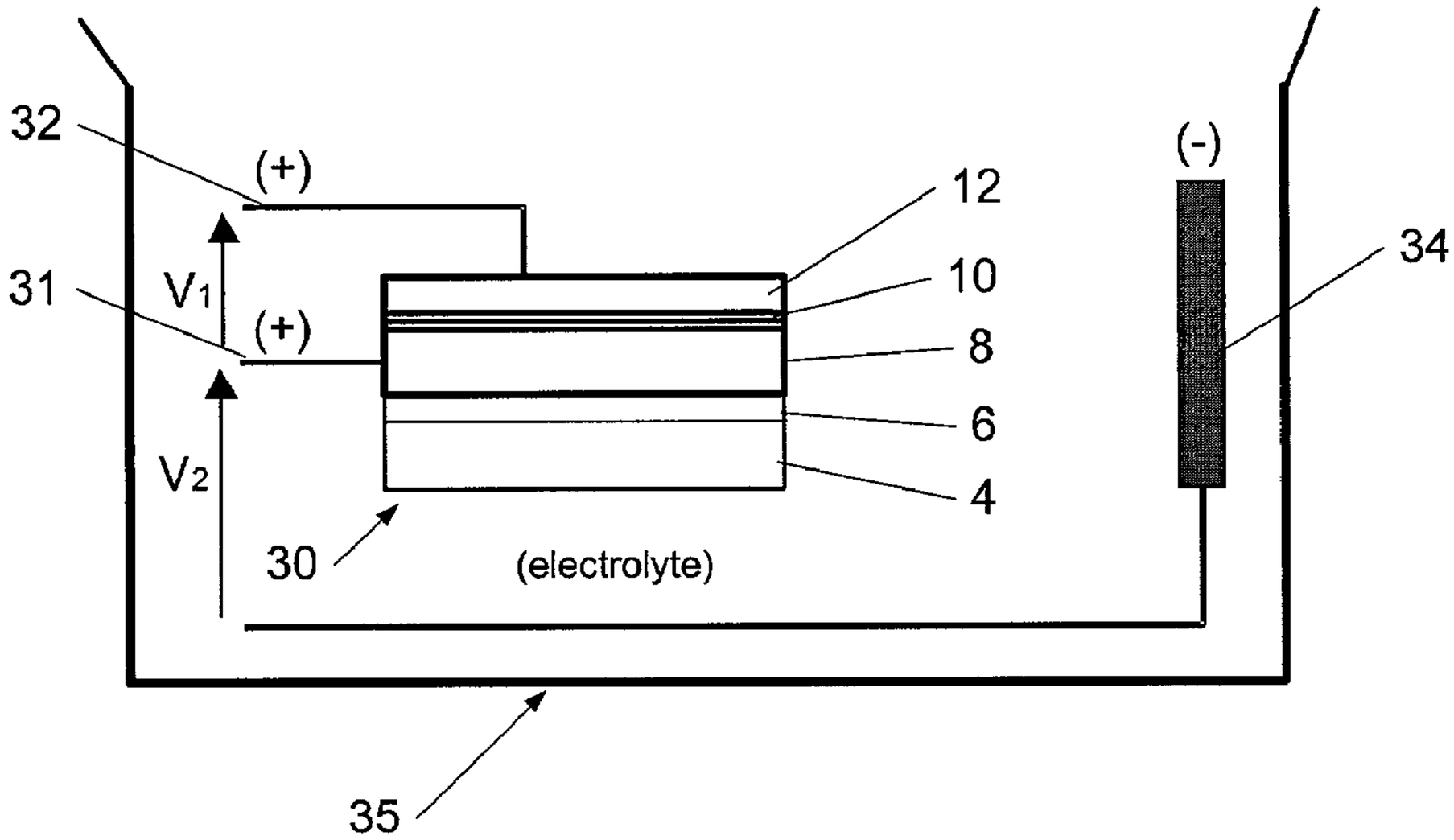


Fig. 4

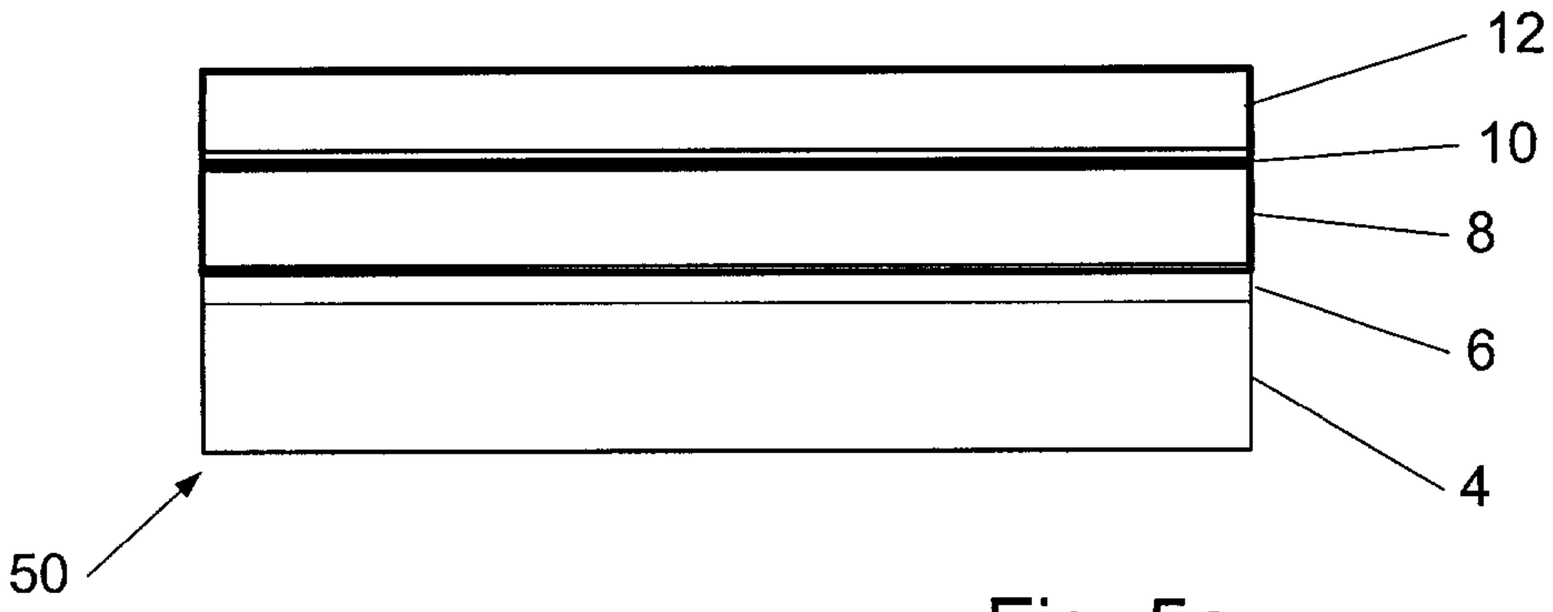


Fig. 5a

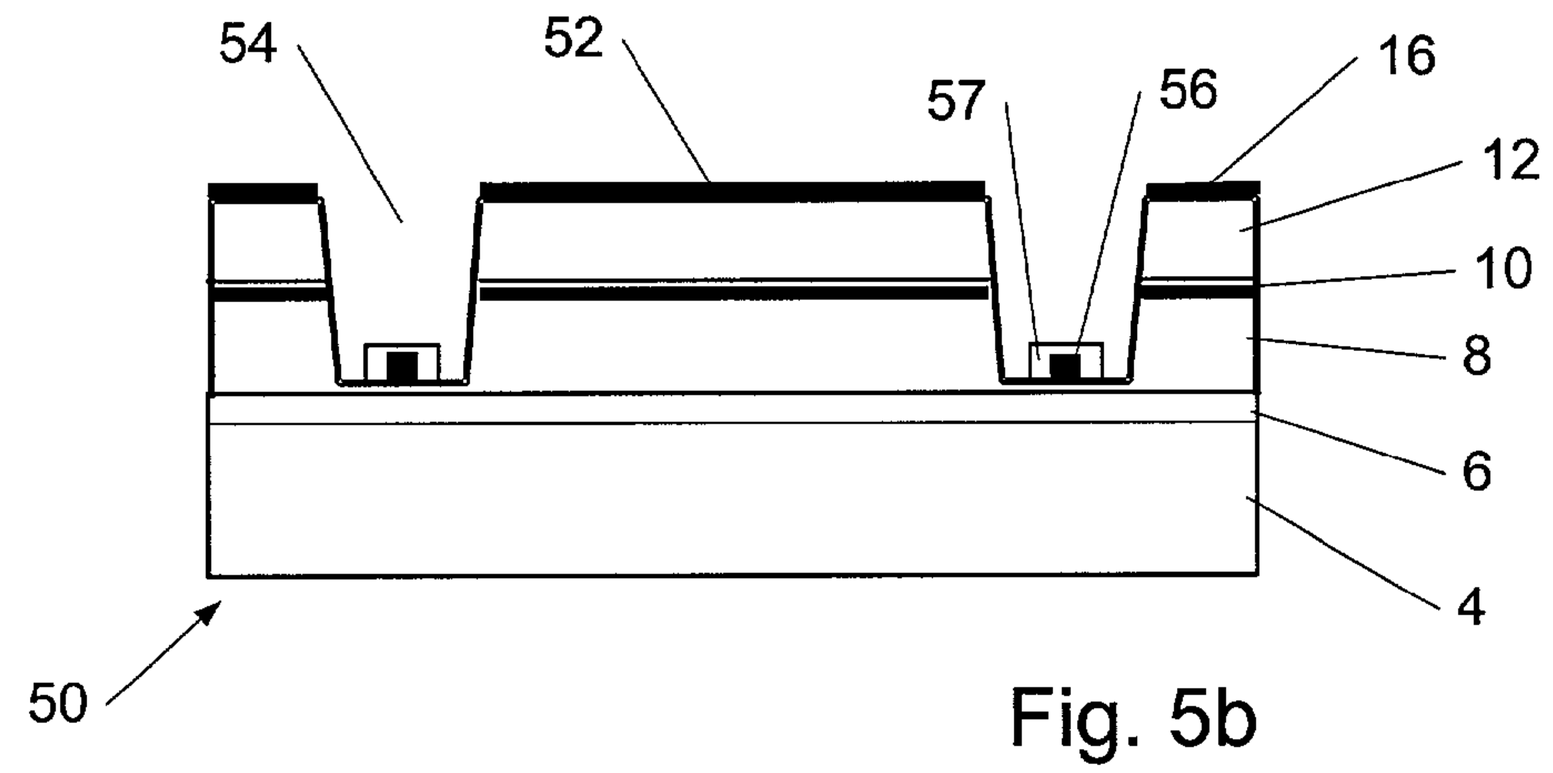


Fig. 5b

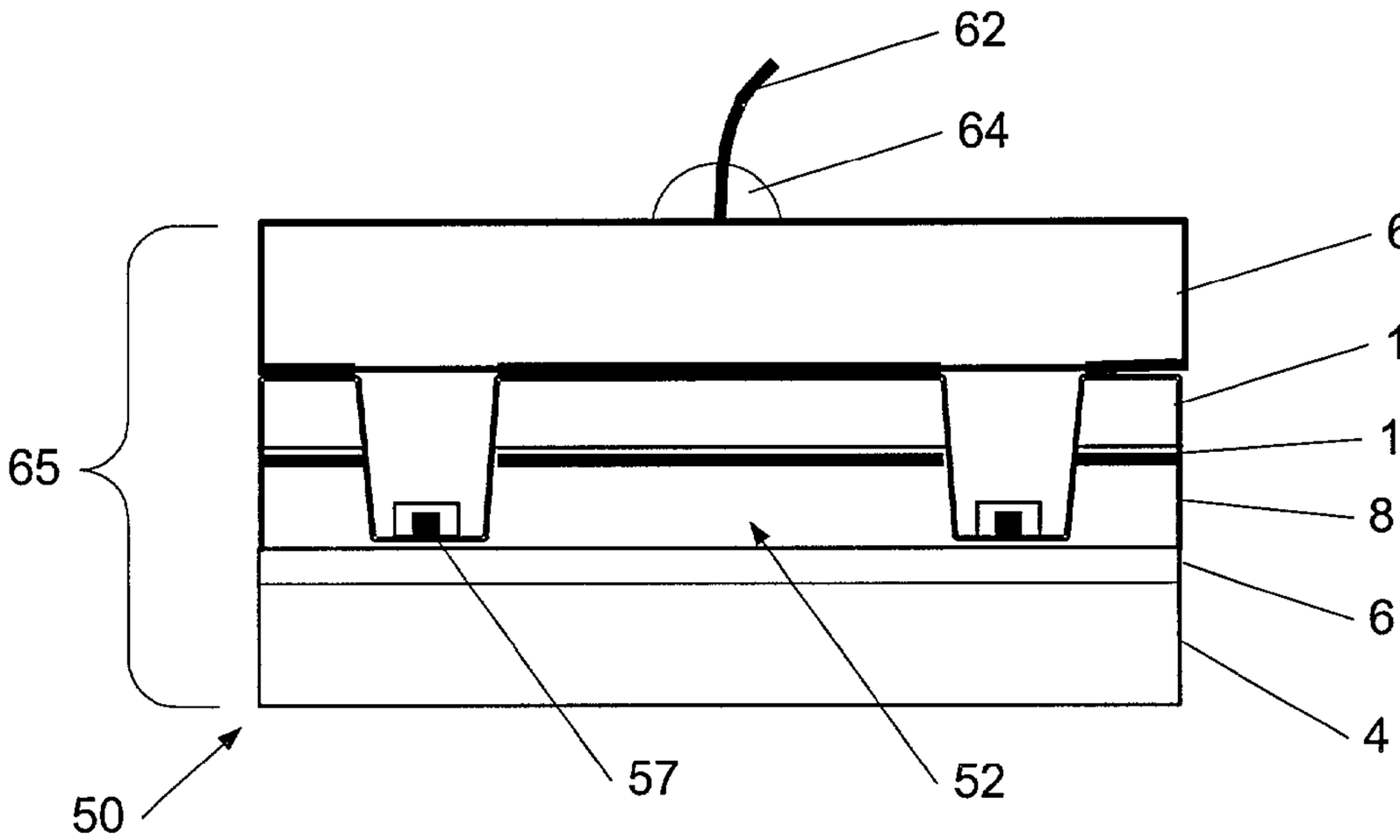


Fig. 5c

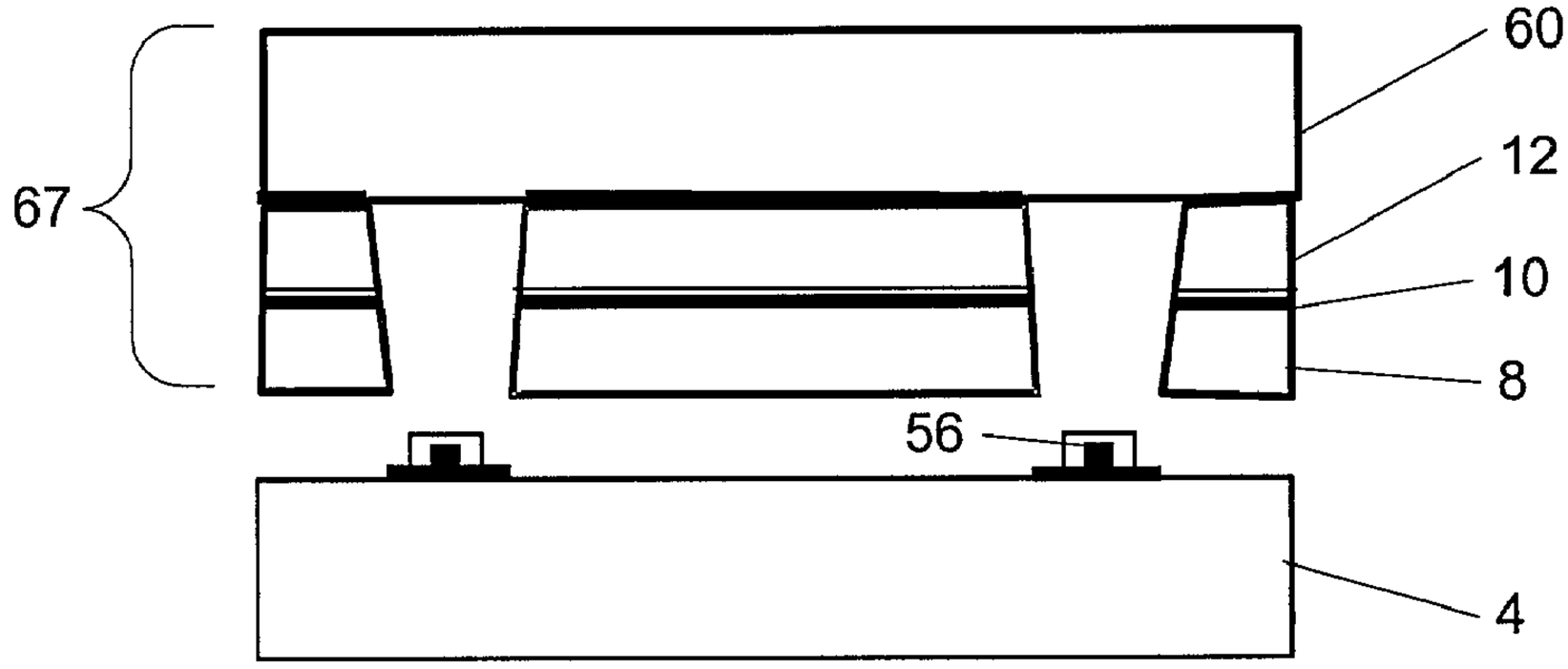


Fig. 5d

Fig. 5e

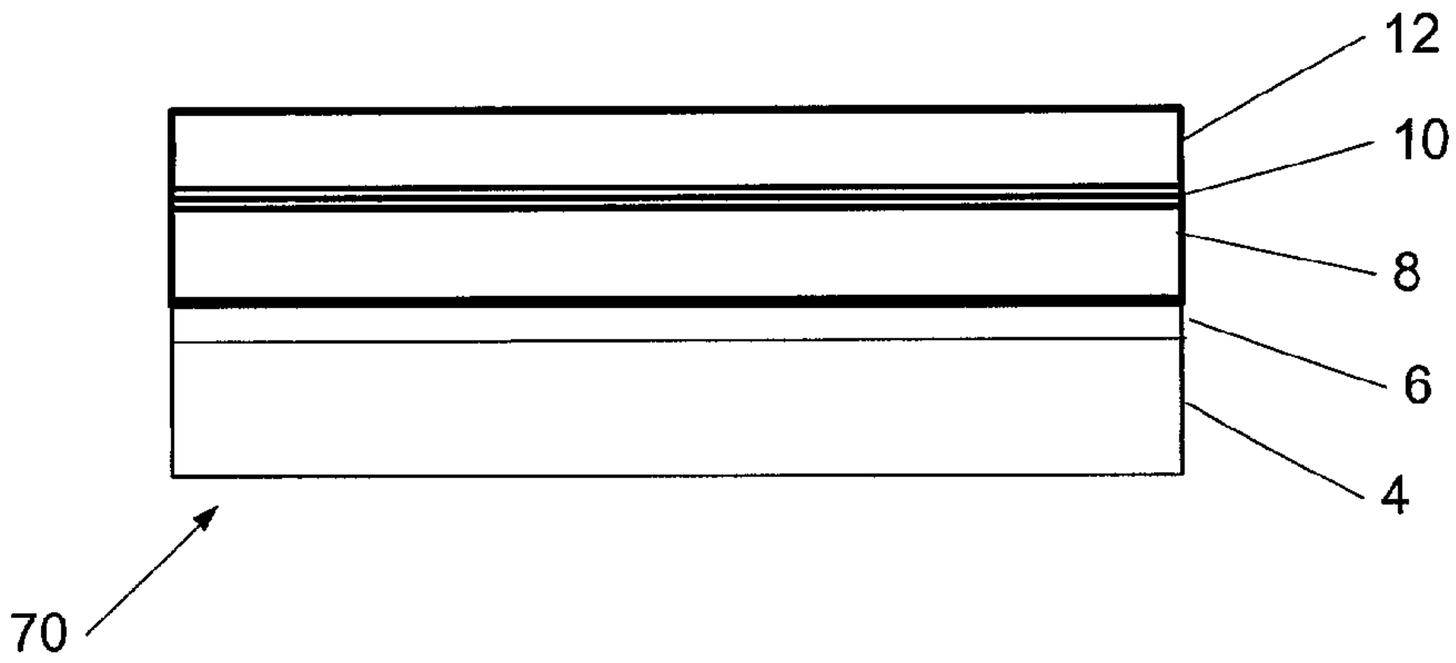


Fig. 6a

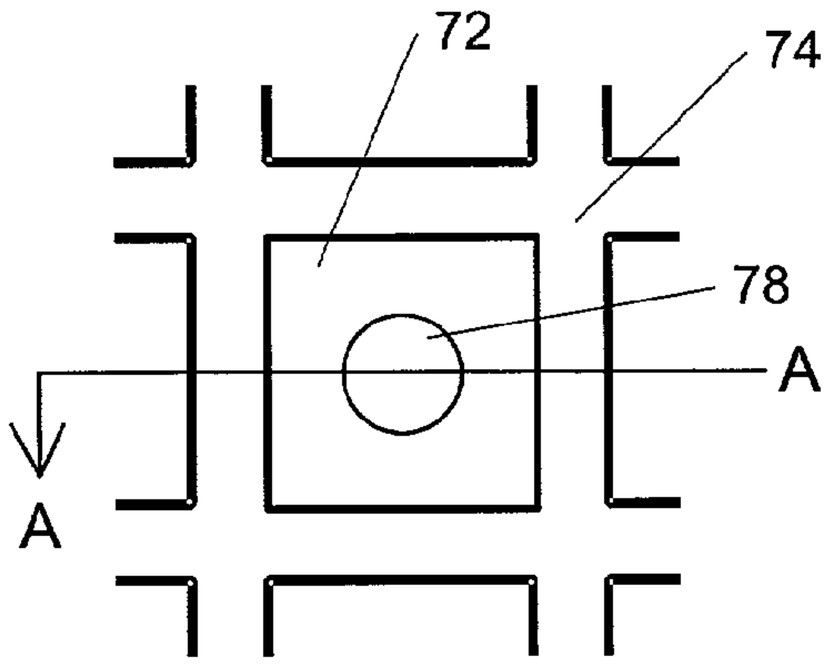


Fig. 6b

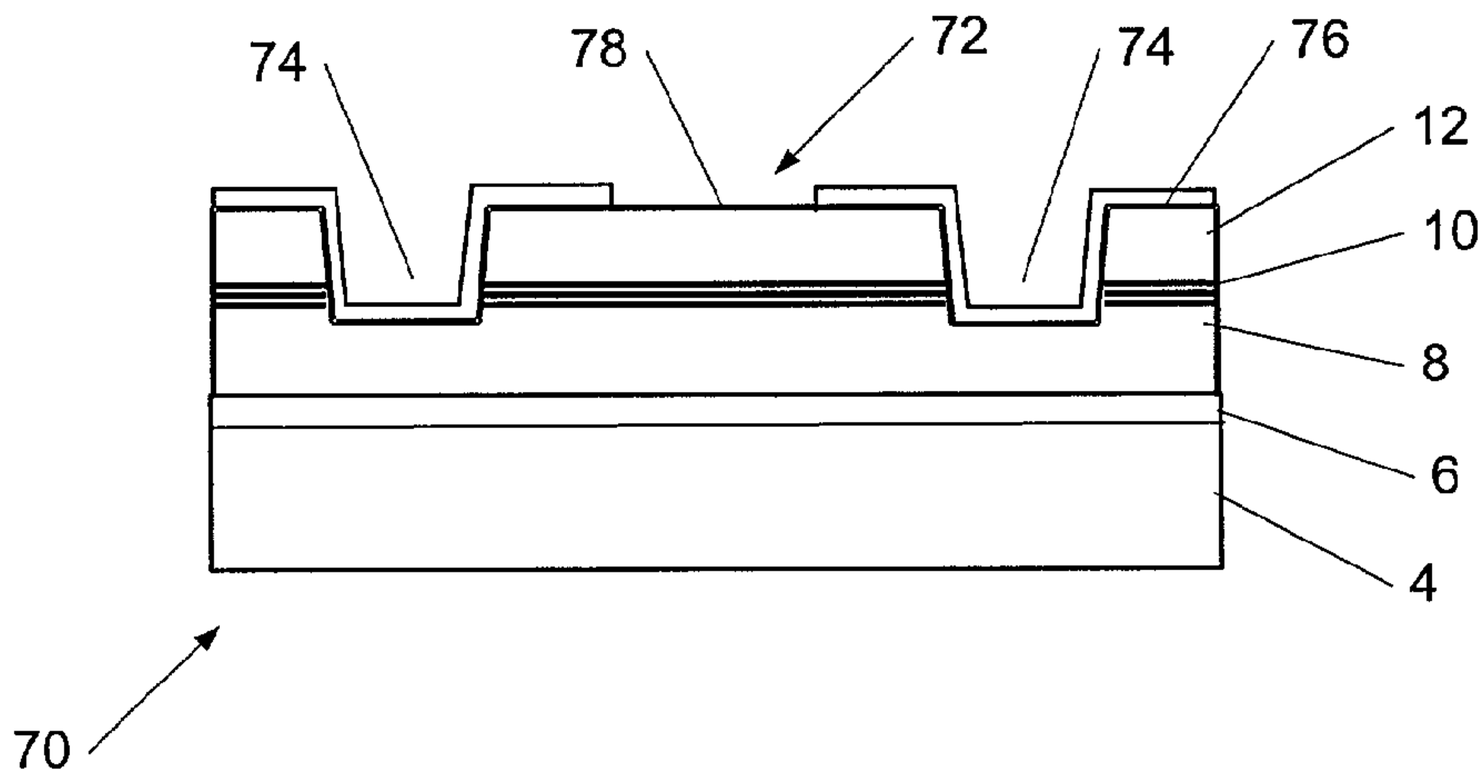


Fig. 6c

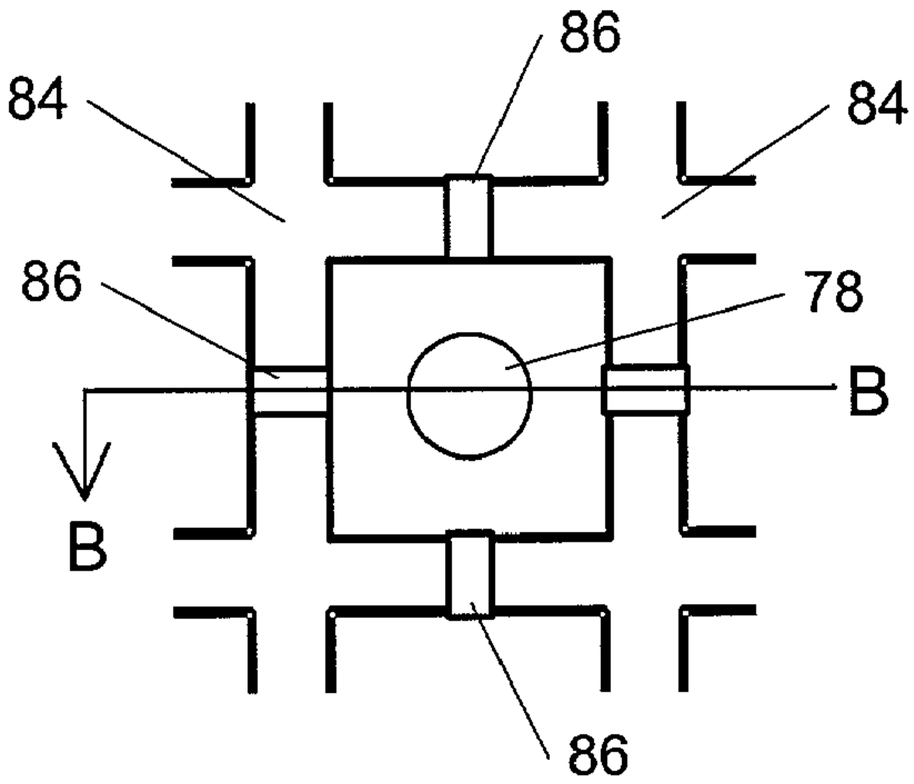


Fig. 6d

Fig. 6e

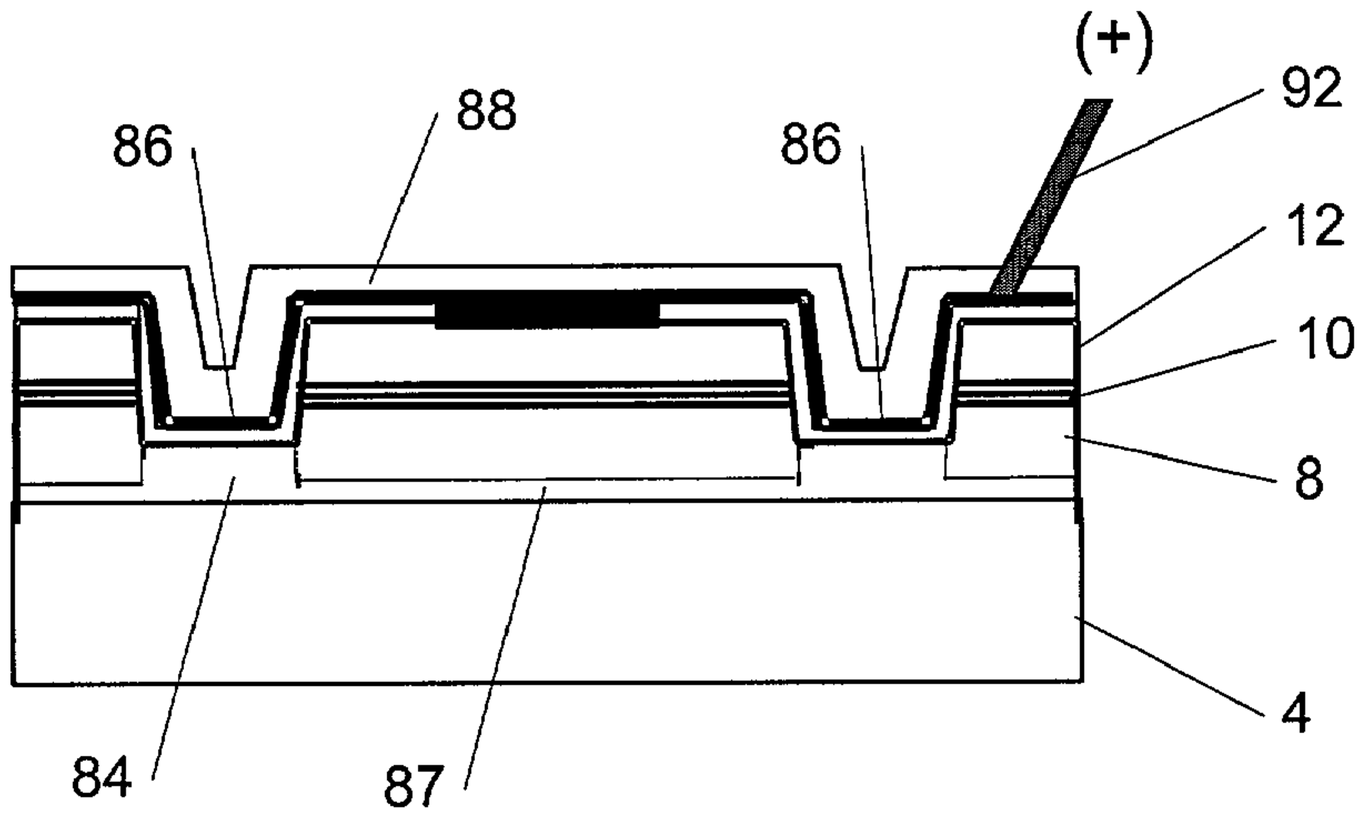


Fig. 6f

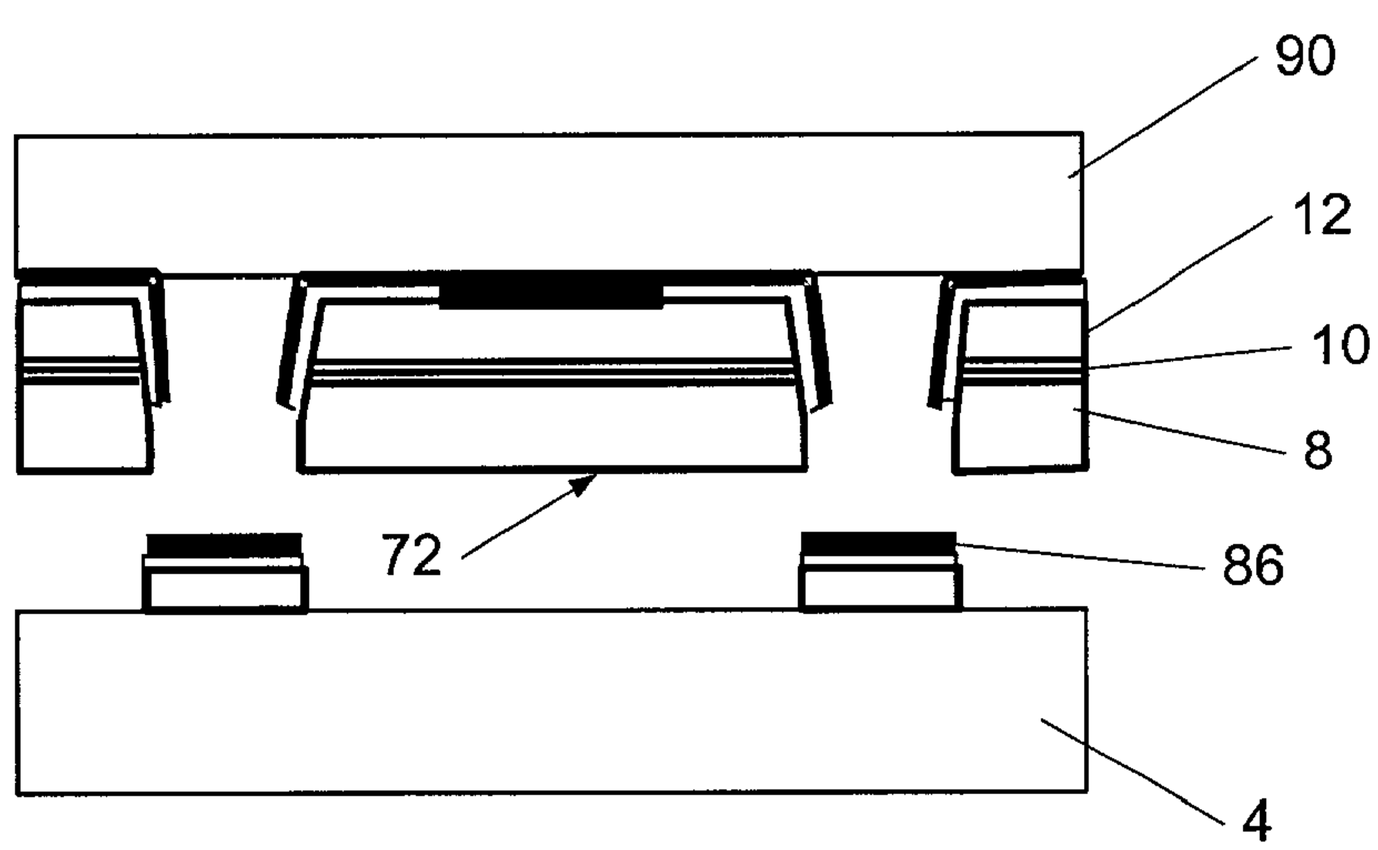


Fig. 6g

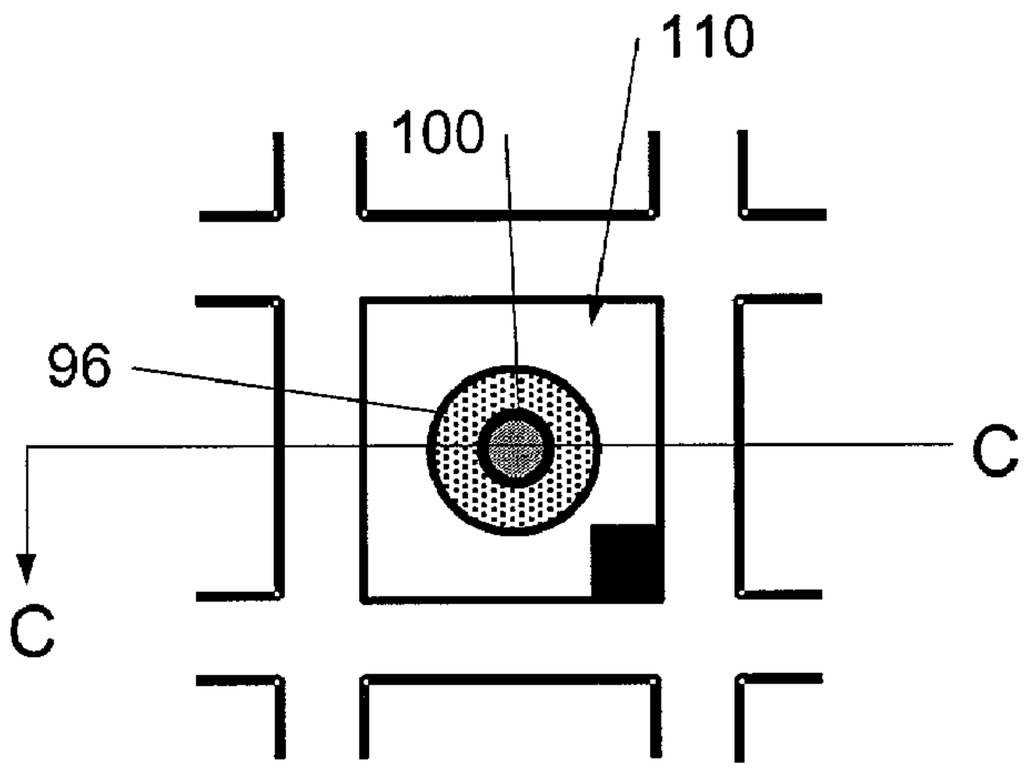


Fig. 6h

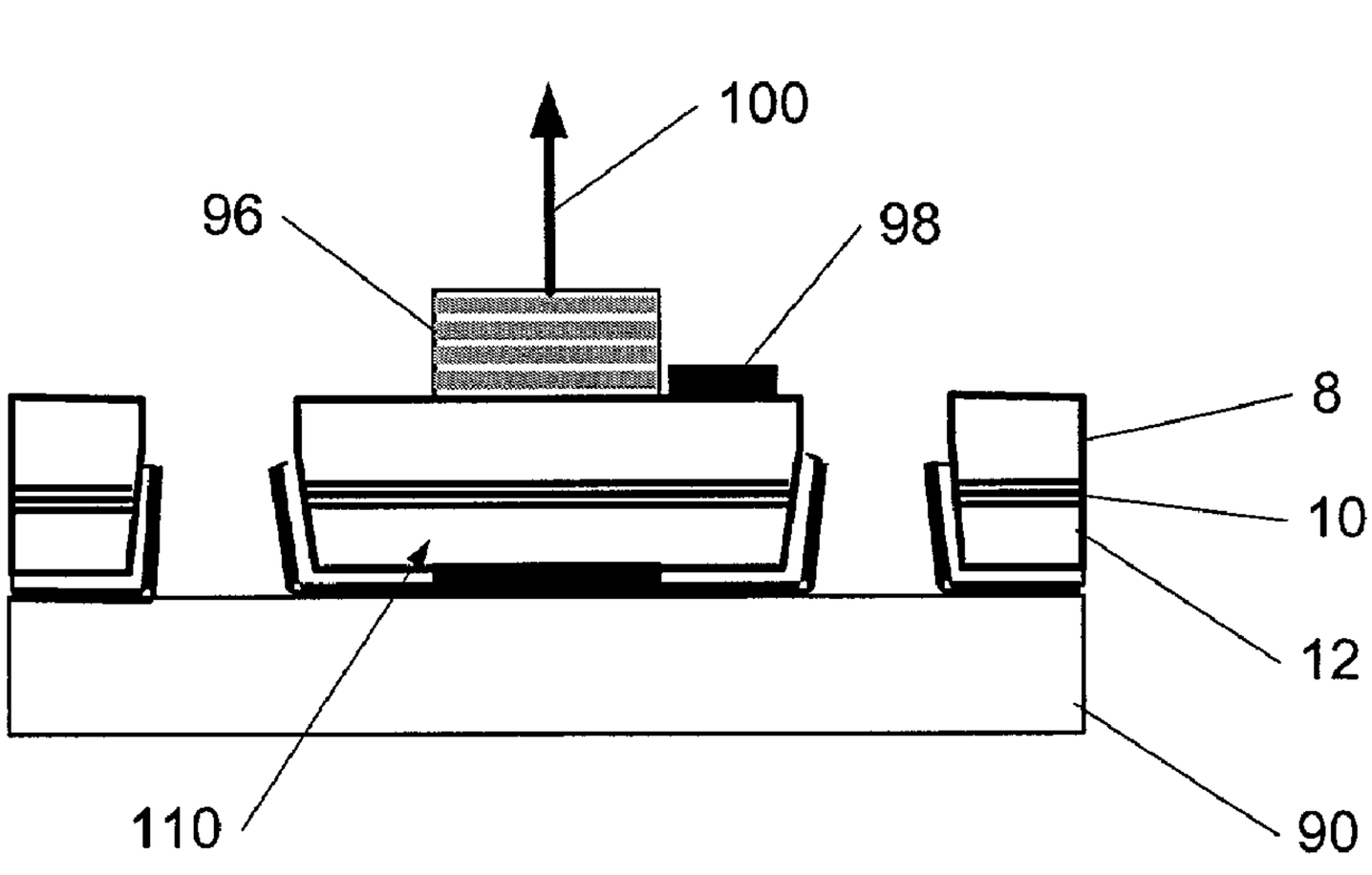


Fig. 6i

METHOD FOR LIFT-OFF OF EPITAXIALLY GROWN SEMICONDUCTORS BY ELECTROCHEMICAL ANODIC ETCHING

FIELD OF THE INVENTION

[0001] The invention relates to a method for lift-off of semiconductor thin films and arrays of fabricated semiconductor devices from insulating growth substrates by using electrochemical anodic etching, and more particularly, to a method for separating GaN-based thin films and GaN-based device structures from a sapphire substrate.

BACKGROUND OF THE INVENTION

[0002] Gallium Nitride (GaN) and its associated alloys are a family of semiconductor materials that exhibit properties suitable for fabrication into special types of optoelectronic and electronic devices. In its most common current application, GaN is used to fabricate blue, green, and other short wavelength light emitting diodes (LEDs). Violet and blue vertical cavity surface emitting lasers (VCSELs), high temperature/high power electronic devices, and other applications have also been demonstrated.

[0003] As a semiconducting material, GaN exhibits properties that are distinct from more common semiconductors like Si and GaAs. Unlike Si and GaAs, GaN is mechanically hard and chemically inert. GaN is also very difficult to synthesize in bulk crystal form. As a result, crystalline GaN is usually grown epitaxially on substrates of dissimilar materials. Such so-called heteroepitaxy is often constrained by the availability of substrate materials that closely match the crystalline and thermal properties of the epitaxial material.

[0004] A common substrate material used for the growth of GaN is c-plane sapphire (α-Al_2O_3), although sapphire is known to have a significant lattice and thermal expansion mismatch to GaN. In spite of these drawbacks, however, sapphire has emerged as the prevalent substrate material because the most mature growth technology has developed on sapphire.

[0005] GaN can be grown on sapphire by, for example, metal-organic chemical vapor deposition (MOCVD) using a so-called two-step growth process. First, a thin buffer layer of GaN is deposited at a relatively low growth temperature of 500° C. to 600° C., followed by growth of a thicker GaN layer at a temperature above 1000° C. nucleated on the buffer layer. The thin buffer layer, commonly referred to as low-temperature (LT) buffer layer, has been shown to be crystalline, but tends to be highly defective and n-type conductive. The thicker GaN layer is nominally single crystalline in the wurtzite crystal structure, but still contains a high density of microstructural defects in the first 0.5 μm near the interface with the LT layer. With increasing thickness of the GaN layer, the defect density gradually decreases to a steady value. At this stage, even though the defect density is still very high by conventional semiconductor device benchmarks, the GaN film has been proven to be of "device quality," as evidenced by the fabrication of LEDs and VCSELs on films of GaN grown by this method.

[0006] While sapphire does have some merits as a growth substrate for GaN, the physical characteristic of sapphire is undesirable for device fabrication. For example, sapphire is electrically insulating. This precludes contacting a GaN device form the substrate side. Furthermore, sapphire has a relatively poor thermal conductivity and is difficult to process by lapping and/or dicing. In addition, since the conductivity of p-type GaN is only a fraction of that of n-type GaN, LEDs fabricated from a conventional GaN/sapphire device structure using conventional methods require large area p-contacts, with both n- and p-contacts to be formed only from one side (the top side) of the device structure.

[0007] As a result, for applications of GaN in light-emitting devices, at least 10% of the die area has to be set aside for forming the n-type contact. With the p-contact formed on the top side of the device, light emitted through the top surface of the device structure will be at least partially obstructed by the p-contact.

[0008] It would therefore be desirable to produce an inverted GaN epilayer structure, with light being emitted through the n-layer and the p-contact being formed across a substantial area of the device without adversely affecting the light emission efficiency.

[0009] Since direct growth of an inverted GaN epilayer structure has not yet been attained, removal of the sapphire substrate from the GaN epilayer structure becomes highly desirable. Conventional physical means of substrate removal, such as lapping, polishing, or chemical etching, have all been hitherto impractical, however, due to the extreme hardness and chemical inertness of sapphire.

[0010] A number of lift-off methods are known in the art for other material systems. For example, a sacrificial layer can be disposed between the device layer(s) and the growth substrate to separate the growth substrate from the epitaxial layer. A typical sacrificial layer is made of a compound that is chemically distinct from the remaining epilayers and can be selectively etched, removed, or decomposed, thereby releasing the epilayer from the growth substrate. This technique has been used successfully with epilayer structures grown on III-V substrates, such as GaAs and InP. First, a thin sacrificial layer, for example, AlAs, is grown on the substrate before growing the intended epilayer structure. Then, the AlAs sacrificial layer is etched away by wet chemical etching, for example, by using a solution of 10% hydrofluoric acid, which is highly selective in etching AlAs as compared to GaAs or low Al-content AlGaAs. So far, a material system that is compatible with the epitaxial growth of GaN or (AlGaIn)N and that can be selectively removed by chemical etching has not been found.

[0011] U.S. Pat. No. 6,071,795 describes a method of laser lift-off for separating a thin film epitaxially grown on a sapphire substrate. A laser beam irradiates the epilayer through the backside of the substrate which locally heats the epilayer near the substrate interface and decomposes the epilayer into its constituents, gallium metal and nitrogen gas. After irradiation, the epilayer and the substrate can be separated by heating above the melting point of Ga metal of 30° C.

[0012] Since both GaN and sapphire are transparent at visible wavelengths, an intense light beam in the UV wavelength range is required, which can only be produced by an expensive high power laser, such as an excimer laser. The limited beam spot size of a laser necessitates that the beam be scanned across a large area in order to lift-off a large

wafer. Such scanning can generate transient spatial nonuniformities in heating and thermal expansion across the wafer which can crack the epilayer during laser lift-off. Moreover, the costs of installing and operating high power lasers undermine the economic viability of using the method of laser lift-off in high volume manufacturing environments.

[0013] It is therefore desirable to develop a less complex method for separating (AlGaIn)N-based thin epitaxial layers as well as fabricated (AlGaIn)N-based device structures from the electrically insulating, transparent substrates, such as sapphire, on which GaN is customarily grown by epitaxy techniques. It is also desirable to develop a method that is low cost, easily controllable, scalable to large wafer areas, suitable for high volume manufacturing environments, and that does not require specific modifications in the device structure, such as the growth of sacrificial layers, to be effective.

SUMMARY OF THE INVENTION

[0014] According to one aspect of the invention, a method is disclosed by which an heteroepitaxial film grown on an insulating substrate can be lifted off the substrate using an electrochemical anodic etching process. The electrochemical anodic etching process exploits the selectivity resulting from different electrochemical etch rates depending on the electrochemical potential of the various layers located near the substrate interface. According to an aspect of the disclosed method, an epitaxial film can be selectively freed from an electrically insulating growth substrate by placing an electrically conductive layer on a surface of the epitaxial film facing away from the insulating substrate to provide an electric contact with the epitaxial film, by placing the epitaxial film having the conductive layer and the insulating substrate in an etching solution, and by applying an electrochemical potential between the epitaxial film and a counter electrode to dissociate an etch layer positioned between the epitaxial film and the insulating substrate to thereby separate the epitaxial film and the insulating substrate from each other.

[0015] According to another aspect of the disclosed method, a light emitting device can be fabricated by providing a semiconductor epitaxial layer structure grown on an electrically insulating substrate and capable of producing light emission under an electric bias; by disposing an electrically conductive layer over a first surface of the epitaxial layer structure facing away from the insulating substrate to provide an electric contact with the epitaxial layer structure; by placing the epitaxial layer structure having the conductive layer and the insulating substrate in an etching solution and applying an electrochemical potential between the epitaxial layer structure and a counter electrode to dissociate a thin etch layer positioned between the epitaxial layer structure and the insulating substrate to thereby separate the epitaxial layer structure and the insulating substrate from each other; and by applying an electric contact to a second surface of the epitaxial layer structure opposite the first surface to provide the electric bias to the epitaxial layer structure.

[0016] Embodiments of the invention may include one or more of the following features. The epitaxial film may be made of a Ill-V semiconductor material, in particular of GaN, AlN, InN and its alloys. The etch layer may be an n-type layer and may include a defect structure having a concentration of defects that is greater than a concentration of defects in the epitaxial film. The etch layer may include a layer that is grown at a growth temperature that is substantially less than a growth temperature of the epitaxial film. For example, the epitaxial film may be grown at 1000° C. or above, whereas the etch layer may include a low-temperature (LT) "seed" layer grown at a temperature of around 500-700° C. and a highly defected region grown at the growth temperature of the epitaxial film. Advantageously, the applied electrochemical potential is greater than the anodization potential of the etch layer and smaller than the anodization potential of the epitaxial film. The insulating growth substrate can be a material that is difficult to etch or lap, such as sapphire, and the epitaxial film can include at least one n-type layer and at least one p-type layer, with one of the n-type layers is disposed adjacent to the etch layer opposite to the growth substrate. Alternatively or in addition, the epitaxial film can include a semiconductor device structure, such as a LED structure, a laser structure, e.g. a VCSEL, a transistor and/or a detector structure.

[0017] The electrochemical potential can be applied between one of the at least one n-type layers and p-type layers and the counter electrode. In addition, a second potential can be applied between an n-type layer and a p-type layer so as to forward bias the n-type layer and p-type layer to cause light emission. The electrically conducting layer can be a host substrate made of, for example, silicon, that may be wafer-bonded to the epitaxial film. To prevent the etching solution from contacting the conductive layer, an insulating layer can be applied over the electrically conductive layer.

[0018] A VCSEL laser can be produced by etching from the top surface trenches that extend through the active layer to define mesas. The mesas are connected by bridges formed from the electrically conductive layer applied, and an insulating layer is applied over the electrically conductive layer to prevent the etching solution from contacting the conductive layer. This permits separation of the VCSELs from the substrate when the conductive layer is a metal that is susceptible to attack by the etching solution.

[0019] Further features and advantages of the present invention will become apparent from the following description of preferred embodiments and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] **FIG. 1** is a schematic diagram of a GaN/sapphire LED device structure;

[0021] **FIG. 2** is a schematic diagram of an inverted GaN LED device structure;

[0022] **FIG. 3** is a schematic diagram of an electrochemical cell with a GaN/sapphire device structure configured as an anode;

[0023] **FIG. 4** is a schematic diagram of an alternative biasing configuration of the electrochemical cell;

[0024] **FIGS. 5***a-e* are schematic diagrams illustrating certain steps of the fabrication method of the invention for LEDs; and

[0025] **FIGS. 6***a-i* are schematic diagrams illustrating certain steps of the fabrication method of the invention for VCSELs.

DETAILED DESCRIPTION OF CERTAIN ILLUSTRATED EMBODIMENTS

[0026] In the figures, similar elements or elements performing a similar function are indicated by identical reference numerals.

[0027] The invention is directed to a method for separating semiconductor epitaxial layers and fabricated semiconductor device structures, in particular GaN-based and (AlGaIn)N-based layers and GaN device structures, from sapphire substrates, using electrochemical anodic etching.

[0028] By way of background information and referring first to **FIG. 1, a** conventional exemplary device structure **2** used in the fabrication of a GaN LED has a sapphire substrate **4**, a low-temperature (LT) buffer layer **6***a* that aids in the growth process, an n-type GaN layer **8**, optionally an active layer **10**, and a p-type GaN layer **12**. Layer **8** will typically be grown at a higher temperature than the LT buffer layer **6***a*. A region **6***b* of the n-type layer **8** which can extend approximately 0.5 μm or more from the LT buffer layer **6***a* into the n-type GaN layer **8** can still include a large number of defects. The combined defect region **6***a*, **6***b* will hereinafter be referred to as "interface region"**6**. Those skilled in the art will appreciate that GaN is merely representative of materials made of Group III-nitrides, such as AlN, GaN, InN and alloys thereof, as well as other semiconductor material systems known in the art and having similar physical and chemical properties. The device structure further includes an n-contact **14** and a p-contact **16**. Since the sapphire substrate **4** is insulating, the n-contact **14** is applied to a top surface **15** of the n-type layer **6** that is exposed, for example, by etching. The p-contact **16** is applied in a conventional manner to a top surface **17** of the p-type layer **12**. Most conventional devices have this type of mesa structure.

[0029] As mentioned above, the top p-type layer **12** has a poor electrical conductivity, so that light emission originates predominantly from a light emitting region **18** located essentially directly under the p-contact **16** which disadvantageously obscures much of the produced light.

[0030] An inverted GaN device structure **20** illustrated in **FIG. 2**, to which the subject matter of the present invention is directed, has the p-type layer **12** at the bottom, with the electrical contact **26** to the p-type layer **12** provided substantially across the entire surface area of the die. The device structure **20** can be prepared by wafer-bonding the p-type layer **12** of the GaN device structure **20** to a host substrate **22**, such as p-type Si or another suitable semiconductor or metal, either directly or by interposing a separate contact layer **27**. Because of the superior electrical conductivity of the n-type GaN, the n-contact **24** can be applied from the top across a much smaller surface area than the p-type contact of the conventional device structure depicted in **FIG. 1**. However, the n-contact **24** can only be applied after the insulating sapphire substrate has been removed. Accordingly, an efficient process for separating the GaN layers or the GaN device structure from the electrically insulating sapphire substrate is desirable.

[0031] As mentioned above, both GaN and sapphire are resistant to most chemicals and sapphire is difficult to remove by lapping. However, it has been observed that GaN can be selectively etched in an electrochemical bath.

[0032] **FIG. 3** shows an electrochemical cell **35** containing a suitable electrolyte, for example, a dilute acid or an alkali solution of NaOH or KOH. The cathode **34** can be made of platinum. The GaN/sapphire device structure **30** forms the anode, with a positive potential V from a suitable power supply **36** applied to the p-type GaN layer **12** through a contact **32** that is insulated from the electrolyte by an insulating material **33**, such as wax. The LT buffer layer **6** of the device structure **30** plays an important role in the etching process, as will now be described.

[0033] It has been observed that when a current is passed through GaN immersed in the electrochemical bath **35**, the GaN will be etched at a significant rate even at room temperature. The reaction rate depends on the magnitude of the electric current, the structural quality of the GaN sample, and the doping type.

[0034] A chemical etching reaction on semiconductor requires the presence of positive carriers called holes on the surface of the semiconductor in order for the reaction to take place. It has been observed that electrochemical etching of n-GaN is favored over p-GaN which may be caused by electronic band bending near the semiconductor surface. For example, holes being the minority carrier in n-type GaN can accumulate near the sample surface, making the n-type GaN more susceptible to etching or oxidation than its p-type counterpart. It has also been observed that the defect density in a region of a sample of a given doping type affects electrochemical etching in that region, with defected regions being etched faster than crystalline regions.

[0035] The ease of etching of a material is represented quantitatively by its anodization potential ϕ, which is defined as the minimum voltage that must be applied between a cathode and a sample of the material configured as an anode in order for etching to occur. It has been observed that the highly defected n-type interface region **6** which includes the n-type LT buffer layer **6***a* and the defected region **6***b* of **FIG. 1**, can be selectively etched with a significantly higher etch rate than the rest of the device structure. The defected n-type interface region **6** thus plays an important role in epitaxial lift-off by electrochemical anodic etching; hence, the defected n-type interface region will hereinafter also be referred to as an "etch layer." Considered in light of the typical layer growth sequence in epitaxial GaN/sapphire, the natural order of selectivity for electrochemical etching of GaN forms the foundation of the present invention for achieving epitaxial lift-off using electrochemical etching.

[0036] As mentioned above, the etch rate depends strongly on the anodization potential ϕ of the anode. As it turns out, the anodization potential ϕ_6 of the defected n-type interface region (or etch layer) **6** is smaller than both the anodization potentials ϕ_{12} of the p-type GaN layer **12** and ϕ_8 of the n-type GaN layer **8** of the device structure **30**. Accordingly, if the voltage V is chosen to be greater than the anodization potential ϕ_6 of the defected n-type interface region **6**, but smaller than either of the anodization potentials ϕ_8 and ϕ_{12}, then the defected n-type interface region **6** will be etched preferentially, thereby releasing the n-type GaN layer **8** from the sapphire substrate **4**. The selectivity will be maintained as long as there is no light with a photon energy greater than the bandgap of GaN illuminating the device structure **30**.

[0037] In the structure shown in **FIG. 3**, the GaN device structure **30** is forward biased, allowing the current to reach all layers **6**, **8**, **10**, **12**, including the etch layer **6**. However,

a particular layer structure (not shown) may include a reverse biased p-n junction. In this case, the external contact is made to a layer from which current can flow to the etch layer **6**. A particular layer or layers that can be exposed, for example, by dry etching. As already noted, to anodically etch a specified region, that region should have a suitable anodization potential and the electrolyte **56** must come in contact with that region. This contact can be achieved by directly exposing the etch layer **6** to the electrolyte. Alternatively, etching may proceed from the n-type GaN layer **8** and the p-type GaN layer **12** until the electrolyte can contact the etch layer **6**. The latter approach has also shown feasibility.

[**0038**] The selectivity and etching rate can be enhanced by illuminating the device structure **30** with sub-bandgap light that can be generated internally in the device structure **30**, either by the etch current flowing through the p-n junction (using the two-terminal configuration of **FIG. 3**) itself or, alternatively, by applying a suitable external forward voltage to the p-n junction (using a three-terminal configuration depicted in **FIG. 4**).

[**0039**] In the basic two-terminal circuit configuration of **FIG. 3**, the total injected current reaches the cathode **34** through the electrolyte. Current injected through contact **32** into the p-type GaN layer **12** flows through the forward-biased p-n junction to the n-type GaN layer **8** and from there to the cathode **34**. Accordingly, light emission will be produced at the forward-biased p-n junction. The photon energy of the emitted light is typically smaller than the bandgap of GaN and will therefore not be substantially absorbed in the GaN layers. However, since the etch layer **6** contains a high number of defect states that form electronic states in the bandgap (mid-gap states) having a lower energy than the bandgap of GaN, the emitted light will be absorbed by the etch layer **6**. Absorption of the emitted light increases the reactivity of the highly defected etch layer **6**, thereby enhancing the etch rate and selectivity.

[**0040**] As seen in **FIG. 3**, with a two-terminal configuration the current passing through the GaN p-n junction cannot be greater than the total anodization current flowing through the electrolyte. As a result, the maximum reaction rate eventually limits the amount of light that can be produced at the p-n junction with the two-terminal configuration of **FIG. 3**.

[**0041**] **FIG. 4** illustrates a corresponding three-terminal circuit configuration mentioned above, which allows a current greater than the anodization current to flow through the p-n junction to produce light emission. A p-n junction biasing voltage V_1 is applied between the anode **32** and an axialiary anode **31** contacting another layer, for example, the n-type GaN layer **8**. The voltage V_1 can be chosen independently of the anodization voltage V_2 to provide greater control over the anodic etching rate by adding a controlled amount of internally produced light.

[**0042**] The present invention does not rely on an electrically conductive substrate. In fact, the present invention does not even require the interface region or etch layer to be a physical layer, but merely a region where a high density of structural defects is confined, such as near the growth interface of a lattice-mismatched heteroepitaxial layer, so as to produce a suitable anodization potential.

[**0043**] An exemplary application of the present invention is the fabrication of light emitting devices, such as LEDs having an improved light extraction efficiency. Another application is the fabrication of lasers, for example, vertical cavity surface emitting lasers(VCSELs). LEDs and lasers have a similar device structure, but differ in their current density and heat-sinking requirements. To improve heat sinking, VCSELs are bonded to a metal host substrate, such as Cu or Al, which has a high electrical and thermal conductivity. Since high conductivity metals tend to react with the electrolyte by shunting the current directly to the electrolyte, VCSELs have to be lifted off the sapphire substrate before being bonded to the metal.

[**0044**] Referring first to **FIGS. 5***a*-**5***e,* GaN LEDs are fabricated by first growing a layer structure **6**, **8**, **10** and **12** on a sapphire substrate **4**, which is similar to the device structure **2** of **FIG. 1**. As seen in **FIG. 5***b,* mesas **52** are formed in the GaN LED wafer **50** by etching trenches **54**, with each mesa **52** to form an LED die. The trenches **54** are etched to a depth so as to be proximate to the GaN/sapphire interface to expose the highly defective interface region **6** (etch layer). When using the three-terminal configuration depicted in **FIG. 4**, metal lines **56** that contact a portion of the n-type GaN layer **8** may be fabricated in the trenches **54**. The metal lines **56** should be covered with an insulator **57** so as not to come into direct contact with the electrolyte. As in **FIG. 1**, Ni/Au or NiO_x/Au can be used as the p-contact metal **16**, as is known in the art. Since, as discussed above with reference to **FIG. 2**, the p-contact **16** need not be transparent, the p-contact layer **16** can have a thickness of several thousand Å.

[**0045**] As illustrated in **FIG. 5***c,* the etched and metalized GaN LED wafer **50** is then wafer-bonded to a host substrate **60**, such as a p-Si wafer, wherein the p-contact **16** can be used as a bonding metal. The so formed wafer-bonded structure **65** is configured as the anode **52** in the electrochemical cell **35** shown in **FIG. 3**. A contact **62** which can be protected from the electrolyte by an insulator **64** as described above with reference to **FIG. 3**, is applied to the host substrate **60**. A dilute acid, such as sulfuric acid, can be used as an electrolyte to minimize spurious reactions with the Si host substrate **60**. Current flows through the host substrate **60** and the mesas **52**, thereby concentrating the current in the mesa areas to etch the defected n-type interface region **6**. As each mesa **52** is progressively undercut at the sapphire substrate **4**, the current flowing through the mesas will decrease due to the greater anodization potentials ϕ_8 and ϕ_{12} of the crystalline layers **8** and **12**, respectively. Hence, the etching process is self-limiting, uniform and easily controllable.

[**0046**] After the defected n-type interface region **6** is etched away, the sapphire substrate **4** with the remaining metal lines **56** can be mechanically removed from the device portion **67**, as indicated in **FIG. 5***d*. A backside p-contact **68** can be applied to the backside of the Si host substrate **60**, with n-contacts **24** contacting the n-type GaN layer **8** of mesa **52**, as indicated in **FIG. 5***e*. As already mentioned above with reference to **FIG. 2**, the contact area of contact **24** can be quite small due to the excellent electrical conductivity of n-type GaN. The resulting GaN LED dies, which substantially correspond to the mesas **52**, can be separated and packaged in the same manner as conventional LEDs.

[**0047**] Referring now to **FIGS. 6***a* through **6***i,* VCSELs have a similar device structure **70** as the LED device

structure **50** of **FIG. 5***a*. The active layer **10** may contain a multiple quantum well (MQW), as is known in the art. As indicated in **FIG. 6***b*, which is a top view of the device structure **70**, a pattern of first trenches **74** is etched in the GaN VCSEL device structure **70**, for example by dry etching, to define mesas **72**. Unlike mesa etching of LEDs, however, the first trenches **74** of the VCSELs are only etched to a depth just below the MQW **10**, as indicated in **FIG. 6***c* which is a cross section of **FIG. 6***b* along the line A-A. A layer **76** of SiO_2 is deposited over the mesas **72** and the first trenches **74** to passivate the surface. A p-contact window **78** is opened on the mesas **72**, and a p-contact metal **82** is applied across the top surface of the device structure **70**, as seen in **FIG. 6***e*. The p-contact metal **82** should be selected so as to have a low resistivity and be reasonably reflective at the lasing wavelength. Combinations of Ni/Pt or NiO_x/Pt are suitable as the p-contact metal **82**. Although the SiO_2 window defines the actual p-contact to the GaN, the p-contact metal **82** should cover the whole mesa top to facilitate subsequent bonding and heat sinking to a host substrate.

[**0048**] Referring seen in **FIG. 6***e*, a layer of photoresist **88** is applied that covers the entire p-metallized device area, whereafter second trenches **84** are opened up by a photolithographic and etching process to expose the defected n-type interface region **6** to the electrolyte. As best seen in the top view of the device structure **70** depicted in **FIG. 6***d*, the second trenches **84**, unlike the trenches **54** of the LED structure **50**, are patterned to be discontinuous along the side face of a mesa. The second trenches **84** are etched down to near the GaN/sapphire interface. Interconnect bridges **86** that are formed of the p-metal **82** left standing after etching the photoresist **88**, interconnect adjacent mesas **72**. **FIG. 6***e* is a cross-sectional view of **FIG. 6***d* along the line B-B. As illustrated in **FIGS. 6***d* and **6***e*, the device structure is an array of mesas **72** linked by the interconnect bridges **86**, with a portion of the photoresist layer **88** covering the interconnect bridges **86** to provent the p-contact metal **82** from coming into contact with the electrolyte during electrochemical anodic etching.

[**0049**] As mentioned above with reference to GaN LEDs, the GaN VCSEL wafer **70** forms the anode in the electrochemical cell **35** as shown in **FIG. 3**. As indicated in **FIG. 6***f*, external contact to the p-metal **82** can be made with a probe tip **92**. Like the p-metal itself, the probe tip **92** should be electrically insulated from the electrolyte. For a three-terminal configuration similar to the one depicted in **FIG. 4**, an additional terminal (not shown) can be applied to an exposed portion of n-type GaN, for example, near at the periphery of the device structure **70** since the entire underlying n-GaN layer **8** is still contiguous. During anodic etching, each mesa **72** is undercut, starting around its perimeter and propagating toward the center of the mesa **72**, leaving a void **87** in place of the defected n-type interface region **6**. The current distribution pattern discriminates against etching underneath the interconnect bridges **86**, leaving the interconnect bridges **86** attached to the sapphire substrate **4**. As a result, at the end of etching, when all of the mesas **72** have been undercut, the interconnect bridges **86** hold the mesas **72** in position, thereby preventing a shift in position and detachment from the sapphire substrate **4**.

[**0050**] Referring now to **FIG. 6***g*, after electrochemical anodic etching, the photoresist layer **88** is removed, and the interconnected VCSEL device structure **70** is mechanically separated from the sapphire substrate **4** and bonded to, for example, a Cu host substrate **90** by using, for example, a thin layer of In metal. The interconnect bridges **86** can remain on the sapphire substrate **4**, similar to the metal lines **56** of the LED structure **50** (**FIG. 5***d*). At this stage, each mesa **72** is an inverted VCSEL device, with the n-side facing up.

[**0051**] **FIGS. 6***h* and **6***i* show a completed VCSEL structure **110**, with **FIG. 6***h* representing a top view and **FIG. 6***i* representing a cross sectional view along the line C-C of **FIG. 6***h*. A mirror, such as a partially reflecting dielectric stack **96** made of, for example, alternating layers of HfO_2/SiO_2 can be deposited on the n-type GaN top side of each inverted mesa **110** to provide optical feedback. N-contact pads **98** can be placed on the mesas **72** adjacent to the dielectric stack **96**. Laser emission **100** will emerge from the partially reflecting dielectric stack **96**.

[**0052**] While the present invention has been disclosed in connection with the preferred embodiments shown and described in detail, various modifications and improvements thereon will become readily apparent to those skilled in the art. Since a high defect concentration is typically observed near the growth interface for heteroepitaxial growth on lattice-mismatched substrates, the present invention may be used with other materials grown on highly defected layers. Accordingly, the spirit and scope of the present invention is to be limited only by the following claims.

We claim:

1. A method for selectively freeing an epitaxial film from an electrically insulating growth substrate comprising

(a) placing an electrically conductive layer on a surface of the epitaxial film facing away from the insulating substrate to provide an electric contact with the epitaxial film,

(b) placing the epitaxial film having the conductive layer and the insulating substrate in an etching solution, and

(c) applying an electrochemical potential between the epitaxial film and a counter electrode to dissociate an etch layer positioned between the epitaxial film and the insulating substrate to thereby separate the epitaxial film and the insulating substrate from each other.

2. The method according to claim 1, wherein the epitaxial film comprises a III-V semiconductor material.

3. The method according to claim 2, wherein the III-V material comprises a material selected from the group consisting of GaN, AlN, InN and alloys thereof.

4. The method according to claim 1, wherein the etch layer is an n-type layer.

5. The method according to claim 1, wherein the etch layer includes a defect structure having a concentration of defects that is greater than a concentration of defects in the epitaxial film.

6. The method according to claim 5, wherein the etch layer includes a layer grown at a growth temperature that is substantially less than a growth temperature of the epitaxial film.

7. The method according to claim 6, wherein the etch layer comprises a low-temperature (LT) GaN layer.

8. The method according to claim 1, wherein the applied electrochemical potential is greater than the anodization potential of the etch layer and smaller than the anodization potential of the epitaxial film.

9. The method according to claim 1, wherein the insulating growth substrate comprises sapphire.

10. The method according to claim 1, wherein the epitaxial film comprises a semiconductor device structure.

11. The method according to claim 10, wherein the semiconductor device structure comprises at least one n-type layer and at least one p-type layer.

12. The method according to claim 11, wherein the semiconductor device structure is one of a light-emitting diode (LED) or a vertical cavity surface emitting laser (VCSEL).

13. The method according to claim 12, wherein one of the at least one n-type layers is disposed adjacent to the etch layer opposite to the growth substrate.

14. The method according to claim 12, wherein the electrochemical potential is applied between one of the at least one n-type layers and p-type layers and the counter electrode, and further including applying a second potential between an n-type layer and a p-type layer so as to forward bias the n-type layer and p-type layer to cause light emission.

15. The method according to claim 1, wherein the electrically conducting layer is a host substrate and placing includes wafer bonding the host substrate to the epitaxial film.

16. The method according to claim 1, wherein the host substrate comprises silicon.

17. The method according to claim 1, and further comprising after step (a):

applying an insulating layer over the electrically conductive layer to prevent the etching solution from contacting the conductive layer.

18. A method for fabricating a light emitting device comprising

(a) providing a semiconductor epitaxial layer structure grown on an electrically insulating substrate and capable of producing light emission under an electric bias,

(b) disposing an electrically conductive layer over a first surface of the epitaxial layer structure facing away from the insulating substrate to provide an electric contact with the epitaxial layer structure,

(c) placing the epitaxial layer structure having the conductive layer and the insulating substrate in an etching solution,

(d) applying an electrochemical potential between the epitaxial layer structure and a counter electrode to dissociate a thin etch layer positioned between the epitaxial layer structure and the insulating substrate to thereby separate the epitaxial layer structure and the insulating substrate from each other, and

(e) applying an electric contact to a second surface of the epitaxial layer structure opposite the first surface to provide the electric bias to the epitaxial layer structure.

19. The method according to claim 18, wherein the semiconductor epitaxial layer structure comprises a material selected from the group consisting of GaN, AlN, InN and alloys thereof.

20. The method according to claim 18, wherein the semiconductor epitaxial layer structure is a vertical cavity surface emitting laser (VCSEL) structure having an active layer, the method further including:

after step (a), etching from the first surface a plurality of trenches that extend through the active layer to define mesas, wherein the mesas are connected by bridges formed from the electrically conductive layer applied in step (b), and

after step (b), applying an insulating layer over the electrically conductive layer to prevent the etching solution from contacting the conductive layer.

21. The method according to claim 20, and further including disposing a reflector on the second surface to provide feedback for the VCSEL.

22. The method according to claim 20, and further including after step (d), connecting the conductive layer with a heat sink.

23. The method according to claim 18, wherein the electrochemical potential is selected to be greater than the anodization potential of the etch layer and smaller than the anodization potential of the epitaxial layer structure.

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