US012057989B1

(12) **United States Patent**
Adl et al.

(10) **Patent No.: US 12,057,989 B1**
(45) **Date of Patent: Aug. 6, 2024**

(54) **ULTRA-WIDE INSTANTANEOUS BANDWIDTH COMPLEX NEUROMORPHIC ADAPTIVE CORE PROCESSOR**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 256 days.

(21) Appl. No.: **17/579,871**

(22) Filed: **Jan. 20, 2022**

Related U.S. Application Data

(63) Continuation-in-part of application No. 17/375,724, filed on Jul. 14, 2021, now Pat. No. 11,863,221.
(Continued)

(51) **Int. Cl.**
H04L 27/38 (2006.01)

(52) **U.S. Cl.**
CPC ***H04L 27/38*** (2013.01)

(58) **Field of Classification Search**
CPC H04L 27/38; G06F 2218/04; G06N 3/084
See application file for complete search history.

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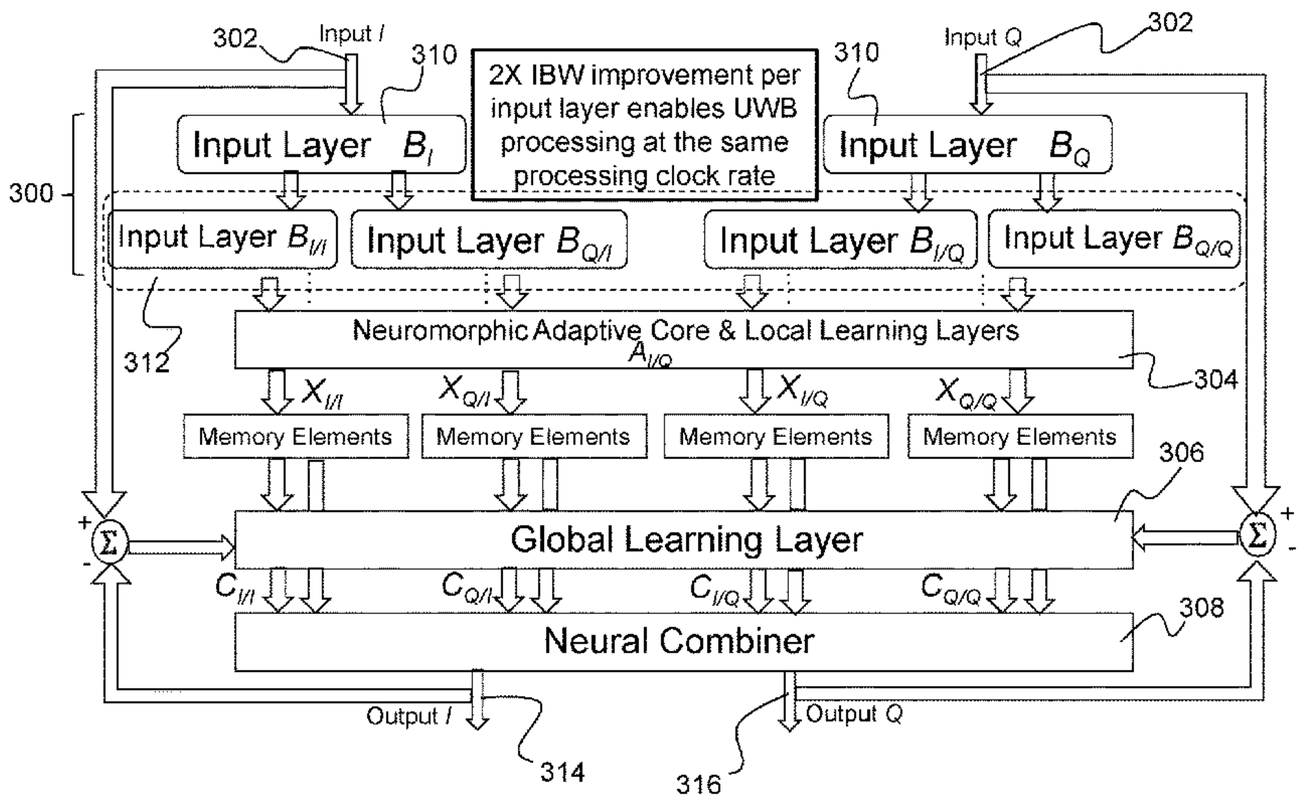
(57) **ABSTRACT**

Described is a system for Neuromorphic Adaptive Core (NeurACore) signal processor for ultra-wide instantaneous bandwidth denoising of a noisy signal. The NeurACore signal processor includes a digital signal pre-processing unit for performing cascaded decomposition of a wideband complex valued In-phase and Quadrature-phase (I/Q) input signal in real time. The wideband complex valued I/Q input signal is decomposed into I and Q sub-channels. The NeurACore signal processor further includes a NeurACore and local learning layers for performing high-dimensional projection of the wideband complex valued I/Q input signal into a high-dimensional state space; a global learning layer for performing a gradient descent online learning algorithm; and a neural combiner for combining outputs of the global learning layer to compute signal predictions corresponding to the wideband complex valued I/Q input signal.

16 Claims, 16 Drawing Sheets



Related U.S. Application Data

(60) Provisional application No. 63/150,024, filed on Feb. 16, 2021, provisional application No. 63/051,877, filed on Jul. 14, 2020, provisional application No. 63/051,851, filed on Jul. 14, 2020.

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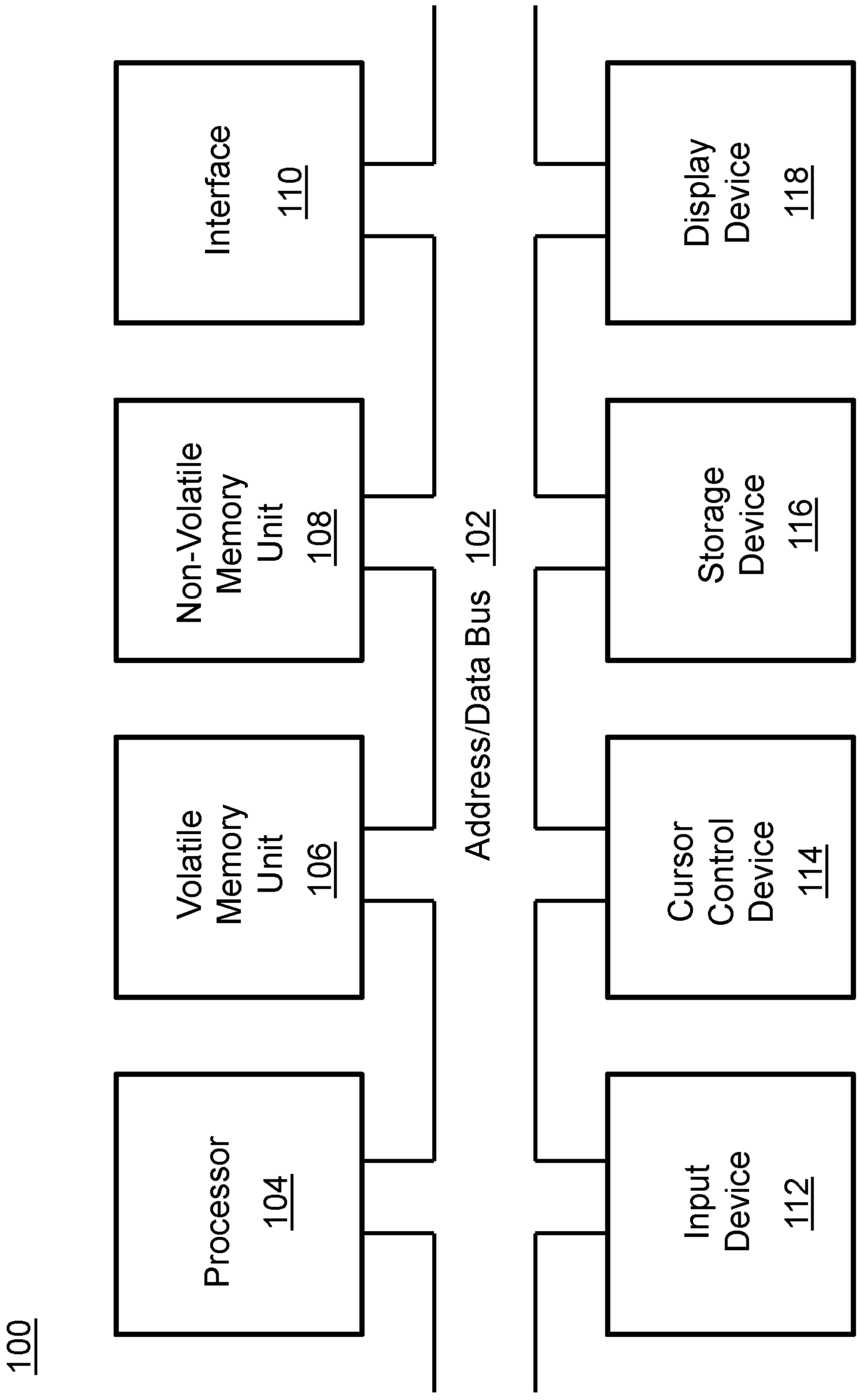

100
Processor 104
Volatile Memory Unit 106
Non-Volatile Memory Unit 108
Interface 110
Address/Data Bus 102
Input Device 112
Cursor Control Device 114
Storage Device 116
Display Device 118

FIG. 1

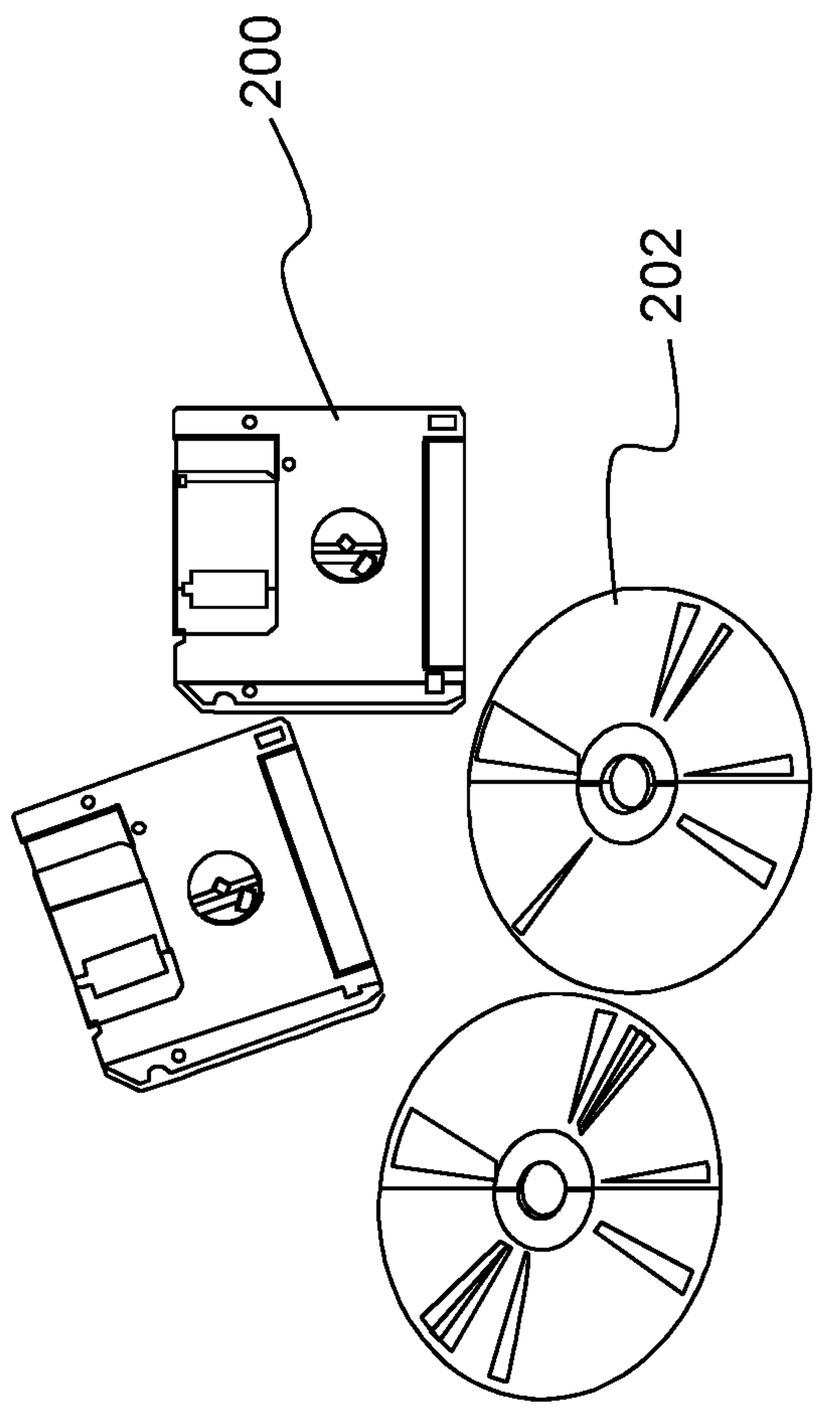


FIG. 2

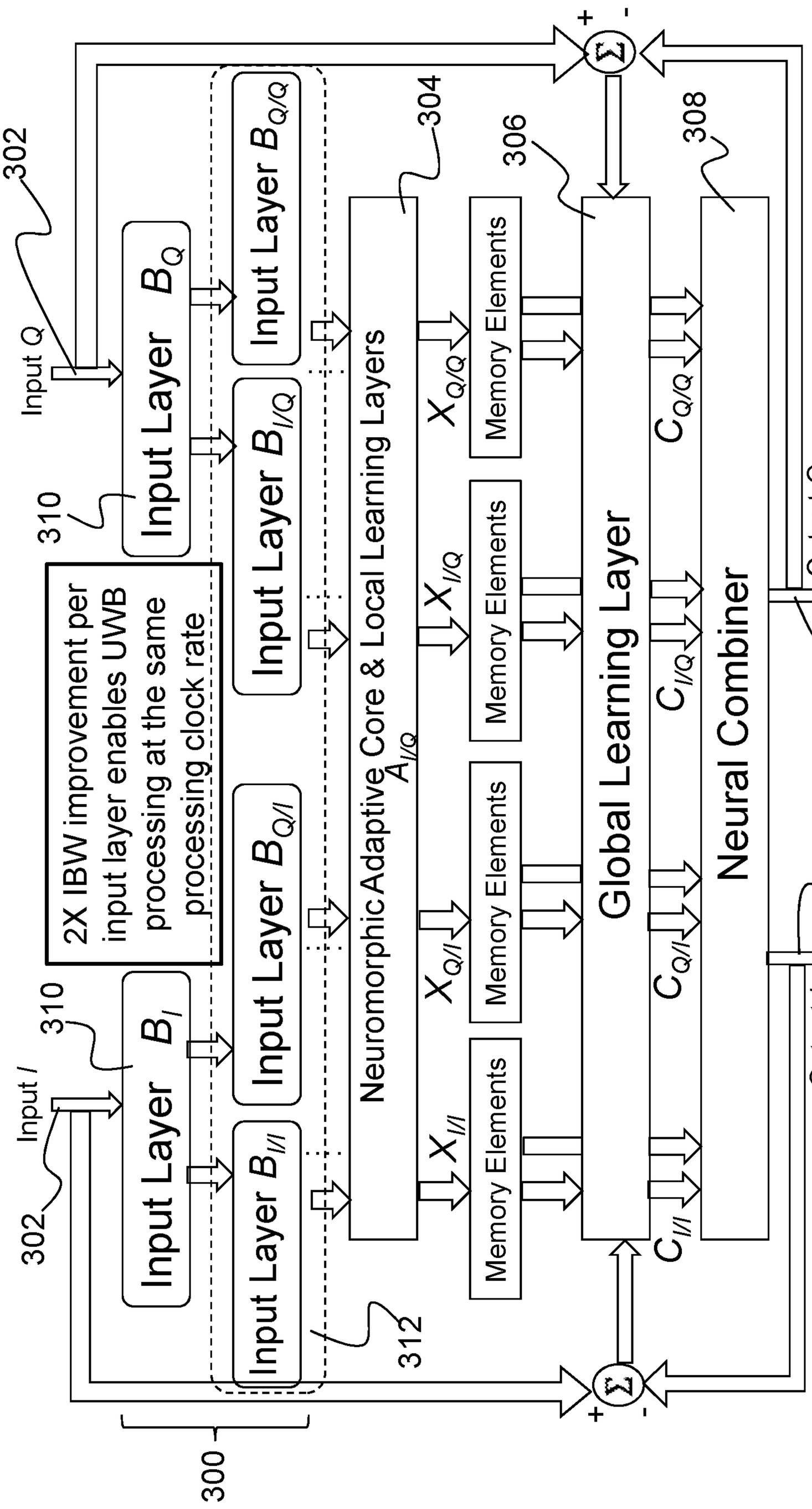

Input Q
Input I
302
Input Layer B_Q
Input Layer B_I
Input Layer $B_{Q/Q}$
Input Layer $B_{I/Q}$
Input Layer $B_{Q/I}$
Input Layer $B_{I/I}$
310
2X IBW improvement per input layer enables UWB processing at the same processing clock rate
304
Neuromorphic Adaptive Core & Local Learning Layers
306
Memory Elements
$X_{Q/Q}$
$X_{I/Q}$
$X_{Q/I}$
$X_{I/I}$
$A_{I/Q}$
308
Global Learning Layer
$C_{Q/Q}$
$C_{I/Q}$
$C_{Q/I}$
$C_{I/I}$
Neural Combiner
Output Q
Output I
314
316
312
300
Σ
+
-

FIG. 3

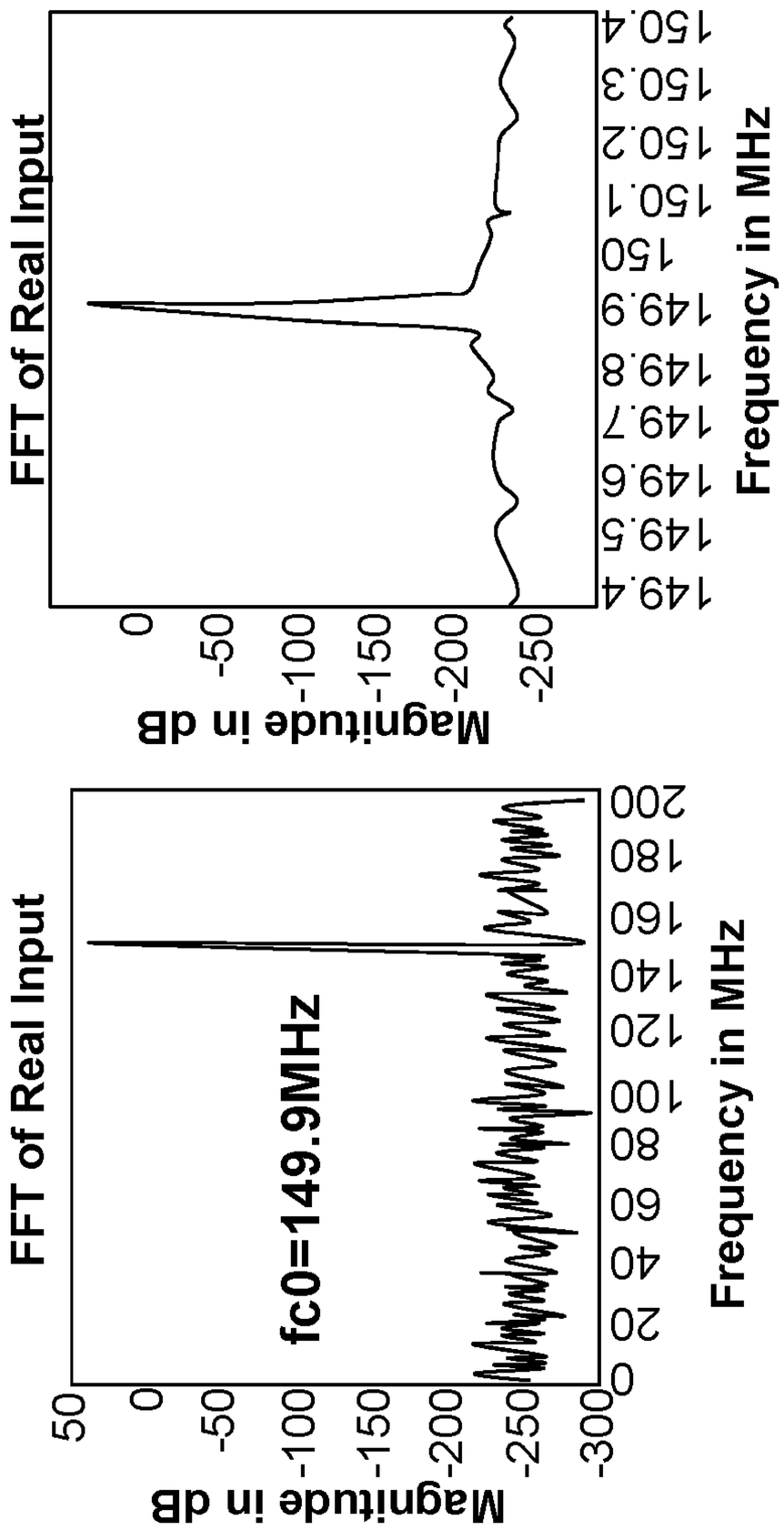

FFT of Real Input
Frequency in MHz
150.4
150.3
150.2
150.1
150
149.9
149.8
149.7
149.6
149.5
149.4
FFT of Real Input
fc0=149.9MHz
Magnitude in dB
Frequency in MHz
50
0
-50
-100
-150
-200
-250
-300
0
20
40
60
80
100
120
140
160
180
200
Real Valued Wideband Input Data
CH=1
fs=400MHz
BW=[0 200] MHz
First Level I/Q Decomposition
CH=2
fs=200MHz
BW=[-100 100] MHz
Second Level I/Q Decomposition
CH=4
fs=100MHz
BW=[-50 50] MHz

FIG. 4A

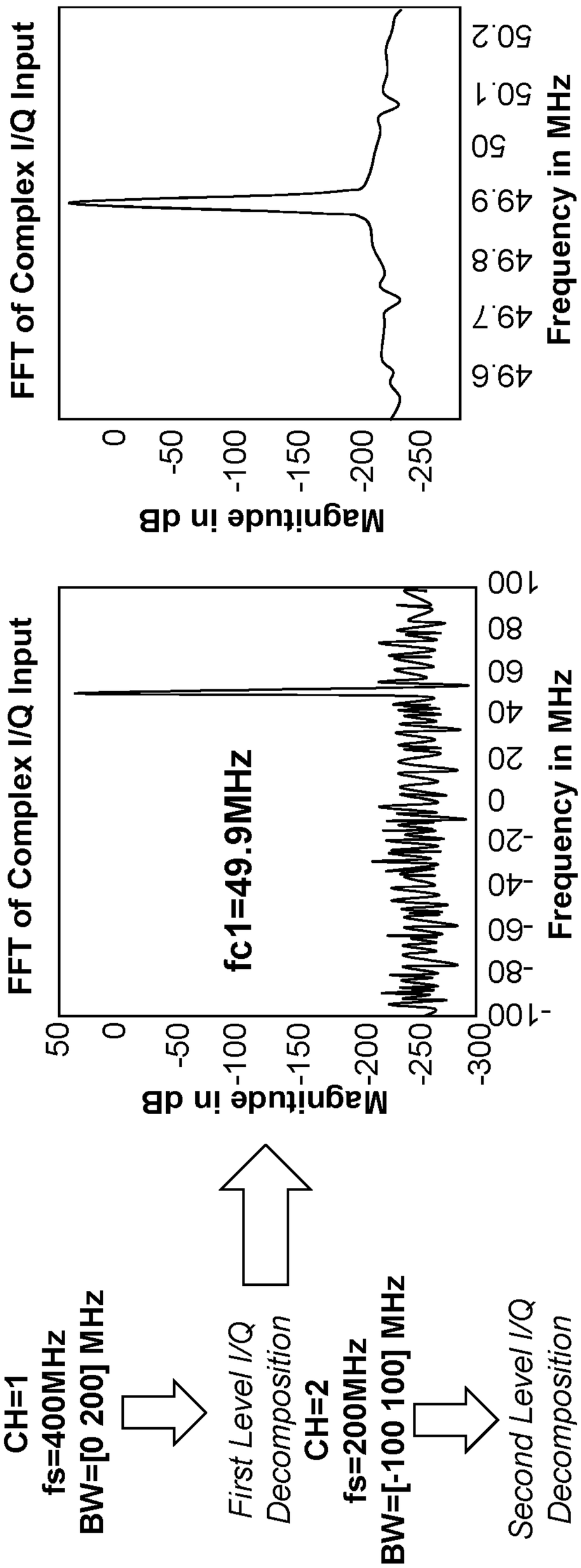

Real Valued
Wideband Input
Data
CH=1
fs=400MHz
BW=[0 200] MHz
First Level I/Q
Decomposition
CH=2
fs=200MHz
BW=[-100 100] MHz
Second Level I/Q
Decomposition
CH=4
fs=100MHz
BW=[-50 50] MHz
FFT of Complex I/Q Input
fc1=49.9MHz
Magnitude in dB
Frequency in MHz
FFT of Complex I/Q Input
Magnitude in dB
Frequency in MHz

FIG. 4B

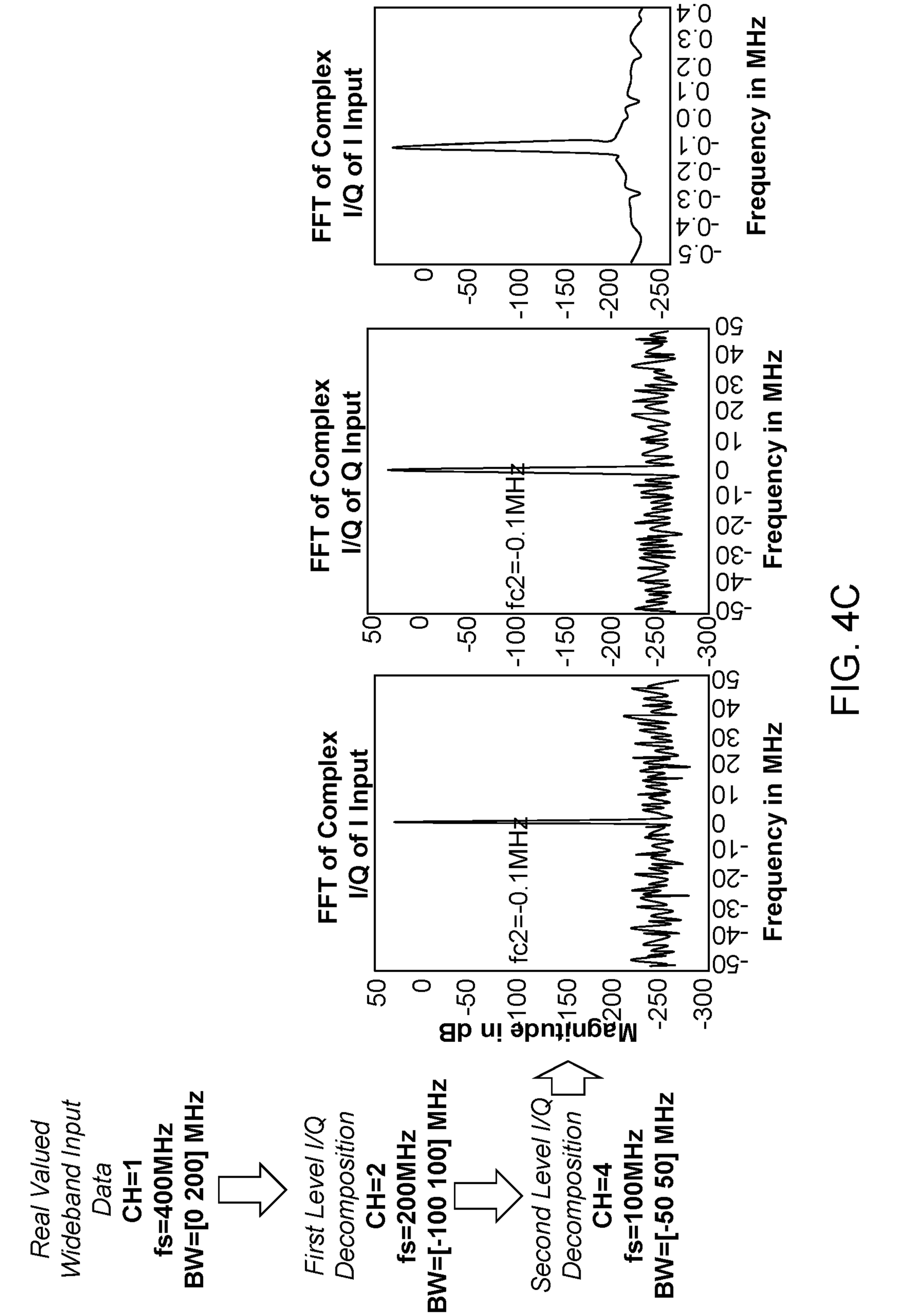
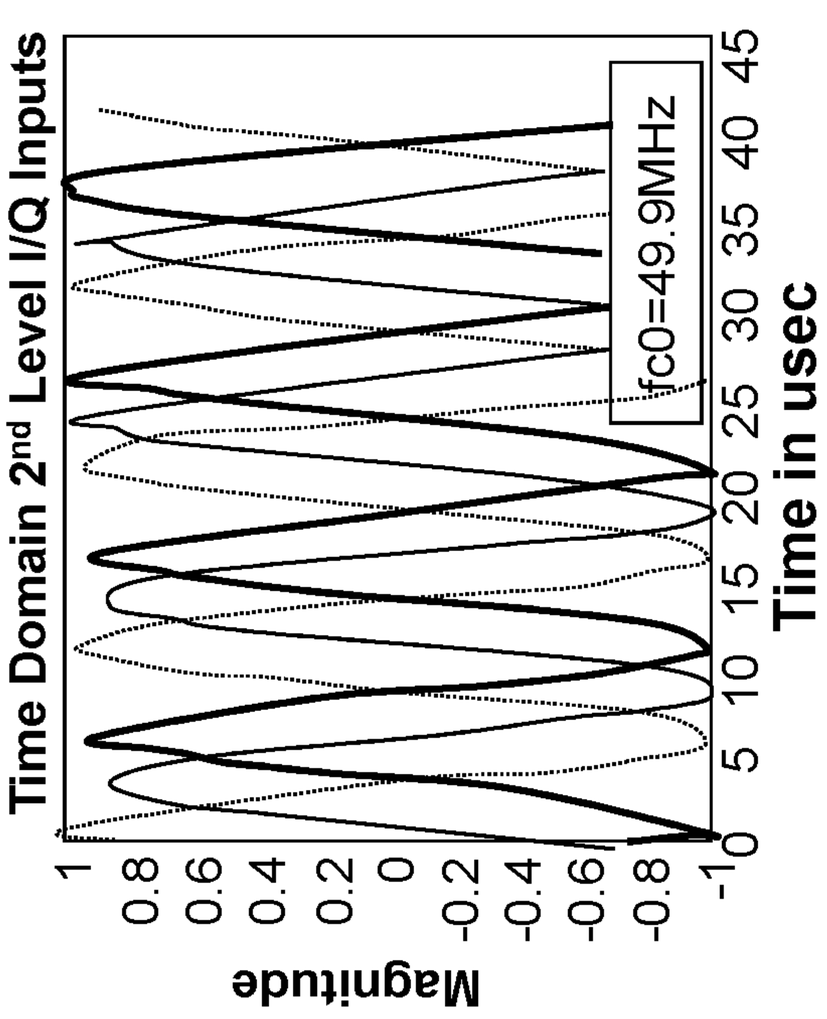

Real Valued
Wideband Input
Data
CH=1
fs=400MHz
BW=[0 200] MHz
First Level I/Q
Decomposition
CH=2
fs=200MHz
BW=[-100 100] MHz
Second Level I/Q
Decomposition
CH=4
fs=100MHz
BW=[-50 50] MHz
FFT of Complex
I/Q of I Input
FFT of Complex
I/Q of Q Input
FFT of Complex
I/Q of I Input
FFT of Complex
I/Q of Q Input
fc2=-0.1MHz
fc2=-0.1MHz
Magnitude in dB
Frequency in MHz
Frequency in MHz
Frequency in MHz
Frequency in MHz

FIG. 4C

FIG. 5A



Real Valued Wideband Input Data
fc0=49.9 MHz
fc0=50.1 MHz
fc0=149.9 MHz
fc0=150.1 MHz
fs=400 MHz
BW=[0 200] MHz

All four frequencies translate into the same 2nd level baseband frequency |fc2|=0.1 MHz

FIG. 5B

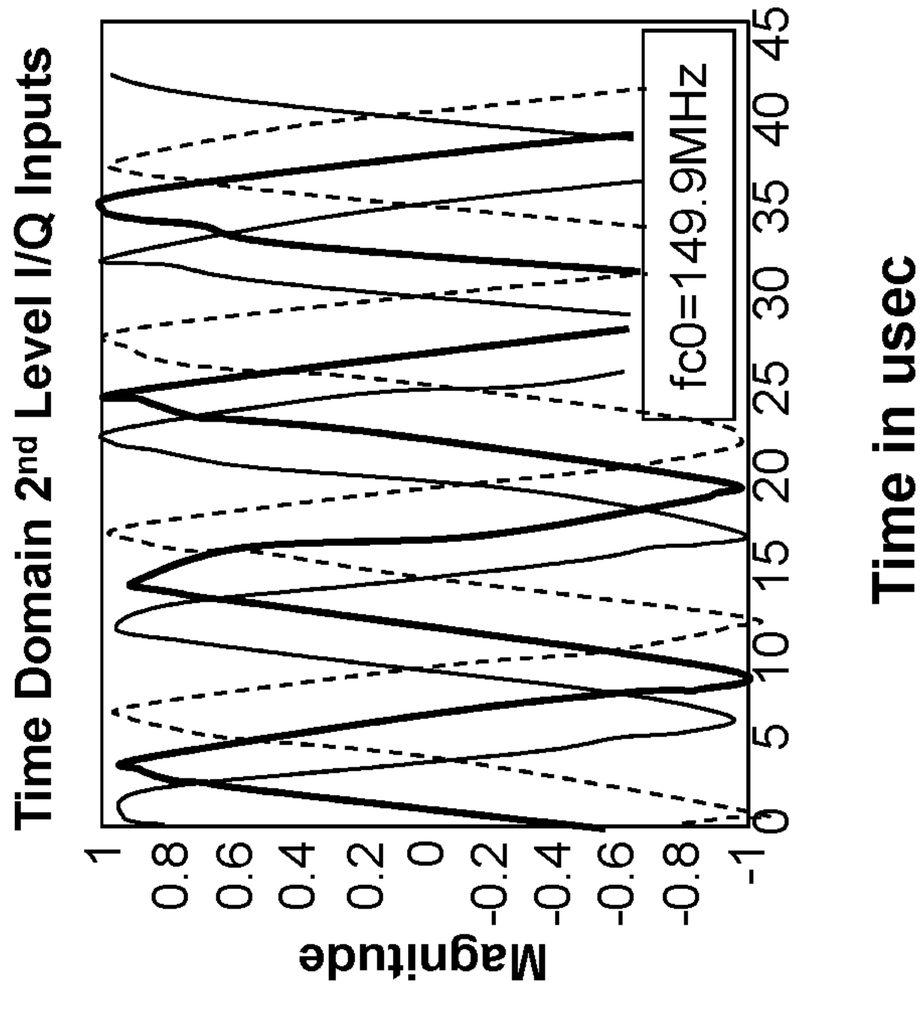
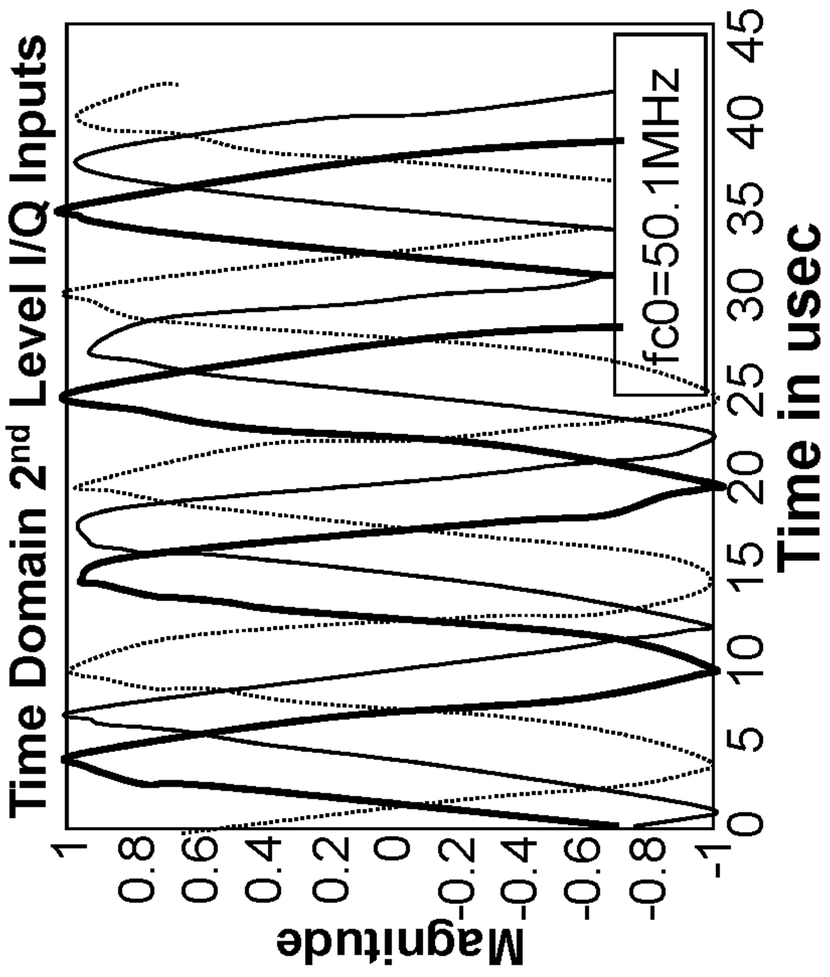


FIG. 5C



Real Valued Wideband Input Data
fc0=49.9 MHz
fc0=50.1 MHz
fc0=149.9 MHz
fc0=150.1 MHz
fs=400 MHz
BW=[0 200] MHz

All four frequencies translate into the same 2nd level baseband frequency |fc2|=0.1 MHz

FIG. 5D

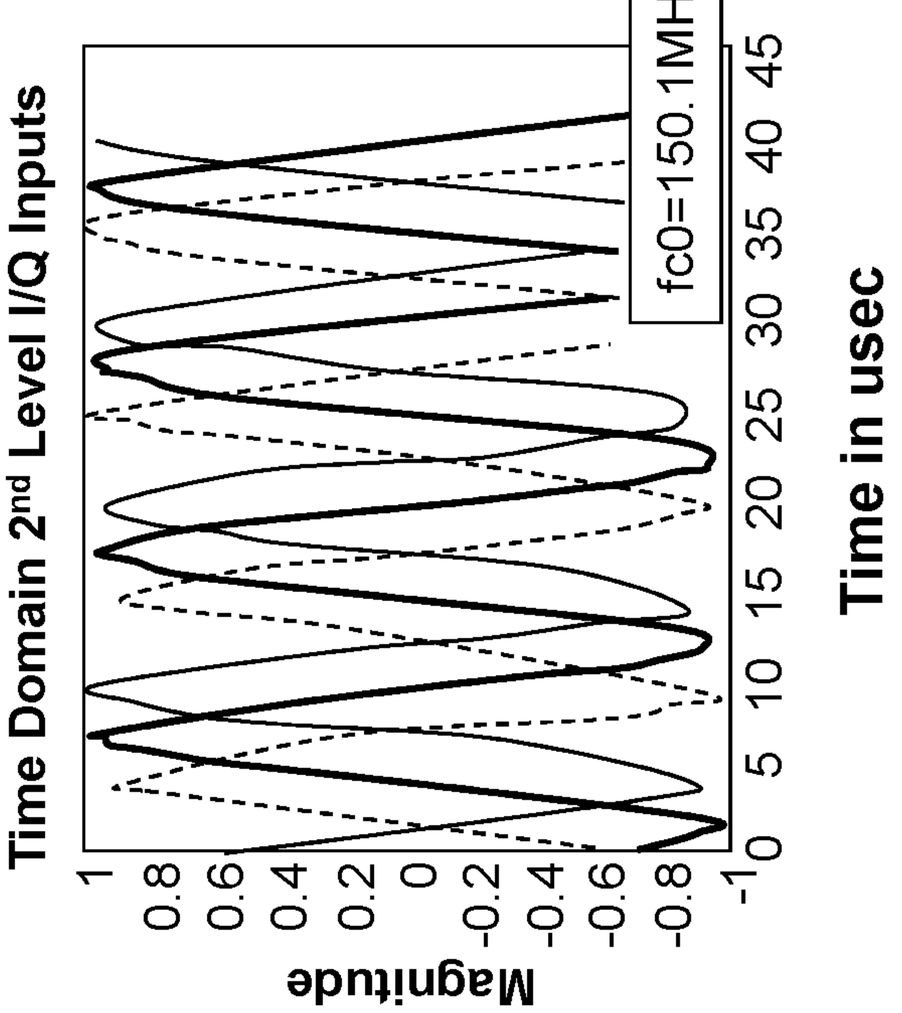


FIG. 6A

$$\begin{bmatrix} \dot{x}_{II} \\ \dot{x}_{IQ} \\ \dot{x}_{QI} \\ \dot{x}_{QQ} \end{bmatrix} = \frac{\omega_0}{2} \begin{bmatrix} \begin{bmatrix} -\frac{3}{Q_0} & -1 \\ 1 & -\frac{3}{Q_0} \end{bmatrix} \begin{bmatrix} 1 & -\frac{1}{Q_0} \\ -\frac{1}{Q_0} & 1 \end{bmatrix} \\ \begin{bmatrix} -1 & -\frac{1}{Q_0} \\ \frac{1}{Q_0} & -1 \end{bmatrix} \begin{bmatrix} -\frac{3}{Q_0} & -1 \\ 1 & -\frac{3}{Q_0} \end{bmatrix} \end{bmatrix} \begin{bmatrix} x_{II} \\ x_{IQ} \\ x_{QI} \\ x_{QQ} \end{bmatrix}$$

FIG. 6B

$$\begin{bmatrix} \dot{x}_{II} \\ \dot{x}_{IQ} \\ \dot{x}_{QI} \\ \dot{x}_{QQ} \end{bmatrix} = \frac{\omega_0}{2} \begin{bmatrix} \begin{bmatrix} -\frac{3}{Q_0} & 1 \\ -1 & -\frac{3}{Q_0} \end{bmatrix} \begin{bmatrix} -1 & \frac{1}{Q_0} \\ -\frac{1}{Q_0} & -1 \end{bmatrix} \\ \begin{bmatrix} 1 & -\frac{1}{Q_0} \\ \frac{1}{Q_0} & 1 \end{bmatrix} \begin{bmatrix} -\frac{3}{Q_0} & 1 \\ -1 & -\frac{3}{Q_0} \end{bmatrix} \end{bmatrix} \begin{bmatrix} x_{II} \\ x_{IQ} \\ x_{QI} \\ x_{QQ} \end{bmatrix}$$

FIG. 6C

$$\begin{bmatrix} \dot{x}_{II} \\ \dot{x}_{IQ} \\ \dot{x}_{QI} \\ \dot{x}_{QQ} \end{bmatrix} = \frac{\omega_0}{2} \begin{bmatrix} \begin{bmatrix} -\frac{3}{Q_0} & 1 \\ -1 & -\frac{3}{Q_0} \end{bmatrix} \begin{bmatrix} 1 & -\frac{1}{Q_0} \\ \frac{1}{Q_0} & 1 \end{bmatrix} \\ \begin{bmatrix} -1 & \frac{1}{Q_0} \\ -\frac{1}{Q_0} & -1 \end{bmatrix} \begin{bmatrix} -\frac{3}{Q_0} & 1 \\ -1 & -\frac{3}{Q_0} \end{bmatrix} \end{bmatrix} \begin{bmatrix} x_{II} \\ x_{IQ} \\ x_{QI} \\ x_{QQ} \end{bmatrix}$$

FIG. 6D

$$\begin{bmatrix} \dot{x}_{II} \\ \dot{x}_{IQ} \\ \dot{x}_{QI} \\ \dot{x}_{QQ} \end{bmatrix} = \frac{\omega_0}{2} \begin{bmatrix} \begin{bmatrix} -\frac{3}{Q_0} & -1 \\ 1 & -\frac{3}{Q_0} \end{bmatrix} \begin{bmatrix} -1 & -\frac{1}{Q_0} \\ \frac{1}{Q_0} & -1 \end{bmatrix} \\ \begin{bmatrix} 1 & \frac{1}{Q_0} \\ -\frac{1}{Q_0} & 1 \end{bmatrix} \begin{bmatrix} -\frac{3}{Q_0} & -1 \\ 1 & -\frac{3}{Q_0} \end{bmatrix} \end{bmatrix} \begin{bmatrix} x_{II} \\ x_{IQ} \\ x_{QI} \\ x_{QQ} \end{bmatrix}$$

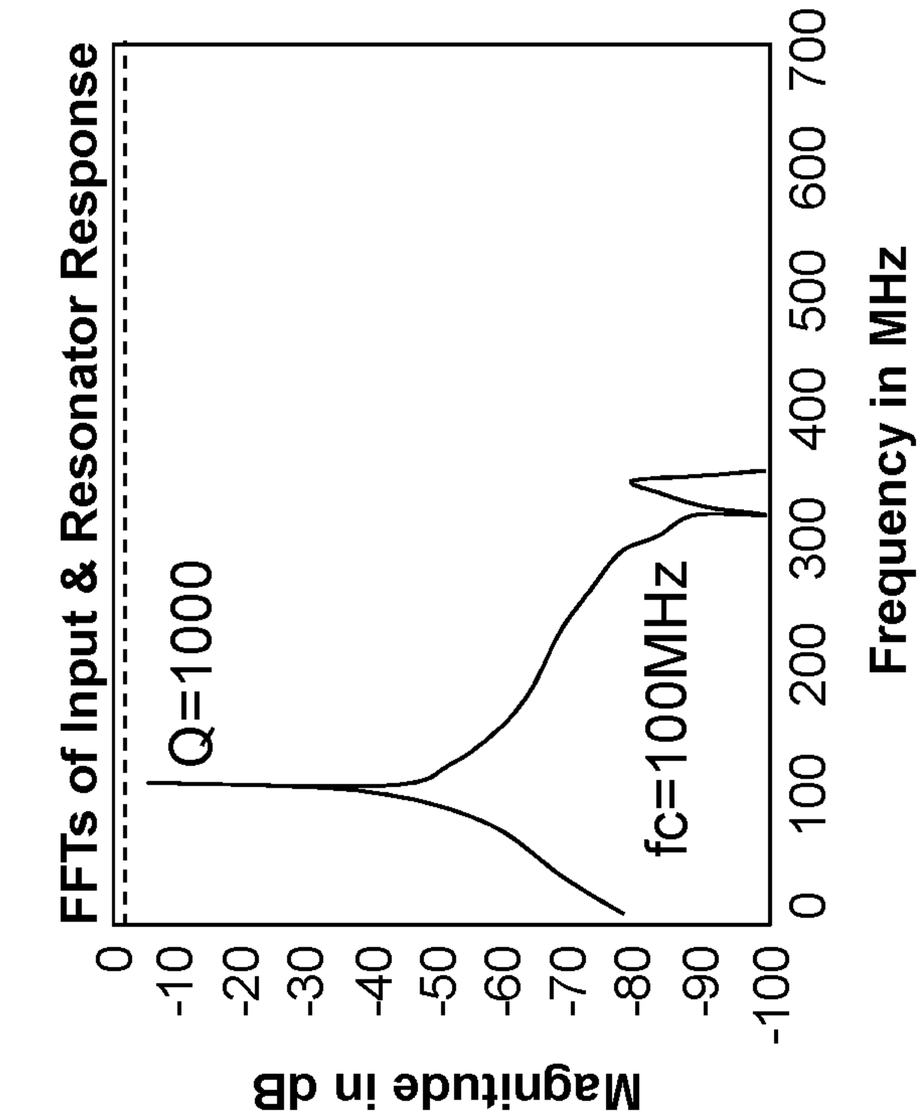

FFTs of Input & Resonator Response
Magnitude in dB
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
Q=1000
fc=100MHz
0
100
200
300
400
500
600
700
Frequency in MHz

FIG. 7B

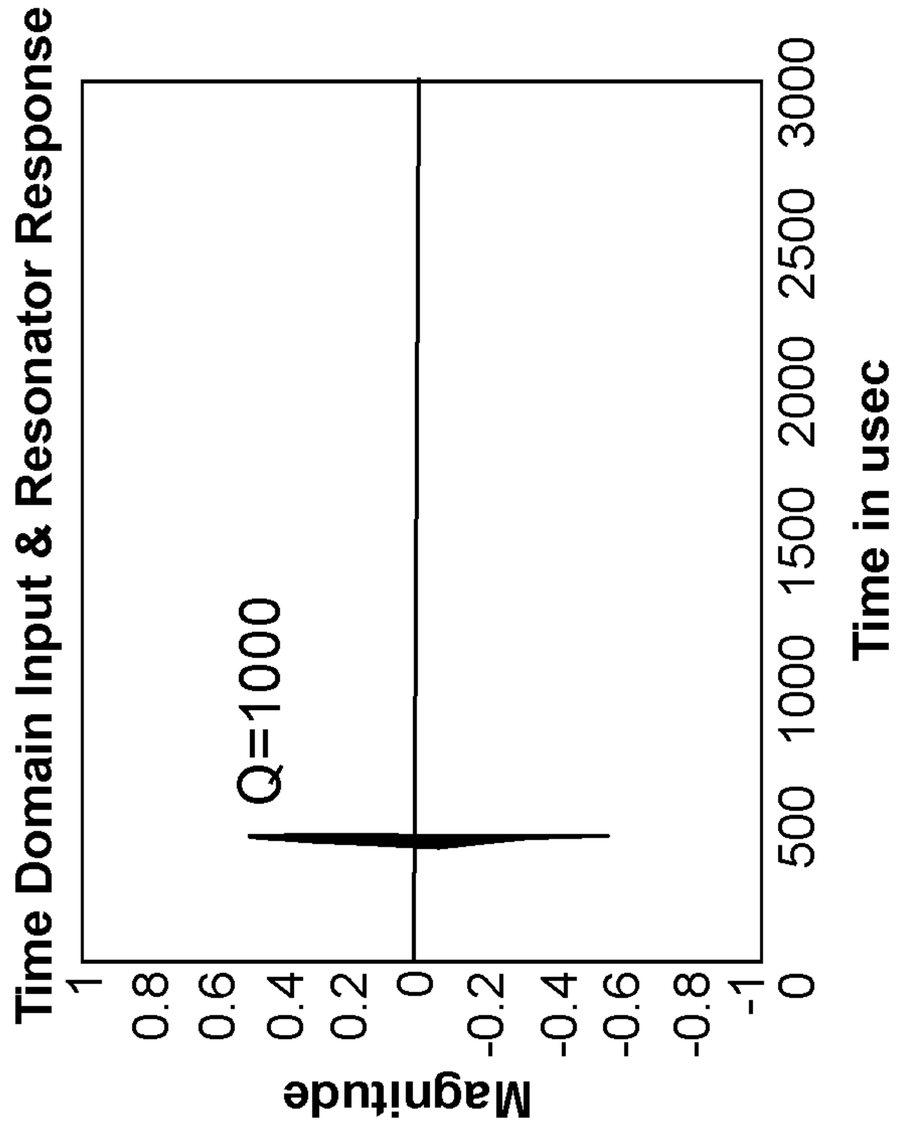

Time Domain Input & Resonator Response
Magnitude
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
Q=1000
0
500
1000
1500
2000
2500
3000
Time in usec

FIG. 7A

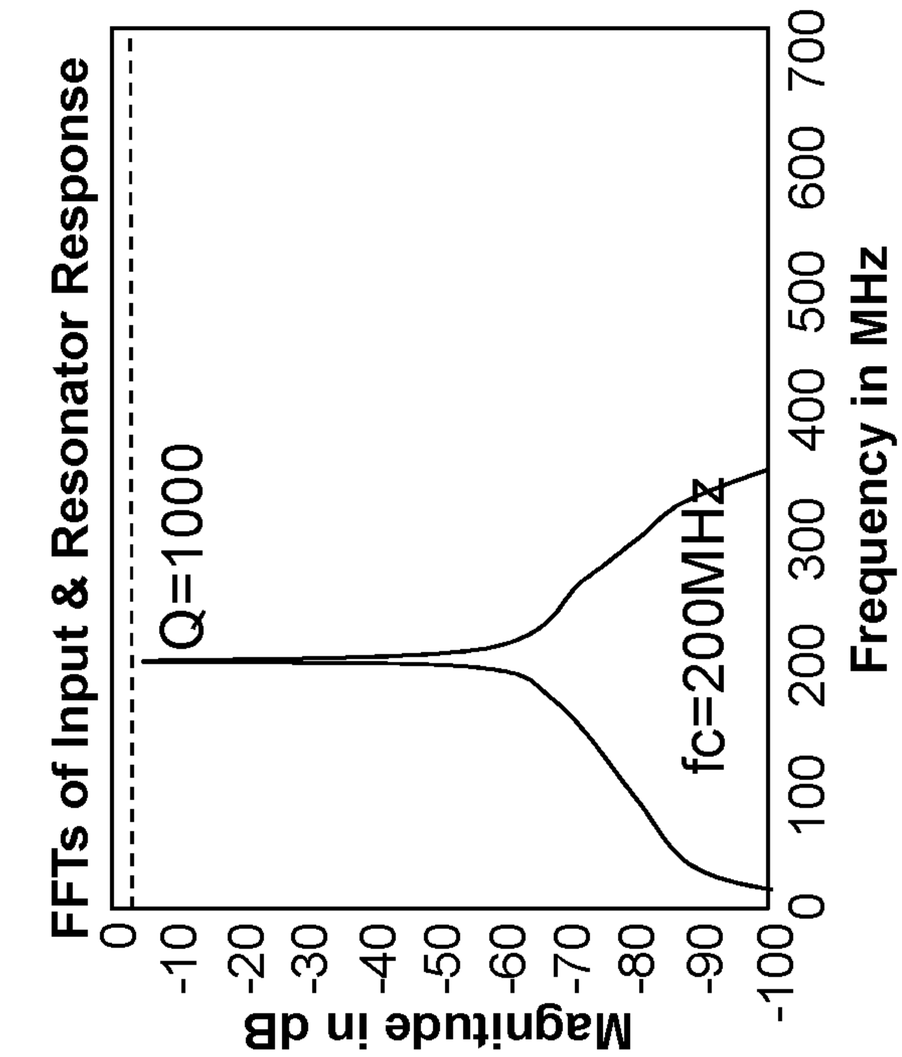

FFTs of Input & Resonator Response
Magnitude in dB
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
100
200
300
400
500
600
700
Frequency in MHz
Q=1000
fc=200MHz

FIG. 7D

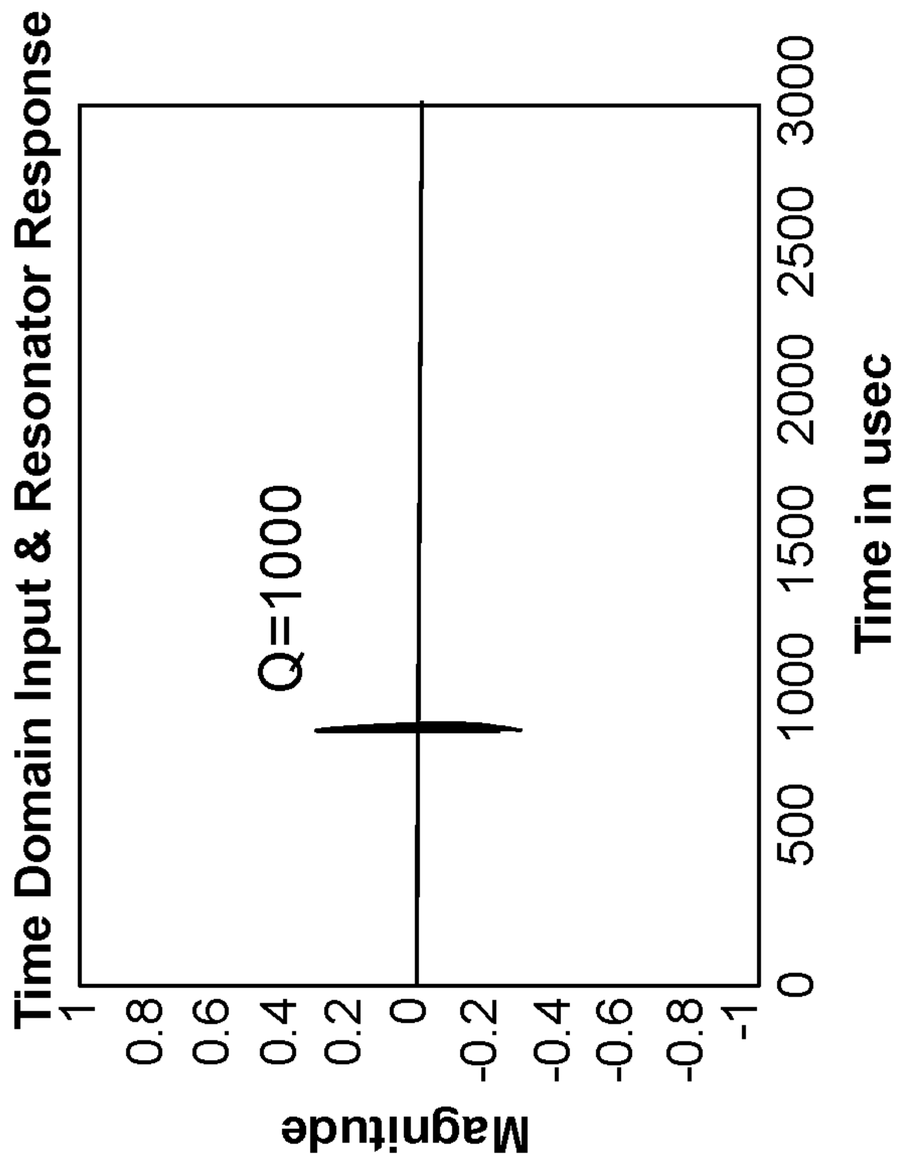

Time Domain Input & Resonator Response
Magnitude
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
500
1000
1500
2000
2500
3000
Time in usec
Q=1000

FIG. 7C

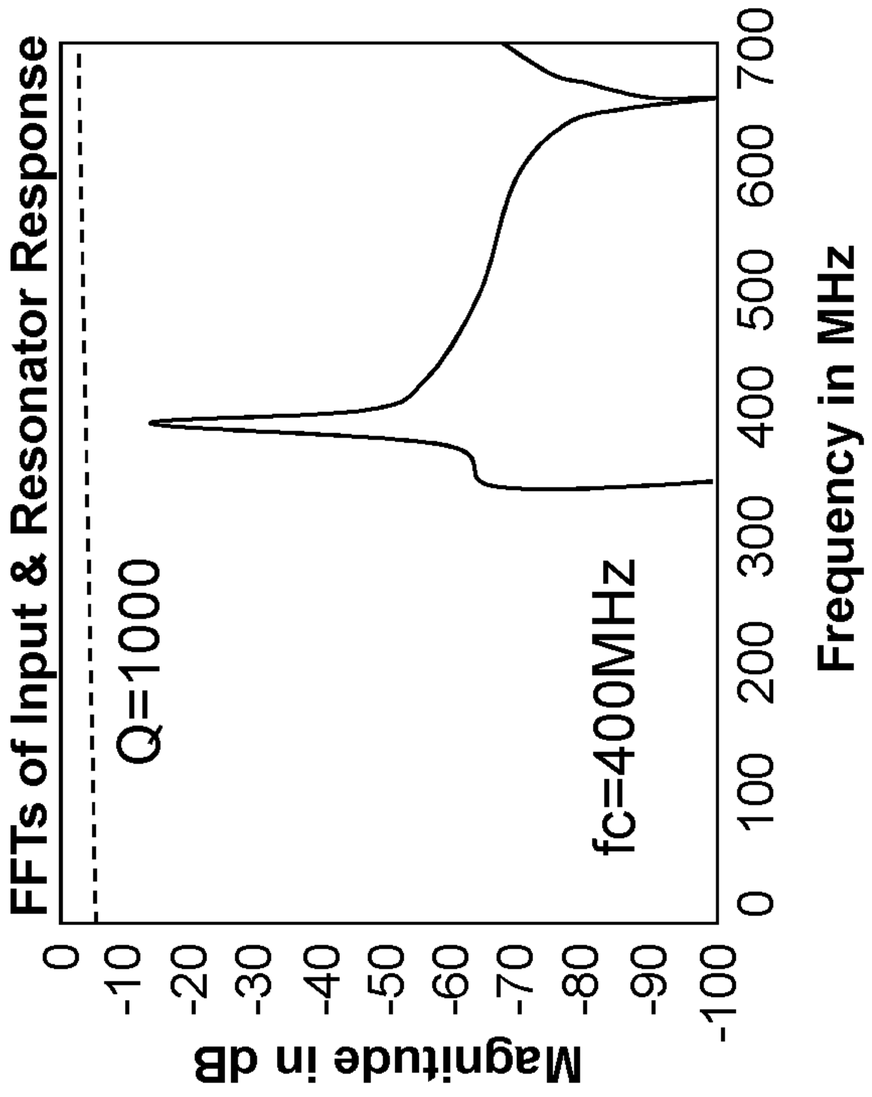

FFTs of Input & Resonator Response
Q=1000
fc=400MHz
Magnitude in dB
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
100
200
300
400
500
600
700
Frequency in MHz

FIG. 7F

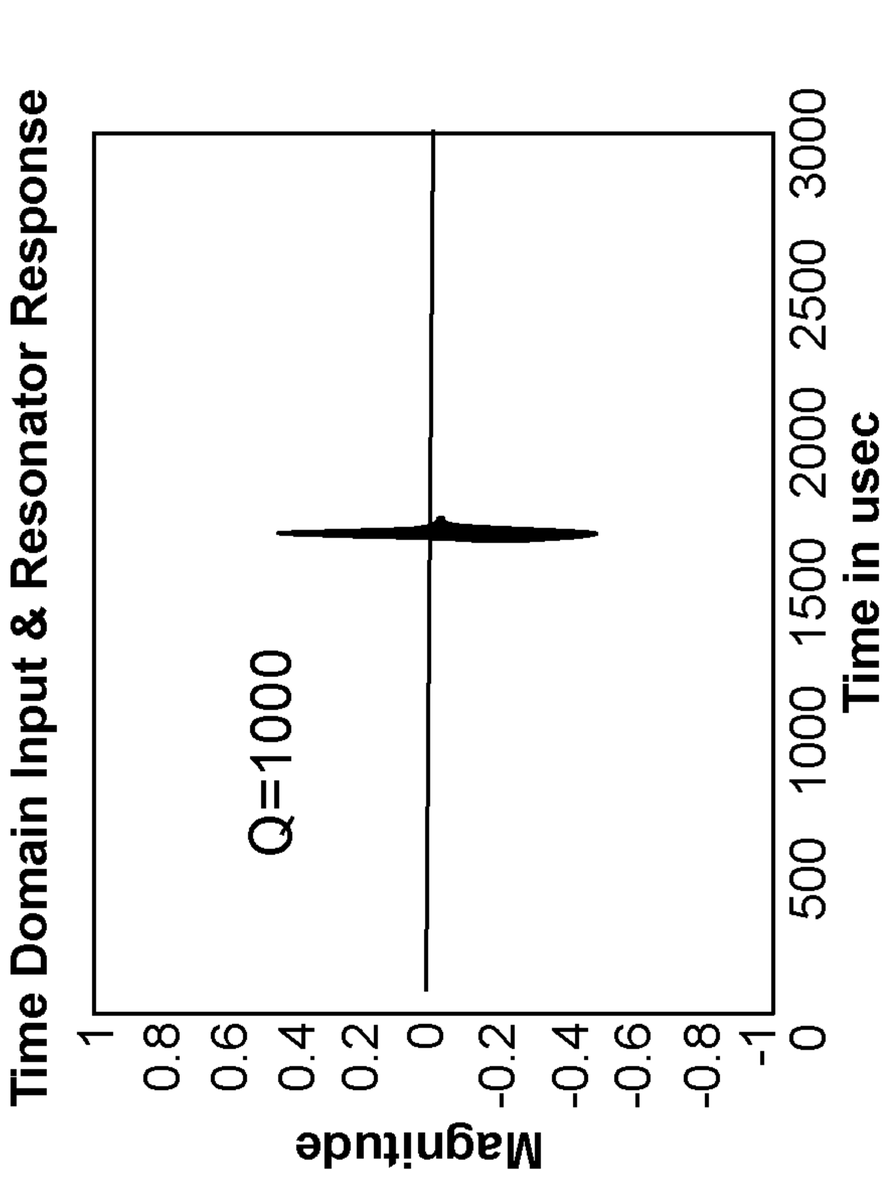

Time Domain Input & Resonator Response
Q=1000
Magnitude
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
500
1000
1500
2000
2500
3000
Time in usec

FIG. 7E

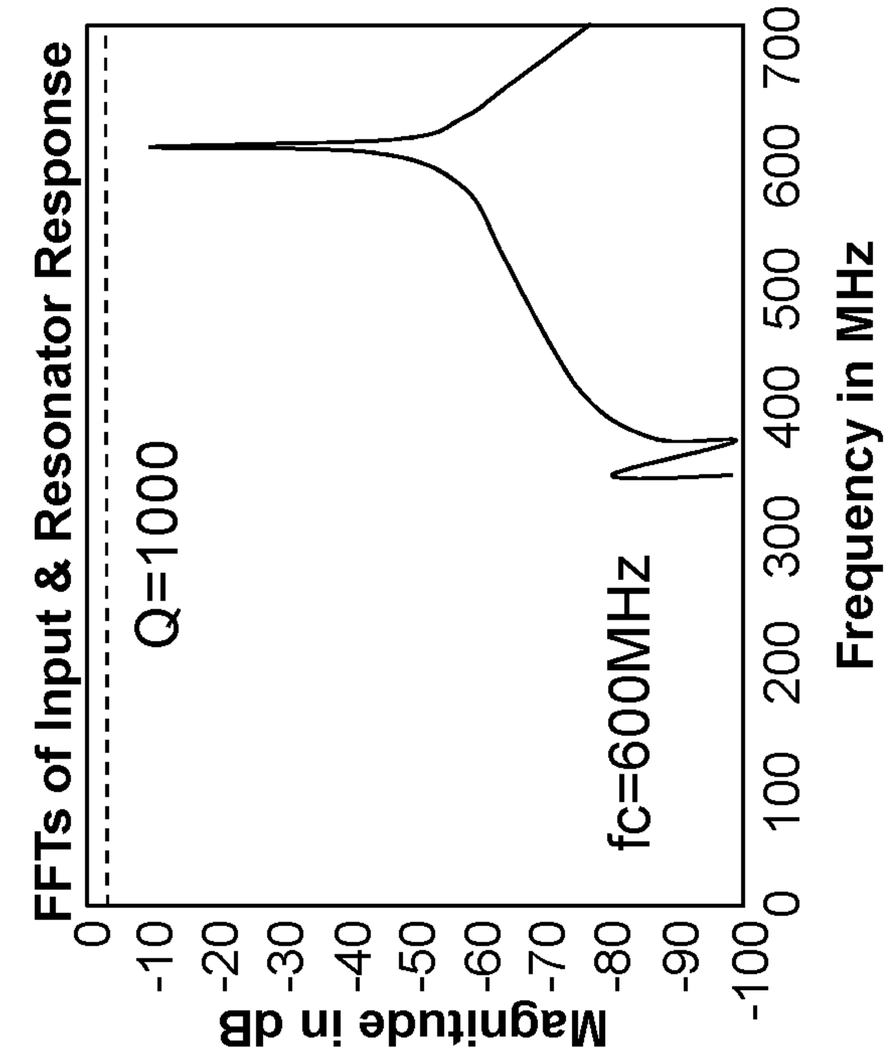

FFTs of Input & Resonator Response
Q=1000
fc=600MHz
Magnitude in dB
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
100
200
300
400
500
600
700
Frequency in MHz

FIG. 7H

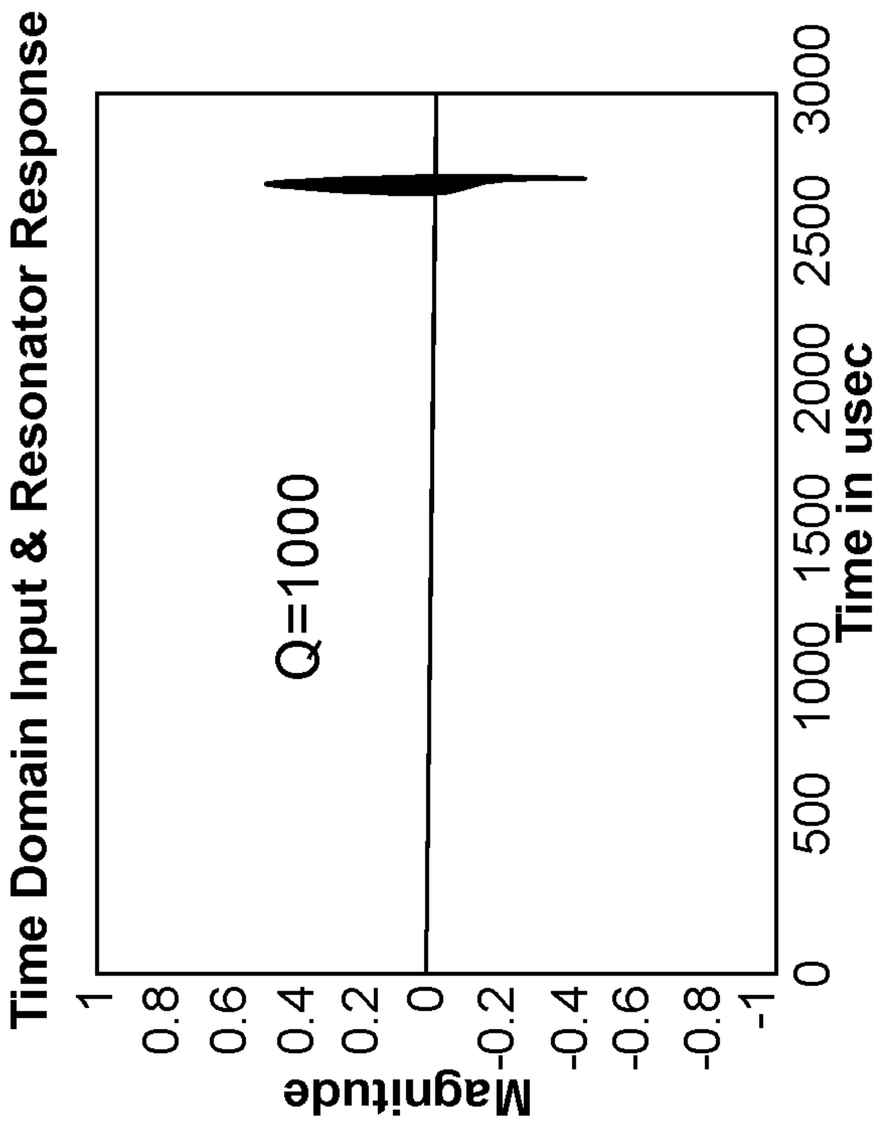

Time Domain Input & Resonator Response
Q=1000
Magnitude
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
500
1000
1500
2000
2500
3000
Time in usec

FIG. 7G

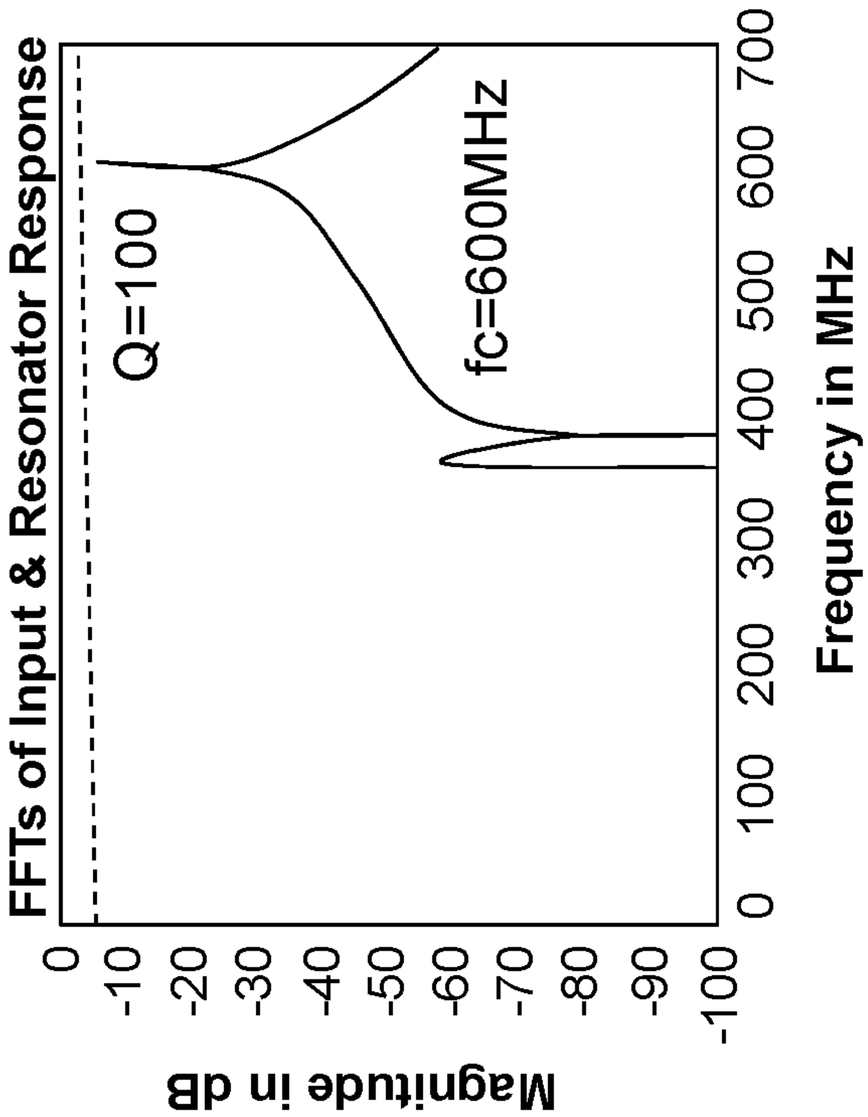

FFTs of Input & Resonator Response
Q=100
fc=600MHz
Magnitude in dB
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
100
200
300
400
500
600
700
Frequency in MHz

FIG. 8B

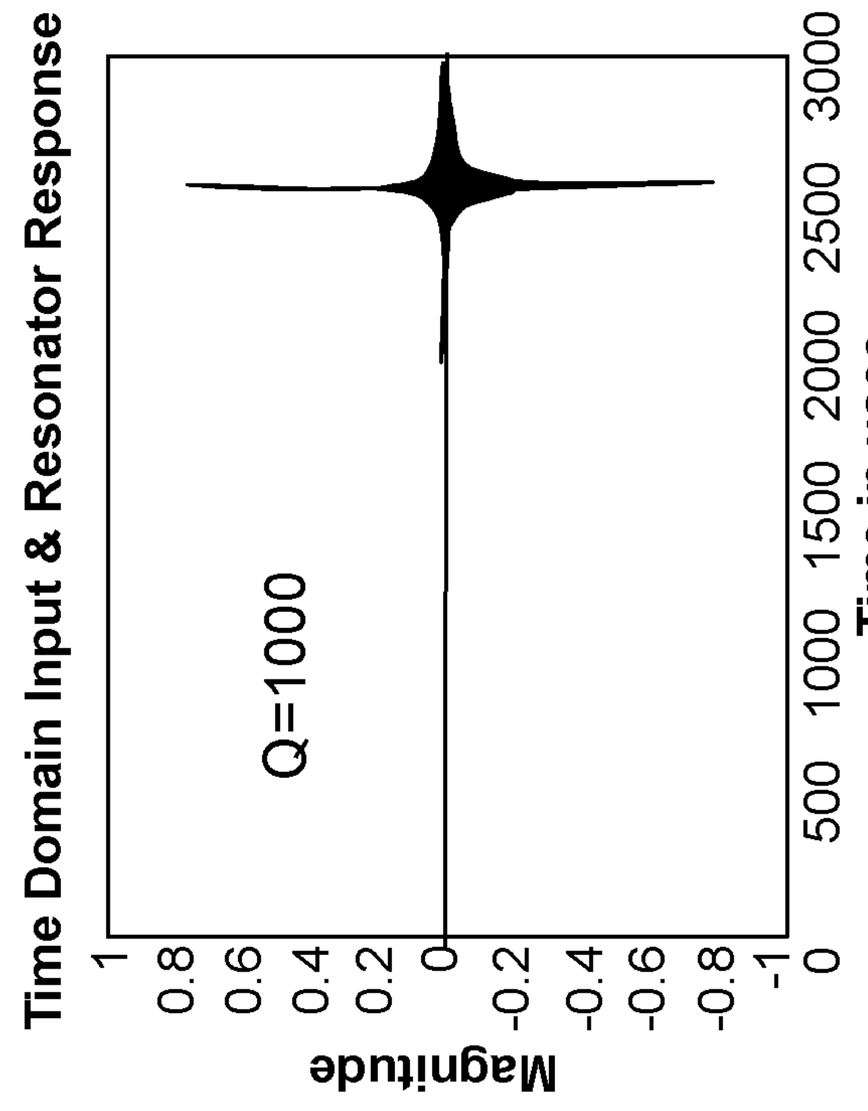

Time Domain Input & Resonator Response
Q=1000
Magnitude
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
500
1000
1500
2000
2500
3000
Time in usec

FIG. 8A

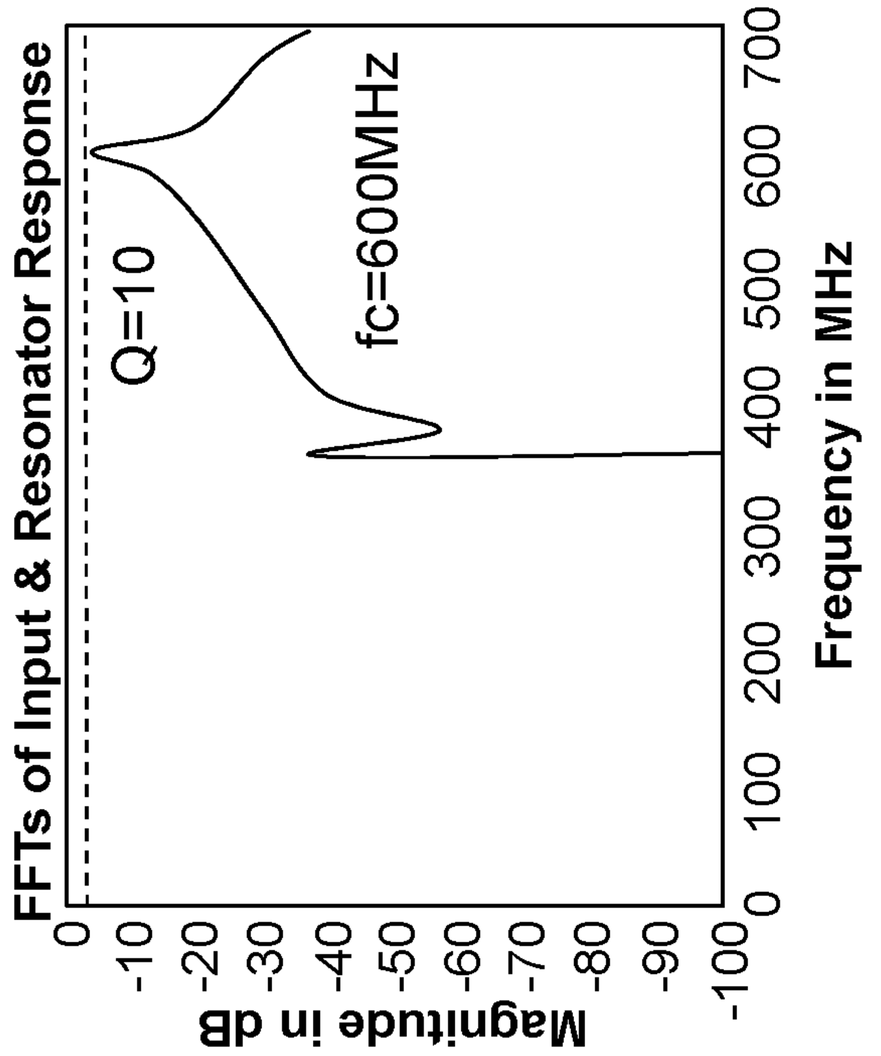

FFTs of Input & Resonator Response
Q=10
fc=600MHz
Magnitude in dB
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
100
200
300
400
500
600
700
Frequency in MHz

FIG. 8D

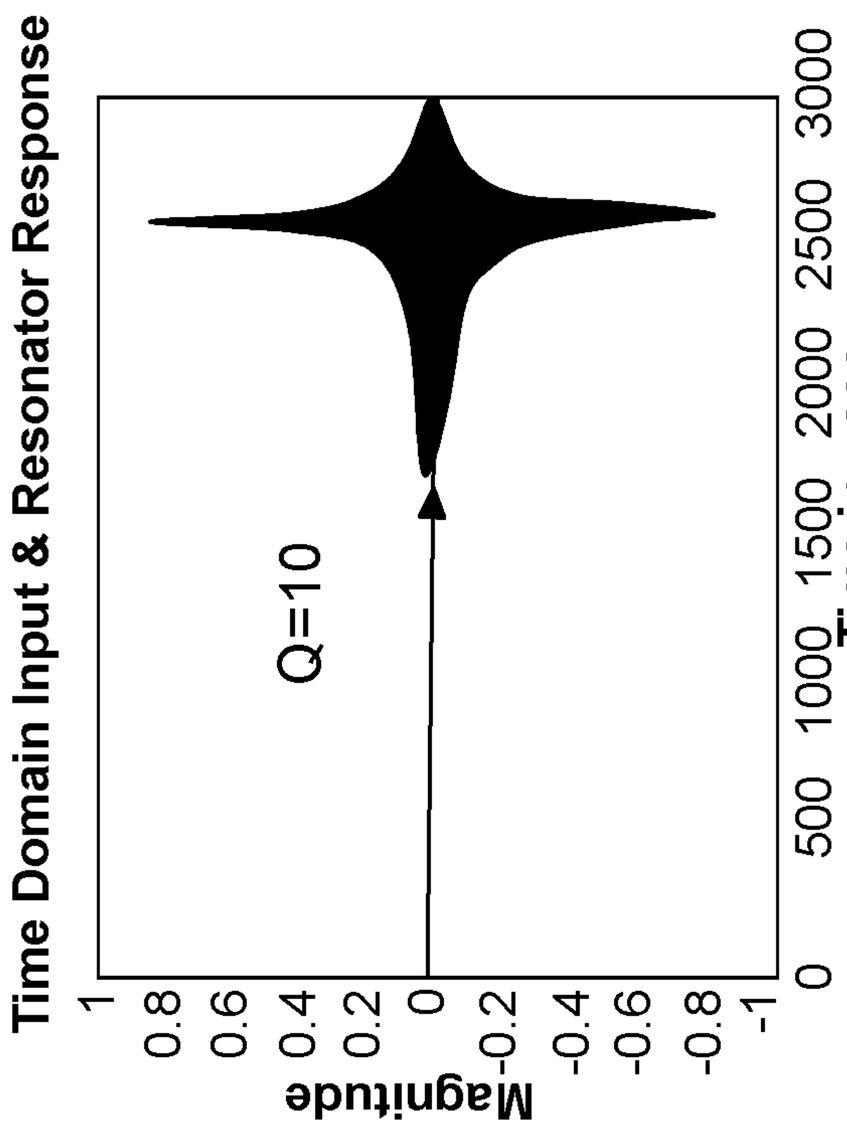

Time Domain Input & Resonator Response
Q=10
Magnitude
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
0
500
1000
1500
2000
2500
3000
Time in usec

FIG. 8C

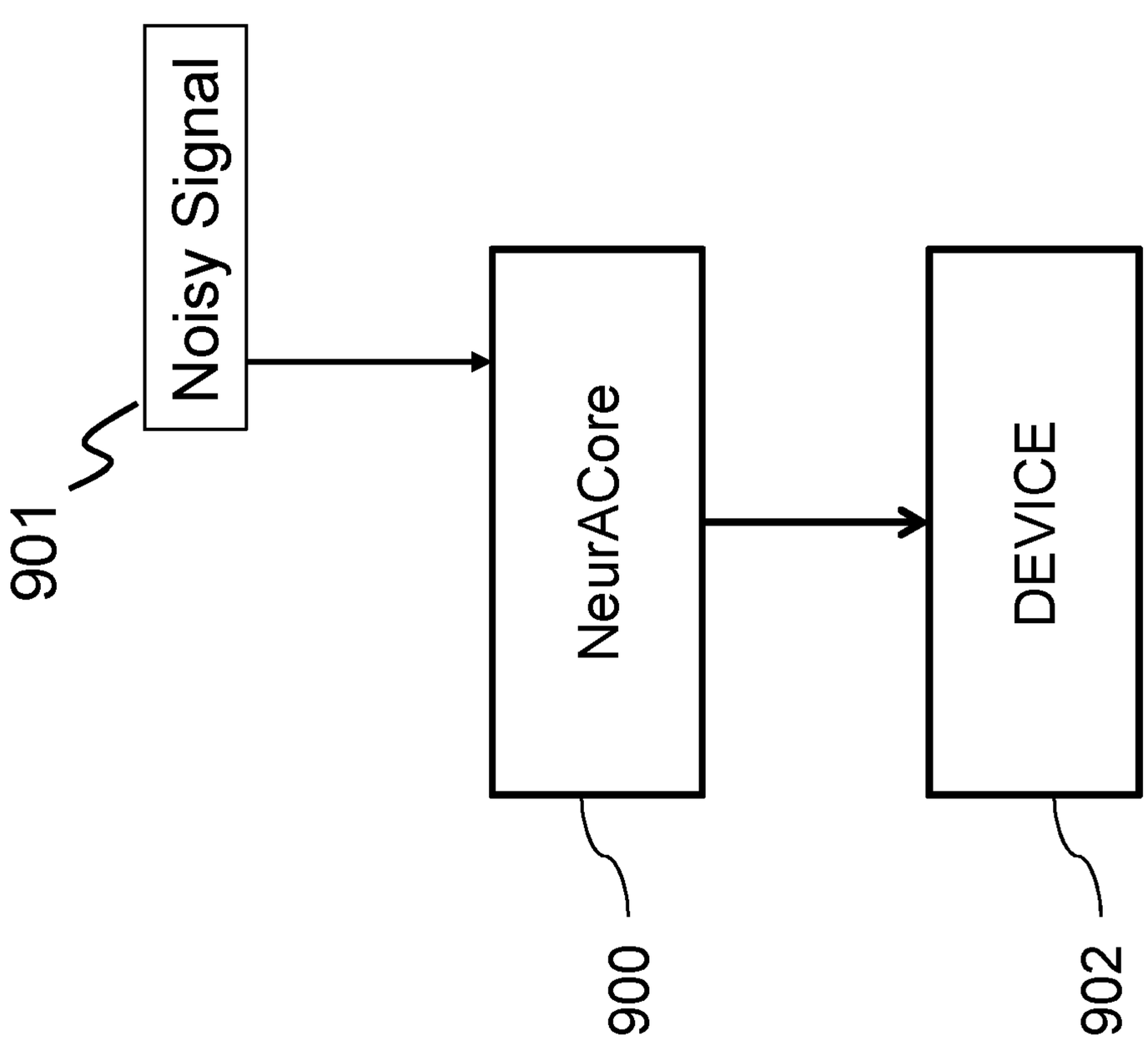


FIG. 9

ULTRA-WIDE INSTANTANEOUS BANDWIDTH COMPLEX NEUROMORPHIC ADAPTIVE CORE PROCESSOR

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a Continuation-in-Part application of U.S. application Ser. No. 17/375,724, filed in the United States on Jul. 14, 2021, entitled, "Low Size, Weight and Power (SWAP) Efficient Hardware Implementation of a Wide Instantaneous Bandwidth Neuromorphic Adaptive Core (NeurACore)", which is a Non-Provisional Application of U.S. Provisional Application No. 63/051,877, filed on Jul. 14, 2020 and U.S. Provisional Application No. 63/051,851, filed on Jul. 14, 2020, the entirety of which are hereby incorporated by reference.

This is also a Non-Provisional Application of U.S. Provisional Application No. 63/150,024, filed in the United States on Feb. 16, 2021, entitled, "Ultra-Wide Instantaneous Bandwidth Complex Neuromorphic Adaptive Core Processor," the entirety of which is incorporated herein by reference.

BACKGROUND OF INVENTION

(1) Field of Invention

The present invention relates to a signal processor and, more particularly, to a signal processor for complex signal denoising in the ultra-wide instantaneous bandwidth.

(2) Description of Related Art

Noise reduction, or denoising, is the process of removing noise from a signal. Noise reduction techniques exist for audio and images. All signal processing devices, both analog and digital, have traits that make them susceptible to noise. Noise can be random or white noise with an even frequency distribution, or frequency-dependent noise introduced by a device's mechanism or signal processing algorithms.

Current systems, such as conventional channelizers, operate over a smaller frequency band and require a large latency to achieve processing results. A channelizer is a term used for algorithms which select a certain frequency band from an input signal. The input signal typically has a higher sample rate that the sample rate of the selected channel. A channelizer is also used for algorithms that select multiple channels from an input signal in an efficient manner. Additionally, current machine learning approaches to signal processing require large quantities of online/offline training data.

Thus, a continuing need exists for a system that does not require any pre-training and enables real-time signal denoising in the ultra-wide bandwidth for both real-valued and complex input signals.

SUMMARY OF INVENTION

The present invention relates to a signal processor and, more particularly, to a Neuromorphic Adaptive Core (NeurACore) signal processor for complex signal denoising in ultra-wide instantaneous bandwidth. The NeurACore signal processor comprises a digital signal pre-processing unit operable for performing cascaded decomposition of a wideband complex valued In-phase and Quadrature-phase (I/Q) input signal in real time. The wideband complex valued I/Q input signal is decomposed into I and Q sub-channels. The

NeurACore signal processor further comprises a NeurACore and local learning layers operable for performing high-dimensional projection of the wideband complex valued I/Q input signal into a high-dimensional state space. A global learning layer of the NeurACore signal processor is operable for performing a gradient descent online learning algorithm, and a neural combiner operable for combining outputs of the global learning layer to compute signal predictions corresponding to the wideband complex valued I/Q input signal.

In another aspect, the cascaded decomposition is a multi-layered I/Q decomposition scheme, wherein for each layer, a sample rate of the layer is reduced by half compared to a preceding layer in the cascaded decomposition.

In another aspect, the cascaded decomposition is a three layer I/Q decomposition scheme, and wherein the gradient descent online learning algorithm is an eight-dimensional gradient descent online learning algorithm.

In another aspect, the gradient descent online learning algorithm uses eight-dimensional state variables and weight matrices by cross coupling the eight-dimensional state variables in weights update equations and output layer update equations.

In another aspect, the digital signal pre-processing is further operable for implementing blind source separation (BSS) and feature extraction algorithms with updates to interpret denoised eight-dimensional state variables.

In another aspect, the NeurACore comprises high-dimensional signal processing nodes with adaptable parameters.

Finally, the present invention also includes a computer program product and a computer implemented method. The computer program product includes computer-readable instructions stored on a non-transitory computer-readable medium that are executable by a computer having one or more processors, such that upon execution of the instructions, the one or more processors perform the operations listed herein. Alternatively, the computer implemented method includes an act of causing a computer to execute such instructions and perform the resulting operations.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention will be apparent from the following detailed descriptions of the various aspects of the invention in conjunction with reference to the following drawings, where:

FIG. **1** is a block diagram depicting the components of a system for complex signal denoising according to some embodiments of the present disclosure;

FIG. **2** is an illustration of a computer program product according to some embodiments of the present disclosure;

FIG. **3** is an illustration of an ultra-wideband Neuromorphic Adaptive Core (NeurACore) architecture according to some embodiments of the present disclosure;

FIG. **4**A is an illustration of real valued wideband input data in a cascaded In-Phase and Quadrature-Phase (I/Q) decomposition concept of frequency translation of a single tone according to some embodiments of the present disclosure;

FIG. **4**B is an illustration of first level I/Q decomposition in a cascaded I/Q decomposition concept of frequency translation of a single tone according to some embodiments of the present disclosure;

FIG. **4**C is an illustration of second level I/Q decomposition in a cascaded I/Q decomposition concept of frequency translation of a single tone according to some embodiments of the present disclosure;

FIG. **5**A is an illustration of a first example of a phase relationship between 2^{nd} level resonator state functions according to some embodiments of the present disclosure;

FIG. **5**B is an illustration of a second example of a phase relationship between 2^{nd} level resonator state functions according to some embodiments of the present disclosure;

FIG. **5**C is an illustration of a third example of a phase relationship between 2^{nd} level resonator state functions according to some embodiments of the present disclosure;

FIG. **5**D is an illustration of a fourth example of a phase relationship between 2^{nd} level resonator state functions according to some embodiments of the present disclosure;

FIG. **6**A is an illustration of an ordinary differential equation for a first four-dimensional (4D) passive oscillator with the same 2^{nd} level baseband frequency according to some embodiments of the present disclosure;

FIG. **6**B is an illustration of an ordinary differential equation for a second 4D passive oscillator with the same 2^{nd} level baseband frequency according to some embodiments of the present disclosure;

FIG. **6**C is an illustration of an ordinary differential equation for a third 4D passive oscillator with the same 2^{nd} level baseband frequency according to some embodiments of the present disclosure;

FIG. **6**D is an illustration of an ordinary differential equation for a second 4D passive oscillator with the same 2^{nd} level baseband frequency according to some embodiments of the present disclosure;

FIG. **7**A is an illustration of the time domain response of a resonator that is designed to resonate at 100 megahertz (MHz) in the original band according to some embodiments of the present disclosure;

FIG. **7**B is an illustration of the frequency domain response of the resonator that is designed to resonate at 100 MHz in the original band according to some embodiments of the present disclosure;

FIG. **7**C is an illustration of the time domain response of a resonator that is designed to resonate at 200 MHz in the original band according to some embodiments of the present disclosure;

FIG. **7**D is an illustration of the frequency domain response of the resonator that is designed to resonate at 200 MHz in the original band according to some embodiments of the present disclosure;

FIG. **7**E is an illustration of the time domain response of a resonator that is designed to resonate at 400 MHz in the original band according to some embodiments of the present disclosure;

FIG. **7**F is an illustration of the frequency domain response of the resonator that is designed to resonate at 400 MHz in the original band according to some embodiments of the present disclosure;

FIG. **7**G is an illustration of the time domain response of a resonator that is designed to resonate at 600 MHz in the original band according to some embodiments of the present disclosure;

FIG. **7**H is an illustration of the frequency domain response of the resonator that is designed to resonate at 400 MHz in the original band according to some embodiments of the present disclosure;

FIG. **8**A is an illustration of of the time domain response of a resonator that is designed to resonate at 600 MHz in the original band with the Q value set for 100 according to some embodiments of the present disclosure;

FIG. **8**B is an illustration of the frequency domain response of the resonator that is designed to resonate at 600 MHz in the original band with the Q value set for 100 according to some embodiments of the present disclosure;

FIG. **8**C is an illustration of the time domain response of a resonator that is designed to resonate at 600 MHz in the original band with the Q value set for 10 according to some embodiments of the present disclosure;

FIG. **8**B is an illustration of the frequency domain response of the resonator that is designed to resonate at 600 MHz in the original band with the Q value set for 10 according to some embodiments of the present disclosure; and

FIG. **9** is a block diagram depicting control of a device according to various embodiments.

DETAILED DESCRIPTION

The present invention relates to a signal processor and, more particularly, to a signal processor for complex signal denoising in the ultra-wide instantaneous bandwidth. The following description is presented to enable one of ordinary skill in the art to make and use the invention and to incorporate it in the context of particular applications. Various modifications, as well as a variety of uses in different applications will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to a wide range of aspects. Thus, the present invention is not intended to be limited to the aspects presented, but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

In the following detailed description, numerous specific details are set forth in order to provide a more thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced without necessarily being limited to these specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring the present invention.

The reader's attention is directed to all papers and documents which are filed concurrently with this specification and which are open to public inspection with this specification, and the contents of all such papers and documents are incorporated herein by reference. All the features disclosed in this specification, (including any accompanying claims, abstract, and drawings) may be replaced by alternative features serving the same, equivalent, or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.

Furthermore, any element in a claim that does not explicitly state "means for" performing a specified function, or "step for" performing a specific function, is not to be interpreted as a "means" or "step" clause as specified in 35 U.S.C. Section 112, Paragraph 6. In particular, the use of "step of" or "act of" in the claims herein is not intended to invoke the provisions of 35 U.S.C. 112, Paragraph 6.

(1) Principal Aspects

Various embodiments of the invention include three "principal" aspects. The first is a system for complex signal denoising. The system is typically in the form of a computer system operating software or in the form of a "hard-coded" instruction set. This system may be incorporated into a wide variety of devices that provide different functionalities. The second principal aspect is a method, typically in the form of software, operated using a data processing system (computer). The third principal aspect is a computer program product. The computer program product generally represents computer-readable instructions stored on a non-tran-

sitory computer-readable medium such as an optical storage device, e.g., a compact disc (CD) or digital versatile disc (DVD), or a magnetic storage device such as a floppy disk or magnetic tape. Other, non-limiting examples of computer-readable media include hard disks, read-only memory (ROM), and flash-type memories. These aspects will be described in more detail below.

A block diagram depicting an example of a system (i.e., computer system **100**) of the present invention is provided in FIG. **1**. The computer system **100** is configured to perform calculations, processes, operations, and/or functions associated with a program or algorithm. In one aspect, certain processes and steps discussed herein are realized as a series of instructions (e.g., software program) that reside within computer readable memory units and are executed by one or more processors of the computer system **100**. When executed, the instructions cause the computer system **100** to perform specific actions and exhibit specific behavior, such as described herein.

The computer system **100** may include an address/data bus **102** that is configured to communicate information. Additionally, one or more data processing units, such as a processor **104** (or processors), are coupled with the address/data bus **102**. The processor **104** is configured to process information and instructions. In an aspect, the processor **104** is a microprocessor. Alternatively, the processor **104** may be a different type of processor such as a parallel processor, application-specific integrated circuit (ASIC), programmable logic array (PLA), complex programmable logic device (CPLD), or a field programmable gate array (FPGA).

The computer system **100** is configured to utilize one or more data storage units. The computer system **100** may include a volatile memory unit **106** (e.g., random access memory ("RAM"), static RAM, dynamic RAM, etc.) coupled with the address/data bus **102**, wherein a volatile memory unit **106** is configured to store information and instructions for the processor **104**. The computer system **100** further may include a non-volatile memory unit **108** (e.g., read-only memory ("ROM"), programmable ROM ("PROM"), erasable programmable ROM ("EPROM"), electrically erasable programmable ROM "EEPROM"), flash memory, etc.) coupled with the address/data bus **102**, wherein the non-volatile memory unit **108** is configured to store static information and instructions for the processor **104**. Alternatively, the computer system **100** may execute instructions retrieved from an online data storage unit such as in "Cloud" computing. In an aspect, the computer system **100** also may include one or more interfaces, such as an interface **110**, coupled with the address/data bus **102**. The one or more interfaces are configured to enable the computer system **100** to interface with other electronic devices and computer systems. The communication interfaces implemented by the one or more interfaces may include wireline (e.g., serial cables, modems, network adaptors, etc.) and/or wireless (e.g., wireless modems, wireless network adaptors, etc.) communication technology.

In one aspect, the computer system **100** may include an input device **112** coupled with the address/data bus **102**, wherein the input device **112** is configured to communicate information and command selections to the processor **100**. In accordance with one aspect, the input device **112** is an alphanumeric input device, such as a keyboard, that may include alphanumeric and/or function keys.

Alternatively, the input device **112** may be an input device other than an alphanumeric input device. In an aspect, the computer system **100** may include a cursor control device **114** coupled with the address/data bus **102**, wherein the cursor control device **114** is configured to communicate user input information and/or command selections to the processor **100**. In an aspect, the cursor control device **114** is implemented using a device such as a mouse, a track-ball, a track-pad, an optical tracking device, or a touch screen. The foregoing notwithstanding, in an aspect, the cursor control device **114** is directed and/or activated via input from the input device **112**, such as in response to the use of special keys and key sequence commands associated with the input device **112**. In an alternative aspect, the cursor control device **114** is configured to be directed or guided by voice commands.

In an aspect, the computer system **100** further may include one or more optional computer usable data storage devices, such as a storage device **116**, coupled with the address/data bus **102**. The storage device **116** is configured to store information and/or computer executable instructions. In one aspect, the storage device **116** is a storage device such as a magnetic or optical disk drive (e.g., hard disk drive ("HDD"), floppy diskette, compact disk read only memory ("CD-ROM"), digital versatile disk ("DVD")). Pursuant to one aspect, a display device **118** is coupled with the address/data bus **102**, wherein the display device **118** is configured to display video and/or graphics. In an aspect, the display device **118** may include a cathode ray tube ("CRT"), liquid crystal display ("LCD"), field emission display ("FED"), plasma display, or any other display device suitable for displaying video and/or graphic images and alphanumeric characters recognizable to a user.

The computer system **100** presented herein is an example computing environment in accordance with an aspect. However, the non-limiting example of the computer system **100** is not strictly limited to being a computer system. For example, an aspect provides that the computer system **100** represents a type of data processing analysis that may be used in accordance with various aspects described herein. Moreover, other computing systems may also be implemented. Indeed, the spirit and scope of the present technology is not limited to any single data processing environment. Thus, in an aspect, one or more operations of various aspects of the present technology are controlled or implemented using computer-executable instructions, such as program modules, being executed by a computer. In one implementation, such program modules include routines, programs, objects, components and/or data structures that are configured to perform particular tasks or implement particular abstract data types. In addition, an aspect provides that one or more aspects of the present technology are implemented by utilizing one or more distributed computing environments, such as where tasks are performed by remote processing devices that are linked through a communications network, or such as where various program modules are located in both local and remote computer-storage media including memory-storage devices.

An illustrative diagram of a computer program product (i.e., storage device) embodying the present invention is depicted in FIG. **2**. The computer program product is depicted as floppy disk **200** or an optical disk **202** such as a CD or DVD. However, as mentioned previously, the computer program product generally represents computer-readable instructions stored on any compatible non-transitory computer-readable medium. The term "instructions" as used with respect to this invention generally indicates a set of operations to be performed on a computer, and may represent pieces of a whole program or individual, separable, software modules. Non-limiting examples of "instruction" include computer program code (source or object code) and

"hard-coded" electronics (i.e., computer operations coded into a computer chip). The "instruction" is stored on any non-transitory computer-readable medium, such as in the memory of a computer or on a floppy disk, a CD-ROM, and a flash drive. In either event, the instructions are encoded on a non-transitory computer-readable medium.

(2) Specific Details of Various Embodiments of the Invention Described is an implementation of the Ultra-Wide Instantaneous Bandwidth (IBW) Neuromorphic Adaptive Core (NeurACore) processor, used for the denoising of real-valued and complex In-Phase and Quadrature-Phase (I/Q) signals (i.e., signals in ultra-wide IBW). IBW refers to the bandwidth in which all frequency components can be simultaneously analyzed. The term "real-time bandwidth" is often used interchangeably with IBW to describe the maximum continuous radio frequency (RF) bandwidth that an instrument generates or acquires. A real-valued signal is a complex signal where all the imaginary component of all the complex values are strictly zero. Real-valued signals have one degree of freedom. Complex signals are often used to represent signals, or data, with two degrees of freedom, such as magnitude and phase, or kinetic and potential energy.

The invention described herein is a system for real-time, real-valued and complex I/Q signal denoising in ultra-wide IBW with processor clock speed that is lower than the data sampling rate. The denoiser according to embodiments of the present disclosure provides detection and denoising capabilities for complex (I/Q) signals, including low probability of intercept (LPI), low probability of detection (LPD), and frequency hopping signals. A LPI radar is a radar employing measures to avoid detection by passive radar detection equipment (such as a radar warning receiver (RWR), or electronic support receiver) while it is searching for a target or engaged in target tracking. LPI and LPD allow an active acoustic source to be concealed or camouflaged so that the signal is essentially undetectable. Frequency-hopping spread spectrum (FHSS) is a method of transmitting radio signals by rapidly changing the carrier frequency among many distinct frequencies occupying a large spectral band. Signals rapidly change, or hop, their carrier frequencies among the center frequencies of these sub-bands in a predetermined order.

Additionally, the denoiser improves the signal-to-noise ratio (SNR) performance by >20 decibels (dB) for a variety of different waveforms, as will be described in detail below. Key advantages of the present invention compared to current state-of-the art systems are the ultra-low latency detection and denoising of wideband input signals. Comparable systems, like a conventional channelizer, would operate over a smaller frequency band and likely require larger latency to achieve the same processing results. Additionally, the system enables detection and denoising of fast frequency hopping signals that cannot be achieved with current frequency channelization-based systems. While current machine learning approaches would require large quantities of online/offline training data, the system described herein does not require any pre-training.

The ultra-wide IBW for the real-time digital signal processing system (i.e., NeurACore) according to embodiments of the present disclosure is defined as where the incoming signal's sample rate is larger than the digital signal processor's (i.e., NeurACore) clock speed. Here, it is assumed that the input signal is uniformly sampled with a sampling clock whose clock speed is fs (sampling frequency, or sampling rate) The samples are quantized and fed to the digital signal processor whose clock rate is fc. In computing, the clock rate refers to the frequency at which the clock generator of a processor can generate pulses, which are used to synchronize the operation of its components. The clock rate is used as an indicator of the processor's speed and is measured in clock cycles per second. The heart of the invention described herein is a cascaded I/Q decomposition that enables NeurACore to achieve an instantaneous bandwidth (IBW) that is significantly higher than the clock speed of the digital processor. The system described herein, which is an ultra-wide IBW real-time denoiser (where fs>fc), greatly improves SWAP (size, weight, and power) of hardware over comparable systems with the same performance, such as a conventional channelizer. In the present invention, the sampling rate is twice the IBW. The input signal with a channelizer typically has a higher sample rate than the sample rate of the selected channel.

The NeurACore processor architecture, depicted in FIG. **3**, consists of several elements. A high-speed (e.g., IBW greater than 200 MHz) digital signal pre-processing unit **300** performs cascaded I/Q decomposition of the complex input signal **302** in real time. A neuromorphic adaptive core and local learning layers **304** perform high-dimensional projection of the input signal into the high-dimensional state space of the core's dynamical model, where $A_{I/Q}$ represents the core state-space coefficients. A global learning layer **306** (i.e., output layer that performs the gradient descent online learning) and neural combiner **308** perform gradient descent-based online learning of the output layer weights from the global learning layer **306** to achieve short-term signal prediction of the input signal without any knowledge of the signal itself. The neural combiner **308** combines the I and Q outputs from the global learning layer **306**. Output I **314** and Output Q **316** represent the signal predictions.

As described above, a unique concept of the invention is the cascaded I/Q signal decomposition and related signal processing algorithms where the wideband complex valued (I/Q) input signal **302** is further decomposed into I and Q sub-channels (i.e., I of I, Q of I, I of Q and Q of Q) for a two layer I/Q decomposition scheme. The advantage of the two layer I/Q signal decomposition is that the sample rate of the four correlated sub-channels is reduced by a factor of two compared to the sample rate of the 1^{st} layer I/Q decomposed input signal **310**. This cascading operation can be continued until the condition offscas<=fc is satisfied. Here, fscas is the required sample rate for the time series data at the last cascading layer. For every new cascading layer, the sample rate is reduced by half (i.e., fscas=fs/2 for a single layer, fscas=fs/4 for two layers, fscas=fs/8 for three layers), where fs is the sample rate of the real-valued input signal.

(2.1) Ultra-Wideband NeurACore Architecture

The basic innovation that enables the ultra-wideband NeurACore architecture is shown in FIG. **3**. To increase the bandwidth of NeurACore beyond the clock speed of the digital processor (i.e., $f_{sampling}>>f_{clock}$), the unique concept of cascaded In-phase and Quadrature-phase (I/Q) signal decomposition and related signal processing algorithms was utilized, as described above. The I/Q decomposition ensures unique and invertible signal transformation between the original I/Q input and its decomposed counterpart, so interpreting and converting back these low sample rate multidimensional signals into the original I/Q signal is always possible.

These cascaded I/Q signal decompositions can be continued to many levels, ensuring that the actual digital signal processor clock speed can always be larger than the sample rate of the last decomposition level (i.e., $f_{final\ I/Q\ sampling}<f_{clock}$). For example, an existing NeurACore hardware implementation (disclosed in U.S. application Ser.

No. 17/375,724, which is hereby incorporated by reference as though fully set forth herein) operated at 300 MSps (mega samples per second), so a three layer I/Q signal decomposition will ensure processing signals with >1 gigahertz (GHz) IBW. This means that most of the internal signals used in the Core and Blind Source Separation (BSS) will be eight-dimensional so one must use an eight-dimensional gradient descent online learning algorithm, as described in detail below.

The following are references that describe the use of the gradient descent online learning algorithm for updating output layer weights for an online learning system: M. Lukosevicius and H. Jaeger, "Reservoir computing approaches to recurrent neural network training", Computer Science Review, 2009, and Jing Dai, et al., "An Introduction to the Echo State Network and its Applications in Power System", 15th International Conference on Intelligent System Applications to Power Systems, 2009, both of which are hereby incorporated by reference as though fully set forth herein. The system according to embodiments of the present disclosure improves upon these approaches by extending the signal processing bandwidth beyond the clock speed of the processor (fs>fc), where the real-time denoising processing algorithm is implemented, and extending the basic gradient descent online learning algorithm into the cascaded I/Q decomposed signal domain. By utilizing additional learning layers, such as the global learning layer, along with the extended capability of the neuromorphic adaptive core **304**, the present invention enables real-time signal denoising in ultra-wide bandwidth for both real-valued and complex (I/Q) input signals.

The most challenging aspect of the unique cascaded I/Q decomposition-based signal processing concept is to design the state space models for the nodes in the neuromorphic adaptive core that behave the same way as the nodes in the current, not cascaded, design (i.e., passive resonators with adaptable Q-values and resonant frequencies). In the current design, the standard two-dimensional state space models are used for these passive resonators that must be abstracted to high-dimensional models, assuming that their state space models will be driven by the cascaded I/Q decomposed high dimensional signals. In other words, one needs to design an abstract high-dimensional oscillator array with adaptable parameters. HRL Laboratories, LLC has developed and verified, by analysis and MatLab simulations, such abstract high dimensional signal processing nodes that form the key building blocks for the ultra-wide bandwidth NeurACore, as described in U.S. application Ser. No. 17/375,724.

The other significant algorithm change in the ultra-wide bandwidth NeurACore design compared to the previously disclosed, not cascaded, version is the online learning algorithm that must utilize the high-dimensional state variables from the core in the online learning/adaptation process. HRL Laboratories, LLC has developed such gradient descent online learning algorithm that is currently utilized in the existing NeurACore field-programmable gate array (FPGA) hardware prototype, as described in U.S. application Ser. No. 17/375,724. In the current hardware implementation, the learning algorithm utilizes two-dimensional (I and Q) state variables along with two-dimensional weight matrices. For the ultra-wide bandwidth NeurACore architecture described herein, the learning algorithm is extended to eight-dimensional state variables and weight matrices by properly cross coupling the eight-dimensional state variables in the weights update and output update equations.

Optionally, the disclosed ultra-wide IBW NeurACore can be extended with Blind Source Separation (BSS) and feature extractions algorithms that also need to be updated to properly interpret the denoised eight-dimensional state variables in order to accurately separate the unknown signal(s) from the signal mixture where all signals are represented by eight-dimensional state variables. Energy and phase maps for the real-time spectrogram are generated from the eight-dimensional state variables. At this stage of the processing one can convert back the abstract high-dimensional energy and phase maps into conventional spectrogram image(s) for the classification algorithm that is trained on conventional spectrogram images. However, the processing scheme described herein enables new classification approaches, where the classifier (e.g., deep learning neural network) can be trained directly on the high-dimensional energy and phase maps. It is believed that the high-dimensional energy and phase maps contain significantly more unique features about the signals than conventional spectrograms and will enable significantly improved classification performance. To increase the bandwidth of the NeurACore beyond the clock speed of the digital processor (i.e., $f_{sampling} >> f_{clock}$), cascaded In-phase and Quadrature-phase (I/Q) signal decomposition and related signal processing algorithms are utilized. The wideband, complex-valued (I/Q) input signal is further decomposed into I and Q sub-channels (i.e., I of I, Q of I, I of Q and Q of Q) for a two layer I/Q decomposition, as shown in FIG. **3**.

A MatLab simulation example showing how a single tone at 149.9 MHz will be translated to −0.1 MHz at the second decomposition level (**312** in FIG. **3**) is depicted in FIGS. **4**A-**4**C. It is assumed that the original sample rate is 400 MHz, corresponding to a 200 MHz bandwidth. At the first decomposition level (**310** in FIG. **3**), the tone is translated to 49.9 MHz, as shown in FIG. **4**B. At the second decomposition level (**312** in FIG. **3**), the single tone translates into four properly phase aligned tones each having resonant frequency of 0.1 MHz, as shown in FIG. **4**C.

FIGS. **5**A-**5**D illustrate all four phase alignment combinations between the four time series representing the four different frequencies in the original wideband signal. All four frequencies, I-of-I, Q-of-I, I-of-Q, and Q-of-Q, (represented by different types of lines (e.g., dashed, solid, bold) shown in FIGS. **5**A-**5**D translate to the same baseband frequency (i.e., 0.1 MHz). However, their phase alignment uniquely identifies each original frequency in the wide band as shown in the figures.

FIGS. **6**A-**6**D depict four coupled Ordinary Differential Equations (ODE) sets for the four four-dimensional (4D) resonators that have the same baseband resonant frequency, but represent four different resonances in the wide band. The ODEs are parameterized by the baseband resonant frequency and quality factor (Q) values. The four ODE systems have a very similar basic structure but have different sign arrangements associated with the required phase constraints between the different states. It is interesting to observe that some of the terms associated with resonator losses are positive. However, the passivity constraints are enforced via the cross-coupling terms and negative loss values in the main diagonal elements.

FIGS. **7**A-**7**H show MatLab simulation results for the 4D resonators excited by a wideband chirp signal. Here, it is assumed a 350 MHz processor clock speed for simulating the 4D resonators and 1.4 G samples per second (Sps) sampling rate for the real valued wideband input time series. The input is a wideband chirp signal with its instantaneous frequency covering the DC-700 MHz frequency band. The overall bandwidth is 700 MHz. After the second level I/Q decomposition, the original 700 MHz bandwidth chirp sig-

nal is converted into four 175 MHz bandwidth signals sampled at 350 MHz sample rate each.

FIGS. **7**A and **7**B show the time domain and frequency domain responses, respectively, of the 1^{st} resonator that is designed to resonate at 100 MHz in the original band. The Q value is set for 1000 to make the resonant frequency clearly visible. This resonator has the state space model that is identical to the model in FIG. **6**A. The simulation result shows proper wideband responses of the 4D resonator with resonant frequency equal to 100 MHz.

FIGS. **7**C and **7**D show the time domain and frequency domain responses, respectively, of the 2^{nd} resonator that is designed to resonate at 200 MHz in the original band. This resonator has the state space model that is identical to the model in FIG. **6**B. The Q value is set for 1000 to make the resonant frequency clearly visible. The simulation result shows proper wideband responses of the 4D resonator with resonant frequency equal to 200 MHz.

FIGS. **7**E and **7**F show the time domain and frequency domain responses, respectively, of the 3^{rd} resonator that is designed to resonate at 400 MHz in the original band. This resonator has the state space model that is identical to the model in FIG. **6**C. The Q value is set for 1000. The simulation result shows proper wideband responses of the 4D resonator with resonant frequency equals to 400 MHz.

FIGS. **7**G and **7**H show the time domain and frequency domain responses, respectively, of the 4^{th} resonator that is designed to resonate at 600 MHz in the original band. This resonator has the state space model that is identical to the model in FIG. **6**D. The Q value is set for 1000. The simulation result shows proper wideband responses of the 4D resonator with resonant frequency equals to 600 MHz. It is important to note that no parasitic resonances are visible on either the time domain or frequency domain plots. The image frequency resonances are suppressed by more than 300 dB.

FIGS. **8**A-**8**D show MatLab simulation results for the 4D resonators excited by a wideband chirp signal. Here, the resonators have different Q values. Additionally, a 350 MHz processor clock speed is assumed for simulating the 4D resonators and 1.4 giga samples per second (GSps) sampling rate for the real valued wideband input time series. The instantaneous frequency of the chirp covers the DC-700 MHz frequency band. The overall bandwidth is 700 MHz. After the second level I/Q decomposition, the original 700 MHz bandwidth chirp signal is converted into four 175 MHz bandwidth signals sampled at 350 MHz sample rate as before.

FIGS. **8**A and **8**B show the time domain and frequency domain responses, respectively, of the 4^{th} resonator that is designed to resonate at 600 MHz in the original band. The Q value is set for 100. This resonator has the state space model that is identical to the model in FIG. **6**D. The simulation result shows proper wideband responses of the 4D resonator with resonant frequency equals to 600 MHz and Q value of 100.

FIGS. **8**C and **8**D show the time domain and frequency domain responses, respectively, of the 4^{th} resonator that is designed to resonate at 600 MHz in the original band. However, unlike FIGS. **8**A and **8**B, here the Q value is set for 10. This resonator also has the state space model that is identical to the model in FIG. **6**D. The simulation result shows proper wideband responses of the 4D resonator with resonant frequency equal to 600 MHz and Q value of 10. The widening of the resonance curve around the resonant frequency is clearly visible on the plots. It is important to note that no parasitic resonances are visible on either the time domain or frequency domain plots. The image frequency resonances are suppressed by more than 300 dB.

The online learning algorithm must utilize the high-dimensional state variables from the core in the online learning/adaptation process. For the ultra-wide bandwidth NeurACore architecture that can achieve >1 GHz IBW, the learning algorithm is extended to eight-dimensional state variables and weights matrices by properly cross-coupling the eight-dimensional state variables in the weights update and outputs update equations. The BSS and feature extractions algorithms are also updated to properly interpret the detected and denoised eight-dimensional state variables in order to accurately separate the unknown signal(s) from the signal mixture where all signals are represented by eight-dimensional state variables. Energy and phase maps for the real-time spectrogram are generated from the eight-dimensional state variables.

During the development of this concept, a systemic gradual approach was utilized in validating the cascaded I/Q decomposition for NeurACore by first focusing on the two-layer version for which most internal signals are four-dimensional and can achieve 2*fs IBW. The two-layer case was validated with four-dimensional state variables, gradient descent equations, and global learning layer for the output weights. The extensions of the BSS and feature extraction algorithms to the two-layer cascaded I/Q formulation were also validated. The lessons learned from the validation of the two-layer version can be incorporated into the generalized three layer and beyond cascaded I/Q algorithm formulation and implementation that will achieve >4*fs IBW.

Many commercial and military signal processing platforms require small size, ultra-wide bandwidth operation, ultra-low C-SWaP (cost, size, weight, and power) signal processing units, and artificial intelligence enhanced with real-time signal processing capability. This includes, but is not limited to radar, communication, acoustic, audio, video, and optical waveforms.

(2.2) Control of a Device

As shown in FIG. **9**, the NeurACore **900** in its hardware implementation has many applications. In one aspect, the system with the NeurACore **900** can be used for signal denoising to denoise noisy input signals **901**. In some aspects, the NeurACore **900** can be used to control a device **902** based on the signal denoising (e.g., a mobile device display, a virtual reality display, an augmented reality display, a computer monitor, a motor, an autonomous vehicle, a machine, a drone, a camera, etc.). In some embodiments, the device **902** may be controlled to cause the device **902** to move or otherwise initiate a physical action based on the denoised signal.

In some embodiments, a drone or other autonomous vehicle may be controlled to move to an area where an object is determined to be based on the imagery. In yet some other embodiments, a camera may be controlled to orient towards the identified object. In other words, actuators or motors are activated to cause the camera (or sensor) to move or zoom in on the location where the object is localized. In yet another aspect, if a system is seeking a particular object and if the object is not determined to be within the field-of-view of the camera, the camera can be caused to rotate or turn to view other areas within a scene until the sought-after object is detected.

In addition, in a non-limiting example of an autonomous vehicle having multiple sensors, such as cameras, which might include noisy signals that need denoising. The system can denoise the signal and then, based on the signal, cause

the autonomous vehicle to perform a vehicle operation. For instance, if two vehicle sensors detect the same object, object detection and classification accuracy is increased and the system described herein can cause a precise vehicle maneuver for collision avoidance by controlling a vehicle component. For example, if the object is a stop sign, the system may denoise a noisy input signal to identify the stop sign and then may cause the autonomous vehicle to apply a functional response, such as a braking operation, to stop the vehicle. Other appropriate responses may include one or more of a steering operation, a throttle operation to increase speed or to decrease speed, or a decision to maintain course and speed without change. The responses may be appropriate for avoiding a collision, improving travel speed, or improving efficiency. Non-limiting examples of devices that can be controlled via the NeurACore include a vehicle or a vehicle component, such as a brake, a steering mechanism, suspension, or safety device (e.g., airbags, seatbelt tensioners, etc.). Further, the vehicle could be an unmanned aerial vehicle (UAV), an autonomous ground vehicle, or a human operated vehicle controlled either by a driver or by a remote operator. As can be appreciated by one skilled in the art, control of other device types is also possible.

Finally, while this invention has been described in terms of several embodiments, one of ordinary skill in the art will readily recognize that the invention may have other applications in other environments. It should be noted that many embodiments and implementations are possible. Further, the following claims are in no way intended to limit the scope of the present invention to the specific embodiments described above. In addition, any recitation of "means for" is intended to evoke a means-plus-function reading of an element and a claim, whereas any elements that do not specifically use the recitation "means for", are not intended to be read as means-plus-function elements, even if the claim otherwise includes the word "means". Further, while particular method steps have been recited in a particular order, the method steps may occur in any desired order and fall within the scope of the present invention.

What is claimed is:

1. A Neuromorphic Adaptive Core (NeurACore) signal processor for ultra-wide instantaneous bandwidth denoising of a noisy signal, comprising:

a digital signal pre-processing unit, the digital signal pre-processing unit being operable for performing cascaded decomposition of a wideband complex valued In-phase and Quadrature-phase (I/Q) input signal in real time,

wherein the wideband complex valued I/Q input signal is decomposed into I and Q sub-channels;

a NeurACore and local learning layers, the NeurACore and local learning layers operable for performing high-dimensional projection of the wideband complex valued I/Q input signal into a high-dimensional state space;

a global learning layer, the global learning layer operable for performing a gradient descent online learning algorithm; and

a neural combiner, the neural combiner operable for combining outputs of the global learning layer to compute signal predictions corresponding to the wideband complex valued I/Q input signal.

2. The NeurACore signal processor as set forth in claim **1**, wherein the cascaded decomposition is a multi-layered I/Q decomposition scheme, wherein for each layer, a sample rate of the layer is reduced by half compared to a preceding layer in the cascaded decomposition.

3. The NeurACore signal processor as set forth in claim **2**, wherein the cascaded decomposition is a three layer I/Q decomposition scheme, and wherein the gradient descent online learning algorithm is an eight-dimensional gradient descent online learning algorithm.

4. The NeurACore signal processor as set forth in claim **3**, wherein the gradient descent online learning algorithm uses eight-dimensional state variables and weight matrices by cross coupling the eight-dimensional state variables in weights update equations and output layer update equations.

5. The NeurACore signal processor as set forth in claim **4**, wherein the digital signal pre-processing is further operable for implementing blind source separation (BSS) and feature extraction algorithms with updates to interpret denoised eight-dimensional state variables.

6. The NeurACore signal processor as set forth in claim **1**, wherein the NeurACore comprises high-dimensional signal processing nodes with adaptable parameters.

7. A computer program product comprising a non-transitory computer-readable medium having computer-readable instructions stored thereon, wherein the computer-readable instructions are executable by a computer having one or more processors for causing the one or more processors to perform operations of:

performing cascaded decomposition of a wideband complex valued In-phase and Quadrature-phase (I/Q) input signal in real time into I and Q sub-channels;

performing high-dimensional projection of the wideband complex valued I/Q input signal into a high-dimensional state space;

performing a gradient descent online learning algorithm; and

combining outputs of the global learning layer to compute signal predictions corresponding to the wideband complex valued I/Q input signal.

8. The computer program product as set forth in claim **7**, wherein the cascaded decomposition is a multi-layered I/Q decomposition scheme, wherein for each layer, a sample rate of the layer is reduced by half compared to a preceding layer in the cascaded decomposition.

9. The computer program product as set forth in claim **8**, wherein the cascaded decomposition is a three layer I/Q decomposition scheme, and wherein the gradient descent online learning algorithm is an eight-dimensional gradient descent online learning algorithm.

10. The computer program product as set forth in claim **9**, wherein the gradient descent online learning algorithm uses eight-dimensional state variables and weight matrices by cross coupling the eight-dimensional state variables in weights update equations and output layer update equations.

11. The computer program product as set forth in claim **10**, wherein blind source separation (BSS) and feature extraction algorithms are implemented with updates to interpret denoised eight-dimensional state variables.

12. A computer implemented method for ultra-wide instantaneous bandwidth denoising of a noisy signal, the method comprising an act of:

causing one or more processers to execute instructions encoded on a non-transitory computer-readable medium, such that upon execution, the one or more processors perform operations of:

performing cascaded decomposition of a wideband complex valued In-phase and Quadrature-phase (I/Q) input signal in real time into I and Q sub-channels;

performing high-dimensional projection of the wideband complex valued I/Q input signal into a high-dimensional state space;

performing a gradient descent online learning algorithm; and

combining outputs of the global learning layer to compute signal predictions corresponding to the wideband complex valued I/Q input signal.

13. The method as set forth in claim **12**, wherein the cascaded decomposition is a multi-layered I/Q decomposition scheme, wherein for each layer, a sample rate of the layer is reduced by half compared to a preceding layer in the cascaded decomposition.

14. The method as set forth in claim **13**, wherein the cascaded decomposition is a three layer I/Q decomposition scheme, and wherein the gradient descent online learning algorithm is an eight-dimensional gradient descent online learning algorithm.

15. The method as set forth in claim **14**, wherein the gradient descent online learning algorithm uses eight-dimensional state variables and weight matrices by cross coupling the eight-dimensional state variables in weights update equations and output layer update equations.

16. The method as set forth in claim **15**, wherein the digital signal pre-processing is further operable for implementing blind source separation (BSS) and feature extraction algorithms with updates to interpret denoised eight-dimensional state variables.

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