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Willard

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(54) **RF SWITCH STACK WITH CHARGE REDISTRIBUTION**

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H04B 1/48 (2006.01)
H03H 11/02 (2006.01)
H03K 17/687 (2006.01)
H04B 1/44 (2006.01)

(52) **U.S. Cl.**

CPC **H03K 17/6874** (2013.01); **H03H 11/02** (2013.01); **H04B 1/44** (2013.01); **H04B 1/48** (2013.01)

(58) **Field of Classification Search**

CPC H03K 17/6874; H03K 17/693; H03K 17/6871; H04B 1/48; H04B 1/44; H03H 11/02

See application file for complete search history.

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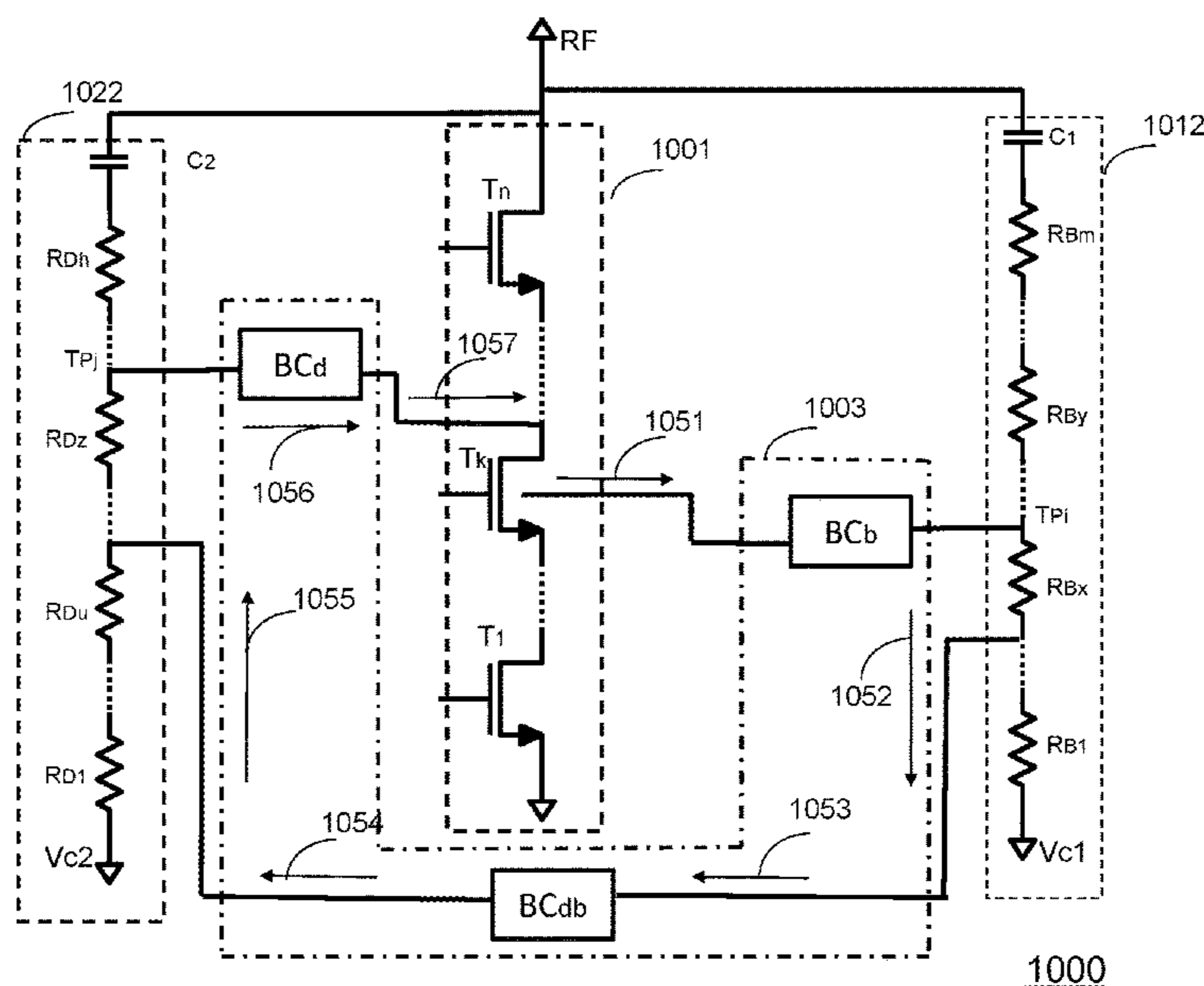
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(57) **ABSTRACT**

Methods and devices to address body leakage current generation and bias voltage distribution associated with body leakage current in an OFF state of a FET switch stack are disclosed. The devices include charge redistribution arrangements and bridge networks to perform coupling/decoupling to/from the FET switch stack. Detailed structures of such bridge networks are also described.

30 Claims, 25 Drawing Sheets



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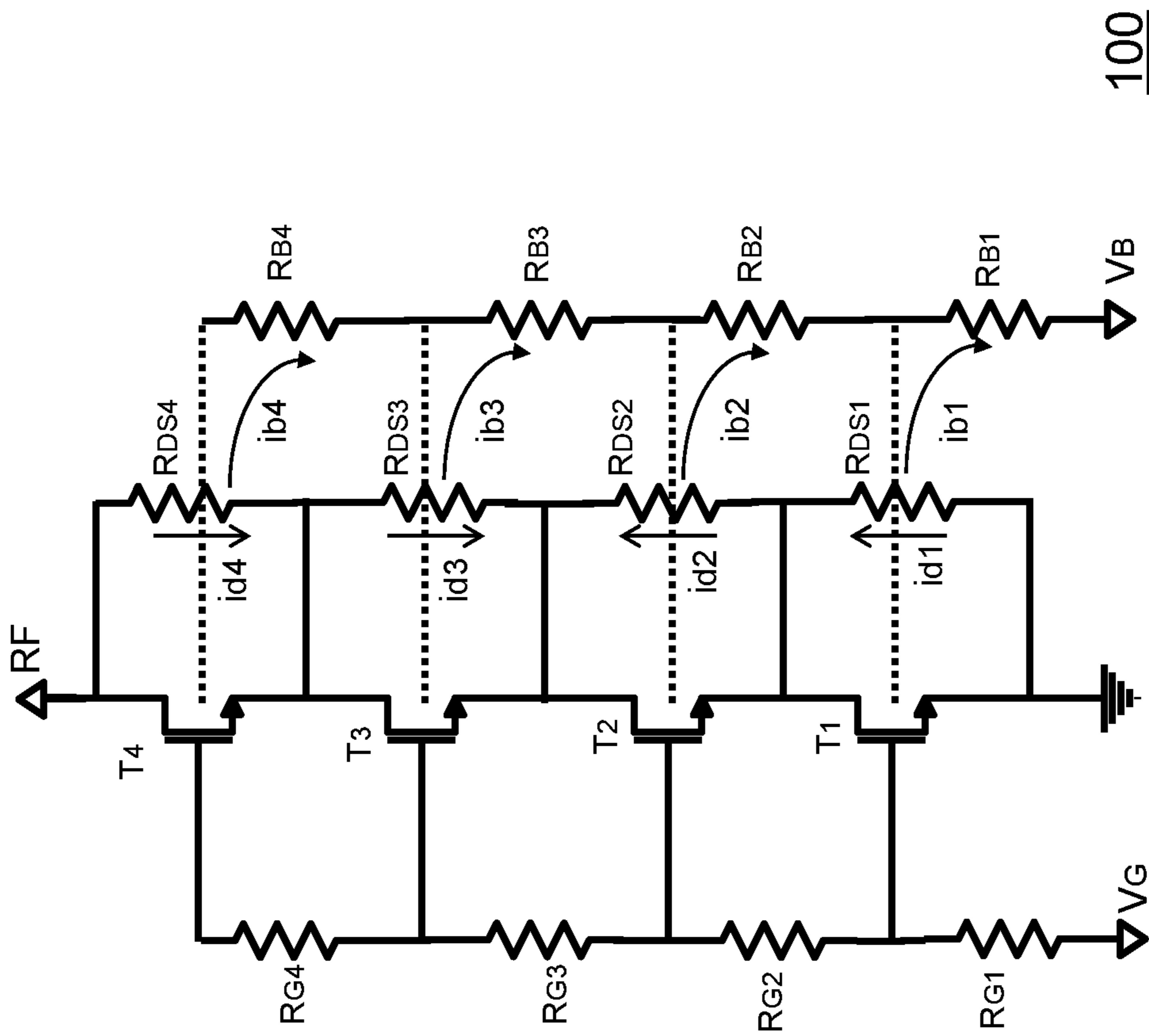


Fig. 1A (PRIOR ART)

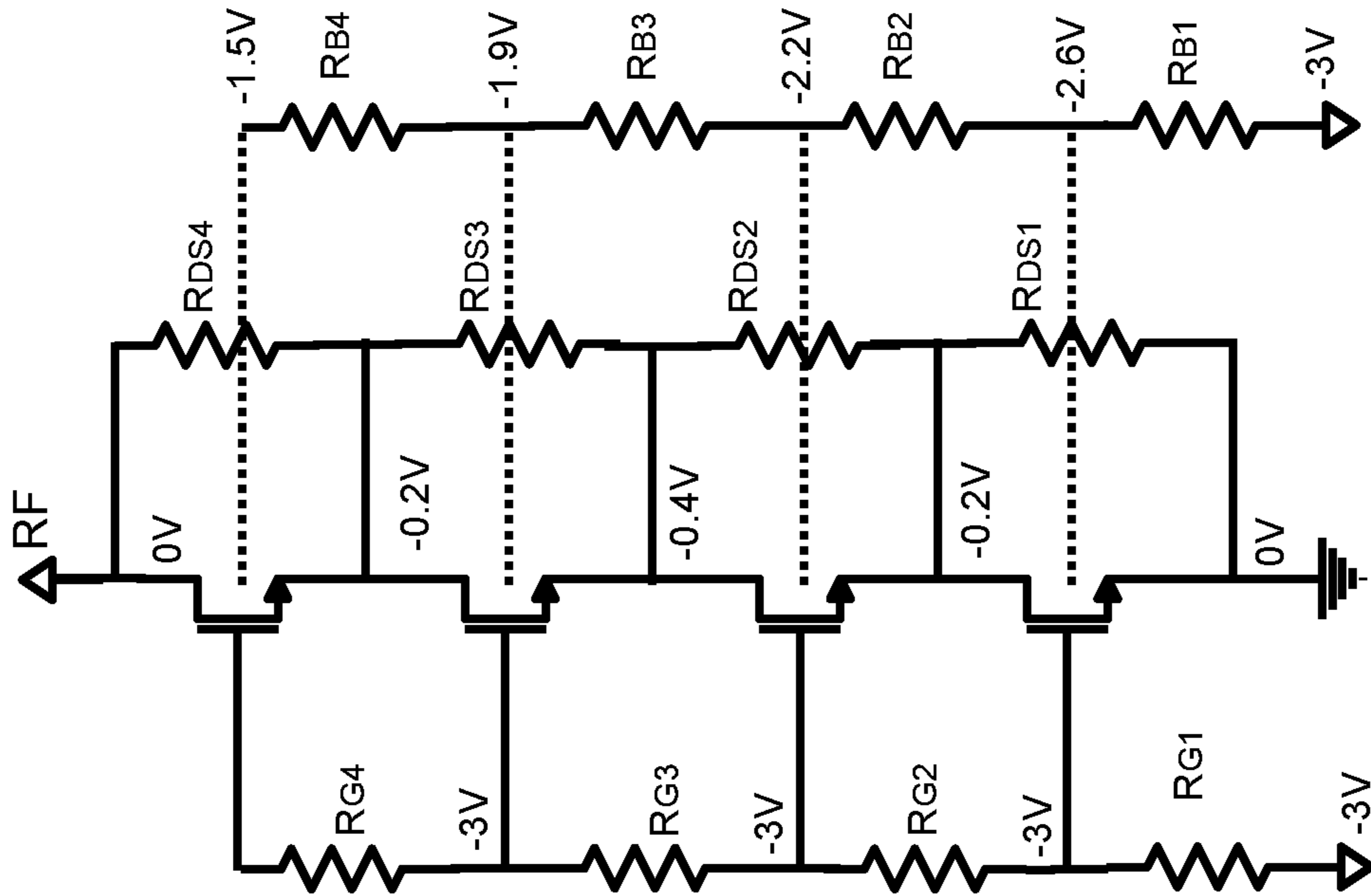


Fig. 1C (PRIOR ART)

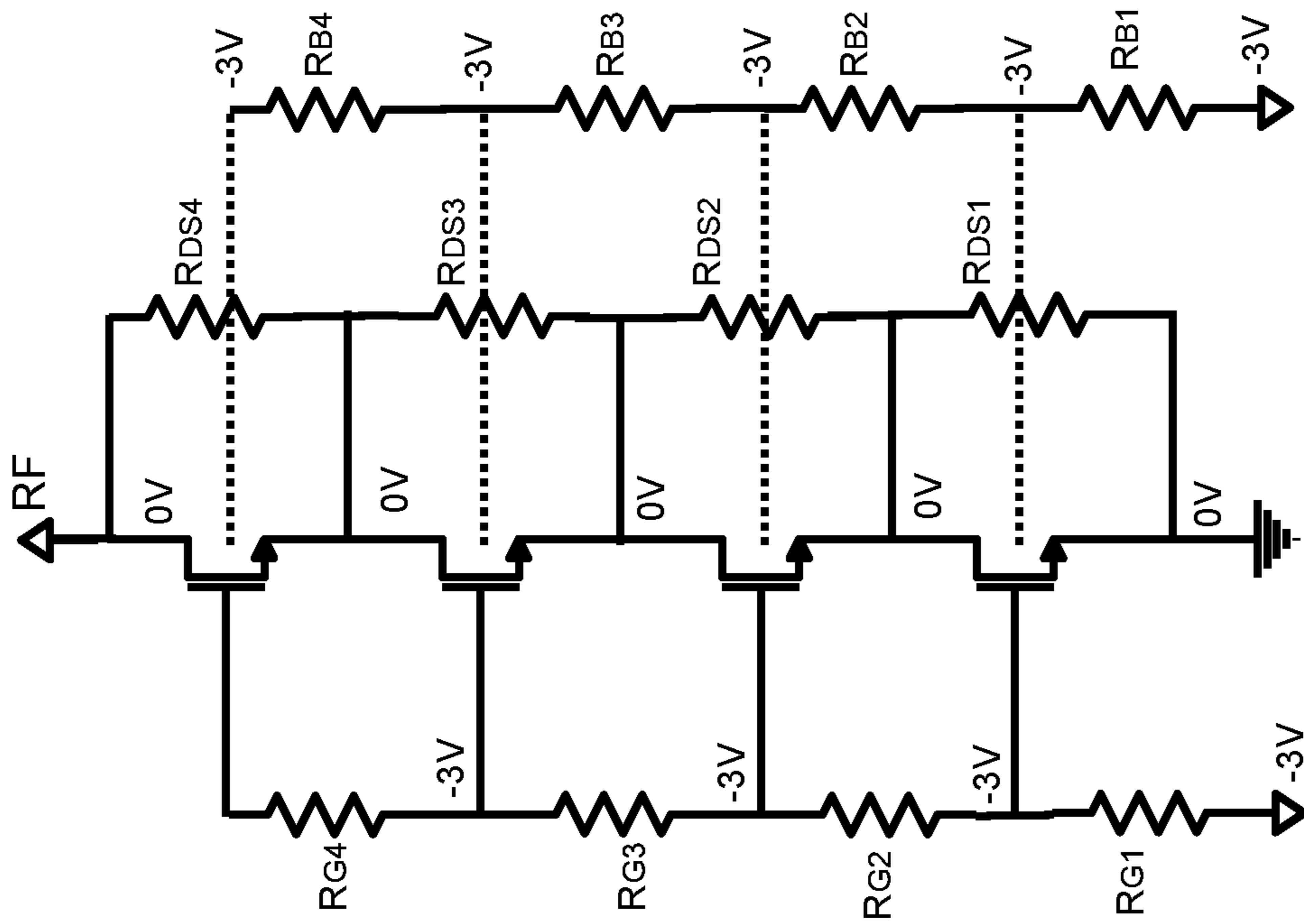


Fig. 1B (PRIOR ART)

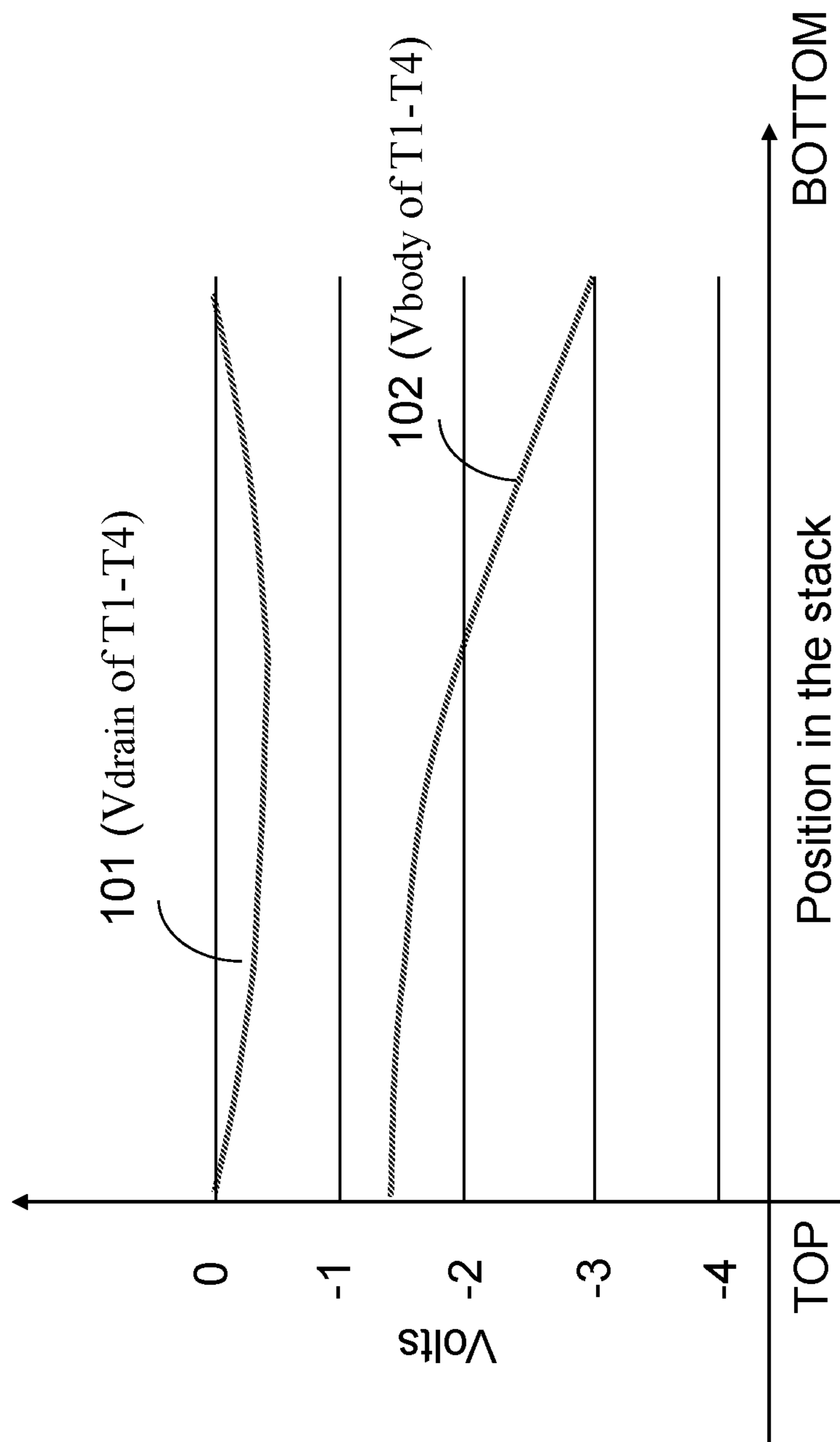


Fig. 2

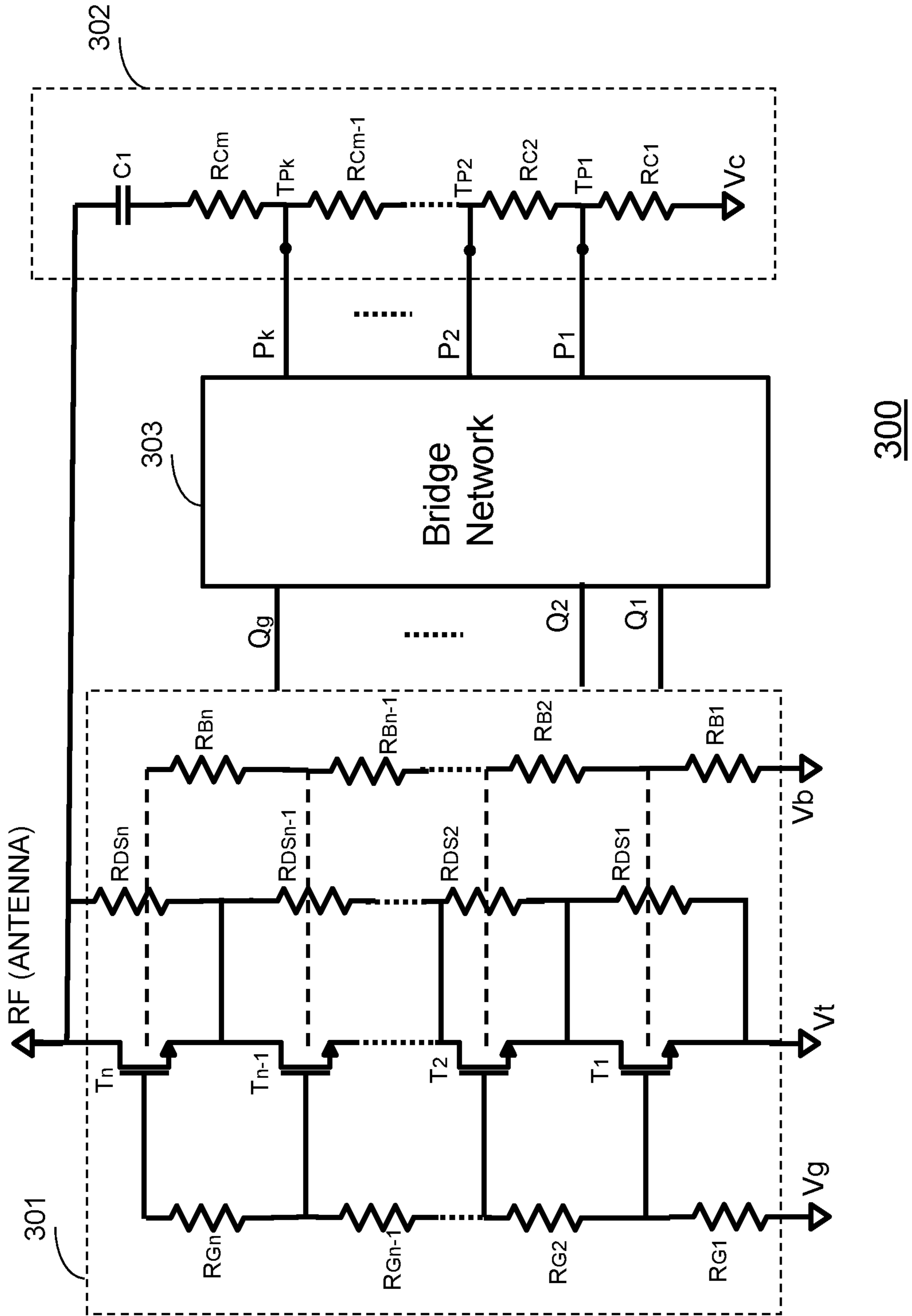


Fig. 3

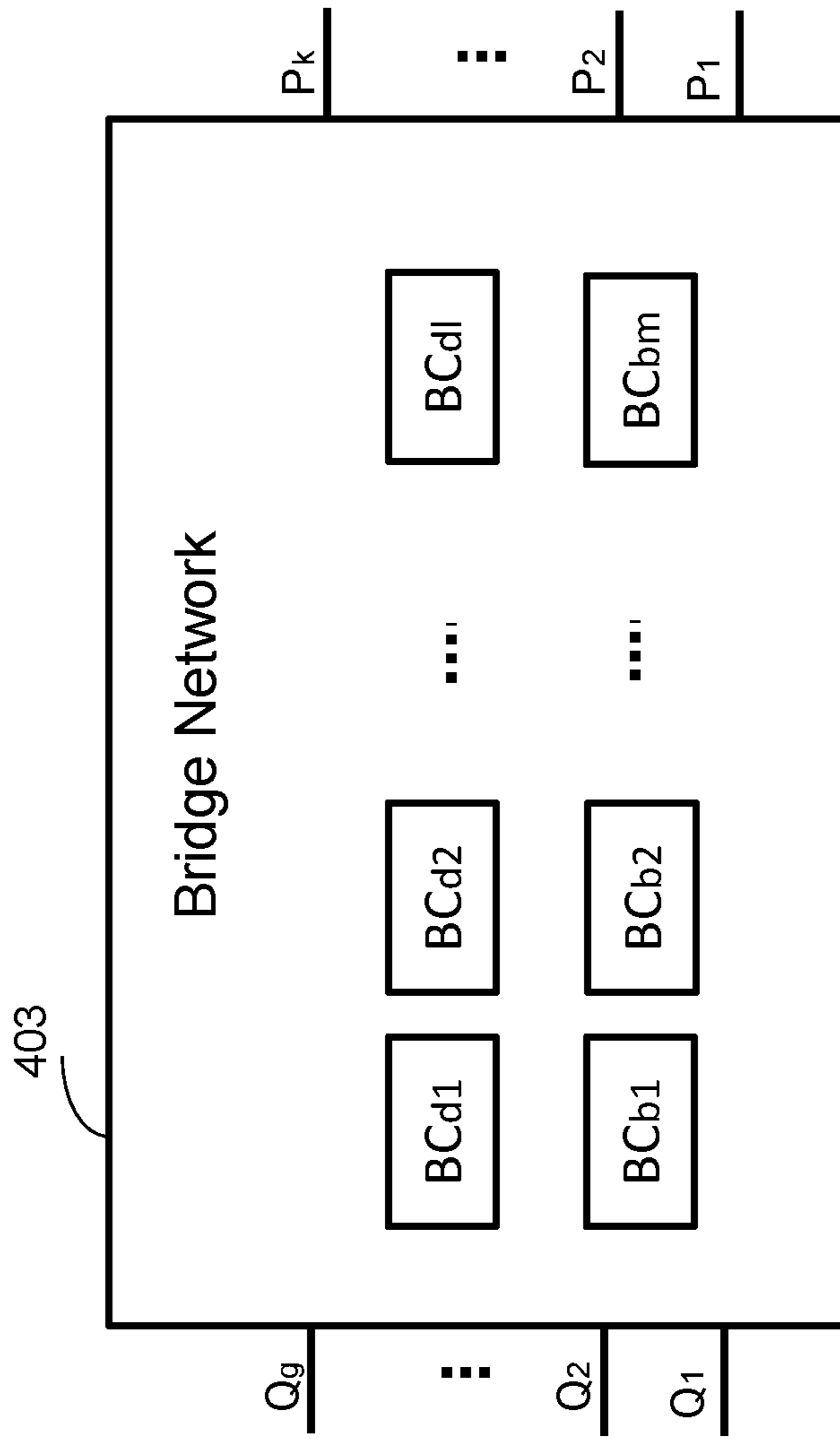


Fig. 4

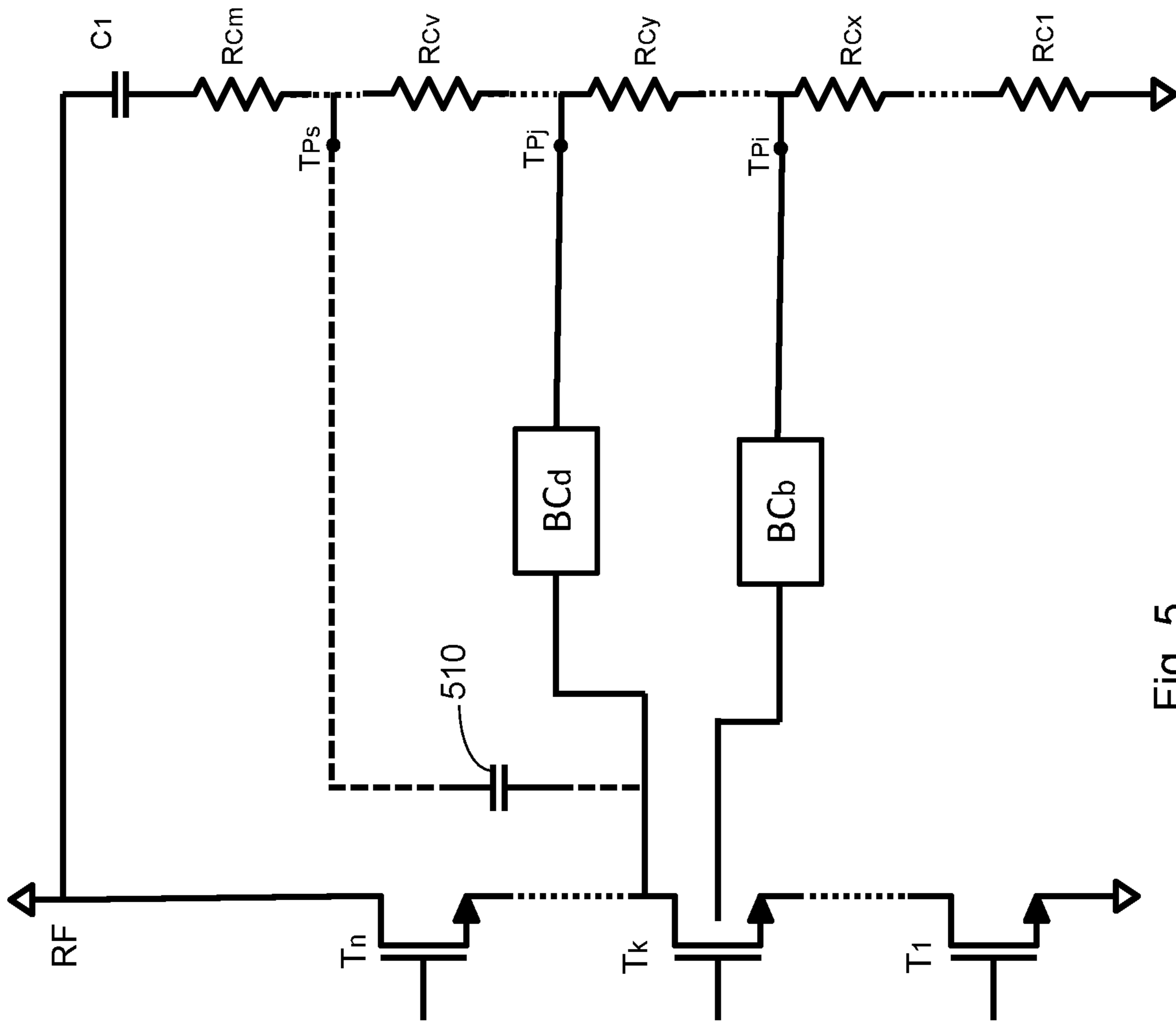


Fig. 5

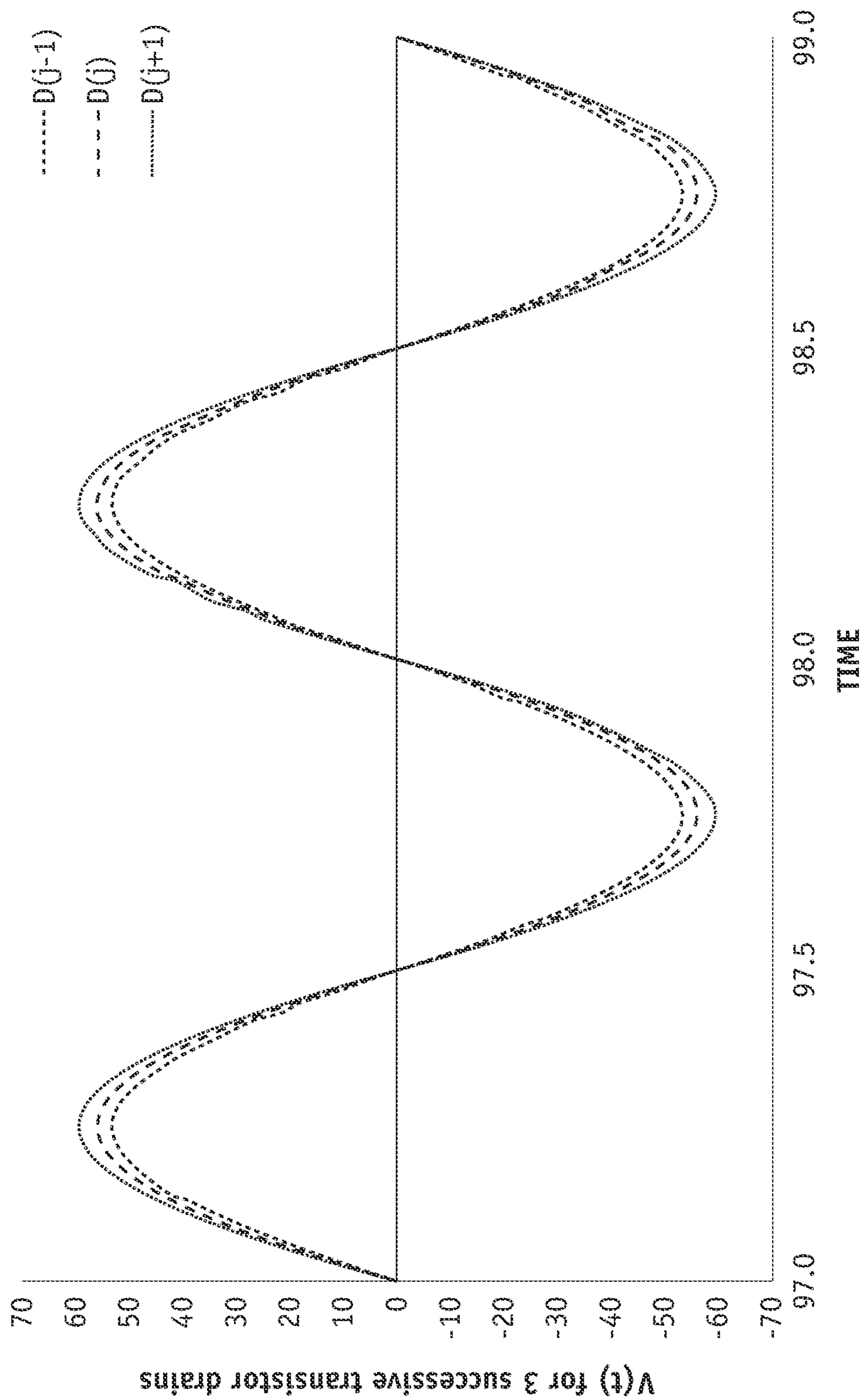


FIG. 6A

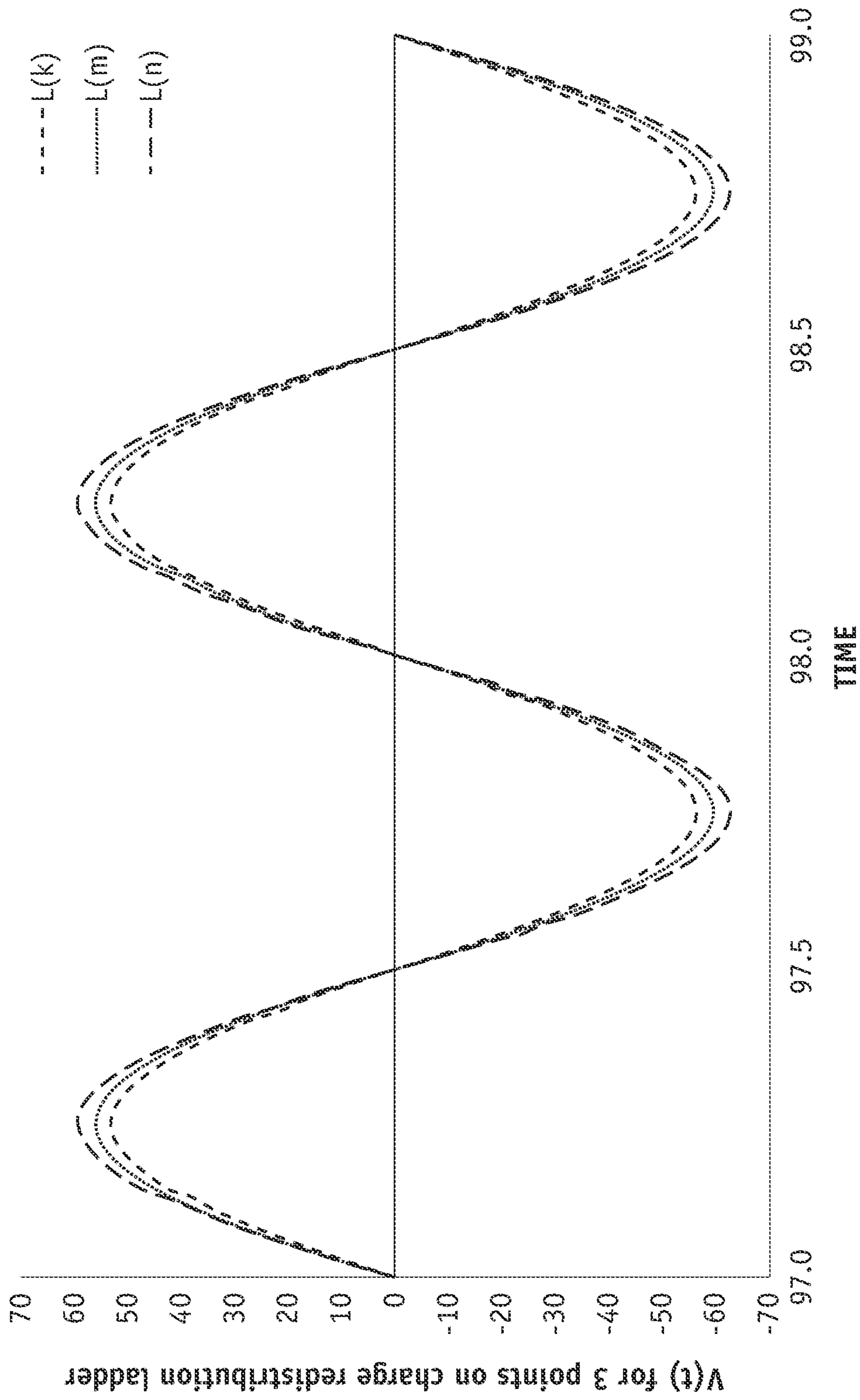


FIG. 6B

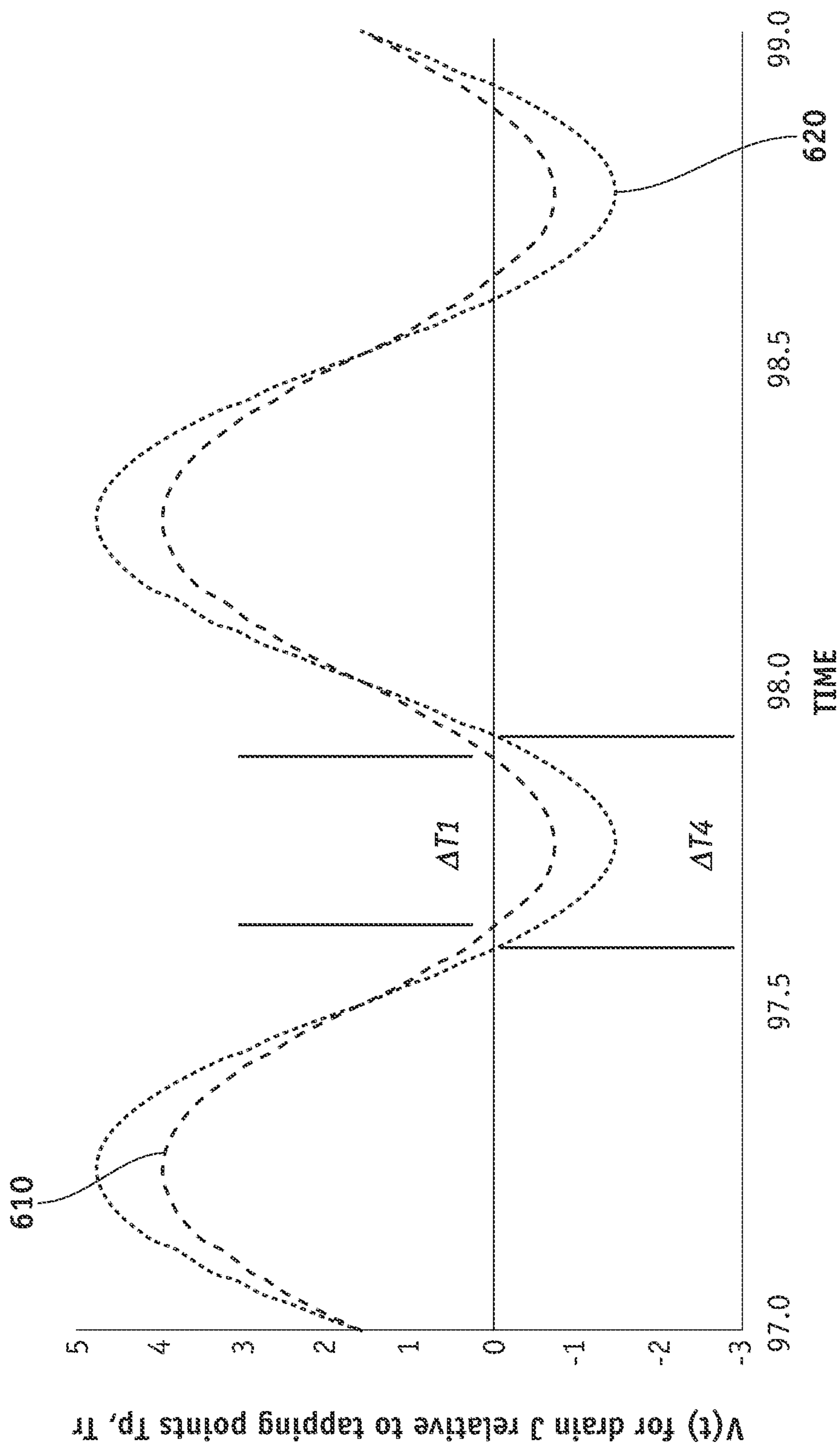


FIG. 6C

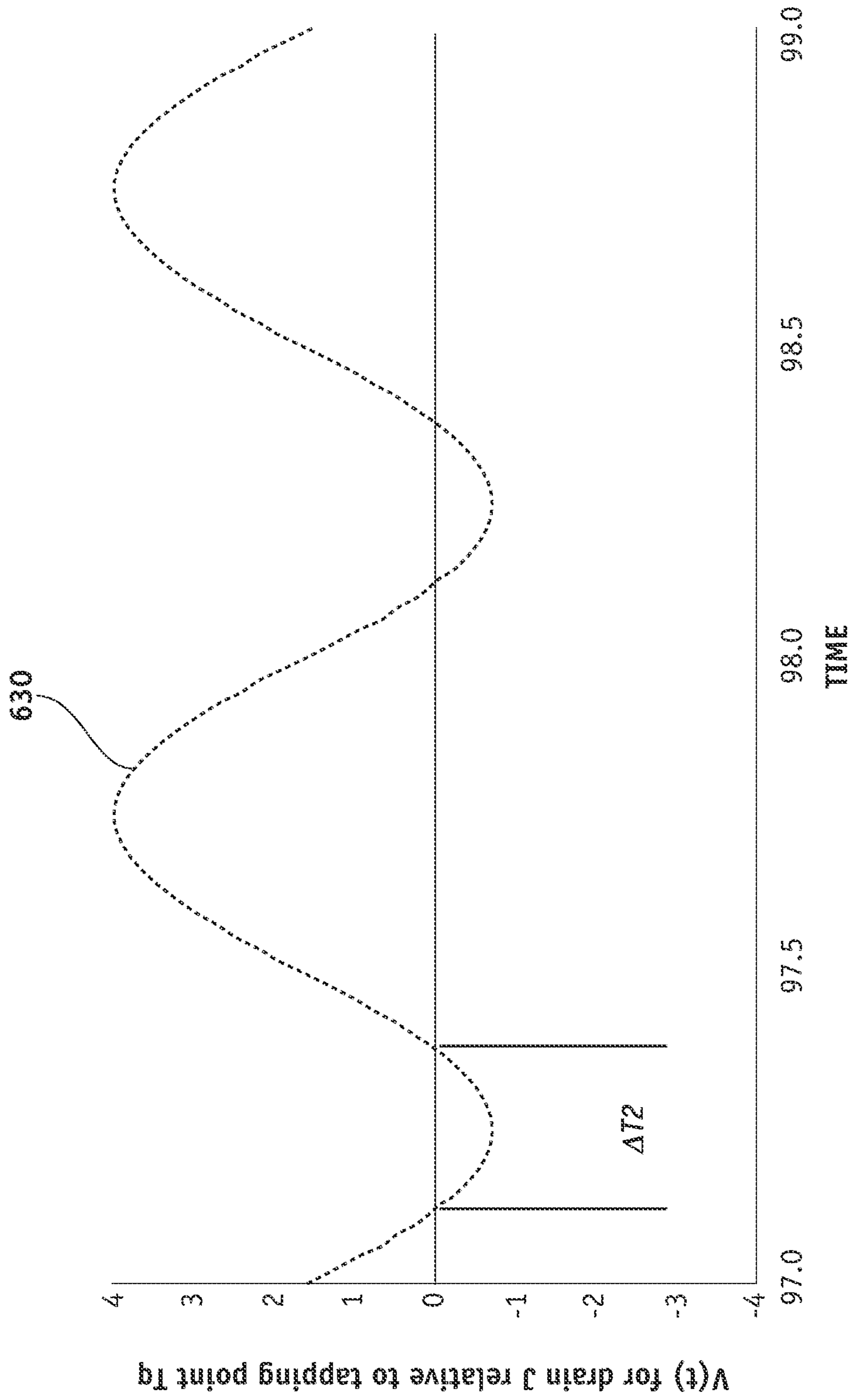


FIG. 6D

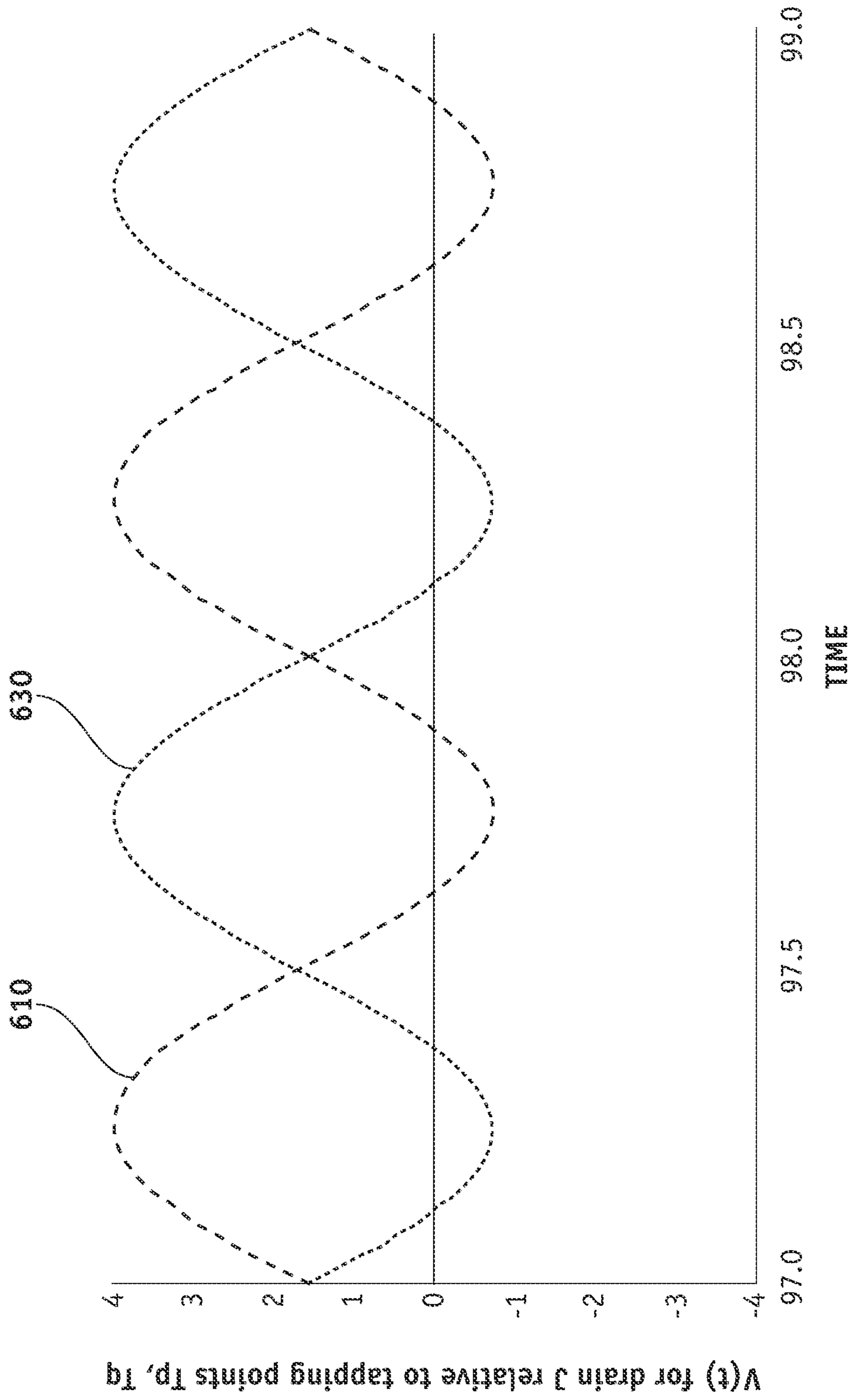


FIG. 6E

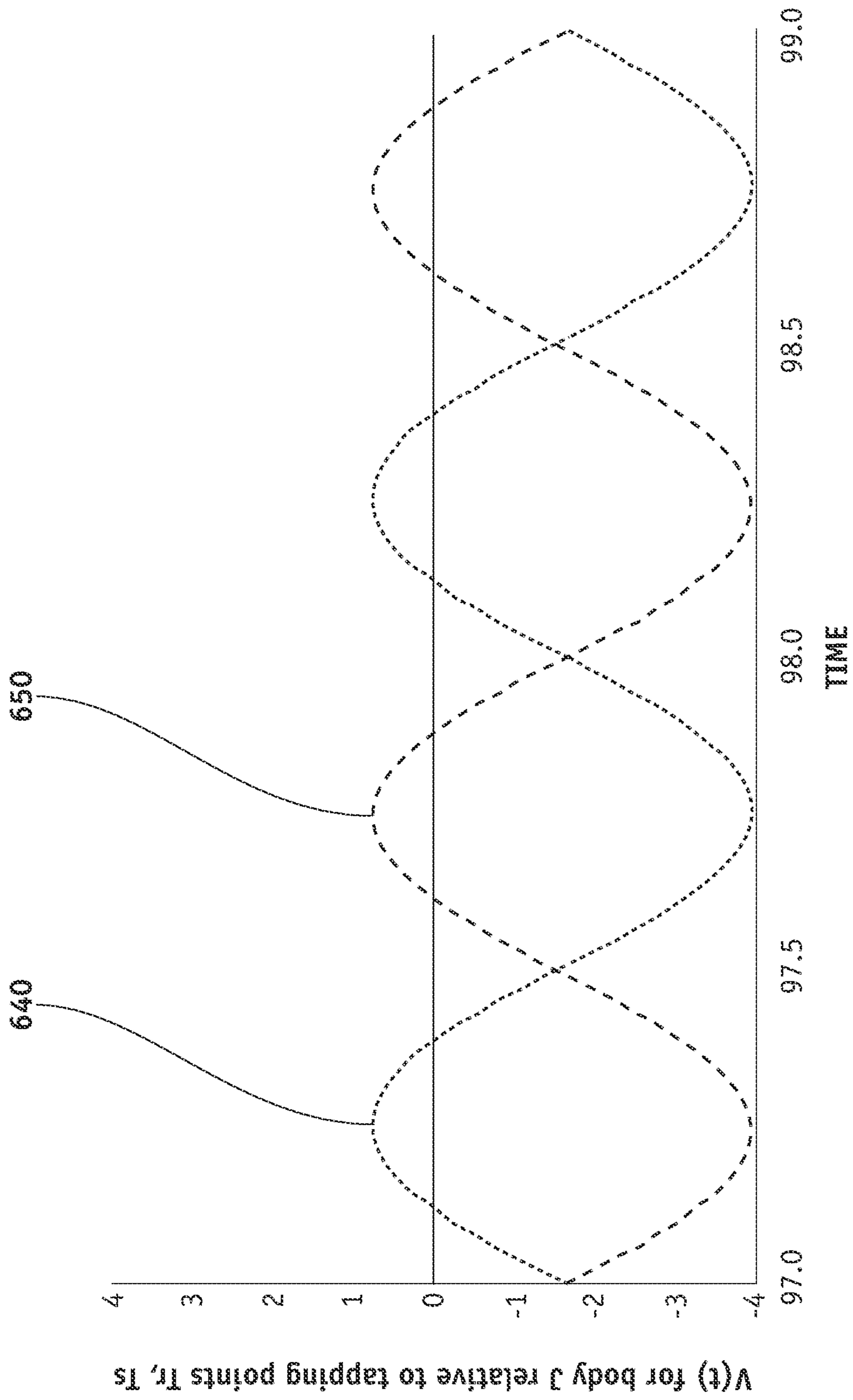


FIG. 6F

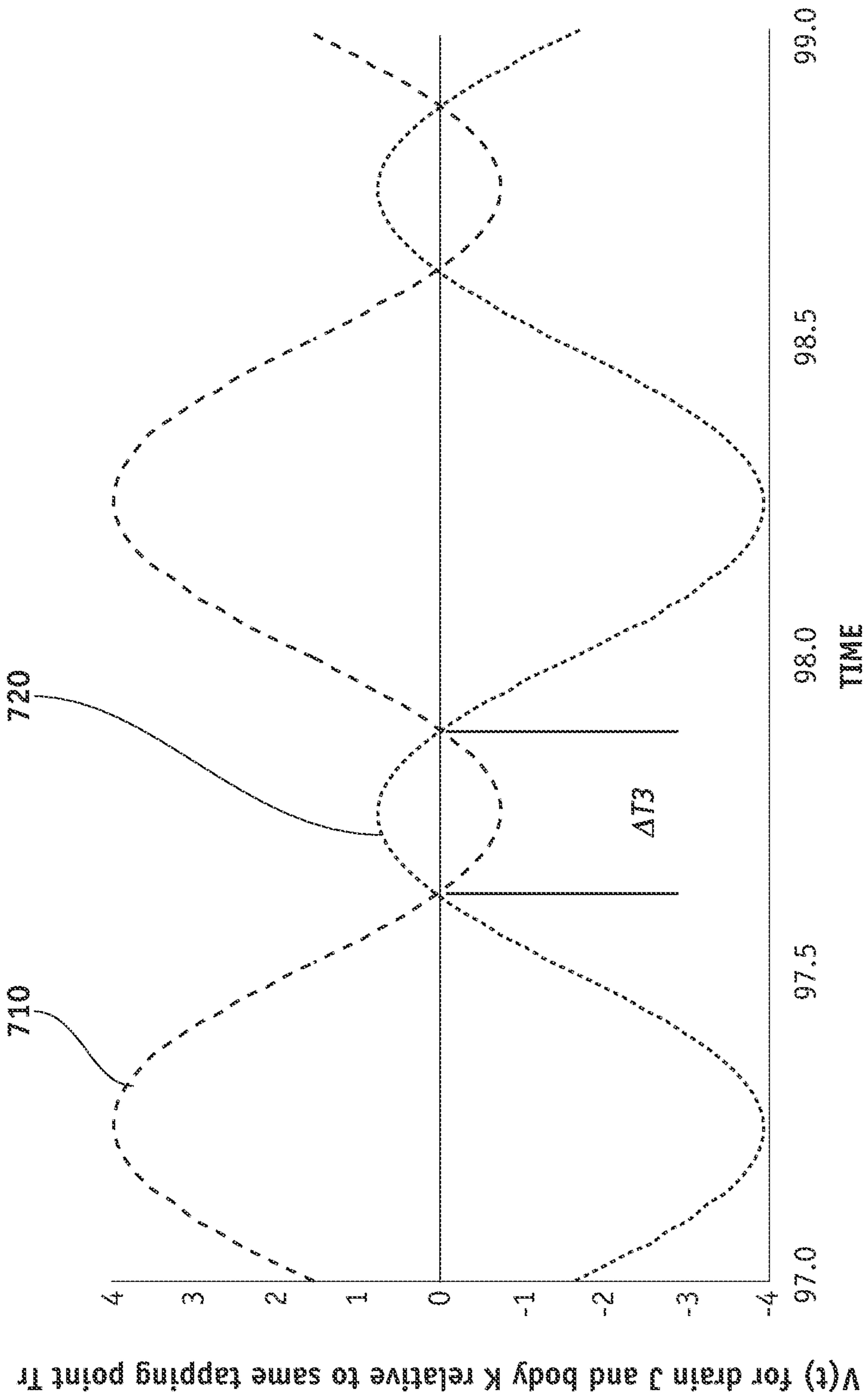


FIG. 7A

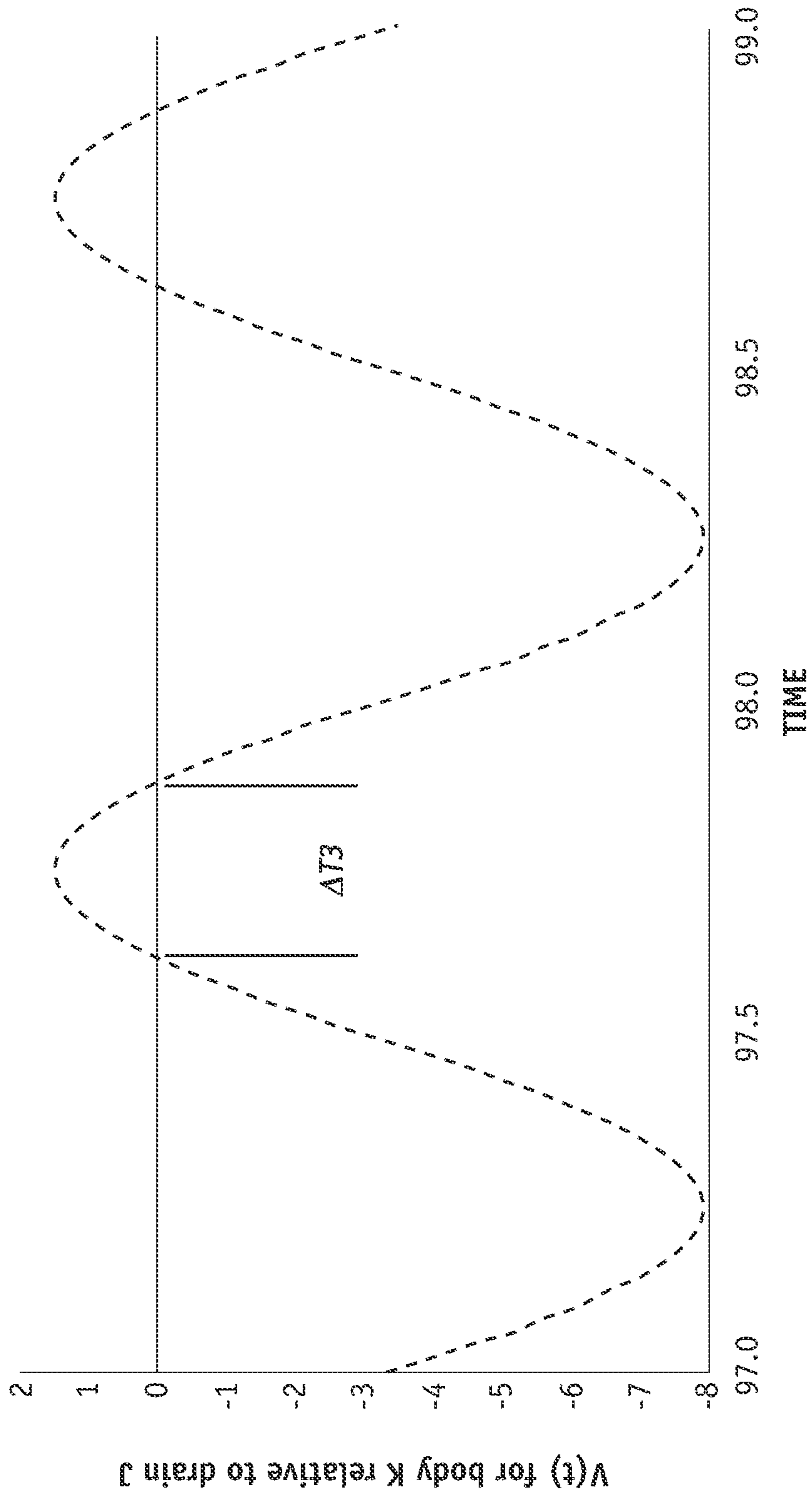
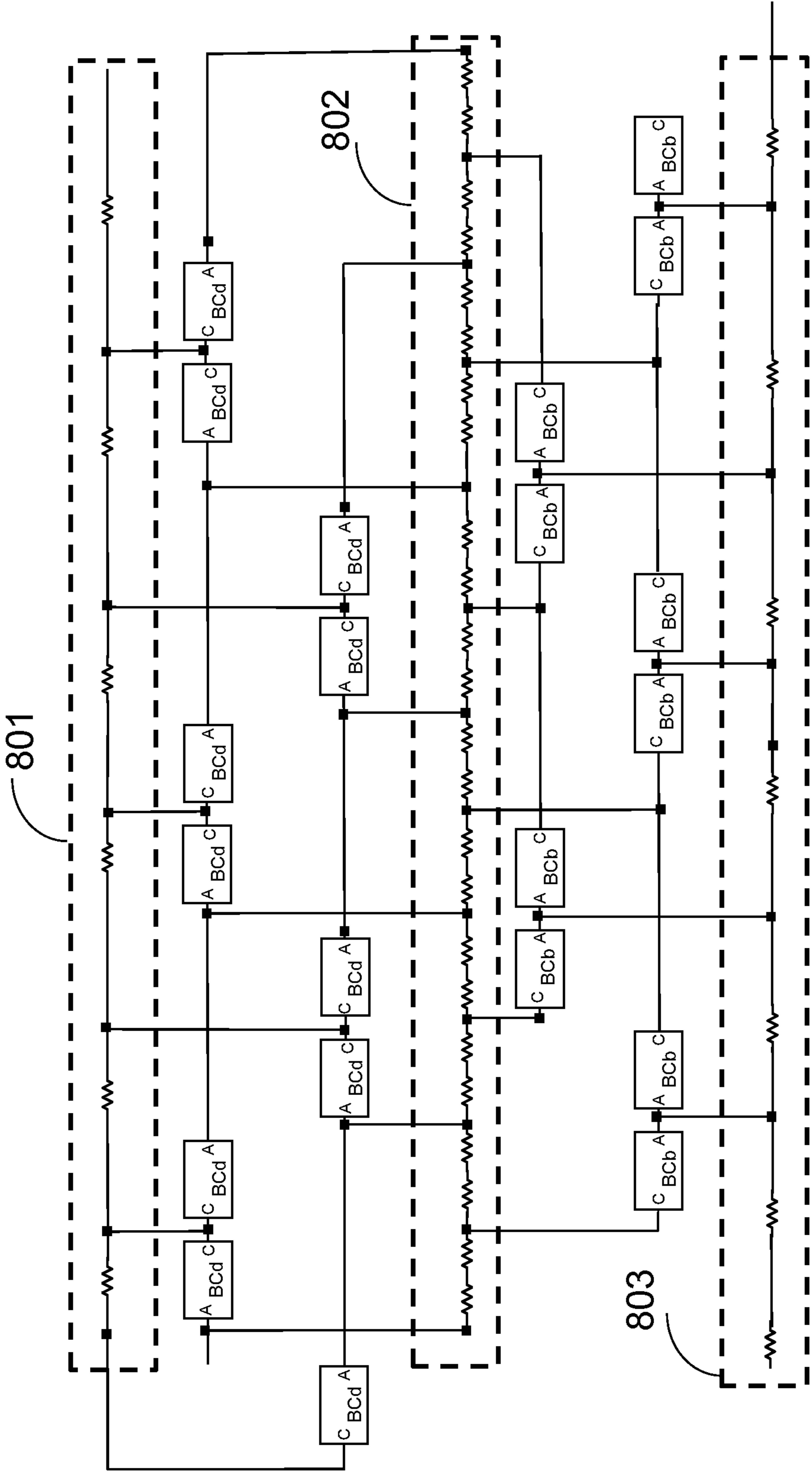


FIG. 7B



800

Fig. 8A

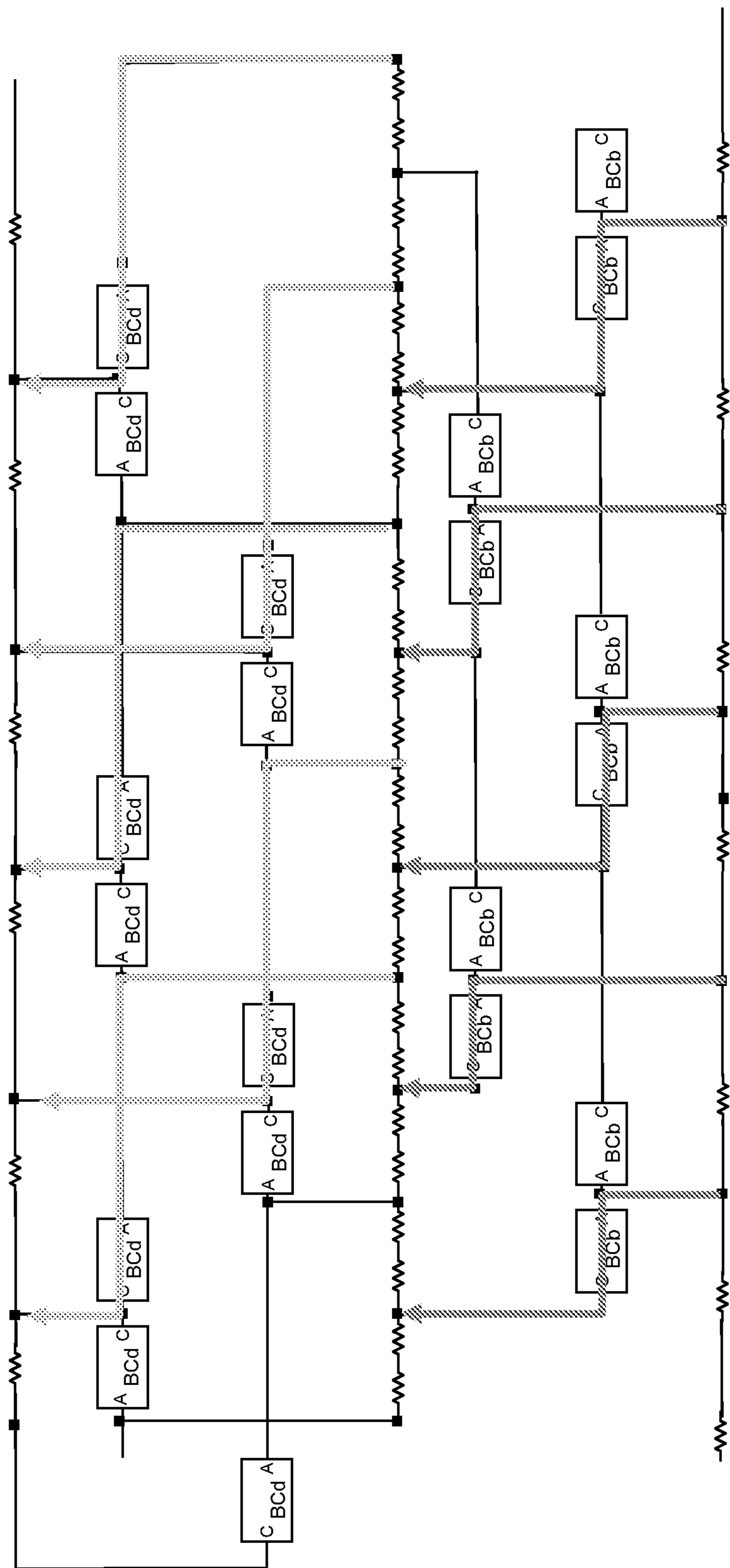


Fig. 8B

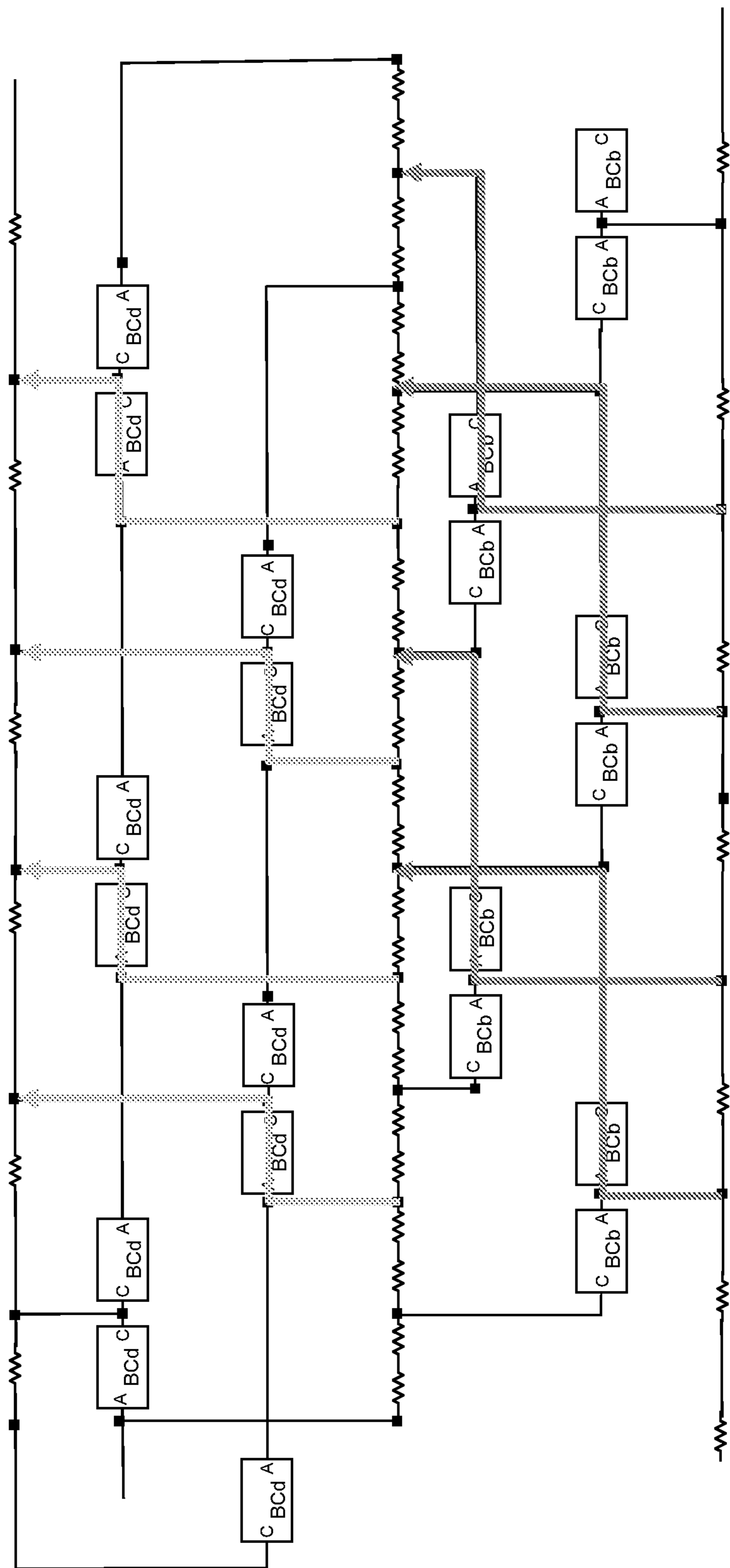


Fig. 8C

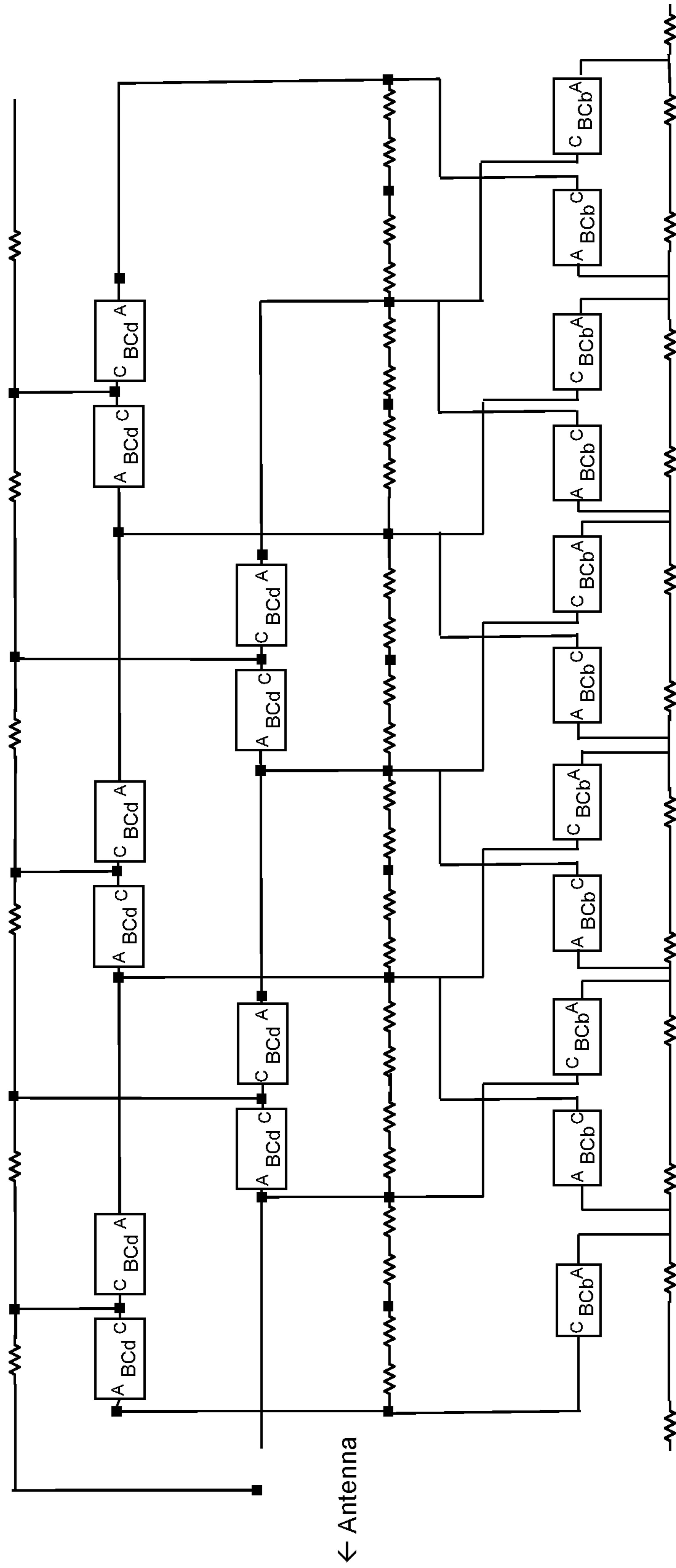


Fig. 8D

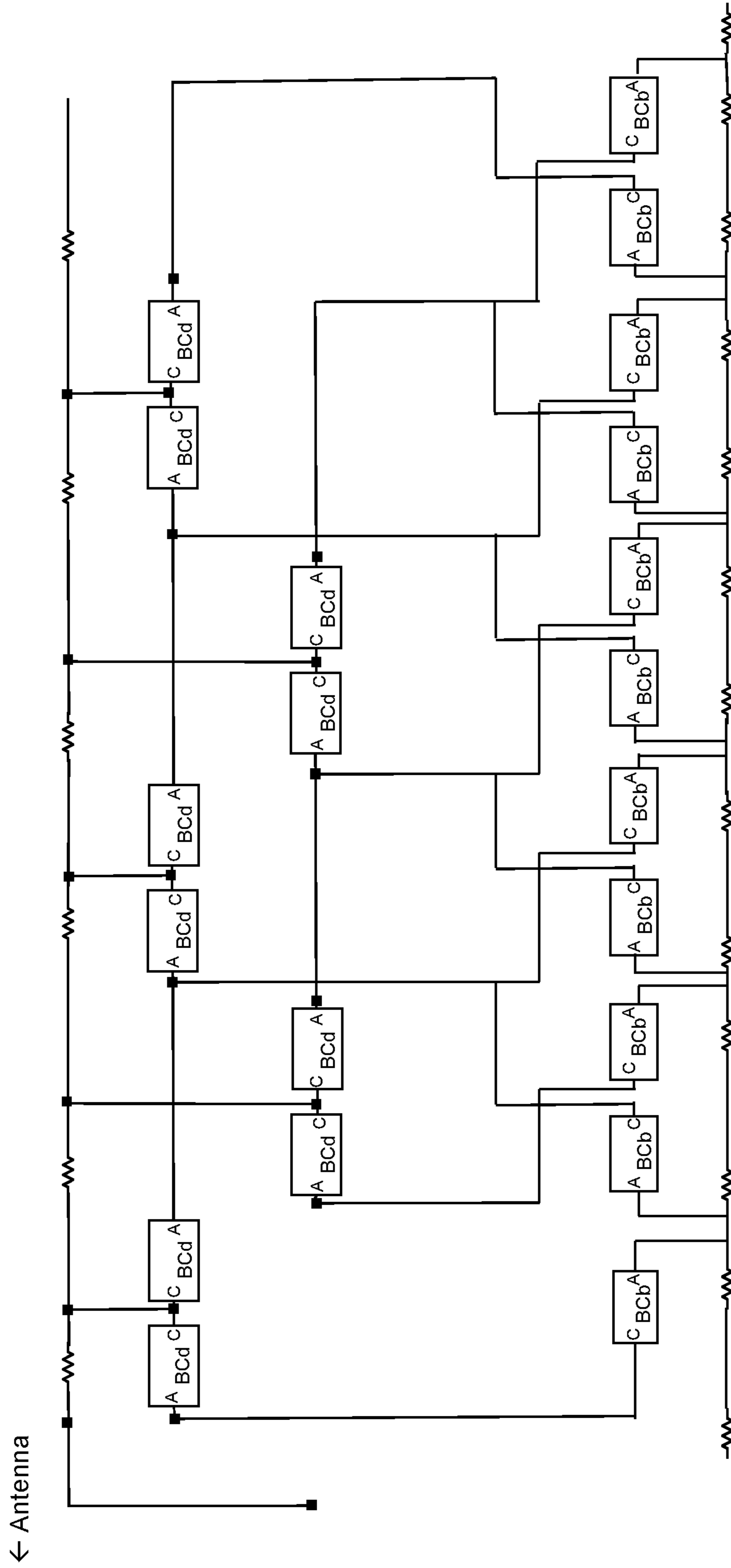


Fig. 8E

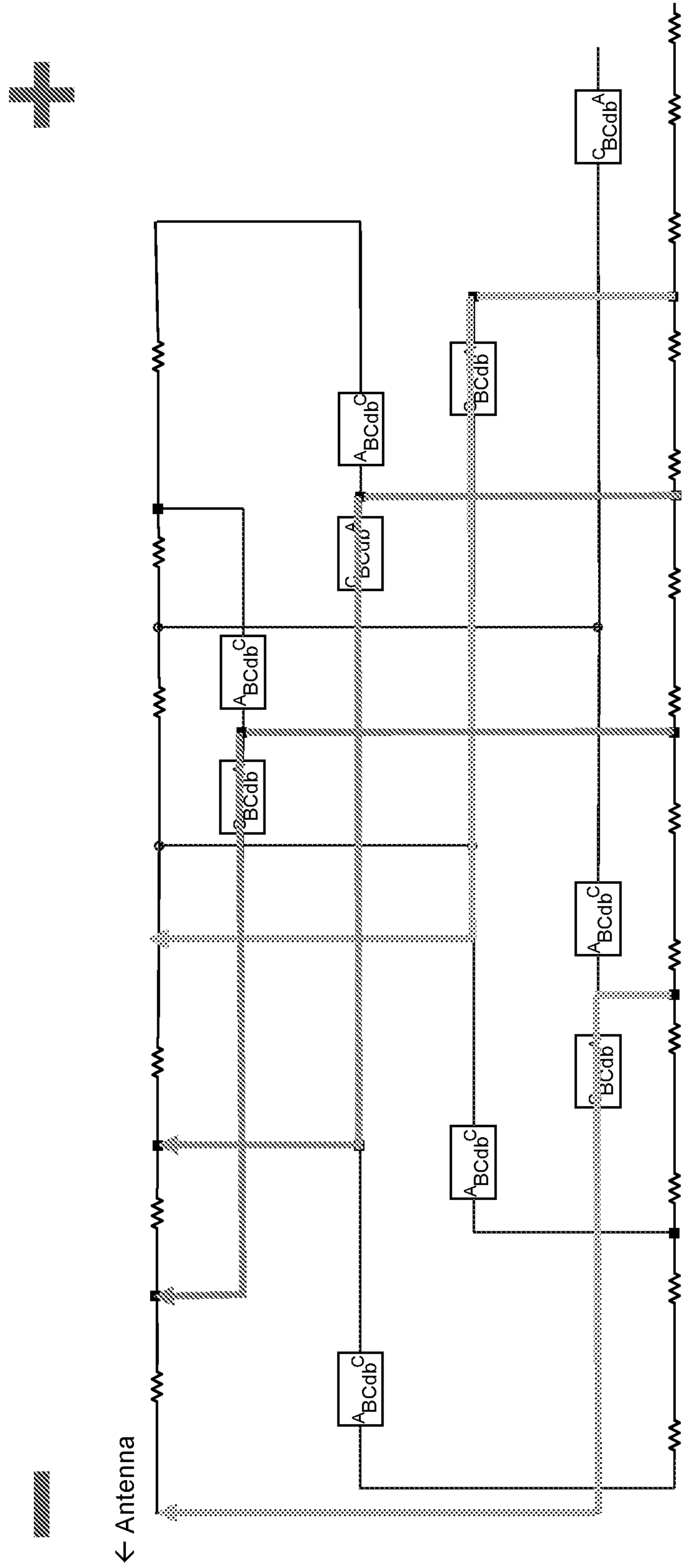


Fig. 8G

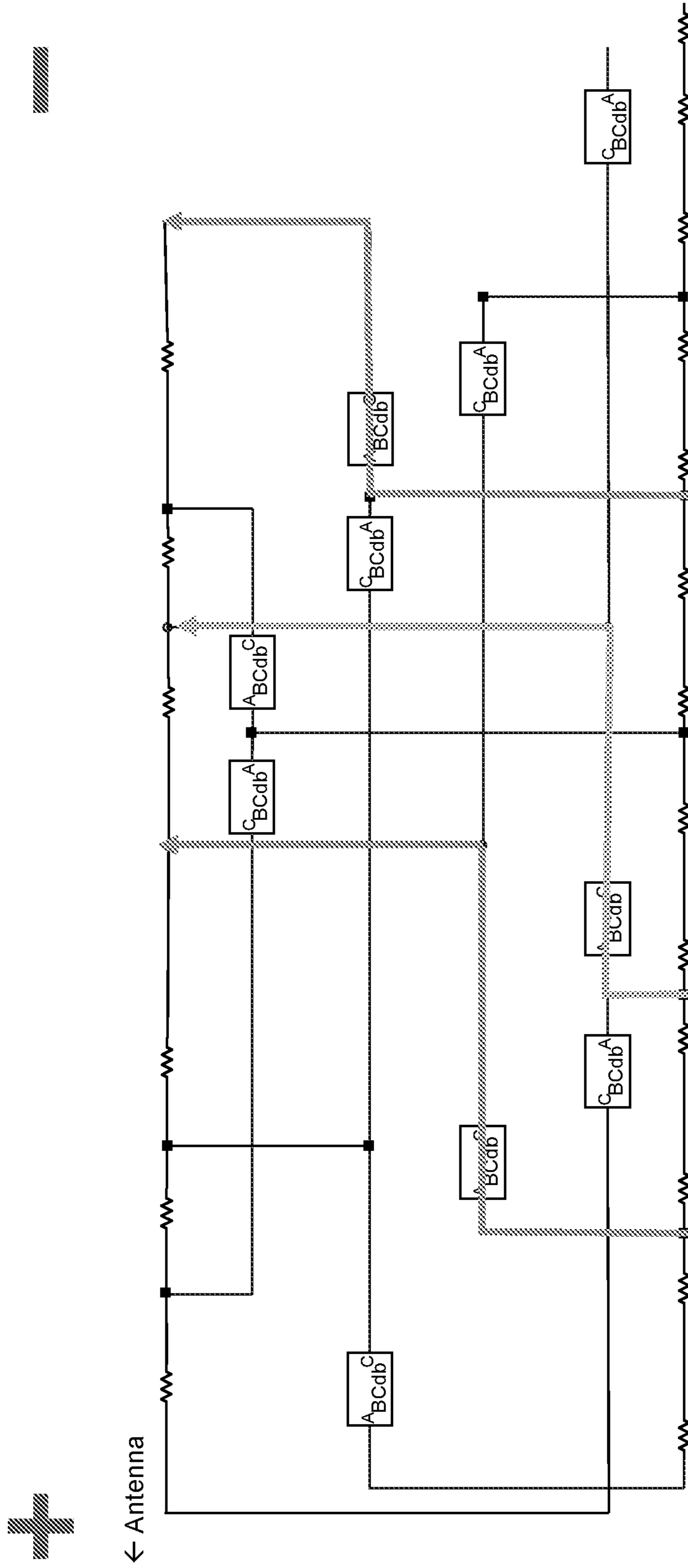


Fig. 8H

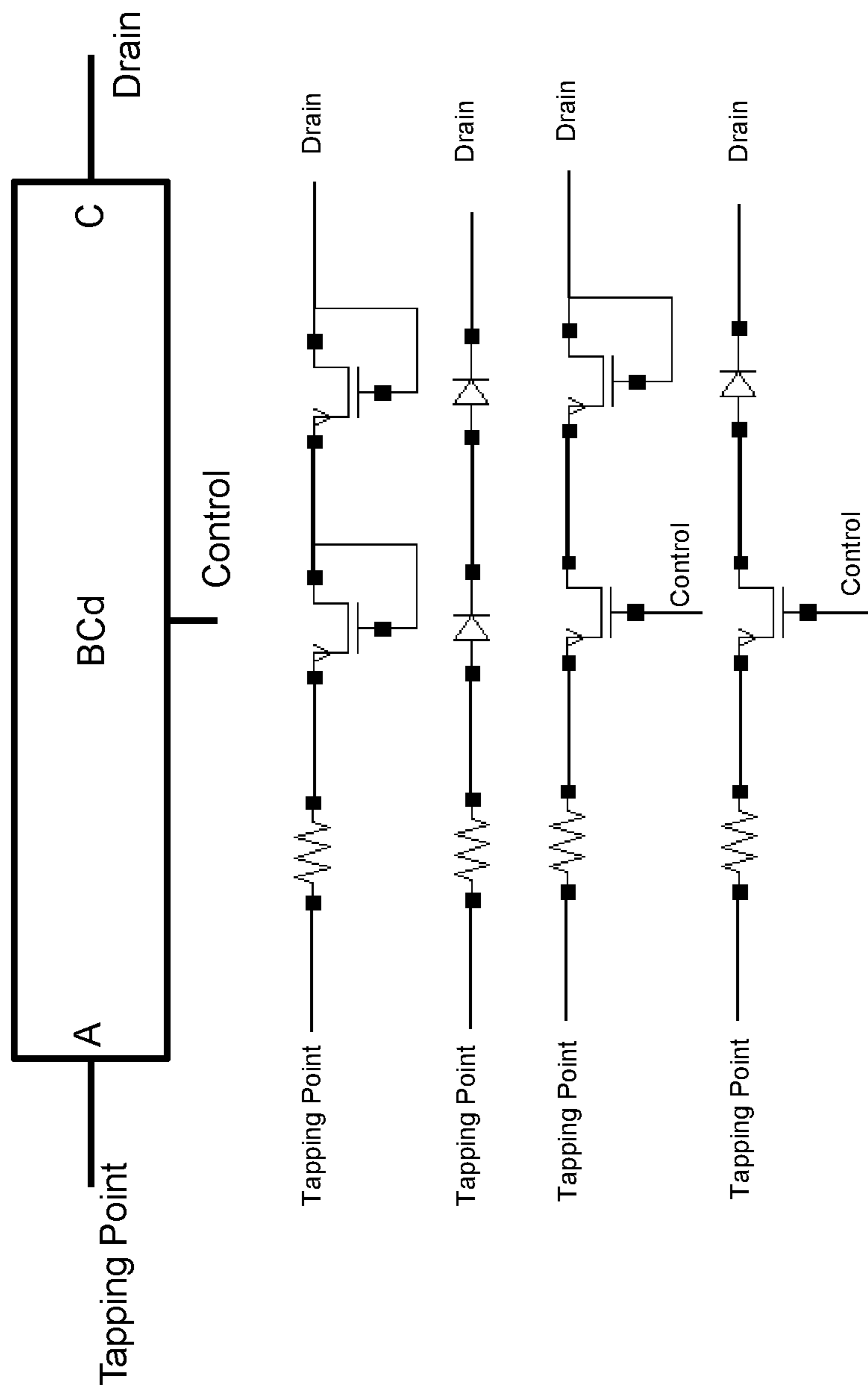


Fig. 9A

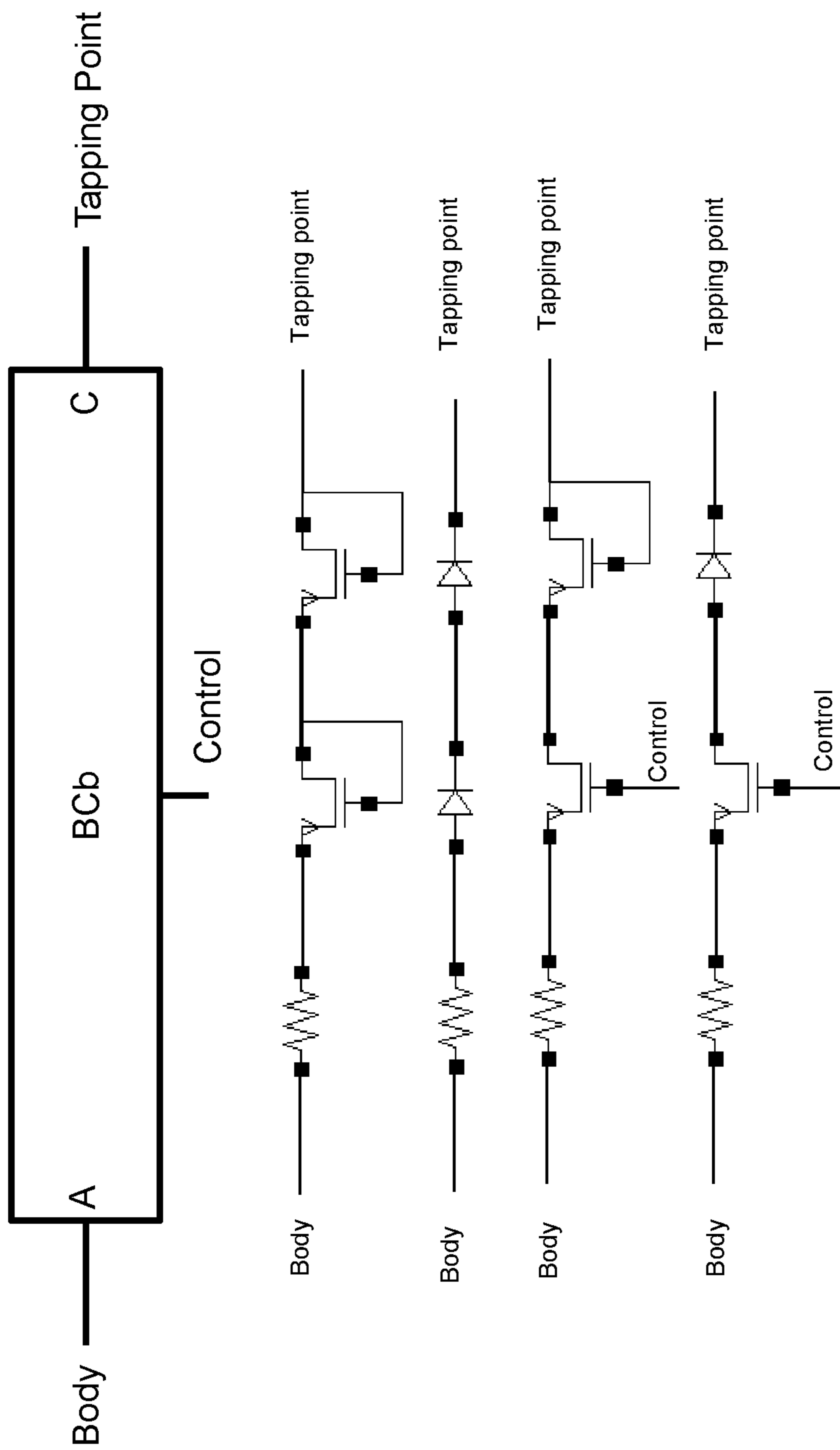


Fig. 9B

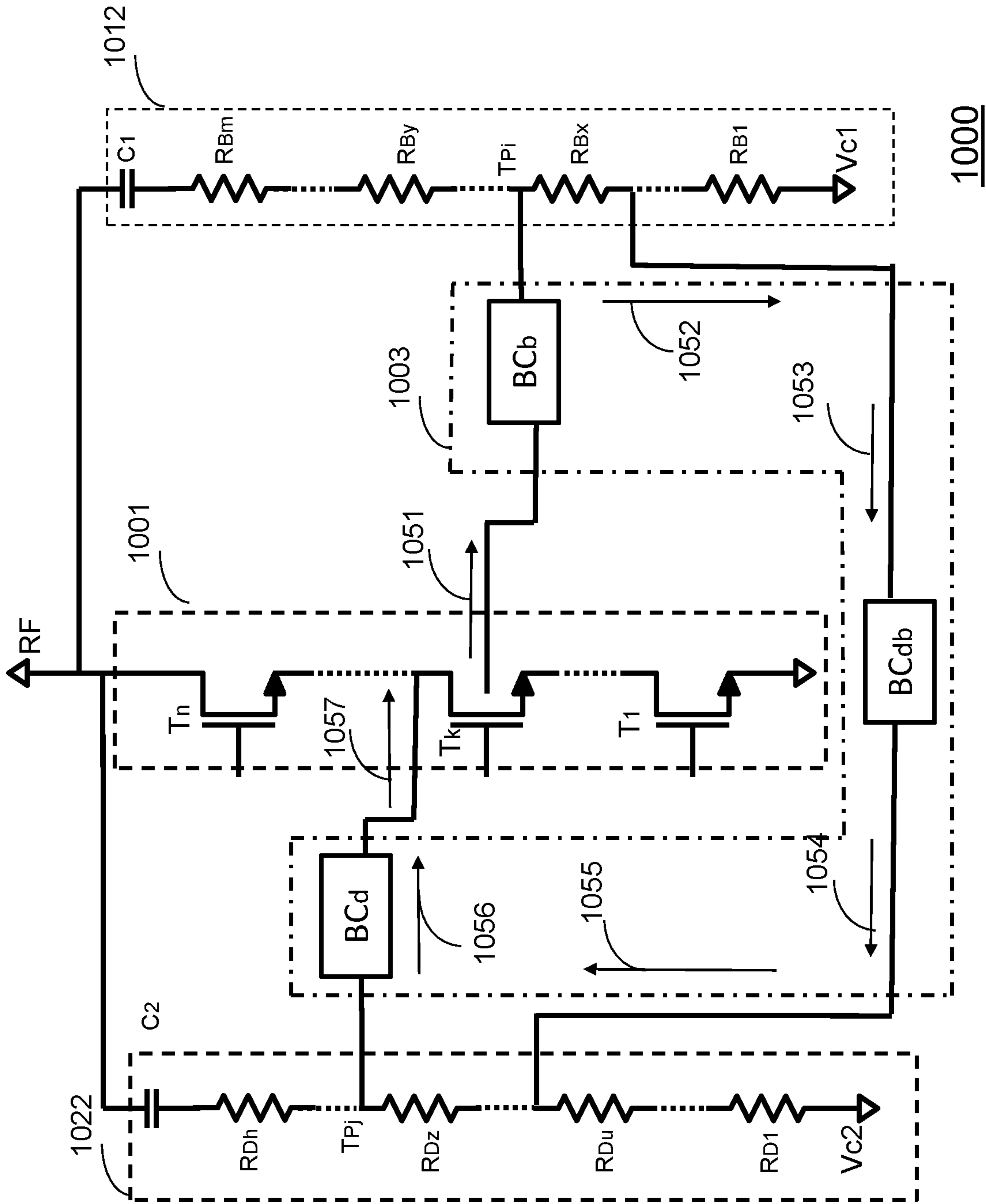


Fig. 10

RF SWITCH STACK WITH CHARGE REDISTRIBUTION

CROSS-REFERENCE TO RELATED APPLICATIONS

The present U.S. patent application Ser. No. 18/161,802, filed on Jan. 30, 2023 is a continuation of U.S. patent application Ser. No. 17/119,840, filed on Dec. 11, 2020, entitled “RE Switch Stack With Charge Redistribution”, which is now U.S. Pat. No. 11,601,126 issued on Mar. 7, 2023, which is incorporated herein by reference in its entirety. The present application may be related to U.S. Pat. No. 10,236,872 B1, filed on Mar. 28, 2018, issued on Mar. 19, 2019, and entitled “AC Coupling Modules For Bias Ladders”, incorporated herein by reference in its entirety. The present application may be also related to U.S. patent application Ser. No. 16/902,032 filed on Jun. 16, 2020, entitled “RF Switch Stack With Charge Control Elements”, also incorporated herein by reference in its entirety.

FIELD

The present disclosure is related to Radio Frequency (RF) switch stacks, and more particularly to methods for designing RF switch stacks including charge redistribution arrangements and related apparatus.

BACKGROUND

When designing communication systems, RF switches are generally implemented in stacked configuration due to the large RF power handling requirement of such switch stacks. FIG. 1A shows a prior art field effect transistor (FET) switch stack (100) including a series arrangement of transistors (T_1, \dots, T_4) arranged in a shunt configuration. As may be the case, the FET switch stack (100) is biased using a gate resistive ladder including gate resistors (R_{G1}, \dots, R_{G4}), a body resistive ladder including body resistors (R_{B1}, \dots, R_{B4}), and a drain-source resistive ladder including drain-source resistors (R_{DS1}, \dots, R_{DS4}).

In typical operative conditions, and when the transistors are in the ON state, the gate of each transistor may be biased at a positive voltage (e.g. +3V) larger than the threshold voltage of the corresponding transistor, and the drain/source/body of the same transistor may be biased at 0V. When the FET switch stack is in the OFF state, the drain/source of each transistor may be biased at 0V and the gate and body of each transistor may be biased at a negative voltage (e.g. -3V). As shown in FIG. 1A, the top end of the drain-source resistive ladder is connected to the antenna or other RF port (RF path), which is essentially a direct current (DC) ground, and the bottom end of the same ladder is connected to ground in both the ON and OFF states in case of a shunt configuration like the one shown in FIG. 1A. On the other hand, the bottom end would be connected to a bottom RF node or terminal in case of a series configuration. As such, and in an ideal/desired situation, when the FET switch stack is in the OFF state, the drain-source ladder would not draw any current, or a negligible current, meaning that the drain of each of the transistors (T_1, \dots, T_4) would experience the same DC voltage of approximately 0V.

When a large RF voltage is applied to the antenna, the FET switch stack (100), the drain-source resistive ladder, the gate resistive ladder and the body resistive ladder are all designed to distribute the RF voltage evenly among the FET switch stack (100). The RF signal, having no DC compo-

nent, does not directly change the DC voltage at any point in the stack. However, during operation, there may be some currents generated within the transistors due to the RF signal applied, which may alter the DC voltage distribution. The RF signal at each point is superimposed on the existing DC voltage. When the FET switch stack (100) is in the “OFF” or non-conducting state, the FET switch stack (100) is designed to conduct no real component of current, which is current in phase with the RF voltage applied. The transistor stack appears as a purely capacitive impedance due to the series gate-drain capacitor C_{gd} , gate-source capacitor C_{gs} , plus an additional inherent capacitance between drain and source of each of the transistors (T_1, \dots, T_4). In the OFF state, the transistors will pass no real current with RF voltage applied across drain to source of the transistors as long as the magnitude of the RF voltage across each transistor is below a critical value (V_{peak}). If the RF voltage exceeds such value, the transistor will fail or “break down” and start conducting real current. The value of V_{peak} for each transistor is a function of the relative DC voltages between the drain/source DC voltage and the gate DC voltage. The more negative the gate voltage relative to the drain/source voltage, the higher the value of V_{peak} . The body DC voltage can also have an impact if it is beyond a certain range, although such impact is generally lower.

Since the maximum voltage each transistor (T_1, \dots, T_4) in the stack can “block” before breaking down is dependent on the amount of negative DC voltage differential between the gate and drain/source terminals, it may be desirable to make the gate terminal appear more negative relative to the drain/source voltage to increase this blocking voltage. This can be accomplished by making the drain/source terminals more positive and/or making the gate terminals more negative.

There may be cases in implementations of switch stacks where it is difficult, inconvenient or impossible to apply the desired DC voltages to every transistor in the stack. One example is if it is too costly to include circuitry that can bias the gate terminals negative relative to the drain/source terminals. Another example would be if it is advantageous to have different DC voltage levels for different transistors in the stack because some transistors may need to block more voltage than others. A third example would be if there are undesirable DC currents being generated within the stack that disturbs the externally applied voltage in a uniform or non-uniform manner. Using the example of leakage current in transistor stacks, the above-mentioned points are further clarified.

In practical conditions, more in particular in stacked switches experiencing large RF swings during the OFF state, each transistor within the stack will generate an undesired leakage current that flows from the drain/source to the body of the transistor. Such generated current is referred to as “Ibody” throughout this document. With reference to FIG. 1A, arrows ($ib1, \dots, ib4$) indicate the body currents, each flowing from the body of the corresponding transistor down through the body resistive ladder and sinking into the power supply (V_B). Moreover, and as indicated by arrows ($id1, \dots, id4$), current will flow from the antenna (DC ground) and ground through the drain-source resistive ladder and to the drain-sources of the transistors within the stack. It is pointed out that as the drain-source resistive ladder is connected at both ends to ground, the current flowing in such ladder may follow different directions, downward or upward as indicated by the arrows ($id1, \dots, id4$), and depending on the location of the current within the drain-source resistive ladder.

As a result of what has been described above, the flow of the unwanted leakage current, I_{body} , throughout the switch stack, modifies the DC voltage distribution across such switch stack. In other words, various switch stack nodes will experience undesired DC bias voltages different from what the biasing circuit would have provided to such nodes in the absence of such leakage current. Throughout the disclosure, the undesired effect of the body leakage current on the DC bias voltage distribution throughout the stack is referred to as the “de-biasing” effect.

With further reference to FIG. 1A, the leakage current flowing from the body to the power supply (V_B) will result in voltage drops across the resistors of the body resistive ladder, and as a result, the body of each of the transistors will experience a less negative voltage compared to the ideal/desired case with no leakage current. With the gate and the body resistive ladders being distinct, gate voltages will also not be impacted by the leakage current circulation across the FET switch stack. On the other hand, the flow of the leakage current from DC grounds to drain/sources of the transistors generates voltage drops across the resistors of the drain-source resistive ladder and as a result, the drain/source of the transistors will experience more negative voltages compared to the ideal/desired case of 0V DC. With the gate voltage remaining the same (e.g. -3V), this means that the gate-source voltages will be less negative compared to the ideal/desired scenario, resulting a degradation of power handling of the transistors. In what follows, this point will be further clarified using a numerical example.

FIGS. 1B-1C each show the FET switch stack (100) of FIG. 1A wherein, in the OFF state, the gate and the body resistive ladders are both biased, for example, with a negative DC voltage of -3V and the drain-source resistive ladder is connected to DC ground through the ports.

FIG. 1B represents the ideal/desired situation where it is assumed there is no body leakage current. As can be seen in FIG. 1B, the drains of all the transistors are all biased at 0V, the gates and the bodies are all at -3V and there is practically no DC current flowing through the resistive ladders. This is the ideal/desired scenario.

I_{body} exists because of the peak difference in potential between drain to gate. Carriers are generated from the peak voltage. Holes exit through the body, electrons exit through the drain/source. Although generation is pulsed, it is filtered by the resistances and capacitances on the way out. On the other hand, FIG. 1C shows how the DC voltage distribution across the stack is changed resulting in the flow of the leakage current within the switch stack. For example, the drains of the transistors (T_1, \dots, T_4) are now experiencing DC voltages of (-0.2V, -0.4V, -0.2V, 0V) respectively, instead of all sitting at the desired DC voltage of 0V as indicated in FIG. 1B. As further shown in FIG. 1C, the middle transistors experience the most change in drain voltage due to the flow of I_{body} from top and bottom of the drain-source ladder towards the center of the ladder.

Continuing with the same example, and as for the body voltages, the bodies of the transistors (T_1, \dots, T_4) may experience voltages of (-2.6V, -2.2V, -1.9V, -1.5V) instead of all being at the desired voltage of -3V. This is further illustrated by the curves (101, 102) of FIG. 2, representing exemplary DC average voltage profiles for drains and bodies of the transistors of a switch stack respectively, plotted with reference to the position of the transistors in the stack (bottom position to the right, top position to the left). As can be noticed from graph (101) and as mentioned previously, the transistor in the middle of the stack experiences the most deviation in DC drain voltage compared to the ideal/desired

scenario, due to the flow of the undesired current “ I_{body} ” within the drain-source resistor ladder. As for the bodies of the transistors, the deviation from the desired voltages is larger for the transistors located closer to the top of the stack, as illustrated by graph (102) of FIG. 2.

One way to reduce the undesired voltage drops across the bias resistors as described above is to reduce all of the biasing resistors values. This comes at the expense of an overall circuit performance degradation. Firstly, as a result of implementing smaller biasing resistances, the equivalent resistance of the switch stack in the OFF state (R_{off}) will be smaller. This will result in a degradation of the Quality factor (Q) of the circuit. In other words, there is a tradeoff between the power handling of the switch stack and overall system performance parameters such as Q, such tradeoff imposing challenges when designing switch stacks as part of RF communication systems.

SUMMARY

As mentioned above, undesired currents generated in switch stacks during operative conditions, more in particular when such switch stacks are in the OFF state, may alter the balance of a desired DC voltage distribution across the switch stack. There is a need for an effective and practical solution to undo such undesired effects on the voltage distribution.

With continued reference to the body leakage current case as mentioned above, there are two issues associated with the presence of the body leakage current, I_{body} , when FET switch stacks are in OFF state:

1. Leakage current generation issue: the negative power supply is required to generate and handle such current circulating within the switch. This current is much larger compared to the near zero current in the ideal/desired scenario where the leakage current would not have been present. This results in a more expensive design, at least from the standpoint of the required space on the chip.
2. Bias voltage distribution issue: the flow of the body leakage current changes the voltage distribution across the stack causing reduced power handling capability for the transistors within the switch stack.

Methods and devices described in the present disclosure address both the generation issue and the distribution issue as described above. As will be detailed later, the disclosed methods and devices allow the biasing resistor values in a FET switch stack to be increased by providing some local charge support at specific points in such switch stacks. According to various embodiments of the present disclosure, this may be performed by redistributing charges through the body and/or drain-source charge redistribution resistive ladders.

According to a first aspect, a field effect transistor (FET) switch stack circuit comprising: a stacked configuration of series-connected FET transistors coupled to a radio frequency (RF) terminal; a charge redistribution resistive ladder coupled to the RF terminal, the charge redistribution resistive ladder comprising series-connected charge redistribution resistors and tapping points; and a drain/source bridge network configured to selectively couple/decouple a first set of one or more tapping points on the charge redistribution resistive ladder with/from drain or source terminals of the FET transistors and a body bridge network configured to selectively couple/decouple a second set of one or more tapping points on the charge redistribution resistive ladder with/from body terminals of the FET tran-

sistors, wherein, when the FET switch stack is in OFF state: the FET switch stack is configured to be coupled to an RF signal at the RF terminal, and to distribute RF voltages at the tapping points; and during a first portion of a period of the RF signal, the drain/source bridge network couples the first set of one or more tapping points to the drain or source terminals of the FET transistors and the body bridge network couples the second set of one or more tapping points to the body terminals of the FET transistors.

According to a second aspect, a field effect transistor (FET) switch stack circuit is described, comprising: i) a stacked configuration of series-connected FET transistors; ii) a drain/source charge redistribution resistive ladder comprising series-connected drain/source charge redistribution resistors and a set of one or more drain/source tapping points in correspondence with drains or sources of FET transistors of the series-connected FET transistors; iii) a body charge redistribution resistive ladder comprising series-connected body charge redistribution resistors and a set of one or more body tapping points in correspondence with bodies of FET transistors of the series-connected FET transistors; and iv) a drain-body bridge network configured to selectively couple/decouple the set of one or more drain/source tapping points with/from the set of one or more body tapping points, thus selectively coupling/decoupling drains or sources of the FET transistors with/from bodies of the FET transistors to redistribute charges throughout the FET transistors.

According to a third aspect, a radio frequency (RF) switch stack circuit is described, comprising: a stack of FET transistors connected in a series configuration and configured to be coupled to an antenna to receive an RF signal; a body resistive ladder comprising body resistors coupled to bodies of FET transistors of the stack of FET transistors; a drain-source resistive ladder comprising drain-source resistors coupled to drain/sources of FET transistors of the stack of FET transistors; a charge redistribution resistive ladder comprising charge transfer resistors and at least one tapping point; and a bridge network configured to selectively couple/decouple the at least one tapping point of the charge redistribution resistive ladder with/from the drain-sources and/or bodies of the transistors of the stack of transistors during a portion of a period of the RF signal in order to selectively source current from the charge redistribution resistive ladder and deliver said current to the drain-source resistive ladder and/or sink current from the body resistive ladder and deliver said current to the charge redistribution resistive ladder.

According to a fourth aspect, a method of adjusting FET switch stack bias when a FET switch stack is in OFF state, the method comprising: coupling a charge redistribution resistive ladder across the FET switch stack, the charge redistribution ladder comprising tapping points; applying an RF signal across the FET switch stack in the OFF state to generate voltages at the tapping points; during a first portion of the RF signal period, coupling a first tapping point to a drain/source terminal of a FET transistor of the FET switch stack, and coupling a second tapping point to a body terminal of the FET transistor of the FET switch stack, thereby pulling up a voltage of the drain/source terminal of the FET transistor and pulling down a voltage of the body terminal of the FET transistor.

Further aspects of the disclosure are provided in the description, drawings, and claims of the present application.

DESCRIPTION OF THE DRAWINGS

FIGS. 1A-1C show prior art FET switch stacks.

FIG. 2 shows prior art graphs illustrating variations of drain and body bias voltages vs. position in a FET switch stack in an OFF state.

FIG. 3 shows an exemplary switch stack according to an embodiment of the present disclosure.

FIG. 4 shows an exemplary bridge network according to an embodiment of the present disclosure.

FIG. 5 shows a FET switch stack according to a further embodiment of the present disclosure.

FIG. 6A shows exemplary RF voltage waveforms for drain/source of transistors in the stack according to embodiments of the present disclosure.

FIG. 6B shows exemplary RF voltage waveforms for body of transistors in the stack according to an embodiment of the present disclosure.

FIGS. 6C-6E show exemplary RF waveforms of a drain-source relative to charge redistribution tapping points according to an embodiment of the present disclosure.

FIG. 6F shows exemplary RF waveforms of a body relative to charge redistribution tapping points according to an embodiment of the present disclosure.

FIG. 7A shows exemplary RF waveforms of the drain terminal of a transistor in the stack and the body terminal of another transistor in the stack, both waveforms relative to the same tapping point according to an embodiment of the present disclosure.

FIG. 7B shows exemplary RF waveforms of the body terminal of a transistor with respect to the drain terminal of another transistor in the stack according to an embodiment of the present disclosure.

FIGS. 8A-8H show exemplary current flow diagrams of a FET switch stack according to various embodiments of the present disclosure.

FIG. 9A shows an exemplary implementation of a drain bridge circuit according to embodiments of the present disclosure.

FIG. 9B shows an exemplary implementation of a body bridge circuit according to embodiments of the present disclosure.

FIG. 10 shows a FET switch stack including two charge redistribution resistive ladders in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

FIG. 3 shows a FET switch stack circuit (300) in accordance with an embodiment of the present disclosure. The FET switch stack circuit (300) comprises a switching circuit (301), a bridge network (303), a charge redistribution resistive ladder (302) comprising a plurality of charge transfer resistors (R_{C1}, \dots, R_{Cm}) connected in series, and a capacitor (C1) serially connected to the plurality of resistors (R_{C1}, \dots, R_{Cm}). The switching circuit (301) comprises a stack of transistors (T_1, \dots, T_n) connected in series, a gate resistive ladder including resistors (R_{G1}, \dots, R_{Gn}), a drain-source resistive ladder including resistors (R_{DS1}, \dots, R_{DSn}), and a body resistive ladder including resistors (R_{B1}, \dots, R_{Bn}). The transistors (T_1, \dots, T_n) are coupled to an RF path on the top side to receive RF signals (e.g. from an antenna) and are coupled to a reference voltage (V_t) at another end. The gate resistive ladder is coupled to gate terminals of transistors (T_1, \dots, T_n), and also coupled to reference voltage (V_g). The body resistive ladder is coupled to the body terminal of transistor (T_n) at one end and coupled

to reference voltage (V_b) at another end. For convenience, a “stack unit” can be defined as a $1/n$ portion of the stack, containing one unit of any components of which there are n in the stack, such as R_{G2} , T_2 , R_{DS2} and R_{B2} .

With continued reference to FIG. 3, the charge redistribution resistive ladder (302) further comprises one or more tapping points ($Tp1, \dots, Tpk$). In operative conditions when the FET switching circuit (301) is in the OFF state, capacitor (C1) couples the RF swing from the antenna to the ladder (302), providing supply voltages across the charge redistribution resistive ladder, and more specifically at the tapping points ($Tp1, \dots, Tpk$). The bridge network (303) comprises nodes ($P1, \dots, Pk$) connected to corresponding tapping points ($Tp1, \dots, Tpk$), and nodes ($Q1, \dots, Qg$) used to connect the bridge network (303) to the switching circuit (301). According to embodiments of the present disclosure, each node ($Q1, \dots, Qg$) is connected either to a drain/source terminal (by connection to a corresponding node on the drain/source resistive ladder) or a body terminal (by connection to a corresponding node on the body resistive ladder) of a corresponding transistor of any one of the transistors (T_1, \dots, T_n) of the switching circuit (301).

In accordance with the teachings of the present disclosure, during a portion of the RF swing cycle, each tapping point (Tpi), $i=1, k$, is selectively coupled to either a drain/source terminal or a body terminal of a corresponding transistor of the switching circuit (301) via a corresponding pair of nodes (Pi, Qj), $i=1, \dots, k, j=1, \dots, g$, of the bridge network (303). During another portion of the RF swing, the tapping point (Tpi) is selectively decoupled from the corresponding drain/source or body terminal of the corresponding transistor of the switching circuit (301). In other words, during a portion of the RF swing cycle, a set of drain/source terminals and tapping points are coupled/paired with each other and a set of body terminals and tapping points are coupled/paired with each other.

In accordance with further embodiments of the present disclosure, the voltages at the tapping points are such that the set of (drain/source-terminal, tapping point) pairs source current from the charge redistribution resistive ladder and deliver it to the drain-source resistive ladder. Additionally, the set of (body terminal, tapping point) pairs sink current from the body resistive ladder and deliver it to the charge redistribution resistive ladder. Since both the sinking and sourcing processes occur along the entire switch stack, the charge redistribution resistive ladder can redistribute charges locally throughout the switch stack, creating a net current flow from the body resistive ladder to the drain-source resistive ladder, thereby reducing the de-biasing effect. In other words, the voltages at the tapping points are such that, when a tapping point is coupled with the drain/source terminal of a transistor, the voltage of such drain/source terminal is pulled up, thereby counter balancing the effect of the body leakage current, which would usually result in a dropping voltage. Similarly, when a tapping point is coupled with the body terminal of a transistor, the voltage of such body terminal is pulled down, to counter-balance the body leakage current, I_{body} , usually resulting in a raised body voltage. In what follows, this point is further clarified using some exemplary embodiments in accordance with the present disclosure.

FIG. 4 shows an exemplary composition (403) of the bridge network (303) previously shown in FIG. 3 according to an embodiment of the present disclosure. The bridge network (403) comprises one or more drain bridge circuits (BC_{d1}, \dots, BC_{dl}), and one or more body bridge circuits (BC_{b1}, \dots, BC_{bm}), where ‘1’ and ‘m’ are integers greater

than or equal to one and independent from each other. With reference to the combination of FIGS. 3-4, each drain bridge circuit may couple a corresponding tapping point of the charge redistribution resistive ladder (302) to the drain/source terminal of a corresponding transistor of the switch stack (301). Similarly, each body bridge circuit may couple a corresponding tapping point of the charge redistribution resistive ladder (302) to the body terminal of a corresponding transistor of the switch stack (301). The person skilled in the art will understand that the use of the term “drain” bridge circuit and “drain” terminal throughout the present disclosure is for conciseness purposes only, as the intended meaning of such terms is that of a “drain/source” bridge circuit and a “drain or source” terminal, as noted above.

Reference will now be made to FIG. 5 where a portion of the FET switch stack circuit (300) of FIG. 3 is shown. For the sake of clarity and ease of understanding, only a subset of the constituents of the switch stack circuit (300) of FIG. 3 is shown in FIG. 5 to illustrate the functionality of the bridge circuits and the interaction of such bridge circuits with the transistors of the switch stack and the charge redistribution resistive ladder. In particular, FIG. 5 shows an example where the bridge network (403) of FIG. 4 only contains one drain bridge circuit (BCd) and one body bridge circuit (BCb) for the sake of simplicity.

As shown in FIG. 5, drain bridge circuit (BCd) is coupled at one end to tapping point (Tp), and at another end, to the drain/source terminal of a transistor (Tk). Similarly, body bridge circuit (BCb) is connected at one end to tapping point (T_{Pj}) and at another end to the body terminal of transistor (Tk). The drain bridge circuit (BCd) is configured so that, during a portion of the RF swing cycle, the drain bridge circuit (BCd) is in a conducting (ON) state, thereby coupling tapping point (T_{Pj}) to the drain/source terminal of transistor (Tk). During another portion of the RF swing, the drain bridge circuit (BCd) is, on the other hand, selectively configured to be in a non-conducting (OFF) state, thereby decoupling/electrically isolating tapping point (T_{Pj}) from the drain/source terminal of transistor (Tk). Similar considerations apply to the body bridge circuit (BCb).

As described previously, when the transistors in the switch stack are in the OFF state, the drain/source of each transistor may be DC-biased at e.g. 0V and the gate and body of each transistor may be DC-biased at a negative voltage (e.g. -3V). The charge redistribution resistive ladder is DC-biased at some intermediate voltage between the voltage on the drain-source resistive ladder and the voltage on the body resistive ladder, for example at the mid-point, which would be -1.5V in this case. As also described previously, when a large RF voltage is applied to the antenna, the FET switch stack (100) of FIG. 1A, the drain-source resistive ladder, the gate resistive ladder and the body resistive ladder are all designed to distribute the RF voltage evenly among the FET switch stack. This is also true for the charge redistribution resistive ladder. Due to the increase in RF amplitude from the ground end to the antenna end, there will be certain tapping points in the charge redistribution resistor ladder or network that are temporarily higher in voltage than certain drain/source terminals for large enough RF amplitude. The difference in RF amplitude at the certain tapping point and the RF amplitude at the certain drain/source terminal is greater than the difference in DC bias point of the charge redistribution resistive ladder and the DC bias point of the drain/source terminals. Similarly, there will be certain tapping points in the charge redistribution resistor network that are temporarily lower in voltage than certain body terminals for large enough RF amplitude. It follows then that

due to the increase in RF amplitude from the ground end to the antenna end, there will be certain points in the body resistor ladder or network that are temporarily higher in voltage than other certain points in the drain/source resistor ladder or network for large enough RF amplitude.

To further illustrate this, reference is made to FIG. 6A, which shows the voltage over time $V(t)$ on three successive drains $D(j-1)$, $D(j)$, and $D(j+1)$ (from lower to higher in the stack) over the course of two cycles (positive-negative-positive-negative) of the RF waveform. Transistors higher in the stack have increased percentage of the total RF signal, that is they have higher peak positive voltage and lower peak negative voltage.

On the other hand, FIG. 6B shows the voltage over time $V(t)$ on three tapping points $L(k)$, $L(m)$, $L(n)$ (from lower to higher in the ladder) of the charge redistribution resistive ladder over the course of the two cycles of the RF waveform. These tapping points line up with successive transistors T_{j-1} , T_j and T_{j+1} , but there can be intermediate tapping points between these. As with the transistor drain/source $V(t)$ waveforms shown in FIG. 6A above, points higher in the ladder have increased percentage of the total RF signal. The person of skill in the art will understand that there can be any number of tapping points in the ladder within one transistor interval, so curves of any intermediate amplitude are possible. DC voltage offset between the tapping points and transistor drain points can also be noticed from FIGS. 6A-6B.

Upon a comparison between FIGS. 6A and 6B, a voltage offset between voltage on drains $D(j-1)$, $D(j)$, and $D(j+1)$ and voltage on lined-up tapping points $L(k)$, $L(m)$, $L(n)$ can be observed. As a consequence, a tapping point may be selected such that the RF amplitude of the tapping point is either greater or less than the RF amplitude at the drain/source terminal. Further, the amount that the RF amplitude at the drain/source terminal is greater or less than the RF amplitude at the tapping point may be adjusted by selecting different tapping points on the charge redistribution ladder. The difference in amplitude combined with the DC offset will set the relative voltage as a function of time between a given drain/source terminal and a specific tapping point in the charge redistribution resistive ladder.

FIG. 6C shows an example of relative voltage waveforms (620), (610) of voltage difference over time between drain (D_j) and ladder tapping points (T_p , T_r) respectively, (T_r being above (T_p), where both (T_p) and (T_r) are below (D_j) when lined up in the stack. In particular, graph (610) shows relative voltage over time with respect to (T_r) and graph (620) shows relative voltage over time with respect to (T_p). With reference to waveform (610), it can be noticed that for tapping point (T_r), voltage on drain (D_j) is positive with respect to tapping point (T_r) for the positive swing portion of the RF cycle, but there is a part of the negative swing portion, $\Delta T1$, where voltage on the drain (D_j) is negative with respect to the voltage on tapping point (T_r). This is due to the fact that tapping point (T_r) is lower in the stack than drain (D_j). Therefore, it has a smaller RF voltage swing, so it becomes less negative than (D_j) during the negative part of the RF signal. Thus, (D_j) is negative with respect to (T_r) for part of the negative swing. Similar observations can be made with reference to tapping point (T_p), graph (620) and time segment $\Delta T4$.

FIG. 6D shows an example of relative voltage waveform (630) of voltage difference over time between drain (D_j) and ladder tapping point (T_q), where (T_q) is above (D_j) when lined up in the stack. In particular, graph (630) shows relative voltage over time of drain (D_j) with respect to (T_q).

Voltage on (D_j) is positive with respect to the voltage on tapping point (T_q) for the negative swing portion of the RF cycle, but there is a part of the positive swing portion, $\Delta T2$, where the voltage difference is negative. This is due to the fact that tapping point (T_q) is higher in the stack than drain (D_j). Therefore, it has a larger RF voltage swing, so it becomes more positive than (D_j) during the positive part of the RF signal. Thus, (D_j) is negative with respect to (T_q) for part of the positive swing.

The two waveforms (610, 630) from FIGS. 6C and 6D respectively, are shown together in FIG. 6E. As can be noticed, during both the positive and negative portions of the RF waveform there is a time window where the drain/source (D_j) is negative with respect to one tapping point or another. For the exemplary case shown in FIG. 6E, the maximum amount that the drain/source is positive with respect to either tapping point is 4 volts. As described above, the drain/source bridge circuits according to embodiments of the present disclosure can be constructed and connected such that they conduct when a drain/source is at a lower voltage than a coupled tapping point (see negative voltage time windows in FIG. 6E) and they block conduction when a drain/source is at a higher voltage than a coupled tapping point (see positive voltage time windows in FIG. 6E).

Analogously to FIG. 6E for a drain/source terminal, FIG. 6F shows relative voltages (640, 650) as a function of time between a given body terminal and two specific tapping points (T_r , T_s) in the charge redistribution resistive ladder. In this case, there is a portion of each half cycle of the RF waveform where the body terminal is positive with respect to one or the other of the tapping points. Additionally, for the specific example shown in the figure, during the entire time span of the RF waveform, the body voltage is never more than 4 volts negative with respect to either tapping point voltage. As described above, with reference to this embodiment, the bridge circuits are constructed and connected such that they conduct when the body is at a higher voltage than the coupled tapping point (positive voltage time windows in FIG. 6F) and they block conduction when the body is at a lower voltage than the coupled tapping point (negative voltage time windows in FIG. 6F).

FIG. 7A shows relative voltage waveforms (710, 720) over time of the drain/source terminal of a first transistor and the body terminal of a second transistor, both relative to the same tapping point (T_r). During the negative portion of the RF cycle there is a segment of time $\Delta T3$ where the body terminal of the second transistor is positive with respect to the tapping point (T_r) at the same time that the drain/source of the first transistor is negative with respect to the tapping point (T_r). It follows that, during that time window, the body of the second transistor is positive with respect to the drain/source of the first transistor. This is better evidenced in FIG. 7B, which shows the voltage over time of the body of the referenced second transistor relative to the voltage over time of the drain/source of the first transistor.

As previously noted in FIG. 6C, graph (620) represents a voltage difference over a tapping point (T_p) that is lower in the stack than the drain/source to which it is coupled. On the other hand, the second graph (610) shown in FIG. 6C represents a voltage difference over another a tapping point (T_r) that is also lower in the stack than the drain/source to which it is coupled, but by a different amount than (T_p). Similarly to the behavior for tapping point (T_p), the drain/source is positive with respect to the tapping point (T_r) for the positive swing portion of the RF cycle, while instead there is a part (time window/segment) of the negative swing portion, $\Delta T4$, where the drain/source voltage is negative

with respect to the voltage of the tapping point (Tr). Graphs (610) and (620) illustrate that both i) the magnitude of the voltage difference and ii) duration of the drain/source being negative with respect to a coupled tapping point can be adjusted by selecting how much lower or higher in the stack the tapping point is relative to the drain/source to which it is coupled. Since the charge redistribution resistive ladder can have any number of tapping points, this qualitative consideration allows adjustment of the voltage difference waveforms to achieve any desired characteristics.

Turning now to the previous representations shown in FIGS. 4 and 5, the following FIGS. 8A-8E will illustrate several current flow examples. Such figures are intended to be schematic and indicative. For example, the transistors are not shown for added clarity. Additionally, only one drain resistor per transistor is shown, so that each point between resistors on the drain/source resistive ladder is tied to a transistor drain. Similarly, only one body resistor per transistor is shown, so that each point between resistors on the body resistive ladder is tied to a transistor body. Moreover, in the exemplary representation of such figures, the charge redistribution resistive ladder is broken into four segments per transistor, also in this case for representation purposes only. The person skilled in the art will understand that there can be any number of segments on any ladder, evenly distributed throughout the transistors or not. Similarly, the person skilled in the art will also understand that there can be more than one drain and/or body resistor on a respective ladder per transistor, in order to allow freedom in the design of tapping points, in order to provide desired voltage relationships between certain points in the three resistive ladders as a function of applied RF voltage.

With initial reference to FIG. 8A, in order to illustrate the current flow during the time period when the bridge circuits, (BCd, BCb) are in a conducting (ON) state, such figure shows a section (800) of a FET switch stack, showing drain-source resistive ladder (801), body resistive ladder (803) and charge redistribution resistive ladder (802). In such figure the left side is the one intended to be closer to the antenna terminal, as indicated. Several drain/source bridge circuits (BCd) are shown, with their respective anodes (A) and cathodes (C) connected between tapping points in the charge redistribution ladder (802) and drain/source terminals in the drain-source resistive ladder/network (801). Several body bridge circuits (BCb) are also shown, with their respective cathodes (C) and anodes (A) connected between tapping points in the charge redistribution resistive ladder (802) and body terminals in the body resistive ladder (803).

With reference to FIG. 6C, FIG. 8B shows current flow (using thick lines and arrows) during the negative portion of the RF signal applied to the antenna, and in particular during time interval $\Delta T1$ of FIG. 6C. As described previously, the nodes in all three resistive ladders (801, 802, 803) have smaller RF voltage amplitude going towards positions "lower" in the stack, i.e. farther away from the antenna and towards the right direction in FIG. 8B. Thus, during the negative part of the RF voltage signal, the nodes towards the right direction have a smaller negative voltage applied, becoming more positive with respect to points closer to the antenna end. Therefore, the bridge circuits BCd and BCb having cathodes connected closer than anodes to the antenna (on the left in this figure) are configured to conduct during this part of the waveform. As a consequence, current flows from the body resistive ladder to the charge redistribution resistive ladder and from the charge redistribution resistive ladder to the drain-source resistive ladder as indicated by the arrows.

On the other hand, FIG. 8C shows current flow during the positive portion of the RF signal applied to the antenna, and in particular during time interval $\Delta T2$ of FIG. 6D. As described previously, the nodes in all three resistive ladders (801, 802, 803) have larger RF voltage amplitude going towards positions "higher" in the stack, i.e. closer to the antenna and towards the left direction in FIG. 8C. Thus, during the positive part of the RF voltage signal, the nodes towards the left direction have a larger positive voltage applied, becoming positive with respect to points farther from the antenna end. Therefore, the bridge circuits BCd and BCb having anodes connected closer than cathodes to the antenna (on the left in this figure) are configured to conduct during this part of the waveform. As a consequence, current flows from the body resistive ladder to the charge redistribution resistive ladder and from the charge redistribution resistive ladder to the drain-source resistive ladder as indicated by the arrows.

With reference to the combined representation shown in FIGS. 8B and 8C, the points where the current from the body resistive ladder is injected into the charge redistribution ladder are separate from the points in the charge redistribution resistive ladder where current is drawn by the drain resistive ladder. The charge redistribution ladder connects those points and enables net current to flow from the body resistive ladder to the drain resistive ladder. As illustrated in FIG. 6C, the characteristics of the relative voltage waveform between a drain/source and a tapping point coupled to it can be adjusted by changing the position in the stack of the tapping point relative to the drain/source. Thus, if a different tapping point in the charge redistribution resistive ladder is chosen, that will change the magnitude and duration of the portion of the waveform where current is flowing from the charge redistribution resistive ladder to the drain/source resistive ladder. The same is true for a body coupled to the charge redistribution resistive ladder. Since tapping points coupled to a drain/source and tapping points coupled to a body can be adjusted to different points along the charge redistribution resistive ladder, it is also possible to have tapping points coupled to a drain/source be the same as tapping points coupled to a body. However, this choice may restrict the relative voltage waveforms (see FIG. 6C) to non-optimum characteristics.

Since the characteristics of a body to tapping point relative voltage waveform is dependent on the position in the stack of the tapping point with reference to the coupled body, this relative position can be changed by moving either the tapping point or the point at which a location in the body resistive ladder is accessed. By dividing a resistor in the body resistive ladder into multiple series resistors, additional access points can be created. By way of example, while FIGS. 8A-8C show one resistor per body in the body resistive ladder, FIG. 8D shows a different embodiment of such configuration where there are two resistive segments (two examples are shown with numerals 803' and 803") per body in the body resistive ladder. Therefore, in FIG. 8D, the points of access to the body resistive ladder are translated by one-half of a stack unit. In order to maintain the same relative position of the charge redistribution resistive ladder to the access of the body resistive ladder, the tapping points on the charge redistribution resistive ladder are also translated by one-half of a stack unit. The resulting configuration provides an embodiment where the same tapping points on the charge redistribution resistive ladder are coupled to both the drain/source resistive ladder and the body resistive ladder.

For the above noted specific case where the same charge redistribution resistive ladder tapping points are coupled to both the drain resistive ladder and the body resistive ladder, current can flow from the body resistive ladder to the drain resistive ladder without passing through any resistors in the charge redistribution resistive ladder. In this case, the charge redistribution resistive ladder does not need to have resistors connecting the tapping points that are common to the body resistive ladder access points and the drain resistive ladder access points. Such specific configuration is shown in FIG. 8E, where all the resistors in the charge redistribution network have been removed and the charge redistribution resistive ladder has been thus omitted. In such case, charge redistribution between the drain/source resistive ladder and the body resistive ladder occurs directly, not just as a consequence induced through the presence of the charge redistribution resistive network. Similarly to the other embodiments, during each half cycle, current will only flow through specific bridge circuits. As drawn, during the positive half-cycle on the RF antenna signal, current will only flow through bridge circuits with anodes oriented to the left/antenna side. During the negative half-cycle, current will only flow through bridge circuits with cathodes on the left/antenna, side.

Thus, in FIG. 8E, body bridge circuits (BCb) that are connected to drain bridge circuits (BCd) with the same anode/cathode orientation can be grouped and referred to as drain-body bridge circuits (BCdb). This combining of the body bridge circuits (BCb) with the drain bridge circuits (BCd) to form body-drain bridge circuits (BCdb) is shown in FIG. 8F. Similarly to the case when the bridge circuits are separate, during the positive half-cycle on the RF antenna signal, current will only flow through bridge circuits with the anode oriented to the left/antenna, side, as shown in FIG. 8H. On the other hand, during the negative half-cycle of the RF antenna signal, current will only flow through bridge circuits with the cathode on the left, or antenna, side, as shown in FIG. 8G.

In view of the above, the person skilled in the art will appreciate that the teachings of the present disclosure provide solutions both to the distribution and generation issues associated with the previously described body leakage current issue.

As already noted in several portions of the present disclosure, the bridge circuits connect drain/source tapping points to drain/source terminals of corresponding transistors such that i) during the time when the voltage of a drain/source tapping point is higher than the voltage of the drain/source terminal of a corresponding transistor, the bridge circuit connecting the drain/source tapping point and drain/source terminal is in an ON state and therefore conducting, and ii) during the time when the voltage of the drain/source tapping point is lower than the voltage of the drain/source terminal of the corresponding transistor, the bridge circuit connecting the drain/source tapping point and drain/source terminal is in an OFF state and therefore not conducting.

Similarly, the bridge circuits connect body tapping points to body terminals of corresponding transistors such that i) during the time when the voltage of a body tapping point is lower than the voltage of the body terminal of a corresponding transistor, the bridge circuit connecting the body tapping point and body terminal is in an ON state and therefore conducting, and ii) during the time when the voltage of the body tapping point is higher than the voltage of the body terminal of the corresponding transistor, the bridge circuit

connecting the body tapping point and body terminal is in an OFF state and therefore not conducting.

In other words, the function of the bridge circuit(s) is to conduct current when their anode is sufficiently positive with respect to their cathode and block current flow when the anode is less positive or negative with respect to their cathode. A bridge circuit may be a two-terminal device or circuit block connecting a tapping point in the charge redistribution ladder to a drain/source or a body terminal of a transistor or connecting a point in a drain/source ladder to a point in a body ladder. Additionally, the bridge circuit may have additional control terminals connecting to additional points in the charge redistribution ladder. Elements within the bridge circuit may include diodes, diode-connected NMOS transistors, diode-connected PMOS transistors, resistors, NMOS transistors utilizing additional control terminal of the bridge circuit and PMOS transistors utilizing additional control terminal of the bridge circuit. Any combination of the above-mentioned exemplary implementations of the bridge circuits may be placed in series, parallel or series/parallel combination.

FIG. 9A shows exemplary implementations of a drain bridge circuit with an anode node connected to a charge redistribution ladder tapping point, a cathode node connected to transistor drain/source and optional control port, which can connect to a different tapping point in the charge redistribution ladder or to some other input signal. The person skilled in the art will understand that these are a few examples of implementations and other implementations in accordance with the teachings of present disclosure and using various combinations of such implementations may also be envisaged.

FIG. 9B shows an exemplary body bridge circuit with a cathode node connected to a charge redistribution ladder tapping point, an anode node connected to transistor body and optional control port, which can connect to a different tapping point in the charge redistribution ladder or to some other input signal. The person skilled in the art will understand that these are a few examples of implementations and other implementations in accordance with the teachings of present disclosure and using various combinations of such implementations may also be envisaged.

Referring back to FIG. 6C, graph (610) represents a smaller negative peak voltage across the bridge circuit in the OFF state. This may represent a preferred scenario over the one represented by graph (620) in terms of the breakdown voltage requirements of the transistor stacks used as part of the design of the bridge circuit shown in FIG. 9A or 9B.

In the above description, the relative voltages of the drains of transistors (Tk) and corresponding tapping points of the redistribution resistive ladder may be selected in a way to ensure a proper transfer of charge to the drain/source terminals. Similarly, the relative voltages of the bodies of transistors (Tk) and corresponding tapping points of the redistribution resistive ladder are selected to ensure a proper transfer of charge from the body terminals. Therefore, the voltages of the terminals of the transistors (Tk) and the tapping points should have a known, consistent relationship.

With reference to FIG. 3, the switching circuit (301) may be configured to divide the full RF signal applied to the antenna among the plurality of transistors (T1, . . . , Tn) connected in series, among the plurality of resistors connected in series in the drain-source resistive ladder, among the plurality of resistors connected in series in the gate resistive ladder, and among the plurality of resistors connected in series in the body resistive ladder. Since each resistor in the drain-source resistor ladder is connected in

parallel with the drain and source terminals of an associated transistor, any discussion of connections referring to either of them applies to both of them.

With further reference to FIG. 3, the charge redistribution resistive ladder (302) may be configured to divide the full RF signal applied to the antenna among the plurality of resistors connected in series.

The full RF signal may be divided in equal or unequal steps in all of the above series connected structures. Further, the division of the RF signal within each of the series connected structures may change as a function of operating conditions of other circuit blocks. Since the operation of the charge redistribution resistive ladder benefits of a precise voltage relationship to the points where it connects to the drain-source resistive ladder, it is preferred that the RF signal division within the redistribution resistive ladder follows the changes in the RF signal division within the drain-source resistive ladder. In other words, as the RF signal division within the series transistor stack changes, the RF signal division within the redistribution resistive ladder may be synchronized with these changes.

In order to maintain such synchronization, the redistribution resistive ladder may have specific tapping points designed to have the same RF signal division as the drain-source resistive ladder under nominal conditions. This condition can be satisfied by providing, for example, a capacitor of suitable size connecting each point of the drain-source resistive ladder to the specific tapping points of the redistribution resistive ladder configured to have the same RF signal division of the drain-source resistive ladder, see, e.g., capacitor (510) shown in FIG. 5. As the RF signal division in the switching circuit changes due to factors described above, the RF signal division in the redistribution resistive ladder will follow due to the capacitive connection between the drain-source resistive ladder and the specific tap points of the redistribution resistive ladder.

In the embodiments described so far, a single charge redistribution resistive ladder is used to provide tapping points to be coupled to drain/source and body terminals of transistors within the FET switch stack. Embodiments in accordance with the present disclosure may also be envisaged wherein two separate charge redistribution resistive ladders are used. In such embodiments, a drain charge redistribution resistive ladder may be used to provide tapping points to be coupled to the drain/source terminals, and a body charge redistribution resistive ladder may be used to provide tapping points to be coupled to the body terminals of corresponding transistors within the FET switch stack. In such embodiments, an additional number of nodes or tapping points can be designed, given that one of the two redistribution ladders will contain only drain/source tapping points and the other will contain only body tapping points. In what follows, such embodiments using two charge redistribution resistive ladders are described in more detail.

FIG. 10 shows a FET switch stack circuit (1000) according to embodiments of the present disclosure. The FET switch stack circuit (1000) comprises a switching circuit (1001), a body charge redistribution resistive ladder (1012), a drain charge redistribution resistive ladder (1022), and a bridge network (1003). The switching circuit (1001) may be similar to the switching circuit (301) of FIG. 3. For ease of understanding, only three stacked transistors are shown in FIG. 10. Additionally, while the bridge network (1003) may comprise more than three bridge circuits, for the sake of clarity and for illustration purposes, only three such circuits are shown in FIG. 10, i.e. drain bridge circuit (BCd), body bridge circuit (BCb) and drain-body bridge circuit (BCdb).

The body charge redistribution ladder (1012) is coupled at one end to the antenna (RF path) and connected to reference voltage (Vc1) at another end. Similarly, the drain charge redistribution ladder (1022) is coupled at one end to the antenna (RF path) and connected to reference voltage (Vc2) at another end.

With continued reference to FIG. 10, body bridge circuit (BCb) is used to couple/decouple tapping points of the body charge redistribution ladder (1012) to/from the body terminals of corresponding transistors, and drain bridge circuit (BCd) is used to couple/decouple tapping points of the drain charge redistribution ladder (1022) to/from the drain/source terminals of corresponding transistors in the switching circuit (1001). However, in order to conserve current, drain-body bridge circuit (BCdb) may also be used to couple/decouple body and drain charge redistribution ladders (1012, 1022). The principle of operation of each of the bridge circuits shown in FIG. 10 is similar to what was described before with regards to bridge circuits (BCb, BCd) of FIG. 5 and bridge circuits (BCdb) of FIG. 8E. In particular, a drain-body bridge circuit (BCdb) like the one shown on the bottom of FIG. 10 couples directly tapping point (Tpi) on the body charge redistribution ladder (1012) with tapping point (Tpj) on the drain charge redistribution ladder (1022), thus redistributing charges between one ladder and the other.

Still with reference to FIG. 10, the path of the charge transfer is as shown by arrows (1051, 1052, . . . , 1057). In other words, charge is transferred from the body to the body bridge circuit (arrow 1051), and then to the drain bridge circuit via the drain-body bridge circuit (arrows 1052, 1053, 1054, 1055), and then to the drain/source terminal (arrows 1056, 1057). In view of this, the body leakage current, I_{body}, is supplied and circulated locally within the circuit structure.

Turning to the capacitive synchronization implemented with reference to the single charge redistribution ladder mentioned before, such synchronization can be extended to the embodiment of FIG. 10, if desired, by connecting capacitors between specific tap points of each resistive redistribution ladder.

Switch stacks designed in accordance with embodiments of the present disclosure may be implemented as part of an integrated circuit chip or an electronic module, wherein the integrated circuit chip or the electronic module are part of a communication device. Further embodiments according to the present disclosure may also be envisaged, wherein the switch stacks as disclosed is part of the RF front-end of an electronic circuit or an electronic module or a communication device.

With further reference to FIGS. 3-10, and in accordance with further embodiments of the present disclosure:

The FET switch stack circuit (300) of FIG. 3 may include two or more transistors.

Bridge circuits with the same or different constituents or a combination thereof may be employed to design switch stacks.

Reference voltages (V_b, V_g) may supply negative voltages when the stack of FETs is in the OFF state.

Reference voltages (V_b, V_g) may supply the same or different voltage values.

Reference voltages (V_b, V_g) may be controlled by one or more bias control circuits to provide proper voltage values during the OFF and ON states of the FET switch stack.

Reference voltage V_t may be ground.

Any tapping point of the charge redistribution ladder (302) of FIG. 3 paired with a drain/source terminal of a first transistor, may also be paired with a body terminal of a second transistor other than the first transistor.

A charge redistribution resistive ladder may comprise one or more tapping points.

The reference voltage (V_c) may supply a voltage value that is half of the voltage value supplied by the reference voltage (V_b) or the reference voltage (V_g). By way of example, and not of limitation, reference voltages (V_b , V_g) may each supply $-3.2V$ and V_c may be halfway at $-1.6V$.

The reference voltage (V_{c1}) may supply a voltage value that is around $\frac{2}{3}$ of the voltage value supplied by the reference voltages (V_b) or (V_g) while the reference voltage (V_{c2}) may supply a voltage value at $\frac{1}{3}$ of the voltage supplied by the reference voltages (V_b) or (V_g). By way of example, and not of limitation, reference voltages (V_b , V_g) may each supply $-3.3V$, and the reference voltages (V_{c1} , V_{c2}) may supply ($-2.2V$, $-1.1V$) respectively.

The term "MOSFET", as used in this disclosure, means any field effect transistor (FET) with an insulated gate and comprising a metal or metal-like, insulator, and semiconductor structure. The terms "metal" or "metal-like" include at least one electrically conductive material (such as aluminum, copper, or other metal, or highly doped polysilicon, graphene, or other electrical conductor), "insulator" includes at least one insulating material (such as silicon oxide or other dielectric material), and "semiconductor" includes at least one semiconductor material.

As should be readily apparent to one of ordinary skill in the art, various embodiments of the invention can be implemented to meet a wide variety of specifications. Unless otherwise noted above, selection of suitable component values is a matter of design choice and various embodiments of the invention may be implemented in any suitable IC technology (including but not limited to MOSFET structures), or in hybrid or discrete circuit forms. Integrated circuit embodiments may be fabricated using any suitable substrates and processes, including but not limited to standard bulk silicon, silicon-on-insulator (SOI), and silicon-on-sapphire (SOS). Unless otherwise noted above, the invention may be implemented in other transistor technologies such as bipolar, GaAs HBT, GaN HEMT, GaAs pHEMT, and MES-FET technologies. However, the inventive concepts described above are particularly useful with an SOI-based fabrication process (including SOS), and with fabrication processes having similar characteristics. Fabrication in CMOS on SOI or SOS processes enables circuits with low power consumption, the ability to withstand high power signals during operation due to FET stacking, good linearity, and high frequency operation (i.e., radio frequencies up to and exceeding 50 GHz). Monolithic IC implementation is particularly useful since parasitic capacitances generally can be kept low (or at a minimum, kept uniform across all units, permitting them to be compensated) by careful design.

Voltage levels may be adjusted or voltage and/or logic signal polarities reversed depending on a particular specification and/or implementing technology (e.g., NMOS, PMOS, or CMOS, and enhancement mode or depletion mode transistor devices). Component voltage, current, and power handling capabilities may be adapted as needed, for example, by adjusting device sizes, serially "stacking" components (particularly FETs) to withstand greater voltages,

and/or using multiple components in parallel to handle greater currents. Additional circuit components may be added to enhance the capabilities of the disclosed circuits and/or to provide additional functional without significantly altering the functionality of the disclosed circuits.

A number of embodiments of the invention have been described. It is to be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, some of the steps described above may be order independent, and thus can be performed in an order different from that described. Further, some of the steps described above may be optional. Various activities described with respect to the methods identified above can be executed in repetitive, serial, or parallel fashion.

It is to be understood that the foregoing description is intended to illustrate and not to limit the scope of the invention, which is defined by the scope of the following claims, and that other embodiments are within the scope of the claims. (Note that the parenthetical labels for claim elements are for ease of referring to such elements, and do not in themselves indicate a particular required ordering or enumeration of elements; further, such labels may be reused in dependent claims as references to additional elements without being regarded as starting a conflicting labeling sequence).

The invention claimed is:

1. A field effect transistor (FET) switch stack circuit comprising:

a stacked configuration of series-connected FET transistors coupled to a radio frequency (RF) terminal;

a charge redistribution resistive ladder coupled to the RF terminal, the charge redistribution resistive ladder comprising series-connected charge redistribution resistors and tapping points; and

a drain/source bridge network configured to selectively couple/decouple a first set of one or more tapping points on the charge redistribution resistive ladder with/from drain or source terminals of the FET transistors and a body bridge network configured to selectively couple/decouple a second set of one or more tapping points on the charge redistribution resistive ladder with/from body terminals of the FET transistors, wherein, when the FET switch stack is in OFF state:

the FET switch stack is configured to be coupled to an RF signal at the RF terminal, and to receive RF voltages at the tapping points;

during a first portion of a period of the RF signal, the drain/source bridge network couples the first set of one or more tapping points to the drain or source terminals of the FET transistors and the body bridge network couples the second set of one or more tapping points to the body terminals of the FET transistors, and

during a second portion of the period of the RF signal separate from the first portion, the drain/source bridge network decouples the first set of one or more tapping points from the drain or source terminals of the FET transistors and the body bridge network decouples the second set of one or more tapping points from the body terminals of the FET transistors.

2. The FET switch stack circuit of claim 1, wherein the FET transistors are further connected to a first reference voltage.

3. The FET switch stack circuit of claim 1, wherein the drain/source bridge network comprises at least one drain/

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source bridge circuit and the body bridge network comprises at least one body bridge circuit.

4. The FET switch stack circuit of claim 3, wherein a drain/source bridge circuit of the at least one drain/source bridge circuit comprises a first anode node connected to a tapping point of the first set of one or more tapping points, a first cathode node connected to a drain or source of a FET transistor; and/or a body bridge circuit of the at least one body bridge circuits comprises a second cathode node connected to a tapping point of the second set of one or more tapping points, a second anode node connected to a body terminal of a FET transistor.

5. The FET switch stack circuit of claim 4, wherein the drain/source bridge circuit comprises a series combination of at least a first diode and at least a first resistor; and/or the body bridge circuit comprises a series combination of at least a second diode and at least a second resistor.

6. The FET switch stack circuit of claim 5, wherein the first diode and/or the second diode are implemented through a PMOS transistor with a gate and a source tied together.

7. The FET switch stack circuit of claim 5, wherein the drain/source bridge circuit further comprises a PMOS transistor arranged in series with the series combination of the at least first diode and the at least first resistor.

8. The FET switch stack circuit of claim 7, wherein the PMOS transistor is configured to receive a control signal at a gate of the PMOS transistor.

9. The FET switch stack circuit of claim 1, wherein the first set of one or more tapping points and the second set of one or more tapping points are distinct.

10. The FET switch stack circuit of claim 1, wherein the first set of one or more tapping points and the second set of one or more tapping points contain the same tapping points.

11. The FET switch stack circuit of claim 1, further comprising a capacitor connected between the charge redistribution resistors and the RF terminal.

12. The FET switch stack circuit of claim 1, further comprising a drain/source resistive ladder to provide access to the drain or source terminals of the FET transistors and a body resistive ladder to provide access to the body terminals of the FET transistor,

the drain/source bridge circuit configured to selectively couple/decouple the first set of one or more tapping points with/from nodes on the drain/source resistive ladder,

the body bridge circuit configured to selectively couple/decouple the second set of one or more tapping points with/from nodes on the body resistive ladder.

13. The FET switch stack circuit of claim 12, wherein couplings between the first set of one or more tapping points and the drain/source resistive ladder and couplings between the second set of one or more tapping points and the body resistive ladder further comprise synchronization capacitors.

14. The FET switch stack circuit of claim 12, wherein a number of the nodes on the drain/source resistive ladder and/or a number of the nodes on the body resistive ladder is same as a number of FET transistors, thus allowing a single connection point on each resistive ladder per FET transistor.

15. The FET switch stack circuit of claim 12, wherein a number on the nodes on the drain/source resistive ladder and/or a number of the nodes on the body resistive ladder is higher than a number of FET transistors, thus allowing plural connection points at different voltages on each resistive ladder per FET transistor.

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16. The FET switch stack circuit of claim 12, wherein the FET transistors are further connected to a first reference voltage.

17. The FET switch stack circuit of claim 12, wherein the first set of one or more tapping points and the second set of one or more tapping points are distinct.

18. The FET switch stack circuit of claim 12, wherein the first set of one or more tapping points and the second set of one or more tapping points contain the same tapping points.

19. The FET switch stack circuit of claim 12, further comprising a capacitor connected between the charge redistribution resistors and the RF terminal.

20. A field effect transistor (FET) switch stack circuit comprising:

a stacked configuration of series-connected FET transistors coupled to a radio frequency (RF) terminal;

a charge redistribution resistive ladder coupled to the RF terminal, the charge redistribution resistive ladder comprising series-connected charge redistribution resistors and tapping points;

a drain/source bridge network configured to selectively couple/decouple a first set of one or more tapping points on the charge redistribution resistive ladder with/from drain or source terminals of the FET transistors and a body bridge network configured to selectively couple/decouple a second set of one or more tapping points on the charge redistribution resistive ladder with/from body terminals of the FET transistors;

wherein,

when the FET switch stack is in OFF state:

the FET switch stack is configured to be coupled to an RF signal at the RF terminal, and to receive RF voltages at the tapping points;

during a first portion of a period of the RF signal, the drain/source bridge network couples the first set of one or more tapping points to the drain or source terminals of the FET transistors and the body bridge network couples the second set of one or more tapping points to the body terminals of the FET transistors;

the drain/source bridge network comprises at least one drain/source bridge circuit and the body bridge network comprises at least one body bridge circuit;

a drain/source bridge circuit of the at least one drain/source bridge circuit comprises a first anode node connected to a tapping point of the first set of one or more tapping points, a first cathode node connected to a drain or source of a FET transistor;

a body bridge circuit of the at least one body bridge circuits comprises a second cathode node connected to a tapping point of the second set of one or more tapping points, a second anode node connected to a body terminal of a FET transistor;

the drain/source bridge circuit comprises a series combination of at least a first diode and at least a first resistor;

the body bridge circuit comprises a series combination of at least a second diode and at least a second resistor, and

the drain/source bridge circuit further comprises a PMOS transistor arranged in series with the series combination of the at least first diode and the at least first resistor.

21. The FET switch stack circuit of claim 20, wherein the PMOS transistor is configured to receive a control signal at a gate of the PMOS transistor.

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22. A field effect transistor (FET) switch stack circuit comprising:

a stacked configuration of series-connected FET transistors coupled to a radio frequency (RF) terminal;

a charge redistribution resistive ladder coupled to the RF terminal, the charge redistribution resistive ladder comprising series-connected charge redistribution resistors and tapping points;

a drain/source bridge network configured to selectively couple/decouple a first set of one or more tapping points on the charge redistribution resistive ladder with/from drain or source terminals of the FET transistors and a body bridge network configured to selectively couple/decouple a second set of one or more tapping points on the charge redistribution resistive ladder with/from body terminals of the FET transistors;

a capacitor connected between the charge redistribution resistors and the RF terminal,

and wherein, when the FET switch stack is in OFF state:

the FET switch stack is configured to be coupled to an RF signal at the RF terminal, and to receive RF voltages at the tapping points; and

during a first portion of a period of the RF signal, the drain/source bridge network couples the first set of one or more tapping points to the drain or source terminals of the FET transistors and the body bridge network couples the second set of one or more tapping points to the body terminals of the FET transistors.

23. A field effect transistor (FET) switch stack circuit comprising:

a stacked configuration of series-connected FET transistors coupled to a radio frequency (RF) terminal;

a charge redistribution resistive ladder coupled to the RF terminal, the charge redistribution resistive ladder comprising series-connected charge redistribution resistors and tapping points;

a drain/source bridge network configured to selectively couple/decouple a first set of one or more tapping points on the charge redistribution resistive ladder with/from drain or source terminals of the FET transistors and a body bridge network configured to selectively couple/decouple a second set of one or more tapping points on the charge redistribution resistive ladder with/from body terminals of the FET transistors;

a drain/source resistive ladder to provide access to the drain or source terminals of the FET transistors and a body resistive ladder to provide access to the body terminals of the FET transistor,

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the drain/source bridge circuit configured to selectively couple/decouple the first set of one or more tapping points with/from nodes on the drain/source resistive ladder,

the body bridge circuit configured to selectively couple/decouple the second set of one or more tapping points with/from nodes on the body resistive ladder, and

wherein, when the FET switch stack is in OFF state:

the FET switch stack is configured to be coupled to an RF signal at the RF terminal, and to receive RF voltages at the tapping points; and

during a first portion of a period of the RF signal, the drain/source bridge network couples the first set of one or more tapping points to the drain or source terminals of the FET transistors and the body bridge network couples the second set of one or more tapping points to the body terminals of the FET transistors.

24. The FET switch stack circuit of claim 23, wherein couplings between the first set of one or more tapping points and the drain/source resistive ladder and couplings between the second set of one or more tapping points and the body resistive ladder further comprise synchronization capacitors.

25. The FET switch stack circuit of claim 23, wherein a number of the nodes on the drain/source resistive ladder and/or a number of the nodes on the body resistive ladder is same as a number of FET transistors, thus allowing a single connection point on each resistive ladder per FET transistor.

26. The FET switch stack circuit of claim 23, wherein a number on the nodes on the drain/source resistive ladder and/or a number of the nodes on the body resistive ladder is higher than a number of FET transistors, thus allowing plural connection points at different voltages on each resistive ladder per FET transistor.

27. The FET switch stack circuit of claim 23, wherein the FET transistors are further connected to a first reference voltage.

28. The FET switch stack circuit of claim 23, wherein the first set of one or more tapping points and the second set of one or more tapping points are distinct.

29. The FET switch stack circuit of claim 23, wherein the first set of one or more tapping points and the second set of one or more tapping points contain the same tapping points.

30. The FET switch stack circuit of claim 23, further comprising a capacitor connected between the charge redistribution resistors and the RF terminal.

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