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(54) **LOOP DELAY COMPENSATION IN A DELTA-SIGMA MODULATOR**

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H03M 1/12 (2006.01)

(52) **U.S. Cl.**
CPC *H03M 3/37* (2013.01); *H03M 3/464* (2013.01); *H03M 1/12* (2013.01); *H03M 3/30* (2013.01)

(58) **Field of Classification Search**
CPC *H03M 3/37*; *H03M 3/464*; *H03M 1/12*
See application file for complete search history.

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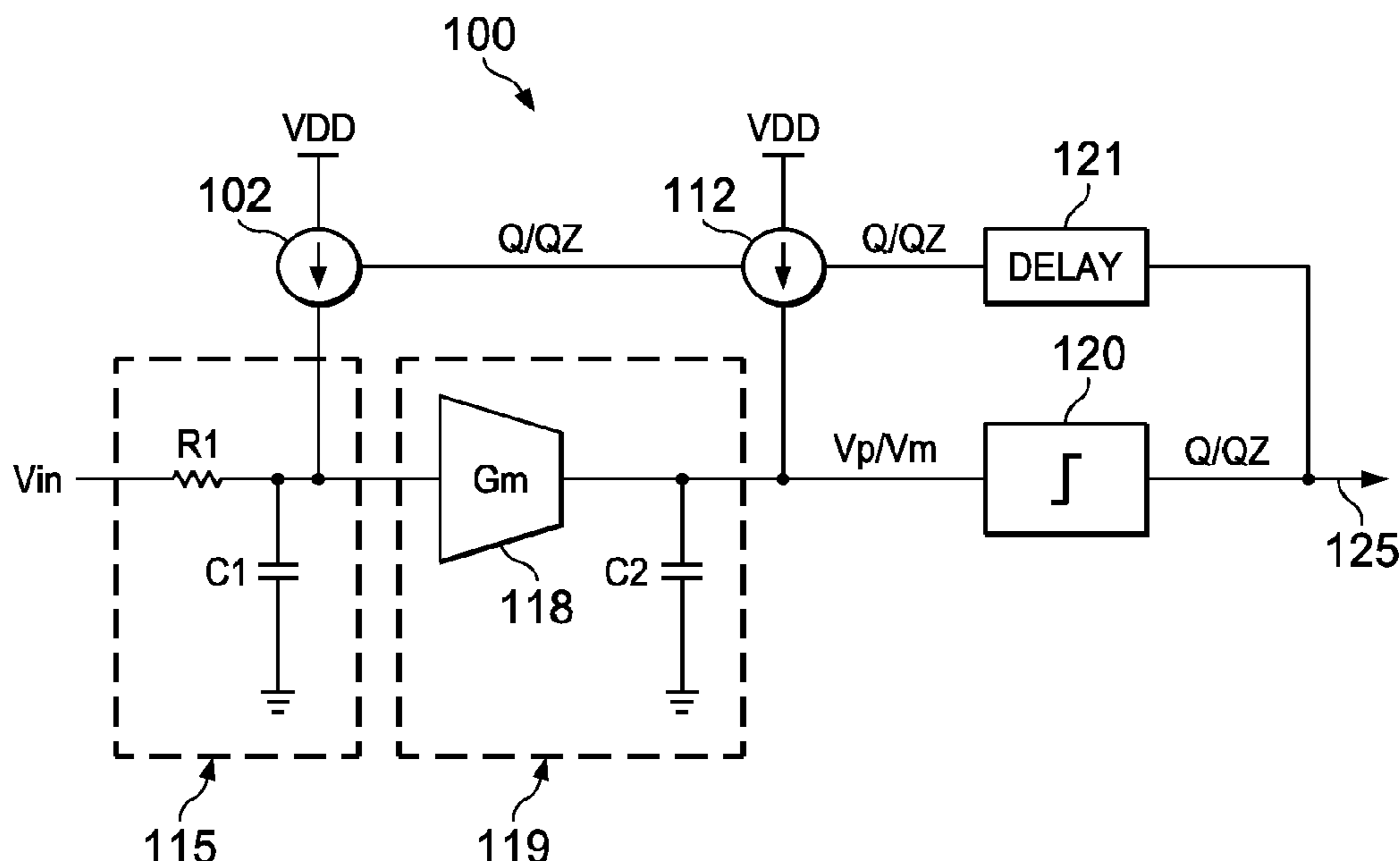
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(57) **ABSTRACT**

A delta-sigma modulator includes a first integrator and a comparator. The comparator's positive input couples to the first integrator's positive output, and the comparator's negative input couples to the first integrator's negative output. A first current DAC comprises a current source device, and first and second transistors. The first transistor has a first transistor control input and first and second current terminals. The first current terminal couples to the current source device, and the second current terminal couples to the first integrator positive output. The second transistor has a second transistor control input and third and fourth current terminals. The third current terminal couples to the current source device, and the fourth current terminal couples to the first integrator negative output. A first capacitive device couples to the second transistor control input and to both the second current terminal and the first integrator positive output.

20 Claims, 2 Drawing Sheets



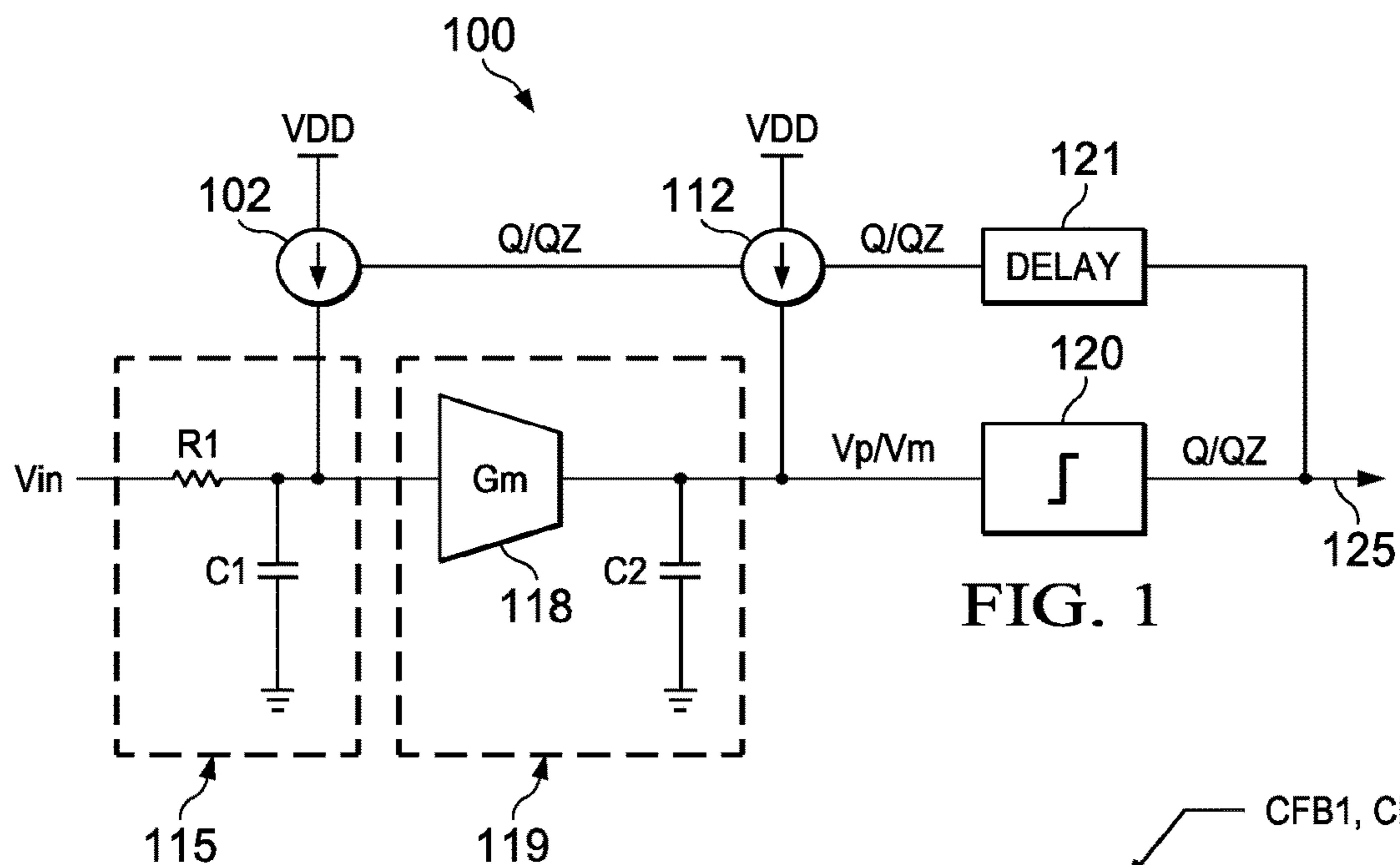


FIG. 1

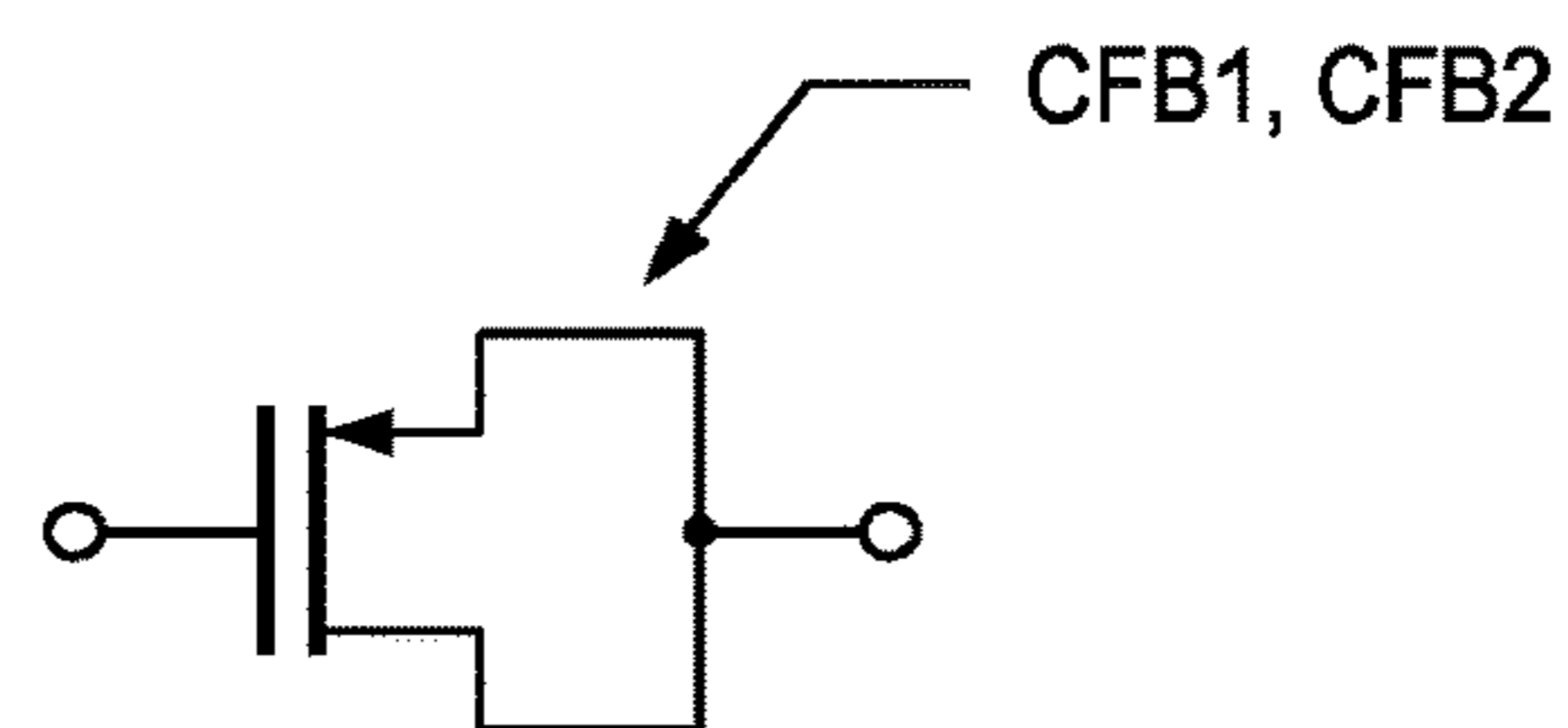


FIG. 3

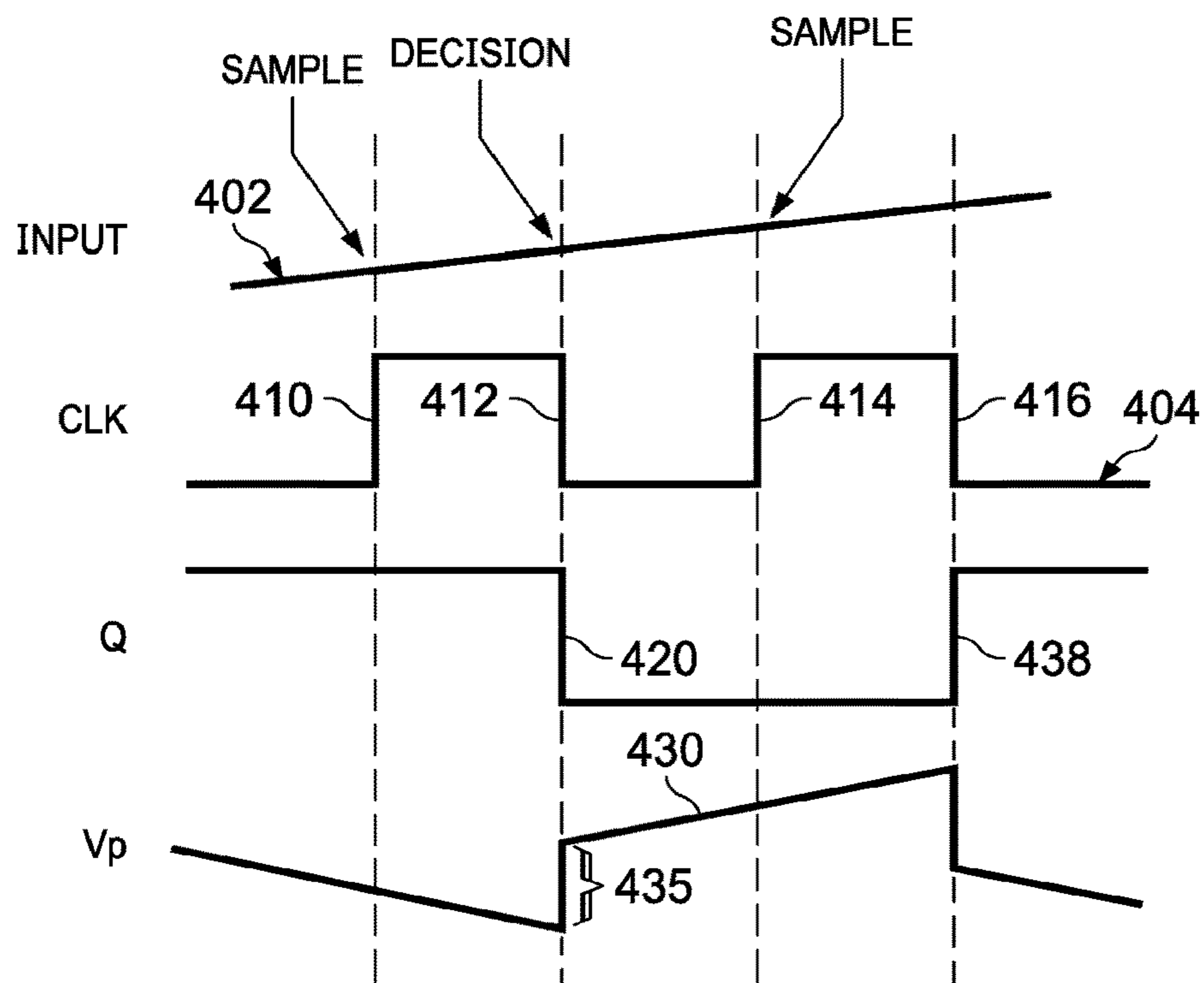


FIG. 4

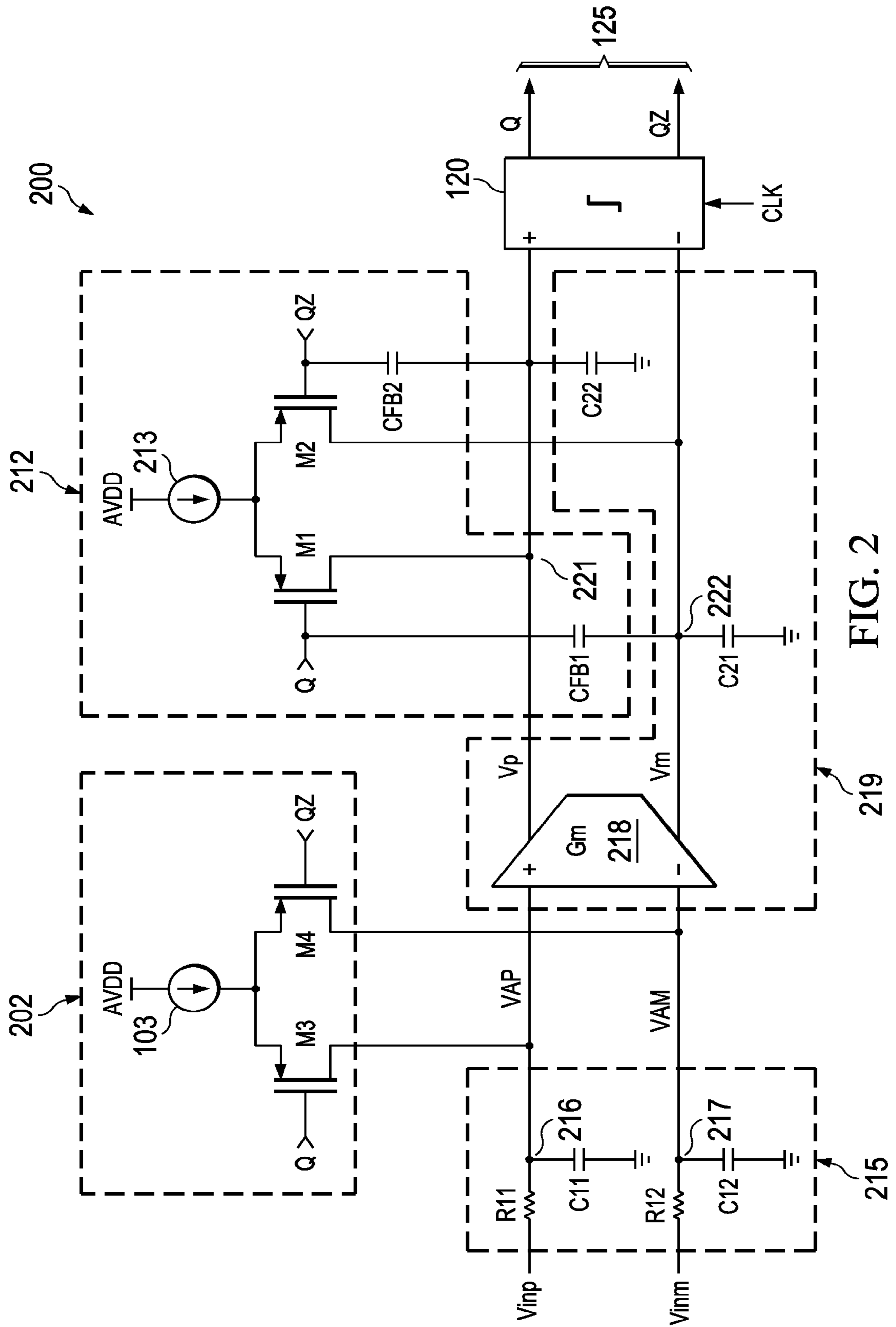


FIG. 2

LOOP DELAY COMPENSATION IN A DELTA-SIGMA MODULATOR

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 16/911,702, filed on Jun. 25, 2020, which is a continuation of U.S. patent application Ser. No. 16/583,510, filed on Sep. 26, 2019 (now U.S. Pat. No. 10,727,859), the subject matter of all is incorporated herein by reference.

BACKGROUND

An analog-to-digital converter (ADC) converts an input analog signal into a digital signal. One type of ADC includes a delta-sigma modulator in which a change in the analog input signal is encoded. The modulator includes, among other components, an integrator and a comparator. The output of the comparator is used to generate a feedback signal for the integrator. Continuous-time delta-sigma modulators suffer from excess loop delay due to the propagation delay through the comparator. The comparator samples the output signal from the integrator and compares the sampled output signal to a threshold. Any propagation delay through the comparator means that the feedback signal from the comparator is not based on the current comparator output signal but rather on a delayed comparator output signal. The comparator delay degrades the performance of the feedback loop, and the comparator delay can cause the modulator to be unstable.

SUMMARY

In one example, a delta-sigma modulator includes a first integrator and a comparator. The comparator's positive input couples to the first integrator's positive output, and the comparator's negative input couples to the first integrator's negative output. A first current DAC comprises a current source device, and first and second transistors. The first transistor has a first transistor control input and first and second current terminals. The first current terminal couples to the current source device, and the second current terminal couples to the first integrator positive output. The second transistor has a second transistor control input and third and fourth current terminals. The third current terminal couples to the current source device, and the fourth current terminal couples to the first integrator negative output. A first capacitive device couples to the second transistor control input and to both the second current terminal and the first integrator positive output.

BRIEF DESCRIPTION OF THE DRAWINGS

For a detailed description of various examples, reference will now be made to the accompanying drawings in which:

FIG. 1 is an example implementation of an ADC with a delta-sigma modulator.

FIG. 2 is another example implementation of an ADC with a delta-sigma modulator and including compensation for the delay introduced by the latch.

FIG. 3 is an example implementation of a capacitor used to compensate for the latch's delay.

FIG. 4 shows example waveforms of the ADC of FIG. 2.

DETAILED DESCRIPTION

FIG. 1 shows an example implementation of a second order delta-sigma modulator 100. In this example, the delta-

sigma modulator 100 includes integrators 115 and 119, a comparator 120, and current digital-to-analog converters (DACs) 102 and 112. Delay 121 is also shown and delay 121 represents the propagation delay through the comparator 120. Integrator 115 includes resistor R1 and capacitor C1. Integrator 119 includes transconductance amplifier (Gm) 118 and capacitor C2. An input voltage, V_{in} , is converted to a digital value which is provided to resistor R1. For simplicity, V_{in} is shown in FIG. 1 as single-ended signal, but V_{in} may comprise a differential signal (V_{inp} and V_{inm}) and is illustrated as such in the example of FIG. 2. The other terminal of resistor R1 is connected to capacitor C1 (which, in turn, is connected to ground) and to an input of Gm 118. The output of Gm 118 also is a differential signal comprising signals V_p and V_m and is coupled to capacitor C2 (which is connected to ground as shown) and to an input of comparator 120.

The output of comparator 120 also is used to control the current DACs 112 and 102. The output of comparator 120 is shown as Q and QZ. Output QZ is the logical inverse of Q. In one example, responsive to Q being logic high, current from current DAC 112 is injected into the node between Gm 118 and comparator 120 comprising V_p . Responsive to Q being low (QZ being high), current from current DAC 112 is injected into the node comprising V_m . Current from current DAC 112 is injected into one, but not both, of the nodes comprising V_p or V_m depending on the state of the Q output of comparator 120. Similarly, current from current DAC 102 is injected into the positive signal node between the integrator 115 and the Gm 119 when Q is high, whereas current from the current DAC 102 is injected into the negative signal node between the integrator 115 and Gm 119 when Q is low.

As noted above, delay 121 represents the propagation delay through the comparator 120. FIG. 1 illustrates that the feedback loop comprising current DACs 102 and 112 uses the previous Q/QZ output from the comparator 120 while the comparator 120 is sampling new values of V_p and V_m . The delay introduced by comparator 120 can cause instability. One solution to the instability problem could be to add a pre-amplifier between integrator 119 and comparator 120, and a third current DAC to inject current into the node between the pre-amplifier and the comparator 120. Such a system would include three feedback loops, with the third feedback loop used to compensate the delay 121 caused by the comparator 120. This system would have three current DACs and a pre-amplifier resulting in a relatively complicated design.

FIG. 2 shows another example implementation of a delta-sigma modulator 200. In the example of FIG. 2, the delta-sigma modulator 200 includes integrators 215 and 219, comparator 120, and current DACs 202 and 212. The input voltage comprises V_{INP} and V_{INM} . The integrator 215 includes two resistor-capacitor pairs R11/C11 and R12/C12. Each input voltage V_{INP}/V_{INM} is provided to its respective resistor R11/R12, and each resistor R11/R12 is connected to its respective capacitor C11/C12 at node 216/217 as shown. The voltage on node 216 is designated V_{AP} and the voltage on node 217 is designated V_{AM} . The positive input of GM 218 is coupled to resistor R11 and capacitor C11 at node 216. The negative input of GM 218 is coupled to resistor R12 and capacitor C12 at node 217. In this example, resistors R11 and R12 have the same resistance and capacitors C11 and C12 have the same capacitance. As such, voltage V_{AP} is provided to the positive input of the GM 218, and voltage V_{AM} is provided to the negative input of the GM 218. The output of GM 218 comprises a differential voltage formed by

voltages VP and VM. The positive output of the GM 218 is coupled to a positive input of comparator 120 at node 221, and the negative output of GM 218 is coupled to a negative input of comparator 120 at node 222. A capacitor C21 is coupled between 222 and ground as shown. Similarly, a capacitor C22 is coupled between node 221 and ground. Capacitors C21 and C22 have the same capacitance in this example. Comparator 120 includes a Q output and its logical inverse, QZ. A clock signal (CLK) is used to cause the comparator 120 to sample the input VPNM.

Current DAC 202 comprises a current source device 103 and a pair of P-type metal oxide semiconductor field effect transistors (PMOS) M3 and M4. In other examples, transistors M3 and M4 can be implemented as different types of transistors. The sources of transistors M3 and M4 are connected to the current source device 103. The drain of transistor M3 is connected to node 216 (VAP), and the drain of transistor M4 is connected to node 217 (VAM). The gate of transistor M3 is coupled to the Q output of comparator 120, and the gate of transistor M4 is coupled to the QZ output of comparator 120. When Q is low and QZ is high, transistor M3 is on and transistor M4 is off, and current from current source device 103 flows through transistor M3 into node 216. Reciprocally, when Q is high and QZ is low, transistor M3 is off, transistor M4 is on, and current from current source device 103 flows through transistor M4 into node 217. As such, the current from current source device 103 flows either into node 216 or node 217 based on the logical state of the output of comparator 120.

Current DAC 212 includes a current source device 213, transistors M1 and M2, and feedback compensation capacitors CFB1 and CFB2. Capacitors CFB1 and CFB2 have the same capacitance in this example. Transistors M1 and M2 comprise PMOS transistors in this example but can be implemented as other types of transistors in other examples. The sources of transistors M1 and M2 are connected to current source device 213. The drain of transistor M1 is connected to node 221 (VP), and the drain of transistor M2 is connected to node 222 (VM). Feedback capacitor CFB1 is connected between the gate of transistor M1 and node 222 (VM). Feedback capacitor CFB2 is connected between the gate of transistor M2 and node 221 (VP). The gate of transistor M1 is controlled by the Q output of comparator 120, and the gate of transistor M2 is controlled by the QZ output of comparator 120.

Feedback capacitors CFB1 and CFB2 compensate the feedback loop for the propagation delay of comparator 120. The feedback coefficient is $AVDD \cdot CFB / (CFB + C2)$, where AVDD is the supply voltage, CFB refers to the capacitance of CFB1 (or CFB2), and C2 refers to the capacitance of C21 (or C22). Capacitors CFB1 and CFB2 represent compensation capacitors and their use to compensate for the delay due the comparator 120 is described below.

In one example, capacitors CFB1 and CFB2 are capacitive devices implemented as actual capacitors. In another example as in FIG. 3, each CFB1/CFB2 capacitor is implemented as a transistor device (e.g., PMOS device) whose drain and source are connected together as shown.

FIG. 4 shows a timing diagram including an input signal 402, the clock signal (CLK) 404, the Q output of comparator 120, and the VP voltage. The input signal 402 represents the difference in voltage between VP and VM (output of Gm 218). In this example the input signal 402 is increasing as shown. The clock signal 404 is used to clock the comparator 120, and has rising edges 410 and 414, and falling edges 412 and 416 as shown. The comparator 120 samples the output signal from GM 218 (VP, VM) at rising edges 410 and 414

of the clock signal 404. The Q and QZ outputs from comparator 120 are available at falling edges 412 and 416. When Q transitions from high to low at 420, transistors M1 and M3 are turned on in their respective current DACs, and current flows into nodes 221 and 216 and charges capacitors C11 and C22 connected to those nodes. As a result, the voltage (VP) across capacitor C22 connected to node 221 increases as shown at 430. Reciprocally, when Q transitions from low to high (at 438), transistors M2 and M4 are turned on in their respective current DACs, and current flows into nodes 222 and 217 and charges capacitors C12 and C21 connected to those nodes. As a result, the voltage (VM) across capacitor C21 connected to node 222 will decrease.

In the absence of compensation capacitors CFB1 and CFB2, the voltages on nodes 221 and 22 will be only linearly increase/decrease due to charging/discharging of the current into capacitors C21/C22. Capacitors CFB1/CFB2 are added in series with capacitors C21/C22 as shown, so that when Q/Qz makes a transition, a voltage division occurs based on the ratios of CFB1/C21 and CFB2/C22. For example, if Q is transitioning from 1.2 V to 0 V (falling edge 420), and the ratio of the capacitances of CFB2 to C22 is 0.1, then a voltage level step up of approximately 120 mV will be seen at capacitor C22, as illustrated at 435. Voltage jump 435 is equivalent to adding a constant voltage when Q is high (or subtracting a constant voltage when Q is low) at the output of GM 218. This voltage addition serves as the compensation for the delay of comparator 120. A corresponding step down on the voltage level of VM on node 222 will occur when M1 turns off and M2 turns on.

In this description, the term “couple” or “couples” means either an indirect or direct wired or wireless connection. Thus, if a first device couples to a second device, that connection may be through a direct connection or through an indirect connection via other devices and connections. The recitation “based on” means “based at least in part on.” Therefore, if X is based on Y, X may be a function of Y and any number of other factors. Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

What is claimed is:

1. A modulator, comprising:

- a first integrator having an input node and a first integrator output;
- a first digital-to-analog converter (DAC) coupled to the first integrator output;
- a second integrator having a second integrator input and a second integrator output, the second integrator input coupled to the first integrator output;
- a comparator having a comparator input and a comparator output, the comparator input directly coupled to the second integrator output;
- a second DAC coupled to the second integrator output; and
- a delay circuit having an input coupled to the comparator output and an output coupled to the first DAC and the second DAC.

2. The modulator of claim 1, further comprising a capacitive device coupled to the second DAC and to the second integrator output.

3. The modulator of claim 2, wherein a propagation delay of the comparator is compensated by the capacitive device.

4. The modulator of claim 2, wherein the capacitive device is a first capacitive device and the modulator further comprises:

- a second capacitive device coupled between the first capacitive device and a ground node.

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5. The modulator of claim 4, wherein:
the comparator output includes a first comparator output
and a second comparator output; and
the second comparator output is configured to output a
logical inverse of the first comparator output.

6. The modulator of claim 2, wherein the capacitive
device comprises a transistor with a first current terminal
and a second current terminal coupled together.

7. The modulator of claim 1, wherein the first integrator
comprises a resistor and a capacitor.

8. The modulator of claim 1, wherein the second integra-
tor comprises a transconductance amplifier and a capacitor.

9. The modulator of claim 1, wherein the input node of the
first integrator is a differential input node.

10. The modulator of claim 1, wherein the first DAC
comprises a current source, a first transistor, and a second
transistor.

11. The modulator of claim 1, wherein the first DAC and
the second DAC are coupled to the comparator output.

12. The modulator of claim 1, wherein the second DAC
further comprises a transistor with a first current terminal
and a second current terminal coupled together.

13. The modulator of claim 1, wherein the first DAC is
configured to:

inject current into a first node between the first integrator
and the second integrator when a signal from the
comparator is high; and

inject current into a second node between the first inte-
grator and the second integrator when the signal from
the comparator is low.

14. A modulator, comprising:

a first integrator having an input node and a first integrator
output;

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a first digital-to-analog converter (DAC) coupled to the
first integrator output;

a second integrator having a second integrator input and
a second integrator output, the second integrator input
coupled to the first integrator output;

a comparator having a comparator input and a comparator
output, the comparator input coupled to the second
integrator output;

a second DAC coupled to the second integrator output;
a first capacitive device coupled to the second DAC and
to the second integrator output; and

a second capacitive device coupled between the first
capacitive device and a ground node.

15. The modulator of claim 14, wherein:

the comparator output includes a first comparator output
and a second comparator output; and

the second comparator output is configured to output a
logical inverse of the first comparator output.

16. The modulator of claim 14, wherein a propagation
delay of the comparator is compensated by the first capaci-
tive device.

17. The modulator of claim 14, wherein the first integrator
comprises a resistor and a capacitor.

18. The modulator of claim 14, wherein the second
integrator comprises a transconductance amplifier and a
capacitor.

19. The modulator of claim 14, wherein the first DAC
comprises a current source, a first transistor, and a second
transistor.

20. The modulator of claim 14, wherein the first DAC and
the second DAC are coupled to the comparator output.

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