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(54) **QUANTUM PROCESSORS**

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(57) **ABSTRACT**

Systems and methods for fabricating a superconducting integrated circuit that includes wiring layers comprising low-noise material are described. A superconducting integrated circuit can be implemented in a computing system that includes a quantum processor. Such a superconducting integrated circuit includes a first set of one or more wiring layers that form a noise-susceptible superconducting device that can decrease processor when exposed to noise. The superconducting integrated circuit can further include a second set of one or more wiring layers that form a superconducting device that is less susceptible to noise. Fabricating a superconducting device that contains low-noise material can include depositing and patterning a wiring layer comprising a first material that is superconductive in a respective range of temperatures and depositing and pattern-
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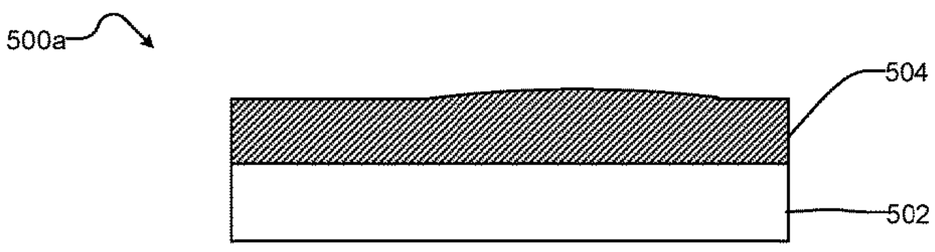

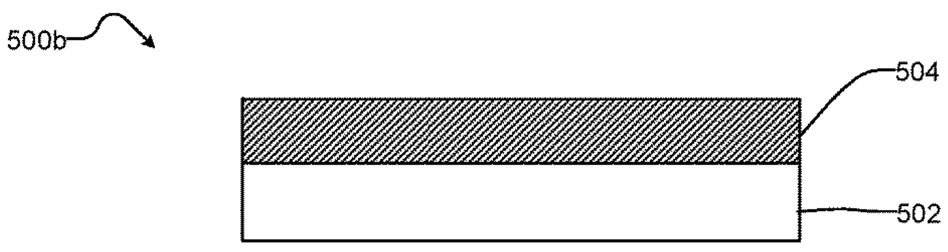

ing a different wiring layer comprising a second material that is superconductive in a respective range of temperatures. The second material can be considered a low-noise material.

18 Claims, 14 Drawing Sheets

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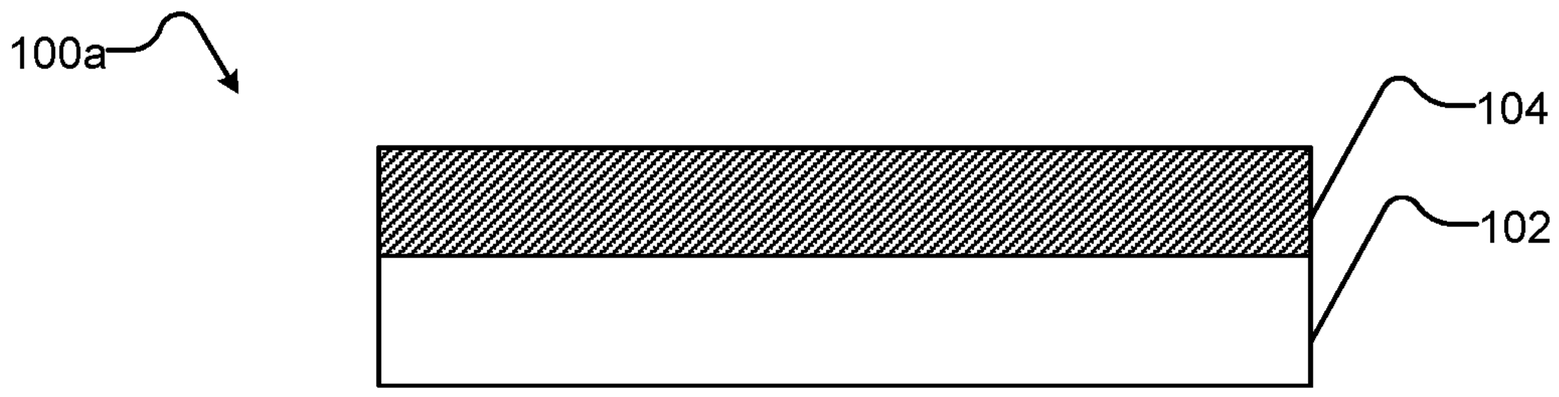

FIGURE 1A

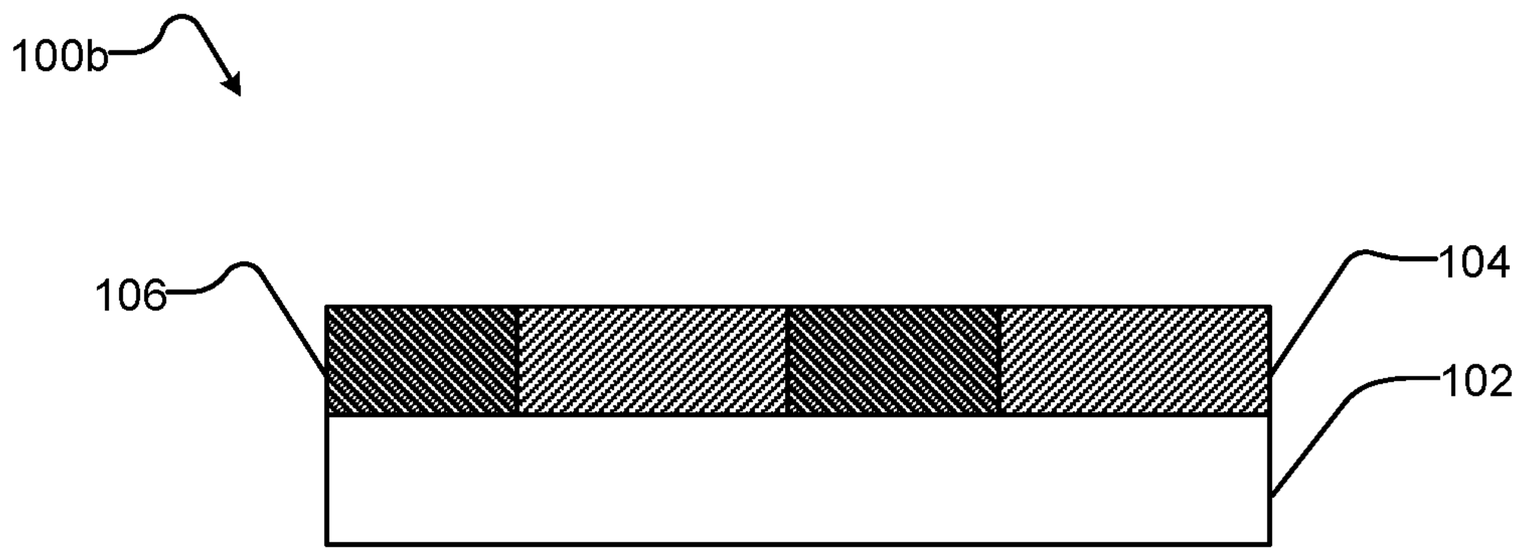

FIGURE 1B

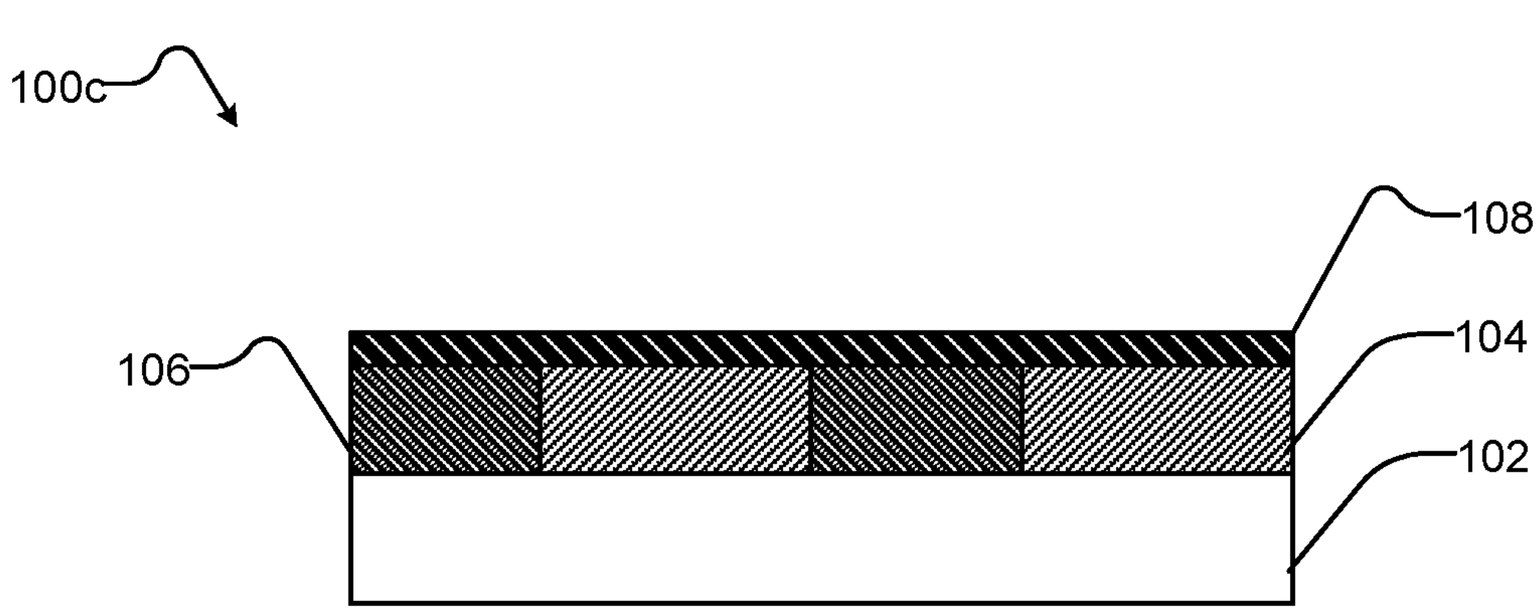

FIGURE 1C

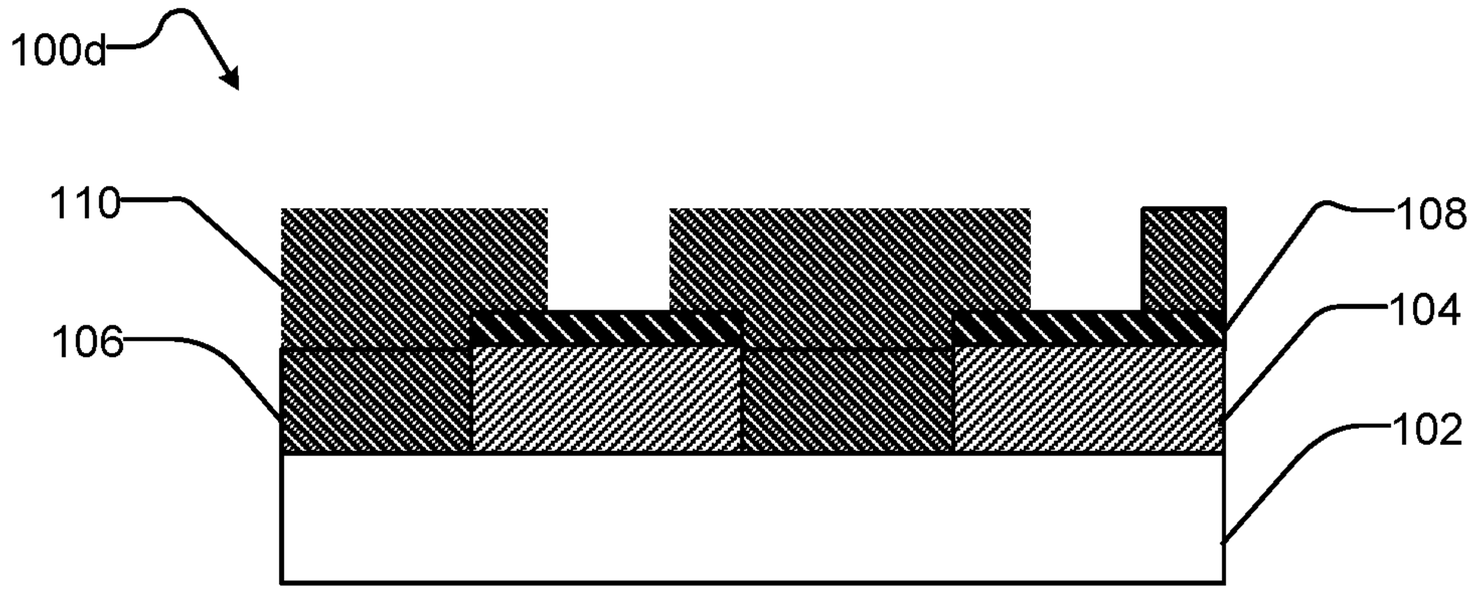

FIGURE 1D

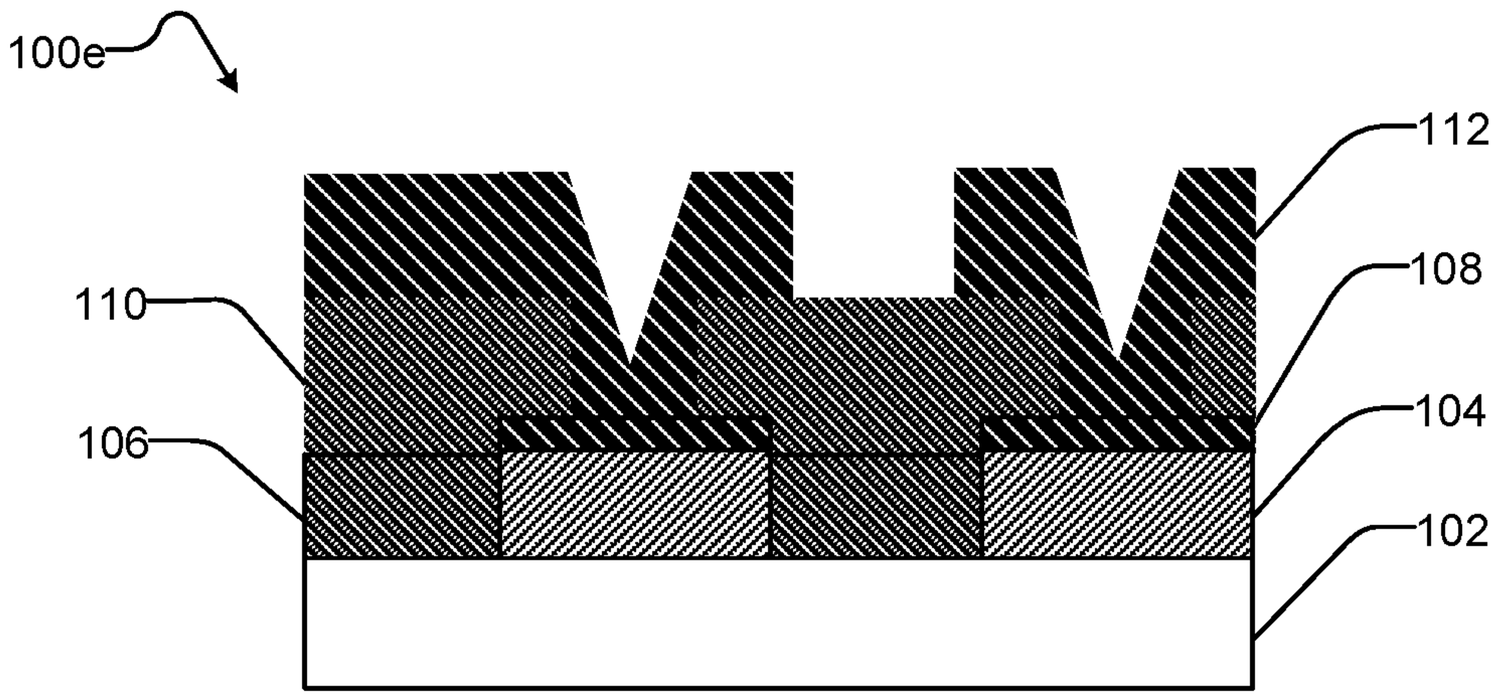

FIGURE 1E

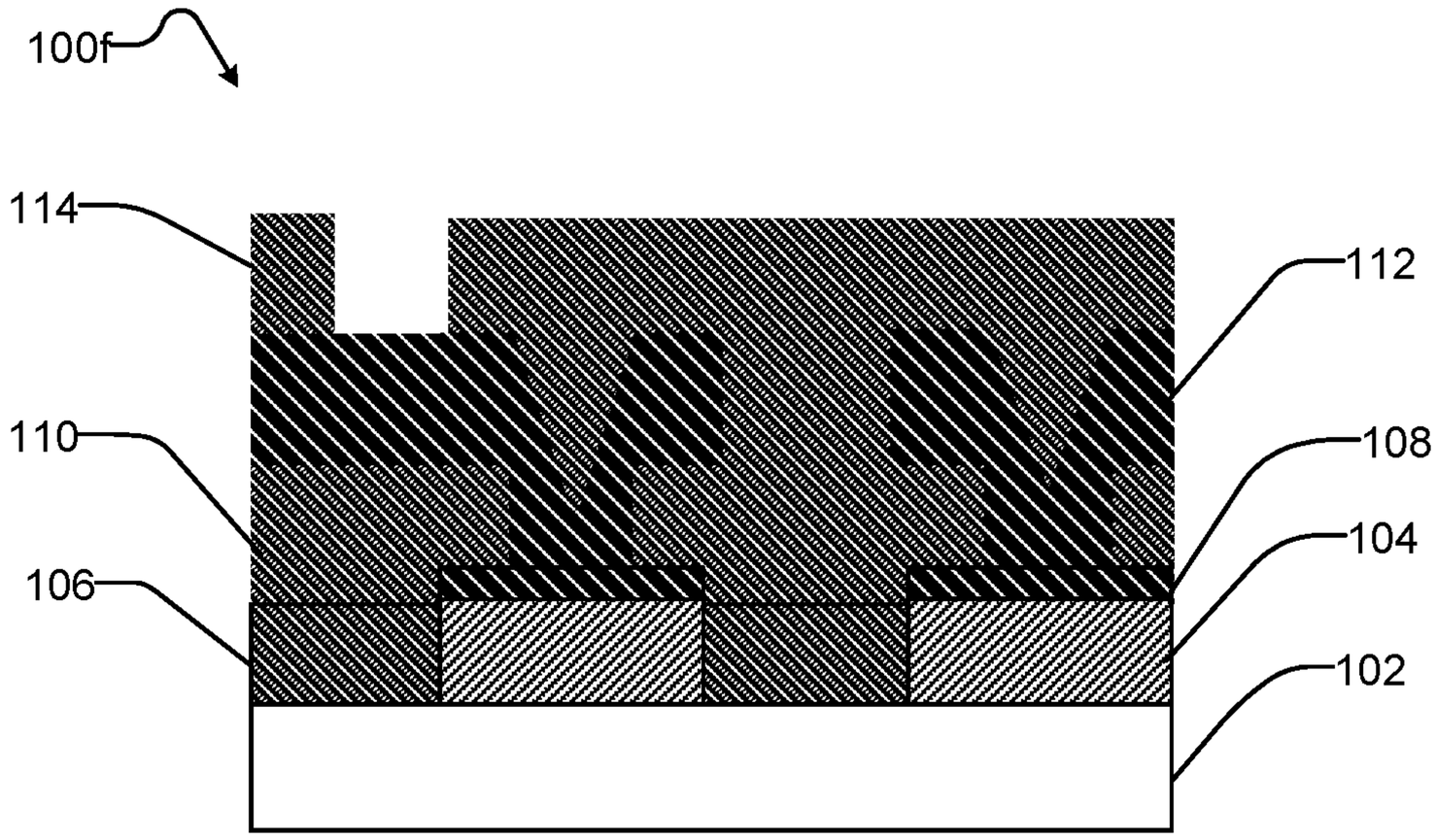

FIGURE 1F

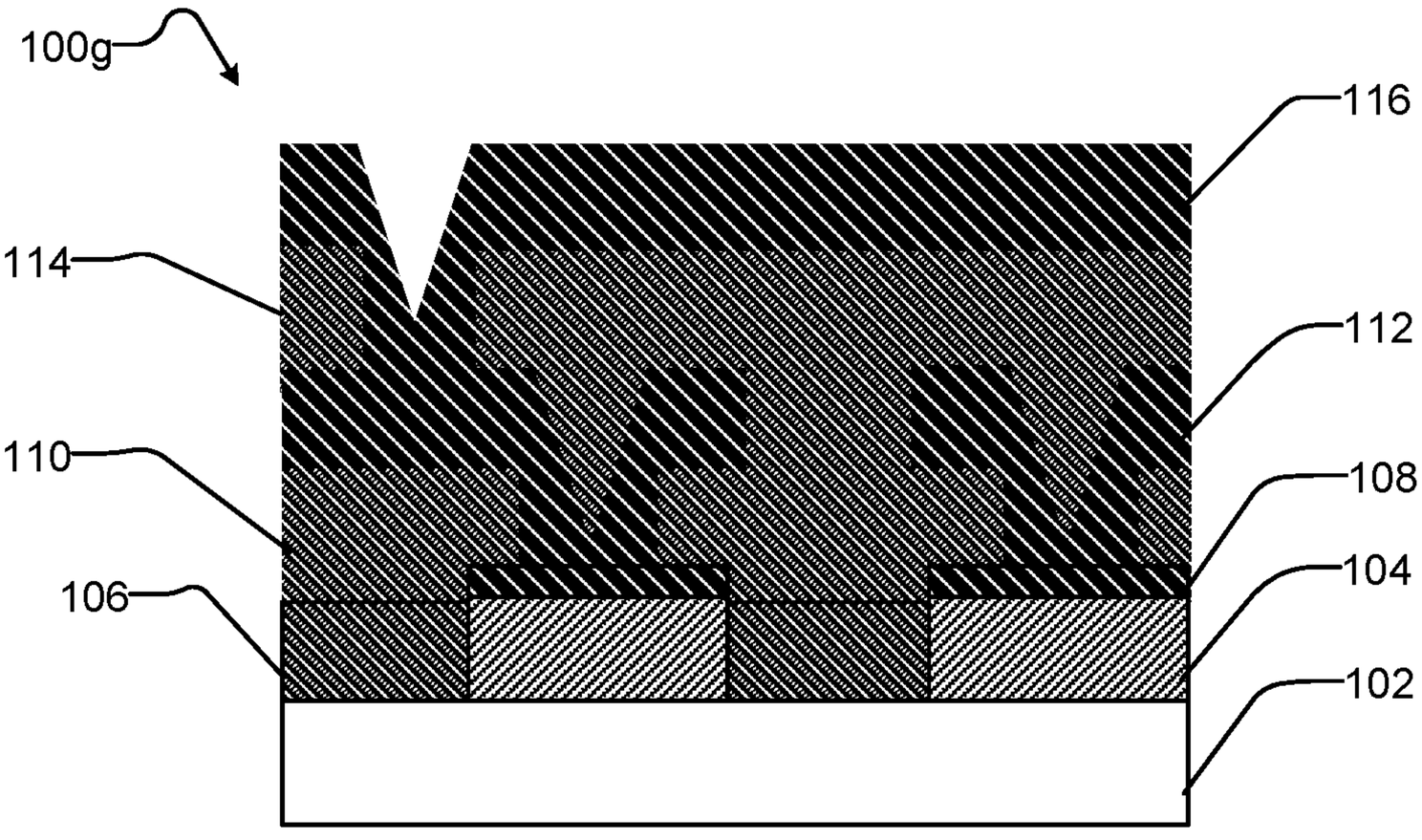

FIGURE 1G

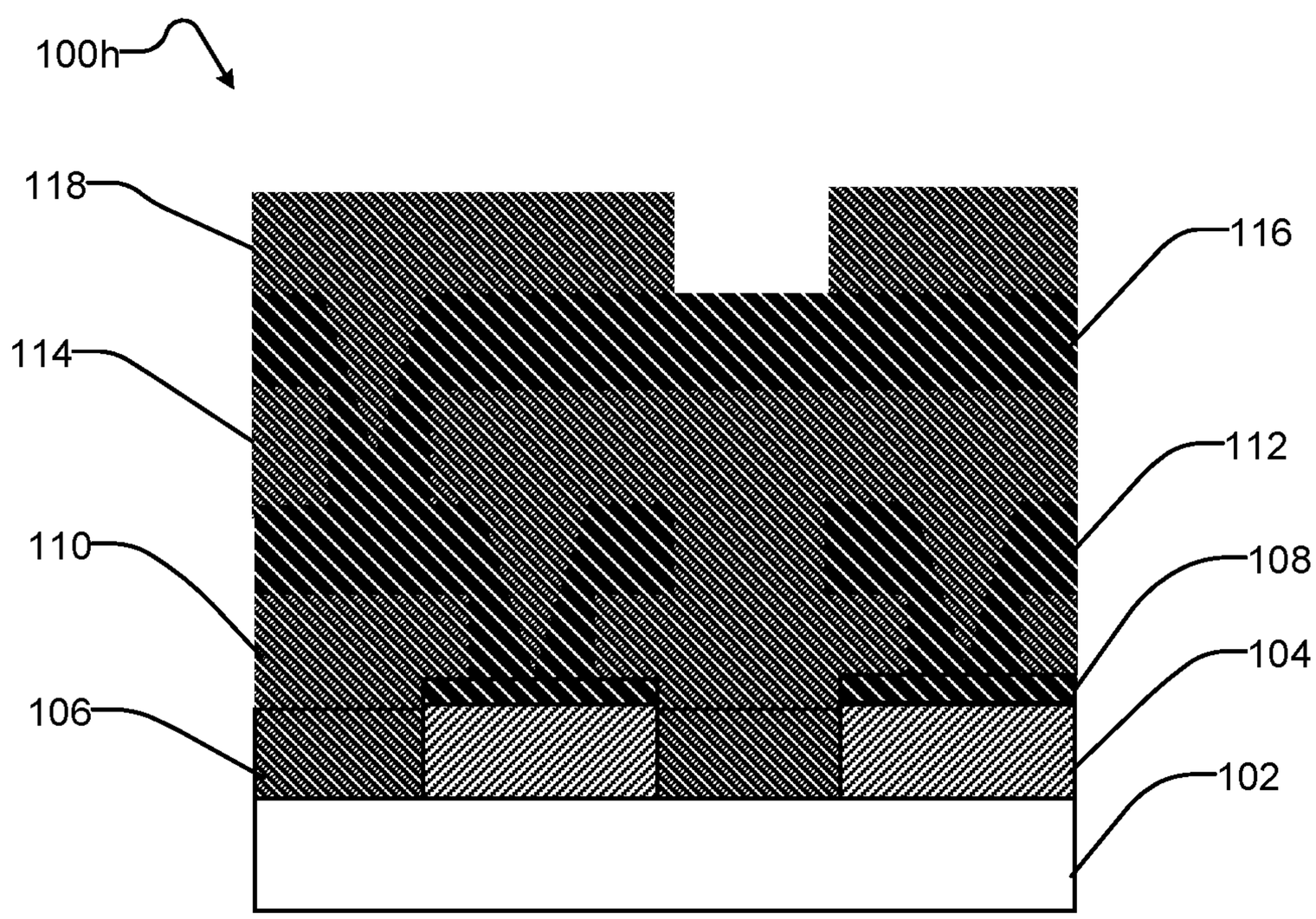

FIGURE 1H

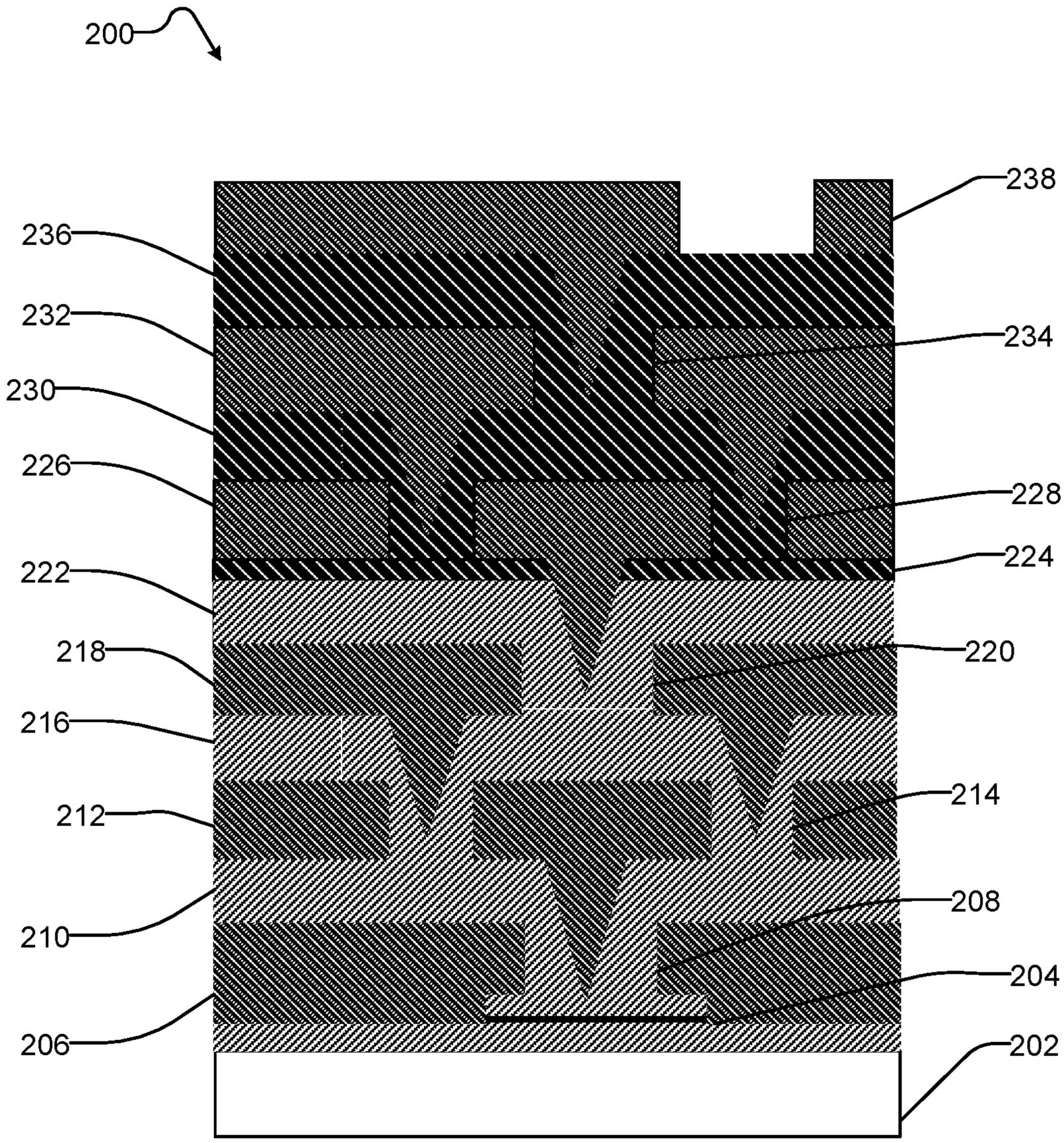
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FIGURE 2

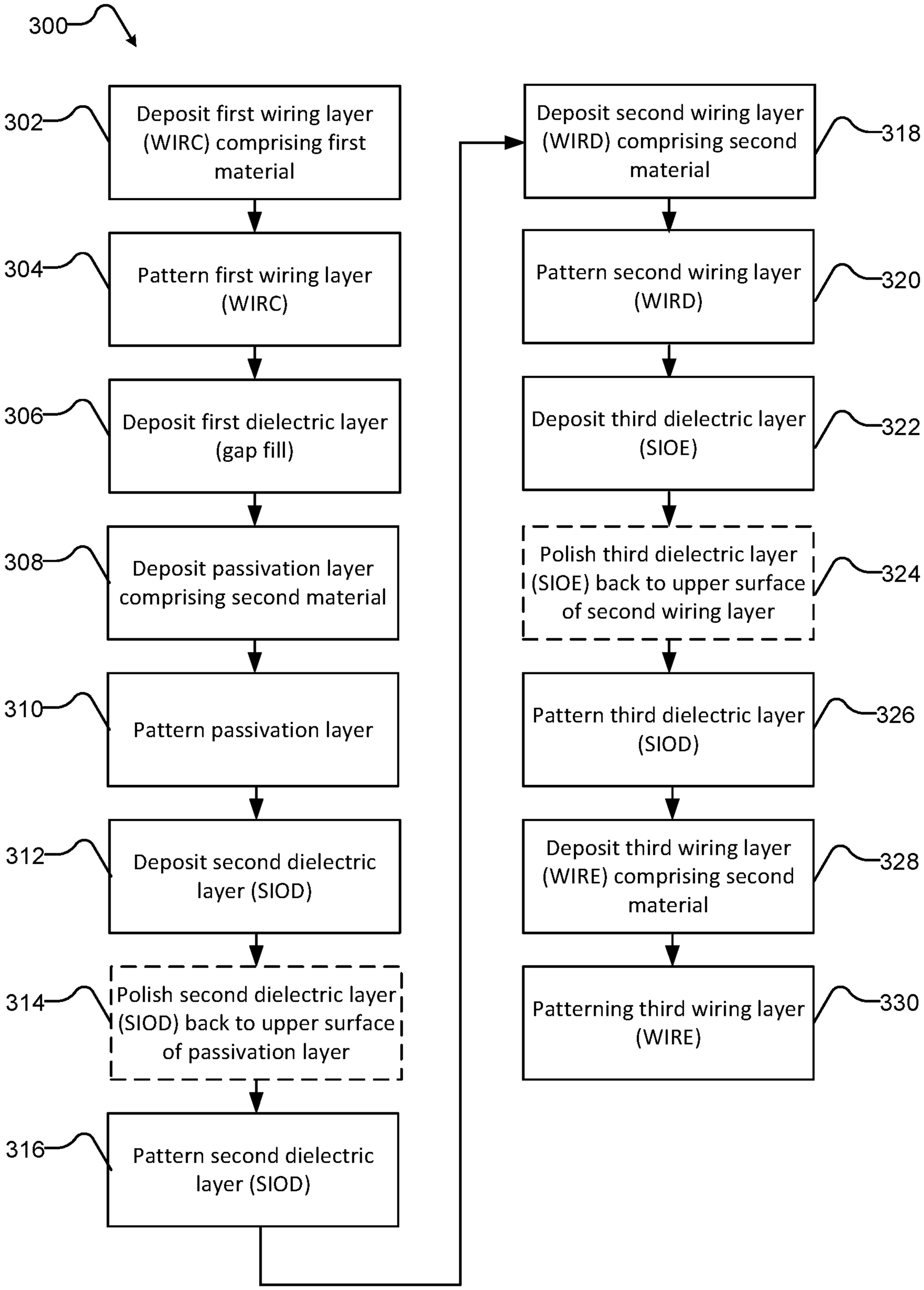
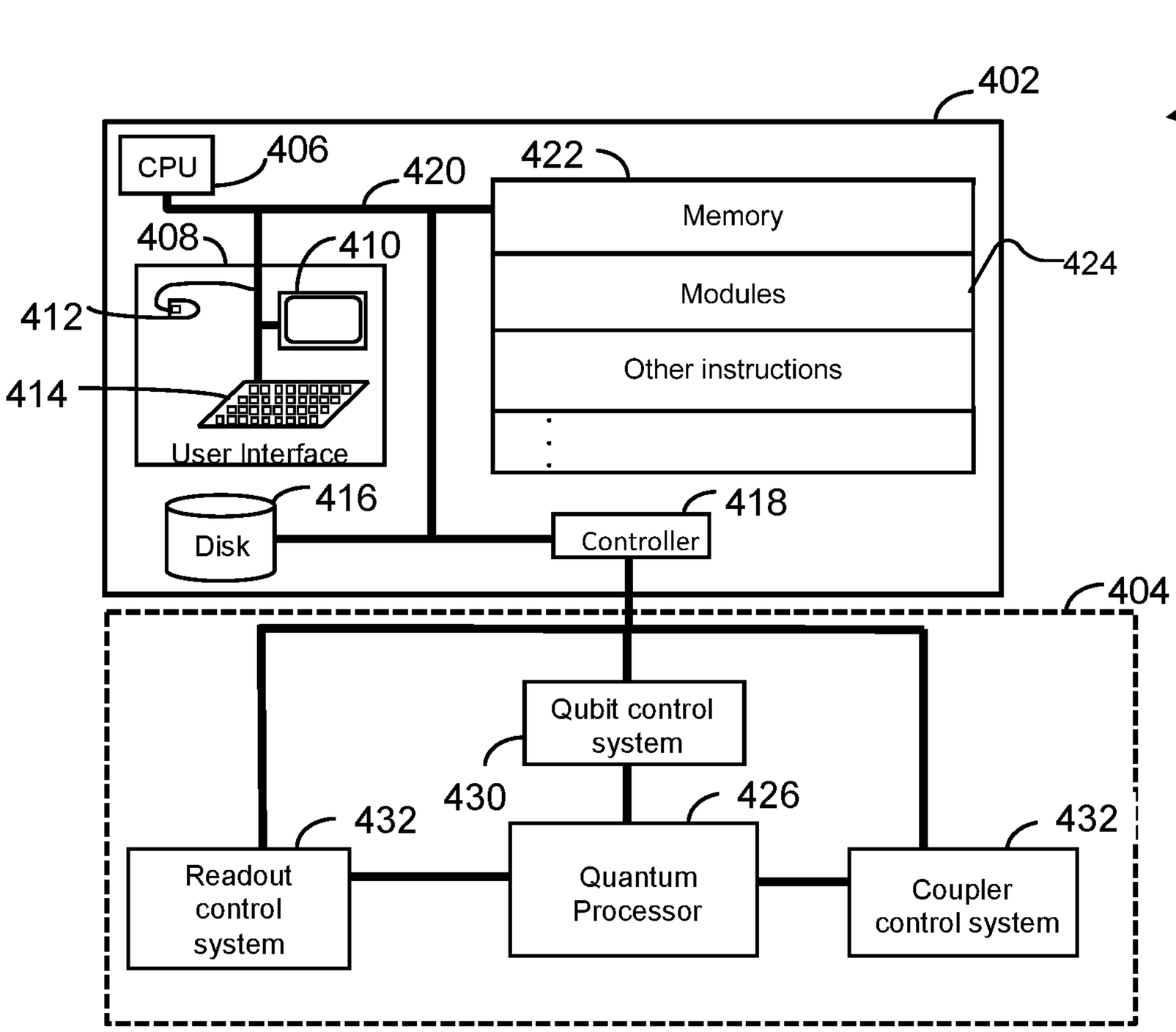

300
302
Deposit first wiring layer (WIRC) comprising first material
304
Pattern first wiring layer (WIRC)
306
Deposit first dielectric layer (gap fill)
308
Deposit passivation layer comprising second material
310
Pattern passivation layer
312
Deposit second dielectric layer (SIOD)
314
Polish second dielectric layer (SIOD) back to upper surface of passivation layer
316
Pattern second dielectric layer (SIOD)
318
Deposit second wiring layer (WIRD) comprising second material
320
Pattern second wiring layer (WIRD)
322
Deposit third dielectric layer (SIOE)
324
Polish third dielectric layer (SIOE) back to upper surface of second wiring layer
326
Pattern third dielectric layer (SIOD)
328
Deposit third wiring layer (WIRE) comprising second material
330
Patterning third wiring layer (WIRE)

FIGURE 3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Memory
Modules
Other instructions
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410
412
414
User Interface
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Disk
418
Controller
404
Qubit control system
430
426
432
Readout control system
Quantum Processor
Coupler control system
432

FIGURE 4

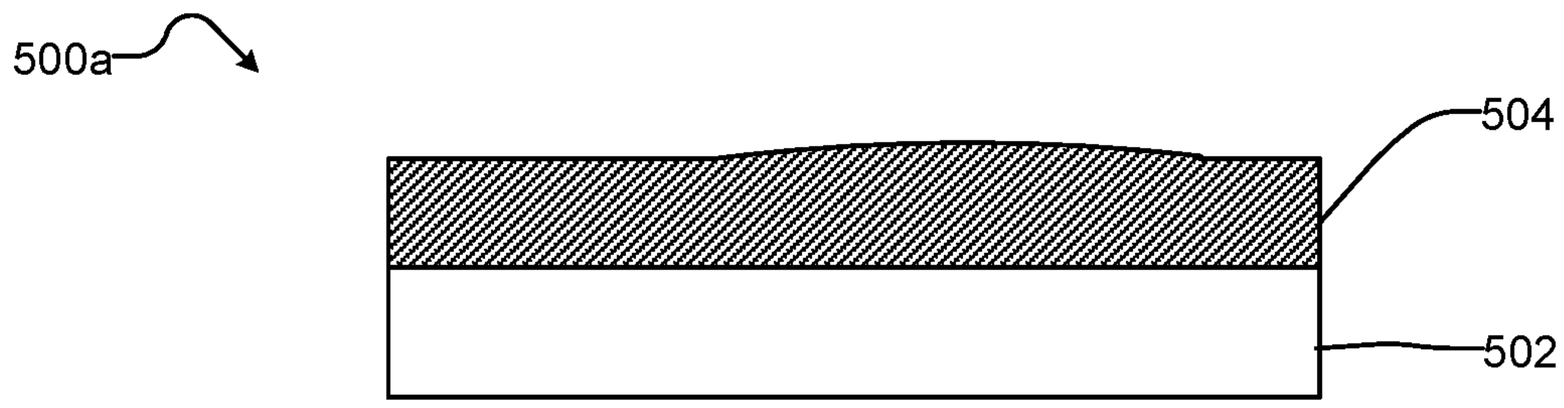

FIGURE 5A

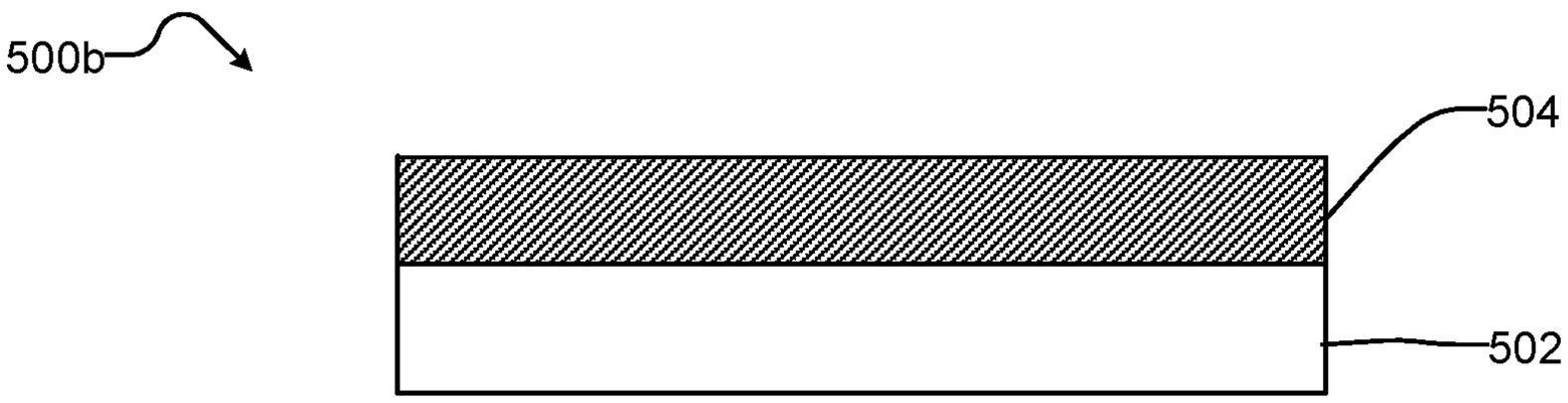

FIGURE 5B

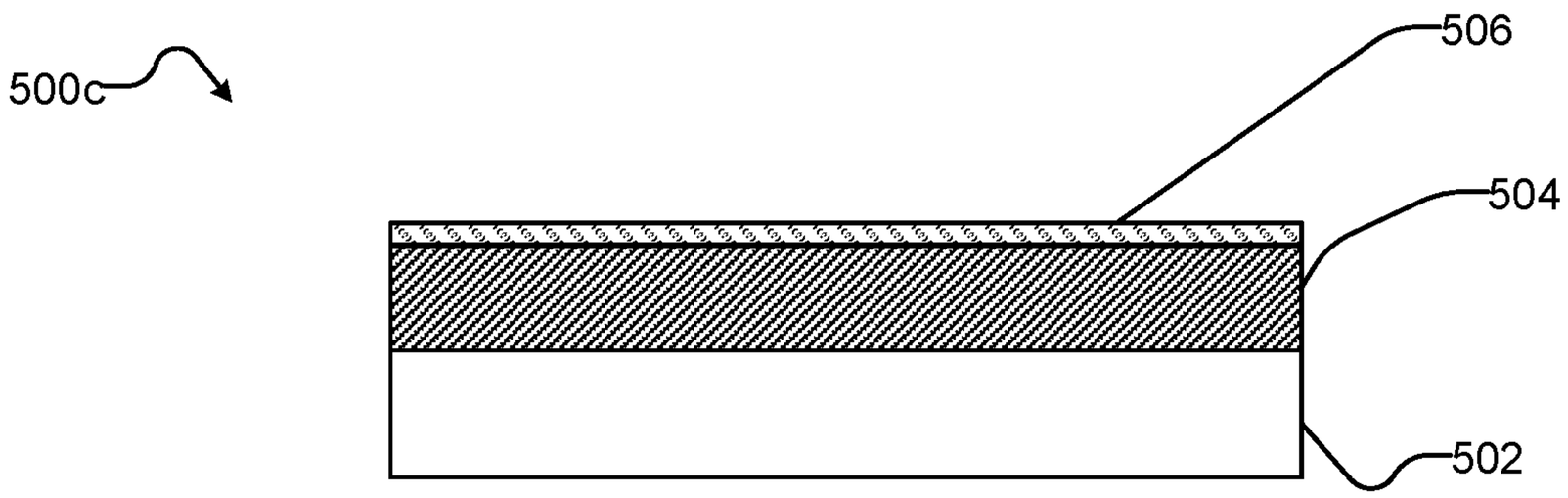

FIGURE 5C

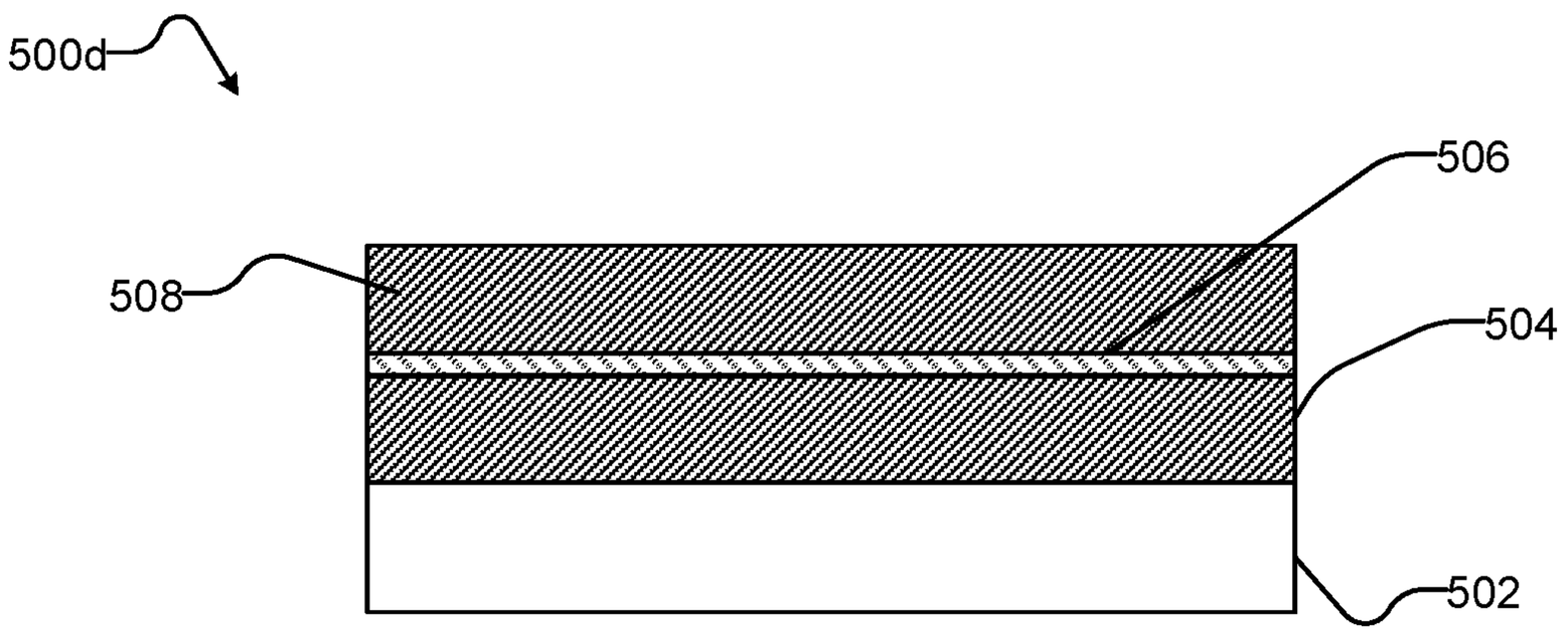

FIGURE 5D

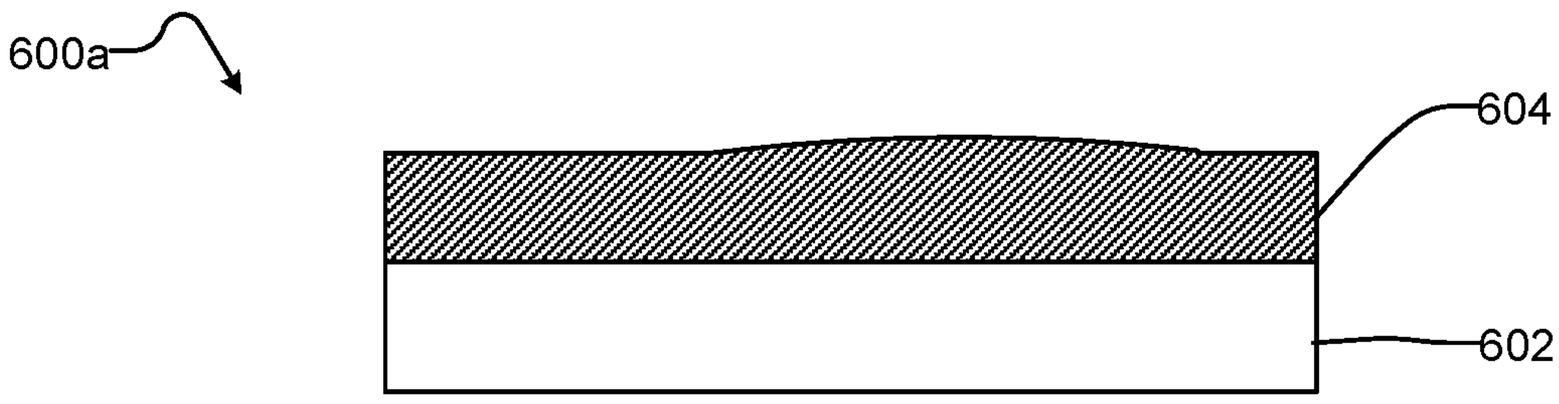

FIGURE 6A

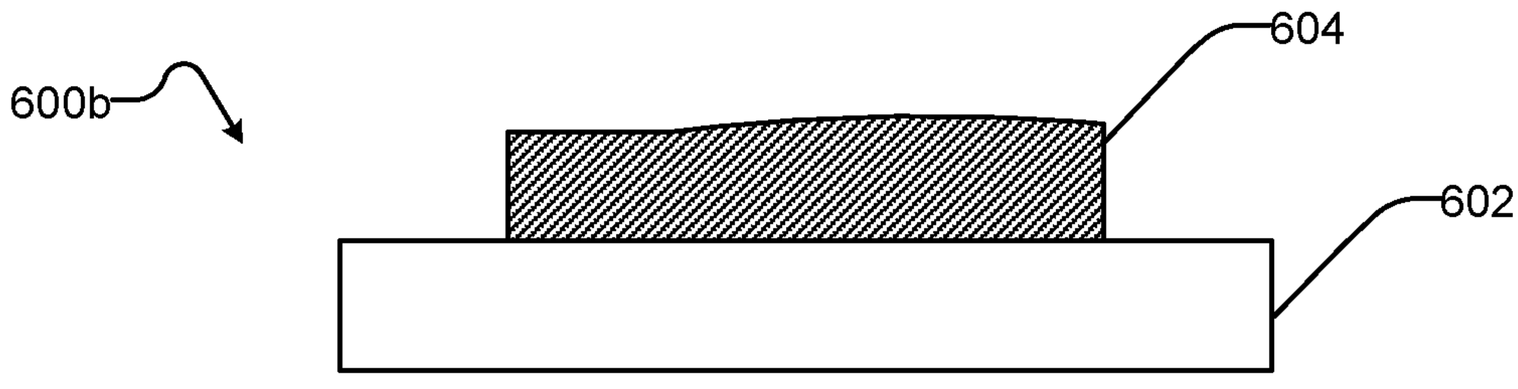

FIGURE 6B

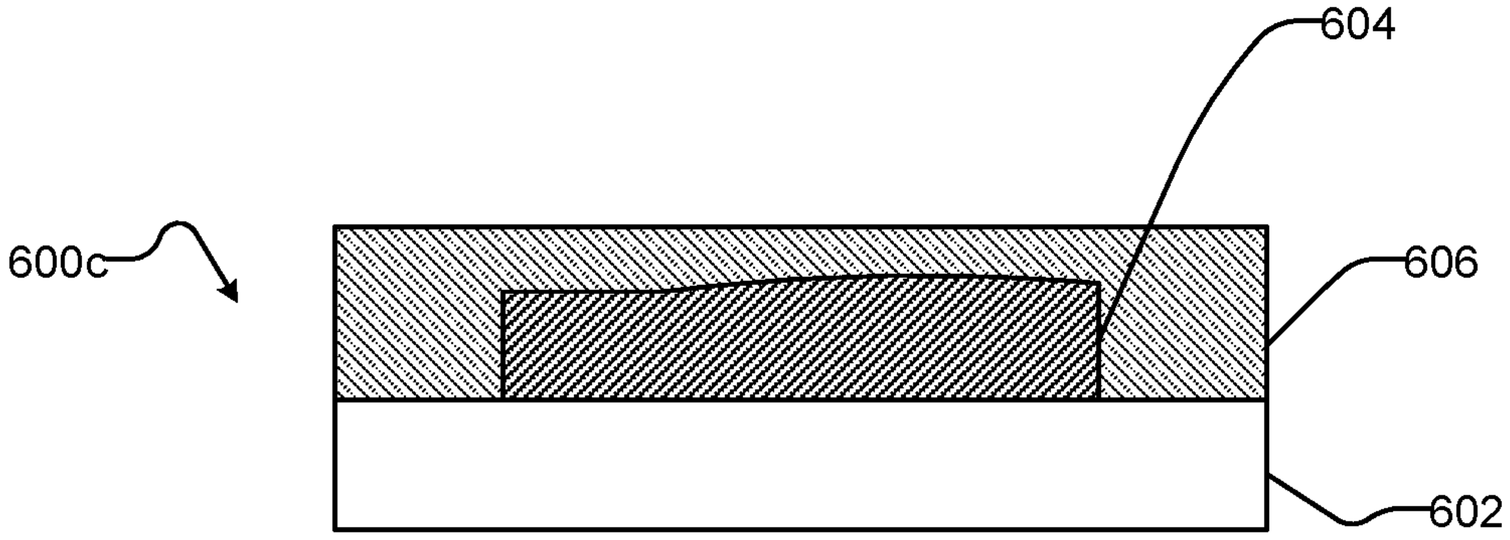

FIGURE 6C

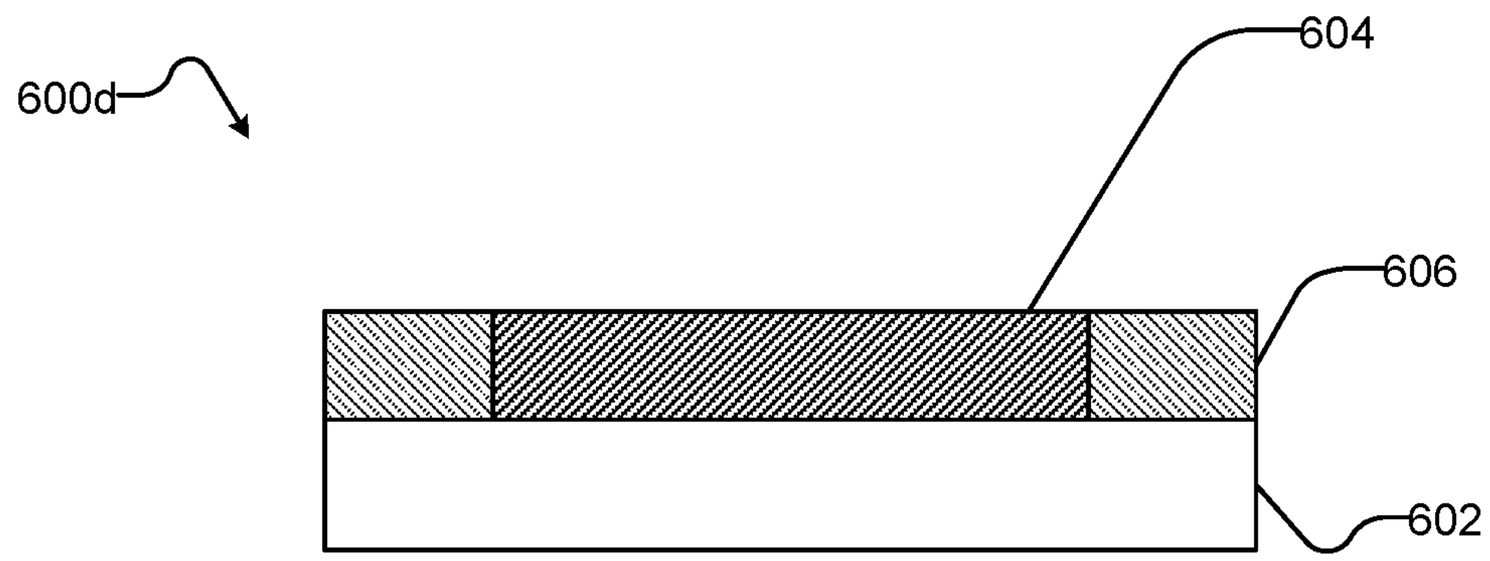

FIGURE 6D

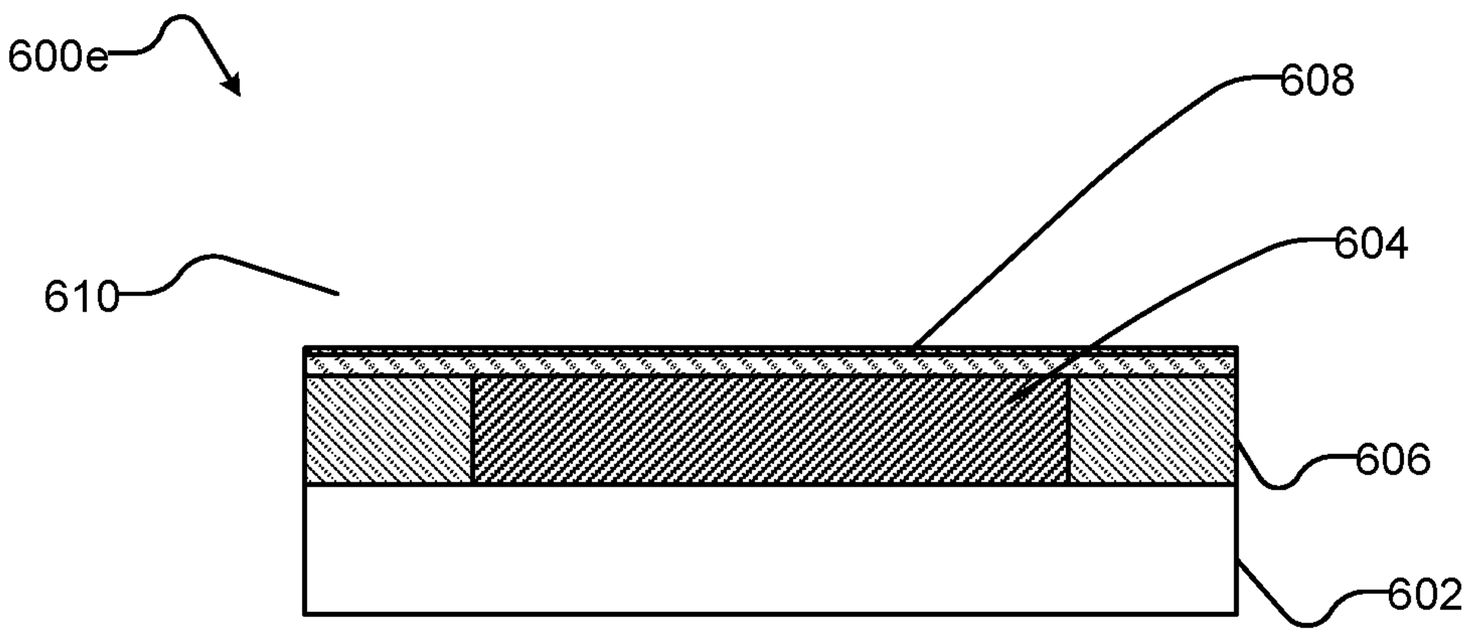

FIGURE 6E

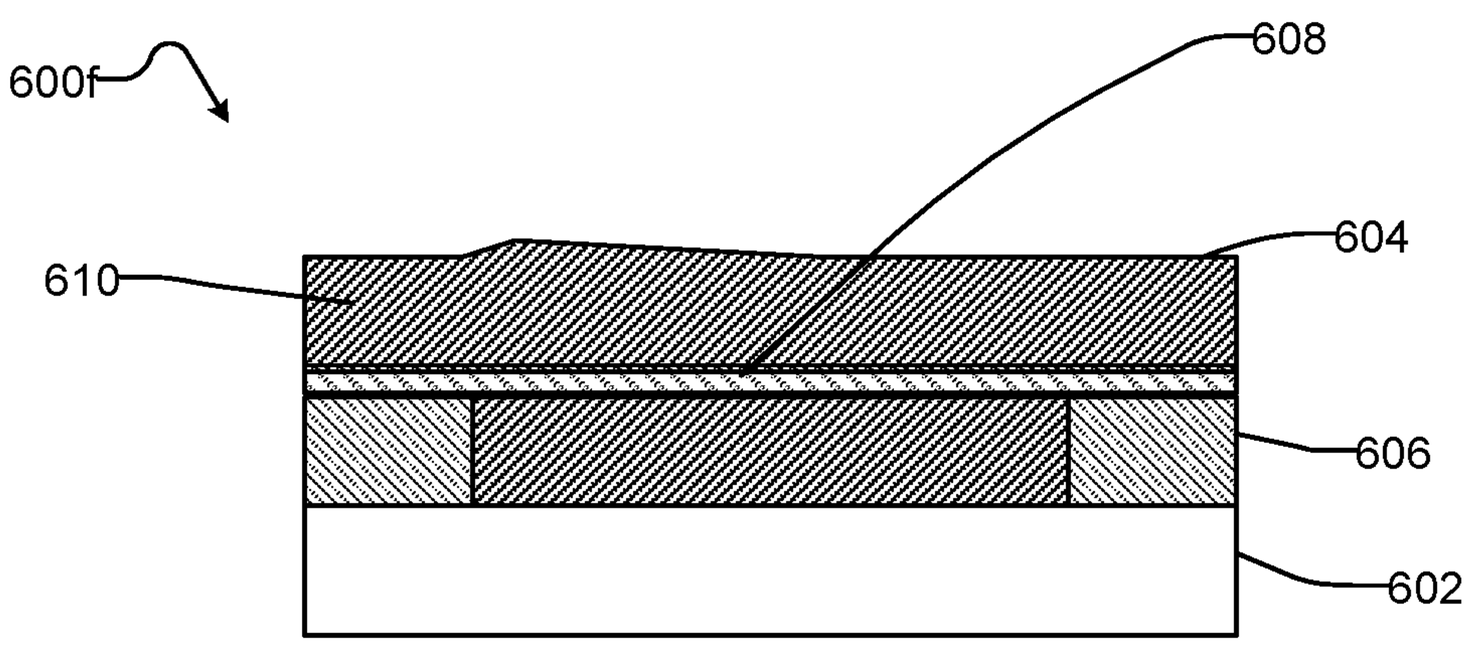

FIGURE 6F

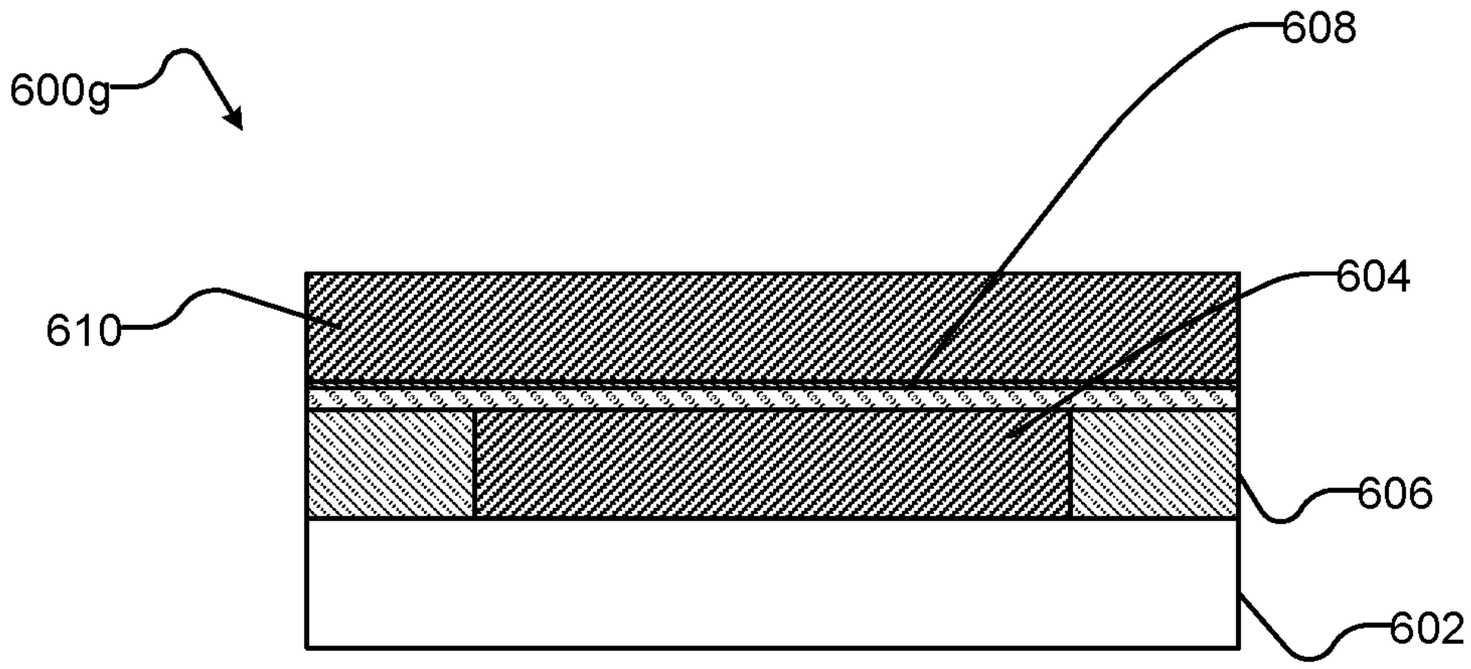

FIGURE 6G

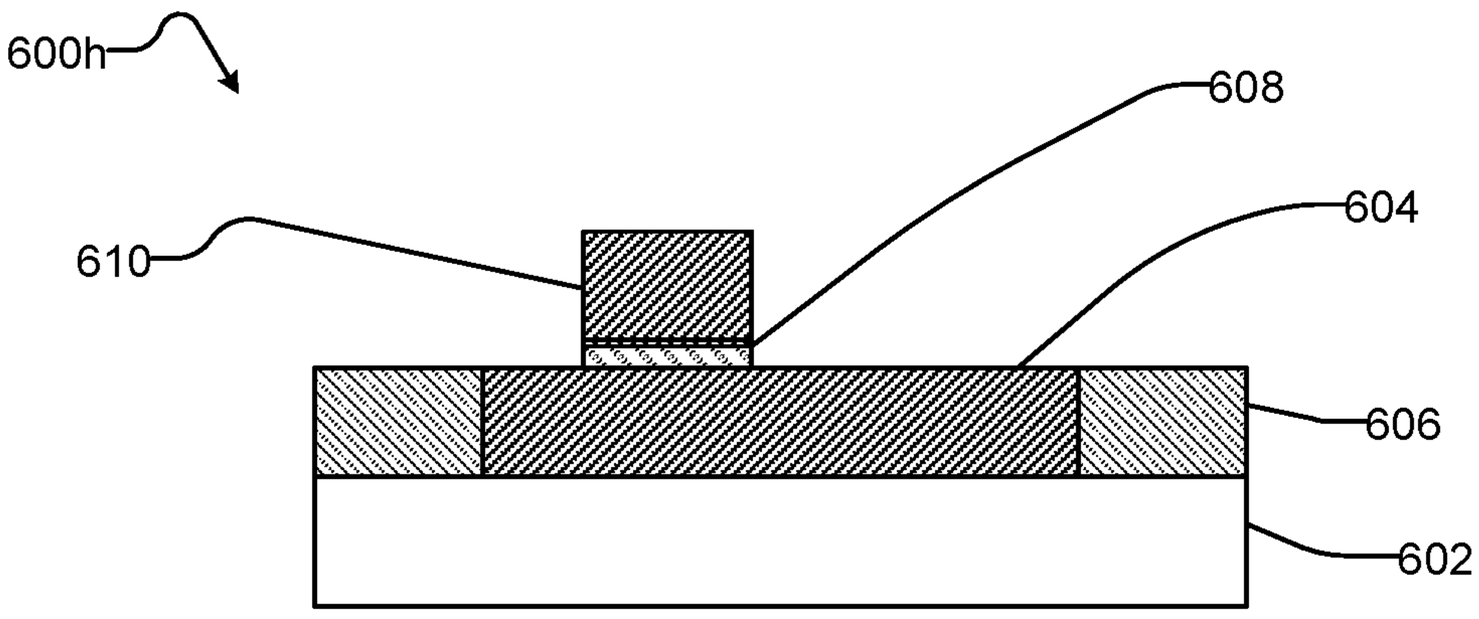

FIGURE 6H

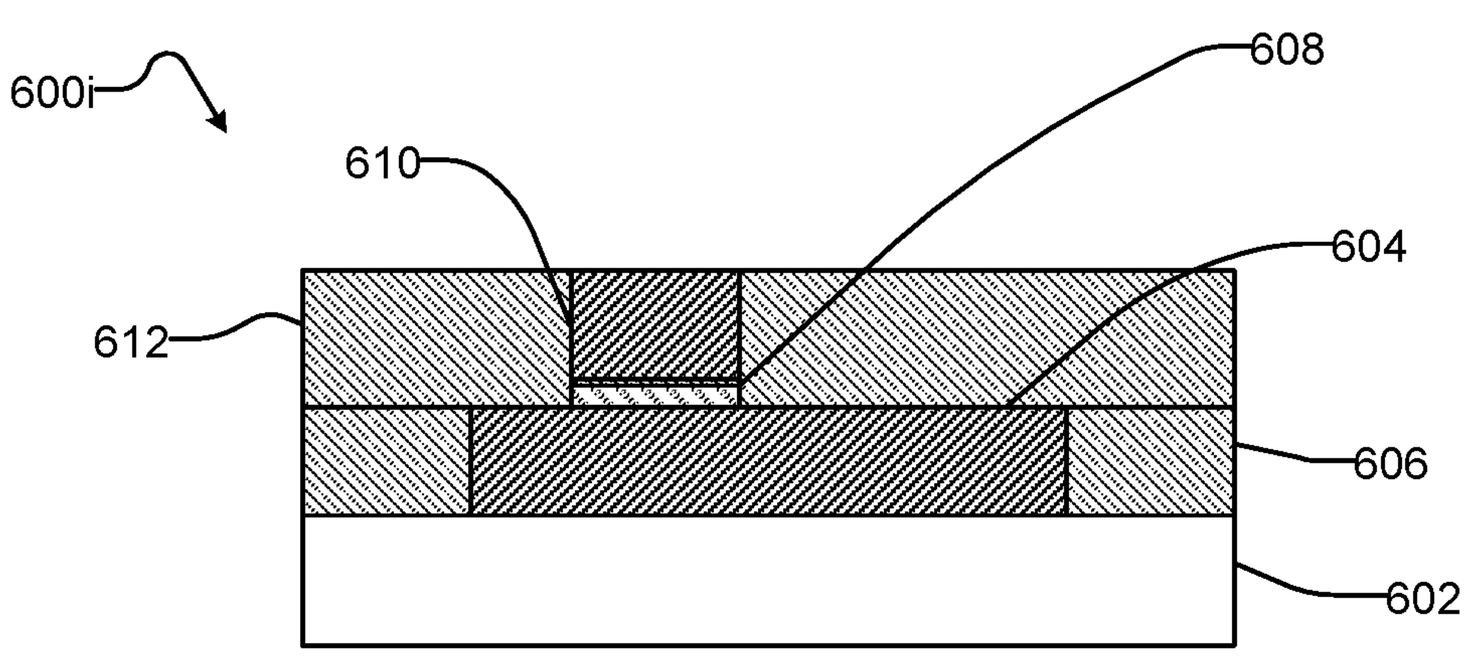

FIGURE 6I

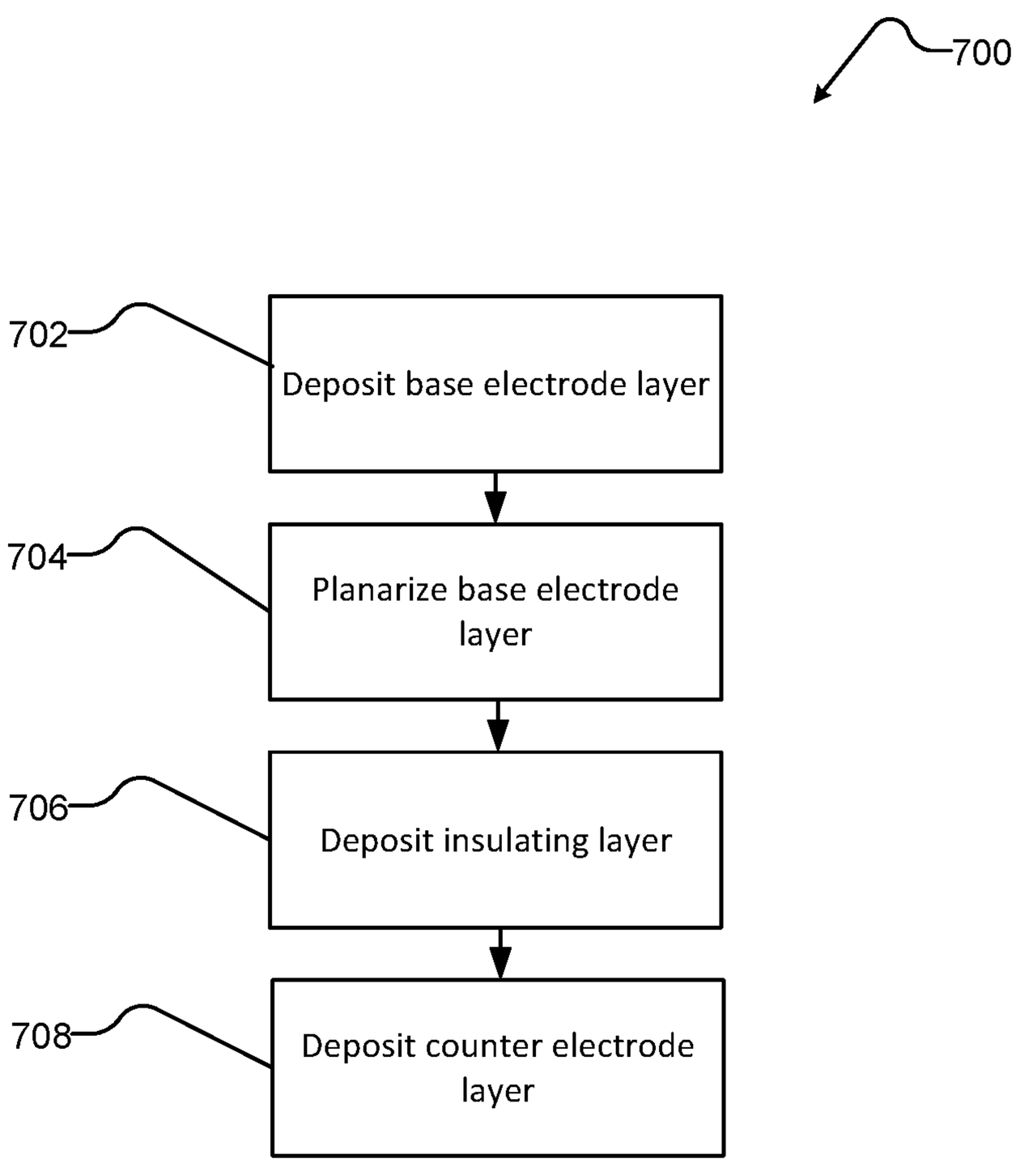
700
702
Deposit base electrode layer
704
Planarize base electrode layer
706
Deposit insulating layer
708
Deposit counter electrode layer

FIGURE 7

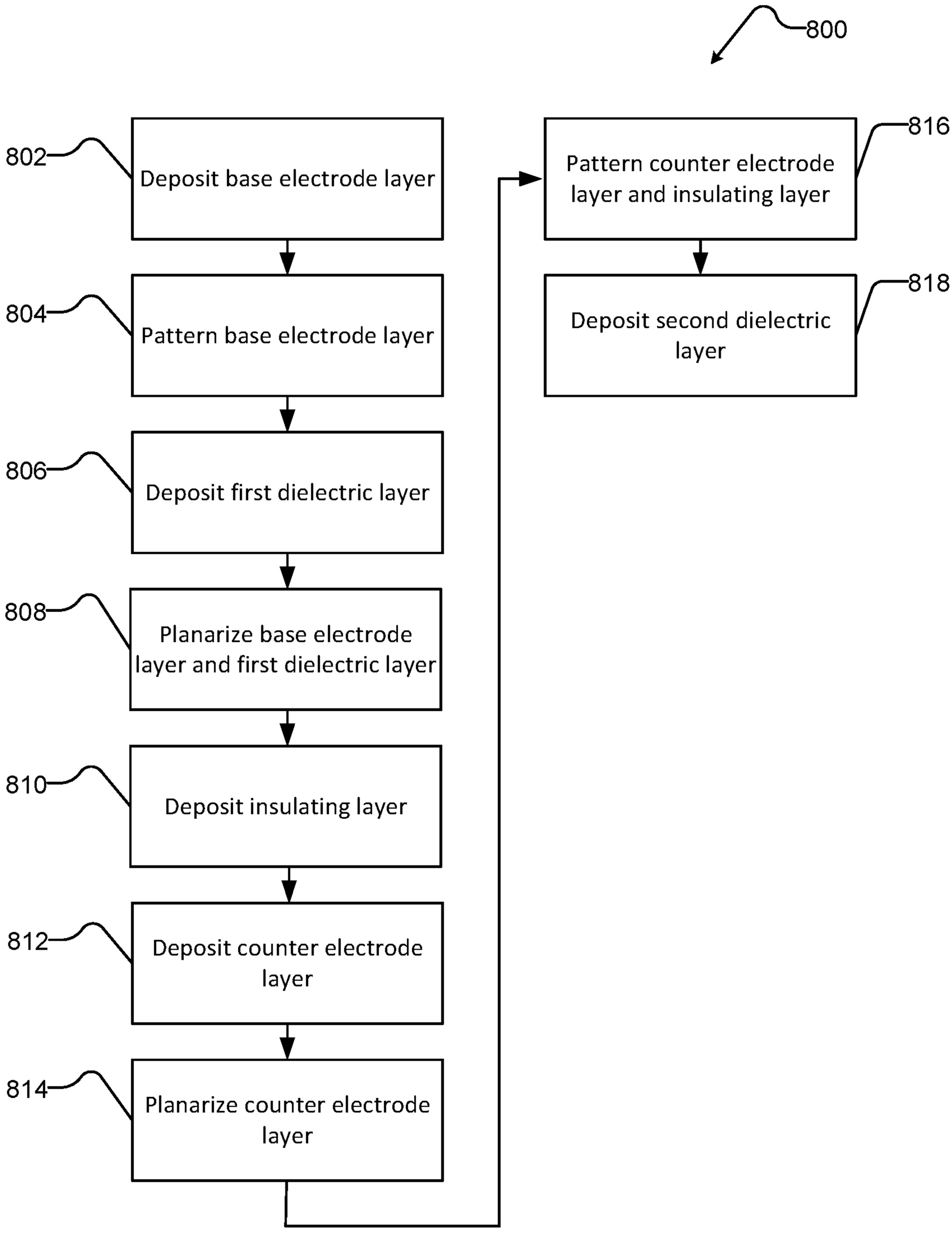
800
802
Deposit base electrode layer
804
Pattern base electrode layer
806
Deposit first dielectric layer
808
Planarize base electrode layer and first dielectric layer
810
Deposit insulating layer
812
Deposit counter electrode layer
814
Planarize counter electrode layer
816
Pattern counter electrode layer and insulating layer
818
Deposit second dielectric layer

FIGURE 8

QUANTUM PROCESSORS

FIELD

This disclosure generally relates to quantum processors, and in particular, relates to quantum processors that include a set of wiring layers comprising more than one type of material to reduce noise in superconductive devices and a base electrode that has been planarized.

BACKGROUND

Superconductive Processor

A quantum processor may take the form of a superconducting processor. However, superconductive processors can include processors that are not intended for quantum computing. For instance, some embodiments of a superconductive processor may not focus on quantum effects such as quantum tunneling, superposition, and entanglement but may rather operate by emphasizing different principles, such as for example the principles that govern the operation of classical computer processors. However, there may still be certain advantages to the implementation of such superconducting "classical" processors. Due to their natural physical properties, superconducting classical processors may be capable of higher switching speeds and shorter computation times than non-superconducting processors, and therefore it may be more practical to solve certain problems on superconducting classical processors. The present systems and methods are particularly well-suited for use in fabricating both superconducting quantum processors and superconducting classical processors.

Superconducting Qubits

Superconducting qubits are a type of superconducting quantum device that can be included in a superconducting integrated circuit. Superconducting qubits can be separated into several categories depending on the physical property used to encode information. For example, they may be separated into charge, flux and phase devices. Charge devices store and manipulate information in the charge states of the device. Flux devices store and manipulate information in a variable related to the magnetic flux through some part of the device. Phase devices store and manipulate information in a variable related to the difference in superconducting phase between two regions of the device. Recently, hybrid devices using two or more of charge, flux and phase degrees of freedom have been developed. Superconducting qubits commonly include at least one Josephson junction. A Josephson junction is a small interruption in an otherwise continuous superconducting current path and is typically realized by a thin insulating barrier sandwiched between two superconducting electrodes. Thus, a Josephson junction is usually formed as a three-layer or "trilayer" structure. Superconducting qubits are further described in, for example, U.S. Pat. Nos. 7,876,248, 8,035,540, and 8,098,179.

Integrated Circuit Fabrication

Traditionally, the fabrication of superconducting integrated circuits has not been performed at state-of-the-art semiconductor fabrication facilities. This may be due to the fact that some of the materials used in superconducting integrated circuits can contaminate the semiconductor facilities. For instance, gold may be used as a resistor in superconducting circuits, but gold can contaminate a fabrication tool used to produce complementary metal-oxide-semiconductor (CMOS) wafers in a semiconductor facility.

Superconductor fabrication has typically been performed in research environments where standard industry practices could be optimized for superconducting circuit production. Superconducting integrated circuits are often fabricated with tools that are traditionally used to fabricate semiconductor chips or integrated circuits. Due to issues unique to superconducting circuits, not all semiconductor processes and techniques are necessarily transferrable to superconductor chip manufacture. Transforming semiconductor processes and techniques for use in superconductor chip and circuit fabrication often requires changes and fine adjustments. Such changes and adjustments typically are not obvious and may require a great deal of experimentation. The semiconductor industry faces problems and issues not necessarily related to the superconducting industry. Likewise, problems and issues that concern the superconducting industry are often of little or no concern in standard semiconductor fabrication.

Any impurities within superconducting chips may result in noise which can compromise or degrade the functionality of the individual devices, such as superconducting qubits, and of the superconducting chip as a whole. Since noise is a serious concern to the operation of quantum computers, measures should be taken to reduce noise wherever possible.

Etching

Etching removes layers of, for example, substrates, dielectric layers, oxide layers, electrically insulating layers and/or metal layers according to desired patterns delineated by photoresists or other masking techniques. Two exemplary etching techniques are wet chemical etching and dry chemical etching.

Wet chemical etching or "wet etching" is typically accomplished by submerging a wafer in a corrosive bath such as an acid bath. In general, etching solutions are housed in polypropylene, temperature-controlled baths.

Dry chemical etching or "dry etching" is commonly employed due to its ability to better control the etching process and reduce contamination levels. Dry etching effectively etches desired layers through the use of gases, either by chemical reaction such as using a chemically reactive gas or through physical bombardment, such as plasma etching, using, for example, argon atoms.

Plasma etching systems have been developed that can effectively etch, for example, silicon, silicon dioxide, silicon nitride, aluminum, tantalum, tantalum compounds, chromium, tungsten, gold, and many other materials. Two types of plasma etching reactor systems are in common use—the barrel reactor system and the parallel plate reactor system. Both reactor types operate on the same principles and vary primarily in configuration. The typical reactor consists of a vacuum reactor chamber made usually of aluminum, glass, or quartz. A radiofrequency or microwave energy source (referred to collectively as RF energy source) is used to activate etchants, for example, fluorine-based or chlorine-based gases. Wafers are loaded into the chamber, a pump evacuates the chamber, and the reagent gas is introduced. The RF energy ionizes the gas and forms the etching plasma, which reacts with the wafers to form volatile products which are pumped away.

Physical etching processes employ physical bombardment. For instance, argon gas atoms may be used to physically bombard a layer to be etched, and a vacuum pump system removes dislocated material. Sputter etching is one physical technique involving ion impact and energy transfer. The wafer to be etched is attached to a negative electrode, or "target," in a glow-discharge circuit. Positive argon ions bombard the wafer surface, resulting in the dislocation of the

surface atoms. Ion beam etching and milling are physical etching processes which use a beam of low-energy ions to dislodge material. The ion beam is extracted from an ionized gas (e.g., argon or argon/oxygen) or plasma, created by an electrical discharge.

Reactive-ion etching (RIE) is a combination of chemical and physical etching. During RIE, a wafer is placed in a chamber with an atmosphere of chemically reactive gas (e.g., CF_4, CCl_4 and many other gases) at a low pressure. An electrical discharge creates an ion plasma with an energy of a few hundred electron volts. The ions strike the wafer surface vertically, where they react to form volatile species that are removed by the low pressure in-line vacuum system.

Planarization

The use of chemical-mechanical planarization (CMP) allows for a near flat surface to be produced. CMP is a standard process in the semiconductor industry. The CMP process uses an abrasive and corrosive chemical slurry in conjunction with a polishing pad and retaining ring that are pressed together by a dynamic polishing head. The dynamic polishing head is rotated with different axes of rotation (i.e., not concentric). This removes material and tends to even out any irregular topography, making the wafer flat or planar. The chemicals in the slurry also react with and/or weaken the material to be removed such that certain materials can be preferentially removed while leaving others relatively intact. The abrasive accelerates this weakening process and the polishing pad helps to wipe the reacted materials from the surface. Advanced slurries can be used to preferentially remove areas of the wafer which are relatively high or protrude in relation to areas of the wafer which are relatively low in order to planarize the topography of the wafer.

Hamiltonian Description of a Quantum Processor

In accordance with some embodiments of the present systems and devices, a quantum processor may be designed to perform adiabatic quantum computation and/or quantum annealing. A common problem Hamiltonian includes first component proportional to diagonal single qubit terms and a second component proportional to diagonal multi-qubit terms. The problem Hamiltonian, for example, may be of the form:

$$H_P \propto -\frac{\varepsilon}{2}\left[\sum_{i=1}^{N} h_i \sigma_i^z + \sum_{j>i}^{N} J_{ij} \sigma_i^z \sigma_j^z\right] \quad (1)$$

where N represents the number of qubits, σ_i^z is the Pauli z-matrix for the i^{th} qubit, h_i and $J_{i,j}$ are dimensionless local fields for the qubits, and couplings between qubits, and ε is some characteristic energy scale for H_P. Here, the σ_i^z and $\sigma_i^z\sigma_j^z$ terms are examples of "diagonal" terms. The former is a single qubit term and the latter a two qubit term. Hamiltonians may be physically realized in a variety of different ways, for example, by an implementation of superconducting qubits.

Noise in a Quantum Processor

Low-noise is a desirable characteristic of quantum devices. Noise can compromise or degrade the functionality of the individual devices, such as superconducting qubits, and of the superconducting processor as a whole. Noise can negatively affect qubit coherence and reduce the efficacy of qubit tunneling. Since noise is a serious concern to the operation of quantum processors, measures should be taken to reduce noise wherever possible so that a transition from coherent to incoherent tunneling is not induced by the environment.

Impurities may be deposited on the metal surface and/or may arise from an interaction with the etch/photoresist chemistry and the metal. Noise can be caused by impurities on the upper surface of the quantum processor. In some cases, superconducting devices that are susceptible to noise are fabricated in the top wiring layers of a superconducting integrated circuit and are thus sensitive to post-fabrication handling. There is a risk of introducing impurities that cause noise during post-fabrication handling. One approach to reducing noise is using a barrier passivation layer, for example, an insulating layer, to overlie the topmost wiring layer. The use of a barrier passivation layer to minimize noise from impurities on the upper surface of a quantum processor is described in U.S. Pat. No. 10,454,015.

Noise can also result from an external environment or surrounding circuitry in a superconducting processor. In a quantum processor, flux noise on qubits interferes with properly annealing the quantum processor because of the steep transition between qubit states as the flux bias is swept. Flux noise can be a result of current flowing through wiring of other devices included in the superconducting processor and can have a particularly negative effect on qubits at their respective degeneracy points. For example, flux noise can introduce errors in calculations carried out by the superconducting processor due to inaccuracies in setting flux bias and coupling strength values. Such values are important to using an integrated circuit as part of a quantum processor. Much of the static control error can be designed out of the processor with careful layout and high-precision flux sources, as well as by adding circuitry, such as an on-chip shield, to tune away any non-ideal flux qubit behavior. However, in many cases, limitations in integrated circuit fabrication capabilities can make it difficult to address noise by changing processor layout and adding circuitry. There is thus a general desire for systems and methods to for fabricating integrated circuits that have reduced flux noise without having to compromise the quantum processor layout by adding additional layers or circuitry.

The foregoing examples of the related art and limitations related thereto are intended to be illustrative and not exclusive. Other limitations of the related art will become apparent to those of skill in the art upon a reading of the specification and a study of the drawings.

BRIEF SUMMARY

There exists a need for scalable systems and methods for fabricating integrated circuits that have reduced flux noise. Past approaches necessitate additional layers, such as overlying passivation layers, or additional circuitry such as on chip shields. The present systems and methods describe fabrication of a superconducting integrated circuit including fabrication of a superconducting integrated circuit with low-noise layers.

A method for fabricating a superconducting integrated circuit may be summarized as including: depositing a first wiring layer comprising a first material that is superconductive in a first range of temperatures, the first range of temperatures including a respective critical temperature; patterning the first wiring layer to form a first set of one or more superconducting traces; depositing a first dielectric layer; polishing the first dielectric layer back to an upper surface of the first wiring layer; depositing a passivation layer to overlie at least a portion of the first wiring layer, the passivation layer comprising a second material that is superconductive in a second range of temperatures, the second range of temperatures including a respective critical tem-

perature; patterning the passivation layer; depositing a second dielectric layer to overlie at least a portion of the passivation metal layer; patterning the second dielectric layer to expose at least a portion of the passivation layer; depositing a second wiring to overlie at least a portion of the passivation layer, the second wiring layer comprising the second material that is superconductive in the second range of temperatures; forming a first set of vias electrically coupling the second wiring layer to the passivation layer, the first set of vias comprising the second material that is superconductive in the second range of temperatures; and patterning the second wiring layer to form a second set of one or more superconducting traces. a first wiring layer including a first set of one or more superconducting traces, the first wiring layer comprising a first material that is superconductive in a first range of temperatures; a passivation layer overlying the first wiring layer, the passivation layer comprising a second material that is superconductive in a second range of temperatures; a second wiring layer including a second set of one or more superconducting traces, the second wiring layer comprising the second material that is superconductive in the second range of temperatures; a first set of vias electrically coupling the passivation layer to the second wiring layer, the first set of vias comprising the second material that is superconductive in the second range of temperatures; a third wiring layer including a third set of one or more superconducting traces, the third wiring layer comprising the second material that is superconductive in the second range of temperatures; and a second set of vias electrically coupling the second wiring layer to the third wiring layer, the second set of vias comprising the second material that is superconductive in the second range of temperatures.

Depositing the first wiring layer may include depositing the first wiring layer comprising the first material that is superconductive at a respective critical temperature that is different from a respective critical temperature of the second range of temperatures. a first wiring layer including a first set of one or more superconducting traces, the first wiring layer comprising a first material that is superconductive in a first range of temperatures; a passivation layer overlying the first wiring layer, the passivation layer comprising a second material that is superconductive in a second range of temperatures; a second wiring layer including a second set of one or more superconducting traces, the second wiring layer comprising the second material that is superconductive in the second range of temperatures; a first set of vias electrically coupling the passivation layer to the second wiring layer, the first set of vias comprising the second material that is superconductive in the second range of temperatures; a third wiring layer including a third set of one or more superconducting traces, the third wiring layer comprising the second material that is superconductive in the second range of temperatures; and a second set of vias electrically coupling the second wiring layer to the third wiring layer, the second set of vias comprising the second material that is superconductive in the second range of temperatures.

The method may further include polishing the second dielectric layer back to an upper surface of the passivation metal layer and re-depositing the second dielectric layer, after depositing the second dielectric layer to overlie at least a portion of the passivation metal layer. The method may further include depositing a third dielectric layer to overlie at least a portion of the second wiring layer. The method may further polishing the third dielectric layer back to the upper surface of the second wiring layer and re-depositing the third dielectric layer.

The method may further include patterning the third dielectric layer to expose at least a portion of the second wiring layer. The method may further include depositing a third wiring layer to overlie the third dielectric layer, the third wiring layer comprising the second material that is superconductive in the second range of temperatures. The method may further include patterning the third wiring layer to form a third set of one or more superconducting traces. The method may further include forming a second set of vias electrically coupling the third wiring layer to the second wiring layer, the second set of vias comprising the second material that is superconductive in the second range of temperatures.

Depositing a first wiring layer may include depositing the first wiring layer to overlie an additional wiring layer, the additional wiring layer comprising the first material that is superconductive in the first range of temperatures. Patterning the first wiring layer to form a first set of one or more superconducting traces may include patterning the first wiring layer to form at least one of: a magnetometer, a transformer, at least a portion of an on-chip shield. Patterning the second wiring layer to form a second set of one or more superconducting traces may include patterning the second wiring layer to form at least one of: a qubit and a coupler.

A superconducting integrated circuit may be summarized as including: a first wiring layer including a first set of one or more superconducting traces, the first wiring layer comprising a first material that is superconductive in a first range of temperatures; a passivation layer overlying the first wiring layer, the passivation layer comprising a second material that is superconductive in a second range of temperatures; a second wiring layer including a second set of one or more superconducting traces, the second wiring layer comprising the second material that is superconductive in the second range of temperatures; a first set of vias electrically coupling the passivation layer to the second wiring layer, the first set of vias comprising the second material that is superconductive in the second range of temperatures; a third wiring layer including a third set of one or more superconducting traces, the third wiring layer comprising the second material that is superconductive in the second range of temperatures; and a second set of vias electrically coupling the second wiring layer to the third wiring layer, the second set of vias comprising the second material that is superconductive in the second range of temperatures.

The first range of temperatures and the second range of temperatures may each include a respective critical temperature, and the critical temperature of the first range of temperatures is higher than the critical temperature of the second range of temperatures. The first material may be or may include niobium. The second material may be or may include aluminum.

The superconducting integrated circuit may include a substrate and a trilayer Josephson junction, the substrate carrying: the trilayer Josephson junction, the first wiring layer, the passivation layer, the second wiring layer, the first set of vias, the third wiring layer, and the second set of vias.

The superconducting integrated circuit may further includes a fourth wiring layer and a third set of vias each overlying the trilayer Josephson junction, the third set of vias electrically coupling the trilayer Josephson junction to the fourth wiring layer. The superconducting integrated circuit may further include a fifth wiring layer and a fourth set of vias each overlying the fourth wiring layer, the fourth set of vias electrically coupling the fourth wiring layer to the fifth wiring layer.

The superconducting integrated circuit may further include a first dielectric layer interposed between the passivation layer and the second wiring layer, the first dielectric layer comprising silicon dioxide. The superconducting integrated circuit may even further include a second dielectric layer interposed between the second wiring layer and the third wiring layer, the second dielectric layer comprising silicon dioxide. The first wiring layer may be thicker than the passivation layer.

The first set of one or more superconducting traces may advantageously form at least a portion of an on-chip shield. The first set of one or more superconducting traces may form at least a portion of a magnetometer. The second set of one or more superconducting traces may form at least a portion of a noise-susceptible device. The second set of one or more superconducting traces may form at least one qubit. The second set of one or more superconducting traces may form at least one coupler. The second set of one or more superconducting traces may form at least a portion of a noise-susceptible device. The third set of one or more superconducting traces may form at least one qubit. The third set of one or more superconducting traces may form at least one coupler.

A method for fabricating a superconducting integrated circuit may be summarized as including: depositing a base electrode layer, the base electrode layer comprising a deposited top surface having a first roughness; planarizing the base electrode layer, the base electrode layer subsequently comprising a planarized top surface having a second surface roughness, the second surface roughness being less than the first surface roughness; depositing an insulating layer to overly at least a portion of the planarized top surface of the base electrode layer; and depositing a counter electrode layer to overly at least a portion of the insulating layer.

Planarizing the base electrode layer may comprise a chemical-mechanical planarization process, and planarizing the base electrode layer may comprise planarizing the base electrode layer such that the planarized top surface of the base electrode layer is atomically smooth.

The method may further include patterning the base electrode layer and depositing a first dielectric layer prior to planarizing the base electrode layer, and planarizing the base electrode layer may further comprise planarizing the dielectric layer. The method may further include planarizing the counter electrode layer.

Depositing a base electrode layer may comprise depositing niobium, depositing a counter electrode layer may comprise depositing niobium, and depositing an insulating layer may comprise depositing a layer of aluminum and oxidizing the layer of aluminum to form aluminum oxide.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

In the drawings, identical reference numbers identify similar elements or acts. The sizes and relative positions of elements in the drawings are not necessarily drawn to scale. For example, the shapes of various elements and angles are not necessarily drawn to scale, and some of these elements may be arbitrarily enlarged and positioned to improve drawing legibility. Further, the particular shapes of the elements as drawn, are not necessarily intended to convey any information regarding the actual shape of the particular elements, and may have been solely selected for ease of recognition in the drawings.

FIGS. **1**A to **1**H are each a respective sectional view of a portion of a superconducting integrated circuit fabricated at successive stages of fabrication, in accordance with the present methods and systems.

FIG. **2** is a sectional view of a portion of a superconducting integrated circuit comprising a trilayer Josephson junction and low-noise wiring layers, in accordance with the present systems and methods.

FIG. **3** is a flowchart illustrating a method for fabricating a portion of a superconducting integrated circuit comprising low-noise wiring layers, in accordance with the present systems and methods.

FIG. **4** is a schematic diagram illustrating a computing system comprising a digital computer and an analog computer that includes a superconducting integrated circuit, in accordance with the present systems and methods.

FIGS. **5**A to **5**D are each a respective sectional view of a portion of a superconducting integrated circuit fabricated at successive stages of fabrication, in accordance with the present methods and systems.

FIGS. **6**A to **6**I are each a respective sectional view of a portion of a superconducting integrated circuit fabricated at successive stages of fabrication, in accordance with the present methods and systems.

FIG. **7** is a flow chart illustrating a method for fabricating a portion of a superconducting integrated circuit comprising a planarized base electrode, in accordance with the present systems and methods.

FIG. **8** is a flow chart illustrating another implementation of a method for fabricating a portion of a superconducting integrated circuit comprising a planarized base electrode, in accordance with the present system and methods.

DETAILED DESCRIPTION

In the following description, certain specific details are set forth in order to provide a thorough understanding of various disclosed implementations. However, one skilled in the relevant art will recognize that implementations may be practiced without one or more of these specific details, or with other methods, components, materials, etc. In other instances, well-known structures associated with computer systems, server computers, and/or communications networks have not been shown or described in detail to avoid unnecessarily obscuring descriptions of the implementations.

Unless the context requires otherwise, throughout the specification and claims that follow, the word "comprising" is synonymous with "including," and is inclusive or open-ended (i.e., does not exclude additional, unrecited elements or method acts).

Reference throughout this specification to "one implementation" or "an implementation" means that a particular feature, structure or characteristic described in connection with the implementation is included in at least one implementation. Thus, the appearances of the phrases "in one implementation" or "in an implementation" in various places throughout this specification are not necessarily all referring to the same implementation. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more implementations.

As used in this specification and the appended claims, the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise. It should also be noted that the term "or" is generally employed in its sense including "and/or" unless the context clearly dictates otherwise.

The headings and Abstract of the Disclosure provided herein are for convenience only and do not interpret the scope or meaning of the implementations.

A quantum processor may require a local bias to be applied on a qubit to implement a problem Hamiltonian. The local bias applied on the qubit can depend on persistent current I_P and external flux bias ϕ_q as described below:

$$\delta h_i = 2|I_P|\delta\phi_q$$

Noise can affect the local bias δh_i in the same way as the external flux bias ϕ_q and thus change the specification of the qubit terms in the problem Hamiltonian. By altering the problem Hamiltonian, noise can introduce errors into the computational result from quantum annealing.

Throughout the present specification, the phrase "noise-susceptible superconducting device" is used to describe a superconducting device for which proper performance is essential to properly annealing a quantum processor. Poor performance of a noise-susceptible device may result in the quantum processor producing inaccurate or suboptimal solutions to a problem. For example, a qubit may be considered a noise-susceptible device or device that is susceptible to noise because noise on the qubits can interfere with properly annealing the quantum processor and/or can lead to a different problem being solved. In comparison, a magnetometer in the quantum processor has a primary purpose of measuring external magnetic fields to support minimizing trapped flux. Noise on a magnetometer may not interfere with properly annealing the quantum processor, and thus, in the present specification, a magnetometer is an example of a device may be described as less susceptible or not susceptible to noise. Note that the phrase "noise-susceptible" or "susceptible to noise" does not necessarily suggest that the device itself is physically more or less sensitive to noise compared to other devices that are not described as noise-susceptible. Sensitivities to processor performance is higher in noise-susceptible devices relative to devices that are described as less susceptible to noise.

Noise in a quantum processor can cause qubits to decohere which reduces the efficacy of tunneling. As a result, processor performance can be diminished, and solutions generated from the processor can be suboptimal. Existing approaches for reducing noise involve modifying processor layouts or adding circuitry to shield qubits which, in some cases, can be impractical. The present systems and methods describe a design in which noise can be reduced in a quantum processor without necessitating significant modifications to the processor layout.

Performance of a superconducting processor can be easily affected by certain superconducting devices that are considered analog circuits, for example, qubits and couplers. Analog circuits can be very susceptible to noise. Since processor performance is particularly sensitive to proper or improper operation of these devices, it is desirable to reduce noise in these devices as much as possible. For a superconducting processor, one of the dominant sources of environmental noise is flux noise. Flux noise can cause decoherence which induces a transition from coherent to incoherent tunneling before the transition is induced by intrinsic phase transitions, which is undesirable as it limits the speed and/or accuracy with which the processor can evolve and produce solutions. Additionally, flux noise can increase spin bath susceptibility which is a "memory" effect that results in diminished sampling and optimization performance. Systems and methods to reduce spin bath polarization are described in U.S. patent application Ser. No. 16/029,026.

One approach to reducing the effect of flux noise is to use a low-noise material for layers of an integrated circuit that include superconducting devices for which reducing noise is particularly important. This can include using a low-noise material for wiring layers that form analog circuitry that contain, for example, qubits and couplers. The low-noise material can be superconducting in a respective range of temperatures. A different superconducting material can be used for layers of an integrated circuit that include superconducting devices for which noise reduction is desired but not required. Such layers can include, for example, part or all of an on-chip shield, a magnetometer, or a transformer. Thus, it can be beneficial for a superconducting integrated circuit to have noise-susceptible superconducting devices that comprise a low-noise material and other superconducting devices that comprise a different superconducting material.

The low-noise material and the different superconducting material can each transition into superconductivity at a respective critical temperature. Critical temperature is an intrinsic property of a superconducting material and is the temperature at which the electrical resistance of the superconducting material drops to zero (i.e., temperature at which it becomes superconductive). At and below the critical temperature, two electrons in a wire comprising the superconducting material will form a Cooper pair and current can persist without additional energy. For example, the critical temperature of niobium is approximately 9.2 Kelvin. At and below a temperature of 9.2 Kelvin, a niobium wire can have zero electrical resistance. Superconductivity can be indicative of a quantum mechanical state and can therefore be useful in fabricating a superconducting integrated circuit such as a quantum processor.

In some cases, it can be advantageous for an on-chip shield of a superconducting integrated circuit to comprise a superconducting material having a different critical temperature than that of a low noise material. Generally, a proximity effect can exist when a superconductor is in contact with a normal conductor, resulting in weak superconductivity in the normal conductor due to Cooper pairs being carried over to the normal conductor for a certain distance. However, a similar proximity effect can exist when a first superconducting material is in contact with a second superconducting material and the respective critical temperatures of each superconducting material are different. In such cases, a gradient of critical temperatures can exist at and near the interface of the first superconducting material and the second superconducting material. The gradient of critical temperatures caused by the proximity effect can be exploited in shielding analog circuitry that comprises one of the superconducting materials. For example, a superconducting integrated circuit can include analog circuitry formed in a wiring layer comprising aluminum and can further include a shield formed in a wiring layer comprising niobium. At an interface of the wiring layer forming analog circuitry and a wiring layer forming the shield, a gradient of critical temperatures can exist. The gradient of critical temperatures can range from a critical temperature of aluminum to a critical temperature of niobium. The gradient of critical temperatures can be beneficial in shielding analog circuitry in the wiring layer comprising aluminum because the shield in the wiring layer comprising niobium transitions into being superconductive at a higher temperature. Thus, the wiring layer comprising niobium captures some spin defects that would otherwise exist in the wiring layer comprising aluminum.

For a superconducting integrated circuit that includes wiring layers comprising more than one material, it is

important that the materials integrate together so that the functionality of the superconducting integrated circuit and thus processor performance, is not compromised. For instance, forming good contacts in vias between a wiring layer comprising a superconducting material having a first critical temperature and another wiring layer comprising a low-noise material (e.g., a superconducting material having a second critical temperature) can be a challenge. Many existing fabrication processes are designed to use only one material for wiring layers in an integrated circuit. Thus, including a second material, such as a low-noise material, for wiring layers that include noise-susceptible devices or analog circuitry requires careful adjustments to process conditions. It is desirable for deposition and patterning of layers comprising a low-noise material to have no negative effects on layers comprising other materials. For example, it is desirable to deposit and pattern a layer comprising a low-noise material without corroding layers comprising other materials or forming a resistive layer.

FIGS. **1**A to **1**H show a sectional view of a portion of a superconducting integrated circuit fabricated at successive stages of fabrication, according to method **300** of FIG. **3**.

FIG. **1**A is a sectional view of a portion of a superconducting integrated circuit **100***a* at a first stage of a fabrication process described by method **300** of FIG. **3**. Integrated circuit **100***a* includes a substrate **102** and a first wiring layer **104** comprising a first material that is superconductive in a first range of temperatures. In some implementations, substrate **102** comprises at least one of: silicon and sapphire. In some implementations, first wiring layer **104** comprises niobium.

FIG. **1**B is a sectional view of a portion of a superconducting integrated circuit **100***b* at a subsequent stage of the fabrication process. Superconducting integrated circuit **100***b* can be formed from integrated circuit **100***a* of FIG. **1**A by patterning first wiring layer **104**, depositing a first dielectric layer **106**, and polishing first dielectric layer **106** back to the upper surface of first wiring layer **104**. Patterning first wiring layer **104** can include masking and then etching first wiring layer **104**. The first wiring layer can include a respective set of one or more superconducting traces. The set of one or more superconducting traces can form a superconducting device that is not susceptible to flux noise relative to a superconducting device that is included in other wiring layers. In one implementation, patterning first wiring layer **104** forms at least one of: a magnetometer, a transformer, and at least a portion of an on-chip shield. In one implementation, the first wiring layer **104** comprises niobium. In one implementation, first dielectric layer **106** comprises silicon dioxide.

FIG. **1**C is a sectional view of a portion of a superconducting integrated circuit **100***c* at a subsequent stage of the fabrication process. Superconducting integrated circuit **100***c* can be formed from integrated circuit **100***b* of FIG. **1**B by depositing a passivation layer **108** comprising a second material that is superconductive in a second range of temperatures. Passivation layer **108** is deposited to overlie first wiring layer **104**. The first range of temperatures and the second range of temperatures each include a respective critical temperature. In one implementation, the critical temperature of the first range of temperatures is higher than the critical temperature of the second range of temperatures. In one implementation, at least some of the temperatures in the first range of temperatures are the same as the temperatures in the second range of temperatures. First wiring layer **104** can be thicker than passivation layer **108**. In one implementation, passivation layer **108** comprises aluminum.

FIG. **1**D is a sectional view of a portion of a superconducting integrated circuit **100***d* at a subsequent stage of the fabrication process. Superconducting integrated circuit **100***d* can be formed from integrated circuit **100***c* of FIG. **1**C by patterning passivation layer **108**, depositing a second dielectric layer **110**, and then patterning second dielectric layer **110**. Patterning passivation layer **108** can include masking passivation layer **108** with the same mask that was used to pattern first wiring layer **104** to form integrated circuit **100***b* in FIG. **1**B, and then etching passivation layer **108**. Passivation layer **108** can provide a surface for vias comprising the second material to adhere to. In one implementation, passivation layer **108** can protect the upper surface of first wiring layer **104**. Depositing second dielectric layer **110** can include polishing second dielectric layer **110** using CMP. Patterning second dielectric layer **110** can include masking and etching second dielectric layer **110** to expose at least a portion of passivation layer **108**. In one implementation, second dielectric layer can comprise silicon dioxide. Optionally, after depositing second dielectric layer **110** and before patterning second dielectric layer **110**, second dielectric layer **110** can be polished back to an upper surface of passivation layer **108** and re-deposited (not illustrated in FIG. **1**D). Re-depositing second dielectric layer **110** can include depositing a respective extended dielectric layer comprising the same material as second dielectric layer **110**.

FIG. **1**E is a sectional view of a portion of a superconducting integrated circuit **100***e* at a subsequent stage of the fabrication process. Superconducting integrated circuit **100***e* can be formed from integrated circuit **100***d* of FIG. **1**D by depositing a second wiring layer **112** to form a first set of vias, and then patterning second wiring layer **112**. Second wiring layer **112** comprises the second material that is superconductive in the second range of temperatures. The first set of vias electrically couples the second wiring layer **112** to passivation layer **108**. Patterning second wiring layer **112** can include masking and etching second wiring layer **112**. Second wiring layer **112** can include a respective set of one or more superconducting traces. The set of one or more superconducting traces can form a noise-susceptible superconducting device that is included in first wiring layer **104**. In one implementation, patterning second wiring layer **112** forms at least one of: a qubit and a coupler. In one implementation, third superconducting layer **112** comprises aluminum. Second wiring layer **112** can sometimes be referred to as a "low-noise wiring layer". In one implementation, passivation layer **108** is etched via sputter etching prior to depositing second wiring layer **112**. In such cases, the first set of vias can electrically couple second wiring layer **112** and first wiring layer **104**.

FIG. **1**F is a sectional view of a portion of a superconducting integrated circuit **100***f* at a subsequent stage of the fabrication process. Superconducting integrated circuit **100***f* can be formed from integrated circuit **100***e* of FIG. **1**E by depositing a third dielectric layer **114**, polishing third dielectric layer **114**, and patterning third dielectric layer **114**. Optionally, after polishing third dielectric layer **114** and before patterning third dielectric layer **114**, third dielectric layer **114** can be polished back to an upper surface of second wiring layer **112** and re-deposited (not illustrated in FIG. **1**F). Re-depositing third dielectric layer **114** can include depositing a respective extended dielectric layer comprising the same material as third dielectric layer **114**. Patterning third dielectric layer **114** can include masking and etching third dielectric layer **114** to expose at least a portion of second wiring layer **112**. In one implementation, third dielectric layer comprises silicon dioxide.

FIG. **1**G is a sectional view of a portion of a superconducting integrated circuit **100***g* at a subsequent stage of the fabrication process. Superconducting integrated circuit **100***g* can be formed from integrated circuit **100***f* of FIG. **1**F by depositing a third wiring layer **116** to form a second set of vias, and then patterning third wiring layer **116**. Third wiring layer **116** comprises the second material that is superconductive in the second range of temperatures. The second set of vias electrically couples the third wiring layer **116** to second wiring layer **112**. Patterning third wiring layer **116** can include masking and etching third wiring layer **116**. The third wiring layer can include a respective set of one or more superconducting traces. The set of one or more superconducting traces can form a noise-susceptible superconducting device. In one implementation, patterning third wiring layer **116** forms at least one of: a qubit and a coupler. In one implementation, third wiring layer comprises aluminum. Third wiring layer **116** can sometimes be referred to as a "low-noise wiring layer".

FIG. **1**H is a sectional view of a portion of a superconducting integrated circuit **100***h* at a subsequent stage of the fabrication process. Superconducting integrated circuit **100***h* can be formed from integrated circuit **100***g* of FIG. **1**G by depositing a fourth dielectric layer **118**, polishing fourth dielectric layer **118**, and patterning fourth dielectric layer **114**. Optionally, after polishing fourth dielectric layer **118** and before patterning fourth dielectric layer **118**, fourth dielectric layer **114** can be polished back to an upper surface of third wiring layer **116** and then re-deposited (not illustrated in FIG. **1**H). Re-depositing fourth dielectric layer **114** can include depositing a respective extended dielectric layer comprising the same material as fourth dielectric layer **114**. Patterning fourth dielectric layer **114** can include masking and etching fourth dielectric layer **118** to expose at least a portion of third wiring layer **116**. An exposed portion of third wiring layer **116** can be used as a bond pad to electrically couple integrated circuit **100***h* to input/output electronics via a printed circuit board or another device. In one implementation, fourth dielectric layer comprises silicon dioxide. In one approach, fourth dielectric layer is a passivation layer that protects the upper surface of third wiring layer **116**.

FIGS. **1**A to **1**H illustrate an integrated circuit wherein devices that are susceptible to noise, for example, qubits and couplers, are in the upper portion of the integrated circuit and devices that are relatively less susceptible to noise are in the lower portion of the integrated circuit. However, in some implementations, it can be advantageous to have noise-susceptible devices in the middle portion (i.e., interposed between the uppermost wiring layer and the bottommost wiring layer) or in the lower portion (i.e., closer to the substrate) of the integrated circuit. In some implementations, there can be more or less than two wiring layers that include noise-susceptible devices. In some implementation, wiring layers that include noise-susceptible devices can be at least partially in the bottommost wiring layer of the integrated circuit. In such cases, a passivation layer may overlie a set of one or more vias that electrically couple a wiring layer that includes noise-susceptible devices and a wiring layer that includes devices that are less susceptible to noise, and the passivation layer may comprise at least some of a material in the wiring layer that includes noise-susceptible devices.

FIG. **2** shows a sectional view of a portion of a superconducting integrated circuit fabricated **200** according to method **300** of FIG. **3**. Integrated circuit **200** is an implementation of integrated circuit **100***h* of FIG. **1**H that further comprises a set of additional wiring layers and a trilayer Josephson junction.

Integrated circuit **200** includes a substrate **202** carrying a trilayer Josephson junction **204**. Trilayer Josephson junction **204** can include two electrodes comprising aluminum that sandwich a thin oxide layer. A first dielectric layer **206** overlies at least a portion of trilayer Josephson junction **204**. First dielectric layer **206** is patterned to expose at least a portion of trilayer Josephson junction **220**.

A first superconducting metal layer is deposited to overlie at least a portion of trilayer Josephson junction **220** and forms a first set of vias **208**. The first superconducting metal layer also overlies at least a portion of first dielectric layer **206**. The first superconducting metal layer can be patterned to form a first wiring layer **210** that includes a respective set of one or more superconducting traces. First set of vias **208** electrically couple trilayer Josephson junction **204** to first wiring layer **210**.

A second dielectric layer **212** overlies at least a portion of first wiring layer **210**. Second dielectric layer **212** is patterned to expose at least a portion of first wiring layer **210**. In one implementation, second dielectric layer **212** can comprise silicon dioxide.

A second superconducting metal layer is deposited to overlie at least a portion of first wiring layer **210** and forms a second set of vias **214**. The second superconducting metal layer also overlies at least a portion of second dielectric layer **212**. The second superconducting metal layer can be patterned to form a second wiring layer **216** that includes a respective set of one or more superconducting traces. Second set of vias **214** electrically couple first wiring layer **210** to second wiring layer **216**.

A third dielectric layer **218** overlies at least a portion of second wiring layer **216**. Third dielectric layer **216** is patterned to expose at least a portion of second wiring layer **216**.

A third superconducting metal layer is deposited to overlie at least a portion of second wiring layer **216** and forms a third set of vias **220**. The third superconducting metal layer also overlies at least a portion of third dielectric layer **218**. The third superconducting metal layer can be patterned to form a third wiring layer **222** that includes a respective set of one or more superconducting traces. Third set of vias **220** electrically couple third wiring layer **222** to second wiring layer **216**.

First wiring layer **210**, second wiring layer **216**, and third wiring layer **222** each include a respective set of one or more superconducting traces. Each set of one or more superconducting traces can form a superconducting device that is not susceptible to noise relative to a superconducting device in another layer of integrated circuit **200**. For example, first wiring layer **210**, second wiring layer **216**, and third wiring layer **222** can each include at least one of: a shield, a magnetometer, and a transformer. First wiring layer **210**, second wiring layer **216**, and third wiring layer **222** each comprise a first material that is superconductive in a first range of temperatures. In one implementation, first wiring layer **210**, second wiring layer **216**, and third wiring layer **222** each comprise niobium. In one implementation, first dielectric layer **206**, second dielectric layer **212**, and third dielectric layer **218** each comprise silicon dioxide.

A fourth superconducting metal layer is deposited to overlie at least a portion of third wiring layer **222**. The fourth superconducting metal layer can be patterned using a mask that has the same geometric pattern as another mask that was used to pattern the third superconducting metal layer to form

third wiring layer **222**. The fourth superconducting metal layer can be patterned to form a passivation layer **224**. Passivation layer **224** can comprise a second material that is superconductive in a second range of temperatures. Passivation layer **224** overlies at least a portion of third wiring layer **222** and is electrically coupled to third wiring layer **222**. Passivation layer **224** can provide a surface that is more suitable for a set of vias comprising the second material to adhere to relative to wiring layer **222**. In one implementation, third wiring layer **222** is thicker than passivation layer **224**. In one implementation, passivation layer **224** comprises aluminum.

A fourth dielectric layer **226** overlies at least a portion of passivation layer **224**. Fourth dielectric layer **226** is patterned to expose at least a portion of passivation layer **224**.

A fifth superconducting metal layer is deposited to overlie at least a portion of passivation layer **224** and forms a fourth set of vias **228**. The fifth superconducting metal layer also overlies at least a portion of fourth dielectric layer **226**. The fifth superconducting metal layer can be patterned to form a fourth wiring layer **230** that includes a respective set of one or more superconducting traces. Fourth set of vias **228** electrically couple fourth wiring layer **230** to passivation layer **224**.

A fifth dielectric layer **232** overlies at least a portion of fourth wiring layer **230**. Fifth dielectric layer **226** is patterned to expose at least a portion of fourth wiring layer **230**.

A sixth superconducting metal layer is deposited to overlie at least a portion of fourth wiring layer **230** and forms a fifth set of vias **234**. The sixth superconducting metal layer also overlies at least a portion of fifth dielectric layer **226**. The sixth superconducting metal layer can be patterned to form a fifth wiring layer **236** that includes a respective set of one or more superconducting traces. Fifth set of vias **234** electrically couple fourth wiring layer **230** to fifth wiring layer **236**.

Fourth wiring layer **230** and fifth wiring layer **236** each include a respective set of one or more superconducting traces. Each set of one or more superconducting traces can form a superconducting device that is noise-susceptible relative to a superconducting device included in at least one of: first wiring layer **210**, second wiring layer **216**, and third wiring layer **222**. For example, fourth wiring layer **230** and fifth wiring layer **236** can each include at least one of: a qubit and a coupler. Fourth wiring layer **230** and fifth wiring layer **236** can sometimes be referred to as "low-noise wiring layers". Passivation layer **224**, fourth wiring layer **230**, and fifth wiring layer **236** each comprise the second material that is superconductive in the second range of temperatures. In one implementation, passivation layer **224**, fourth wiring layer **230**, and fifth wiring layer **236** each comprise aluminum. In one implementation, fourth dielectric layer **226** and fifth dielectric layer **232** comprise silicon dioxide. In one implementation, fourth dielectric layer **226** and fifth dielectric layer **232** comprise an electrically insulative material that is different from first dielectric layer **206**, second dielectric layer **212**, and third dielectric layer **218**.

Elements of integrated circuit **200** comprise the first material that is superconductive in the first range of temperatures and the second material that is superconductive in the second range of temperatures. The first range of temperatures and the second range of temperatures can each include a respective critical temperature. In one implementation, the critical temperature of the first range of temperatures can be higher than the critical temperature of the second range of temperatures. For example, the first material can transition into being superconductive at 9 Kelvin and the second material can transition into being superconductive at 1.2 Kelvin. In one implementation, at least some of the temperatures in the first range of temperatures are the same as the temperatures in the second range of temperatures.

FIG. **3** is a flowchart illustrating a method **300** for fabricating a portion of a superconducting integrated circuit with low-noise, in accordance with the present systems and methods. Method **300** includes acts **302-330**, though in other implementations, certain acts can be omitted and/or additional acts can be added. Method **300** can be performed by, for example, integrated circuit fabrication equipment in response to an initiation of a fabrication process.

At **302**, a first wiring layer comprising a first material is deposited to overlie a substrate. The first material is superconductive in a first range of temperatures. In one implementation, the first wiring layer comprising the first material can be deposited to overlie a least a portion of an additional wiring layer. In some implementations, the first wiring layer comprises aluminum.

At **304**, the first wiring layer is patterned. Patterning the first wiring layer can form a respective set of one or more superconducting traces. The first wiring layer can include a superconducting device that is less susceptible to noise relative to another superconducting device in another wiring layer. In one implementation, patterning the first wiring layer can form at least a portion of an on-chip shield. In one implementation, patterning the first wiring layer can form at least a portion of a magnetometer or a transformer. Patterning the first wiring layer can include masking and etching the first wiring layer.

At **306**, a first dielectric layer is deposited to overlie at least a portion of the first wiring layer. The first dielectric layer can fill an opening in between one or more superconducting traces of the first wiring layer. The first dielectric layer is polished back to an upper surface of the first wiring layer. At least a portion of the first wiring layer can be exposed.

At **308**, a passivation layer comprising a second material is deposited to overlie at least a portion of the first wiring layer. The second material is superconductive in a second range of temperatures. The passivation layer can form a surface that is suitable for vias comprising the second material to adhere to. The first range of temperatures and the second range of temperatures each include a respective critical temperature. In one implementation, the critical temperature of the first range of temperatures is higher than the critical temperature of the second range of temperatures. In one implementation, at least some of the temperatures in the first range of temperatures are the same as the temperatures in the second range of temperatures.

At **310**, the passivation layer is patterned. Patterning the passivation layer can include masking and etching the passivation layer. The passivation layer can be patterned using a mask that has a geometric pattern that is the same as another mask used to pattern the first wiring layer in act **304**.

At **312**, a second dielectric layer is deposited to overlie at least a portion of the passivation layer. The second dielectric layer can overlie at least a portion of the first wiring layer. The second dielectric layer can fill an opening in between one or more superconducting traces of the second wiring layer.

Optionally, at **314**, the second dielectric layer is polished back to an upper surface of the passivation layer, redeposited, and then polished back to a respective thickness.

At **316**, the second dielectric layer is patterned. Patterning the second dielectric layer can expose at least a portion of

the passivation layer. Patterning the second dielectric layer can include masking and etching the second dielectric layer.

At **318**, a second wiring layer comprising the second material is deposited to overlie at least a portion of the passivation layer. The second wiring layer can overlie at least a portion of the second dielectric layer. The second material is superconductive in the second range of temperatures. Depositing the second wiring layer can form a first set of vias that electrically couple the passivation layer to the second wiring layer.

At **320**, the second wiring layer is patterned. Patterning the second wiring layer can form a respective set of one or more superconducting traces. The second wiring layer can include a superconducting device that is noise-susceptible. In one implementation, patterning the second wiring layer can form at least one of: a qubit and a coupler. Patterning the second wiring layer can include masking and etching the second wiring layer.

At **322**, a third dielectric layer is deposited to overlie at least a portion of the second wiring layer. The third dielectric layer can fill an opening in between one or more superconducting traces of the second wiring layer.

Optionally, at **324**, the third dielectric layer is polished back to an upper surface of the second wiring layer, redeposited, and then polished back to a respective thickness.

At **326**, the third dielectric layer is patterned. Patterning the third dielectric layer can expose at least a portion of the second wiring layer. Patterning the third dielectric layer can include masking and etching the third dielectric layer.

At **328**, a third wiring layer comprising the second material is deposited to overlie at least a portion of the second wiring layer. The third wiring layer can overlie at least a portion of the third dielectric layer. The second material is superconductive in the second range of temperatures. Depositing the third wiring layer can form a second set of vias that electrically couple the second wiring layer to the third wiring layer.

At **330**, the third wiring layer is patterned. Patterning the third wiring layer can form a respective set of one or more superconducting traces. The third wiring layer can include a superconducting device that is noise-susceptible. In one implementation, patterning the third wiring layer can form at least one of: a qubit and a coupler. Patterning the third wiring layer can include masking and etching the third wiring layer.

FIG. **4** illustrates a computing system **400** comprising a digital computer **402**. The example digital computer **402** includes one or more digital processors **406** that may be used to perform classical digital processing tasks. Digital computer **402** may further include at least one system memory **422**, and at least one system bus **420** that couples various system components, including system memory **422** to digital processor(s) **406**. System memory **422** may store a set of modules **424**.

The digital processor(s) **406** may be any logic processing unit or circuitry (e.g., integrated circuits), such as one or more central processing units ("CPUs"), graphics processing units ("GPUs"), digital signal processors ("DSPs"), application-specific integrated circuits ("ASICs"), programmable gate arrays ("FPGAs"), programmable logic controllers ("PLCs"), etc., and/or combinations of the same.

In some implementations, computing system **400** comprises an analog computer **404**, which may include one or more quantum processors **426**.

Quantum processor **426** can be at least one superconducting integrated circuit that includes noise-susceptible superconducting devices comprising a first material and regular superconducting devices comprising a second material. The first material and the second material can each be superconductive in a respective range of temperatures. Quantum processor **426** can include at least one integrated circuit that is fabricated using methods as described in greater detail herein. Digital computer **402** may communicate with analog computer **404** via, for instance, a controller **418**. Certain computations may be performed by analog computer **404** at the instruction of digital computer **402**, as described in greater detail herein.

Digital computer **402** may include a user input/output subsystem **408**. In some implementations, the user input/output subsystem includes one or more user input/output components such as a display **410**, mouse **412**, and/or keyboard **414**.

System bus **420** can employ any known bus structures or architectures, including a memory bus with a memory controller, a peripheral bus, and a local bus. System memory **422** may include non-volatile memory, such as read-only memory ("ROM"), static random access memory ("SRAM"), Flash NAND; and volatile memory such as random access memory ("RAM") (not shown).

Digital computer **402** may also include other non-transitory computer- or processor-readable storage media or non-volatile memory **416**. Non-volatile memory **416** may take a variety of forms, including: a hard disk drive for reading from and writing to a hard disk (e.g., magnetic disk), an optical disk drive for reading from and writing to removable optical disks, and/or a solid state drive (SSD) for reading from and writing to solid state media (e.g., NAND-based Flash memory). Non-volatile memory **416** may communicate with digital processor(s) via system bus **420** and may include appropriate interfaces or controllers **418** coupled to system bus **420**. Non-volatile memory **416** may serve as long-term storage for processor- or computer-readable instructions, data structures, or other data (sometimes called program modules) for digital computer **402**.

Although digital computer **402** has been described as employing hard disks, optical disks and/or solid state storage media, those skilled in the relevant art will appreciate that other types of nontransitory and non-volatile computer-readable media may be employed. Those skilled in the relevant art will appreciate that some computer architectures employ nontransitory volatile memory and nontransitory non-volatile memory. For example, data in volatile memory can be cached to non-volatile memory. Or a solid-state disk that employs integrated circuits to provide non-volatile memory.

Various processor- or computer-readable instructions, data structures, or other data can be stored in system memory **422**. For example, system memory **422** may store instruction for communicating with remote clients and scheduling use of resources including resources on the digital computer **402** and analog computer **404**. Also for example, system memory **422** may store at least one of processor executable instructions or data that, when executed by at least one processor, causes the at least one processor to execute the various algorithms to execute instructions. In some implementations system memory **422** may store processor- or computer-readable calculation instructions and/or data to perform pre-processing, co-processing, and post-processing to analog computer **404**. System memory **422** may store a set of analog computer interface instructions to interact with analog computer **404**.

Analog computer **404** may include at least one analog processor such as quantum processor **426**. Analog computer **404** can be provided in an isolated environment, for example, in an isolated environment that shields the internal

elements of the quantum computer from heat, magnetic field, and other external noise. The isolated environment may include a refrigerator, for instance a dilution refrigerator, operable to cryogenically cool the analog processor, for example to temperature below approximately 1° Kelvin.

Analog computer **404** can include programmable elements such as qubits, couplers, and other devices. Qubits can be read out via readout system **428**. Readout results can be sent to other computer- or processor-readable instructions of digital computer **402**. Qubits can be controlled via a qubit control system **430**. Qubit control system **430** can include on-chip DACs and analog lines that are operable to apply a bias to a target device. Couplers that couple qubits can be controlled via a coupler control system **432**. Couple control system **432** can include tuning elements such as on-chip DACs and analog lines. Qubit control system **430** and coupler control system **432** can be used to implement a quantum annealing schedule as described herein on analog processor **404**. Programmable elements can be included in quantum processor **426** in the form of an integrated circuit. Qubits and couplers can be positioned in layers of the integrated circuit that comprise a first material. Other devices, such as readout control system **432**, can be positioned in other layers of the integrated circuit that comprise a second material.

In some implementations, such as when forming a Josephson junction, three layers are required, that is, a base electrode, an insulating layer, and a counter electrode. The three layers are also referred to in the present application as a trilayer. The trilayer is also referred to in the present application as a Josephson junction trilayer. In these implementations, the base electrode layer is formed of a first superconducting material. The base electrode layer may, for example, be formed through a film deposition process, and the application may require that the base electrode layer have a certain thickness. For example, there may be certain thickness requirements in order to conduct a certain amount of superconducting current. In order to form high-integrity Josephson junctions, it may be desirable for the top surface of this base layer to be smooth prior to receiving the insulating layer. In some implementations, the insulating layer may be formed of a second superconducting material that is oxidized to form an insulating layer or may be formed from direct deposition of a layer of insulating material. The insulating layer is also referred to in the present application as a barrier layer. The barrier layer is also referred to in the present application as a tunnel barrier layer.

FIGS. **5**A to **5**D show sectional views of a portion of a superconducting integrated circuit fabricated at successive stages of fabrication, according to method **700** of FIG. **7**.

FIG. **5**A shows a sectional view of a portion of a superconducting integrated circuit **500***a* at a first stage of a fabrication process described by method **700** of FIG. **7**. In the depicted implementation, integrated circuit **500***a* includes a substrate **502**. In some implementations, substrate **502** may be at least one of silicon and sapphire. A base electrode layer **504** is deposited on substrate **502**. Base electrode layer **504** has a deposited top surface having a first roughness. It will be understood that the first roughness may be raised due to topological features formed during deposition of base electrode layer **504**. Base electrode layer **504** may be a first material that is superconductive in a first range of temperatures. In some implementations, base electrode layer **504** may be formed from niobium.

FIG. **5**B shows a sectional view of a portion of a superconducting integrated circuit **500***b* at a subsequent stage of the fabrication process. Superconducting integrated circuit **500***b* can be formed from integrated circuit **500***a* of FIG. **5**A by planarizing base electrode layer **504** to provide a planarized top surface having a second surface roughness that is less than the first surface roughness of base electrode layer **504**. Planarizing dielectric layer **506** and base electrode layer **504** may involve the use of a chemical-mechanical planarization process (also referred to in the present application as CMP) to reduce the roughness or surface topography created in the depositing of base electrode layer **504**. CMP is also referred to in the present application as a chemical-mechanical polishing process. In some implementations, the planarized top surface of base electrode layer **504** may be atomically smooth.

FIG. **5**C shows a sectional view of a portion of a superconducting integrated circuit **500***c* at a subsequent stage of the fabrication process. Superconducting integrated circuit **500***c* can be formed from integrated circuit **500***b* of FIG. **5**B by depositing an insulating layer **506** to overly at least a portion of base electrode layer **504**. In some implementations, insulating layer **506** may be formed by depositing a layer of aluminum, and allowing surface oxidation to form a layer of aluminum oxide on the top surface of the layer of aluminum. In other implementations, the insulating layer may be formed by direct deposition of aluminum oxide. In yet other implementations, the insulating layer may be formed by direct deposition of another insulating material.

FIG. **5**D shows a sectional view of a portion of a superconducting integrated circuit **500***d* at a subsequent stage of the fabrication process. Superconducting integrated circuit **500***d* can be formed from integrated circuit **500***c* of FIG. **5**C by depositing a counter electrode layer **508** to overly at least a portion of insulating layer **506**. Counter electrode layer **508** may be a first material that is superconductive in a first range of temperatures. In some implementations, counter electrode layer **508** may be formed from niobium. In some implementations, it may be desired to planarize the top surface of counter electrode layer **508** after deposition, in a similar manner to that described above with respect to FIG. **5**B.

It will be understood that while the stages of fabrication shown in FIG. **5**A to **5**D are shown as being completed on substrate **502**, similar processing operations may be employed at different locations on a superconducting integrated circuit, and multiple similar structures may be formed at varying heights within the circuit. It will further be understood that in some implementations, further processing operations may be included in the fabrication process, as will be discussed further below. For example, in some implementations, it may be desired to pattern the trilayer of FIG. **5**D, such as through masking and etching counter electrode layer **508**, insulating layer **506**, and base electrode layer **504**.

FIGS. **6**A to **6**I show sectional views of a portion of a superconducting integrated circuit fabricated at successive stages of fabrication, according to method **800** of FIG. **8**.

FIG. **6**A shows a sectional view of a portion of a superconducting integrated circuit **600***a* at a first stage of a fabrication process described by method **800** of FIG. **8**. In the depicted implementation, integrated circuit **600***a* includes a substrate **602**. In some implementations, substrate **602** may be at least one of silicon and sapphire. A base electrode layer **604** is deposited on substrate **602**. Base electrode layer **604** has a deposited top surface having a first roughness. It will be understood that the first roughness may be raised due to topological features formed during deposition of base electrode layer **604**. Base electrode layer **604** may be a first material that is superconductive in a first range

of temperatures. In some implementations, base electrode layer **504** may be formed from niobium.

FIG. **6**B shows a sectional view of a portion of a superconducting integrated circuit **600***b* at a subsequent stage of the fabrication process. Superconducting integrated circuit **600***b* can be formed from integrated circuit **600***a* of FIG. **6**A by patterning base electrode layer **604**. Patterning base electrode layer **604** may include masking and etching base electrode layer **604**.

FIG. **6**C shows a sectional view of a portion of a superconducting integrated circuit **600***c* at a subsequent stage of the fabrication process. Superconducting integrated circuit **600***c* can be formed from integrated circuit **600***b* of FIG. **6**B by depositing a dielectric layer **606**. In some implementations, dielectric layer **606** may comprise silicon dioxide.

FIG. **6**D shows a sectional view of a portion of a superconducting integrated circuit **600***d* at a subsequent stage of the fabrication process. Superconducting integrated circuit **600***d* can be formed from integrated circuit **600***c* of FIG. **6**C by planarizing dielectric layer **606** and base electrode layer **604** to provide a planarized top surface having a second surface roughness that is less than the first surface roughness of base electrode layer **604**. Planarizing dielectric layer **606** and base electrode layer **604** may involve the use of a chemical-mechanical planarization process (also referred to in the present application as CMP) to reduce the level of dielectric layer **606** to be planar with base electrode layer **604** and reduce the roughness or surface topography created in the depositing of base electrode layer **604**. CMP is also referred to in the present application as a chemical-mechanical polishing process. In some implementations, the planarized top surface of base electrode layer **604** may be atomically smooth.

FIG. **6**E shows a sectional view of a portion of a superconducting integrated circuit **600***e* at a subsequent stage of the fabrication process. Superconducting integrated circuit **600***e* can be formed from integrated circuit **600***d* of FIG. **6**D by depositing an insulating layer **608** to overly at least a portion of the smooth upper surface. In some implementations, insulating layer **608** may be formed by depositing a layer of aluminum, and allowing surface oxidation to form a layer of aluminum oxide on the top surface of the layer of aluminum. In other implementations, the insulating layer may be formed by direct deposition of aluminum oxide. In yet other implementations, the insulating layer may be formed by direct deposition of another insulating material.

FIG. **6**F shows a sectional view of a portion of a superconducting integrated circuit **600***f* at a subsequent stage of the fabrication process. Superconducting integrated circuit **600***f* can be formed from integrated circuit **600***e* of FIG. **6**E by depositing a counter electrode layer **610** to overly at least a portion of insulating layer **608**. Counter electrode layer **610** may be a first material that is superconductive in a first range of temperatures. In some implementations, counter electrode layer **610** may be formed from niobium.

FIG. **6**G shows a sectional view of a portion of a superconducting integrated circuit **600***g* at a subsequent stage of the fabrication process. Superconducting integrated circuit **600***g* can be formed from integrated circuit **600***f* by planarizing counter electrode layer **610** after deposition, in a similar manner to that described above with respect to FIG. **6**D.

FIG. **6**H shows a sectional view of a portion of a superconducting integrated circuit **600***h* at a subsequent stage of the fabrication process. Superconducting integrated circuit **600***h* can be formed from integrated circuit **600***g* by patterning insulating layer **608** and counter electrode **610**. This may, for example, include masking and etching insulating layer **608** and counter electrode **610**.

FIG. **6**I shows a sectional view of a portion of a superconducting integrated circuit **600***i* at a subsequent stage of the fabrication process. Superconducting integrated circuit **600***i* can be formed from integrated circuit **600***h* by depositing a second dielectric layer **612**. In some implementations, second dielectric layer **612** may comprise silicon dioxide. It will be understood that the patterning of insulating layer **608** and counter electrode **610** and deposition of second dielectric layer **612** may occur prior to planarization of counter electrode **610**, in a similar manner to the order of steps shown in FIGS. **6**A through **6**D.

It will be understood that while the stages of fabrication shown in FIG. **6**A to **6**I are shown as being completed on substrate **602**, similar processing steps may be employed at different locations on a superconducting integrated circuit, and multiple similar structures may be formed at varying heights within the circuit.

FIG. **7** is a flowchart illustrating a method **700** for fabricating a portion of a superconducting integrated circuit including planarization of a base electrode layer, in accordance with the present systems and methods. Method **700** includes acts **702-708**, though in other implementations, certain acts can be omitted and/or additional acts can be added. Method **700** can be performed by, for example, integrated circuit fabrication equipment in response to an initiation of a fabrication process.

At **702**, a base electrode layer is deposited. Base electrode layer may be deposited to overly a substrate in some implementations, or, in other implementations, may be placed over other structures such as other wiring layers and/or dielectric layers. In some implementations, the base electrode layer may be formed of niobium.

At **704**, the base electrode layer is planarized to provide a top surface having a lower surface roughness than the surface roughness of the top surface prior to planarizing. In some implementations, planarization may include polishing the base electrode layer back to a smooth surface. In some implementations, the planarization may be a CMP as discussed above.

At **706**, an insulating layer is deposited to overlie at least a portion of the base electrode layer. In some implementations, the insulating layer may be a layer of aluminum on which a layer of aluminum oxide is formed. In other implementations, the insulating layer may be formed by direct deposition of aluminum oxide or another insulating material.

At **708**, a counter electrode layer is deposited to overlie at least a portion of the base electrode layer and the insulating layer. In some implementations, the counter electrode may be formed of niobium.

It will be understood that other acts or operations may be included in forming the trilayer, as discussed further below with respect to method **800**. The counter electrode layer may be planarized after deposition in order to form a surface with reduced surface roughness at the top of the trilayer. Alternatively, after forming the trilayer, the trilayer may be patterned, and a dielectric material may be deposited over and around the trilayer. Planarization may then be performed to polish the dielectric layer back to the top surface of the counter electrode layer, and the dielectric layer and the counter electrode layer may be polished back to form a top surface of the counter electrode layer having reduced surface roughness.

Performing planarization of the base electrode layer prior to deposition of the insulating layer may provide a smoother

surface on which to deposit the insulating layer and the counter electrode. In some implementations, the film morphology may be a contributor to the integrity of structures formed, such as when Josephson junctions are formed. CMP may be used to polish the exposed base electrode surface in order to provide an atomically smooth surface prior to deposition of the insulating layer. In some implementations, the counter electrode layer may also be planarized in order to form a surface with reduced surface roughness prior to forming additional structures and electrical connections. For both the base electrode layer and the counter electrode layer, providing a reduced surface roughness of an electrode layer may serve to improve electrical connections formed with that layer by way of the smoothed surface.

FIG. **8** is a flowchart illustrating a method **800** for fabricating a portion of a superconducting integrated circuit including planarization of a base electrode layer, in accordance with the present systems and methods. Method **800** includes acts **802-812**, though in other implementations, certain acts can be omitted and/or additional acts can be added. Method **800** can be performed by, for example, integrated circuit fabrication equipment in response to an initiation of a fabrication process.

At **802**, a base electrode layer is deposited. Base electrode layer may be deposited to overly a substrate in some implementations, or, in other implementations, may be placed over other structures such as other wiring layers and/or dielectric layers. In some implementations, the base electrode layer may be formed of niobium.

At **804**, the base electrode layer is patterned. Patterning the base electrode layer may include masking and etching the base electrode layer.

At **806**, a dielectric layer is deposited to overlie at least a portion of the base electrode. The dielectric layer can fill openings around or between elements of the base electrode layer.

At **808**, the base electrode layer and the dielectric layer are planarized to provide a top surface having a lower surface roughness than the surface roughness of the top surface prior to planarizing. In some implementations, planarization may include polishing the dielectric layer back to an upper surface of the base electrode layer, and the dielectric layer and the base electrode layer may be polished back to a smooth surface. In some implementations, the planarization may be a CMP as discussed above.

At **810**, an insulating layer is deposited to overlie at least a portion of the surface formed by the base electrode layer and the dielectric layer. In some implementations, the insulating layer may be a layer of aluminum on which a layer of aluminum oxide is formed. In other implementations, the insulating layer may be formed by direct deposition of aluminum oxide or another insulating material.

At **812**, a counter electrode layer is deposited to overlie at least a portion of the base electrode layer and the insulating layer. In some implementations, the counter electrode may be formed of niobium.

At **814**, the counter electrode layer is planarized to provide a top surface having a lower surface roughness, as described at act **808** for the base electrode.

At **816**, the counter electrode layer and the insulating layer are patterned. Patterning the counter electrode layer and the insulating layer may include masking and etching the counter electrode layer and the insulating layer.

At **818**, a second dielectric layer is deposited. The dielectric layer can fill openings around or between elements formed by the counter electrode layer and the insulating layer. The second dielectric layer may be applied over the counter electrode layer and polished back to the surface of the counter electrode layer. It will also be understood that the second dielectric layer may be applied prior to planarizing the counter electrode, as described with respect to the base electrode at **808**. In this implementation, the second dielectric layer will be polished back to expose the upper surface of the counter electrode layer, and then both the second dielectric layer and the counter electrode layer may be polished back to form a top surface of the counter electrode layer having reduced surface roughness.

In view of the teachings of the implementations of methods **700** and **800** as discussed herein, it will be understood that the order of the acts or operations may be varied. For example, in method **800**, the base electrode layer may be planarized prior to being patterned and prior to the first dielectric layer being deposited. The surface roughness of the base electrode layer may be reduced prior to patterning and depositing of the first dielectric layer, and it may only be required to polish the first dielectric layer back to the surface of the base electrode layer.

Performing planarization of the base electrode layer and the dielectric layer prior to subsequent deposition acts may advantageously provide a smoother surface on which to deposit the insulating layer and the counter electrode. Similarly, performing planarization of the counter electrode layer may advantageously improve electrical connection to subsequent structures. Providing a reduced surface roughness of an electrode layer may serve to improve electrical connections formed with that layer by way of the smoothed surface. In some implementations, the film morphology may be a contributor to the integrity of structures formed, such as when Josephson junctions are formed. CMP may be used to polish the exposed base electrode surface in order to provide an atomically smooth surface prior to deposition of the insulating layer.

The above described method(s), process(es), or technique(s) could be implemented by a series of processor readable instructions stored on one or more nontransitory processor-readable media. Some examples of the above described method(s), process(es), or technique(s) method are performed in part by a specialized device such as an adiabatic quantum computer or a quantum annealer or a system to program or otherwise control operation of an adiabatic quantum computer or a quantum annealer, for instance a computer that includes at least one digital processor. The above described method(s), process(es), or technique(s) may include various acts, though those of skill in the art will appreciate that in alternative examples certain acts may be omitted and/or additional acts may be added. Those of skill in the art will appreciate that the illustrated order of the acts is shown for exemplary purposes only and may change in alternative examples. Some of the exemplary acts or operations of the above described method(s), process(es), or technique(s) are performed iteratively. Some acts of the above described method(s), process(es), or technique(s) can be performed during each iteration, after a plurality of iterations, or at the end of all the iterations.

The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the implementations to the precise forms disclosed. Although specific implementations of and examples are described herein for illustrative purposes, various equivalent modifications can be made without departing from the spirit and scope of the disclosure, as will be recognized by those skilled in the relevant art. The teachings provided herein of the various implementations can be applied to other methods of quantum computation,

not necessarily the exemplary methods for quantum computation generally described above.

The various implementations described above can be combined to provide further implementations. All of the commonly assigned US patent application publications, US patent applications, foreign patents, and foreign patent applications referred to in this specification and/or listed in the Application Data Sheet are incorporated herein by reference, in their entirety, including but not limited to: U.S. patent application Ser. No. 16/681,431, U.S. Provisional Patent Application No. 62/760,253, U.S. Pat. Nos. 7,876,248, 8,035,540, 8,098,179, 10,454,015, US Patent Publication No. 2018/0219150, and U.S. patent application Ser. No. 16/029,026.

These and other changes can be made to the implementations in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the claims to the specific implementations disclosed in the specification and the claims, but should be construed to include all possible implementations along with the full scope of equivalents to which such claims are entitled. Accordingly, the claims are not limited by the disclosure.

The invention claimed is:

1. A quantum processor comprising:

a first superconductive programmable device comprising a first type of material that has a respective critical temperature at which the first type of material superconducts, the respective critical temperature of the first type of material being an intrinsic property of the first type of material, the first superconductive programmable device comprising at least one first superconducting wiring layer and a first Josephson junction, the at least one first superconducting wiring layer comprising one or more first superconducting traces, and each of the at least one first superconducting wiring layer and the first Josephson junction comprising the first type of material;

a second superconductive device comprising a second type of material that has a respective critical temperature at which the second type of material superconducts, the respective critical temperature of the second type of material being an intrinsic property of the second type of material, the respective critical temperature of the second type of material being different from the respective critical temperature of the first type of material, the second superconductive device comprising at least one second superconducting wiring layer, the at least one second superconducting wiring layer comprising one or more second superconducting traces comprising the second type of material, and the first superconductive programmable device is more susceptible to noise than the second superconductive device; and

an insulative dielectric, the insulative dielectric separating at least a portion of the first superconductive programmable device from at least a portion of the second superconductive device.

2. The quantum processor of claim **1**, wherein the first superconductive programmable device comprises one of a qubit or a coupler.

3. The quantum processor of claim **1**, wherein the second superconductive device comprises one of a magnetometer, a transformer, an on-chip shield, and a readout control system.

4. The quantum processor of claim **1**, wherein the first type of material comprises aluminum and the second type of material comprises niobium.

5. The quantum processor of claim **1**, further comprising a passivation layer separating the first superconducting programmable device from the second superconducting device.

6. A quantum processor comprising:

a first portion comprising one or more first wiring layers comprising a first type of material that has a respective critical temperature at which the first type of material superconducts, the respective critical temperature of the first type of material being an intrinsic property of the first type of material;

a second portion comprising one or more second wiring layers comprising a second type of material that has a respective critical temperature at which the second type of material superconducts, the respective critical temperature of the second type of material being an intrinsic property of the second type of material, the respective critical temperature of the second type of material being different from the respective critical temperature of the first type of material being, the second portion distinct from the first portion;

a first superconductive programmable device comprising wiring in the first portion and a first Josephson junction, the wiring in the first portion comprising one or more first superconducting traces; and

a second superconductive device comprising wiring in the second portion, the wiring in the second portion comprising one or more second superconducting traces, and the first superconductive device is more susceptible to noise than the second superconductive device.

7. The quantum processor of claim **6**, wherein the one or more first wiring layers comprise analog circuitry.

8. The quantum processor of claim **6**, wherein the first superconductive programmable device comprises one of a qubit or a coupler.

9. The quantum processor of claim **6**, wherein the second superconductive device comprises one of a magnetometer, a transformer, an on-chip shield, and a readout control system.

10. The quantum processor of claim **6**, wherein the first type of material comprises aluminum and the second type of material comprises niobium.

11. The quantum processor of claim **6**, wherein an interface of the first portion and the second portion comprises a gradient of critical temperatures between the critical temperature of the first type of material and the critical temperature of the second type of material.

12. The quantum processor of claim **6**, further comprising a passivation layer interposed between the first portion and the second portion.

13. The quantum processor of claim **6**, wherein the second portion overlies the first portion.

14. The quantum processor of claim **6**, wherein the first portion overlies the second portion.

15. The quantum processor of claim **6**, further comprising a third portion comprising one or more additional wiring layers, the first portion being interposed between the second portion and the third portion.

16. The quantum processor of claim **6**, further comprising a substrate, the first portion and the second portion overlying the substrate.

17. The quantum processor of claim **16**, wherein the second portion overlies the substrate, and the first portion overlies the second portion.

18. The quantum processor of claim **6**, wherein the first portion comprises at least two wiring layers and the second portion comprises at least two wiring layers.

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