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(54) **ELECTRICAL REDUNDANCY FOR BONDED STRUCTURES**

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**H01L 25/065** (2023.01)  
**H01L 23/00** (2006.01)

(52) **U.S. Cl.**  
CPC ..... **H01L 25/0657** (2013.01); **H01L 24/06** (2013.01); **H01L 24/26** (2013.01); **H01L 24/93** (2013.01)

(58) **Field of Classification Search**  
CPC ..... H01L 25/0657; H01L 25/50; H01L 24/06; H01L 24/26; H01L 24/93  
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,753,536 A 5/1998 Sugiyama et al.  
5,771,555 A 6/1998 Eda et al.  
(Continued)

FOREIGN PATENT DOCUMENTS

JP 2013-033786 A 2/2013  
JP 2018-160519 10/2018  
(Continued)

OTHER PUBLICATIONS

Calderoni, Alessandro, "Memory Devices and Selectors for High-Density Memory Technology," International Electron Devices Meeting, Short Course 2: Technologies for Memory-Centric Computing, Dec. 8, 2019, 330 pages.

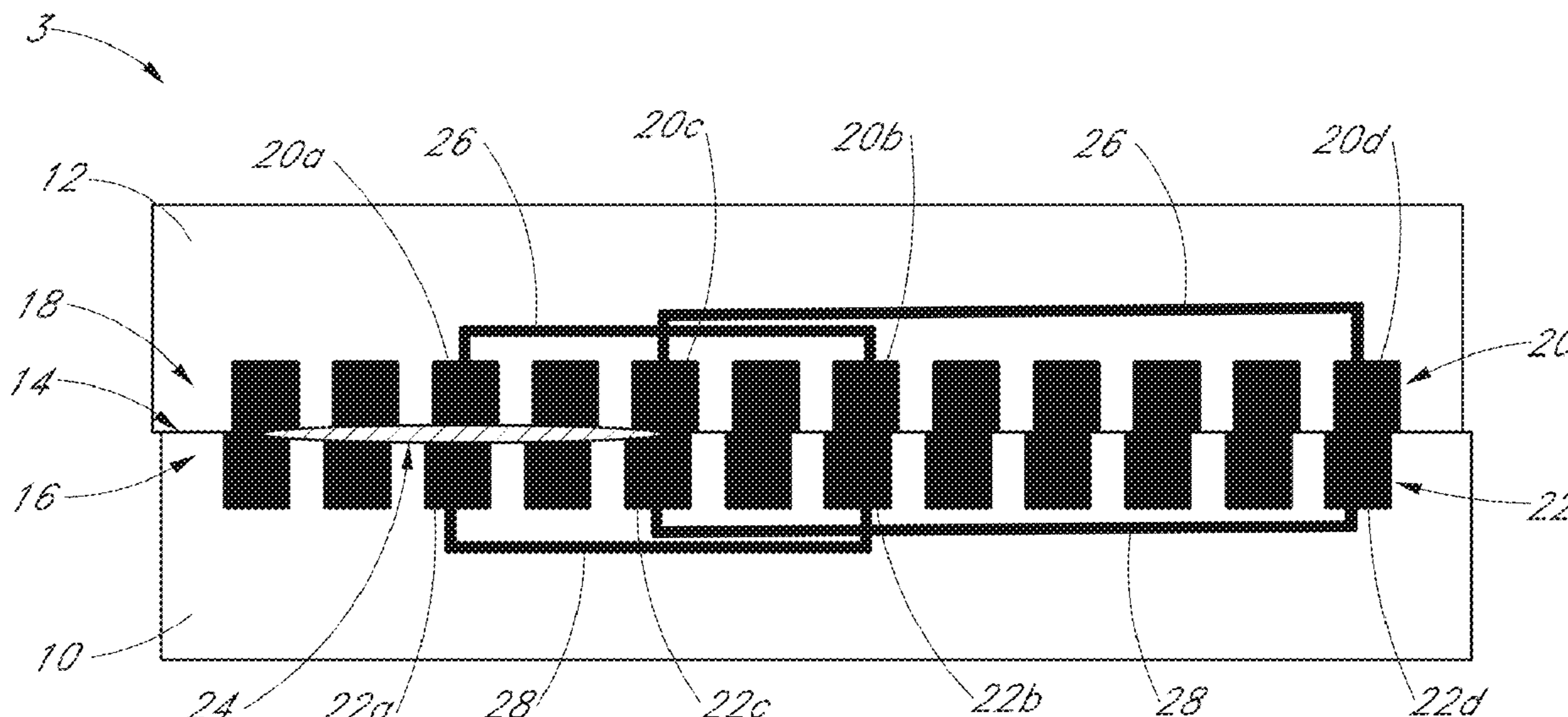
(Continued)

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(57) **ABSTRACT**

An element that is configured to bond to another element is disclosed. A first element that can include a first plurality of contact pads on a first surface. The first plurality of contact pads includes a first contact pad and a second contact pad that are spaced apart from one another. The first and second contact pads are electrically connected to one another for redundancy. The first element can be prepared for direct bonding. The first element can be bonded to a second element to form a bonded structure. The second element has a second plurality of contact pads on a second surface. At least one of the second plurality of contact pads is bonded and electrically connected to at least one of the first plurality of contact pads.

**33 Claims, 5 Drawing Sheets**



(56)

References Cited

U.S. PATENT DOCUMENTS

6,080,640 A	6/2000	Gardner et al.	10,522,499 B2	12/2019	Enquist et al.
6,255,899 B1	7/2001	Bertin et al.	10,707,087 B2	7/2020	Uzoh et al.
6,423,640 B1	7/2002	Lee et al.	10,727,219 B2	7/2020	Uzoh et al.
6,465,892 B1	10/2002	Suga	10,784,191 B2	9/2020	Huang et al.
6,887,769 B2	5/2005	Kellar et al.	10,790,262 B2	9/2020	Uzoh et al.
6,908,027 B2	6/2005	Tolchinsky et al.	10,804,255 B1 *	10/2020	Agarwal ..... H03K 3/037
7,045,453 B2	5/2006	Canaperi et al.	10,840,135 B2	11/2020	Uzoh
7,105,980 B2	9/2006	Abbott et al.	10,840,205 B2	11/2020	Fountain, Jr. et al.
7,193,423 B1	3/2007	Dalton et al.	10,854,578 B2	12/2020	Morein
7,385,283 B2	6/2008	Wu et al.	10,879,212 B2	12/2020	Uzoh et al.
7,750,488 B2	7/2010	Patti et al.	10,886,177 B2	1/2021	DeLaCruz et al.
7,803,693 B2	9/2010	Trezza	10,892,246 B2	1/2021	Uzoh
8,183,127 B2	5/2012	Patti et al.	10,923,408 B2	2/2021	Huang et al.
8,259,461 B2	9/2012	Hollis	10,923,413 B2	2/2021	DeLaCruz
8,349,635 B1	1/2013	Gan et al.	10,950,547 B2	3/2021	Mohammed et al.
8,377,798 B2	2/2013	Peng et al.	10,964,664 B2	3/2021	Mandalapu et al.
8,441,131 B2	5/2013	Ryan	10,985,133 B2	4/2021	Uzoh
8,476,165 B2	7/2013	Trickett et al.	10,991,804 B2	4/2021	DeLaCruz et al.
8,482,132 B2	7/2013	Yang et al.	10,998,292 B2	5/2021	Lee et al.
8,501,537 B2	8/2013	Sadaka et al.	11,004,757 B2	5/2021	Katkar et al.
8,524,533 B2	9/2013	Tong et al.	11,011,494 B2	5/2021	Gao et al.
8,620,164 B2	12/2013	Heck et al.	11,011,503 B2	5/2021	Wang et al.
8,647,987 B2	2/2014	Yang et al.	11,031,285 B2	6/2021	Katkar et al.
8,697,493 B2	4/2014	Sadaka	11,056,348 B2	7/2021	Theil
8,716,105 B2	5/2014	Sadaka et al.	11,088,099 B2	8/2021	Katkar et al.
8,802,538 B1	8/2014	Liu	11,127,738 B2	9/2021	DeLaCruz et al.
8,809,123 B2	8/2014	Liu et al.	11,158,606 B2	10/2021	Gao et al.
8,841,002 B2	9/2014	Tong	11,171,117 B2	11/2021	Gao et al.
9,064,862 B2	6/2015	Hwang et al.	11,176,450 B2	11/2021	Teig et al.
9,093,350 B2	7/2015	Endo et al.	11,256,004 B2	2/2022	Haba et al.
9,142,517 B2	9/2015	Liu et al.	11,264,357 B1	3/2022	DeLaCruz et al.
9,171,756 B2	10/2015	Enquist et al.	11,276,676 B2	3/2022	Enquist et al.
9,184,125 B2	11/2015	Enquist et al.	11,296,044 B2	4/2022	Gao et al.
9,224,704 B2	12/2015	Landru	11,329,034 B2	5/2022	Tao et al.
9,230,941 B2	1/2016	Chen et al.	11,348,898 B2	5/2022	DeLaCruz et al.
9,257,399 B2	2/2016	Kuang et al.	11,355,443 B2	6/2022	Huang et al.
9,299,736 B2	3/2016	Chen et al.	11,367,652 B2	6/2022	Uzoh et al.
9,312,229 B2	4/2016	Chen et al.	2004/0084414 A1	5/2004	Sakai et al.
9,331,149 B2	5/2016	Tong et al.	2005/0184398 A1	8/2005	Zhou et al.
9,337,235 B2	5/2016	Chen et al.	2006/0057945 A1	3/2006	Hsu et al.
9,385,024 B2	7/2016	Tong et al.	2007/0111386 A1	5/2007	Kim et al.
9,394,161 B2	7/2016	Cheng et al.	2011/0292708 A1	12/2011	Kang et al.
9,431,368 B2	8/2016	Enquist et al.	2011/0316572 A1	12/2011	Rahman
9,437,572 B2	9/2016	Chen et al.	2014/0175655 A1	6/2014	Chen et al.
9,443,796 B2	9/2016	Chou et al.	2015/0064498 A1	3/2015	Tong
9,461,007 B2	10/2016	Chun et al.	2015/0085195 A1	3/2015	Pereira et al.
9,496,239 B1	11/2016	Edelstein et al.	2015/0206824 A1	7/2015	Ramachandra et al.
9,536,848 B2	1/2017	England et al.	2015/0243611 A1	8/2015	Liu et al.
9,559,081 B1	1/2017	Lai et al.	2015/0346279 A1 *	12/2015	Douskey ..... G01R 31/3177 714/727
9,620,481 B2	4/2017	Edelstein et al.	2015/0380341 A1	12/2015	Chiou et al.
9,656,852 B2	5/2017	Cheng et al.	2016/0181228 A1	6/2016	Higuchi et al.
9,723,716 B2	8/2017	Meinhold	2016/0343682 A1	11/2016	Kawasaki
9,728,521 B2	8/2017	Tsai et al.	2017/0069593 A1	3/2017	Chou et al.
9,741,620 B2	8/2017	Uzoh et al.	2017/0125383 A1	5/2017	Liu
9,799,587 B2	10/2017	Fujii et al.	2017/0250160 A1	8/2017	Wu et al.
9,852,988 B2	12/2017	Enquist et al.	2018/0175012 A1	6/2018	Wu et al.
9,893,004 B2	2/2018	Yazdani	2018/0182639 A1	6/2018	Uzoh et al.
9,899,442 B2	2/2018	Katka	2018/0182666 A1	6/2018	Uzoh et al.
9,929,050 B2	3/2018	Lin	2018/0190580 A1	7/2018	Haba et al.
9,941,241 B2	4/2018	Edelstein et al.	2018/0190583 A1	7/2018	DeLaCruz et al.
9,941,243 B2	4/2018	Kim et al.	2018/0219038 A1	8/2018	Gambino et al.
9,953,941 B2	4/2018	Enquist	2018/0323177 A1	11/2018	Yu et al.
9,960,142 B2	5/2018	Chen et al.	2018/0323227 A1	11/2018	Zhang et al.
10,002,844 B1	6/2018	Wang et al.	2018/0323952 A1	11/2018	Chang et al.
10,026,605 B2	7/2018	Doub et al.	2018/0331066 A1	11/2018	Uzoh et al.
10,075,657 B2	9/2018	Fahim et al.	2019/0096741 A1	3/2019	Uzoh et al.
10,204,893 B2	2/2019	Uzoh et al.	2019/0115277 A1	4/2019	Yu et al.
10,269,756 B2	4/2019	Uzoh	2019/0131277 A1	5/2019	Yang et al.
10,276,619 B2	4/2019	Kao et al.	2019/0198409 A1	6/2019	Katkar et al.
10,276,909 B2	4/2019	Huang et al.	2019/0265411 A1	8/2019	Huang et al.
10,418,277 B2	9/2019	Cheng et al.	2019/0333550 A1	10/2019	Fisch
10,446,456 B2	10/2019	Shen et al.	2019/0385935 A1	12/2019	Gao et al.
10,446,487 B2	10/2019	Huang et al.	2019/0385966 A1	12/2019	Gao et al.
10,446,532 B2	10/2019	Uzoh et al.	2019/0385982 A1 *	12/2019	Lee ..... H01L 23/562
10,508,030 B2	12/2019	Katkar et al.	2020/0013637 A1	1/2020	Haba
			2020/0013765 A1	1/2020	Fountain, Jr. et al.
			2020/0035641 A1	1/2020	Fountain, Jr. et al.
			2020/0035643 A1	1/2020	Hirata et al.

(56)

References Cited

U.S. PATENT DOCUMENTS

2020/0075534 A1 3/2020 Gao et al.  
 2020/0075553 A1 3/2020 DeLaCruz et al.  
 2020/0118973 A1 4/2020 Wang et al.  
 2020/0126906 A1 4/2020 Uzoh et al.  
 2020/0194396 A1 6/2020 Uzoh  
 2020/0227367 A1 7/2020 Haba et al.  
 2020/0279821 A1 9/2020 Haba et al.  
 2020/0286875 A1 9/2020 Nishida et al.  
 2020/0294908 A1 9/2020 Haba et al.  
 2020/0328162 A1 10/2020 Haba et al.  
 2020/0328164 A1 10/2020 DeLaCruz et al.  
 2020/0328165 A1 10/2020 DeLaCruz et al.  
 2020/0335408 A1 10/2020 Gao et al.  
 2020/0371154 A1 11/2020 DeLaCruz et al.  
 2020/0395321 A1 12/2020 Katkar et al.  
 2020/0402959 A1 12/2020 Eom et al.  
 2020/0411483 A1 12/2020 Uzoh et al.  
 2021/0020601 A1 1/2021 Chen et al.  
 2021/0082865 A1 3/2021 Baraskar et al.  
 2021/0098412 A1 4/2021 Haba et al.  
 2021/0118864 A1 4/2021 DeLaCruz et al.  
 2021/0143125 A1 5/2021 DeLaCruz et al.  
 2021/0143921 A1 5/2021 Nasrullah et al.  
 2021/0181510 A1 6/2021 Katkar et al.  
 2021/0193603 A1\* 6/2021 DeLaCruz ..... G01R 31/275  
 2021/0193624 A1 6/2021 DeLaCruz et al.  
 2021/0242152 A1\* 8/2021 Fountain, Jr. .... H01L 24/80  
 2021/0296282 A1 9/2021 Gao et al.  
 2021/0305202 A1 9/2021 Uzoh et al.  
 2021/0366820 A1 11/2021 Uzoh  
 2021/0407941 A1 12/2021 Haba  
 2022/0077063 A1 3/2022 Haba  
 2022/0077087 A1 3/2022 Haba  
 2022/0139867 A1 5/2022 Uzoh  
 2022/0139869 A1 5/2022 Gao et al.  
 2022/0208650 A1 6/2022 Gao et al.  
 2022/0208702 A1 6/2022 Uzoh  
 2022/0208723 A1 6/2022 Katkar et al.  
 2022/0246497 A1 8/2022 Fountain, Jr. et al.  
 2022/0285303 A1 9/2022 Mirkarimi et al.  
 2022/0319901 A1 10/2022 Suwito et al.  
 2022/0320035 A1 10/2022 Uzoh et al.  
 2022/0320036 A1 10/2022 Gao et al.  
 2023/0005850 A1 1/2023 Fountain, Jr.  
 2023/0019869 A1 1/2023 Mirkarimi et al.  
 2023/0036441 A1 2/2023 Haba et al.  
 2023/0067677 A1 3/2023 Lee et al.  
 2023/0069183 A1 3/2023 Haba  
 2023/0100032 A1 3/2023 Haba et al.  
 2023/0115122 A1 4/2023 Uzoh et al.  
 2023/0122531 A1 4/2023 Uzoh  
 2023/0123423 A1 4/2023 Gao et al.  
 2023/0125395 A1 4/2023 Gao et al.  
 2023/0130259 A1 4/2023 Haba et al.  
 2023/0132632 A1 5/2023 Katkar et al.  
 2023/0140107 A1 5/2023 Uzoh et al.  
 2023/0142680 A1 5/2023 Guevara et al.  
 2023/0154816 A1 5/2023 Haba et al.  
 2023/0154828 A1 5/2023 Haba et al.  
 2023/0187264 A1 6/2023 Uzoh et al.  
 2023/0187317 A1 6/2023 Uzoh  
 2023/0187412 A1 6/2023 Gao et al.  
 2023/0197453 A1 6/2023 Fountain, Jr. et al.  
 2023/0197496 A1 6/2023 Theil  
 2023/0197559 A1 6/2023 Haba et al.  
 2023/0197560 A1 6/2023 Katkar et al.  
 2023/0197655 A1 6/2023 Theil et al.

2023/0207402 A1 6/2023 Fountain, Jr. et al.  
 2023/0207437 A1 6/2023 Haba  
 2023/0207474 A1 6/2023 Uzoh et al.  
 2023/0207514 A1 6/2023 Gao et al.  
 2023/0215836 A1 7/2023 Haba et al.  
 2023/0245950 A1 8/2023 Haba et al.

FOREIGN PATENT DOCUMENTS

WO WO 2005/043584 A2 5/2005  
 WO WO 2021/133671 A1 7/2021

OTHER PUBLICATIONS

Derbyshire, Katherine, "The Darker Side of Hybrid Bonding," Semiconductor Engineering, Dec. 17, 2020, 6 pages.  
 Ker, Ming-Dou et al., "Fully process-compatible layout design on bond pad to improve wire bond reliability in CMOS Ics," IEEE Transactions on Components and Packaging Technologies, Jun. 2002, vol. 25, No. 2, pp. 309-316.  
 Moriceau, H. et al., "Overview of recent direct wafer bonding advances and applications," Advances in Natural Sciences—Nanoscience and Nanotechnology, 2010, 11 pages.  
 Nakanishi, H. et al., "Studies on SiO<sub>2</sub>-SiO<sub>2</sub> bonding with hydrofluoric acid. Room temperature and low stress bonding technique for MEMS," Sensors and Actuators, 2000, vol. 79, pp. 237-244.  
 Oberhammer, J. et al., "Sealing of adhesive bonded devices on wafer level," Sensors and Actuators A, 2004, vol. 110, No. 1-3, pp. 407-412, see pp. 407-412, and Figures 1(a)-1(l), 6 pages.  
 Plobi, A. et al., "Wafer direct bonding: tailoring adhesion between brittle materials," Materials Science and Engineering Review Journal, 1999, R25, 88 pages.  
 International Search Report and Written Opinion dated Apr. 22, 2021, International Application No. PCT/US2020/066467, 12 pages.  
 Peters, Laura, "The Path To Known Good Interconnects," semiengineering.com/the-path-to-known-good-interconnects, Jan. 19, 2023, 13 pages (printed Jan. 24, 2023).  
 Morrison, Jim et al., "Samsung Galaxy S7 Edge Teardown," Tech Insights (posted Apr. 24, 2016), includes description of hybrid bonded Sony IMX260 dual-pixel sensor, <https://www.techinsights.com/blog/samsung-galaxy-s7-edge-teardown>, downloaded Jul. 11, 2023, 9 pages.  
 Sony IMX260 image, cross section of Sony dual-pixel sensor product labeled IMX260, showing peripheral probe and wire bond pads in a bonded structure. The part in the image was shipped in Apr. 2016. Applicant makes no representation that the part in the image is identical to the part identified in the separately submitted reference Morrison et al. (Tech Insights article dated Apr. 24, 2016), describing and showing a similar sensor product within the Samsung Galaxy S7; however the imaged part and the part shown in the Morrison et al. article share the part name "Sony IMX260".  
 Image of cross-section of onsemi's AR0820 CMOS Image Sensor. The product in the image was shipped on Sep. 16, 2021. Applicant makes no representation that the product in the image is identical to the product identified in the Bush, Nov. 8, 2018, ElectronicsWeekly.com article ("Bush article"); however, they share a product number.  
 Bush, Steve, "Electronica: Automotive power modules from On Semi," ElectronicsWeekly.com, indicating AR0820 product was to be demonstrated at a Nov. 2018 trade show, <https://www.electronicweekly.com/news/products/power-supplies/electronica-automotive-power-modules-semi:2018-11/> (published Nov. 8, 2018; downloaded Jul. 26, 2023) ("Bush article").

\* cited by examiner

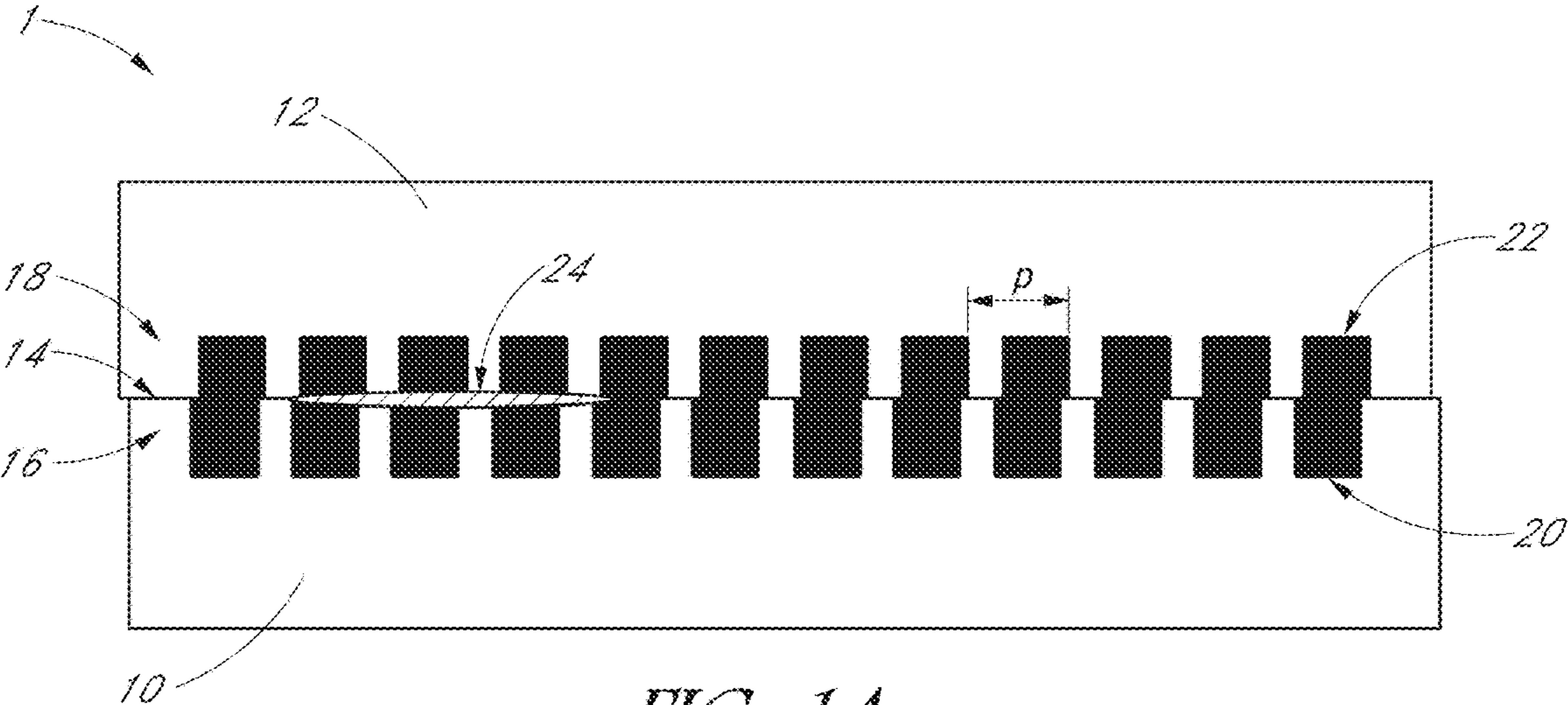


FIG. 1A

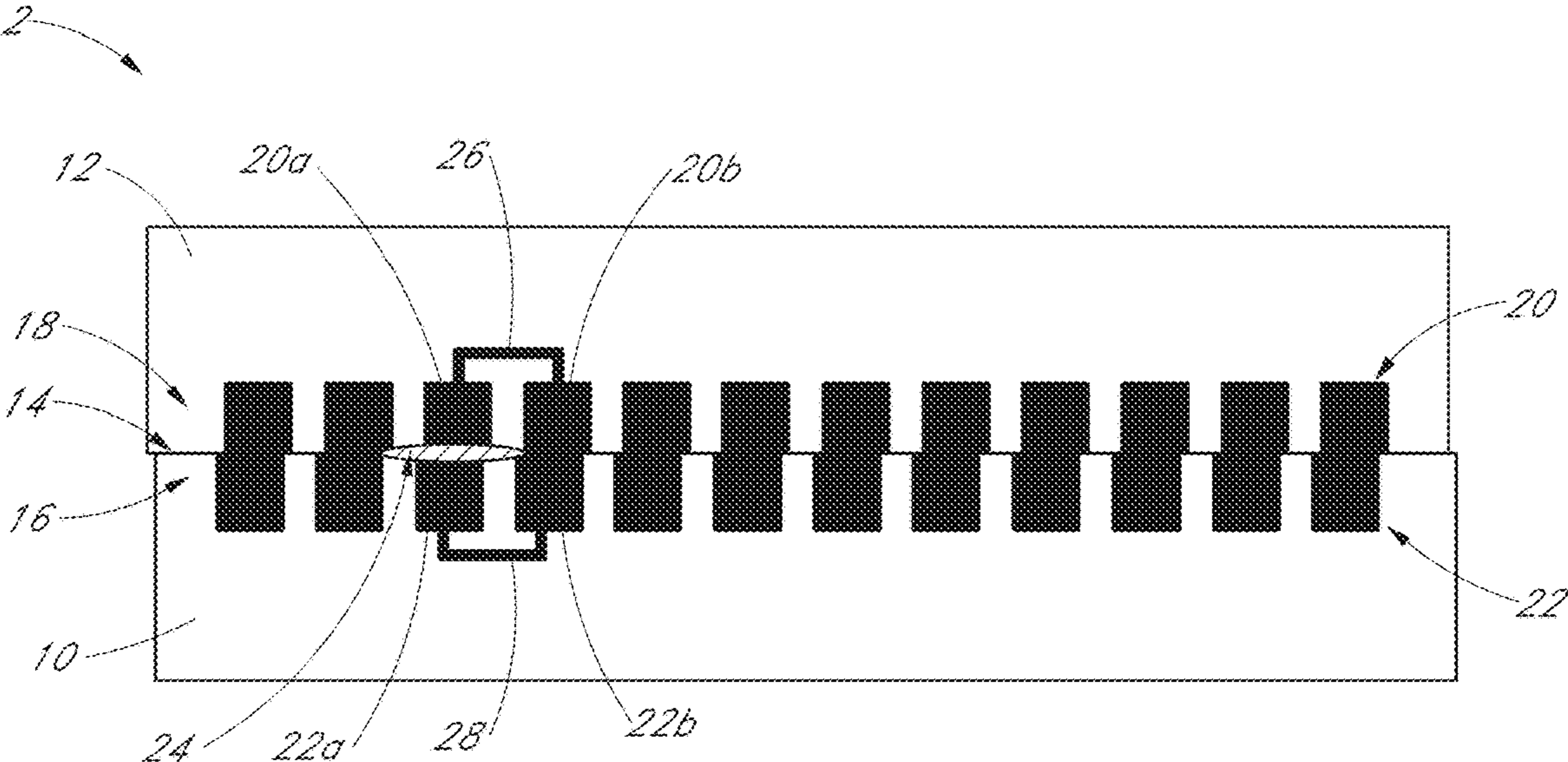


FIG. 1B

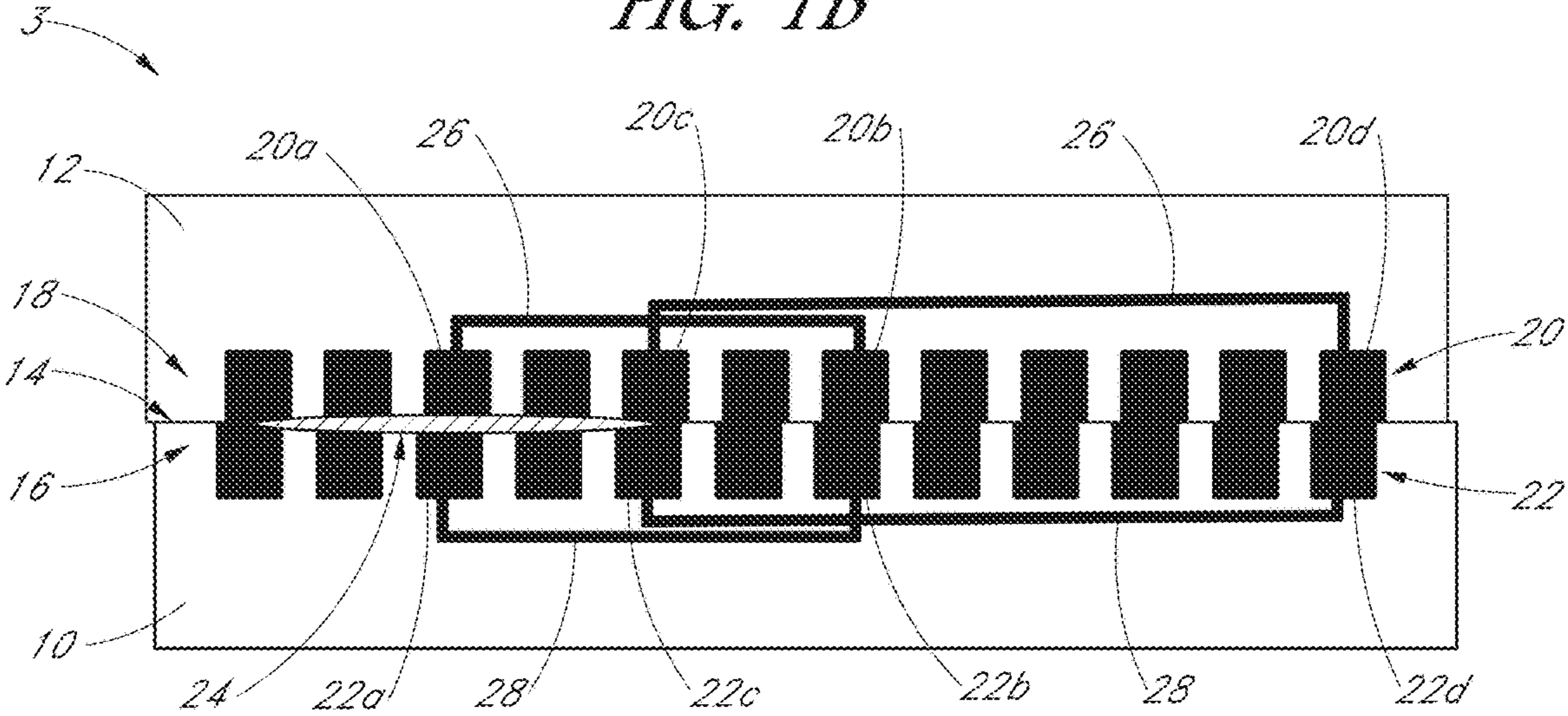
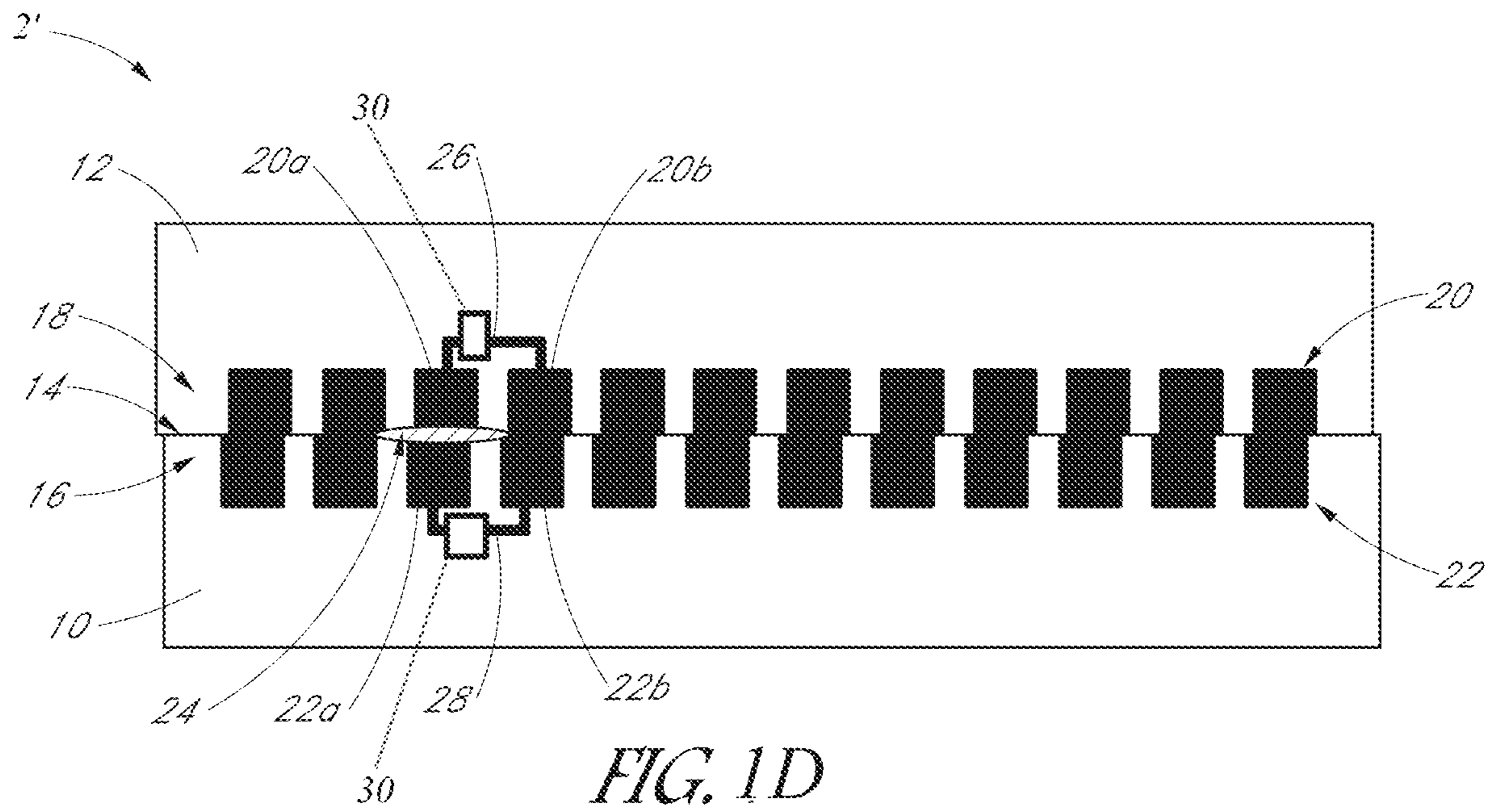


FIG. 1C



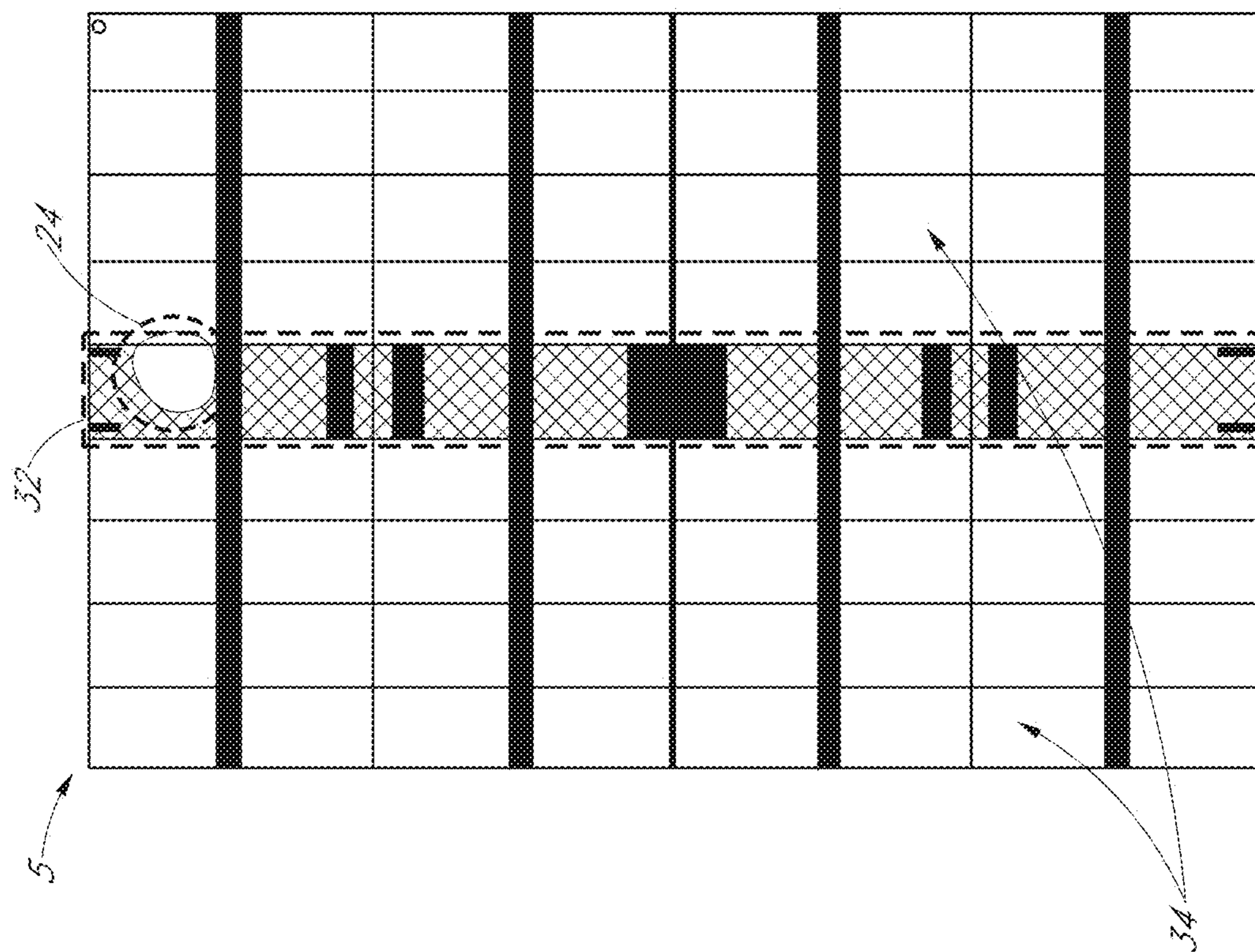


FIG. 2A

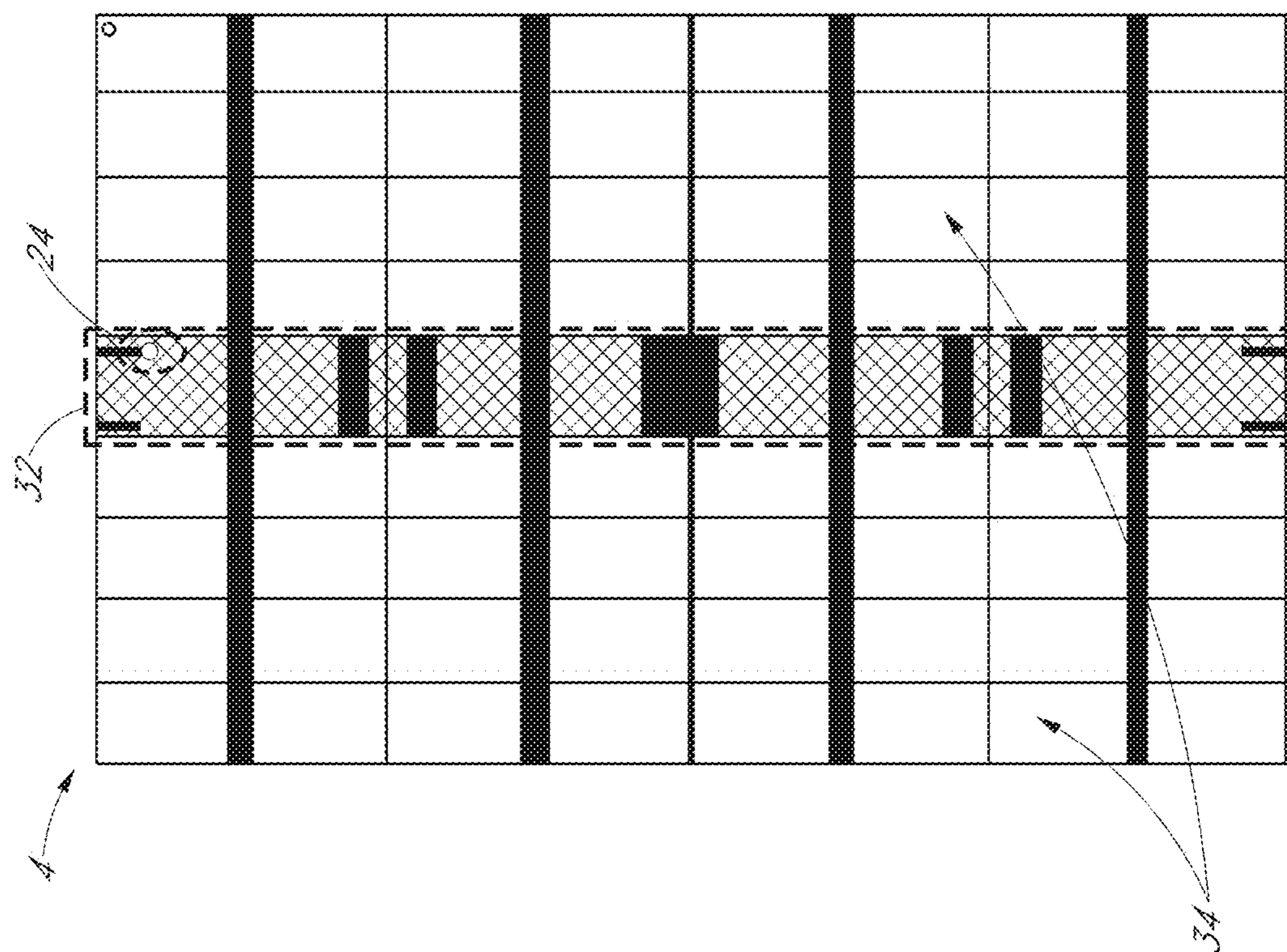


FIG. 2B

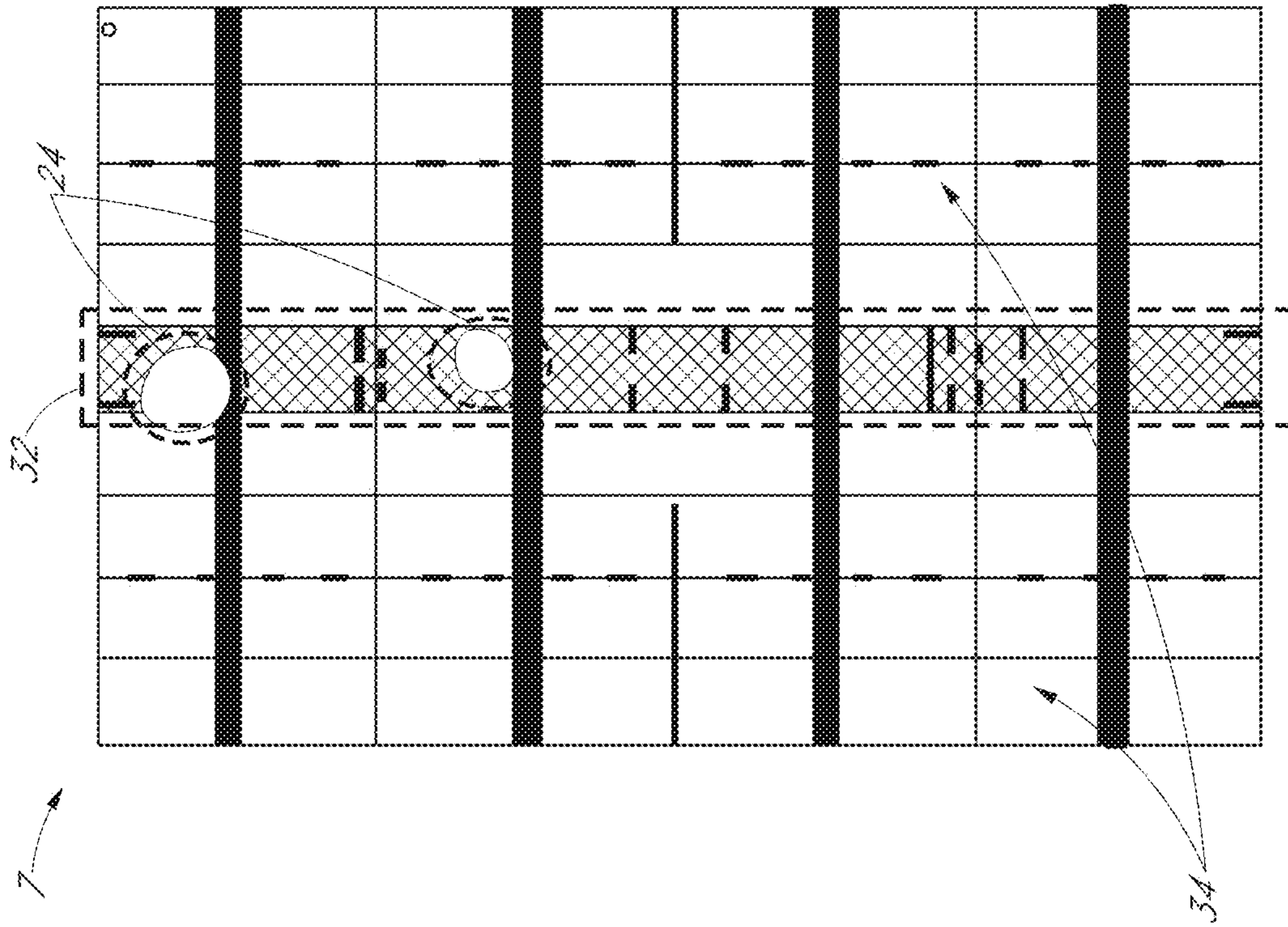


FIG. 2D

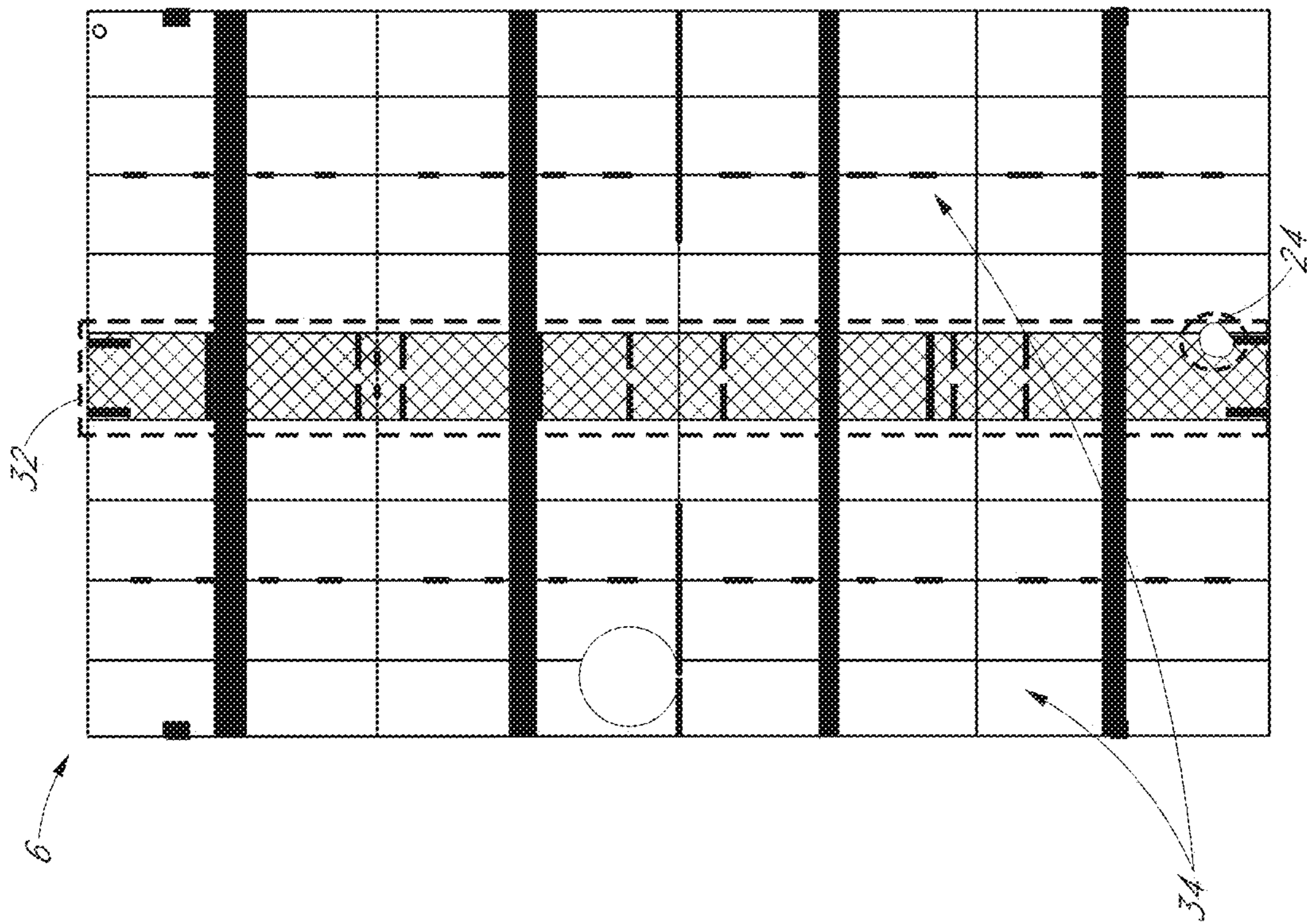


FIG. 2C

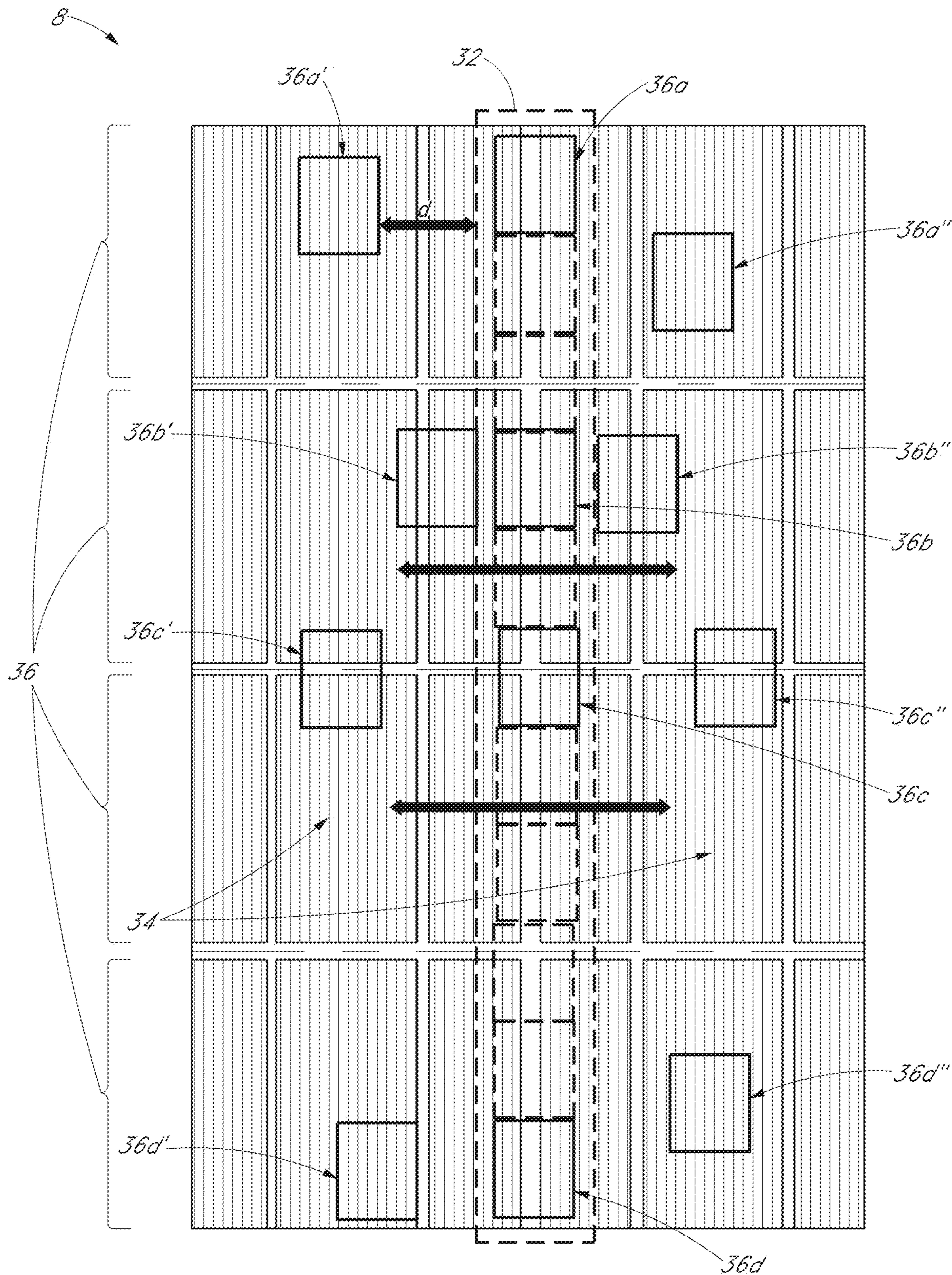


FIG. 2E



## ELECTRICAL REDUNDANCY FOR BONDED STRUCTURES

### CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to U.S. Provisional Patent Application No. 62/953,046, filed Dec. 23, 2019, the entire contents of which are hereby incorporated by reference herein in their entirety and for all purposes.

### BACKGROUND

#### Field of the Invention

The field relates to electrical redundancy for bonded structures and, in particular, for structures that are directly bonded without an adhesive.

#### Description of the Related Art

Multiple semiconductor elements (such as integrated device dies) may be stacked on top of one another in various applications, such as high bandwidth memory (HBM) devices or other devices that utilize vertical integration. The stacked elements can electrically communicate with one another through arrays of contact pads. It can be important to ensure that the electrical connections between contact pads on two stacked elements are reliable.

### BRIEF DESCRIPTION OF THE DRAWINGS

Specific implementations will now be described with reference to the following drawings, which are provided by way of example, and not limitation.

FIG. 1A is a schematic side sectional view of a bonded structure comprising a first element and a second element stacked on and bonded to the first element along a bonding interface.

FIG. 1B is a schematic side sectional view of a bonded structure comprising a first element and a second element stacked on and bonded to the first element along a bonding interface, according to one embodiment.

FIG. 1C is a schematic side sectional view of a bonded structure comprising a first element and a second element stacked on and bonded to the first element along a bonding interface, according to another embodiment.

FIG. 1D is a schematic side sectional view of a bonded structure comprising a first element and a second element stacked on and bonded to the first element along a bonding interface, according to another embodiment.

FIG. 2A is a schematic top plan view of a bonded structure showing example locations of faults.

FIG. 2B is a schematic top plan view of another bonded structure showing example locations of faults.

FIG. 2C is a schematic top plan view of another bonded structure showing example locations of faults.

FIG. 2D is a schematic top plan view of another bonded structure showing example locations of faults.

FIG. 2E is a schematic top plan view of another bonded structure having zones for redundant pads to provide backup connections in the event that bonding generates faults that interfere with some connections in a hybrid bonded structure.

### DETAILED DESCRIPTION

Two or more semiconductor elements (such as integrated device dies) may be stacked on or bonded to one another to

form a bonded structure. Conductive contact pads of one element may be electrically connected to corresponding conductive contact pads of another element. Any suitable number of elements can be stacked in the bonded structure.

In some embodiments, the elements are directly bonded to one another without an adhesive. In other embodiments, the elements may be bonded with a conductive adhesive, such as solder, etc.

In various embodiments, a dielectric field region of a first element (e.g., a first semiconductor device die with active circuitry) can be directly bonded (e.g., using dielectric-to-dielectric bonding techniques, such as the ZiBond® technique used by Xperi Corporation of San Jose, Calif.) to a corresponding dielectric field region of a second element (e.g., a second semiconductor device die with active circuitry) without an adhesive. For example, dielectric-to-dielectric bonds may be formed without an adhesive using the direct bonding techniques disclosed at least in U.S. Pat. Nos. 9,391,143 and 10,434,749, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes. Dielectrics that can be treated and activated for direct bonding include, for example, inorganic dielectrics, particularly those including silicon, such as silicon oxide (SiO<sub>2</sub>), silicon nitride (SiN), silicon carbide (SiC), silicon oxynitride (SiON), silicon oxycarbide (SiOC), silicon carbonitride (SiCN), etc.

In various embodiments, the hybrid direct bonds can be formed without an intervening adhesive. For example, dielectric bonding surfaces can be polished to a high degree of smoothness. The bonding surfaces can be cleaned and exposed to a plasma and/or etchants to activate the surfaces. In some embodiments, the surfaces can be terminated with a species after activation or during activation (e.g., during the plasma and/or etch processes). Without being limited by theory, in some embodiments, the activation process can be performed to break chemical bonds at the bonding surface, and the termination process can provide additional chemical species at the bonding surface that improves the bonding energy during direct bonding. In some embodiments, the activation and termination are provided in the same step, e.g., a plasma or wet etchant to activate and terminate the surfaces. In other embodiments, the bonding surface can be terminated in a separate treatment to provide the additional species for direct bonding. In various embodiments, the terminating species can comprise nitrogen. Further, in some embodiments, the bonding surfaces can be exposed to fluorine. For example, there may be one or multiple fluorine peaks near layer and/or bonding interfaces. Thus, in the directly bonded structures, the bonding interface between two dielectric materials can comprise a very smooth interface with higher nitrogen content and/or fluorine peaks at the bonding interface. Additional examples of activation and/or termination treatments may be found throughout U.S. Pat. Nos. 9,564,414; 9,391,143; and 10,434,749, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes.

In various embodiments, conductive contact pads of the first element can be directly bonded to corresponding conductive contact pads of the second element. For example, a hybrid bonding technique can be used to provide conductor-to-conductor direct bonds along a bond interface that includes covalently direct bonded dielectric-to-dielectric surfaces, prepared as described above. In various embodiments, the conductor-to-conductor (e.g., contact pad to contact pad) direct bonds and the dielectric-to-dielectric bonds can be formed using the direct hybrid bonding techniques disclosed at least in U.S. Pat. Nos. 9,716,033 and

9,852,988, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes.

For example, dielectric bonding surfaces can be prepared and directly bonded to one another without an intervening adhesive. Conductive contact pads (which may be surrounded by nonconductive dielectric field regions) may also directly bond to one another without an intervening adhesive. In some embodiments, the respective contact pads can be recessed below the dielectric field regions, for example, recessed by less than 20 nm, less than 15 nm, or less than 10 nm, for example, recessed in a range of 2 nm to 20 nm, or in a range of 4 nm to 10 nm. With such slight recessing or corresponding protrusion, the contact pads are still considered to be at the relevant element surface within the meaning of the present application. The dielectric field regions can be initially directly bonded to one another without an adhesive and without external pressure at room temperature in some embodiments and, subsequently, the bonded structure can be annealed. Upon annealing, the contact pads can expand and contact one another to form a metal-to-metal direct bond. Beneficially, the use of the hybrid bonding techniques known by the trade name Direct Bond Interconnect, or DBI®, can enable fine pixel pitches as explained above and/or high density of pads connected across the direct bond interface (e.g., small or fine pitches for regular arrays). In some embodiments, the pitch of the bonding pads may be less than 40 microns or less than 10 microns or even less than 2 microns. For some applications the ratio of the pitch of the bonding pads (a size of a pad plus a spacing between the pad to an adjacent pad) to one of the dimensions of the bonding pad (the size of the pad) is less than 5, or less than 3 and sometimes desirably less than 2. In various embodiments, the contact pads can comprise copper, although other metals may be suitable. In some embodiments, bonding pads can have two or more different pitches. For example, a pitch of the bonding pads may be about 40 microns in one area of the first and/or second element, and another pitch of the bonding pads may be 10 microns in another area of the first and/or second element.

In various embodiments, the contact pads can be formed in respective first and second arrays of pads on the first and second elements. If any debris or surface contaminant is present at the surface of the first or second elements, voids may be created at the bond interface, or debris may intervene between opposing contact pads. In addition, reactant byproducts generated during bonding and annealing, e.g. hydrogen and water vapor, may also form voids at the bond interface. These voids may effectively inhibit the joining of particular contact pads in the vicinity, creating openings or other failures in the bond. For example, any void larger than the pad diameter (or pitch) can potentially create an opening and hybrid bond failure.

Beneficially, various embodiments disclosed herein can provide electrical redundancy such that redundant contact pads (e.g., a pair of electrically redundant pads) are laterally separated by a spacing large enough to overcome typical void dimensions. In such embodiments, electrical connection can be made between two directly bonded elements even if one pair of corresponding contact pads are not directly connected due to a void at the bond interface, because a redundant pair for the same desired electrical connection are directly connected. The disclosed embodiments can accordingly improve device yield. In some cases, speed may be affected if, for example, the void occurs for a pad with a short connection. In various embodiments, redundancy may not be implemented for all the contact pads of an

element, and instead may be implemented for only a subset of the connections desired across the bond interface. In other embodiments, however, each desired connection across the bond interface may be provided with one or more redundant contact pads on both sides of the bond interface (redundant bond pad pairs). In some embodiments, the electrical redundancy may be provided for only signal pads, and may not be provided for power and ground pads. In other embodiments, electrical redundancy may also be provided for power and/or ground pads.

As explained herein, two or more pads for the same element (the same side of a bond interface) can be provided with pad redundancy by electrically shorting the two or more pads together. In various embodiments, the pads can be shorted together by a wire or trace that does not include any active circuitry or switches. The two or more pads can be spaced or offset for redundancy by a spacing in a range of 1 micron to 10 microns for pads near one another, or by a spacing in a range of 50 microns to 100 microns for pads in different regions of the bonded structure. In some arrangements, pads offset by large dimensions, when implemented due to voids, may affect speed due to increases in impedance with lengthened current paths; however, such redundancy improves the probability of making an adequate electrical contact even if the openings or voids may not be completely eliminated. In large devices, the electrical redundancy may result in lateral trace routing designs more complicated than in other structures.

In some embodiments, the element can comprise active circuitry, a switch, and/or an electronic fuse that is coupled to the trace. The active circuitry, switch or electronic fuse can selectively connect a preferred electrical path. Some logic may also be implemented in the first or second element such that when one or more contact pads in the first preferred electrical path is detected to have a faulty connection, the switch or electronic fuse may be activated to disconnect the preferred path and make the electrical connection for another electrical path utilizing redundant pads.

FIG. 1A is a schematic side sectional view of a bonded structure 1 comprising a first element 10 (e.g., a first semiconductor device die) and a second element 12 (e.g., a second semiconductor device die) stacked on and bonded to the first element 10 along a bonding interface 14. In the illustrated embodiment, the first and second elements 10, 12 are directly bonded without an adhesive. For example, corresponding dielectric field regions (e.g., a first dielectric field region 16 and a second dielectric field region 18) and corresponding contact pads (e.g., first contact pads 20 and second contact pads 22) may be directly bonded without an intervening adhesive in a direct hybrid bond arrangement. As explained above, if one or both of the first and second elements 10, 12 is contaminated or includes debris on the bonding surface(s), then one or more faults 24 may be present so as to impair direct hybrid bonding between the first and second elements at those locations. The fault(s) can include a void or an opening, and/or a debris. If the fault(s) 24 are at or near contact pads, then the electrical connection between two opposing or corresponding contact pads 20, 22 may be ineffective.

FIG. 1B is a schematic side sectional view of a bonded structure 2 comprising a first element 10 (e.g., a first semiconductor device die) and a second element 12 (e.g., a second semiconductor device die) stacked on and bonded to the first element 10 along a bonding interface 14. FIG. 1C is a schematic side sectional view of a bonded structure 3 comprising a first element 10 (e.g., a first semiconductor device die) and a second element 12 (e.g., a second semi-

conductor device die) stacked on and bonded to the first element **10** along a bonding interface **14**. As in FIG. 1A, in FIGS. 1B and 1C, corresponding dielectric field regions (e.g., a first dielectric field region **16** and a second dielectric field region **18**) and corresponding contact pads (e.g., first contact pads **20** and second contact pads **22**) may be directly bonded without an intervening adhesive in direct hybrid bonding arrangements.

In FIGS. 1B and 1C, in the event that one or more contact pads (e.g., the first contact pads **20**) may not electrically and/or directly contact one or more corresponding pads (e.g., the second contact pads **22**) on opposite dies or semiconductor elements (“an unconnected pad **20a**, **22a**,” see the first pad in FIGS. 1B and 1C) due to, for example, the fault(s) **24**, one or more conductive lines, shown in the form of traces **26**, **28**, can connect the unconnected pad **20a**, **22a** to another contact pad **20b**, **22b** to provide electrical redundancy. Although connections from the pads to internal circuitry are not shown, the skilled artisan will readily appreciate such connections exist, and that the traces **26**, **28** effectively connect that internal circuitry to both pads **20a**, **20b** or **22a**, **22b**. In some embodiments, internal circuitry **30** (see FIG. 1D) including a switch or an electronic fuse may also be used to allow either or both of pad pairs **20a**, **22a** and **20b**, **22b** to be in the electrical path connecting those contact pads to internal electrical circuitry in the bonded structure **2**. The internal circuitry **30** (see FIG. 1D) can be connected via conductive lines such as the traces **26** and/or **28** of first element or second element. The internal circuitry may also include some logic component to select one pad pair (e.g., the pads **20a**, **22a**) over other (e.g., the pads **20b**, **22b**). The trace(s) **26**, **28** can be provided in both the first and second elements **10**, **12**, as shown in FIGS. 1B and 1C. In other embodiments, the trace(s) **26**, **28** can be provided in only one of the first and second elements **10**, **12**. The trace(s) **26**, **28** can serve to electrically short a first unconnected contact pad **20a**, **20c**, **22a**, **22c** to a second functional and connected contact pad **20b**, **20d**, **22b**, **22d** to provide electrical redundancy. Thus, even though the first pad **20a** may not be electrically connected to a corresponding pad **22a** on the second element **12** (or vice versa), the second pad **20b** can provide the connection so that the bonded structure **2**, **3** maintains all electrical connections. In some embodiments, the trace(s) **26**, **28** connecting redundant pads lack switches or other circuitry that may otherwise add to complexity and impedance, and may be implemented entirely within the back-end-of-line (BEOL). FIGS. 1B and 1C show redundant for unconnected or poorly connected pad pairs **20a/22a**, **20c/22c** for purposes of illustration of the advantage of such redundancy. Of course, the skilled artisan will understand that the actual voids resulting in the unconnected or poorly connected pads do not exist at the time of die design, and may not occur at all after bonding, and the redundancy is best viewed as a prophylactic measure. Provision of the redundant connections greatly improves chances of successfully completing the desired electrical connections, regardless of whether such voids actually form in the course of direct hybrid bonding.

In FIG. 1B, the trace(s) **26**, **28** can connect and electrically short two pads **20a**, **20b/22a**, **22b** within each element that are near one another. In the illustrated embodiment, the trace(s) can connect two adjacent pads. In FIG. 1C, the trace(s) **26**, **28** can connect and short two pads **20a**, **20b/20c**, **20d/22a**, **22b/22c**, **22d** that are relatively far apart from one another, e.g., in different regions of the bonded structure. Providing an increased spacing between the first and second contact pads can beneficially improve the probability of

adequate electrical redundancy, since the increased spacing between shorted pads may be able to effectively position the second connected contact pad sufficiently far away from the fault(s) and the first unconnected contact pad. Therefore, a bonded structure with a trace(s) that connects pads that are relatively far apart can be particularly beneficial when the bonded structure has a relatively large fault(s).

In some embodiments, in which pads **20**, **22** form part of a regular array or distribution of contact pads, the first and second pads **20a**, **20b/22a**, **22b** can be spaced apart by a spacing that is at least a pitch  $p$  of the contact pads **20**, **22**, at least twice the pitch  $p$  of the contact pads **20**, **22**, at least three times the pitch  $p$ , or at least five times the pitch  $p$ . For purposes of this comparison, the pitch  $p$  can be associated with a minimum pitch of pads **20**, **22** along the first or second elements **10**, **12**, in cases where the shorted pads **20**, **22** may be parts of pad groups with different pitches. In some embodiments, the first and second pads **20a**, **20b/22a**, **22b** can be spaced apart by a spacing that is in a range of two to 1000 times the minimum pitch  $p$  of the pads **20**, **22**, in a range of two to 500 times the pitch  $p$ , or in a range of two to fifty times the pitch  $p$ . In some embodiments, the first and second pads **20a**, **20b/22a**, **22b** can be spaced apart such that at least one contact pad is disposed between the first and second pads **20a**, **20b/22a**, **22b**. For example, the first and second pads **20a**, **20b/22a**, **22b** can be spaced apart such that at least two contact pads, at least three contact pads, or at least four contact pads are disposed between the first and second pads. However, the skilled artisan will appreciate that even adjacent pads can be adequately spaced for achieving the desired redundancy, as shown in FIG. 1B, and that not all dies have regular bond pad patterns (i.e., not all semiconductor elements have identifiable pitches). In various embodiments, the first and second contact pads **20a**, **20b/22a**, **22b** can be spaced apart by a spacing in a range of 2 microns to 100 microns, in a range of 10 microns to 100 microns, in a range of 10 microns to 5 mm, in a range of 10 microns to 1000 microns, in a range of 50 microns to 5 mm, in a range of 50 microns to 1000 microns, in a range of 50 micron to 500 microns, in a range of 100 microns to 1000 microns, in a range of 100 microns to 500 microns, or in a range of 50 microns to 1500 microns.

FIG. 1D is a schematic side sectional view of a bonded structure **2'** comprising a first element **10** (e.g., a first semiconductor device die) and a second element **12** (e.g., a second semiconductor device die) stacked on and bonded to the first element **10** along a bonding interface **14**. The bonded structure **2'** illustrated in FIG. 1D is generally similar to the bonded structure **2** illustrated in FIG. 1B. The bonded structure **2'** can include internal circuitry **30** that is electrically coupled to the trace(s) **26**, **28**. The internal circuitry **30** can include a switch or an electronic fuse. In some embodiments, the internal circuitry **30** may be used to allow either or both of pad pairs **20a**, **22a** and **20b**, **22b** to be in the electrical path to be enabled. The internal circuitry **30** may also include some logic component to select one pad pair (e.g., the pads **20a**, **22a**) over other (e.g., the pads **20b**, **22b**). While illustrated as controlling conductivity along the traces **26**, **28** of both elements **10**, **12**, the skilled artisan will appreciate that the circuitry **30** can be provided on only one of the elements **10**, **12**. The internal circuitry **30** may be included in bonded structures that are the same as or general similar to the bonded structure **3** illustrated in FIG. 1C.

FIGS. 2A-2E are schematic top plan views of example bonded structures **4-8**. The bonded structures **4-8** can include devices. The devices in FIGS. 2A-2E represent stacked devices such as high bandwidth memory (HBM)

devices and other three-dimensional stacked devices. As shown in the top views of FIGS. 2A-2E, the bonded structures 4-8 can each comprise a high density via region or a conductive via region 32 in which conductive vias transfer signals vertically to dies within the stack of semiconductor elements, and peripheral regions 34 where there is room to provide redundant contact pads. It can be important to provide electrical redundancy for pads that are located within the conductive via regions 32. Beneficially, the space provided by the peripheral regions 34 or zones may include empty space that can be used for redundant contact pads.

As shown in FIG. 2A, the size of a fault 24 located in the via region 32 may be sufficiently small such that only a few pads may utilize the electrical redundancies disclosed herein. By contrast, in FIG. 2B, the size of the fault 24 may be sufficiently large such that a large number of pads (e.g., a majority or the entirety of pads in a particular zone or region) may utilize the electrical redundancies.

FIGS. 2C and 2D illustrate other examples of potential fault 24 locations and sizes that may interfere with electrical connections between directly bonded elements, such as dies. As in FIG. 2A, the size of a fault 24 located in the via region 32 shown in FIG. 2C may be sufficiently small such that only a few pads may utilize the electrical redundancies disclosed herein. By contrast, as in FIG. 2B, the size of the faults 24 may be sufficiently large in FIG. 2D such that a large number of pads (e.g., a majority or the entirety of pads in a particular zone or region) may utilize the electrical redundancies.

For example as shown in the top view of FIG. 2E, the bonded structure 8 can include a plurality of zones 36 along the conductive via regions 32 in which it may be important to provide electrical redundancy. In some embodiments, one zone of the plurality of zones 36 can include 50-1000 pads, e.g., about 200 to about 500 conductive pads. For example, for a first zone 36a of primary contacts, one or more redundant zones 36a', 36a" in the peripheral regions 34 can include contact pads electrically shorted to corresponding pads in the first zone 36a. Similarly, in a second zone 36b of primary contacts, one or more redundant zones 36b', 36b" in the peripheral regions 34 can include contact pads electrically shorted to corresponding pads in the second zone 36b. In a third zone 36c of primary pads, one or more redundant zones 36c', 36c" in the peripheral regions 34 can include contact pads electrically shorted to corresponding pads in the third zone 36c. In a fourth zone 36d of primary pads, one or more redundant zones 36d', 36d" in the peripheral regions 34 can include contact pads electrically shorted to corresponding pads in the fourth zone 36d.

In some embodiments, each of the redundant zones 36a', 36a", 36b', 36b", 36c', 36c", 36d', 36d" in the peripheral regions 34 can be spaced apart from the conductive via regions 32 by a distance d. In some embodiments, the distance d can be at least 10 microns. For example, the distance d can be in a range of 10 microns to 1000 microns, in a range of 50 microns to 1500 microns, or in a range of 100 microns to 1000 microns. In some embodiments, the distance d can be at least a pitch of the contact pads, or at least twice the pitch of the contact pads. For example, the distance d can be two to 1000 times the pitch, or two to 500 times the pitch. This distance d can be selected based upon experimentation to maximize the changes that no one given fault can interfere with both the primary and the redundant pad pairs.

In various embodiments, redundant pads may be provided only for signal pads, such that the connecting lines comprise signal lines, and may not be provided for power and/or ground pads. In other embodiments, redundant pads may

also be provided for power and/or ground pads. Any suitable number of zones may be provided. Each zone can have a plurality of pads. In some embodiments, redundancy can be provided on a per pad basis, such that each pad may include one or more corresponding redundant pads to which it is electrically shorted. Minor logic circuits can decide which zone is to be used. For example, logic circuits can be used to decide which redundant zone is to be used for unconnected pads.

In various embodiments, the first and second contact pads can be shorted within an element (e.g., in the first and/or second elements or dies), and can be separated by greater than 5 times a pitch of the pads. In some embodiments, first and second pads can be shorted in each of the first and second elements (e.g., upper and lower dies). In some embodiments, at least four contact pads can be disposed laterally between the first and second contact pads. In some embodiments, there is a void or delamination (e.g., debonding or lack of bonding) under one of the first and second contact pads. In some embodiments, two or more redundant contact pads can be shorted to at least one through substrate via (TSV). In some embodiments, two or more redundant contact pads can be shorted to two or more TSVs, which can provide the ability to shift signal traffic using redundancies based on openings, hot spots, etc.

Thus, in one embodiment, a bonded structure is disclosed. The bonded structure can include a first element having a first plurality of contact pads at a first surface, the first plurality of contact pads including a first contact pad and a second contact pad spaced apart from one another by at least 10 microns, the first and second contact pads electrically shorted to one another. The bonded structure can include a second element stacked on the first element, the second element having a second plurality of contact pads at a second surface, at least one of the second plurality of contact pads bonded and electrically connected to at least one of the first plurality of contact pads.

In some embodiments, the first and second contact pads can be spaced apart from one another by at least five times a first pitch of the first plurality of contact pads. The first and second contact pads can be spaced apart from one another by a spacing that is in a range of two to 1000 times the first pitch. The first and second contact pads can be spaced apart from one another by a spacing that is in a range of two to 500 times the pitch. The first and second contact pads can be spaced apart by at least 2 microns. The first and second contact pads can be spaced apart by a spacing in a range of 10 microns to 1000 microns. The first and second contact pads can be spaced apart by a spacing in a range of 50 microns to 1500 microns. The first and second contact pads can be spaced apart by a spacing in a range of 100 microns to 1000 microns. The at least one of the first plurality of contact pads can be directly bonded to the at least one of the second plurality of contact pads without an intervening adhesive. The bonded structure can include first and second dielectric field regions on the first and second elements, the first and second dielectric field regions directly bonded to one another without an adhesive. The first contact pad of the first element can be disposed opposite a third contact pad of the second element. The second contact pad of the first element can be disposed opposite a fourth contact pad of the second element. A void can be disposed between at least a portion of the first and third contact pads. The second and fourth contact pads can physically and electrically contact one another. The first and third contact pads may not be directly electrically connected to one another. The first contact pad of the first element can be disposed opposite a

third contact pad of the second element. The second contact pad of the first element can be disposed opposite a fourth contact pad of the second element. At least a portion of the first and third contact pads can be located at a bonding fault along a bonding interface between the first and second elements. The second and fourth contact pads can physically and electrically contact one another.

In another embodiment, a bonded structure is disclosed. The bonded structure can include a first element having a first plurality of spaced contact pads having a first pitch at a first surface, the first plurality of contact pads including a first contact pad and a second contact pad of the first plurality spaced apart from one another, the first and second contact pads electrically shorted to one another. The bonded structure can include a second element stacked on the first element, the second element having a second plurality of spaced contact pads at a second surface, at least one of the second plurality of contact pads bonded and electrically connected to at least one of the first plurality of contact pads.

In some embodiments, the first and second contact pads can be spaced apart from one another by at least five times the first pitch. The first and second contact pads can be spaced apart from one another by a spacing that is in a range of two to 1000 times the first pitch. The first and second contact pads can be spaced apart from one another by a spacing that is in a range of two to 500 times the pitch. The first and second contact pads can be spaced apart from one another by at least 10 microns. The first and second contact pads can be spaced apart by a spacing in a range of 10 microns to 1000 microns. The first and second contact pads can be spaced apart by a spacing in a range of 50 microns to 1500 microns. The first and second contact pads can be spaced apart by a spacing in a range of 100 microns to 1000 microns. The at least one of the first plurality of contact pads can be directly bonded to the at least one of the second plurality of contact pads without an intervening adhesive. The bonded structure can include first and second dielectric field regions on the first and second elements, the first and second dielectric field regions directly bonded to one another without an adhesive. The first contact pad of the first element can be disposed opposite a third contact pad of the second element. The second contact pad of the first element can be disposed opposite a fourth contact pad of the second element. A void can be disposed between at least a portion of the first and third contact pads. The second and fourth contact pads can physically and electrically contact one another. The first and third contact pads may not be directly electrically connected to one another. The first contact pad of the first element can be disposed opposite a third contact pad of the second element. The second contact pad of the first element can be disposed opposite a fourth contact pad of the second element. At least a portion of the first and third contact pads can be located at a bonding fault along a bonding interface between the first and second elements. The second and fourth contact pads can physically and electrically contact one another.

In one embodiment, the first contact pad and the second contact pad are spaced apart from one another by at least twice the first pitch.

In one aspect, a first element that is configured to directly bond to a second element without an intervening adhesive is disclosed. The first element can include a first plurality of contact pads that are positioned at a first surface of the first element. The first plurality of contact pads include a first contact pad and a second contact pad that are spaced apart from one another by at least 10 microns. The first plurality of contact pads are prepared for direct bonding. The first

element can also include a conductive line that electrically connects the first and second contact pads. The first and second contact pads are electrically connected to one another through the conductive line. The first element can further include a first dielectric field region positioned at the first surface of the first element. The first dielectric field region are disposed at least partially between the first and second contact pads. The first dielectric field region is prepared for direct bonding.

In one embodiment, the first and second contact pads are spaced apart from one another by at least five times a first pitch of the first plurality of contact pads. The first and second contact pads are spaced apart from one another by a spacing that is in a range of two to 1000 times the first pitch.

In one embodiment, the first and second contact pads are spaced apart by a spacing in a range of 10 microns to 1000 microns.

In one embodiment, each of the first plurality of contact pads is prepared to directly bond to each of a second plurality of contact pads of the second element without an intervening adhesive. The first dielectric field region on the first element is prepared to directly bond to a second dielectric field region of the second element without an adhesive.

In one embodiment, the first element further include a circuitry that is coupled to the first contact pad and the second contact pad along the conductive line. The circuitry can be configured to selectively enable shorting the first contact pad to the second contact pad. The circuitry comprises a switch or an electronic fuse.

In one aspect, a bonded structure is disclosed. The bonded structure can include a first element that has a first plurality of contact pads at a first surface. The first plurality of contact pads includes a first contact pad and a second contact pad that are spaced apart from one another. The first and second contact pads are electrically connected to one another. The bonded structure can also include a second element that is stacked on the first element. The second element has a second plurality of contact pads at a second surface corresponding to the first plurality of contact pads of the first element. At least one of the second plurality of contact pads is bonded and electrically connected to at least one of the first plurality of contact pads.

In one embodiment, the first contact pad and the second contact pad are spaced apart from one another according to a first pitch across the first plurality of contact pads.

In one embodiment, the first contact pad and the second contact pad are spaced apart from one another by at least twice the first pitch.

In one embodiment, the first and second contact pads are spaced apart from one another by at least five times the first pitch.

In one embodiment, the first and second contact pads are spaced apart from one another by a spacing that is in a range of two to 1000 times the first pitch.

In one embodiment, the first and second contact pads are spaced apart from one another by a spacing that is in a range of two to 500 times the pitch.

In one embodiment, the first and second contact pads are spaced apart from one another by at least 2 microns.

In one embodiment, the first and second contact pads are spaced apart from one another by at least 10 microns.

The first and second contact pads can be spaced apart by a spacing in a range of 10 microns to 1000 microns.

In one embodiment, the at least one of the first plurality of contact pads is directly bonded to the at least one of the second plurality of contact pads without an intervening

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adhesive. The bonded structure can further include first and second dielectric field regions on the first and second elements. The first and second dielectric field regions can be directly bonded to one another without an adhesive.

In one embodiment, the first contact pad of the first element is disposed opposite a third contact pad of the second element. The second contact pad of the first element can be disposed opposite a fourth contact pad of the second element. A void can be disposed between at least a portion of the first and third contact pads. The second and fourth contact pads can be physically and electrically contact one another. The first and third contact pads may not directly connected to one another.

In one embodiment, the first contact pad of the first element is disposed opposite a third contact pad of the second element. The second contact pad of the first element can be disposed opposite a fourth contact pad of the second element. At least a portion of the first and third contact pads can be located at a bonding fault along a bonding interface between the first and second elements. The second and fourth contact pads physically and electrically contact one another.

In one embodiment, the first contact pad and the second contact pad are electrically connected to one another by way of circuitry configured to selectively short the first contact pad to the second contact pad.

All of these embodiments are intended to be within the scope of this disclosure. These and other embodiments will become readily apparent to those skilled in the art from the following detailed description of the embodiments having reference to the attached figures, the claims not being limited to any particular embodiment(s) disclosed. Although this certain embodiments and examples have been disclosed herein, it will be understood by those skilled in the art that the disclosed implementations extend beyond the specifically disclosed embodiments to other alternative embodiments and/or uses and obvious modifications and equivalents thereof. In addition, while several variations have been shown and described in detail, other modifications will be readily apparent to those of skill in the art based upon this disclosure. It is also contemplated that various combinations or sub-combinations of the specific features and aspects of the embodiments may be made and still fall within the scope. It should be understood that various features and aspects of the disclosed embodiments can be combined with, or substituted for, one another in order to form varying modes of the disclosed implementations. Thus, it is intended that the scope of the subject matter herein disclosed should not be limited by the particular disclosed embodiments described above, but should be determined only by a fair reading of the claims that follow.

What is claimed is:

1. A first element configured to directly bond to a second element without an intervening adhesive, the first element comprising:

- a first plurality of contact pads at a first surface of the first element, the first plurality of contact pads including a first contact pad and a second contact pad spaced apart from one another by at least 10 microns, the first plurality of contact pads prepared for direct bonding;
- a conductive line electrically connecting the first and second contact pads; and
- a first dielectric field region at the first surface of the first element, the first dielectric field region disposed at least partially between the first and second contact pads, the first dielectric field region prepared for direct bonding,

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wherein the first plurality of contact pads further includes a third contact pad positioned between the first contact pad and the second contact pad, the third contact pad is electrically non-redundant of the first and second contact pads.

2. The first element of claim 1, wherein the first and second contact pads are spaced apart from one another by a spacing that is in a range of two to 1000 times a pitch of two adjacent contact pads of the first plurality of contact pads.

3. The first element of claim 1, wherein the conductive line is a signal line.

4. The first element of claim 1, wherein the first and second contact pads are spaced apart by a spacing in a range of 10 microns to 1000 microns.

5. The first element of claim 1, wherein each of the first plurality of contact pads is prepared to directly bond to each of a second plurality of contact pads of the second element without an intervening adhesive, and the first dielectric field region on the first element is prepared to directly bond to a second dielectric field region of the second element without an adhesive.

6. The first element of claim 1, further comprising a circuitry coupled to the first contact pad and the second contact pad along the conductive line, the circuitry configured to selectively enable electrical shorting the first contact pad to the second contact pad.

7. A bonded structure comprising:

a first element having a first plurality of contact pads at a first surface, the first plurality of contact pads including a first contact pad and a second contact pad spaced apart from one another by at least 10 microns, the first and second contact pads electrically shorted to one another; and

a second element stacked on the first element, the second element having a second plurality of contact pads at a second surface, at least one of the second plurality of contact pads bonded and electrically connected to at least one of the first plurality of contact pads,

wherein the first plurality of contact pads further includes a third contact pad positioned between the first contact pad and the second contact pad, and wherein no electrical redundancy is provided for the third contact pad.

8. The bonded structure of claim 7, wherein the first and second contact pads are spaced apart from one another by at least five times a first pitch of the first plurality of contact pads.

9. The bonded structure of claim 7, wherein the first and second contact pads are spaced apart by a spacing in a range of 50 microns to 1500 microns.

10. The bonded structure of claim 7, further comprising first and second dielectric field regions on the first and second elements, the first and second dielectric field regions directly bonded to one another without an adhesive, wherein the at least one of the first plurality of contact pads is directly bonded to the at least one of the second plurality of contact pads without an intervening adhesive.

11. The bonded structure of claim 7, wherein the first contact pad of the first element is disposed opposite a fourth contact pad of the second element, wherein the second contact pad of the first element is disposed opposite a fifth contact pad of the second element, wherein a void is disposed between at least a portion of the first and fourth contact pads, and wherein the second and fifth contact pads physically and electrically contact one another.

12. The bonded structure of claim 7, wherein the first contact pad of the first element is disposed opposite a fourth contact pad of the second element, wherein the second

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contact pad of the first element is disposed opposite a fifth contact pad of the second element, wherein at least a portion of the first and fourth contact pads are located at a bonding fault along a bonding interface between the first and second elements, and wherein the second and fifth contact pads physically and electrically contact one another.

**13.** A bonded structure comprising:

a first element having a first plurality of contact pads at a first surface, the first plurality of contact pads including a first contact pad and a second contact pad spaced apart from one another, and an intervening contact pad disposed between the first and second contact pads, wherein the first and second contact pads are electrically connected to one another and the intervening contact pad is electrically non-redundant of the first and second contact pads; and

a second element stacked on the first element, the second element having a second plurality of contact pads on a second surface, at least one of the second plurality of contact pads bonded and electrically connected to at least one of the first plurality of contact pads.

**14.** The bonded structure of claim **13**, wherein the first and second contact pads are spaced apart from one another by at least five times a pitch of the first plurality of contact pads.

**15.** The bonded structure of claim **13**, wherein the first and second contact pads are spaced apart from one another by a spacing that is in a range of two to 1000 times a pitch of the first plurality of contact pads.

**16.** The bonded structure of claim **13**, wherein the first and second contact pads are spaced apart from one another by a spacing that is in a range of two to 500 times a pitch of the first plurality of contact pads.

**17.** The bonded structure of claim **13**, wherein the at least one of the first plurality of contact pads is directly bonded to the at least one of the second plurality of contact pads without an intervening adhesive.

**18.** The bonded structure of claim **17**, further comprising first and second dielectric field regions on the first and second elements, the first and second dielectric field regions directly bonded to one another without an adhesive.

**19.** The bonded structure of claim **13**, wherein the first contact pad of the first element is disposed opposite a third contact pad of the second element, wherein the second contact pad of the first element is disposed opposite a fourth contact pad of the second element, wherein a void is disposed between at least a portion of the first and third

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contact pads, and wherein the second and fourth contact pads physically and electrically contact one another.

**20.** The bonded structure of claim **13**, wherein the first contact pad and the second contact pad are spaced apart from one another by at least twice a pitch of the first plurality of contact pads.

**21.** The bonded structure of claim **7**, wherein the first element comprises a first zone having a third plurality of contact pads including the first contact pad and a second zone having a fourth plurality of contact pads including the second contact pad, the third plurality of contact pads are electrically shorted to corresponding pads of the fourth plurality of contact pads in the second zone.

**22.** The bonded structure of claim **13**, wherein the first and second contact pads electrically connected to one another through a conductive trace.

**23.** The bonded structure of claim **13**, wherein the first and second contact pads are signal pads.

**24.** The bonded structure of claim **13**, wherein the first and second contact pads are spaced apart from one another by at least **10** microns.

**25.** The bonded structure of claim **13**, wherein the first and second contact pads are spaced apart from one another by a spacing in a range of **1** micron to **10** microns.

**26.** The bonded structure of claim **13**, wherein the first and second contact pads are spaced apart from one another by a spacing in a range of **2** microns to **100** microns.

**27.** The bonded structure of claim **26**, wherein the first and second contact pads are spaced apart from one another by a spacing in a range of **50** microns to **100** microns.

**28.** The bonded structure of claim **22**, wherein the conductive trace is formed in a back-end-of line (BEOL) layer.

**29.** The bonded structure of claim **22**, wherein the conductive trace lacks switches and other circuitry between the first and second contact pads.

**30.** The bonded structure of claim **13**, further comprising a plurality of pads disposed between the first and second contact pads, the plurality of pads comprising the intervening contact pad.

**31.** The first element of claim **1**, wherein no electrical redundancy is provided for the third contact pad.

**32.** The first element of claim **31**, wherein the first and second contact pads are signal pads.

**33.** The first element of claim **32**, wherein the third contact pad is a power or ground pad.

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