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Ned et al.

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(54) **SENSOR HEADER ASSEMBLY FOR INCREASED RELIABILITY IN HIGH-PRESSURE ENVIRONMENTS**

13/025; G01L 19/14; G01L 19/0038; G01L 19/0084; G01L 9/0055; G01L 9/0075; G01L 19/0069; G01L 9/0052; (Continued)

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(57) **ABSTRACT**

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Header construction and techniques are disclosed that utilize header layers that provide support for electrical interconnections. A sensor header assembly includes: an upper header layer having upper through holes arranged in a first configuration; a lower header layer having lower through holes arranged in a second configuration axially offset relative to the first configuration; depressions extending from the lower header layer top surface and partially through the lower header layer, each depression defining a footprint corresponding to the first configuration of the corresponding upper through holes of the upper header layer; upper header pins extending through the corresponding upper through holes and at least partially into the corresponding lower level depressions; and lower header pins extending through the corresponding lower through holes and in electrical communication with the corresponding upper header pins. The depressions form support surfaces for supporting at least the corresponding upper header pins during high-pressure operation.

(65) **Prior Publication Data**

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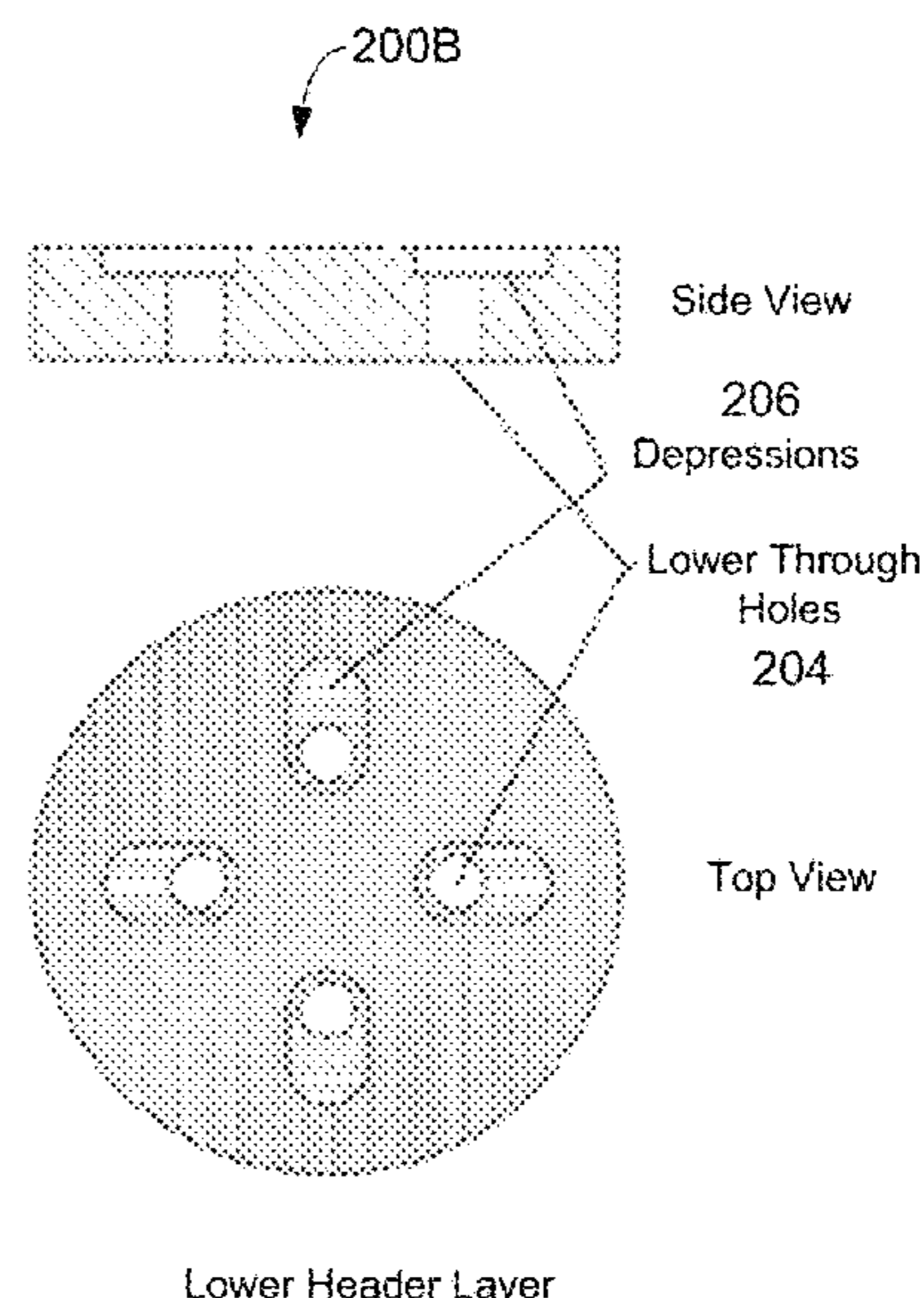
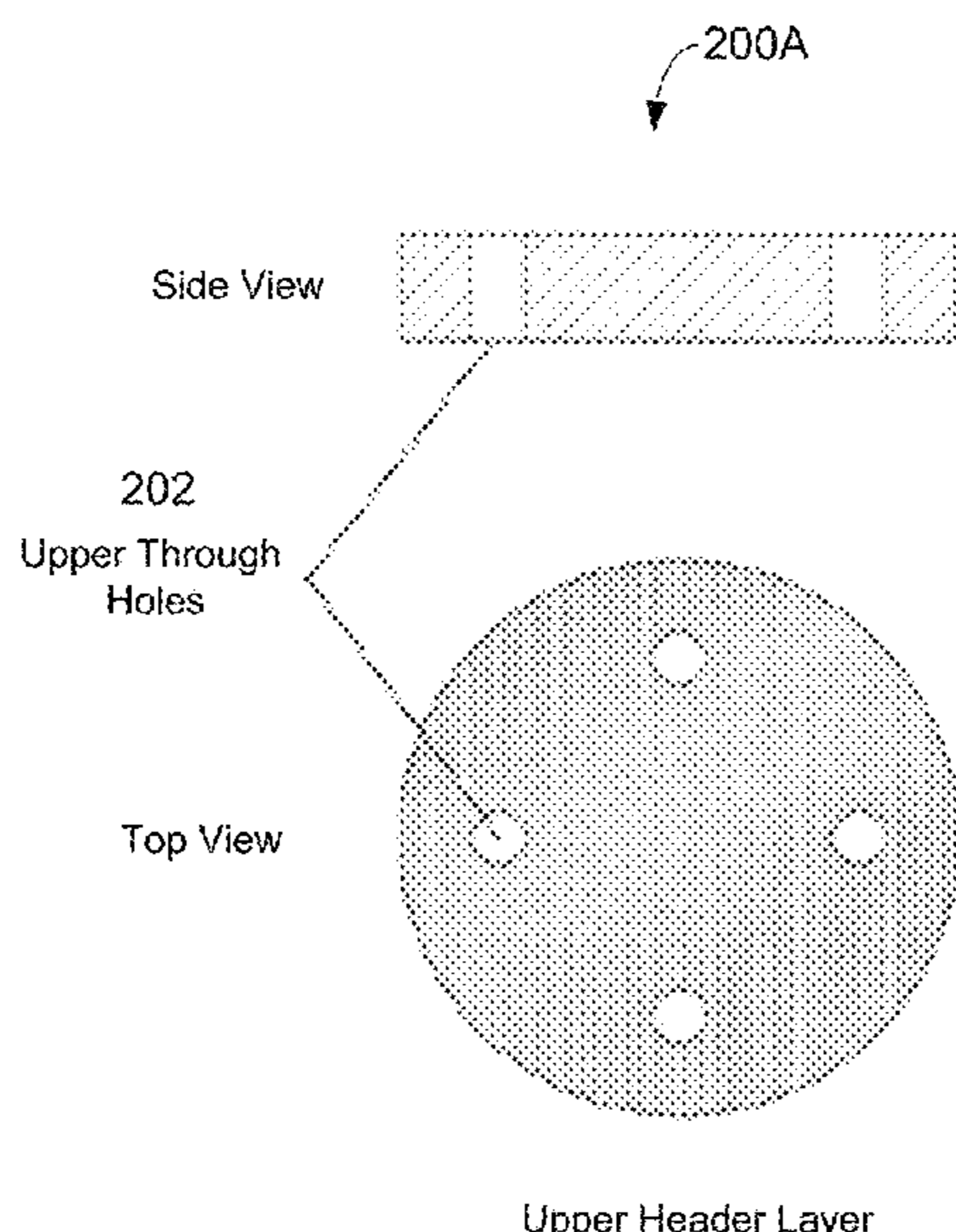
(63) Continuation of application No. 17/034,533, filed on Sep. 28, 2020, now Pat. No. 11,467,049, which is a (Continued)

(51) **Int. Cl.**
G01L 19/00 (2006.01)
G01L 19/14 (2006.01)

(52) **U.S. Cl.**
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(58) **Field of Classification Search**
CPC G01L 19/147; G01L 9/0042; G01L 19/04; G01L 9/0054; G01L 9/0072; G01L

20 Claims, 7 Drawing Sheets



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(58) **Field of Classification Search**

CPC G01L 9/0073; G01L 19/0092; G01L 19/0618; G01L 19/0645; G01L 19/143; G01L 9/0051; G01L 19/0007; G01L 19/0046; G01L 19/06; G01L 19/0627; G01L 19/0681; G01L 27/002; G01L 9/00; G01L 9/0041; G01L 9/0044; G01L 11/025; G01L 11/04; G01L 19/0023; G01L 19/0672; G01L 19/069; G01L 19/142; G01L 19/145; G01L 19/16; G01L 7/00; G01L 9/0047; G01L 9/06; G01L 9/065; G01L 9/12; G01L 11/02; G01L 13/00; G01L 15/00; G01L 19/0015; G01L 19/003; G01L 19/02; G01L 19/0609; G01L 19/083; G01L 19/10; G01L 19/148; G01L 27/005; G01L 7/08; G01L 7/082; G01L 7/163; G01L 7/166; G01L 9/0045; G01L 9/0048; G01L 9/006; G01L 9/007; G01L 9/0076; G01L 9/04; G01L 9/045; G01L 9/125; G01L 11/00; G01L 17/00;

G01L 19/00; G01L 19/0076; G01L 19/08; G01L 19/141; G01L 19/146; G01L 1/142; G01L 1/2262; G01L 1/246; G01L 21/12; G01L 23/16; G01L 27/007; G01L 7/04; G01L 7/063; G01L 7/084; G01L 7/086; G01L 7/16; G01L 9/0002; G01L 9/0007; G01L 9/0016; G01L 9/0019; G01L 9/0022; G01L 9/0027; G01L 9/0033; G01L 9/0039; G01L 9/005; G01L 9/0058; G01L 9/0077; G01L 9/0079; G01L 9/008; G01L 9/0092; G01L 9/0095; G01L 9/025; G01L 9/08; G01L 9/085; G01L 9/105; G01L 9/14; G01L 9/16

USPC 73/700–756
See application file for complete search history.

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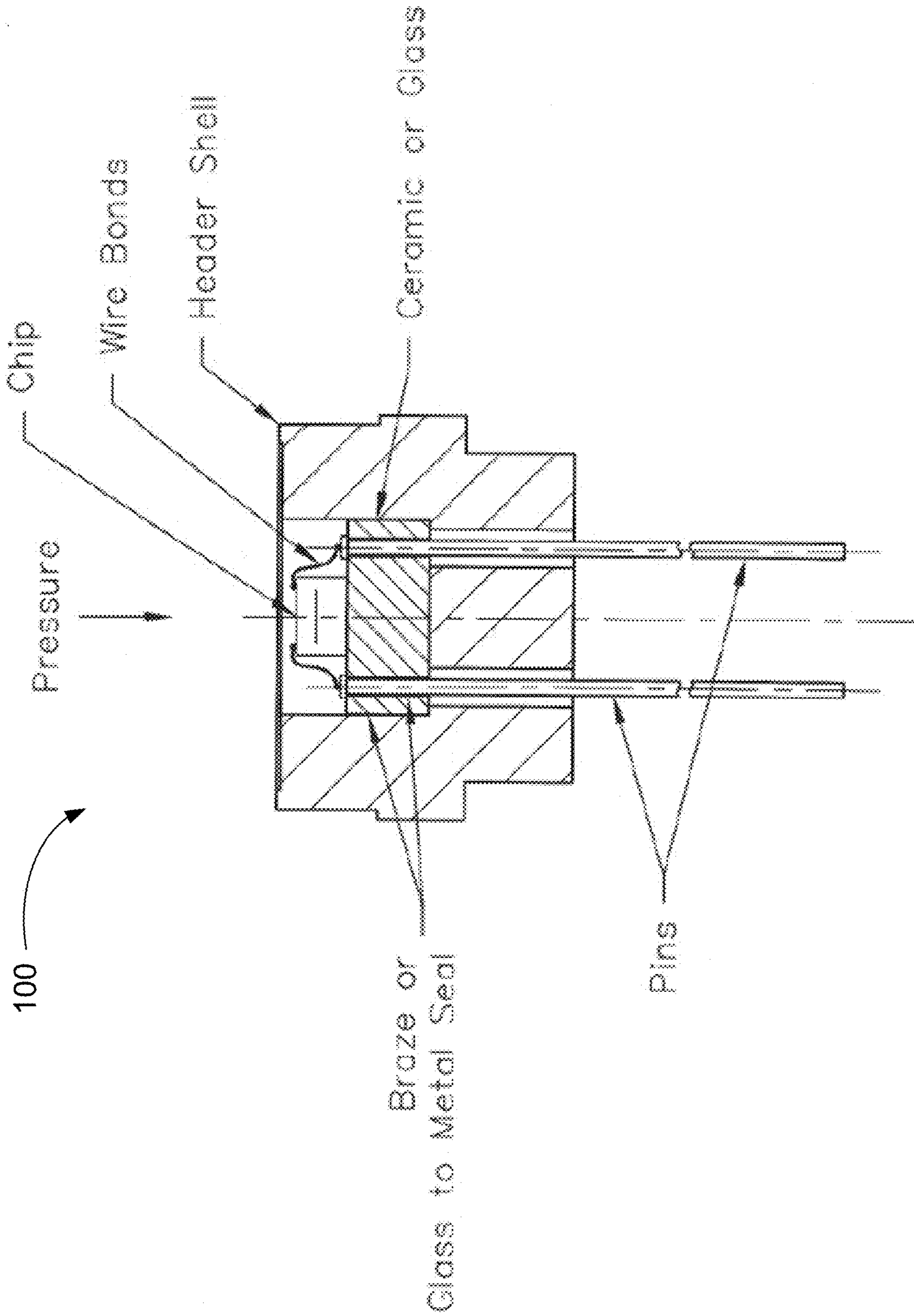


FIG. 1 (Prior Art)

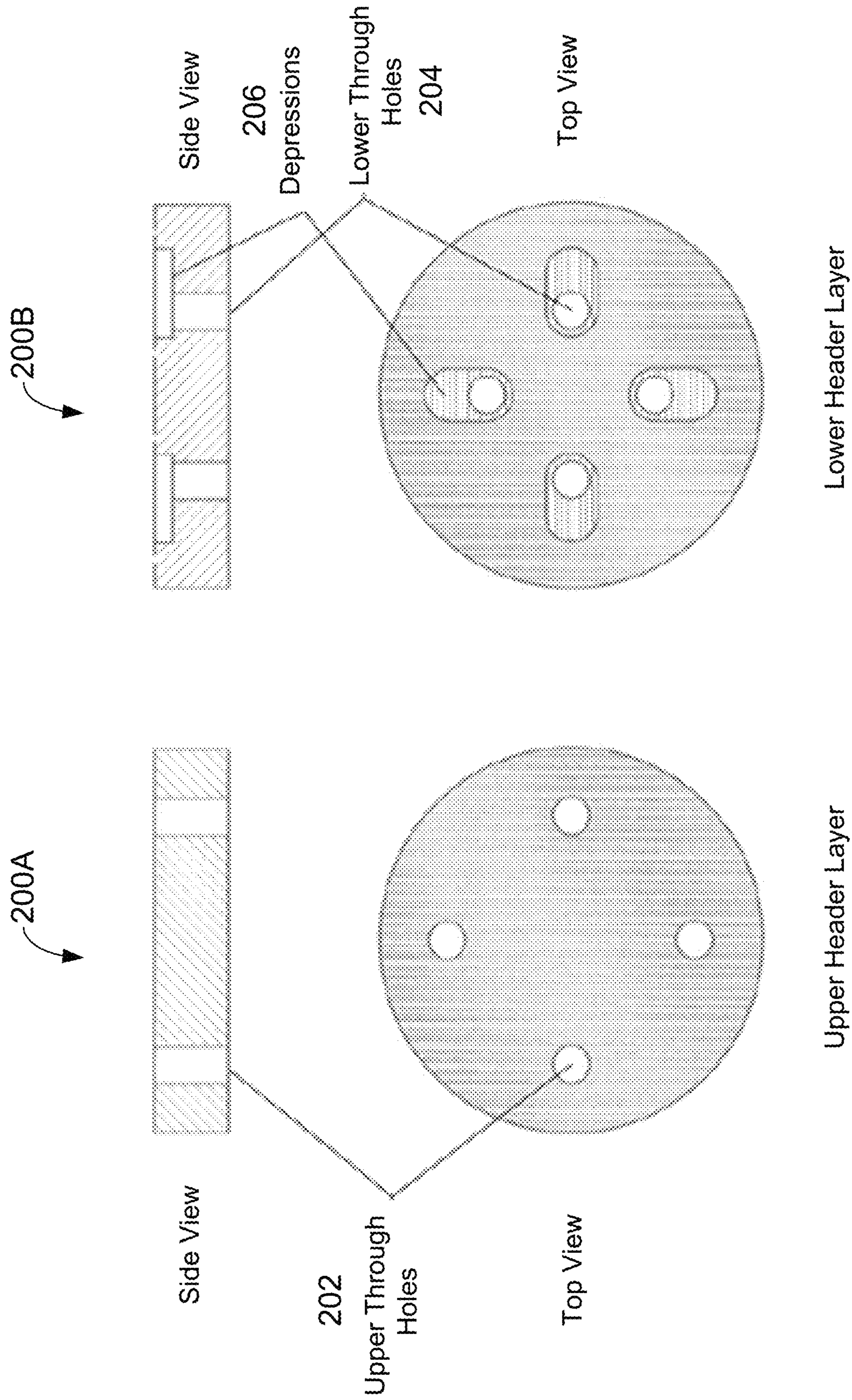


FIG. 2

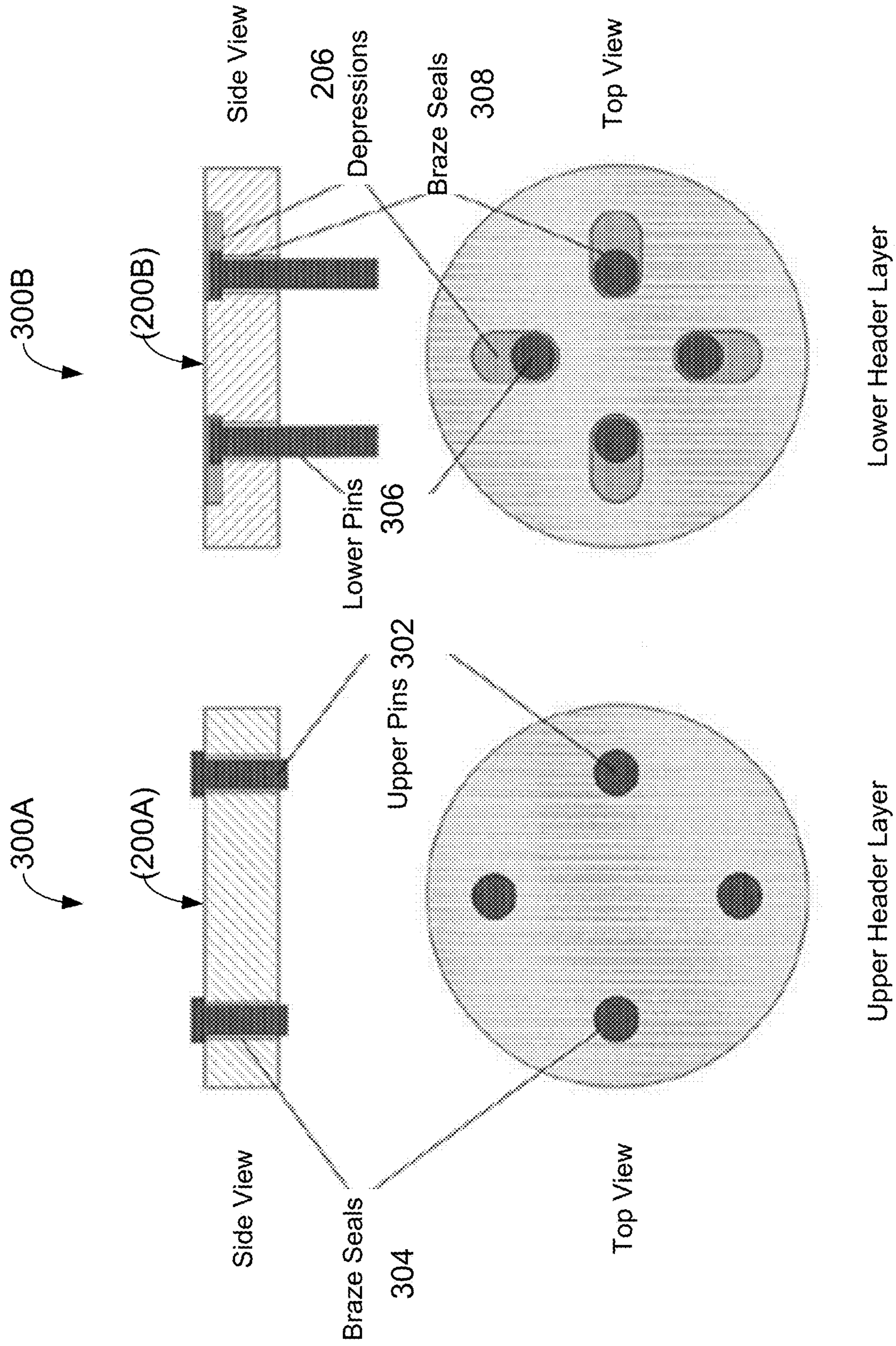


FIG. 3

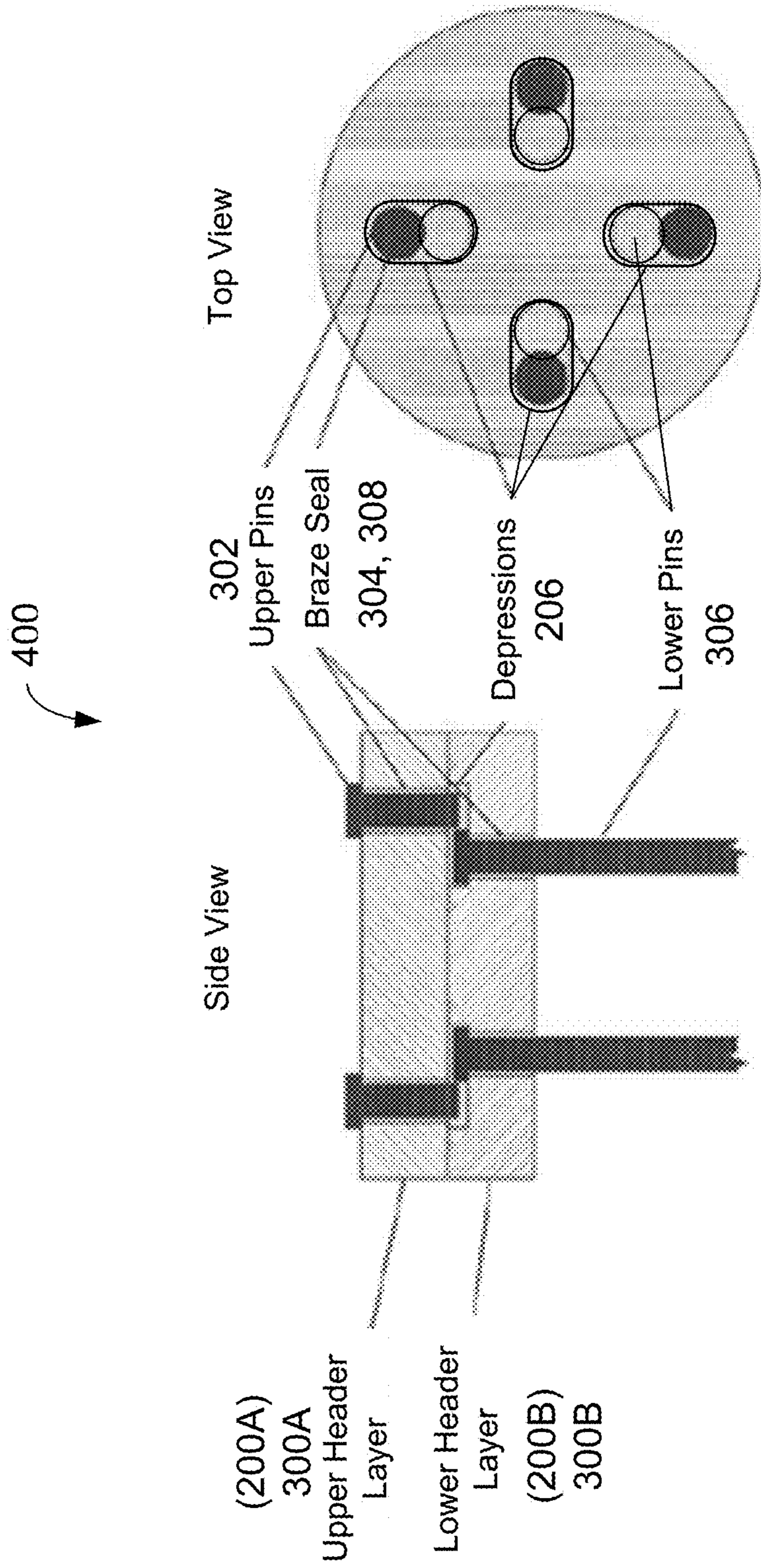


FIG. 4

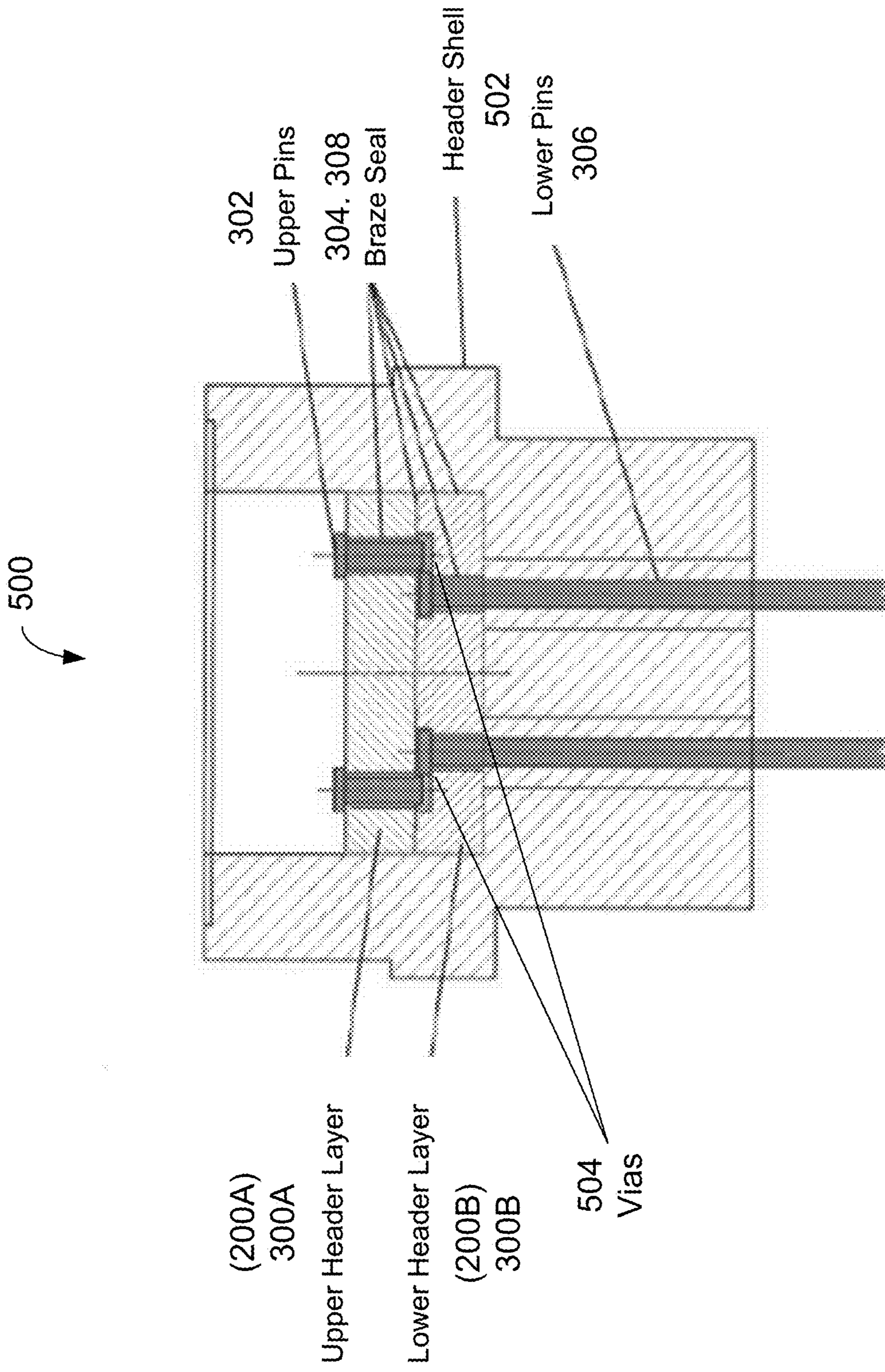


FIG. 5

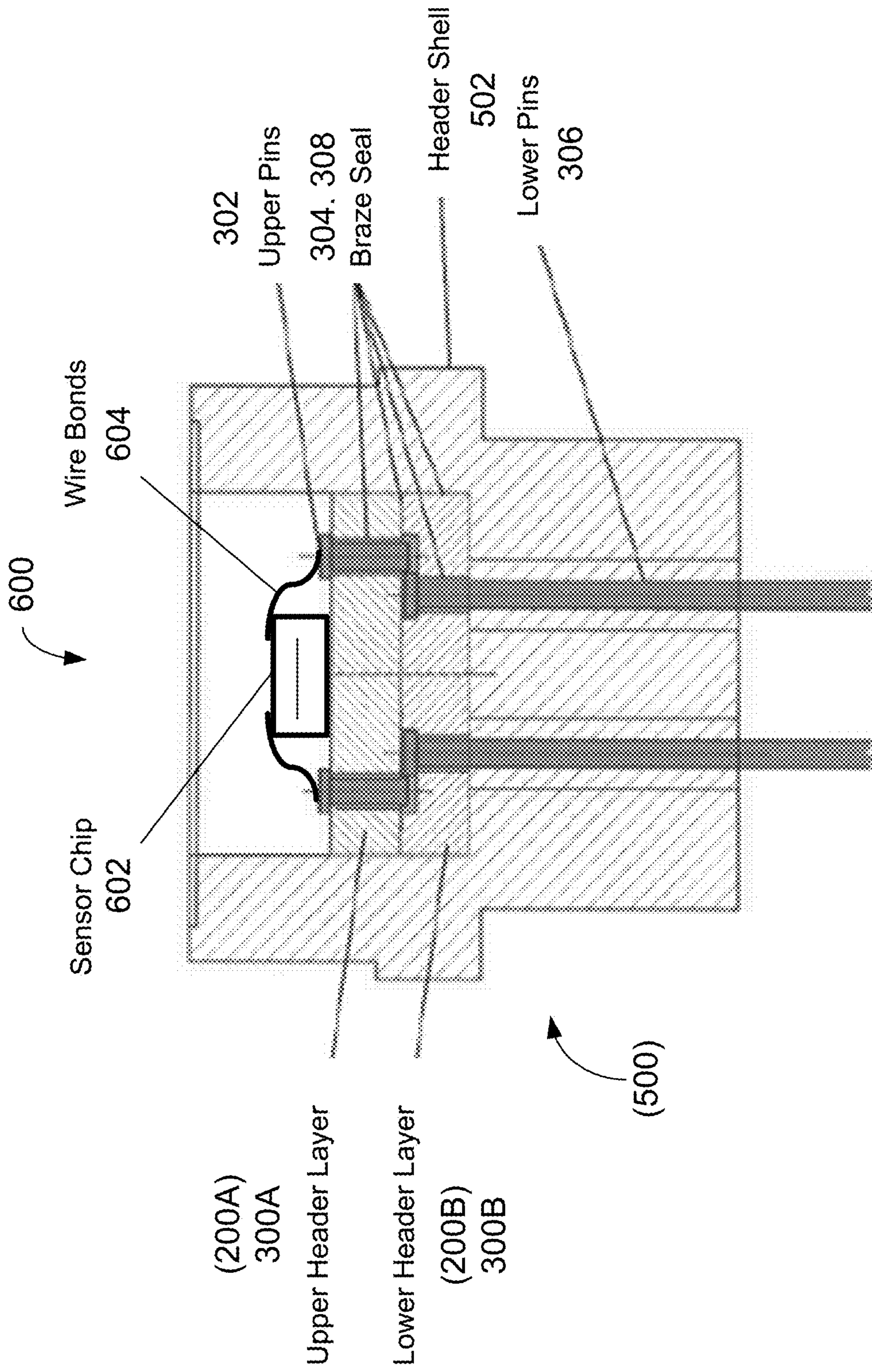


FIG. 6

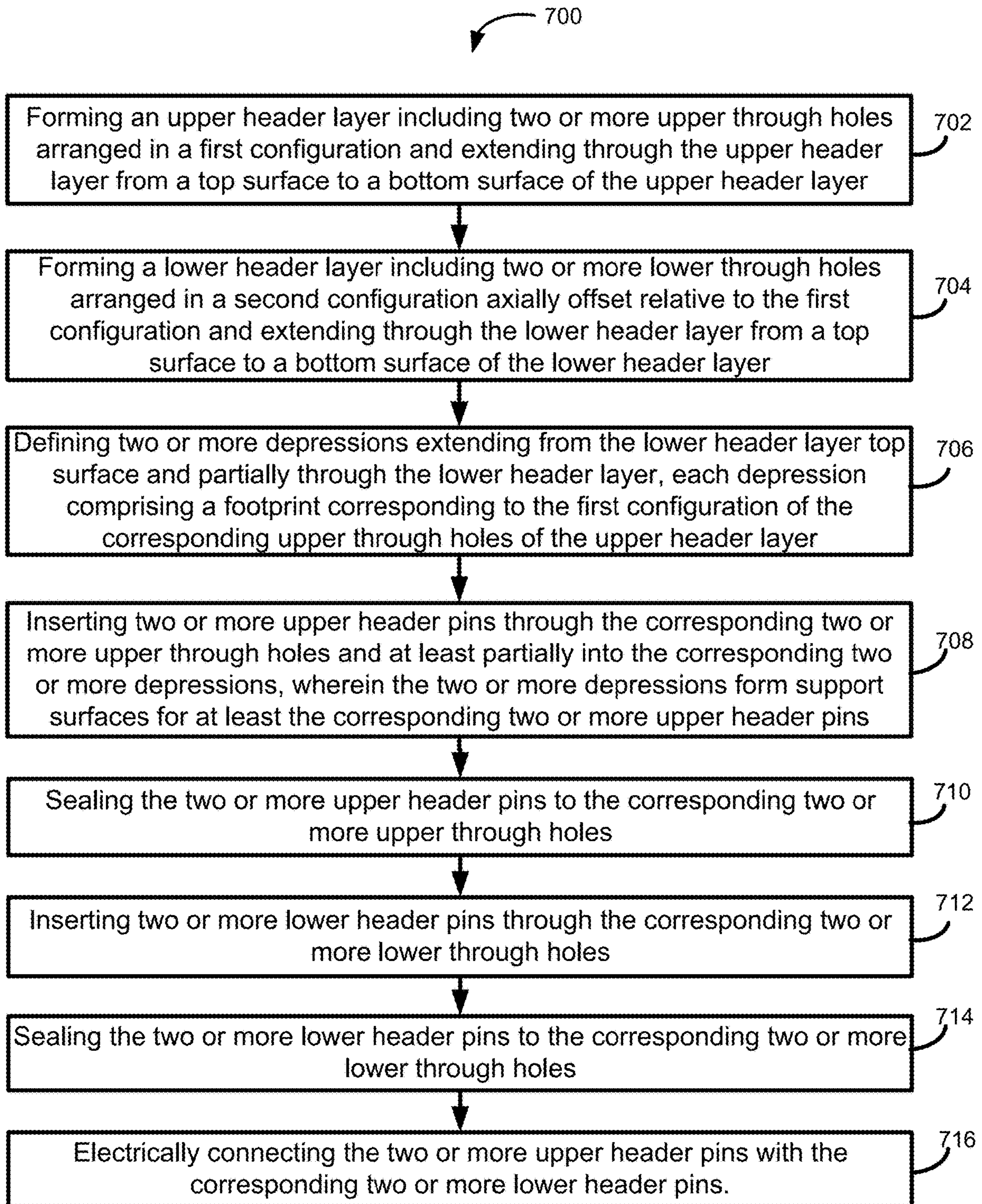


FIG. 7

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**SENSOR HEADER ASSEMBLY FOR
INCREASED RELIABILITY IN
HIGH-PRESSURE ENVIRONMENTS**

CROSS-REFERENCE TO RELATED
APPLICATIONS

This application is a continuation claiming priority under 35 U.S.C. § 120 to U.S. patent application Ser. No. 17/034,533, filed 28 Sep. 2020, and published as U.S. Patent Application Publication No. US20210010891 on 14 Jan. 2021, which is a continuation of U.S. patent application Ser. No. 16/205,836, filed 30 Nov. 2018, and issued as U.S. Pat. No. 10,788,386 on 29 Sep. 2020, the contents of which are incorporated herein by reference as if fully set forth.

FIELD

The disclosed technology relates to sensor device packaging and electrical interconnections suitable for extreme high-pressure operability, and in particular, to sensor header construction and techniques utilizing header layers configured to provide support for the electrical interconnections.

BACKGROUND

Traditional high-pressure sensor headers are typically constructed utilizing glass to metal seals and/or ceramic to metal brazing to secure and seal electrical interconnection pins to a header shell. For example, FIG. 1 depicts a prior art sensor assembly having a high-pressure sensing element (chip) mounted on the header and electrically interconnected to the header pins. As pressure is applied to the sensing element, a pressure signal is generated and communicated to an external circuit, for example, via the header pins.

The materials in these traditional header designs are typically selected to withstand high pressure. However, both the glass-to-metal sealing and the brazing technologies have limitations in the pressure and/or stress levels that they can withstand. For example, when such sensor assemblies are exposed to extreme high-pressures, the header pins can dislodge, move out of place, create open circuits, etc., and decrease the reliability of the sensor. Increasing the sealing surface area or introducing tapered holes to accept the header pins for either brazing or glass-to-metal sealing can only marginally help the seals withstand higher pressures.

A need exists for sensor header systems and methods capable of reliable operation in high-pressure environments.

BRIEF SUMMARY

Certain example implementations of the disclosed technology may include a sensor header configured for reliable operation in high-pressure environments.

In one example implementation, a sensor header assembly is provided that includes: an upper header layer having two or more upper through holes arranged in a first configuration and extending through the upper header layer from a top surface to a bottom surface of the upper header layer; a lower header layer having two or more lower through holes arranged in a second configuration axially offset relative to the first configuration and extending through the lower header layer from a top surface to a bottom surface of the lower header layer; two or more depressions extending from the lower header layer top surface and partially through the lower header layer, each depression defining a footprint corresponding to the first configuration of the corresponding

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upper through holes of the upper header layer; two or more upper header pins extending through the corresponding two or more upper through holes and at least partially into the corresponding two or more depressions; and two or more lower header pins extending through the corresponding two or more lower through holes and in electrical communication with the corresponding two or more upper header pins. The two or more depressions form support surfaces for at least the corresponding two or more upper header pins.

In another example implementation, a method is provided that includes: forming an upper header layer including two or more upper through holes arranged in a first configuration and extending through the upper header layer from a top surface to a bottom surface of the upper header layer; forming a lower header layer including two or more lower through holes arranged in a second configuration axially offset relative to the first configuration and extending through the lower header layer from a top surface to a bottom surface of the lower header layer; defining two or more depressions extending from the lower header layer top surface and partially through the lower header layer, each depression comprising a footprint corresponding to the first configuration of the corresponding upper through holes of the upper header layer; inserting two or more upper header pins through the corresponding two or more upper through holes and at least partially into the corresponding two or more depressions, wherein the two or more depressions form support surfaces for at least the corresponding two or more upper header pins; sealing the two or more upper header pins to the corresponding two or more upper through holes; inserting two or more lower header pins through the corresponding two or more lower through holes; sealing the two or more lower header pins to the corresponding two or more lower through holes; and electrically connecting the two or more upper header pins with the corresponding two or more lower header pins.

In another example implementation, a sensor assembly is provided that includes: a header assembly; a header shell surrounding and sealed to at least a portion of the header assembly; and a sensor chip. The header assembly includes: an upper header layer having two or more upper through holes arranged in a first configuration and extending through the upper header layer from a top surface to a bottom surface of the upper header layer; a lower header layer having two or more lower through holes arranged in a second configuration axially offset relative to the first configuration and extending through the lower header layer from a top surface to a bottom surface of the lower header layer; two or more depressions extending from the lower header layer top surface and partially through the lower header layer, each depression defining a footprint corresponding to the first configuration of the corresponding upper through holes of the upper header layer; two or more upper header pins extending through the corresponding two or more upper through holes and at least partially into the corresponding two or more depressions; and two or more lower header pins extending through the corresponding two or more lower through holes and in electrical communication with the corresponding two or more upper header pins. The two or more depressions form support surfaces for at least the corresponding two or more upper header pins. The sensor device is configured for increased reliability when used in high-pressure environments.

Other implementations, features, and aspects of the disclosed technology are described in detail herein and are considered a part of the claimed disclosed technology. Other implementations, features, and aspects can be understood

with reference to the following detailed description, accompanying drawings, and claims.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 depicts a cross-sectional side view of a prior art pressure sensor device 100.

FIG. 2 depicts example cross-sectional side views and top views of an upper ceramic layer 200A and a lower ceramic layer 200B, according to an example implementation of the disclosed technology.

FIG. 3 depicts example cross-sectional side views and top views of an upper ceramic layer 200A and a lower ceramic layer 200B, as shown in FIG. 2, with upper pins 302 and lower pins 306 inserted into the associated through holes, according to an example implementation of the disclosed technology.

FIG. 4 depicts an example cross-sectional side view and top view of a layered assembly 400 in which the upper ceramic layer sub assembly 300A is stacked on the lower ceramic layer sub assembly 300B with upper pins 302 offset from the lower pins 306 and supported by at least a portion of the lower ceramic layer 200B.

FIG. 5 depicts an example cross-sectional side view of a sensor housing assembly 500 including a header shell 502 according to an example implementation of the disclosed technology, in which the upper ceramic layer sub assembly 300A is stacked on the lower ceramic layer sub assembly 300B with upper pins 302 offset from and in electrical communication with the lower pins 306.

FIG. 6 depicts an example cross-sectional side view of a sensor assembly 600 (including the sensor housing assembly 500 as shown in FIG. 5) and an installed sensor chip 602.

FIG. 7 is a flow diagram of an assembly method 700, according to an example implementation of the disclosed technology.

DETAILED DESCRIPTION

The disclosed technology includes devices and techniques for providing electronic device packaging and interconnections suitable for ultra-high-pressure operability. Certain example implementations of the disclosed technology may utilize two or more ceramic layers, each having through holes configured to accept respective header pins. In an example implementation, at least one of the ceramic layers includes through holes that are axially offset from corresponding through holes of an adjacent ceramic layer, such that a base is defined for supporting one or more header pins. As will be explained below, the disclosed technology provides a header structure that can improve a pressure sensor reliability, particularly when operating in extreme high-pressure environments.

FIG. 1 depicts a prior art sensor assembly having a high-pressure sensing element (chip) mounted on the header and electrically interconnected to substantially straight header pins. Certain aspects of the technology disclosed herein may provide pressure handling improvements over such prior art designs and will be explained below with reference to FIG. 2 through FIG. 7.

FIG. 2 depicts example cross-sectional side views and top views of an upper (or front) ceramic layer 200A and a lower ceramic layer 200B, according to an example implementation of the disclosed technology. As shown on the left half of FIG. 2, the upper ceramic layer 200A may include through holes 202 disposed in a first configuration. As shown on the right half of FIG. 2, the lower ceramic layer

200B may include through holes 204 disposed in a second configuration, for example, having an offset relative to the through holes 202 of the upper ceramic layer 200A.

According to an example implementation of the disclosed technology, and as depicted in FIG. 2, the lower ceramic layer 200B may include depressions 206, for example, surrounding the through holes 204, and extending only partially through the thickness of the lower ceramic layer 200B. The depressions 206 may have a footprint larger than the diameter of the through holes 204 such that a support shelf is defined adjacent to the through holes 204 of the lower ceramic layer 200B and aligned with the through holes 202 of the upper ceramic layer 200A. In certain example implementations, the upper ceramic layer 200A may be fabricated independently of the lower ceramic layer 200B.

FIG. 3 depicts example cross-sectional side views and top views of an upper ceramic layer 200A and a lower ceramic layer 200B, as shown in FIG. 2, with upper pins 302 and lower pins 306 inserted into the associated through holes. In an example implementation, the upper pins 302 may be sealed to the through holes of the upper ceramic layer 200A by a braze seal 304. In an example implementation, the upper pins 302 may protrude through the thickness of the upper ceramic layer 200A and into at least a portion of the corresponding depressions 206 of the lower ceramic layer 200B for making electrical connection with the lower pins 306 (as will be discussed below in FIG. 4). In an example implementation, the lower pins 306 may be sealed to the through holes of the lower ceramic layer 200B by a braze seal 308.

In certain example implementations, the upper pins 302 may be braze sealed 304 to the through holes of the upper ceramic layer 200A to produce an upper ceramic layer sub assembly 300A. Similarly, the lower pins 306 may be braze sealed 308 to the through holes of the lower ceramic layer 200B to produce a lower ceramic layer sub assembly 300B. In certain example implementations, the upper ceramic layer sub assembly 300A may be fabricated independently of the lower ceramic layer sub assembly 300B.

FIG. 4 depicts an example cross-sectional side view (left) and top view (right) of a layered assembly 400 in which the upper ceramic layer sub assembly 300A may be stacked on the lower ceramic layer sub assembly 300B with upper pins 302 axially offset from the lower pins 306. In accordance with certain example implementations of the disclosed technology, the upper pins 302 may be designed to be axially (or laterally) offset with respect to the lower pins 306 when the upper ceramic layer sub assembly 300A is stacked on the lower ceramic layer sub assembly 300B. As will be explained below with reference to FIG. 5, vias may be utilized within the depressions 206, for example, so that when the ceramic layers are assembled the pins for one ceramic layer terminate next to and are electrically connected with the corresponding pins of the next adjacent ceramic layer.

FIG. 5 depicts an example cross-sectional side view of a sensor housing assembly 500 including a header shell 502, according to an example implementation of the disclosed technology. In certain example implementations, vias 504 (such as metalized interconnecting channels) may be utilized to join and electrically connect the upper pins 302 and the lower pins 306. In certain example implementations, the vias 504 may be disposed within the depression area (for example, in the depressions 206 as shown in FIGS. 2-4). In accordance with certain example implementations of the disclosed technology, at least a portion of the upper pins 302

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may be supported by at least a portion of the vias **504** and/or the lower ceramic layer **200B** corresponding to the area of the depressions **206**.

In accordance with certain example implementations of the disclosed technology, the joining surface of the two ceramic layers **200A** and **200B** may be fabricated in such a way so that metalized vias **504** physically interlock and electrically connect the pins from one ceramic to the next. This approach enables the upper pins **302**, which may be exposed to the pressure media, to be supported by both the braze seals **304** and **308** as well as the underlying ceramic layer (i.e., the lower ceramic layer **200B**). In certain example implementations, the lower pins **306** protruding from the lower ceramic layer **200B** may be at least partially isolated from high-pressure exposure, which may be transferred through the upper pins **302** and terminated/supported by a portion of the lower ceramic layer **200B**. This approach may further enable fabrication of ultra-high-pressure headers using traditional materials without experiencing the electrical/mechanical pin failure associated with traditional sealing technologies.

FIG. **6** depicts an example cross-sectional side view of a sensor assembly **600** (including the sensor housing assembly **500** as shown in FIG. **5**) with an installed sensor chip **602** electrically connected to the upper pins **302** by wire bonds **604**. In accordance with certain example implementations of the disclosed technology, a similar approach as discussed above with respect to FIGS. **2-5** may be utilized to house a sensor chip having contact electrodes configured to interconnect directly with the upper pins **302** (not shown) without the wire bonds **604**.

FIG. **7** is a flow diagram of an assembly method **700**, according to an example implementation of the disclosed technology. In block **702**, the method **700** includes forming an upper header layer including two or more upper through holes arranged in a first configuration and extending through the upper header layer from a top surface to a bottom surface of the upper header layer. In block **704**, the method **700** includes forming a lower header layer including two or more lower through holes arranged in a second configuration axially offset relative to the first configuration and extending through the lower header layer from a top surface to a bottom surface of the lower header layer. In block **706**, the method **700** includes defining two or more depressions extending from the lower header layer top surface and partially through the lower header layer, each depression comprising a footprint corresponding to the first configuration of the corresponding upper through holes of the upper header layer. In block **708**, the method **700** includes inserting two or more upper header pins through the corresponding two or more upper through holes and at least partially into the corresponding two or more depressions, wherein the two or more depressions form support surfaces for at least the corresponding two or more upper header pins. In block **710**, the method **700** includes sealing the two or more upper header pins to the corresponding two or more upper through holes. In block **712**, the method **700** includes inserting two or more lower header pins through the corresponding two or more lower through holes. In block **714**, the method **700** sealing the two or more lower header pins to the corresponding two or more lower through holes. In block **716**, the method **700** includes electrically connecting the two or more upper header pins with the corresponding two or more lower header pins.

In certain example implementations, electrically connecting the two or more upper header pins with the correspond-

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ing two or more lower header pins includes disposing two or more electrically conductive vias in the corresponding two or more depressions.

Certain example implementations of the disclosed technology can further include mounting a sensor chip to the top surface of the upper header layer, wherein the sensor chip comprises one or more sensor contact pads. Certain example implementations of the disclosed technology include attaching a first end of one or more wire bond interconnections to the respective one or more sensor contact pads. Certain example implementations of the disclosed technology include attaching a second end of the one or more wire bond interconnections to the respective one or more of the upper pins. Certain example implementations of the disclosed technology can include sealing a header shell to at least a portion of the upper header layer.

According to an example implementation of the disclosed technology, a sensor header assembly is provided that includes: an upper header layer having two or more upper through holes arranged in a first configuration and extending through the upper header layer from a top surface to a bottom surface of the upper header layer; a lower header layer having two or more lower through holes arranged in a second configuration axially offset relative to the first configuration and extending through the lower header layer from a top surface to a bottom surface of the lower header layer; two or more depressions extending from the lower header layer top surface and partially through the lower header layer, each depression defining a footprint corresponding to the first configuration of the corresponding upper through holes of the upper header layer; two or more upper header pins extending through the corresponding two or more upper through holes and at least partially into the corresponding two or more depressions; and two or more lower header pins extending through the corresponding two or more lower through holes and in electrical communication with the corresponding two or more upper header pins. The two or more depressions form support surfaces for at least the corresponding two or more upper header pins.

Certain example implementations of the disclosed technology can include two or more electrically conductive vias disposed in the corresponding two or more depressions and configured to electrically couple the two or more upper header pins with the corresponding two or more lower header pins.

In certain implementations, the upper and lower header layers comprise a ceramic material.

In certain example implementations, the upper header pins are braze sealed to at least a portion of the corresponding upper through holes, and the lower header pins are braze sealed to at least a portion of the corresponding lower through holes.

In certain example implementations, the upper header pins include heads having a diameter larger than the diameter of the upper through holes.

In certain example implementations, at least a top portion of the upper header pins are configured as connection pads for electrical connection to at least one component.

Certain example implementations of the disclosed technology can include one or more wire bond interconnections electrically connecting the connection pads with the at least one component.

In certain example implementations, the lower header pins have heads with a diameter larger than a diameter of the lower through holes.

In accordance with certain example implementations of the disclosed technology, the depressions can include a

footprint around the lower through holes having a diameter greater than a diameter of the lower pin heads and a depth such that a top portion of the lower pin heads do not extend above the top surface of the lower header layer.

Certain example implementations of the disclosed technology can include a header shell sealed to at least a portion of the upper header layer, the lower header layer, and the lower pins.

Certain example implementations described herein may be utilized to address the need for enhancing the reliability of sensor devices, particularly for use in high-pressure environments. Certain example implementations provide one or more structures support header pins for increased stability under high-pressure environments. Furthermore, in certain example implementations, the disclosed technology may further prevent or reduce degradation of the associated enclosed internal sensor components.

It is important to recognize that it is impractical to describe every conceivable combination of components or methodologies for purposes of describing the claimed subject matter. However, a person having ordinary skill in the art will recognize that many further combinations and permutations of the subject technology are possible. Accordingly, the claimed subject matter is intended to cover all such alterations, modifications, and variations that are within the spirit and scope of the claimed subject matter.

Throughout the specification and the claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The terms “connect,” “connecting,” and “connected” mean that one function, feature, structure, or characteristic is directly joined to or in communication with another function, feature, structure, or characteristic. The term “couple,” “coupling,” and “coupled” mean that one function, feature, structure, or characteristic is directly or indirectly joined to or in communication with another function, feature, structure, or characteristic. Relational terms such as “first” and “second,” and the like may be used solely to distinguish one entity or action from another entity or action without necessarily requiring or implying any actual such relationship or order between such entities or actions. The term “or” is intended to mean an inclusive “or.” Further, the terms “a,” “an,” and “the” are intended to mean one or more unless specified otherwise or clear from the context to be directed to a singular form. The term “include” and its various forms are intended to mean including but not limited to. The terms “substantially,” “essentially,” “approximately,” “about” or any other version thereof, are defined as being close to as understood by one of ordinary skill in the art, and in one non-limiting embodiment the term is defined to be within 10%, in another embodiment within 5%, in another embodiment within 1% and in another embodiment within 0.5%. A device or structure that is “configured” in a certain way is configured in at least that way but may also be configured in ways that are not listed.

As disclosed herein, numerous specific details are set forth. However, it is to be understood that embodiments of the disclosed technology may be practiced without these specific details. References to “one embodiment,” “an embodiment,” “example embodiment,” “various embodiments,” and other like terms indicate that the embodiments of the disclosed technology so described may include a particular function, feature, structure, or characteristic, but not every embodiment necessarily includes the particular function, feature, structure, or characteristic. Further, repeated use of the phrase “in one embodiment” does not necessarily refer to the same embodiment, although it may.

Although this disclosure describes specific examples, embodiments, and the like, certain modifications and changes may be made without departing from the scope of the disclosed technology, as set forth in the claims below.

For example, although the example methods, devices, and systems, described herein are in conjunction with a pressure transducer or a sensor, the skilled artisan will readily recognize that the example methods, devices or systems may be used in other methods, devices or systems and may be configured to correspond to such other example methods, devices or systems as needed. Further, while at least one example, embodiment, or the like has been presented in the detailed description, many variations exist. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present disclosure. Any benefits, advantages, or solutions to problems that are described herein with regard to specific embodiments or examples are not intended to be construed as a critical, required, or essential feature or element of any or all of the claims.

What is claimed is:

1. A header assembly, comprising:

an upper header layer;

a lower header layer;

two or more upper header pins extending through corresponding two or more upper through holes of the upper header layer;

two or more lower header pins extending through corresponding two or more lower through holes of the lower header layer; and

metalized interconnecting channels configured to join and electrically connect the upper header pins and the lower header pins.

2. The header assembly of claim 1, further comprising two or more depressions extending from a top surface of the lower header layer and partially through the lower header layer, each of the two or more depressions defining a footprint configured to accept bottom-end portions of the upper header pins and head portions of the lower header pins.

3. The header assembly of claim 2, wherein at least a portion of the footprint provides a support surface for the upper header pins such that the lower header pins are at least partially isolated from a pressure applied to the upper header pins.

4. The header assembly of claim 2, wherein the two or more depressions have a diameter greater than a diameter of the head portions of the lower header pins and a depth such that a top portion of the head portions of the lower header pins do not extend above the top surface of the lower header layer.

5. The header assembly of claim 2, wherein the metalized interconnecting channels are disposed within the corresponding two or more depressions and configured to electrically couple the two or more upper header pins with the corresponding two or more lower header pins.

6. The header assembly of claim 5, wherein the metalized interconnecting channels are configured to physically interlock and electrically connect the two or more upper header pins with the corresponding two or more lower header pins.

7. The header assembly of claim 1, wherein the lower header pins are at least partially isolated from a pressure applied to the upper header pins.

8. The header assembly of claim 1, wherein the two or more upper through holes of the upper header layer are

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arranged in a first configuration and extending through the upper header layer from a top surface to a bottom surface of the upper header layer.

9. The header assembly of claim 8, wherein the two or more lower through holes of the lower header layer are arranged in a second configuration axially offset relative to the first configuration and extending through the lower header layer from a top surface to a bottom surface of the lower header layer.

10. The header assembly of claim 1, wherein the upper and lower header layers comprise a ceramic material.

11. The header assembly of claim 1, wherein the upper header pins are brazed sealed to at least a portion of the corresponding upper through holes, and wherein the lower header pins are brazed sealed to at least a portion of the corresponding lower through holes.

12. The header assembly of claim 1, wherein the upper header pins comprise heads having a diameter larger than a diameter of the upper through holes.

13. The header assembly of claim 12, wherein at least a top portion of the upper header pins are configured as connection pads for electrical connection to at least one component.

14. The header assembly of claim 13, further comprising one or more wire bond interconnections electrically connecting the connection pads with the at least one component.

15. The header assembly of claim 1, further comprising a header shell sealed to at least a portion of the upper header layer, the lower header layer, and the lower header pins.

16. A method, comprising:

inserting two or more lower header pins through corresponding two or more lower through holes of a lower header layer;

inserting two or more upper header pins through corresponding two or more upper through holes of an upper header layer;

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stacking the upper header layer on the lower header layer; and

electrically connecting the two or more upper header pins with the corresponding two or more lower header pins.

17. The method of claim 16, further comprising sealing the two or more lower head pins to at least a portion of the through holes of the lower header layer to produce a lower header layer assembly; and

sealing the two or more upper head pins to at least a portion of the through holes of the upper header layer to produce an upper header layer assembly.

18. The method of claim 16, wherein the lower header pins comprise heads having a diameter larger than a diameter of the lower through holes; and wherein the lower header layer comprises two or more depressions extending from a top surface of the lower header layer and partially through the lower header layer, each of the two or more depressions defining a footprint configured to accept bottom-end portions of the upper header pins and the heads of the lower header pins.

19. The method of claim 16 wherein the two or more lower header pins are inserted through the corresponding two or more lower through holes of the lower header layer such that a top portion of the heads of the lower header pins do not extend above the top surface of the lower header layer.

20. The method of claim 16, further comprising disposing two or more electrically conductive vias in the corresponding two or more depressions, wherein the electrically conductive vias and depressions form support surfaces for at least the corresponding two or more upper header pins so that the lower header pins are at least partially isolated from a pressure applied to the upper header pins.

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