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Kim et al.

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(45) **Date of Patent: Aug. 22, 2023**

(54) **SEMICONDUCTOR DEVICE**

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(73) Assignee: **SAMSUNG ELECTRONICS CO., LTD.**, Suwon-si (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **17/546,690**

(22) Filed: **Dec. 9, 2021**

(65) **Prior Publication Data**

US 2022/0102498 A1 Mar. 31, 2022

Related U.S. Application Data

(63) Continuation of application No. 16/806,629, filed on Mar. 2, 2020, now Pat. No. 11,217,667.

(30) **Foreign Application Priority Data**

Jul. 23, 2019 (KR) 10-2019-0089217

(51) **Int. Cl.**
H01L 29/08 (2006.01)
H01L 29/78 (2006.01)
H01L 27/088 (2006.01)
H01L 29/06 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/0847*** (2013.01); ***H01L 27/0886*** (2013.01); ***H01L 29/0653*** (2013.01); ***H01L 29/0673*** (2013.01); ***H01L 29/785*** (2013.01); ***H01L 29/7853*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 29/0847; H01L 29/78696; H01L 27/0886; H01L 29/66795; H01L 21/823468; H01L 29/42392; H01L 29/0673; H01L 29/0653
See application file for complete search history.

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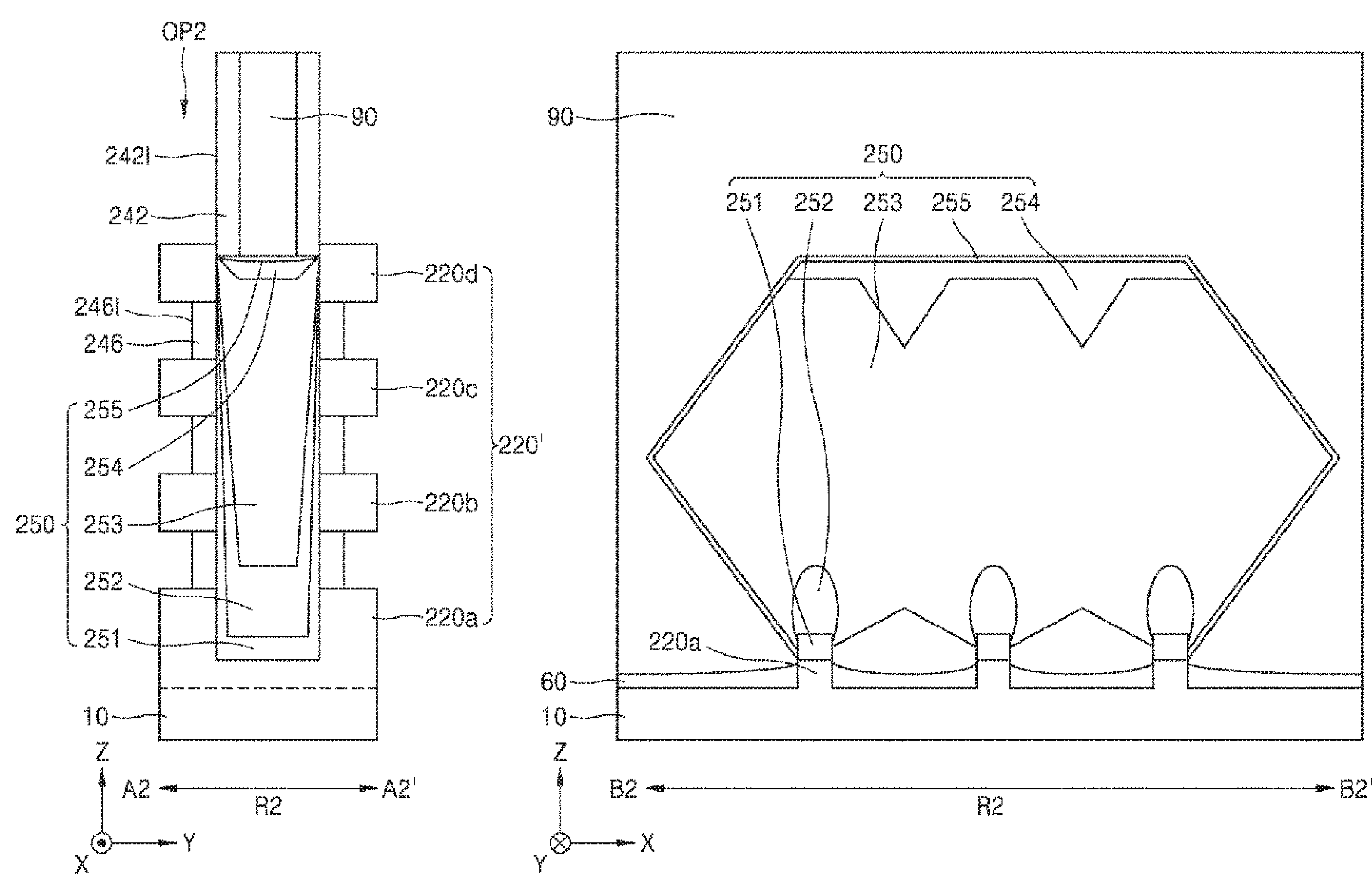
(Continued)

Primary Examiner — Changhyun Yi
(74) *Attorney, Agent, or Firm* — Sughrue Mion, PLLC

(57) **ABSTRACT**

A semiconductor device includes a substrate, a fin structure on the substrate, a gate structure on the fin structure, a gate spacer on at least on side surface of the gate structure, and a source/drain structure on the fin structure, wherein a topmost portion of a bottom surface of the gate spacer is lower than a topmost portion of a top surface of the fin structure, and a topmost portion of a top surface of the source/drain structure is lower than the topmost portion of the top surface of the fin structure.

21 Claims, 53 Drawing Sheets



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11,217,667	B2 *	1/2022	Kim H01L 21/823468
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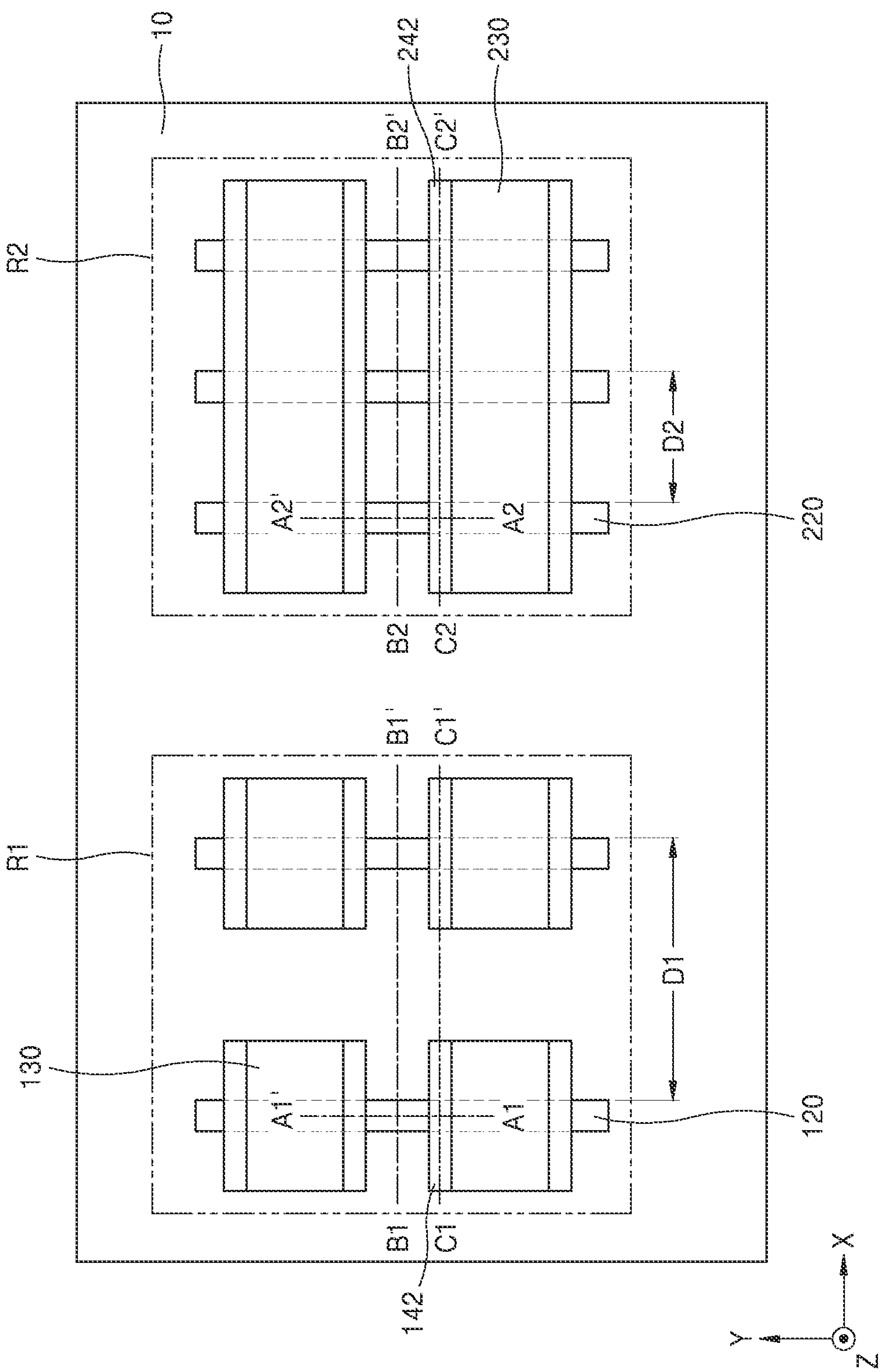
2019/0131181	A1 *	5/2019	Van Dal H01L 27/0886
2020/0105889	A1 *	4/2020	Liaw H01L 21/823418

* cited by examiner

FIG. 1A


10
242
230
B2'
C2'
R2
D2
A2'
A2
220
B2
C2
B1'
C1'
R1
130
D1
A1'
A1
120
B1
C1
142
X
Y
Z

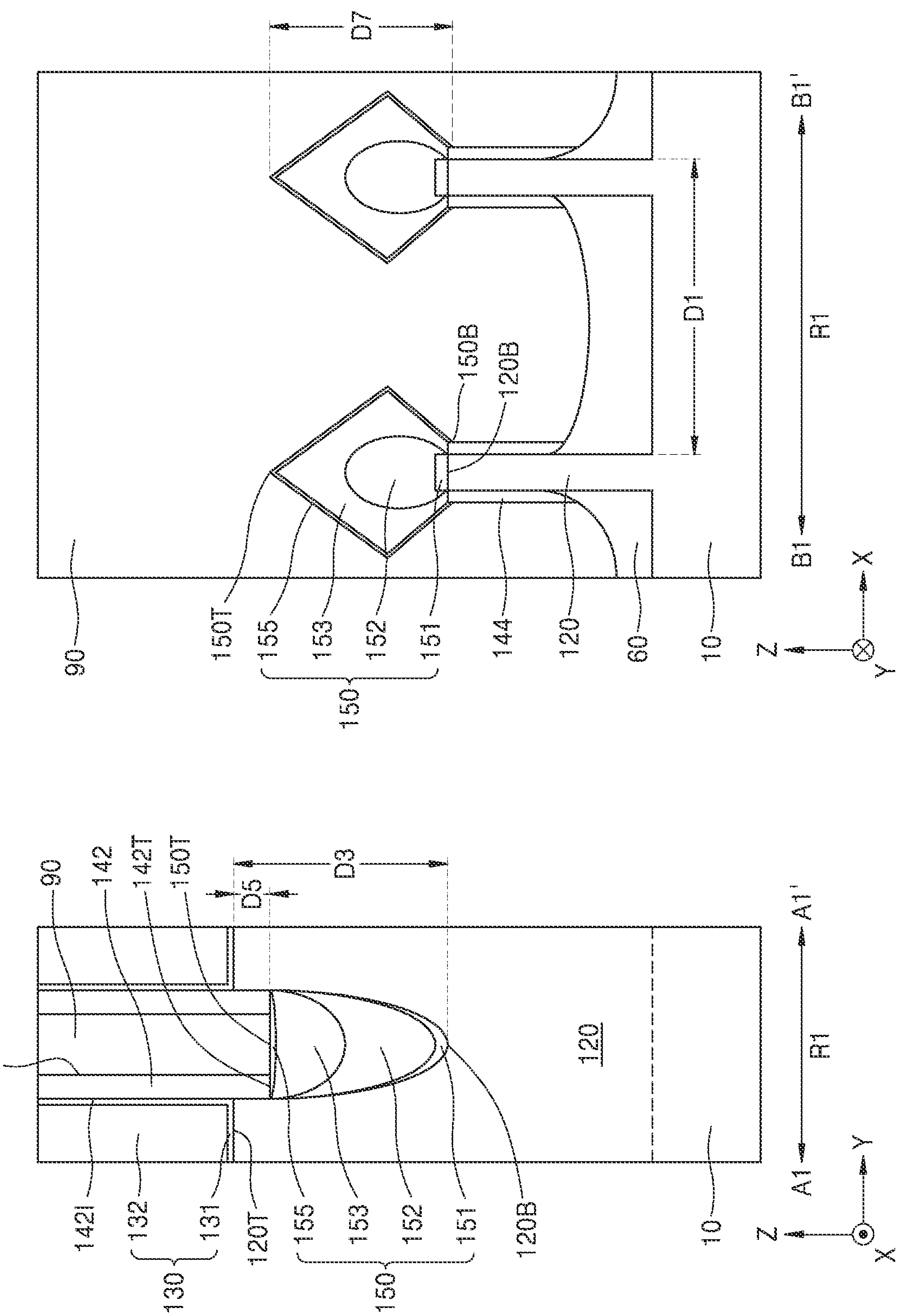

1000
D7
150B
120B
D1
R1
B1
B1'
X
Y
Z
90
150T
155
153
152
151
144
120
60
10
150
1420
142
142T
150T
D5
D3
120
A1
A1'
142I
132
131
120T
130
120B

FIG. 1B

FIG. 1C

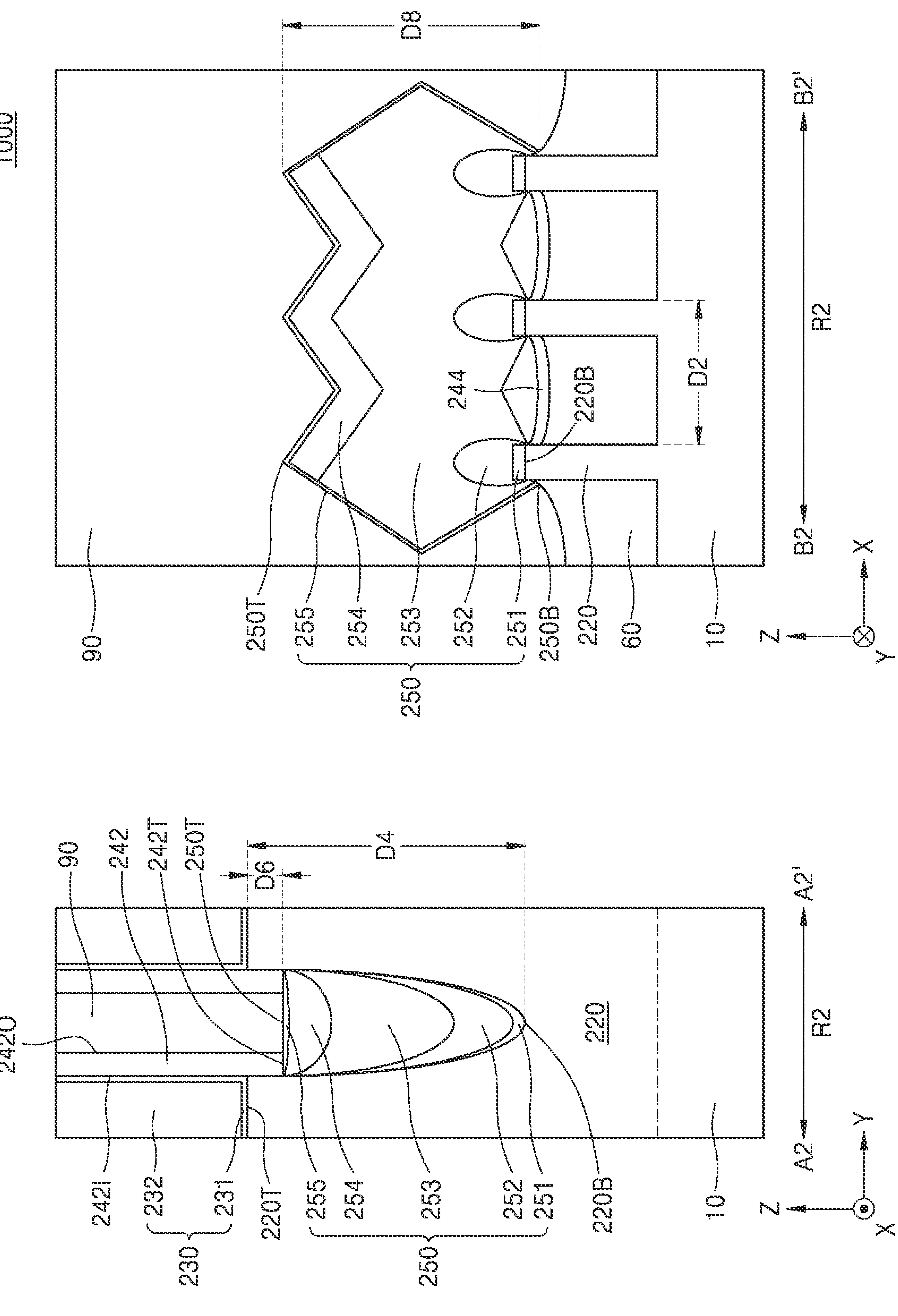

1000
D8
B2
B2'
R2
D2
244
220B
90
250T
255
254
253
252
251
250B
220
60
10
250
Z
X
Y
242O
242
242T
D6
D4
A2
A2'
242I
232
231
220T
230
Z
Y
X

FIG. 1D

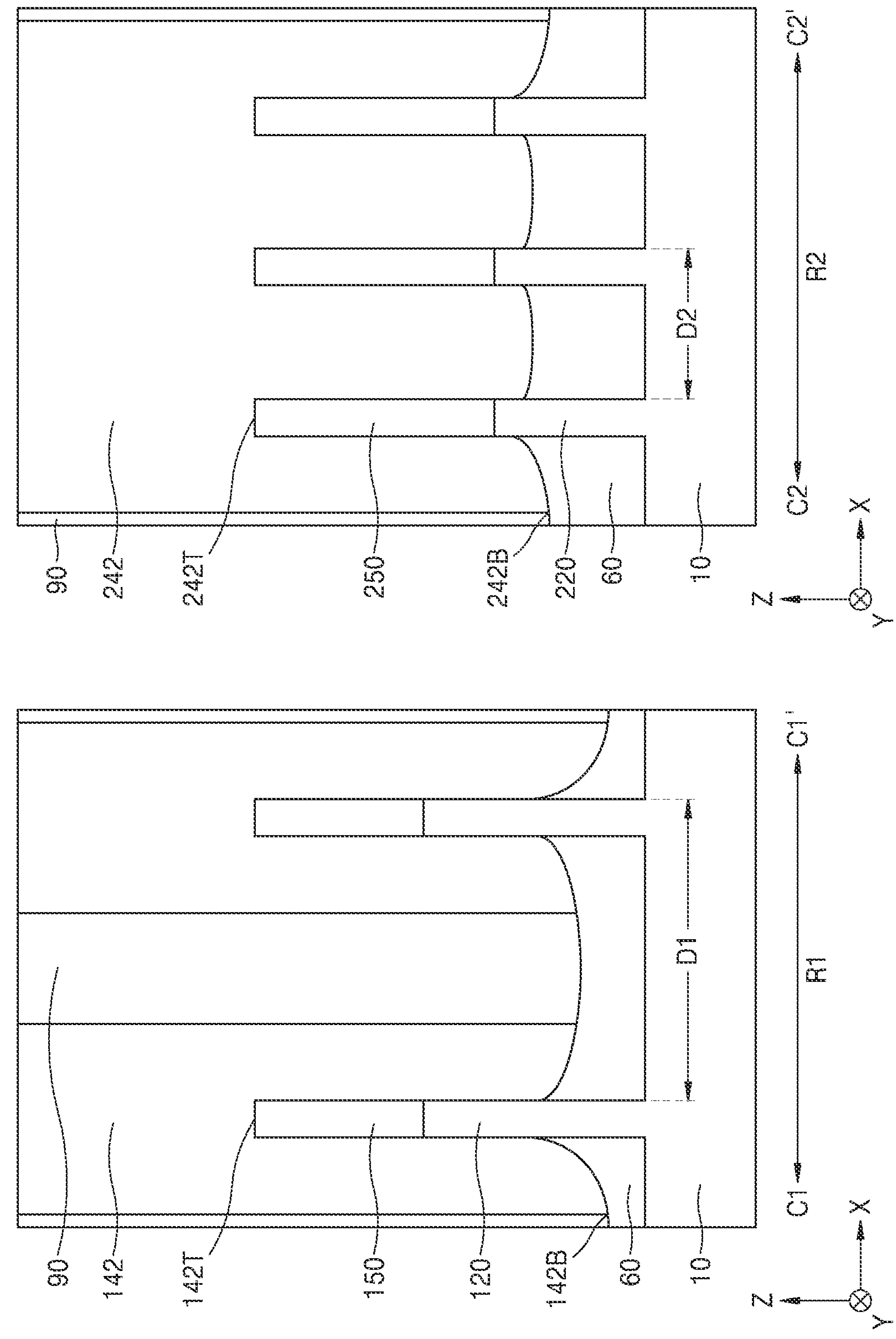

90
142
142T
150
120
142B
60
10
C1
C1'
D1
R1
Z
X
Y
90
242
242T
250
242B
220
60
10
C2
C2'
D2
R2
Z
X
Y

FIG. 2

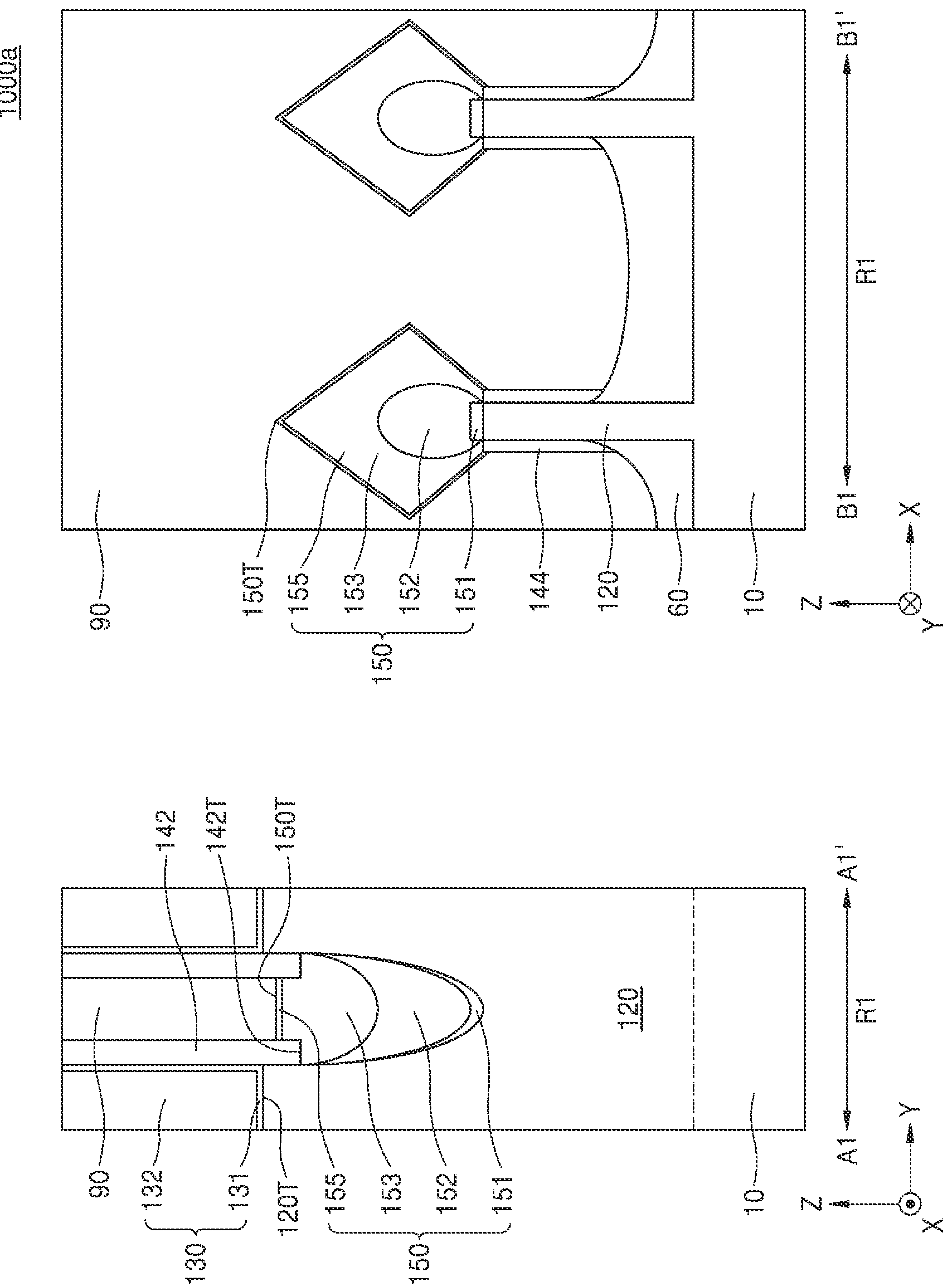

1000a
90
150T
155
153
152
151
150
144
120
60
10
B1
R1
B1'
Z
X
Y
132
131
130
120T
142
142T
A1
A1'

FIG. 3

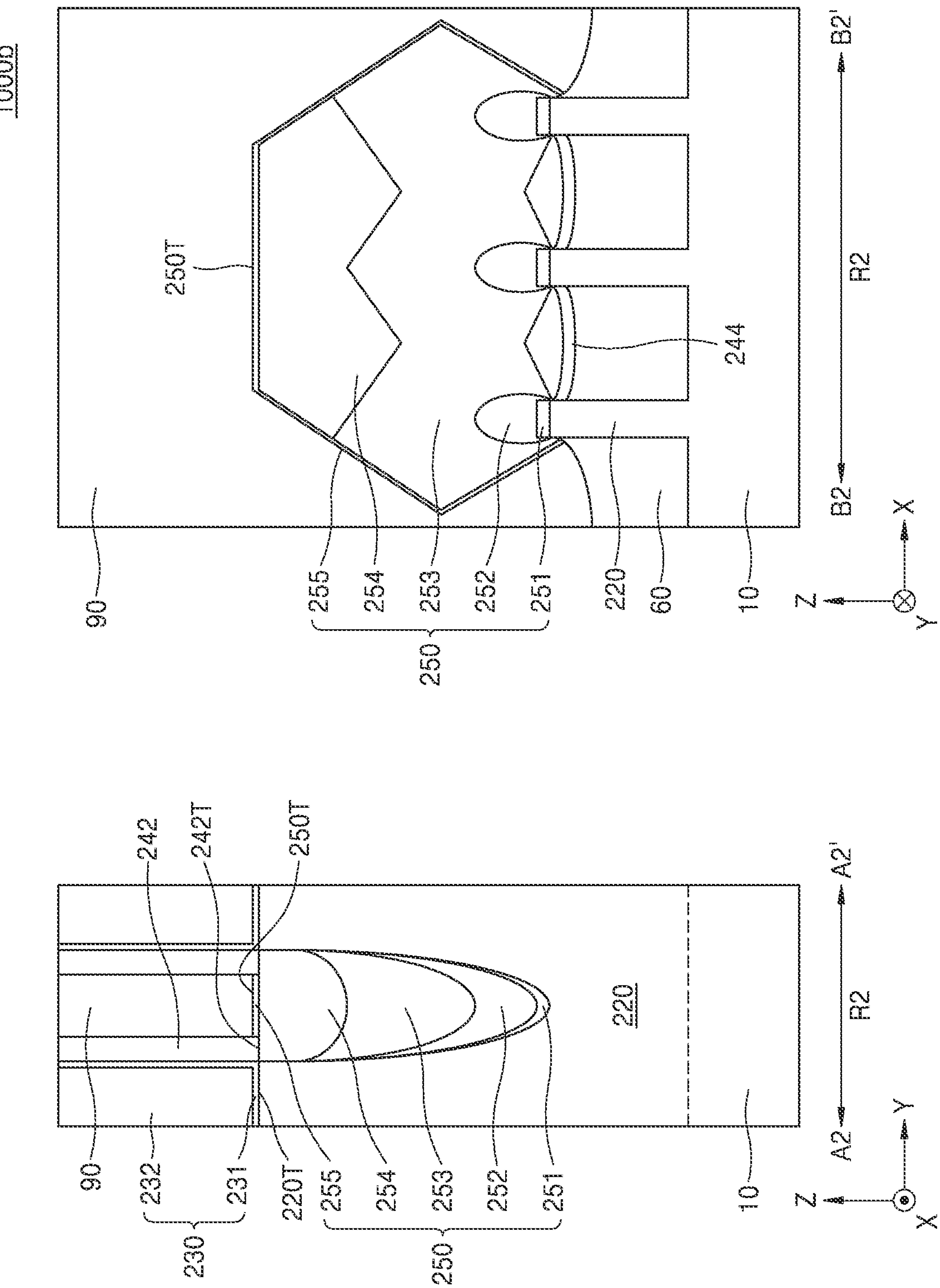

1000b
250T
244
90
255
254
253
252
251
250
220
60
10
B2
B2'
R2
Z
X
Y
242
242T
250T
220
90
232
231
230
220T
255
254
253
252
251
250
10
A2
A2'
R2
Z
Y
X

FIG. 4A

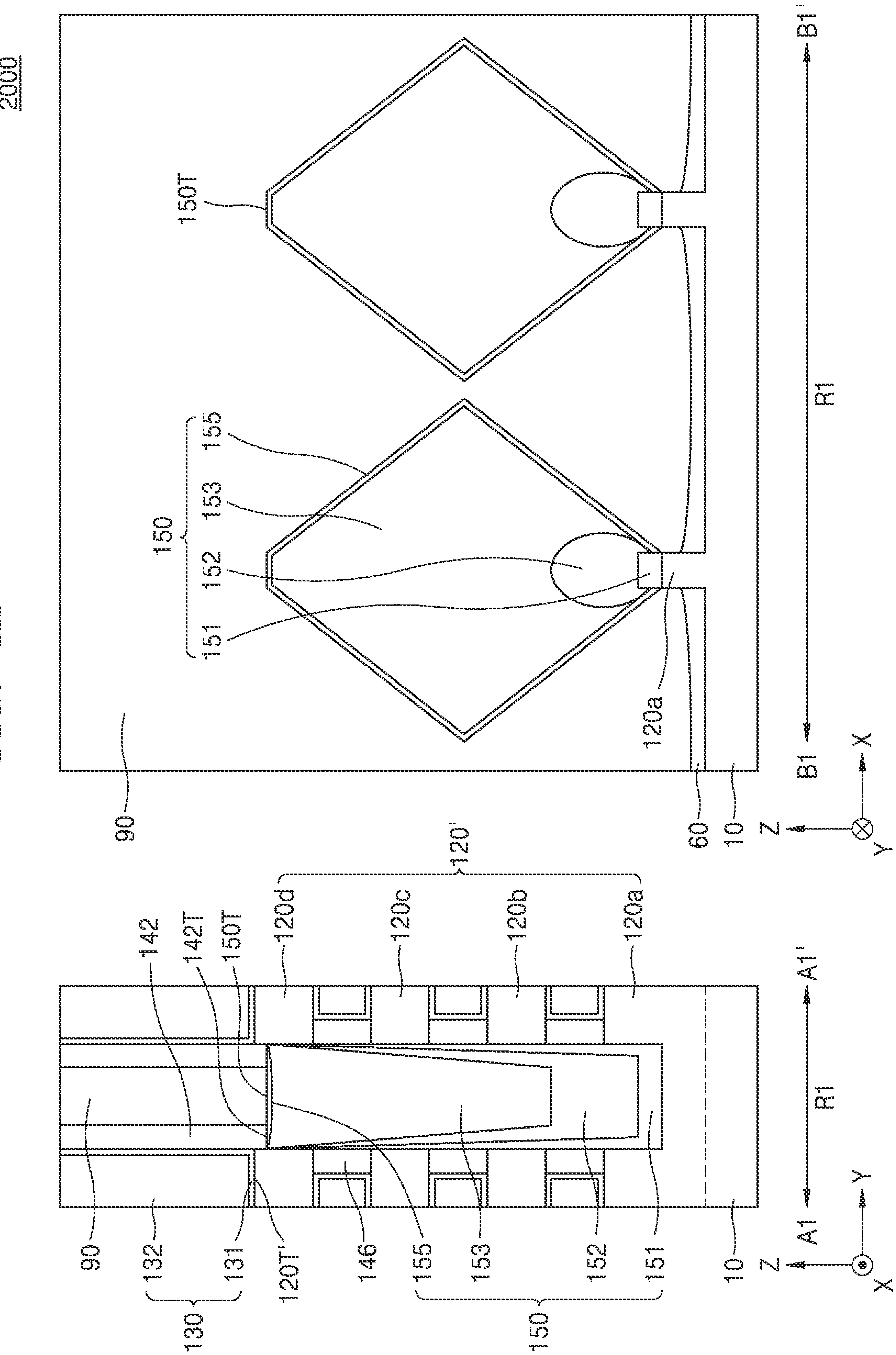

2000
150T
150
151
152
153
155
90
60
10
120a
B1
B1'
R1
Z
X
Y
120'
120d
120c
120b
142
142T
A1
A1'
130
132
131
120T'
146

FIG. 4B

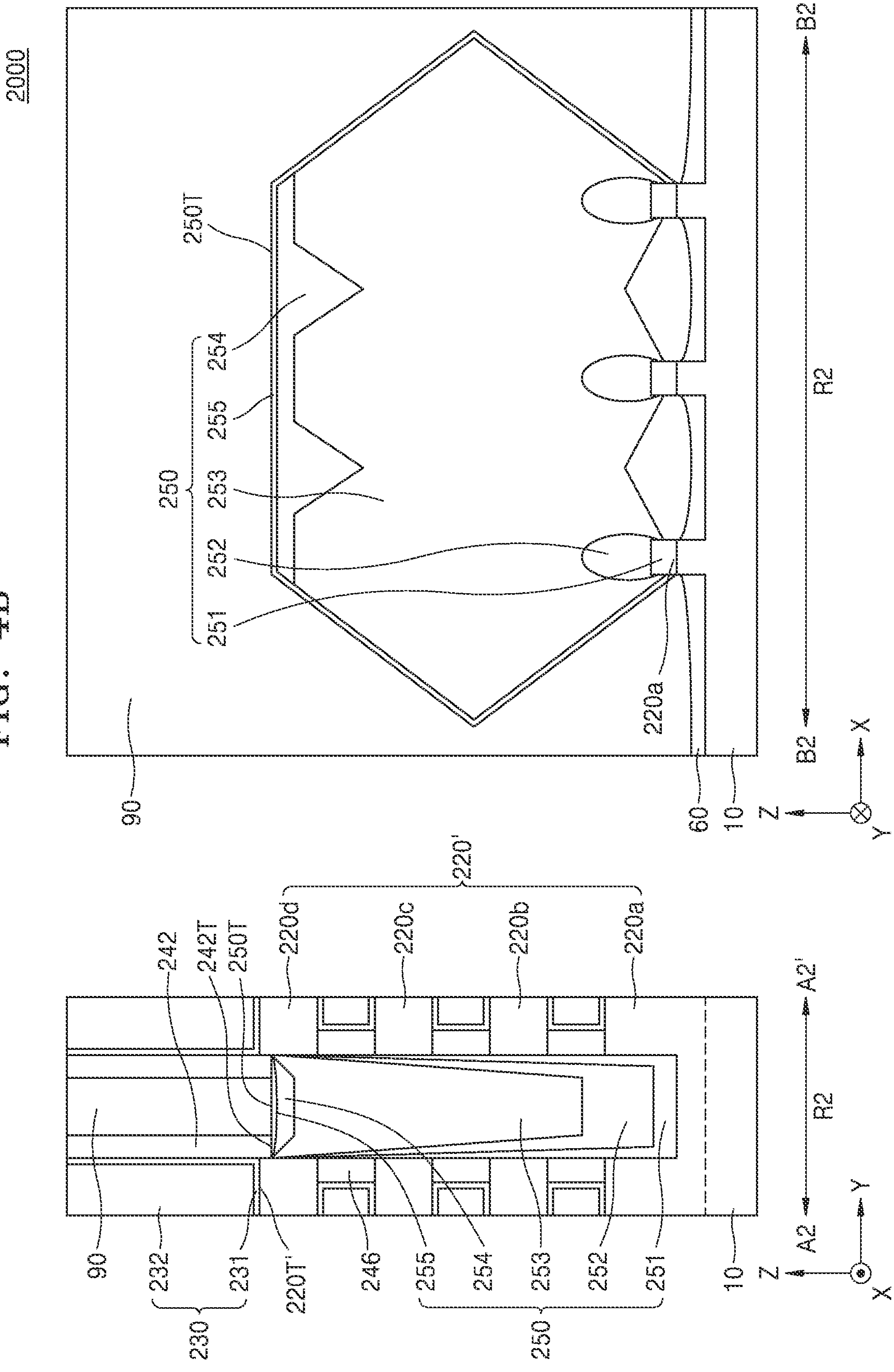

2000
90
250T
250
251
252
253
254
255
220a
60
10
B2
B2'
R2
Z
X
Y
242
242T
250T
220d
220c
220b
220a
220'
A2
A2'
R2
90
232
231
220T'
246
255
254
253
252
251
10
230
250
Z
Y
X

FIG. 5A

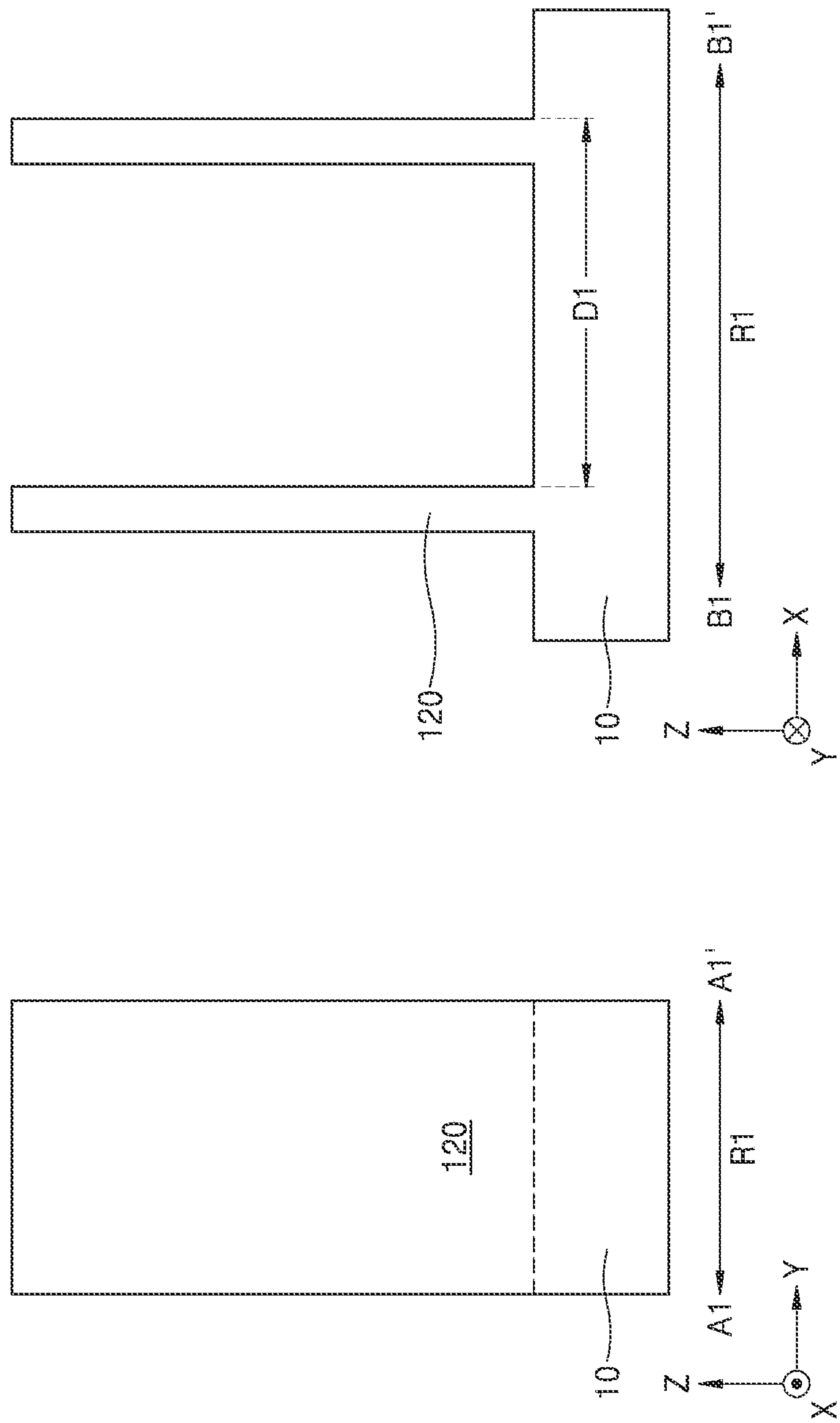


FIG. 5B

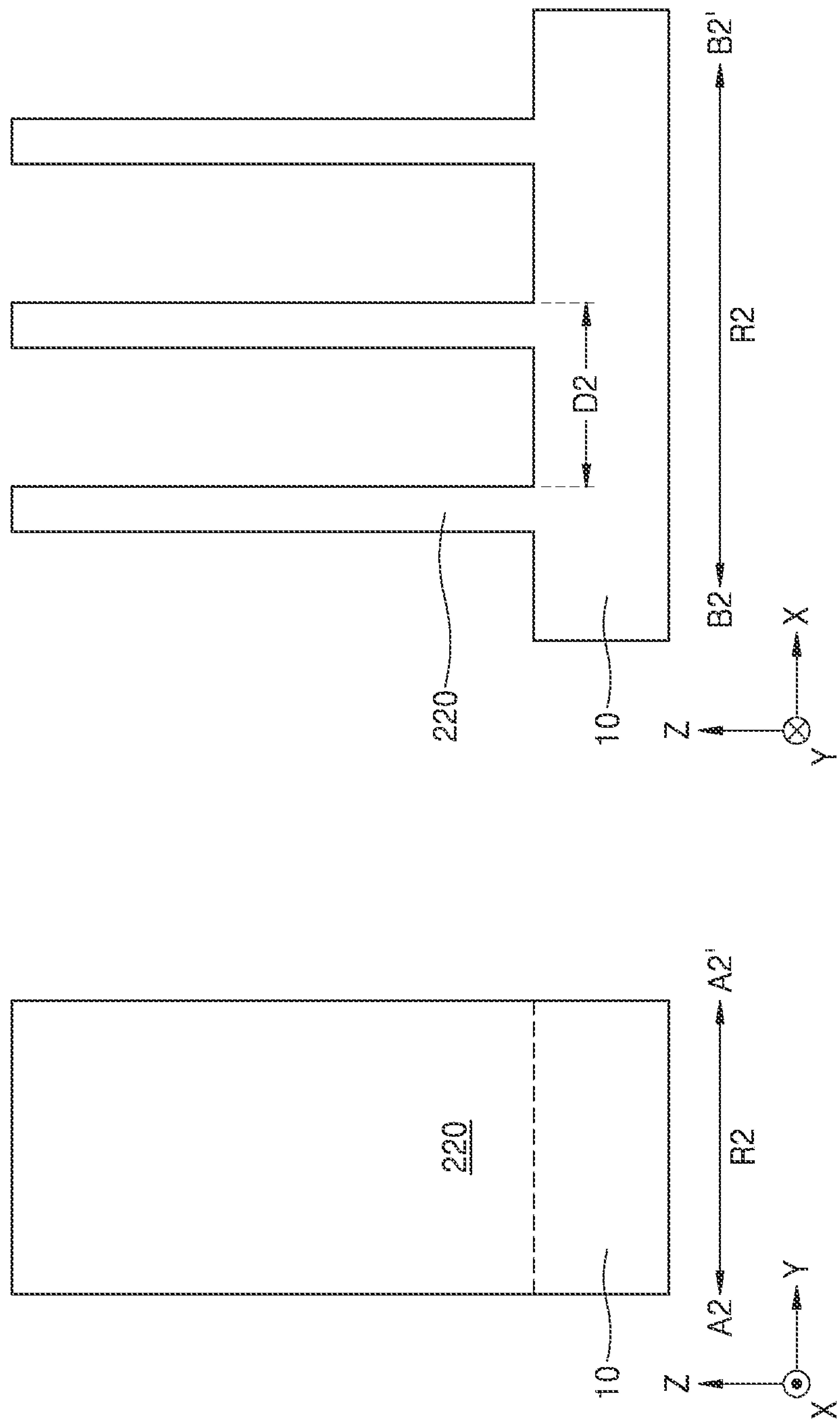


FIG. 6A

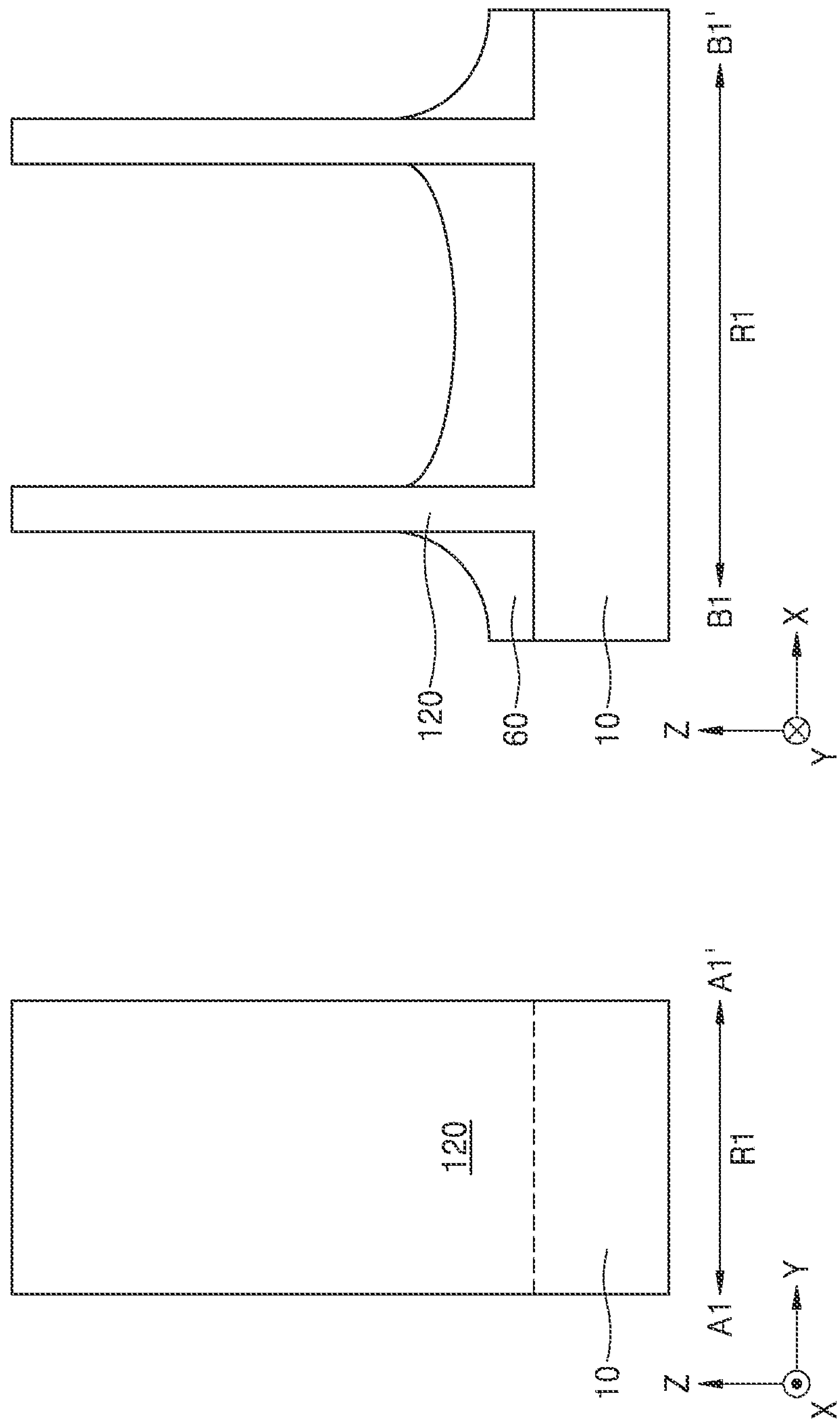


FIG. 6B

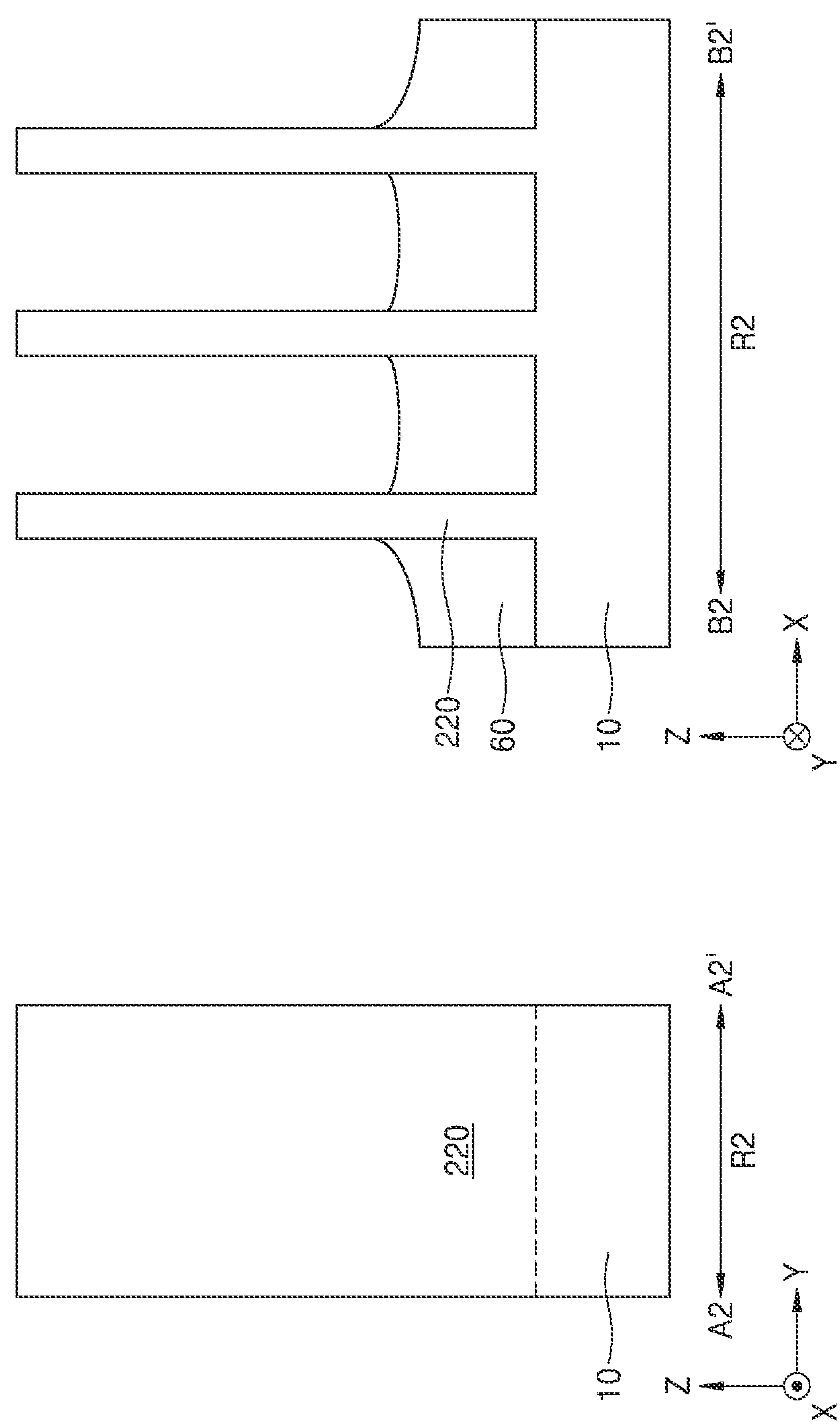


FIG. 7A

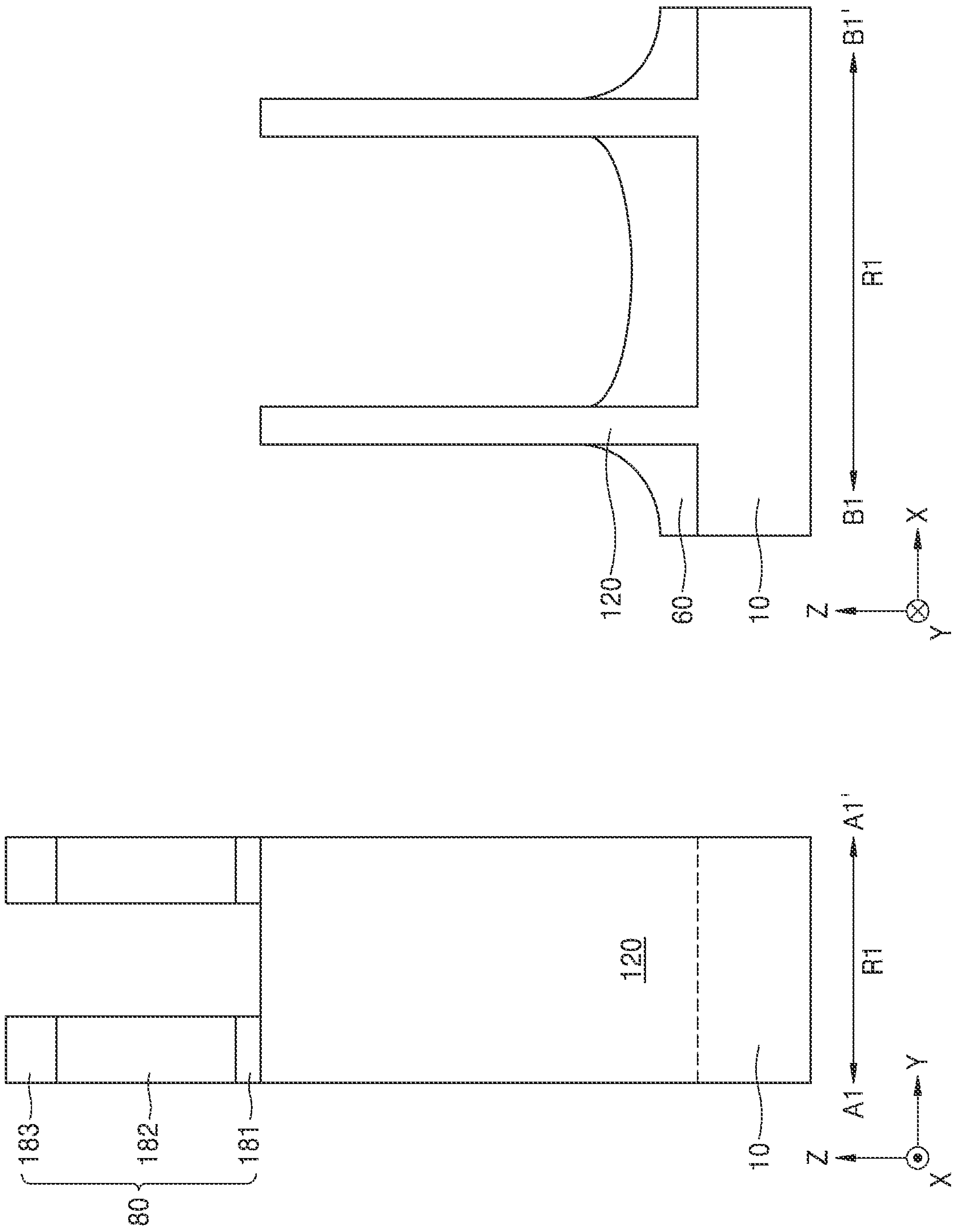


FIG. 7B

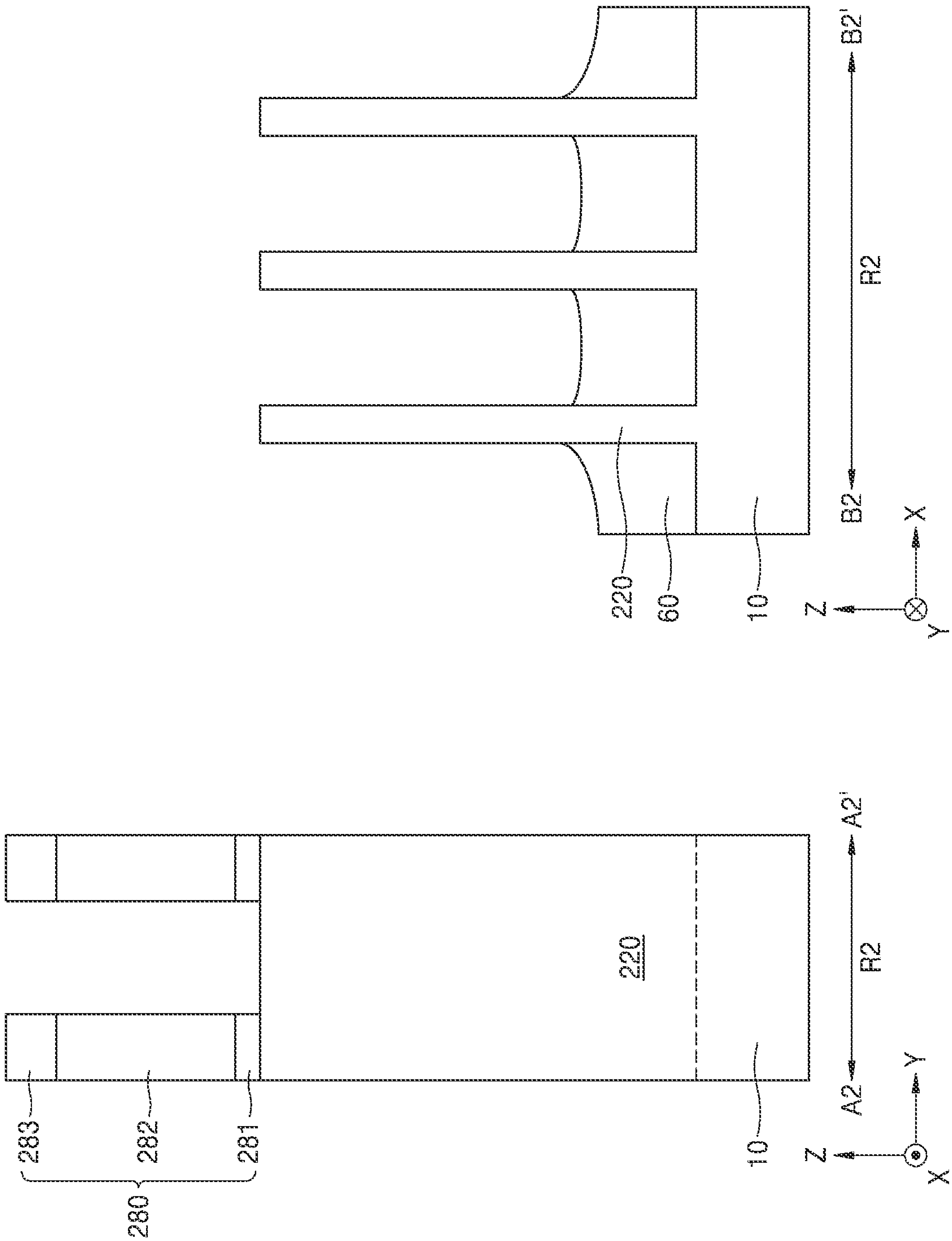


FIG. 8A

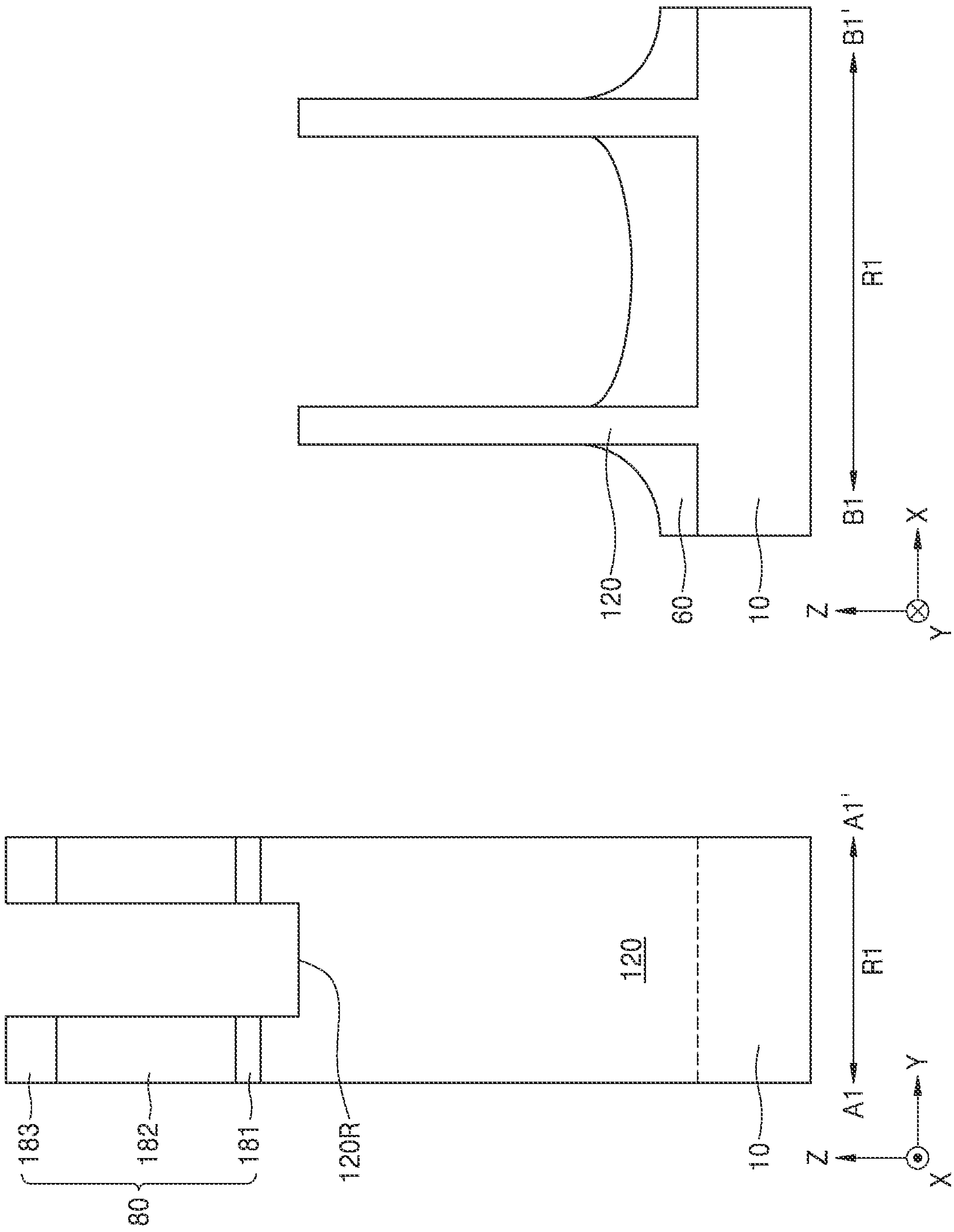


FIG. 8B

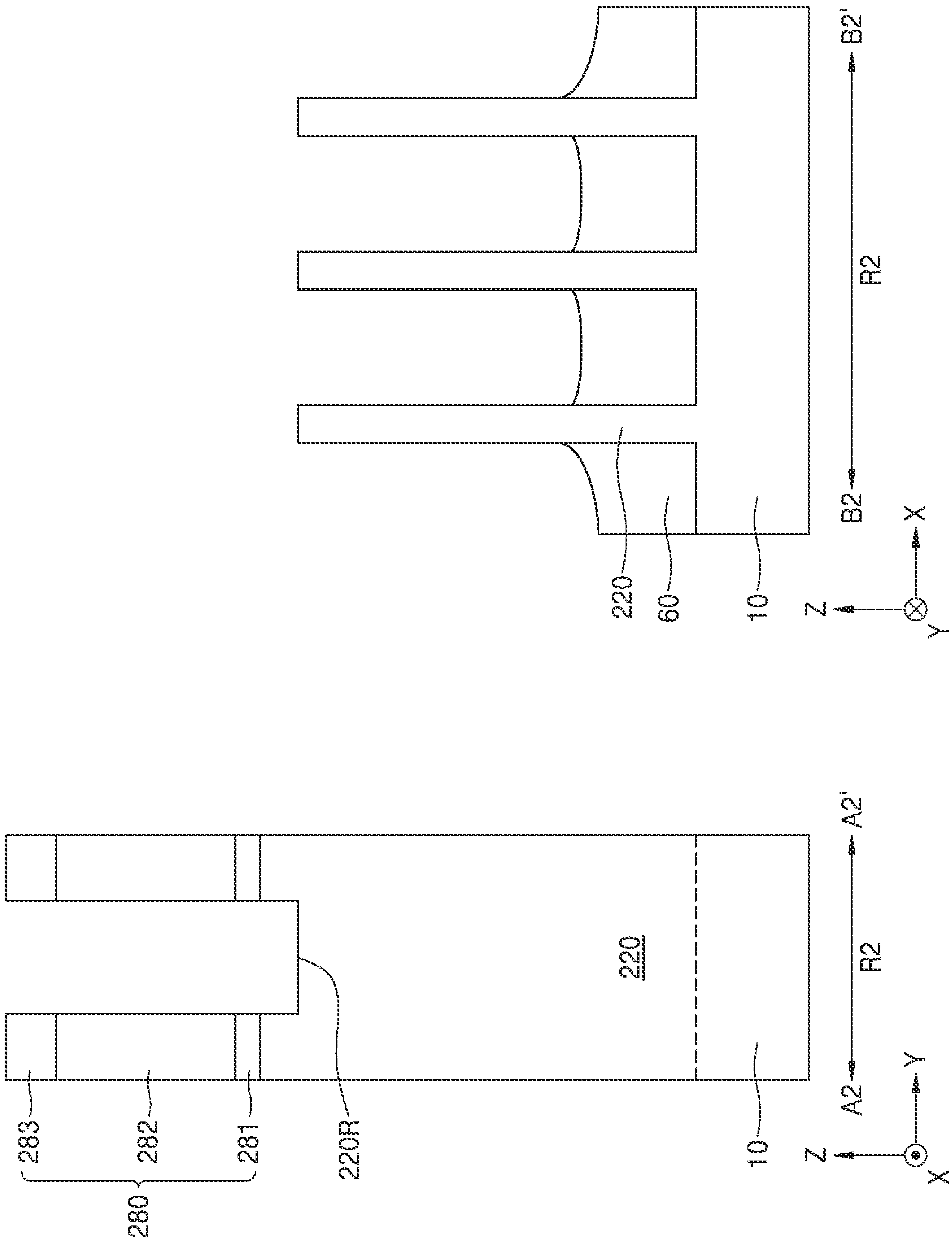
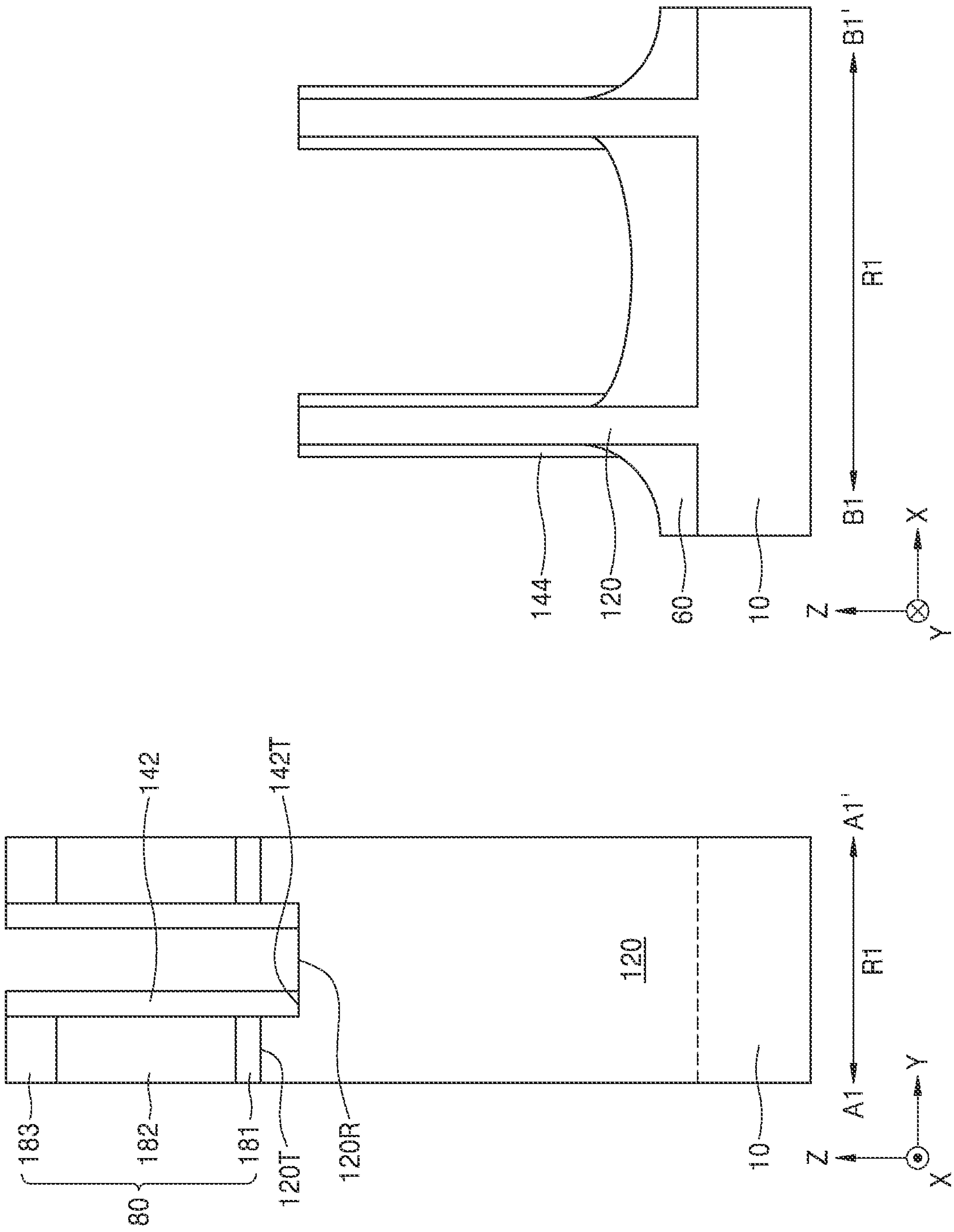
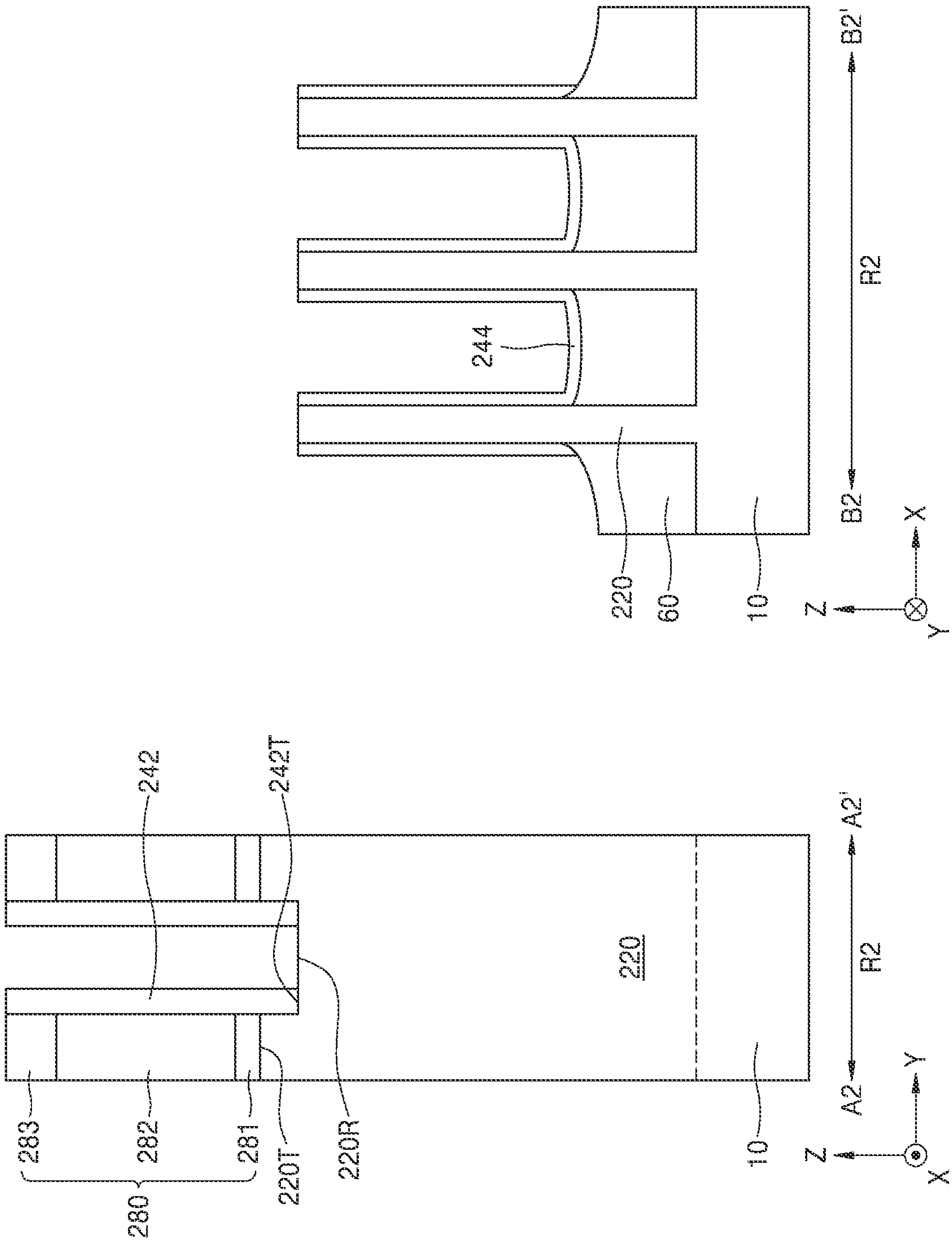


FIG. 9A



183
182
181
180
120T
120R
142
142T
120
10
A1
A1'
R1
Z
Y
X
144
120
60
10
B1
B1'
R1
Z
X
Y

FIG. 9B



220
60
10
244
B2
B2'
R2
Z
X
Y
283
282
281
280
220T
220R
242
242T
A2
A2'

FIG. 10A

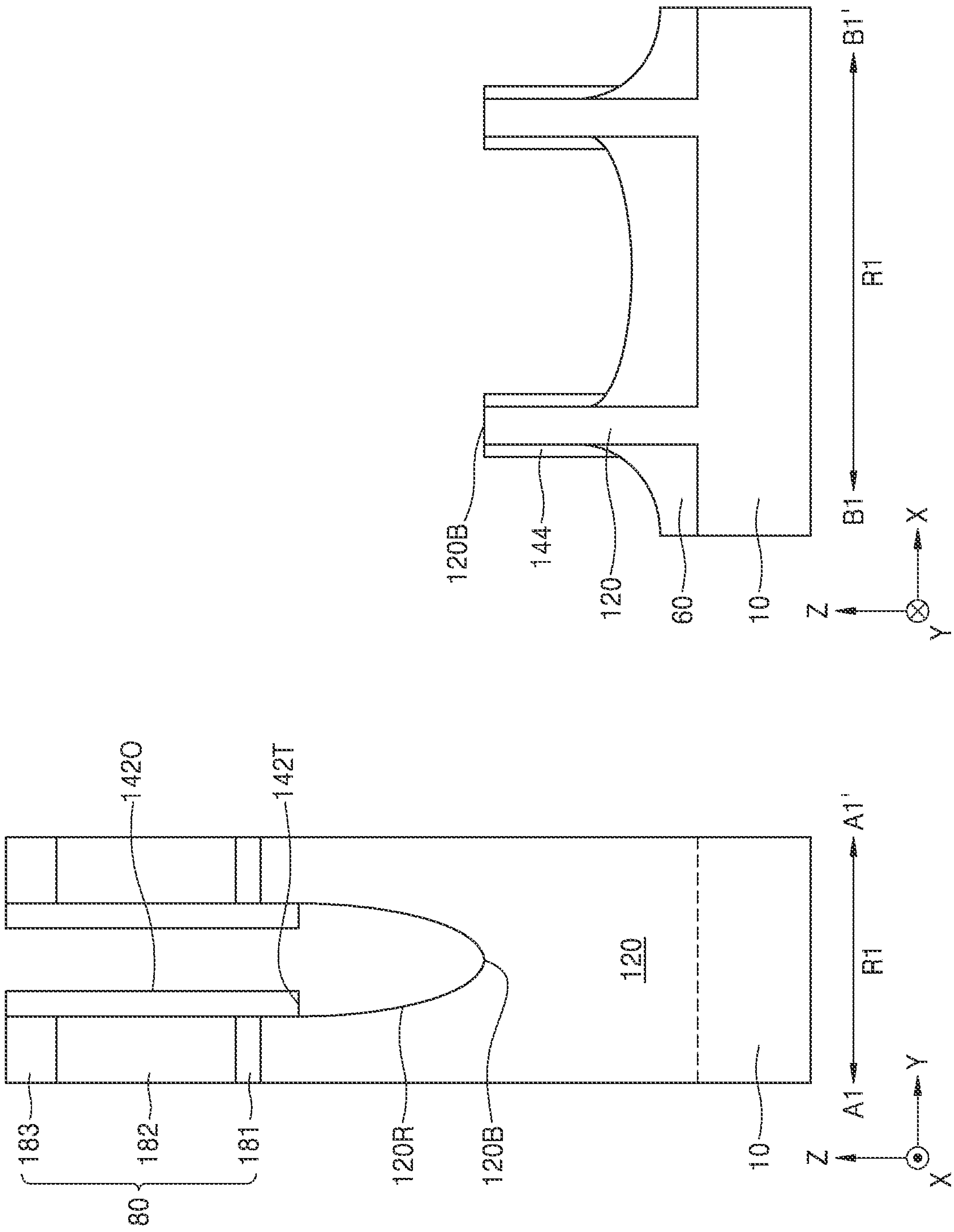

180
183
182
181
120R
120B
10
142O
142T
120
R1
A1
A1'
Z
Y
X
120B
144
120
60
10
B1
B1'
R1
Z
X
Y

FIG. 10B

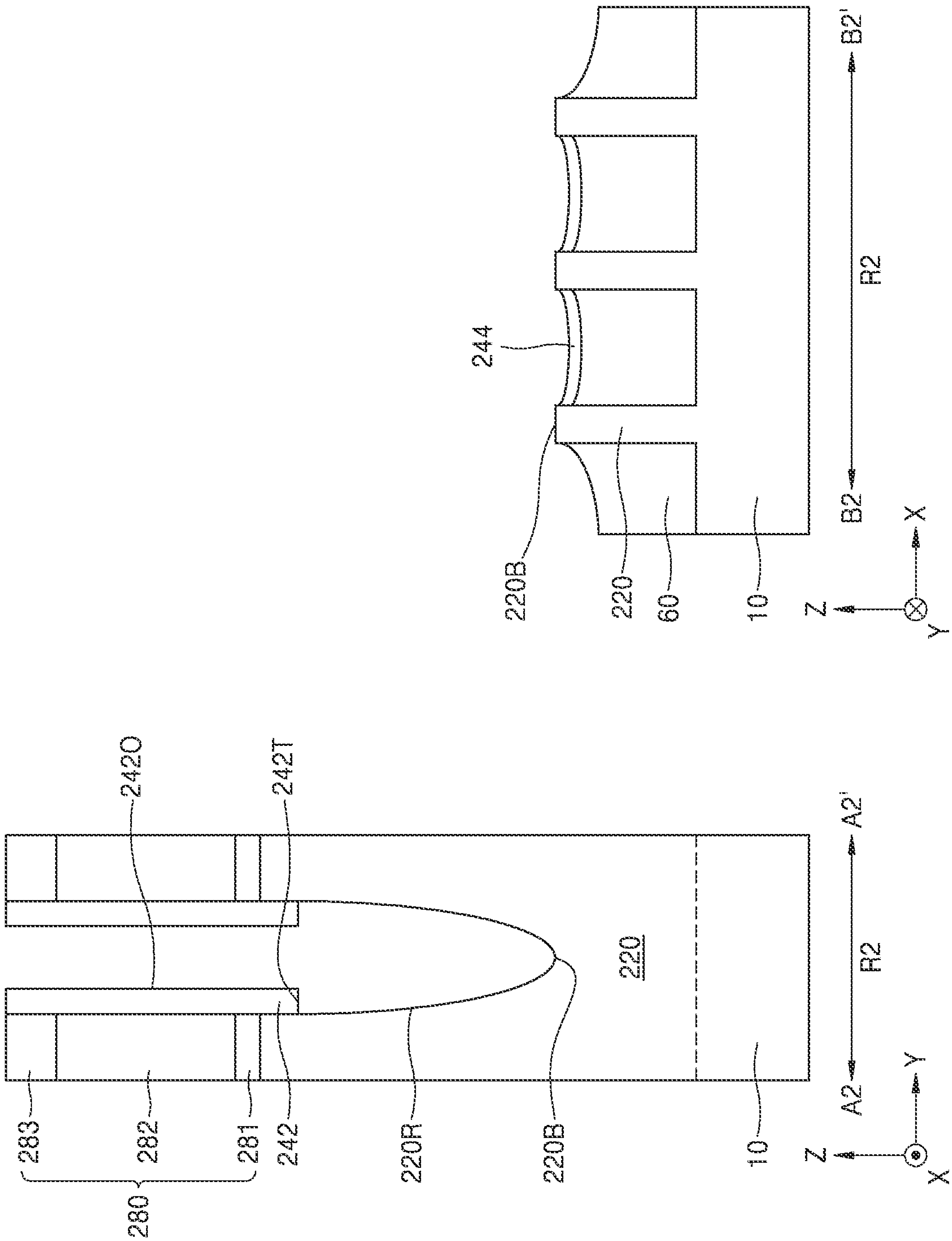

280
283
282
281
242
220R
220B
10
2420
242T
220
R2
A2
A2'
Z
Y
X
220B
220
60
10
244
B2
B2'
R2
Z
X
Y

FIG. 11A

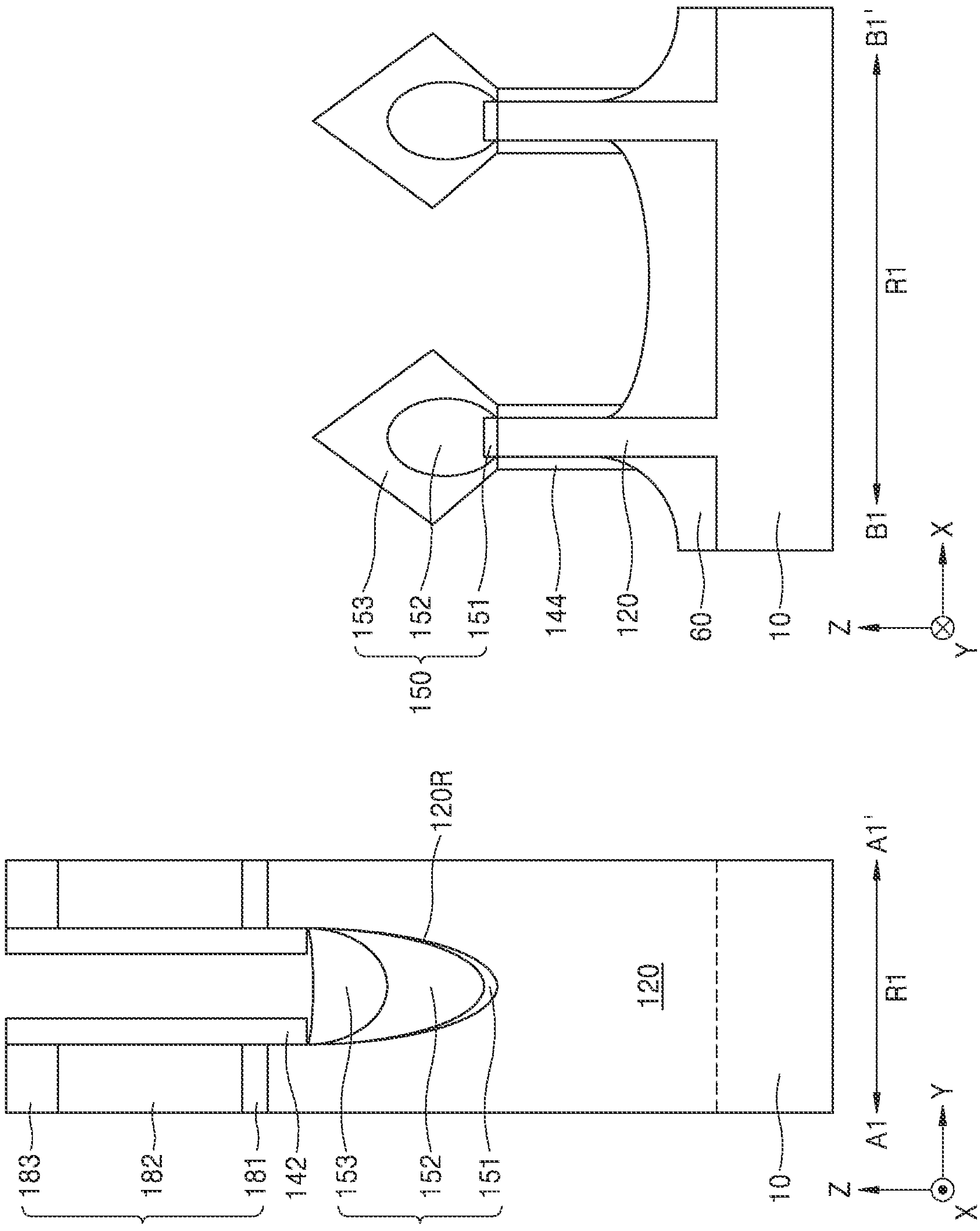
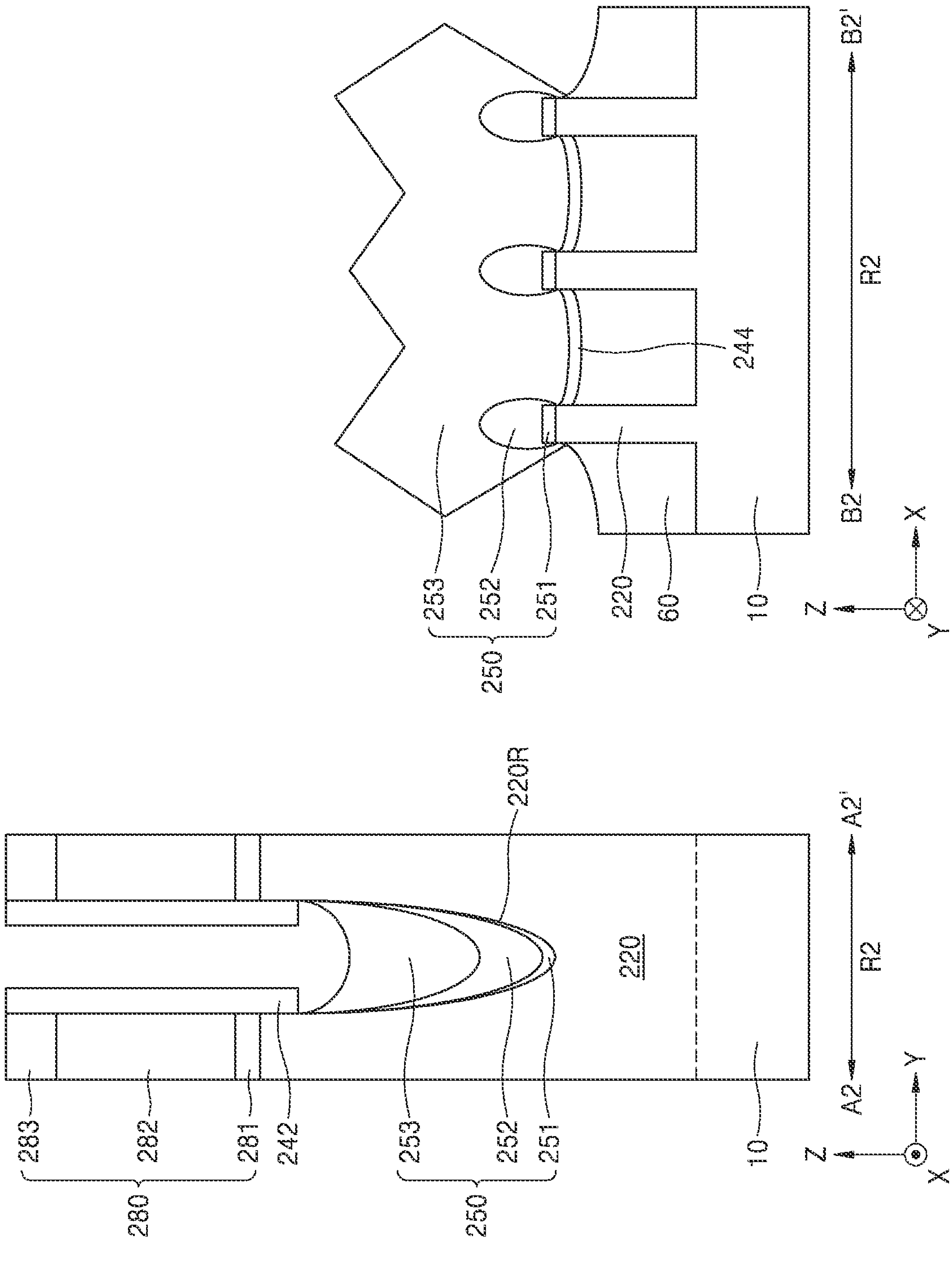

153
152
151
150
144
120
60
10
B1
B1'
R1
Z
X
Y
183
182
181
180
142
153
152
151
150
120R
120
10
A1
A1'
R1
Z
Y
X

FIG. 11B



283
282
281
280
242
253
252
251
250
220R
220
10
A2
A2'
R2
Z
Y
X
244
60
B2
B2'

FIG. 11C

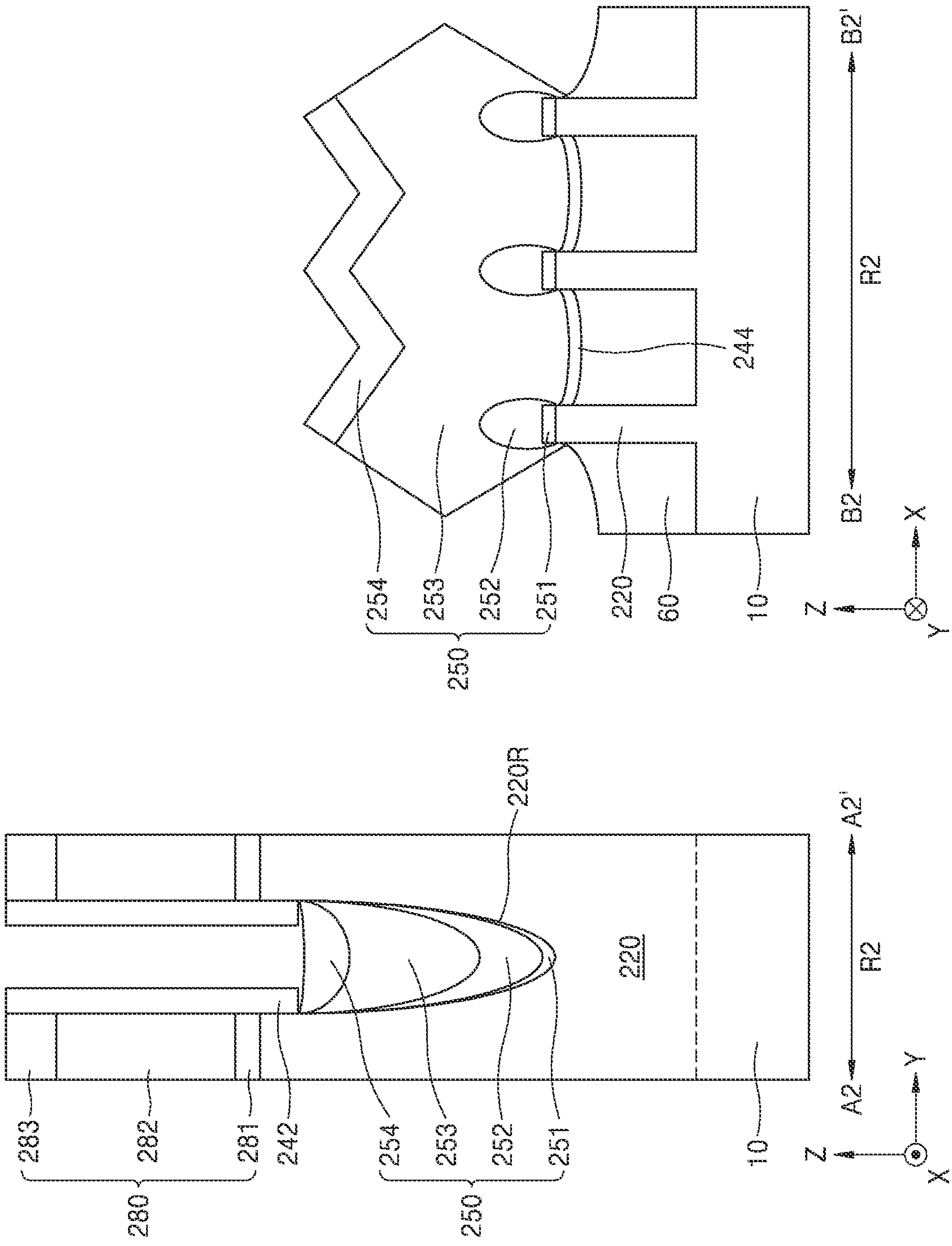

280
283
282
281
242
250
254
253
252
251
220R
220
10
A2
A2'
R2
Z
Y
X
250
254
253
252
251
220
60
10
244
B2
B2'
R2
Z
X
Y

FIG. 12A

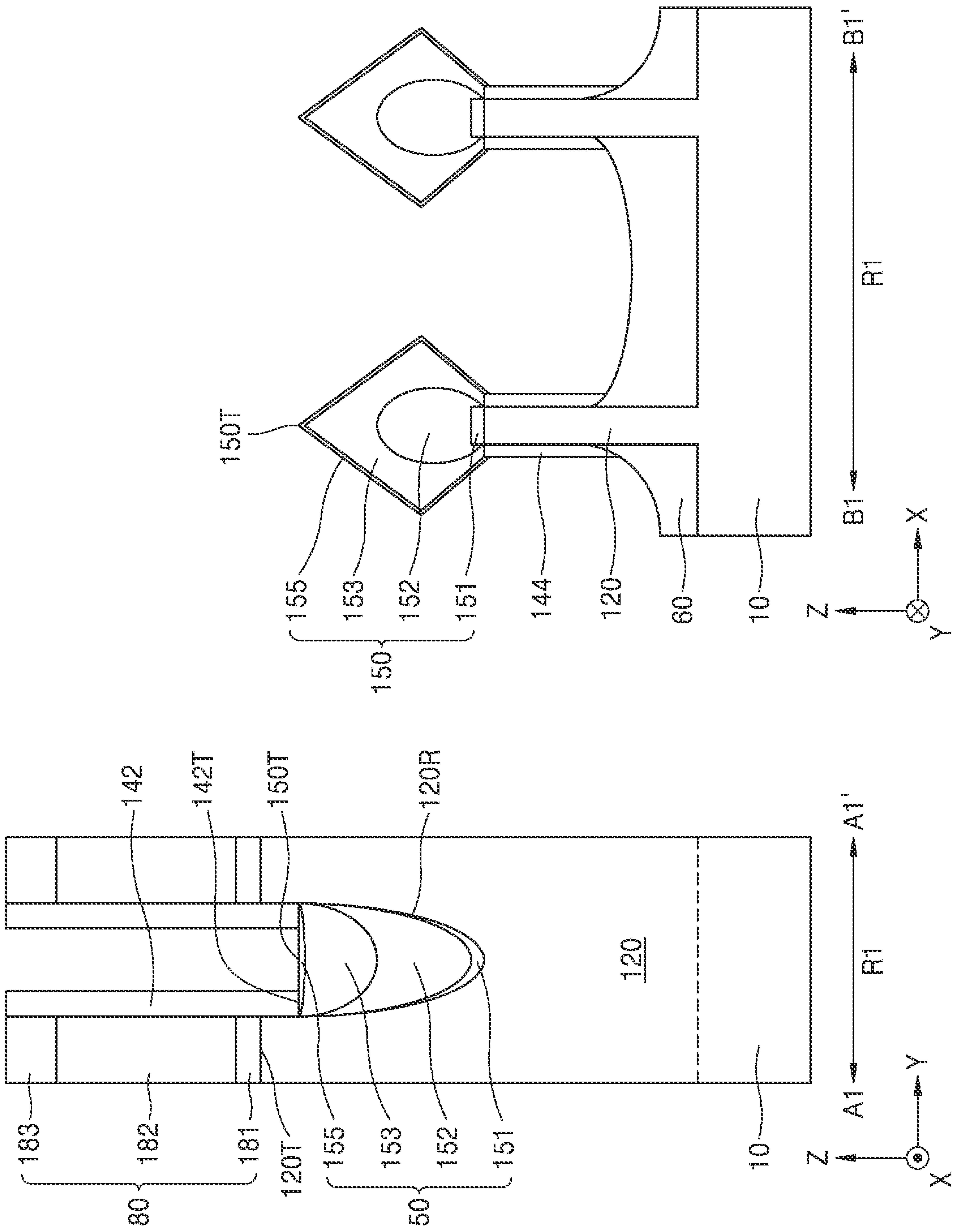

183
182
181
180
120T
155
153
152
151
150
10
142
142T
150T
120R
120
R1
A1
A1'
Z
Y
X
150T
155
153
152
151
150
144
120
60
10
B1
B1'
R1
Z
X
Y

FIG. 12B

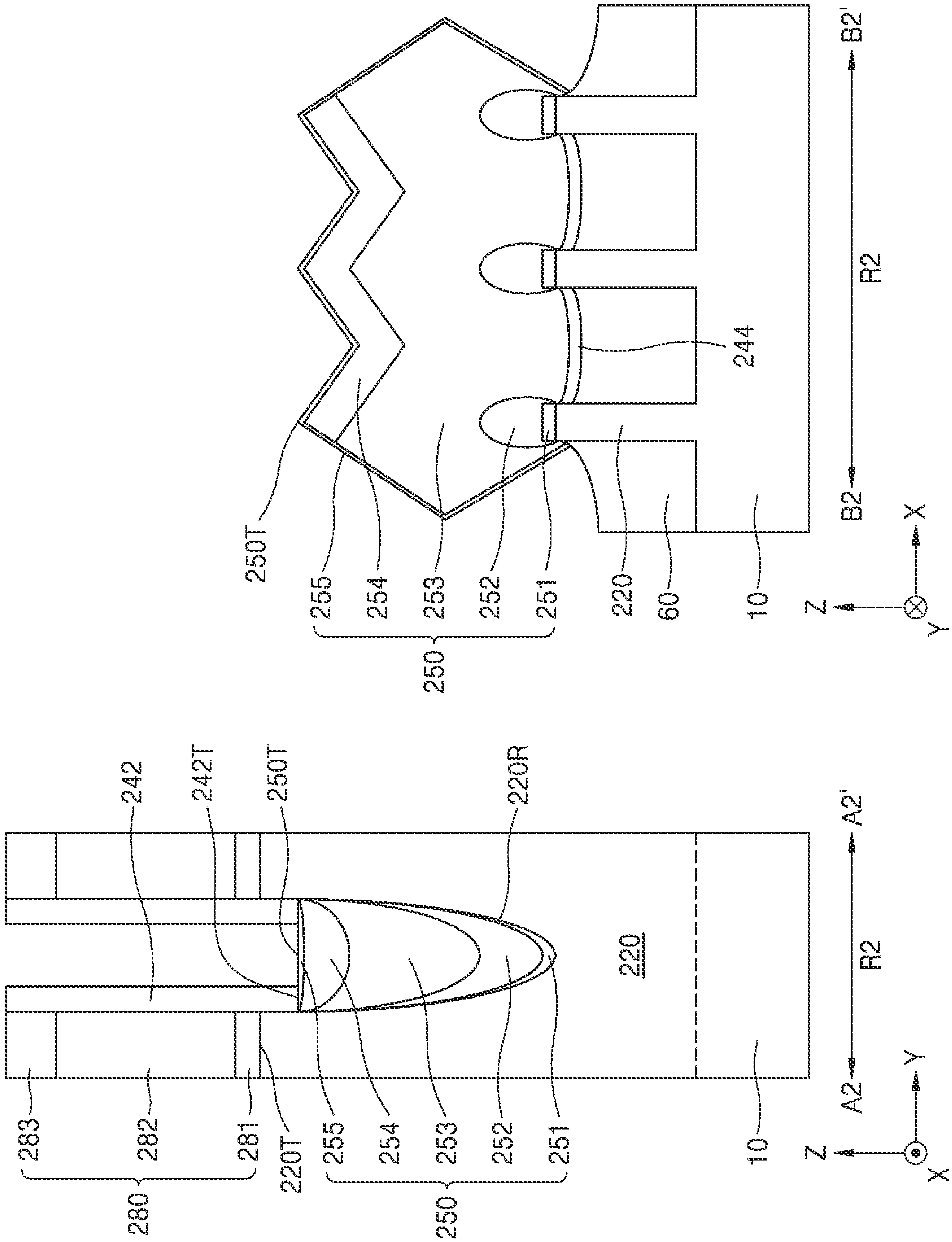

283
282
281
280
220T
255
254
253
252
251
250
242
242T
250T
220R
220
10
A2
A2'
R2
Z
Y
X
250T
255
254
253
252
251
250
220
60
10
244
B2
B2'
R2
Z
X
Y

FIG. 13A

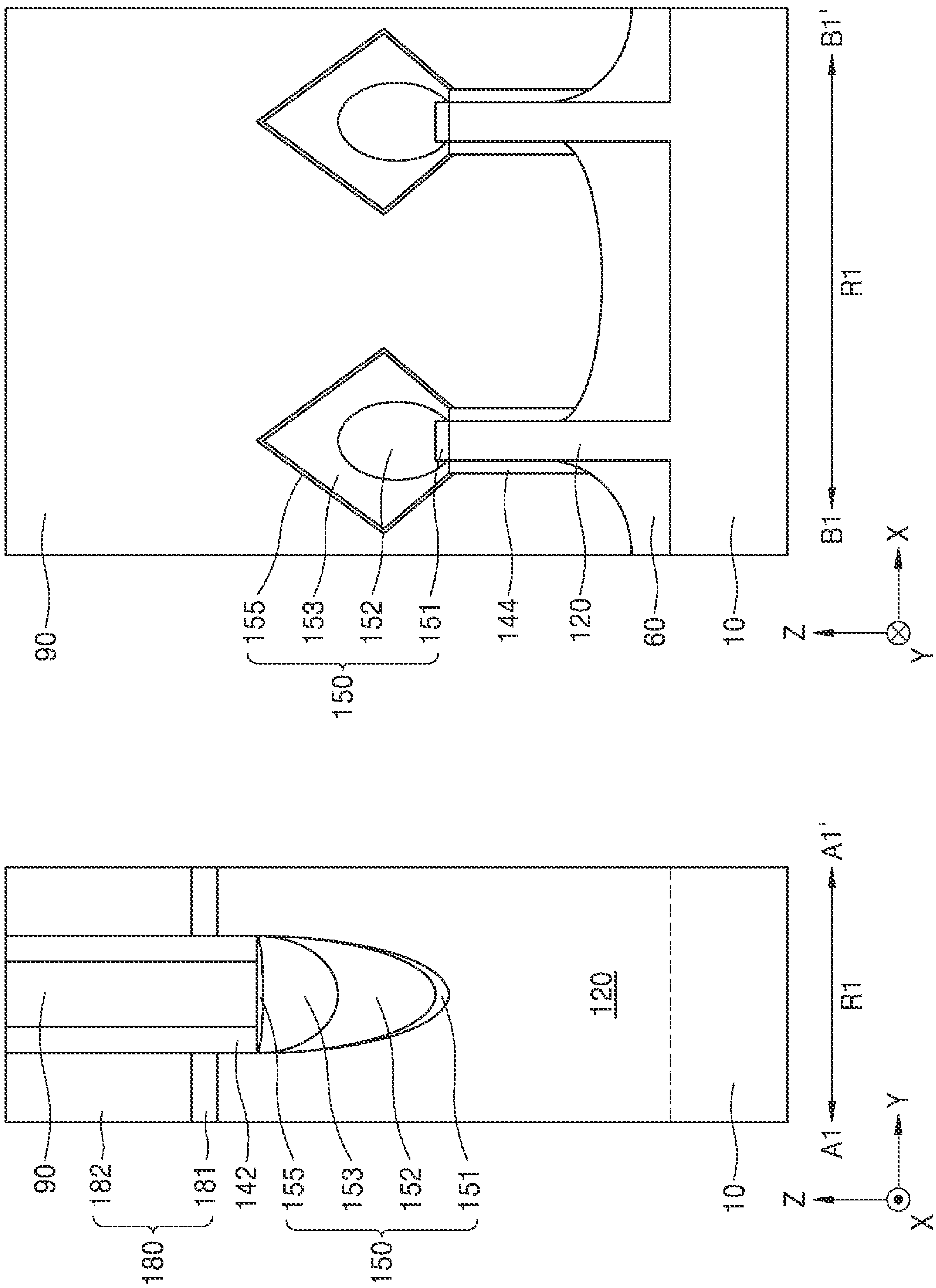

90
155
153
152
151
150
144
120
60
10
B1
B1'
R1
Z
Y
X
90
182
181
180
142
155
153
152
151
150
120
10
A1
A1'
R1
Z
X
Y

FIG. 13B

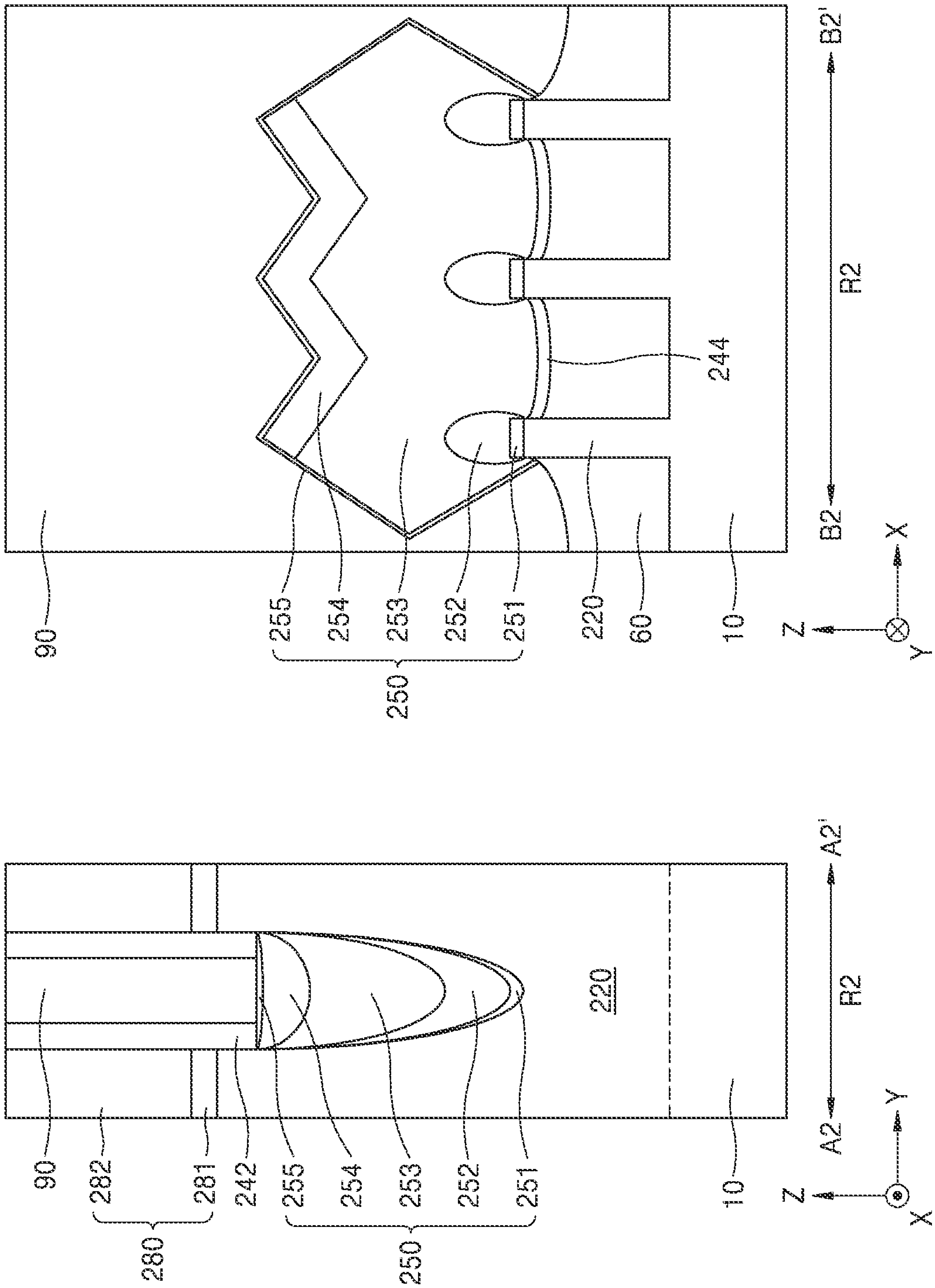

90
282
281
280
242
255
254
253
252
251
250
220
10
A2
A2'
R2
Z
Y
X
255
254
253
252
251
250
220
60
10
244
B2
B2'
R2
Z
X
Y

FIG. 14A

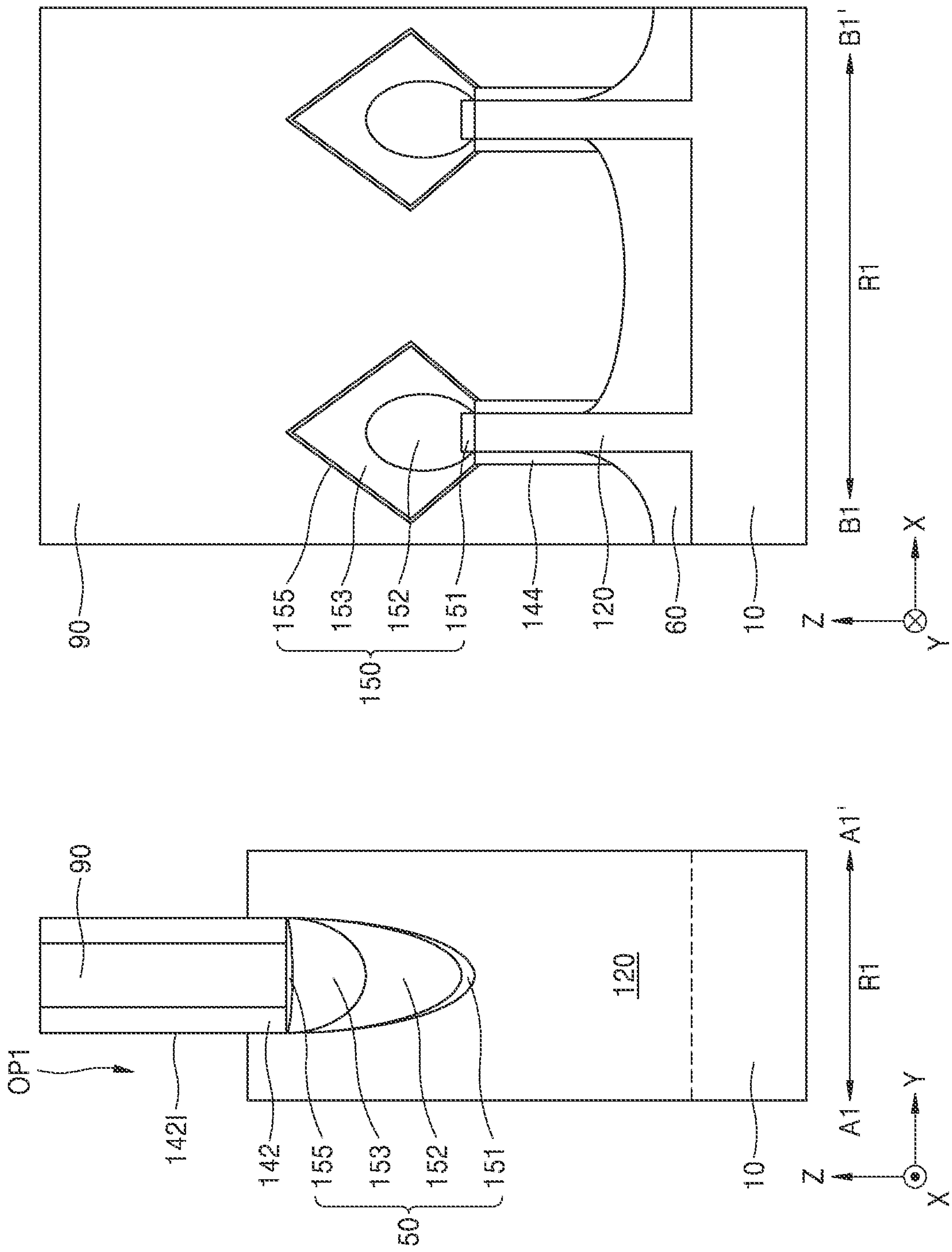

90
155
153
152
151
150
144
120
60
10
B1
B1'
R1
Z
X
Y
OP1
142I
142
A1
A1'

FIG. 14B

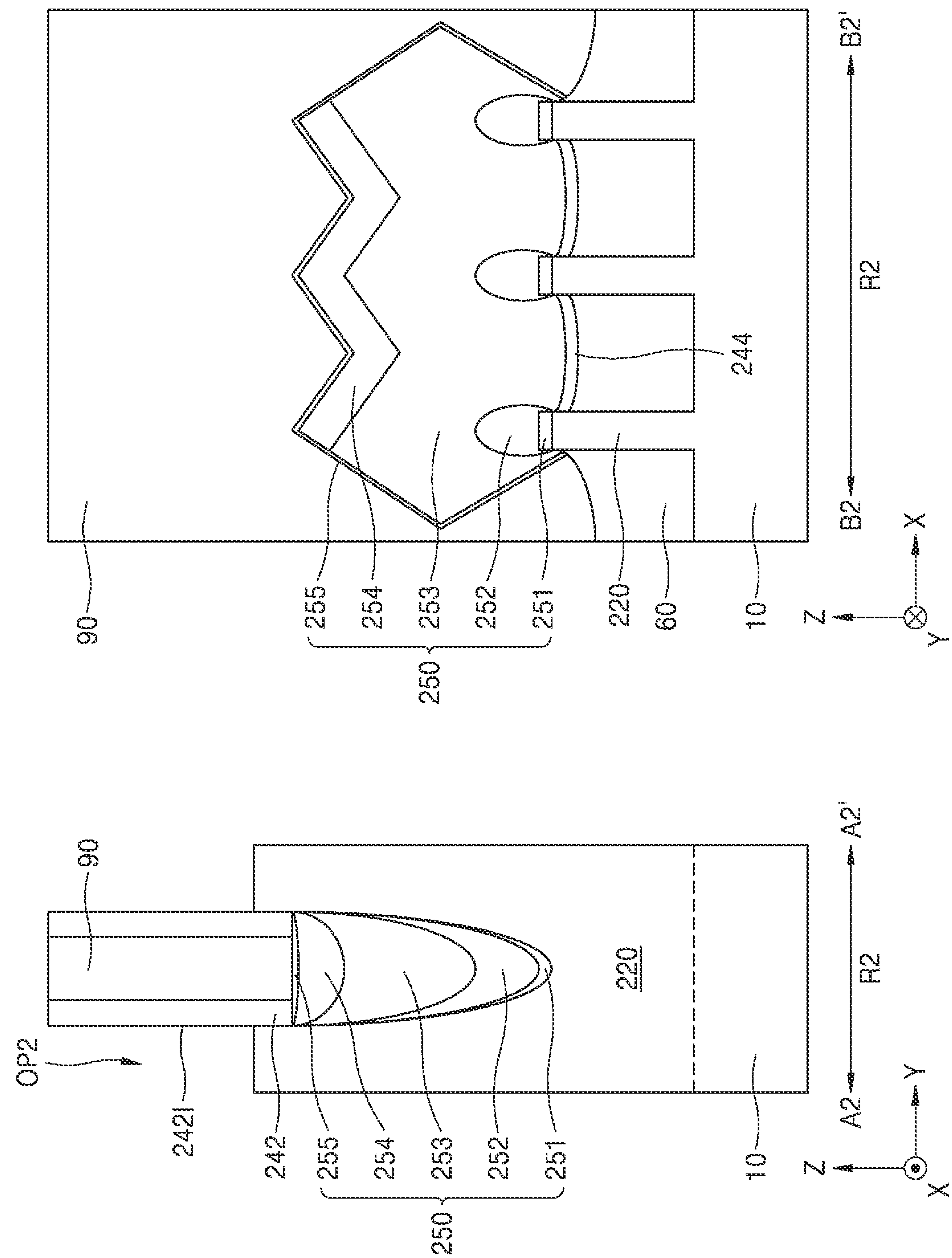

90
255
254
253
252
251
220
60
10
250
244
B2
B2'
R2
Z
X
Y
OP2
242I
242
A2
A2'
Y

FIG. 15A

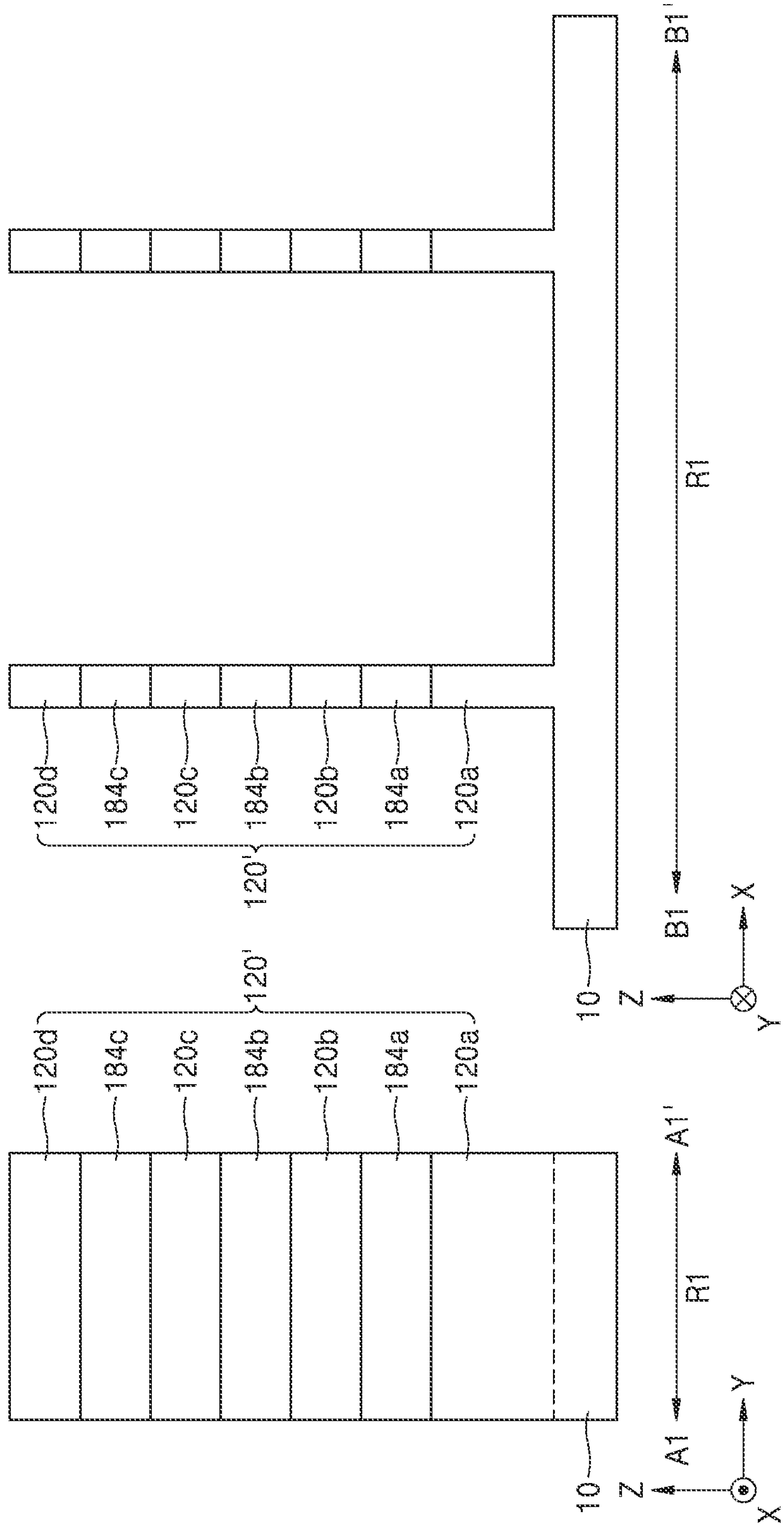


FIG. 15B

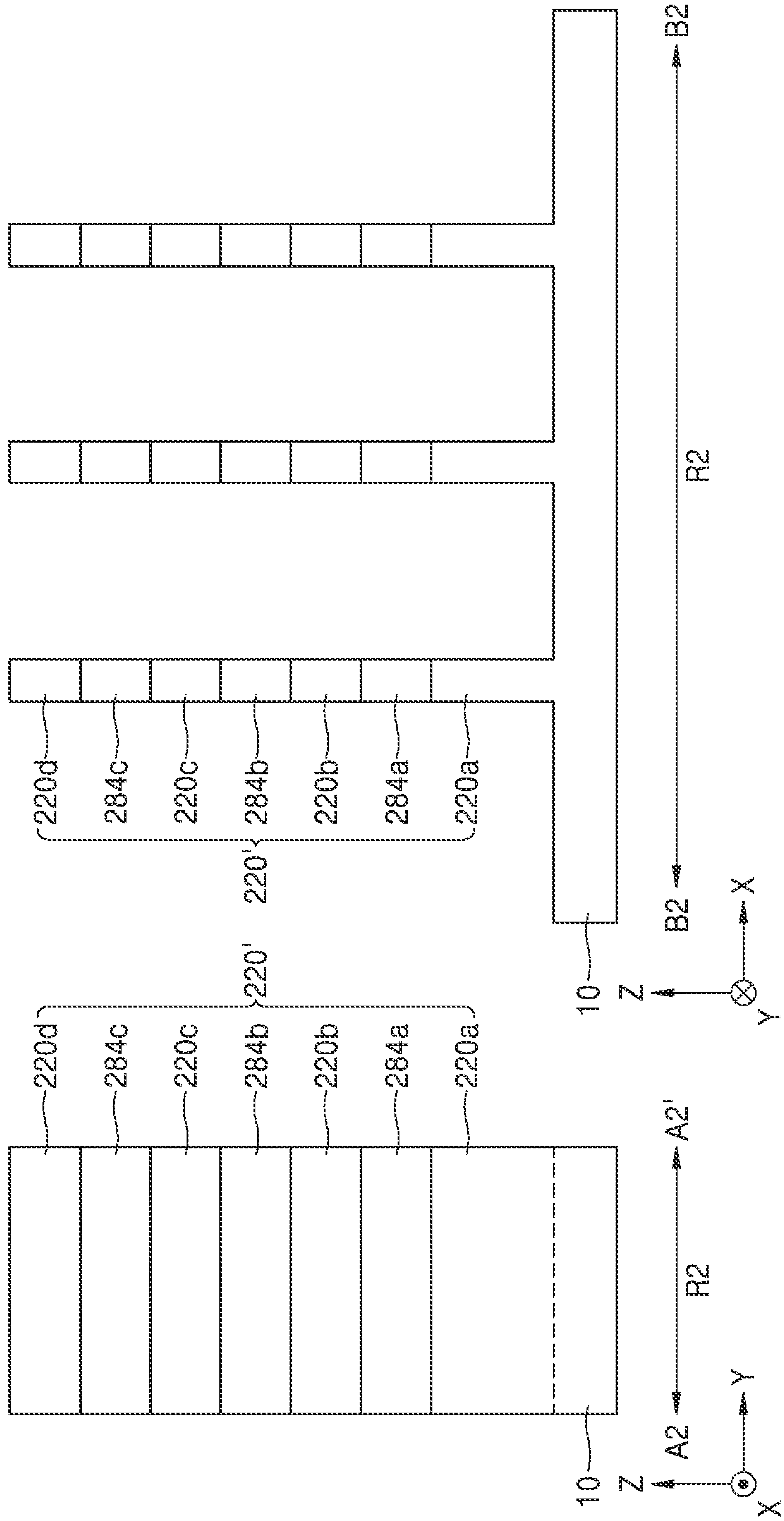

220'
220d
284c
220c
284b
220b
284a
220a
10
A2
R2
A2'
Z
Y
X
220'
220d
284c
220c
284b
220b
284a
220a
10
B2
R2
B2'
Z
X
Y

FIG. 16A

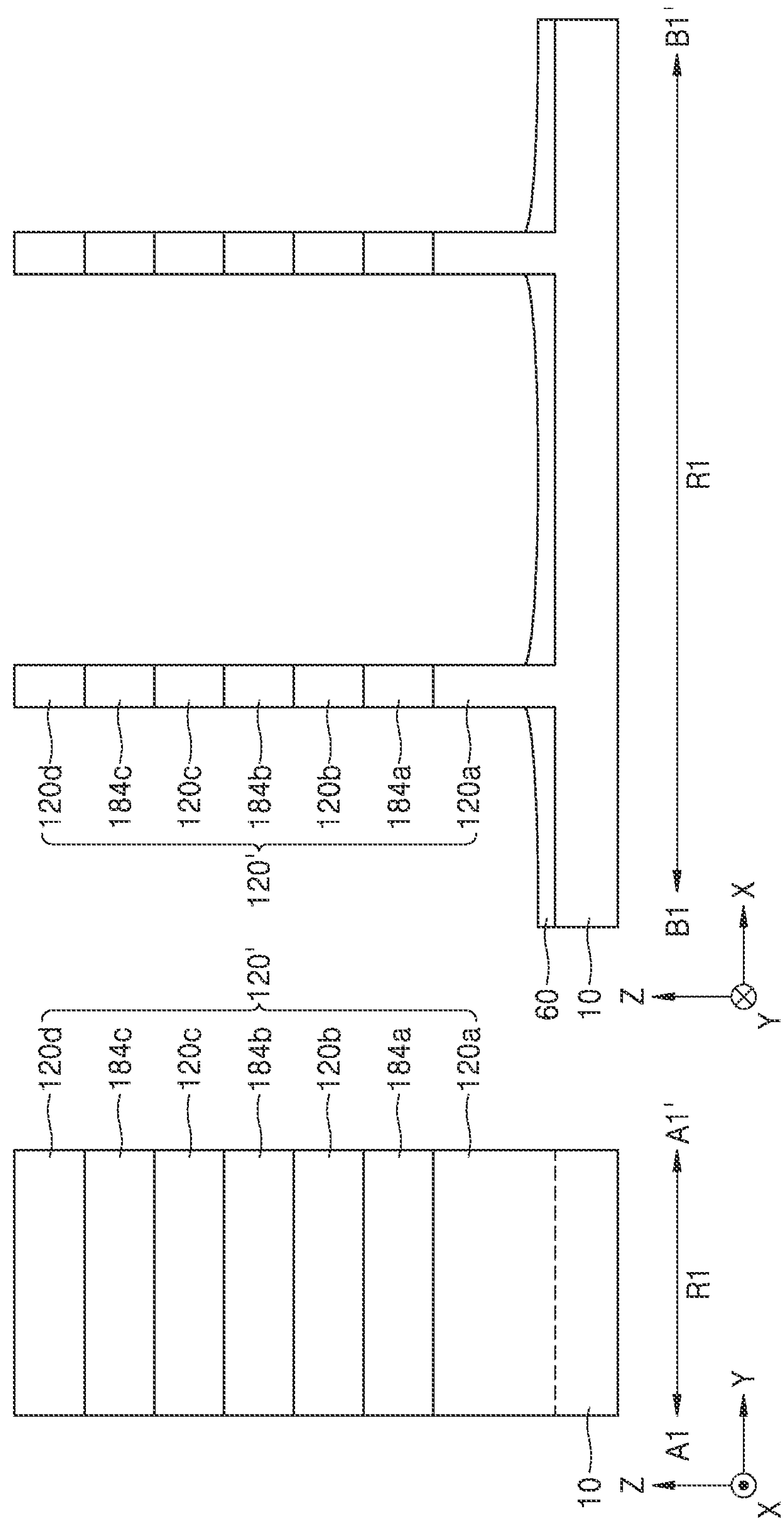


FIG. 16B

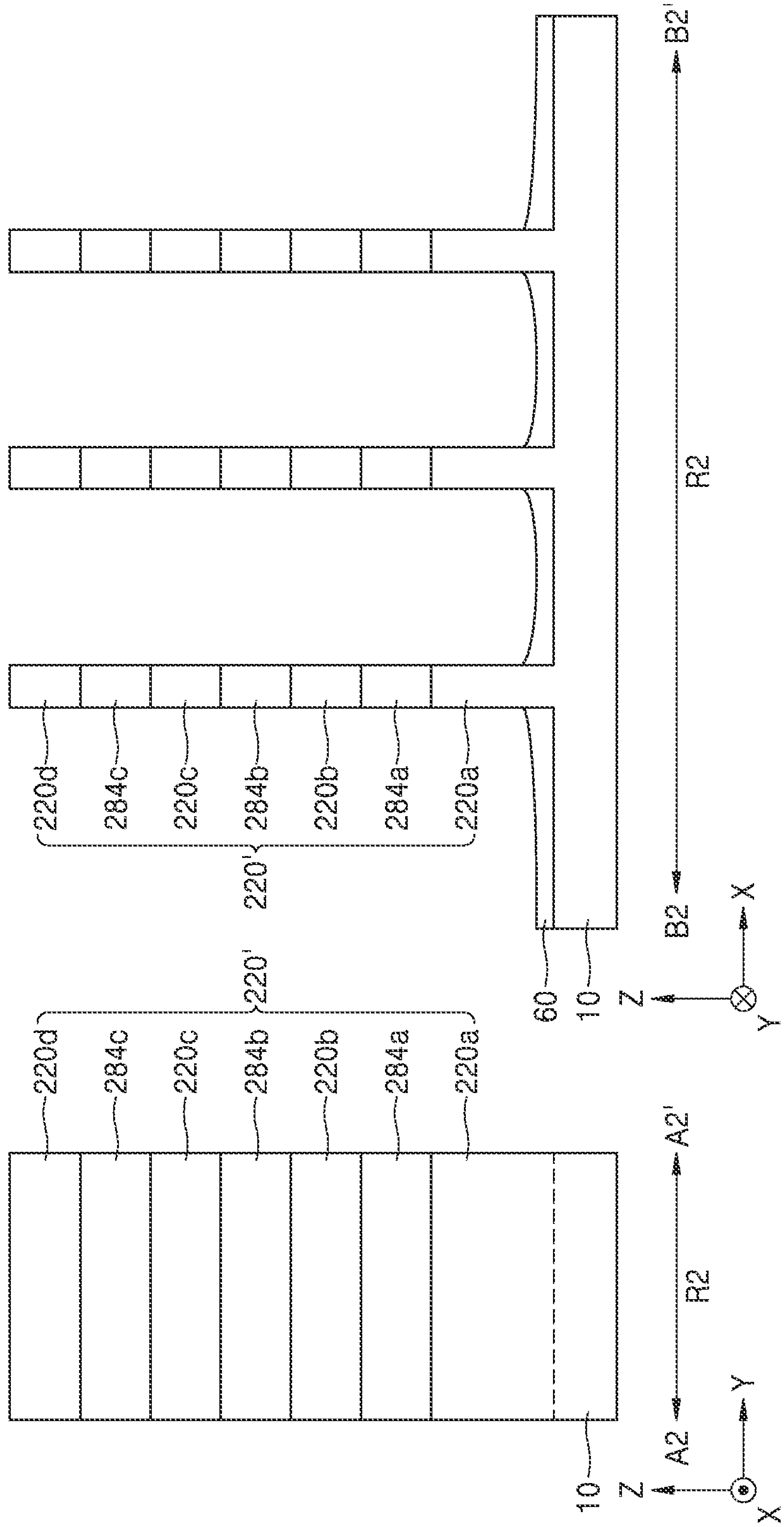

220'
220d
284c
220c
284b
220b
284a
220a
10
A2
R2
A2'
Z
Y
X
220'
220d
284c
220c
284b
220b
284a
220a
60
10
B2
R2
B2'
Z
X
Y

FIG. 17A

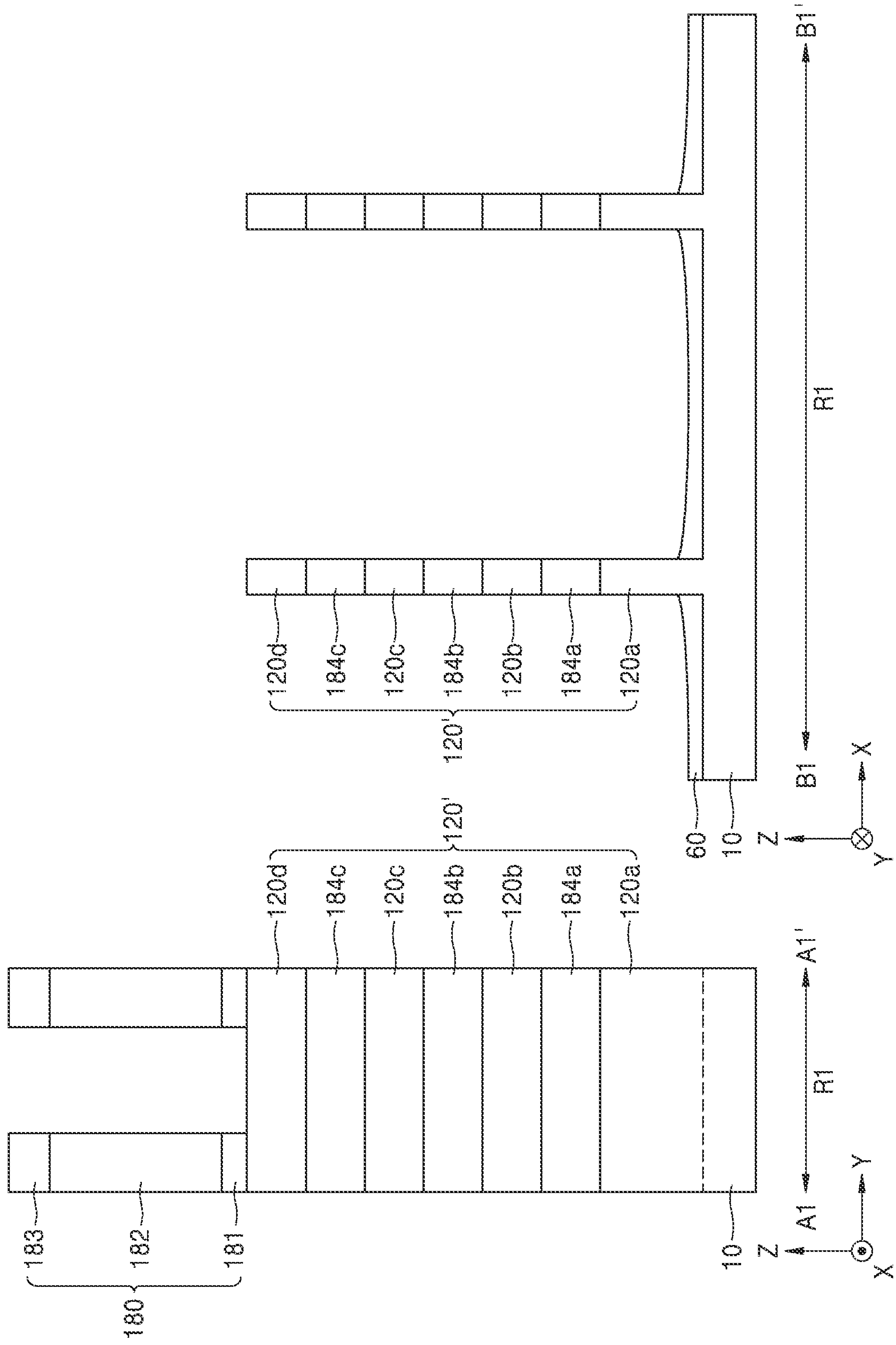

183
182
181
180
10
A1
A1'
R1
Z
Y
X
120d
184c
120c
184b
120b
184a
120a
120'
60
10
B1
B1'
R1
Z
X
Y

FIG. 17B

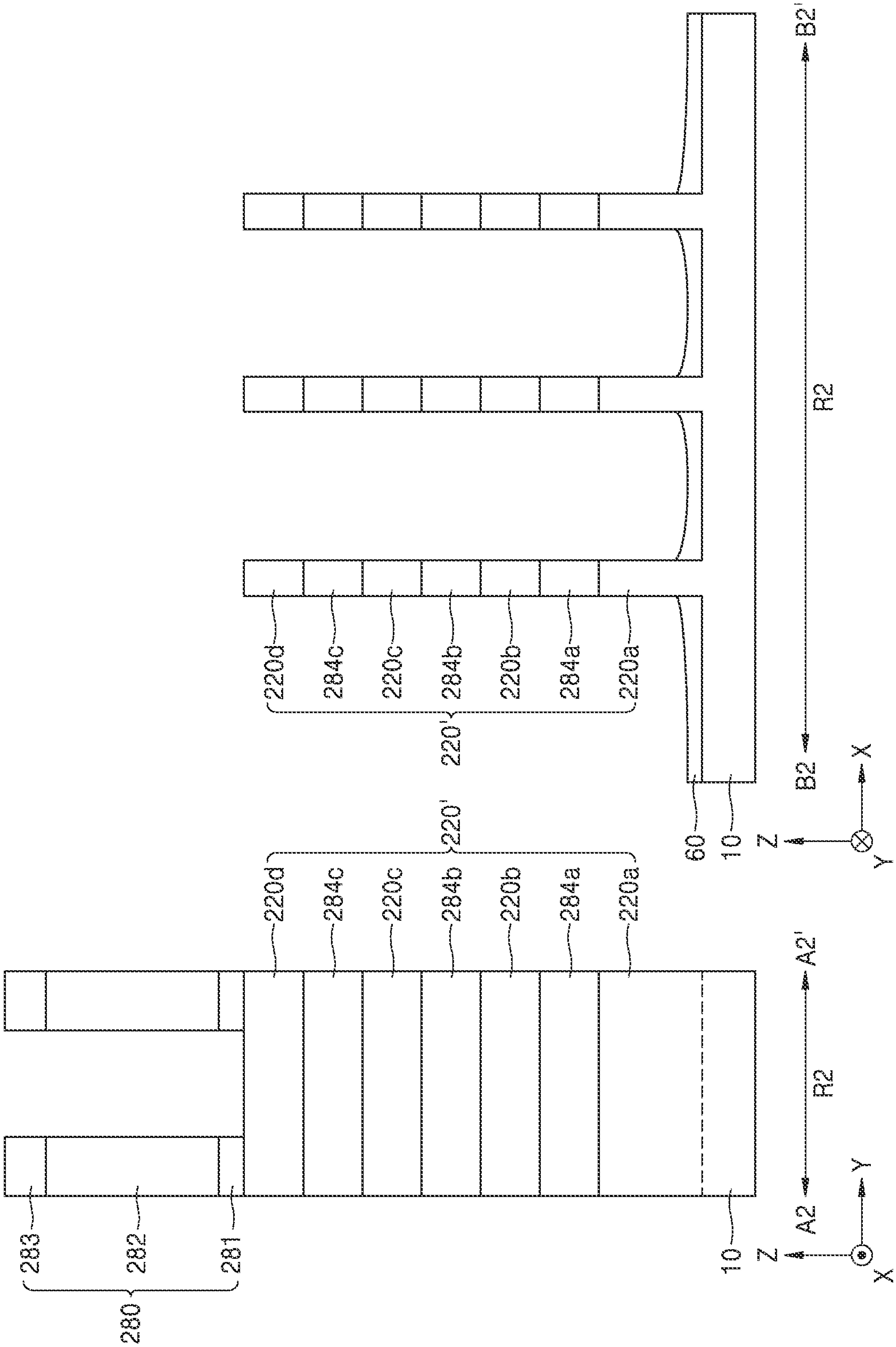
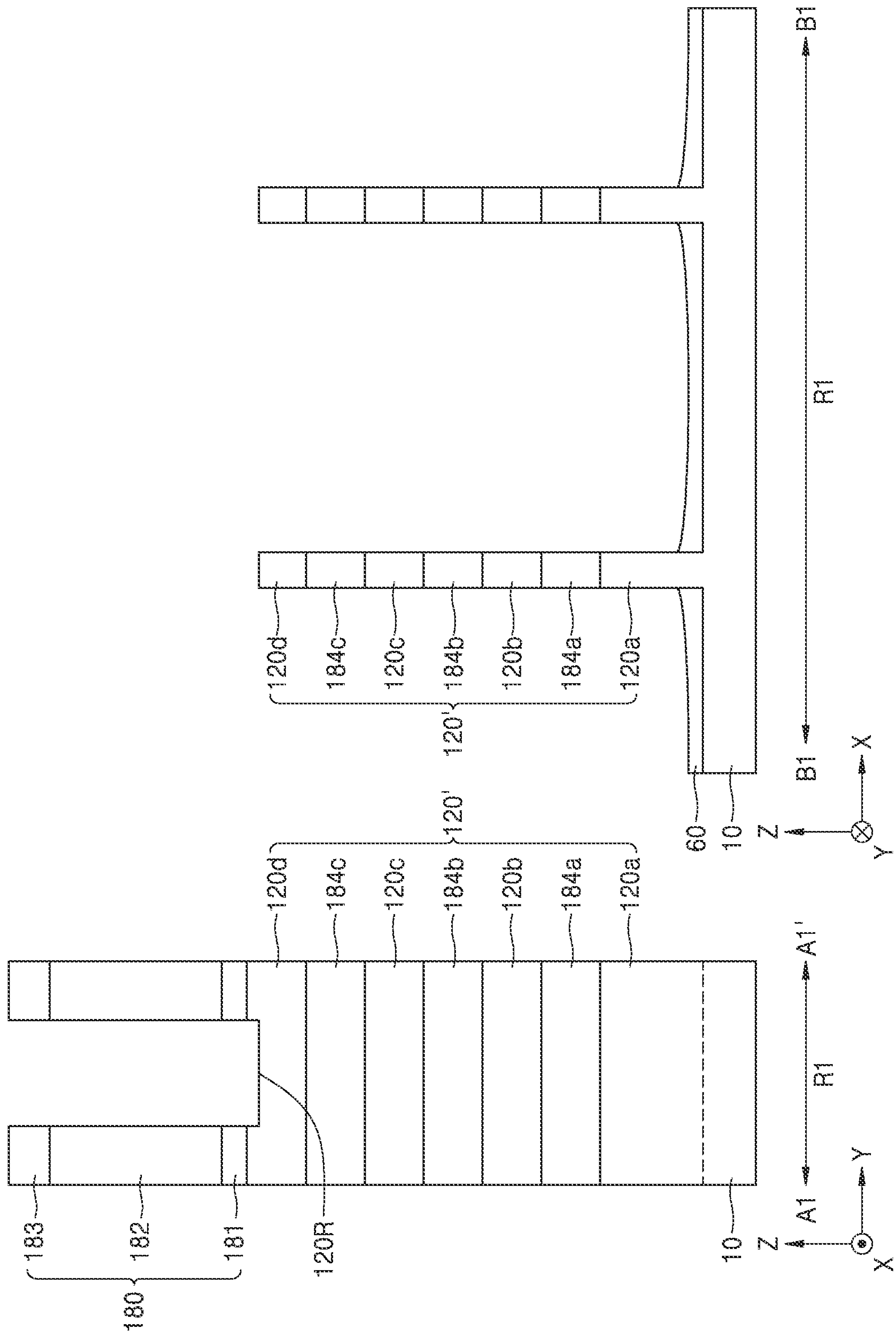

280
283
282
281
10
A2
A2'
R2
Z
Y
X
220'
220d
284c
220c
284b
220b
284a
220a
60
B2
B2'

FIG. 18A



180
183
182
181
120R
10
A1
A1'
R1
120'
120d
184c
120c
184b
120b
184a
120a
60
B1
B1'
Z
X
Y

FIG. 18B

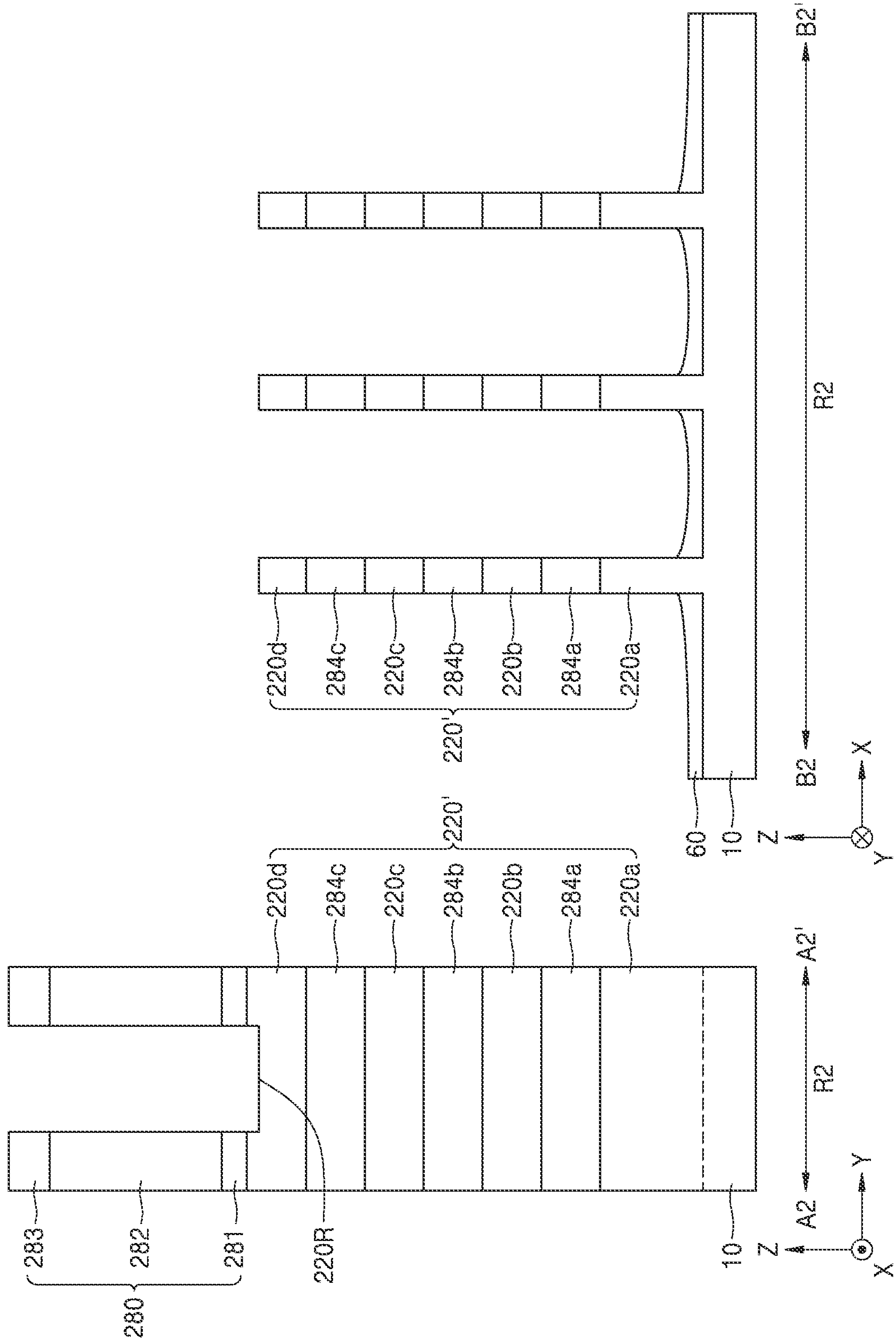
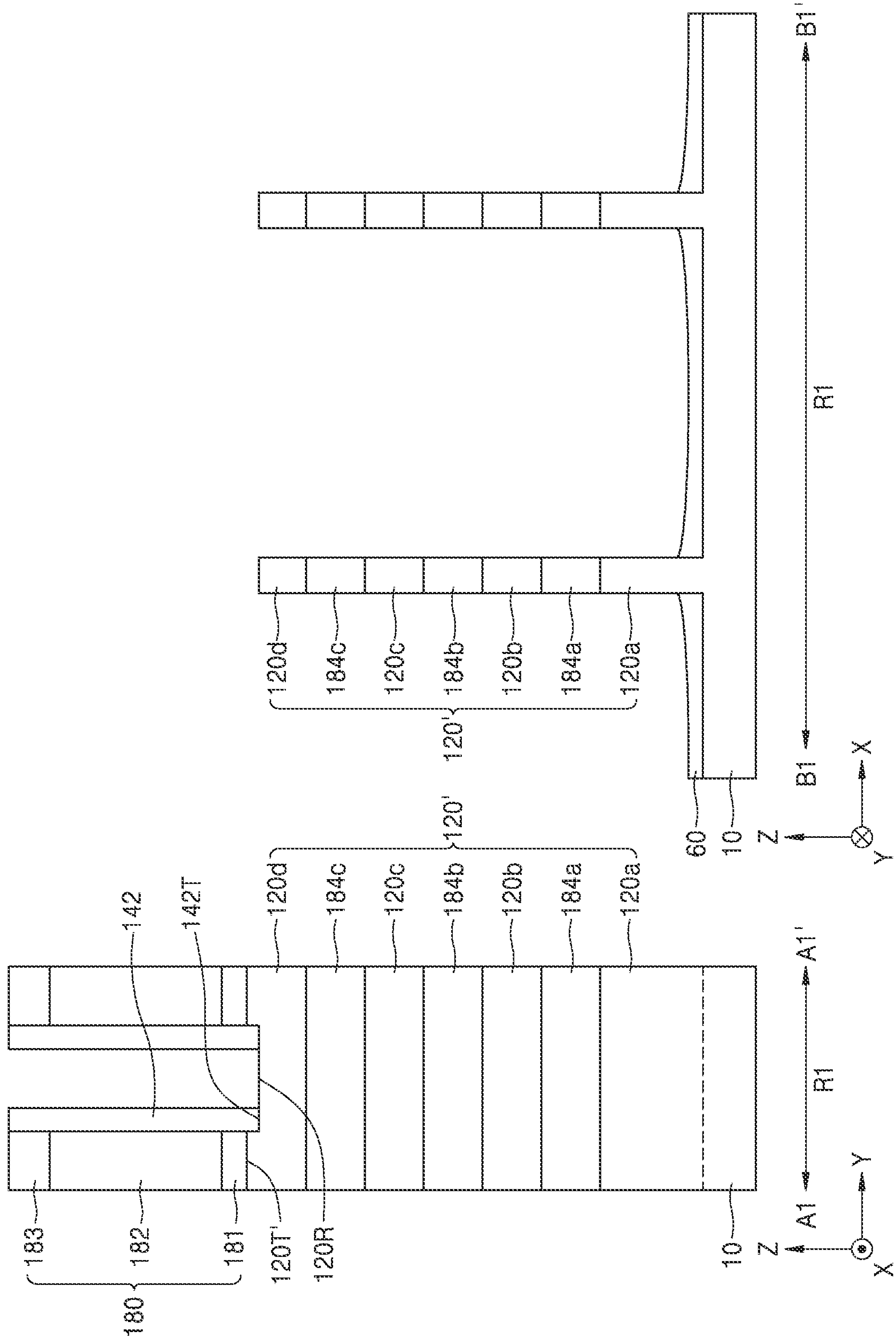

280
283
282
281
220R
10
A2
R2
A2'
220'
220d
284c
220c
284b
220b
284a
220a
Z
Y
X
60
10
B2
B2'
X
Y

FIG. 19A



180
183
182
181
120T'
120R
142
142T
120'
120d
184c
120c
184b
120b
184a
120a
10
60
A1
A1'
R1
B1
B1'
Z
Y
X

FIG. 19B

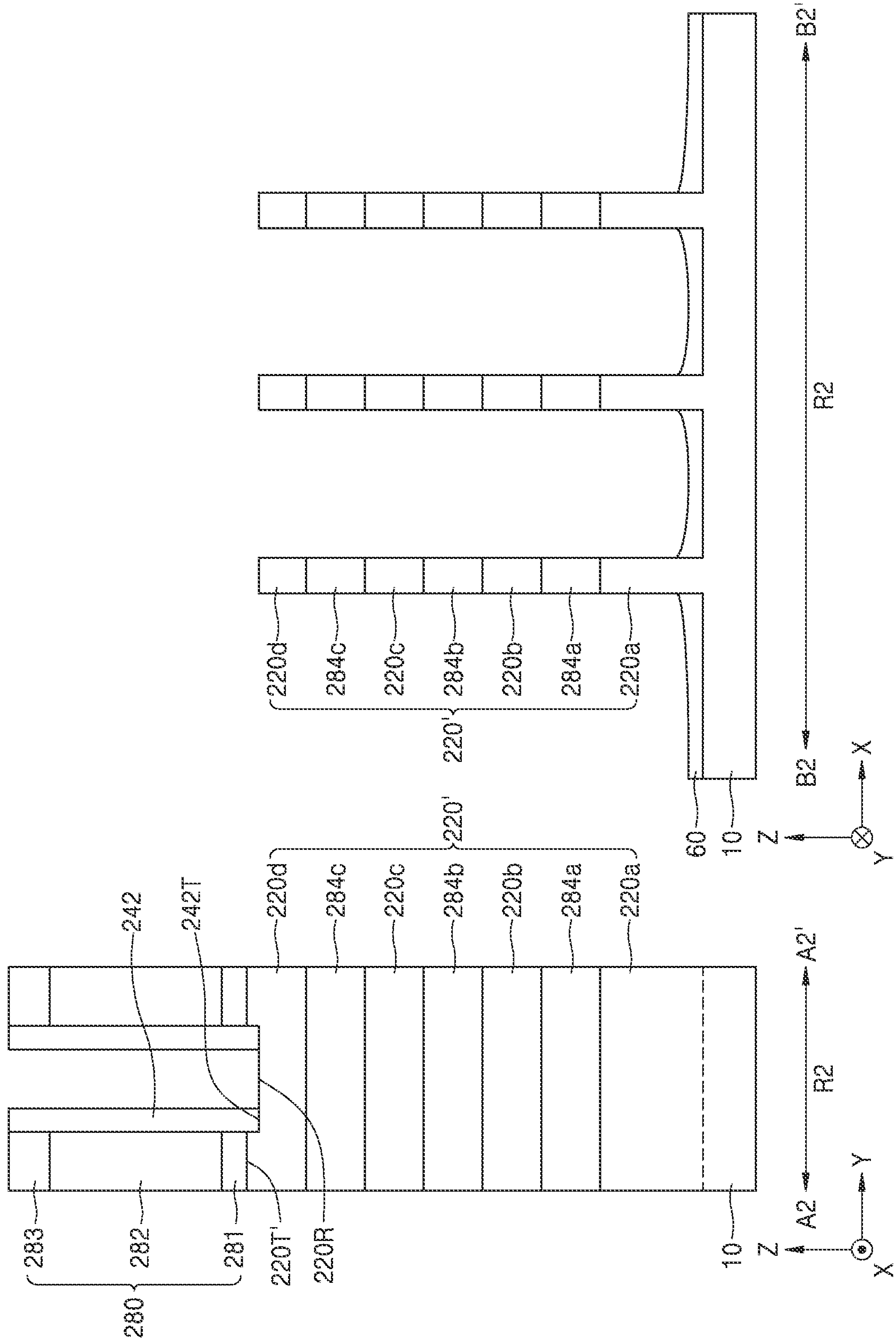
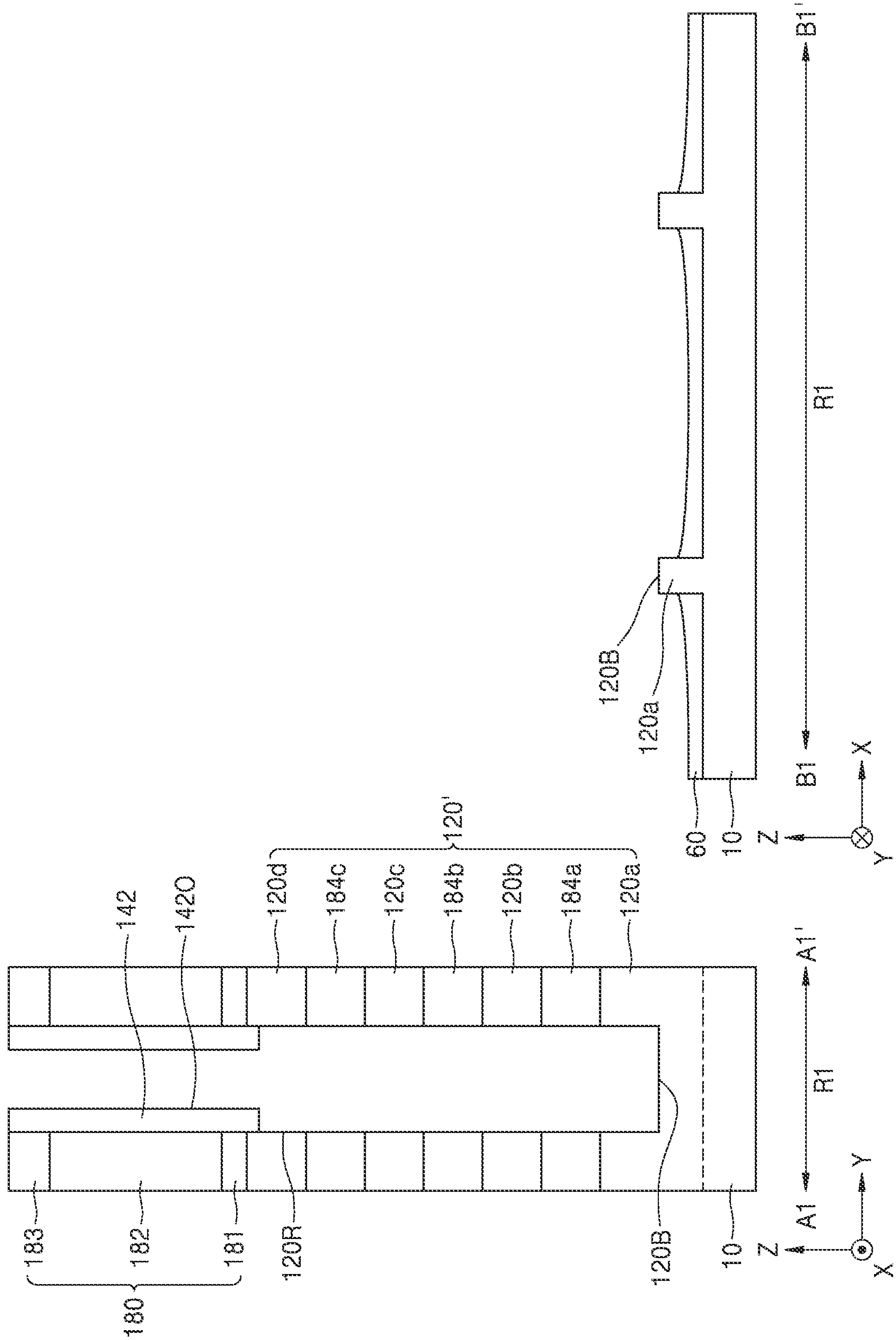
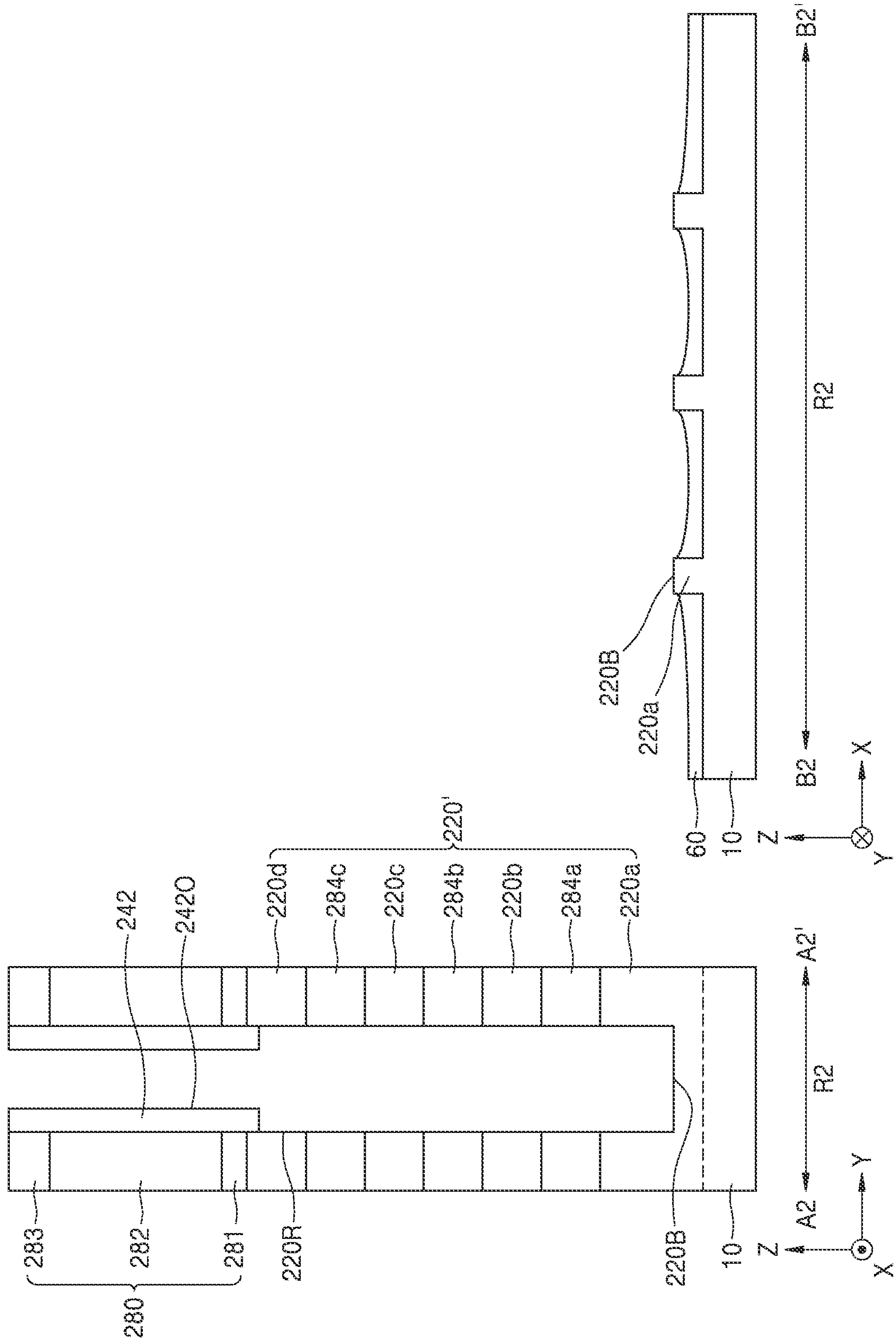

280
283
282
281
220T'
220R
242
242T
220'
220d
284c
220c
284b
220b
284a
220a
10
60
A2
A2'
R2
B2
B2'
Z
X
Y

FIG. 20A



180
183
182
181
120R
120B
10
142
142O
120'
120d
184c
120c
184b
120b
184a
120a
A1
R1
A1'
Z
Y
X
60
120B
120a
B1
R1
B1'

FIG. 20B



283
282
281
280
220R
242
242O
220d
284c
220c
284b
220b
284a
220a
220'
220B
10
A2
R2
A2'
Z
Y
X
60
10
220a
220B
B2
R2
B2'
Z
X
Y

FIG. 21A

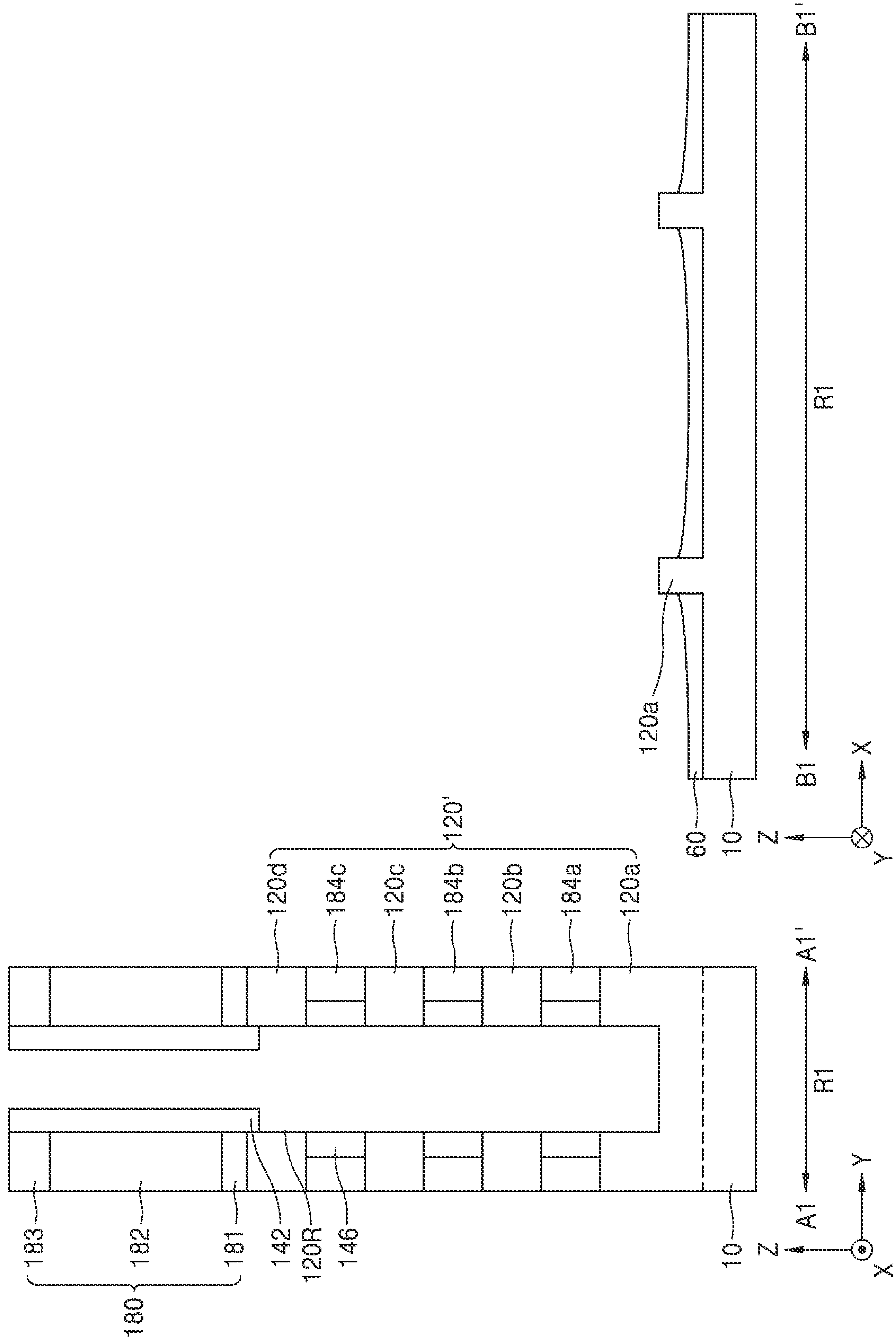
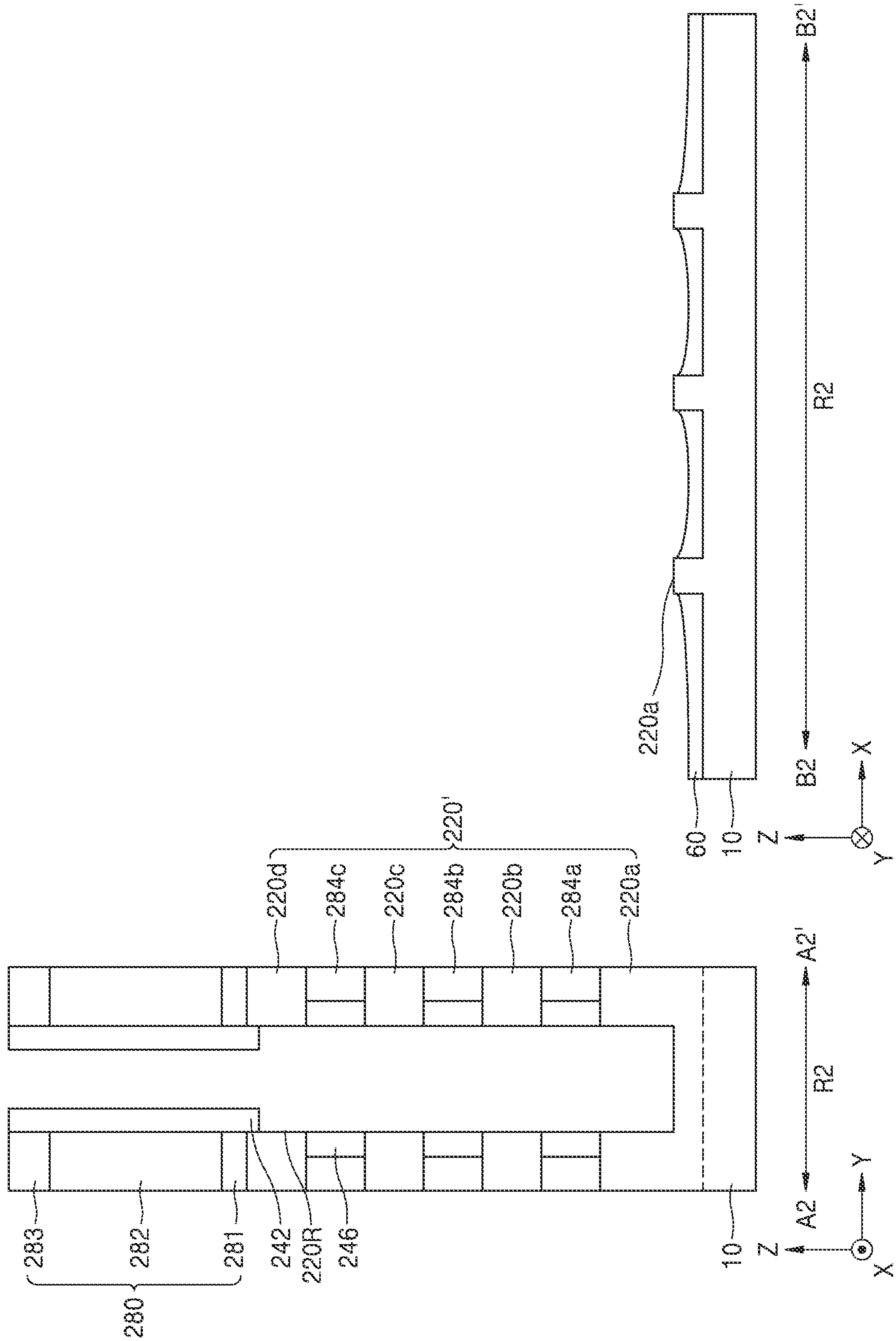

183
182
181
180
142
120R
146
10
A1
R1
A1'
Z
Y
X
120d
184c
120c
184b
120b
184a
120a
120'
60
10
B1
R1
B1'
120a

FIG. 21B



283
282
281
280
242
220R
246
10
A2
A2'
R2
Z
Y
X
220d
284c
220c
284b
220b
284a
220a
220'
60
10
B2
B2'
R2
220a
Z
X
Y

FIG. 22A

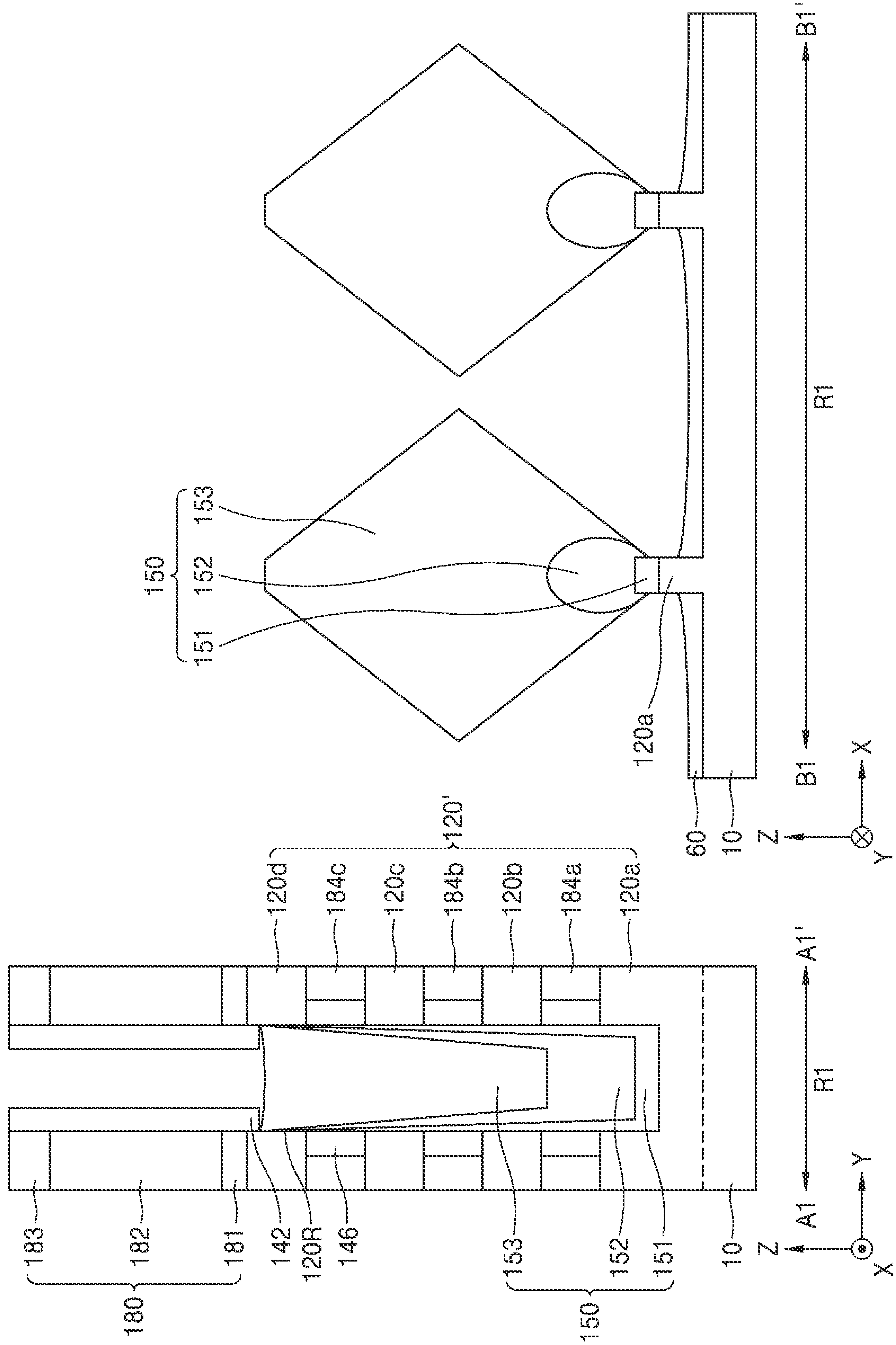

150
151
152
153
120a
60
10
B1
R1
B1'
Z
X
Y
120'
120d
184c
120c
184b
120b
184a
120a
A1
R1
A1'
180
183
182
181
142
120R
146
150
153
152
151
10
Z
Y
X

FIG. 22B

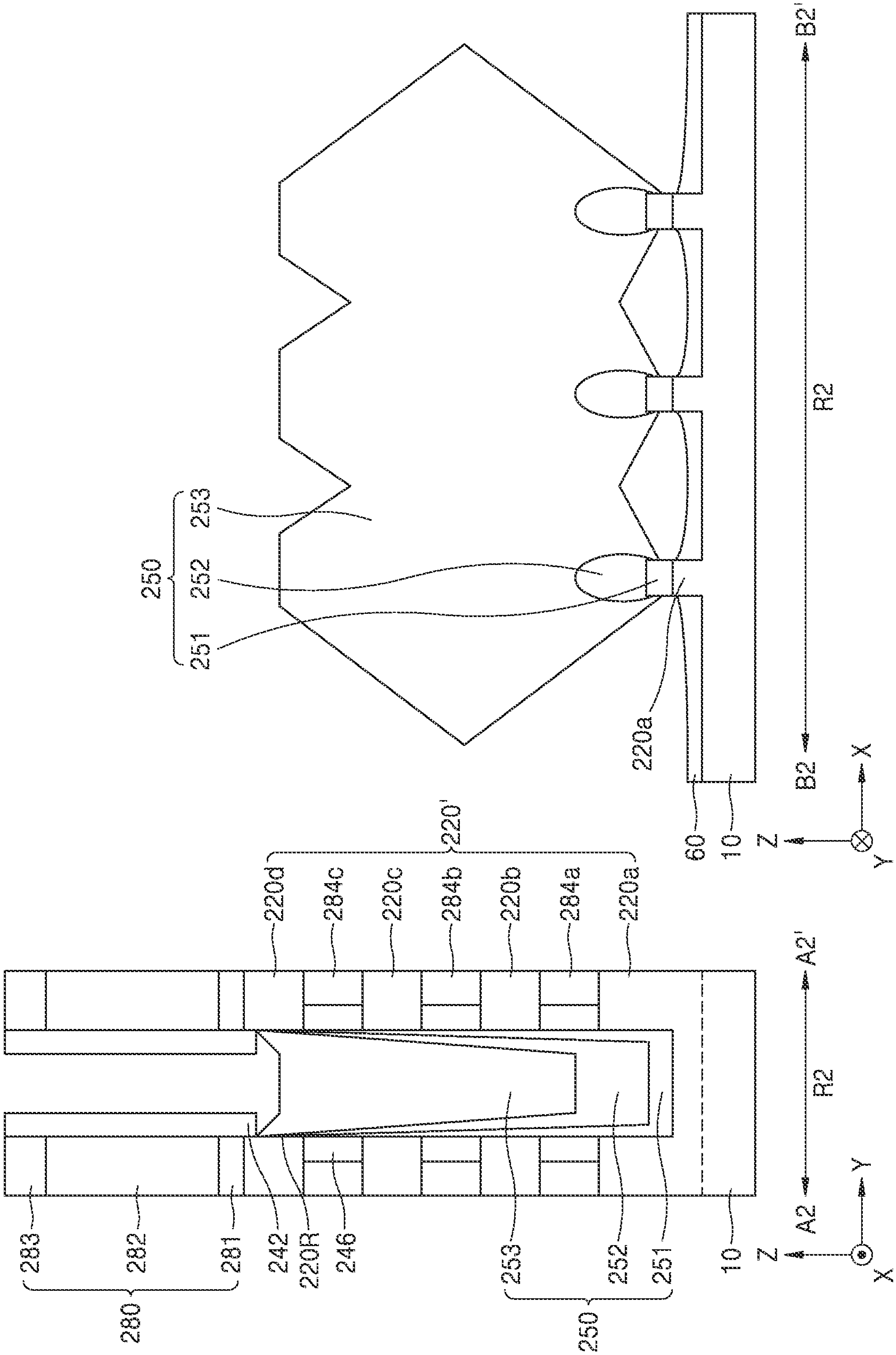

280
283
282
281
242
220R
246
250
253
252
251
10
A2
R2
A2'
Z
Y
X
220'
220d
284c
220c
284b
220b
284a
220a
60
B2
B2'

FIG. 23

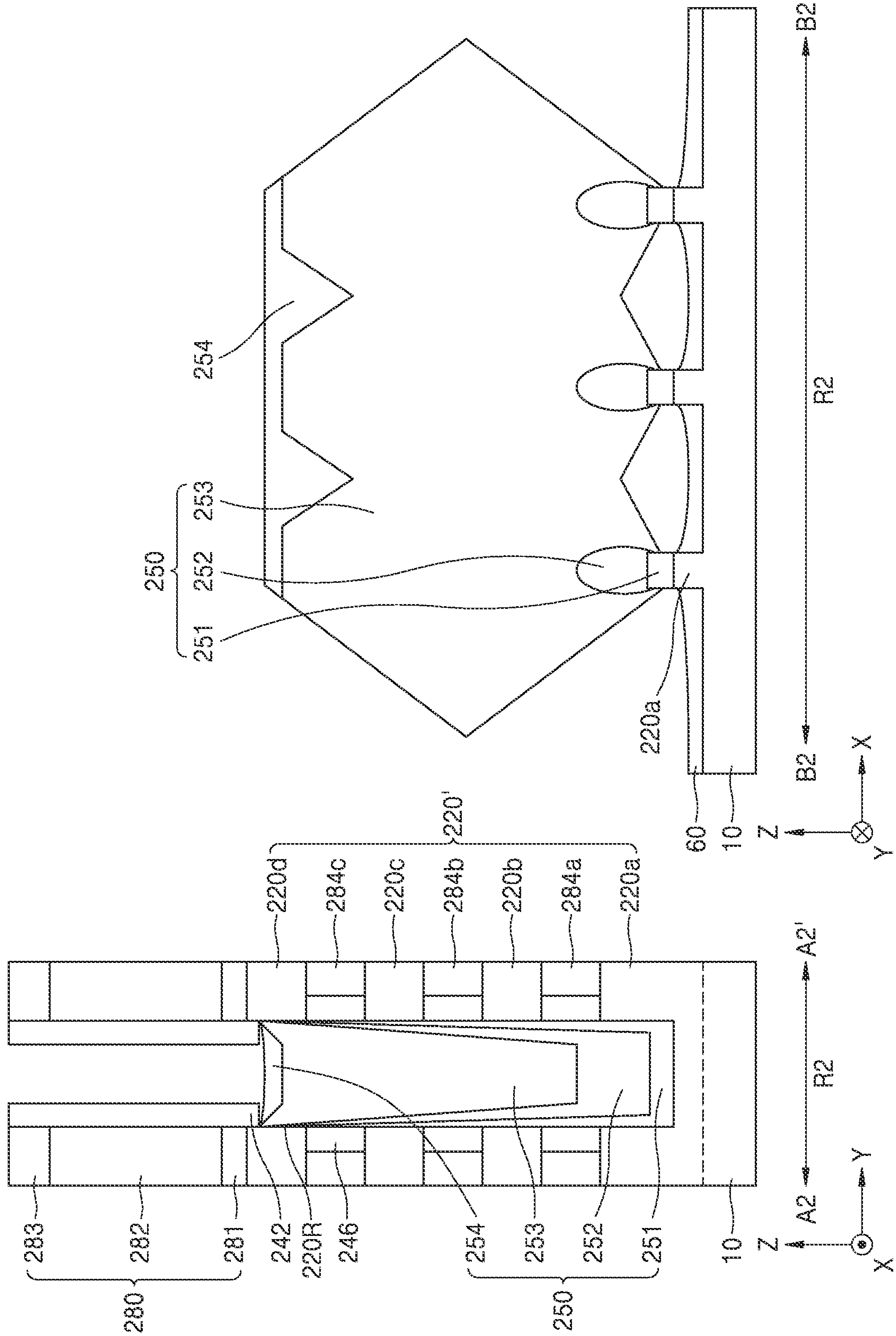

283
282
281
280
242
220R
246
254
253
252
251
250
10
A2
A2'
R2
220d
284c
220c
284b
220b
284a
220a
220'
Z
Y
X
60
220a
B2
B2'
254
253
252
251
250

FIG. 24A

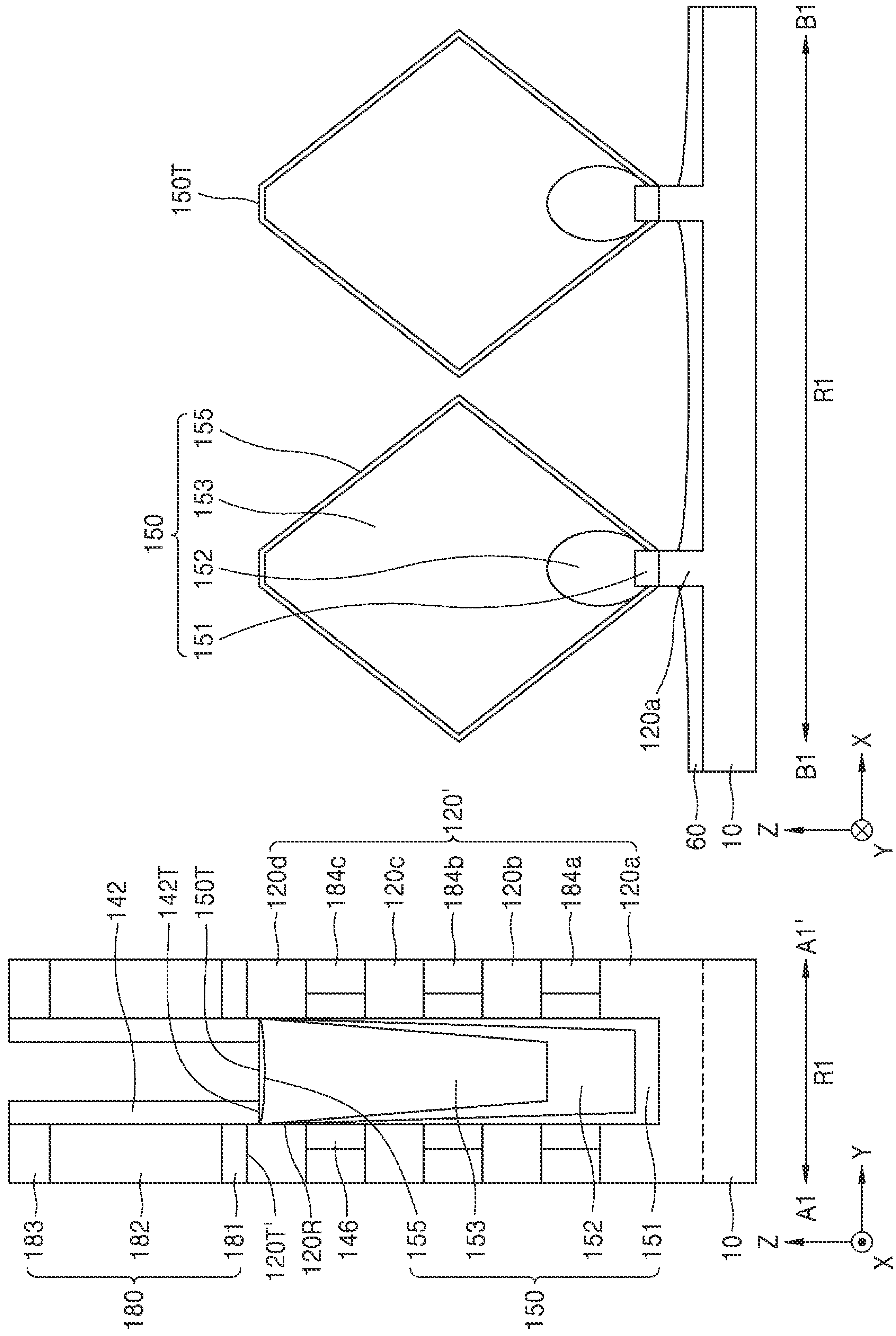

183
182
181
120T'
120R
146
155
153
152
151
10
180
150
142
142T
150T
120d
184c
120c
184b
120b
184a
120a
120'
A1
A1'
R1
Z
Y
X
150T
155
153
152
151
150
120a
60
10
B1
B1'
R1

FIG. 24B

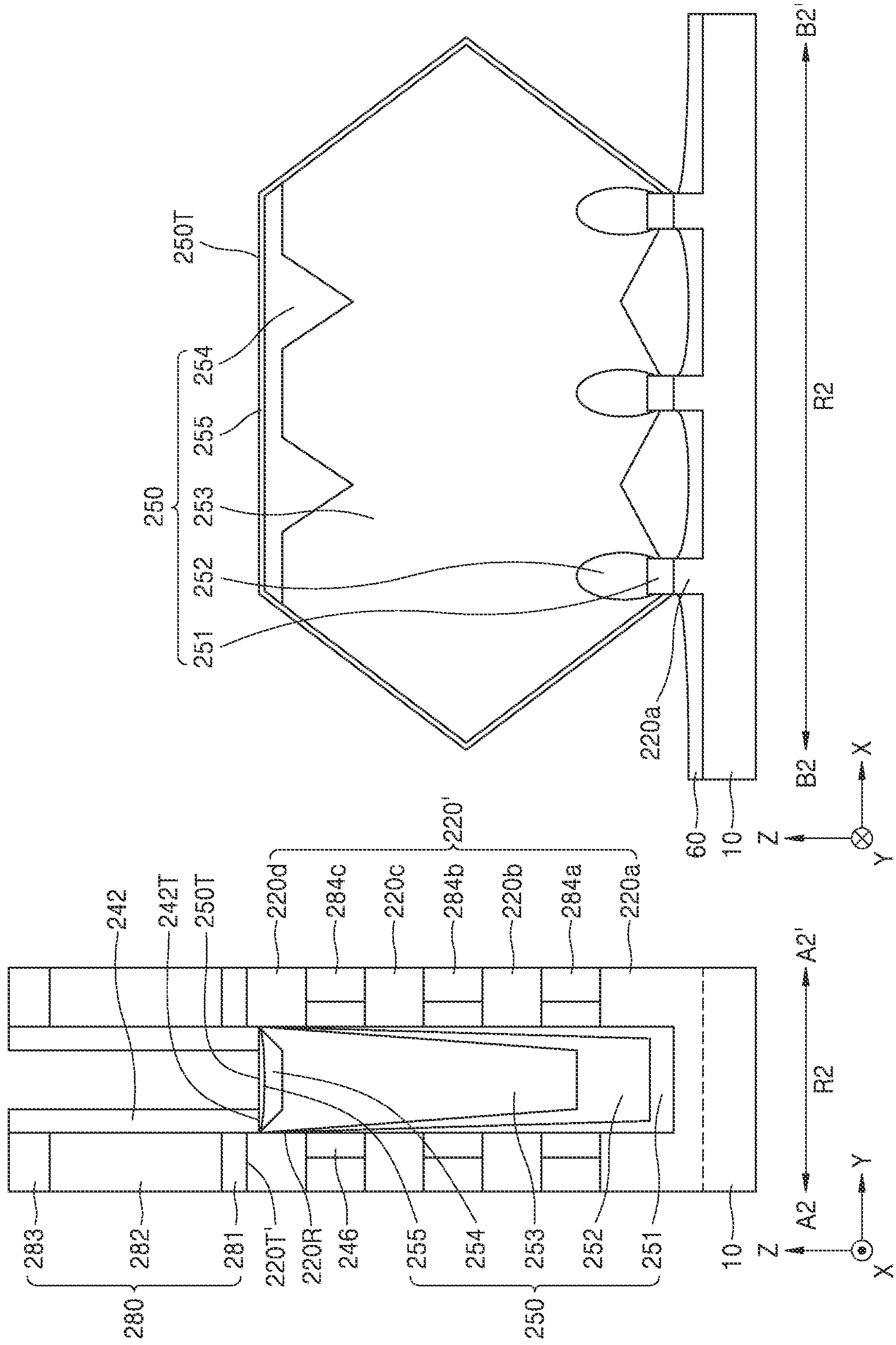

250T
250
251
252
253
255
254
220a
B2
B2'
R2
60
10
Z
X
Y
283
282
281
220T'
220R
246
255
254
253
252
251
10
280
250
242
242T
250T
220d
284c
220c
284b
220b
284a
220a
220'
A2
A2'

FIG. 25A

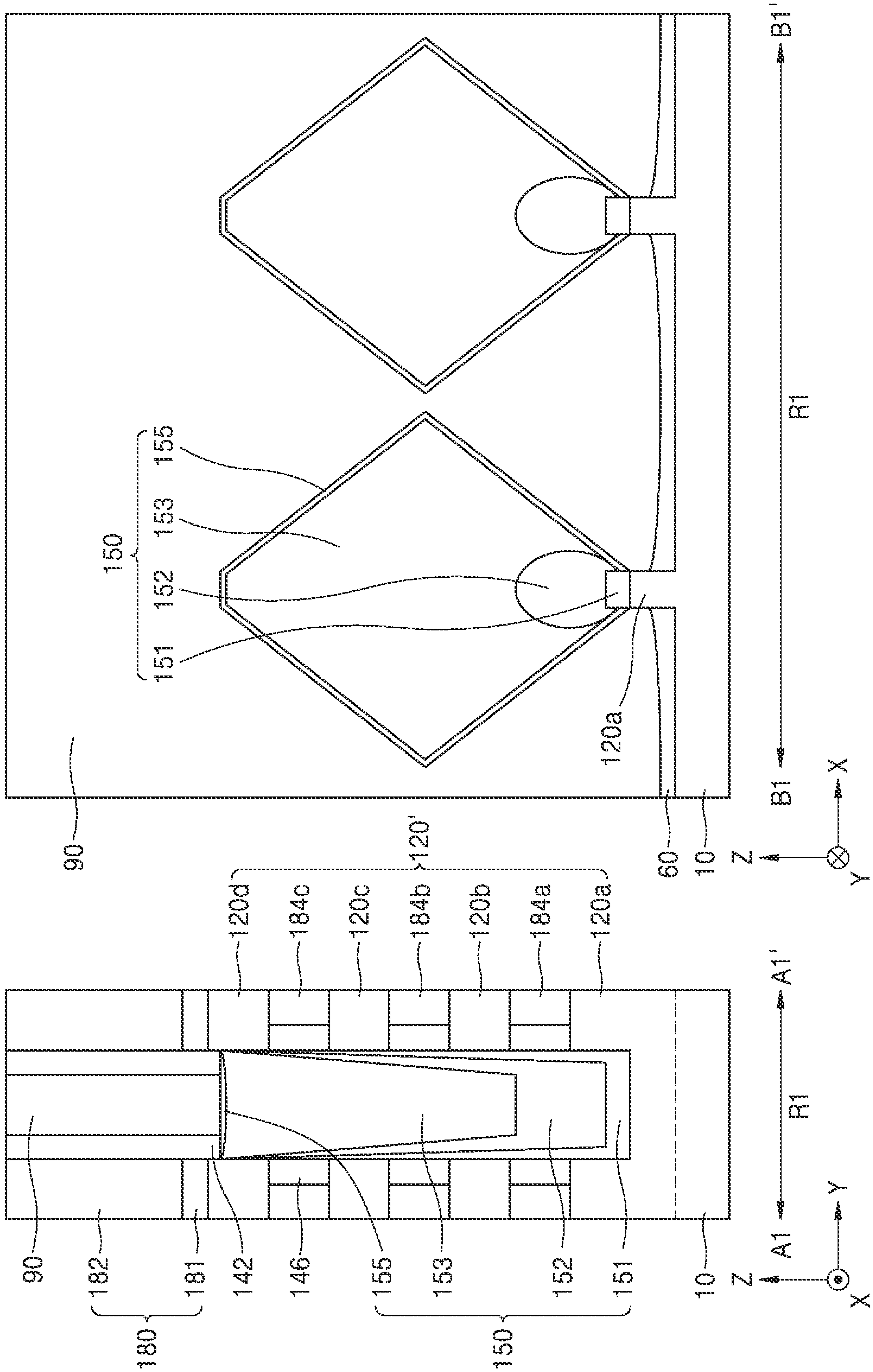
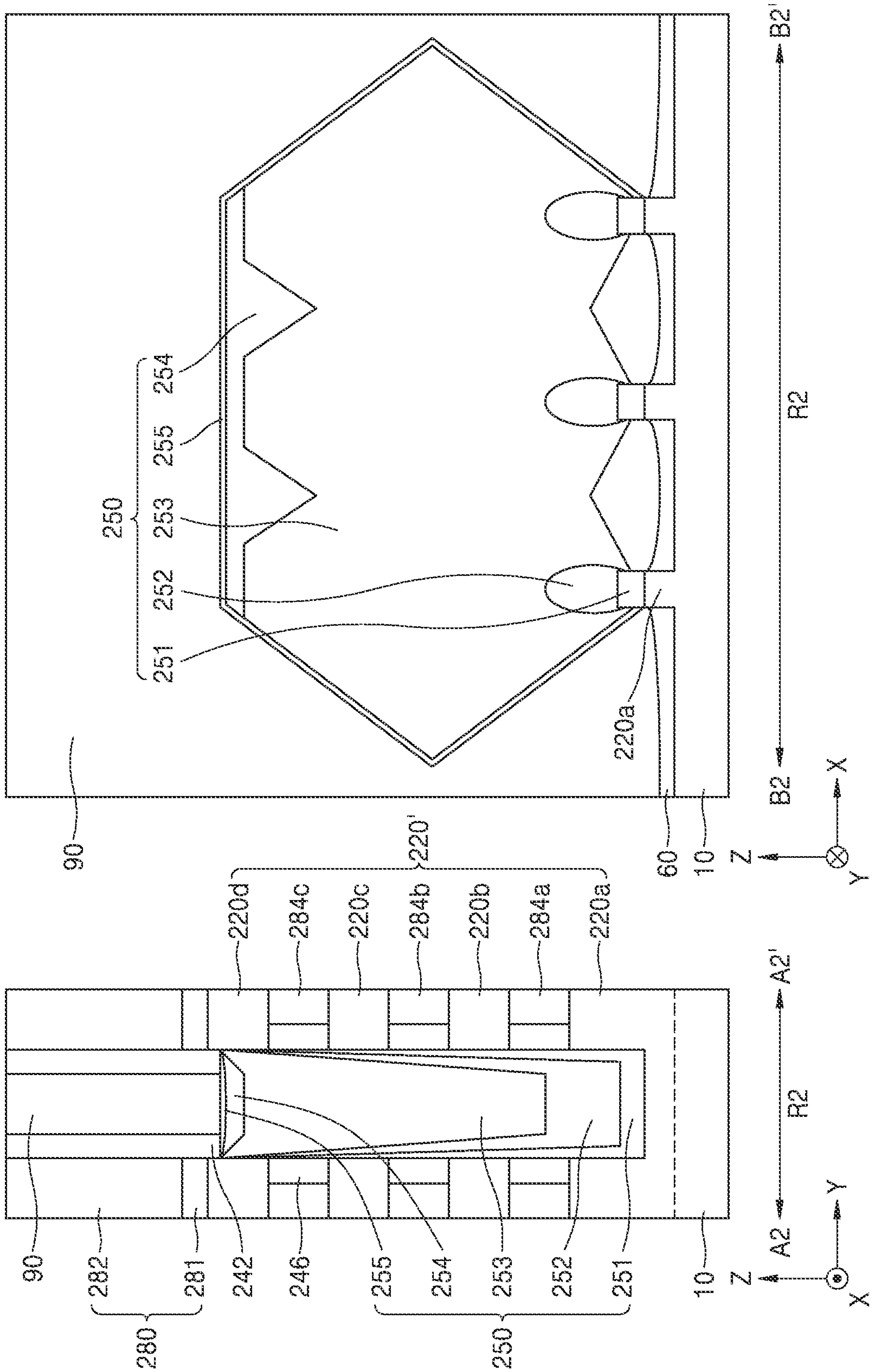

90
150
151
152
153
155
120a
60
10
B1
B1'
R1
Z
X
Y
120'
120d
184c
120c
184b
120b
184a
120a
A1
A1'
182
181
142
146
180

FIG. 25B



90
250
251
252
253
254
255
220a
60
10
B2
B2'
R2
Z
X
Y
220'
220d
284c
220c
284b
220b
284a
220a
A2
A2'
282
281
242
246
280

FIG. 26A

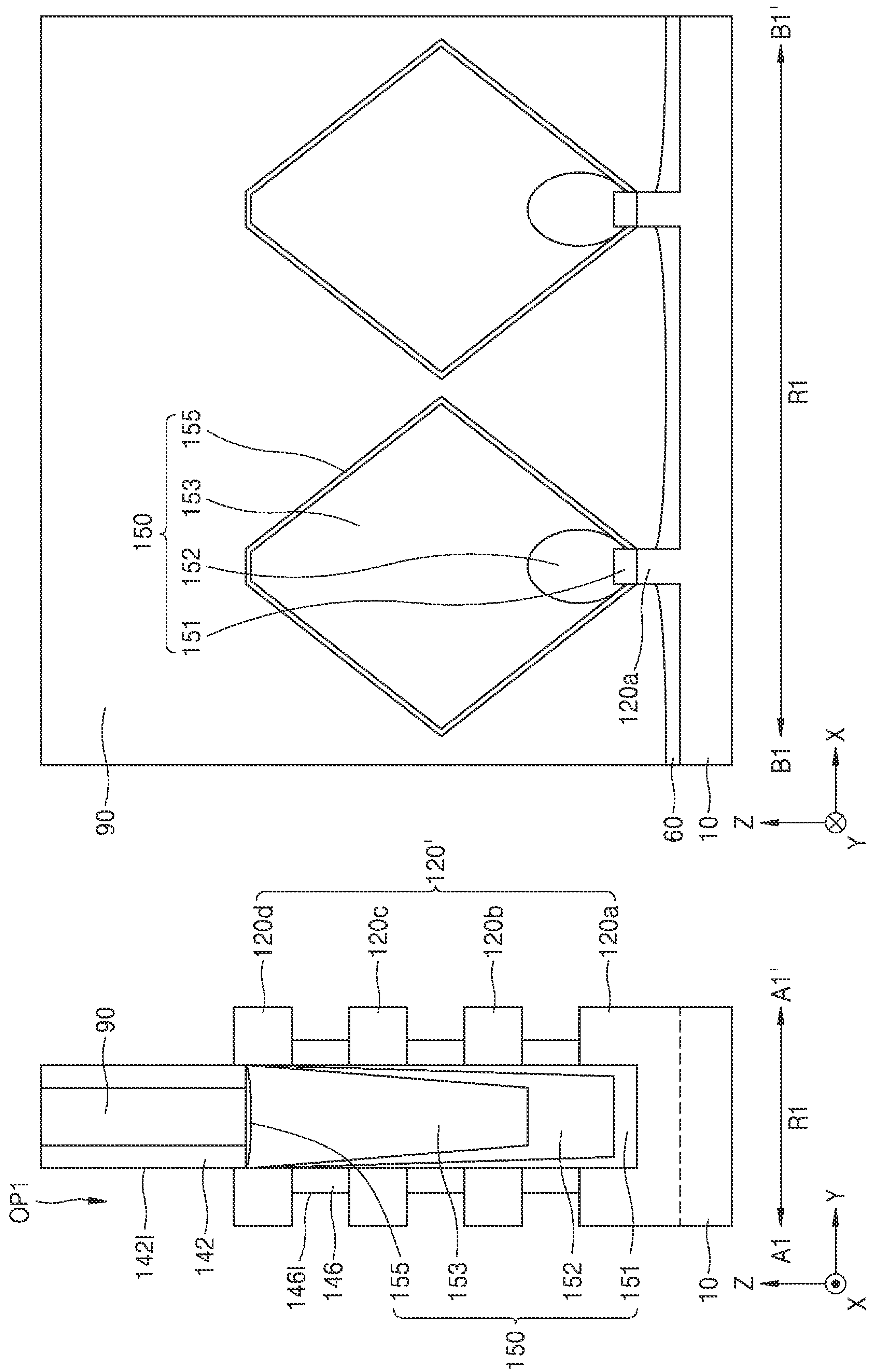

90
150
151
152
153
155
120a
60
10
B1
B1'
R1
Z
X
Y
OP1
142l
142
146l
146
120'
120a
120b
120c
120d
A1
A1'

FIG. 26B

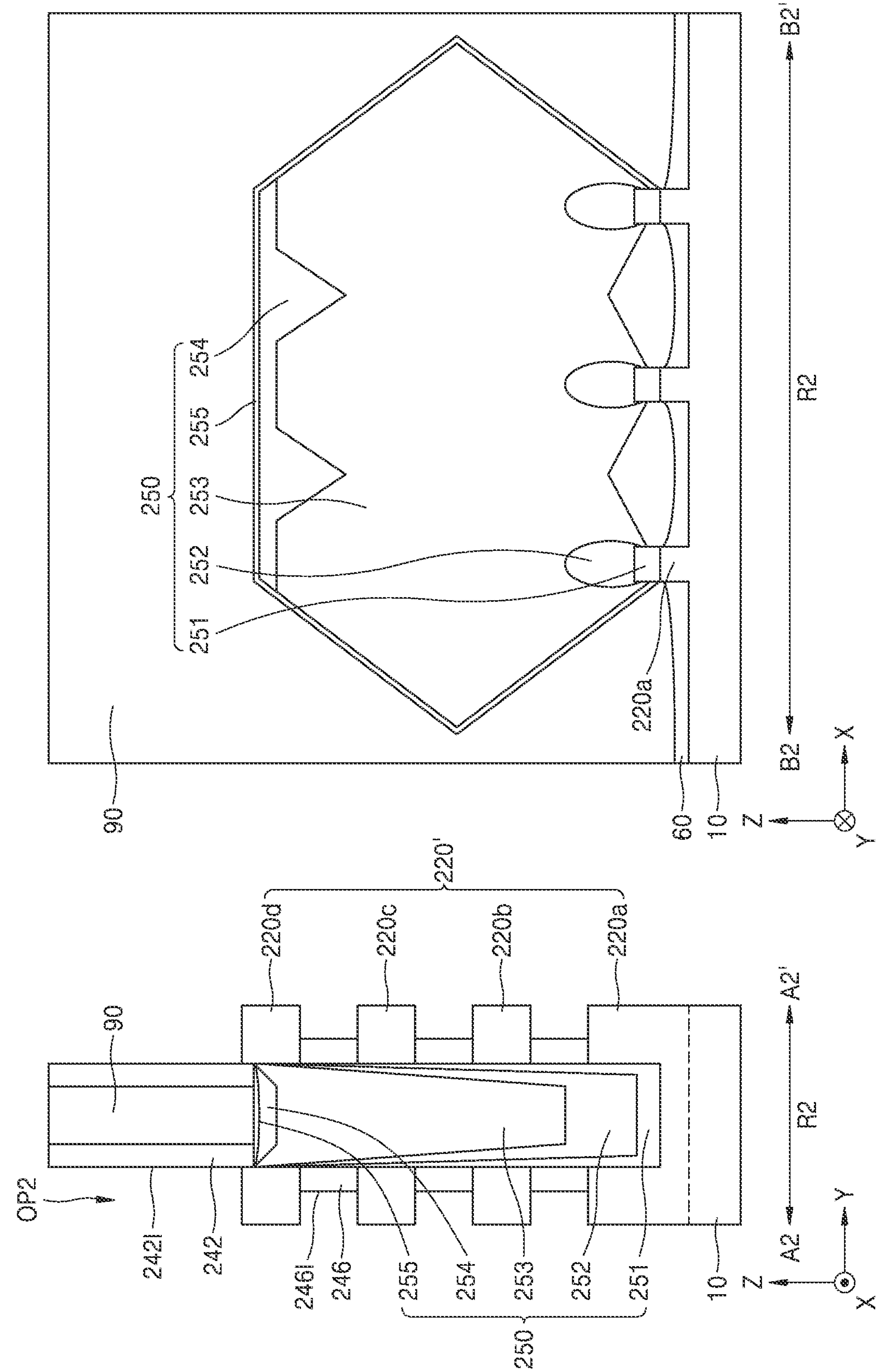
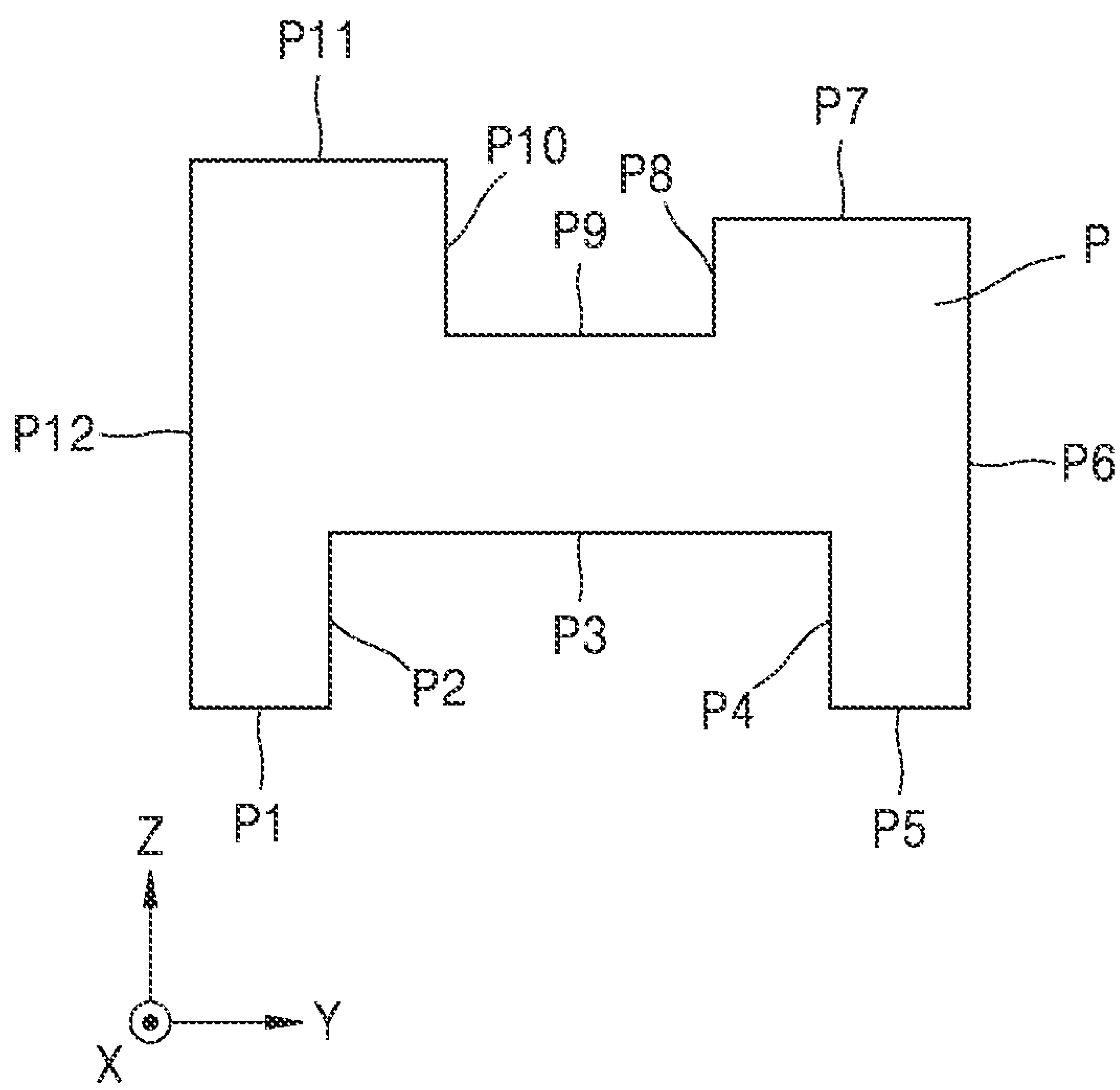

90
60
10
220a
251
252
253
255
254
250
B2
B2'
R2
Z
X
Y
OP2
242l
242
246l
246
255
254
253
252
251
250
10
A2
A2'
R2
220a
220b
220c
220d
220'
90
Z
Y
X

FIG. 27



SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is a Continuation Application of U.S. patent application Ser. No. 16/806,629 filed Mar. 2, 2020, which is based on and claims priority under 35 U.S.C. § 119 to Korean Patent Application Nos. 10-2019-0089217 filed on Jul. 23, 2019, in the Korean Intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

BACKGROUND

1. Field

The disclosure relates to a semiconductor device, and more particularly, to a semiconductor device including a transistor and a method of manufacturing the same.

2. Description of Related Art

Fin field effect transistors (finFETs) including fin-shaped channels have been developed to achieve high integration, high operation speed, and low power consumption of semiconductor devices. Recently, gate-all-around field effect transistors (GAAFETs) including a plurality of channels spaced in the vertical direction and multi-bridge channel field effect transistors (MBCFETs) have been developed to achieve higher integration, faster operation speed, and lower power consumption.

SUMMARY

The disclosure provides a semiconductor device having excellent performance without defects.

In accordance with an aspect of the disclosure, a semiconductor device includes a substrate; a fin structure on the substrate; a gate structure on the fin structure; a gate spacer on at least one side surface of the gate structure; and a source/drain structure on the fin structure, wherein a topmost portion of a bottom surface of the gate spacer is lower than a topmost portion of a top surface of the fin structure, and a topmost portion of a top surface of the source/drain structure is lower than the topmost portion of the top surface of the fin structure.

The gate spacer may include an inner side surface contacting the gate structure and an outer side surface opposite to the inner side surface, and the source/drain structure may include a portion such that a distance from the portion of the source/drain structure to the gate structure in a horizontal direction is smaller than a distance from the outer side surface of the gate spacer to the gate structure in the horizontal direction.

The topmost portion of the bottom surface of the gate spacer may be higher than a bottommost portion of the top surface of the fin structure.

The source/drain structure may be doped with a p-type dopant.

The fin structure may include a plurality of channels separated from each other in a vertical direction, the topmost portion of the bottom surface of the gate spacer may be lower than a topmost portion of a top surface of a topmost channel from among the plurality of channels, and the topmost portion of the top surface of the source/drain structure may be lower than the topmost portion of the top surface of the topmost channel.

In accordance with an aspect of the disclosure, a semiconductor device includes a substrate comprising a first region and a second region; a first fin structure on the first region; a second fin structure on the second region; a first gate structure on the first fin structure; a second gate structure on the second fin structure; a first gate spacer on at least one side surface of the first gate structure; a second gate spacer on at least one side surface of the second gate structure; a first source/drain structure on the first fin structure; and a second source/drain structure on the second fin structure, wherein a topmost portion of a bottom surface of the first gate spacer is lower than a topmost portion of a top surface of the first fin structure, and wherein a topmost portion of a top surface of the first source/drain structure is lower than the topmost portion of the top surface of the first fin structure.

The first source/drain structure may include a first source/drain layer and a first capping layer directly on the first source/drain layer, and the second source/drain structure may include a second source/drain layer, a third source/drain layer on the second source/drain layer, and a second capping layer on the third source/drain layer.

A Si concentration of the first source/drain layer may be lower than a Si concentration of the first capping layer, and a Si concentration of the second source/drain layer may be lower than a Si concentration of the second capping layer.

A Si concentration of the third source/drain layer may be lower than a Si concentration of the second source/drain layer.

The first source/drain layer and the second source/drain layer may include a substantially same first composition, and the first capping layer and the second capping layer may include a substantially same second composition.

The first source/drain layer, the second source/drain layer, and the third source/drain layer may include SiGe.

The first source/drain layer, the second source/drain layer, and the third source/drain layer may include a p-type dopant.

A distance from the topmost portion of the top surface of the first fin structure to a bottommost portion of the top surface of the first fin structure in a vertical direction may be less than a distance from a topmost portion of a top surface of the second fin structure to a bottommost portion of the top surface of the second fin structure in the vertical direction.

A topmost portion of a bottom surface of the second gate spacer may be lower than a bottommost portion of a top surface of the second fin structure.

A height of a topmost portion of a bottom surface of the second gate spacer may be greater than or equal to a height of a bottommost portion of a top surface of the second fin structure.

In accordance with an aspect of the disclosure, a semiconductor device includes a substrate comprising a first region and a second region; a plurality of first fin structures on the first region; a plurality of second fin structures on the second region; a plurality of first gate structures, each first gate structure from among the plurality of first gate structures being on a respective first fin structure from among the plurality of first fin structures; a second gate structure on the plurality of second fin structures; a plurality of first gate spacers, each first gate spacer from among the plurality of first gate spacers being on side surfaces of a respective first gate structure from among the plurality of first gate structures; a second gate spacer on side surfaces of the second gate structure; a plurality of first source/drain structures, each first source/drain structure being on a respective first fin structure from among the plurality of first fin structures; and a second source/drain structure on the plurality of second fin structures, wherein a topmost portion of a bottom surface of each first gate spacer from among the plurality of first gate spacers is lower than a topmost portion of a top surface of a respective first fin structure from among the plurality of first fin structures, and a topmost portion of a top surface of each first source/drain structure from among the plurality of first source/drain structures is lower than a topmost portion of a top surface of a respective first fin structure from among the plurality of first fin structures.

The plurality of first source/drain structures may be separated from one another, and the second source/drain structure may contact all of the plurality of second fin structures.

A pitch between adjacent first fin structures from among the plurality of first fin structures may be greater than a pitch between adjacent second fin structures from among the plurality of second fin structures.

A length of each first source/drain structure from among the plurality of first source/drain structures in a vertical direction may be less than a length of the second source/drain structure in the vertical direction.

Each first source/drain structure from among the plurality of first source/drain structures may include a first predetermined number of layers, and the second source/drain structure may include a second predetermined number of layers, the second predetermined number being greater than the first predetermined number.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other aspects, features, and advantages of certain embodiments of the disclosure will be more apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

FIG. **1**A is a plan view of a semiconductor device according to an embodiment;

FIG. **1**B is a cross-sectional view of a semiconductor device according to an embodiment, taken along lines A**1**-A**1**' and B**1**-B**1**' of FIG. **1**A;

FIG. **1**C is a cross-sectional view of a semiconductor device according to an embodiment, taken along lines A**2**-A**2**' and B**2**-B**2**' of FIG. **1**A;

FIG. **1**D is a cross-sectional view of the semiconductor device according to an embodiment, taken along lines C**1**-C**1**' and C**2**-C**2**' of FIG. **1**A;

FIG. **2** is a cross-sectional view of a semiconductor device according to an embodiment, taken along the lines A**1**-A**1**' and B**1**-B**1**' of FIG. **1**A;

FIG. **3** is a cross-sectional view of a semiconductor device according to an embodiment, taken along the lines A**2**-A**2**' and B**2**-B**2**' of FIG. **1**A;

FIG. **4**A is a cross-sectional view of a semiconductor device according to an embodiment, taken along the lines A**1**-A**1**' and B**1**-B**1**' of FIG. **1**A;

FIG. **4**B is a cross-sectional view of the semiconductor device according to an embodiment, taken along the lines A**2**-A**2**' and B**2**-B**2**' of FIG. **1**A;

FIGS. **5**A to **14**B are diagrams showing a method of manufacturing a semiconductor device according to an embodiment;

FIGS. **15**A to **26**B are diagrams showing a method of manufacturing a semiconductor device according to an embodiment; and

FIG. **27** is a conceptual diagram for describing terms described in the disclosure.

DETAILED DESCRIPTION OF EMBODIMENTS

FIG. **27** is a conceptual diagram for describing terms described in the disclosure.

Referring to FIG. **27**, in this specification, a vertical direction refers to a Z direction indicated throughout the drawings. Z coordinates may also be referred to as heights. The expression that a first point is higher than a second point means that the Z coordinate of the first point is greater than the Z coordinate of the second point, regardless of the X and Y coordinates of the first point and the second point, and the expression that a first point is lower than a second point means that the Z coordinate of the first point is smaller than the Z coordinate of the second point, regardless of the X and Y coordinates of the first point and the second point. The expression that a first point is at the same height as a second point means that the Z coordinate of the first point and the Z coordinate of the second point are the same regardless of the X and Y coordinates of the first point and the second point.

In the conceptual example shown in FIG. **27**, the bottom surface of an object P may include first to fifth surfaces P**1** to P**5**. The top surface of the object P may include seventh to eleventh surfaces P**7** to P**11**. The third surface P**3** may be referred to as the topmost portion of the bottom surface of the object P, and the first surface P**1** and the fifth surface P**5** may be referred to as bottommost portions of the bottom surface of the object P. The eleventh surface P**11** may be referred to as the topmost portion of the top surface of the object P, and the ninth surface P**9** may be referred to as the bottommost portion of the top surface of the object P. A sixth surface P**6** and a twelfth surface **12** may be referred to as side surfaces of the object P. Side surfaces are not necessarily parallel to the vertical direction and may be defined as surfaces interconnecting the top surface with the bottom surface.

FIG. **1**A is a plan view of a semiconductor device according to example embodiments. FIG. **1**B is a cross-sectional view of a semiconductor device **1000** according to an embodiment, taken along lines A**1**-A**1**' and B**1**-B**1**' of FIG. **1**A. FIG. **1**C is a cross-sectional view of the semiconductor device **1000** according to an embodiment, taken along lines A**2**-A**2**' and B**2**-B**2**' of FIG. **1**A. FIG. **1**D is a cross-sectional view of the semiconductor device **1000** according to an embodiment, taken along lines C**1**-C**1**' and C**2**-C**2**' of FIG. **1**A.

Referring to FIGS. **1**A to **1**D, the semiconductor device **1000** may include a substrate **10**, a first fin structure **120** on a first region R**1** of the substrate **10**, and a first gate structure **130** on the first fin structure **120**, first gate spacers **142** on side surfaces of the first gate structure **130**, and a first source/drain structure **150** on the first fin structure **120**. In some embodiments, the semiconductor device **1000** may include a second fin structure **220** on a second region R**2** of the substrate **10**, a second gate structure **230** on the second fin structure **220**, second gate spacers **242** on side surfaces of the second gate structure **230**, and a second source/drain structure **250** on the second fin structure **220**.

In some embodiments, the semiconductor device **1000** may include the substrate **10**, a plurality of first fin structures **120** on the first region R**1** of the substrate **10**, a plurality of second fin structures **220** on the second region R**2** of the substrate **10**, a plurality of first gate structures **130** respectively located on the first fin structures **120**, a second gate structure **230** located on the second fin structures **220**, a plurality of first gate spacers **142** respectively located on side surfaces of the first gate structures **130**, second gate spacers **242** located on side surfaces of the second gate structure **230**, a plurality of first source/drain structures **150** respectively located on the first fin structures **120**, and a second source/drain structure **250** located on the second fin structures **220**.

The substrate **10** may include the first region R**1** and the second region R**2**. In some embodiments, the first region R**1** and the second region R**2** may also be referred to as a static RAM (SRAM) region and a logic region, respectively, but are not limited thereto. The substrate **10** may include a semiconductor material like a Group IV semiconductor material, a Group III-V semiconductor material, a Group II-VI semiconductor material, or a combination thereof. The Group IV semiconductor material may include, for example, silicon (Si), germanium (Ge), or silicon-germanium (SiGe). The Group III-V semiconductor material may include, for example, gallium arsenide (GaAs), indium phosphorus (InP), gallium phosphorus (GaP), indium arsenic (InAs), indium antimony (InSb), or indium gallium arsenide (InGaAs). The Group II-VI semiconductor material may include, for example, zinc telluride (ZnTe) or cadmium sulfide (CdS). The substrate **10** may include a bulk wafer or an epitaxial layer.

The first fin structure **120** and the second fin structure **220** may be located on the top surface of the substrate **10**. In some embodiments, first fin structure **120** and second fin structure **220** may extend in the Y direction as shown in FIGS. **1B-1D**. In some embodiments, the first fin structures **120** may extend in the Y direction parallel to one another and may be apart (i.e., separated) from one another in the X direction. The second fin structures **220** may extend in the Y direction parallel to one another and may be apart (i.e., separated) from one another in the X direction. In some embodiments, a horizontal direction (e.g., the X direction) pitch D**1** between the first fin structures **120** may be greater than a horizontal direction (e.g., the X direction) pitch D**2** between the second fin structures **220**. The pitch may also be referred to as a repeating distance. For example, the horizontal direction (e.g., the X direction) pitch D**1** between the first fin structures **120** may be about twice the horizontal direction (e.g., the X direction) pitch D**2** between the second fin structures **220**.

Each of the first fin structures **120** and the second fin structures **220** may be formed from the substrate **10**, an epitaxial layer, or a combination thereof. Each of the first fin structures **120** and the second fin structures **220** may include a semiconductor material. In some embodiments, each of the first fin structures **120** and the second fin structures **220** may include the same material as that of the substrate **10**.

The topmost portion **120**T of the top surface of the first fin structure **120** may contact the first gate structure **130**. The bottommost portion **120**B of the top surface of the first fin structure **120** may contact the first source/drain structure **150** as shown in FIG. **1B**. The topmost portion **220**T of the top surface of the first fin structure **220** may contact the second gate structure **230**. The bottommost portion **220**B of the top surface of the first fin structure **220** may contact the second source/drain structure **250** as shown in FIG. **1C**. In some embodiments, a distance D**3** from the topmost portion **120**T of the top surface of the first fin structure **120** to the bottommost portion **120**B of the top surface of the first fin structure **120** in the vertical direction Z may be less than a distance D**4** from the topmost portion **220**T of the top surface of the second fin structure **220** to the bottommost portion **220**B of the top surface of the second fin structure **220**, and thus, the first source/drain structure **150** may be smaller than the second source/drain structure **250** in the vertical direction Z.

In some embodiments, the semiconductor device **1000** may further include a device isolation layer **60** on the top surface of the substrate **10**. The device isolation layer **60** may surround side surfaces of the lower portion of the first fin structure **120** and side surfaces of the lower portion of the second fin structure **220**. The device isolation layer **60** may include a single layer or a plurality of layers. The device isolation layer **60** may include, for example, silicon oxide, silicon nitride, or a combination thereof.

In some embodiments, the semiconductor device **1000** may further include first fin spacers **144** on the side surfaces of the first fin structure **120** and second fin spacers **244** on side surfaces of the second fin structure **220**. For example, the first fin spacers **144** may be located on both side surfaces of the first fin structure **120** apart from each other in the X direction as shown in FIG. **1B**, and the second fin spacers **244** may be located on both side surfaces of the second fin structure **220** apart from each other in the X direction as shown in FIG. **1C**. The first fin spacer **144** and the second fin spacer **244** may include, for example, silicon oxide, silicon nitride, or a combination thereof.

In some embodiments, the first gate structure **130** and the second gate structure **230** may extend in the X direction. The first gate structure **130** may be located on the topmost portion **120**T of top surface of the first fin structure **120** as shown in FIG. **1B**, and the second gate structure **230** may be located on the topmost portion **220**T of top surface of the second fin structure **220** as shown in FIG. **1C**. The first gate structure **130** may be located on the top surface of the first fin structure **120** and both side surfaces of the first fin structure **120** apart from each other in the X direction, and the second gate structure **230** may be located on the top surface of the second fin structure **220** and both side surfaces of the second fin structure **220** apart from each other in the X direction.

In some embodiments, the first gate structures **130** are respectively located on the first fin structures **120**, whereas a single second gate structure **230** may be located on all of the second fin structures **220**. In other words, the single second gate structure **230** may extend throughout and across all of the second fin structures **220**. In an embodiment, a plurality of second gate structures **230** may instead be respectively located on the second fin structures **220**. Although FIG. **1A** shows that the single second gate structure **230** extends throughout three second fin structures **220**, the single second gate structure **230** may contact fewer or more than three second fin structures **220**.

The first gate structure **130** may include a first gate insulation layer **131** on the first fin structure **120** and a first gate electrode layer **132** on the first gate insulation layer **131**. Also, the second gate structure **230** may include a second gate insulation layer **231** on the second fin structure **220** and a second gate electrode layer **232** on the second gate insulation layer **231**. The first gate insulation layer **131** and the second gate insulation layer **231** may each include a high-k layer (i.e., a high-dielectric constant layer). The high-k layer may include a high-k material having a higher dielectric constant than that of silicon oxide. The high-k material may include, for example, hafnium oxide, lanthanum oxide, zircon oxide, tantalum oxide, or a combination thereof.

In some embodiments, the first gate insulation layer **131** may further include an interface layer between the high-k layer of the first gate insulation layer **131** and the first fin structure **120**, and the second gate insulation layer **231** may further include an interface layer between the high-k layer of the second gate insulation layer **231** and the second fin structure **220**. The interface layers of the first gate insulation layer **131** and the second gate insulation layer **231** may each include, for example, silicon oxide, silicon nitride, or a combination thereof.

In some embodiments, the first gate electrode layer **132** and the second gate electrode layer **232** may include threshold voltage control layers, barrier layers, and filling layers sequentially stacked on the first gate insulation layer **131** and the second gate insulation layer **231**, respectively. The threshold voltage control layers may include, for example, titanium nitride, titanium aluminum, titanium aluminum oxide, titanium aluminum carbide, titanium aluminum nitride, titanium aluminum oxynitride, titanium aluminum carbonitride, titanium aluminum oxycarbonitride, titanium oxynitride, titanium oxycarbonitride, titanium silicon nitride, titanium silicon oxynitride, tantalum nitride, tantalum oxynitride, tantalum aluminum nitride, tantalum aluminum oxynitride, tungsten nitride, tungsten carbonitride, aluminum oxide, or combinations thereof. The barrier layers may include titanium nitride, tantalum nitride, or a combination thereof. The filling layers may include tungsten, for example.

The first gate spacer **142** and the second gate spacer **242** may each include, for example, silicon oxide, silicon nitride, or a combination thereof. The first gate spacer **142** may be located on both side surfaces of the first gate structure **130** and may be apart from each other in the Y direction, and the second gate spacer **242** may be located on both side surfaces of the second gate structure **230** and may be apart from each other in the Y direction. The first gate spacer **142** may have an inner side surface **142**I contacting the first gate structure **130** and an outer side surface **142**O opposite to the inner side surface **142**I and contacting an interlayer insulation layer **90** to be described below, and the second gate spacer **242** may have an inner side surface **242**I contacting the gate structure **230** and an outer side surface **242**O opposite to the inner side surface **242**I and contacting the interlayer insulation layer **90**.

In some embodiments, the topmost portion **142**T of the bottom surface of the first gate spacer **142** may contact the first source/drain structure **150** as shown in FIG. **1**B, and the bottommost portion **142**B of the bottom surface of the first gate spacer **142** may contact the device isolation layer **60** as shown in FIG. **1**D. The topmost portion **242**T of the bottom surface of the second gate spacer **242** may contact the second source/drain structure **250** as shown in FIG. **1**C, and the bottommost portion **242**B of the bottom surface of the second gate spacer **242** may contact the device isolation layer **60** as shown in FIG. **1**D.

The topmost portion **142**T of the bottom surface of the first gate spacer **142** may be lower than the topmost portion **120**T of the top surface of the first fin structure **120** as shown in FIG. **1**B. For example, a distance D**5** from the topmost portion **120**T of the top surface of the first fin structure **120** to the topmost portion **142**T of the bottom surface of the first gate spacer **142** in the vertical direction Z may be from about 1 nm to about 20 nm, e.g., from about 5 nm to about 15 nm. Therefore, the topmost portion **250**T of the top surface of the first source/drain structure **150** may be lower than the topmost portion **120**T of the top surface of the first fin structure **120** to prevent abnormal growth of the first source/drain structure **150**, and thus first source/drain structures **150** adjacent to one another may be prevented from being merged with one another.

In some embodiments, the topmost portion **242**T of the bottom surface of the second gate spacer **242** may be lower than the topmost portion **220**T of the top surface of the second fin structure **220** as shown in FIG. **1**C. For example, a distance D**6** from the topmost portion **220**T of the top surface of the second fin structure **220** to the topmost portion **242**T of the bottom surface of the second gate spacer **242** in the vertical direction Z may be from about 1 nm to about 20 nm, e.g., from about 5 nm to about 15 nm. In some embodiments, the distance D**5** from the topmost portion **120**T of the top surface of the first fin structure **120** to the topmost portion **142**T of the bottom surface of the first gate spacer **142** in the vertical direction Z may be substantially identical to the distance D**6** from the topmost portion **220**T of the top surface of the second fin structure **220** to the topmost portion **242**T of the bottom surface of the second gate spacer **242** in the vertical direction Z. In other words, a difference between two distances D**5** and D**6** may be within a difference between etching depths of two structures respectively located on two regions of a substrate, and may be the difference that may occur when the two structures are simultaneously etched under the same etching conditions. In some embodiments, the first fin structure **120** may be etched, such that the topmost portion **142**T of the bottom surface of the first gate spacer **142** becomes lower than the topmost portion **120**T of the top surface of the first fin structure **120**. At this time, the second fin structure **220** may be also etched together, and thus the topmost portion **242**T of the bottom surface of the second gate spacer **242** may become lower than the topmost portion **220**T of the top surface of the second fin structure **220**. In this case, it is not necessary to prevent the second fin structure **220** from being etched, separate operations (e.g., formation of a mask on the second fin structure **220** before etching the first fin structure **120** and removal of the mask after the first fin structure **120** is etched) may not be needed, and thus the overall manufacturing process may become simple and easy.

The topmost portion **142**T of the bottom surface of the first gate spacer **142** may be higher than the bottommost portion **120**B of the top surface of the first fin structure **120** as shown in FIG. **1**B. In other words, after the first gate spacers **142** are formed and before the first source/drain structure **150** is formed, the first fin structure **120** may be further etched. In some embodiments, the topmost portion **242**T of the bottom surface of the second gate spacer **242** may be higher than the bottommost portion **220**B of the top surface of the second fin structure **220** as shown in FIG. **1**C. In other words, after the second gate spacers **242** are formed and before the second source/drain structure **250** is formed, the second fin structure **220** may be further etched.

The first source/drain structures **150** are formed apart from one another, because they may cause a defect of the semiconductor device **1000** when merged. On the other hand, the second source/drain structure **250** may contact all of the second fin structures **220**. In other words, the second source/drain structure **250** may extend throughout the second fin structures **220**. In other words, the second source/drain structure **250** may have a structure in which respective portions of the source/drain structure **250** that are starting to grow from each of the second fin structures **220** independently are merged with one another. Although FIG. **1**A shows that the single second source/drain structure **250** extends throughout the three second fin structures **220**, the single second source/drain structure **250** may contact fewer or more than three second fin structures **220**. The second source/drain structure **250** may have a merged structure, thereby increasing the mobility of charge carriers and reducing the resistance and the contact resistance of the second source/drain structure **250**. Therefore, the performance of the semiconductor device **1000** may be improved. The first source/drain structure **150** may be located on the bottommost portion **120**B of the top surface of the first fin structure **120**, and the second source/drain structure **250** may be located on the bottommost portion **220**B of the top surface of the second fin structure **220**. In some embodiments, the bottommost portion **150**B of the bottom surface of the first source/drain structure **150** may be lower than the bottommost portion **120**B of the top surface of the first fin structure **120** as shown in FIG. **1**B. However, in an embodiment, the bottommost portion **150**B of the bottom surface of the first source/drain structure **150** may instead be higher than the bottommost portion **120**B of the top surface of the first fin structure **120** or may be at the same height as the bottommost portion **120**B of the top surface of the first fin structure **120**. In the same regard, the bottommost portion **250**B of the bottom surface of the second source/drain structure **250** may be lower than the bottommost portion **220**B of the top surface of the second fin structure **220** as shown in FIG. **1**C. However, in an embodiment, the bottommost portion **250**B of the bottom surface of the second source/drain structure **250** may instead be higher than the bottommost portion **220**B of the top surface of the second fin structure **220** or may be at the same height as the bottommost portion **220**B of the top surface of the second fin structure **220**.

When the first source/drain structure **150** reaches the topmost portion **142**T of the bottom surface of the first gate spacer **142**, the growth of the first source/drain structure **150** may be suppressed. Since the topmost portion **142**T of the bottom surface of the first gate spacer **142** is lower than the topmost portion **120**T of the top surface of the first fin structure **120**, the topmost portion **150**T of the top surface of the first source/drain structure **150** may be lower than the topmost portion **120**T of the top surface of the first fin structure **120**. Therefore, abnormal growth of the first source/drain structure **150** may be prevented, and the first source/drain structures **150** adjacent to one another may be prevented from being merged with one another. In some embodiments, the topmost portion **150**T of the top surface of the first source/drain structure **150** may be at the same height as the topmost portion **142**T of the bottom surface of the first gate spacer **142**, as shown in FIG. **1**B. In some embodiments, the topmost portion **150**T of the top surface of the first source/drain structure **150** may instead be lower than the topmost portion **142**T of the bottom surface of the first gate spacer **142**.

In some embodiments, the topmost portion **250**T of the top surface of the second source/drain structure **250** may be lower than the topmost portion **220**T of the top surface of the second fin structure **220** as shown in FIG. **1**C. In some embodiments, the topmost portion **250**T of the top surface of the second source/drain structure **250** may be at the same height as the topmost portion **242**T of the bottom surface of the second gate spacer **242**, as shown in FIG. **1**C. In some embodiments, the topmost portion **250**T of the top surface of the second source/drain structure **250** may instead be higher or lower than the topmost portion **242**T of the bottom surface of the second gate spacer **242**.

In some embodiments, a length D7 of the first source/drain structure **150** in the vertical direction Z may be less than a length D**8** of the second source/drain structure **250** in the vertical direction Z. The length D**7** of the first source/drain structure **150** in the vertical direction Z is defined as the distance from the bottommost portion **150**B of the bottom surface of the first source/drain structure **150** to the topmost portion **150**T of the top surface of the first source/drain structure **150** in the vertical direction Z, whereas the length D**8** of the second source/drain structure **250** in the vertical direction Z is defined as the distance from the bottommost portion **250**B of the bottom surface of the second source/drain structure **250** to the topmost portion **250**T of the top surface of the second source/drain structure **250** in the vertical direction. When the second source/drain structure **250** is larger than the first source/drain structure **150** in the vertical direction Z, the mobility of charge carriers may be increased and the resistance and the contact resistance of the second source/drain structure **250** may be reduced. Therefore, the semiconductor device **1000** may exhibit improved performance.

In some embodiments, the first source/drain structure **150** may include a portion closer to the first gate structure **130** in the horizontal direction (e.g., the Y direction) than the outer side surface **142**O of the first gate spacer **142** is. In other words, a distance from the portion of the first source/drain structure **150** in the Y direction to the first gate structure **130** may be smaller than a distance from the outer side surface **142**O of the first gate spacer **142** to the first gate structure **130**. In other words, the extension range of at least a portion of the first source/drain structure **150** in the horizontal direction (e.g., the Y direction) may overlap the extension range of the first gate spacer **142** in the horizontal direction (e.g., the Y direction). In some embodiments, the second source/drain structure **250** may include a portion closer to the second gate structure **230** in the horizontal direction (e.g., the Y direction) than the outer side surface **242**O of the second gate spacer **242** is. In other words, a distance from the portion of the second source/drain structure **250** in the Y direction to the second gate structure **230** may be smaller than a distance from the outer side surface **242**O of the second gate spacer **242** to the second gate structure **230**. In other words, the extension range of at least a portion of the second source/drain structure **250** in the horizontal direction (e.g., the Y direction) may overlap the extension range of the second gate spacer **242** in the horizontal direction (e.g., the Y direction).

In some embodiments, the number of layers constituting the first source/drain structure **150** may be less than the number of layers constituting the second source/drain structure **250**. For example, the first source/drain structure **150** may include first to third source/drain layers **151** to **153** and a capping layer (i.e., a first capping layer) **155** that are sequentially stacked on the first fin structure **120**, and the second source/drain structure **250** may include first to third source/drain layers **251** to **253** sequentially stacked on the second fin structure **220**, a fourth source/drain layer **254** on the third source/drain layer **253**, and a capping layer (i.e., a second capping layer) **255** on the fourth source/drain layer **254**. Although FIG. **1**B shows that the first source/drain structure **150** includes four layers (including the capping layer **155**) and the second source/drain structure **250** includes five layers (including the capping layer **255**), the number of layers constituting the first source/drain structure **150** may be more or less than four and the number of layers constituting the second source/drain structure **250** may be more or less than five.

In some embodiments, the compositions of the first to third source/drain layers **151** to **153** and the capping layer **155** of the first source/drain structure **150** may be substantially the same as the compositions of the first to third source/drain layer **251** to **253** and the capping layer **255** of the second source/drain structure **250**. In other words, a difference between concentrations of two layers may be within a difference between compositions of the two layers which may incidentally occur when the two layers are formed respectively on two regions of a substrate at the same time under the same deposition condition.

In some embodiments, the capping layer **155** of the first source/drain structure **150** and the capping layer **255** of the second source/drain structure **250** may include Si. In some embodiments, the first to third source/drain layers **151** to **153** of the first source/drain structure **150** and first to fourth source/drain layers **251** to **254** of the second source/drain structure **250** may include SiGe. Also, the first to third source/drain layers **151** to **153** of the first source/drain structure **150** and the first to fourth source/drain layers **251** to **254** of the second source/drain structure **250** may be doped with a p-type dopant. The p-type dopant may include, for example, B, Al, Ga, In, or a combination thereof.

In some embodiments, the Si concentration of the first to third source/drain layers **151** to **153** of the first source/drain structure **150** may be reduced (i.e., may decrease) from the first source/drain layer **151** to the third source/drain layer **153**. For example, the Si concentrations of the first to third source/drain layers **151** to **153** of the first source/drain structure **150** may be from about 70% to about 90%, from about 50% to about 70%, and from about 40% to about 50%, respectively. Also, the dopant concentration of the first to third source/drain layers **151** to **153** of the first source/drain structure **150** may be increased from the first source/drain layer **151** to the third source/drain layer **153**. For example, the dopant concentrations of the first to third source/drain layers **151** to **153** of the first source/drain structure **150** may be from about 1.0×10^{18} cm^{-3} to about 1.0×10^{19} cm^{-3}, from about 1.0×10^{20} cm^{-3} to about 3.0×10^{20} cm^{-3}, and from about 3.0×10^{20} cm^{-3} to about 5.0×10^{20} cm^{-3}, respectively.

In some embodiments, the Si concentration of the first to fourth source/drain layers **251** to **254** of the second source/drain structure **250** may be reduced (i.e., may decrease) from the first source/drain layer **251** to the fourth source/drain layer **254**. For example, the Si concentrations of the first to fourth source/drain layers **251** to **254** of the second source/drain structure **250** may be from about 70% to about 90%, from about 50% to about 70%, from about 40% to about 50%, and from about 35% to about 45%, respectively. Also, the dopant concentration of the first to fourth source/drain layers **251** to **254** of the second source/drain structure **250** may be increased from the first to fourth source/drain layers **251** to **254**. For example, the dopant concentrations of the first to fourth source/drain layers **251** to **254** of the second source/drain structure **250** may be from about 1.0×10^{18} cm^{-3} to about 1.0×10^{19} cm^{-3}, from about 1.0×10^{20} cm^{-3} to about 3.0×10^{20} cm^{-3}, from about 3.0×10^{20} cm^{-3} to about 5.0×10^{20} cm^{-3}, and from about 3.0×10^{20} cm^{-3} to about 5.0×10^{20} cm^{-3}, respectively.

In some embodiments, the Si concentrations of the first to third source/drain layers **151** to **153** of the first source/drain structure **150** may be lower than the Si concentration of the capping layer **155** of the first source/drain structure **150**. For example, the Si concentration of the capping layer **155** of the first source/drain structure **150** may be nearly 100% (e.g., 95% or higher or 99% or higher). In some embodiments, the Si concentrations of the first to fourth source/drain layers **251** to **254** of the second source/drain structure **250** may be lower than the Si concentration of the capping layer **255** of the second source/drain structure **250**. For example, the Si concentration of the capping layer **255** of the second source/drain structure **250** may be nearly 100% (e.g., 95% or higher or 99% or higher).

In some embodiments, the semiconductor device **1000** may further include an interlayer insulation layer **90**. The interlayer insulation layer **90** may be located on the first source/drain structure **150**, the second source/drain structure **250**, the outer side surface **142**O of the first gate spacer **142**, the outer side surface **242**O of the second gate spacer **242**, and the device isolation layer **60**. The interlayer insulation layer **90** may include, for example, silicon oxide, silicon nitride, or a combination thereof.

Since the topmost portion **142**T of the bottom surface of the first gate spacer **142** of the semiconductor device **1000** may be lower than the topmost portion **120**T of the top surface of the first fin structure **120**, the topmost portion **150**T of the top surface of the first source/drain structure **150** may be lower than the topmost portion **120**T of the top surface of the first fin structure **120**. Also, growth of the first source/drain structure **150** may be suppressed while the second source/drain structure **250** is being grown. Therefore, abnormal growth and overgrowth of the first source/drain structure **150** may be prevented, and the second source/drain structure **250** may be large. For example, the second source/drain structure **250** may have a merged structure. Therefore, the performance of the semiconductor device **1000** may be improved due to an increase in the size of the second source/drain structure **250** while preventing a defect of the semiconductor device **1000** due to the merging of the first source/drain structures **150**.

FIG. **2** is a cross-sectional view of a semiconductor device **1000***a* according to an embodiment, taken along the lines **A1**-**A1'** and **B1**-**B1'** of FIG. **1**A.

Referring to FIG. **2**, the topmost portion **150**T of the top surface of the first source/drain structure **150** may be higher than the topmost portion **142**T of the bottom surface of the first gate spacer **142**, but may still be lower than the topmost portion **120**T of the top surface of the first fin structure **120**. Since the topmost portion **150**T of the top surface of the first source/drain structure **150** is still lower than the topmost portion **120**T of the top surface of the first fin structure **120**, abnormal growth of the first source/drain structure **150** may be prevented, and thus the first source/drain structures **150** may be prevented from being merged. Therefore, a defect of the semiconductor device **1000***a* may be prevented.

FIG. **3** is a cross-sectional view of a semiconductor device **1000***b* according to an embodiment, taken along the lines **A2**-**A2'** and **B2**-**B2'** of FIG. **1**A.

Referring to FIG. **3**, the topmost portion **242**T of the bottom surface of the second gate spacer **242** may be at the same height of the topmost portion **220**T of the top surface of the second fin structure **220** or higher than the topmost portion **220**T of the top surface of the second fin structure **220**. Therefore, in some embodiments, the topmost portion **250**T of the top surface of the second source/drain structure **250** may be at the same height as the topmost portion **220**T of the top surface of the second fin structure **220** or higher than the topmost portion **220**T of the top surface of the second fin structure **220**. Therefore, the second source/drain structure **250** having a larger size may be formed, and thus the semiconductor device **1000***b* may exhibit improved performance. However, in another embodiments, the topmost portion **250**T of the top surface of the second source/drain structure **250** may be lower than the topmost portion **220**T of the top surface of the second fin structure **220** as shown, for example, in FIG. **1**C.

FIG. **4**A is a cross-sectional view of a semiconductor device **2000** according to an embodiment, taken along the lines A**1**-A**1**' and B**1**-B**1**' of FIG. **1**A. FIG. **4**B is a cross-sectional view of the semiconductor device **2000** according to an embodiment, taken along the lines A**2**-A**2**' and B**2**-B**2**' of FIG. **1**A.

Referring to FIGS. **4**A and **4**B, a first fin structure **120'** may include a plurality of first channels **120***a* to **120***d* apart (i.e., separated) from one another in the vertical direction Z, and a second fin structure **220'** may include a plurality of second channels **220***a* to **220***d* apart (i.e., separated) from one another in the vertical direction Z. Although in FIGS. **4**A and **4**B the first fin structure **120'** includes four first channels **120***a* to **120***d* and the second fin structure **220'** includes four second channels **220***a* to **220***d*, the first fin structure **120'** may include more or fewer than four first channels and the second fin structure **220'** may include more or fewer than four second channels.

The first gate structure **130** may contact the top surface of a bottommost first channel, that is, the first channel **120***a*. and both the bottom surfaces and the top surfaces of the remaining first channels, the first channels **120***b* to **120***d*, whereas the second gate structure **230** may contact the top surface of a second bottommost channel, that is, the second channel **220***a*, and both the bottom surfaces and top surfaces of remaining second channels **220***b* to **220***d*. The first gate structure **130** may further contact both side surfaces of the first channels **120***a* to **120***d*, the side surfaces being apart from each other in the X direction, and the second gate structure **230** may further contact both side surfaces of the second channels **220***a* to **220***d*, the side surfaces being apart from each other in the X direction. In other words, the first gate structure **130** may surround the first channels **120***a* to **120***d*, and the second gate structure **230** may surround the second channels **220***a* to **220***d*.

The first gate insulation layer **131** may contact the top surface of the bottommost first channel, that is, the first channel **120***a*, the bottom surfaces and the top surfaces of the remaining first channels, that is, the first channels **120***b* to **120***d*, and the both side surfaces of the first channels **120***a* to **120***d*, the side surfaces being apart from each other in the X direction, whereas the second gate insulation layer **231** may contact the top surface of the bottommost second channel, that is, the second channel **220***a*, the bottom surfaces and the top surfaces of the remaining second channels, that is, the second channels **220***b* to **220***d*, and the both side surfaces of the second channels **220***a* to **220***d*, the side surfaces being apart from each other in the X direction. The first gate electrode layer **132** may be located on the first gate insulation layer **131**, and the second gate electrode layer **232** may be located on the second gate insulation layer **231**.

The first gate spacers **142** may be located on the side surfaces of a portion of the first gate structure **130** that is located on the top surface of a topmost first channel, that is, the first channel **120***d*. The topmost portion **142**T of the bottom surface of the first gate spacer **142** may be lower than the topmost portion **120**T' of the top surface of the topmost first channel, that is, the first channel **120***d*. The second gate spacers **242** may be located on the side surfaces of a portion of the second gate structure **230** that is on the top surface of a topmost second channel, that is, the second channel **220***d*. In some embodiments, the topmost portion **242**T of the bottom surface of the second gate spacer **242** may be lower than the topmost portion **220**T' of the top surface of the topmost second channel, that is, the second channel **220***d*. In an embodiment, the topmost portion **242**T of the bottom surface of the second gate spacer **242** may instead be at the same height as the topmost portion **220**T' of the top surface of the topmost second channel, that is, the second channel **220***d*, or may be higher than the topmost portion **220**T' of the top surface of the topmost second channel, that is, the second channel **220***d*.

The first source/drain structure **150** may contact the first channels **120***a* to **120***d* of the first fin structure **120'**, and the second source/drain structure **250** may contact the second channels **220***a* to **220***d* of the second fin structure **220'**. The topmost portion **150**T of the top surface of the first source/drain structure **150** may be lower than the topmost portion **120**T' of the top surface of the topmost first channel, that is, the first channel **120***d*. In some embodiments, the topmost portion **250**T of the top surface of the second source/drain structure **250** may be lower than the topmost portion **220**T' of the top surface of the topmost second channel, that is, the second channel **220***d*. In an embodiment, the topmost portion **250**T of the top surface of the second source/drain structure **250** may instead be at the same height as the topmost portion **220**T' of the top surface of the topmost second channel, that is, the second channel **220***d* or higher than the topmost portion **220**T' of the top surface of the topmost second channel, that is, the second channel **220***d*.

In some embodiments, the semiconductor device **2000** may further include a plurality of first inner spacers **146** located between respective portions of the first gate structure **130**, that are located between the first channels **120***a* to **120***d*, and the first source/drain structure **150**. Also, the semiconductor device **2000** may further include a plurality of second inner spacers **246** located between respective portions of the second gate structure **230**, that are located between the second channels **120***a* to **120***d*, and the second source/drain structure **250**. The first inner spacers **146** and the second inner spacers **246** may include, for example, silicon oxide, silicon nitride, or a combination thereof.

FIGS. **5**A to **14**B are diagrams showing a method of manufacturing a semiconductor device according to an embodiment.

Referring to FIGS. **5**A and **5**B, the first fin structure **120** may be formed on the first region R**1** of the substrate **10**, and the second fin structure **220** may be formed on the second region R**2** of the substrate **10**. The first fin structure **120** and the second fin structure **220** may be formed by etching the substrate **10** or may be formed by forming an epitaxial layer on the substrate **10** and then etching the epitaxial layer. In some embodiments, a pitch D**1** of the first fin structures **120** may be greater than a pitch D**2** of the second fin structures **220** as shown in FIGS. **5**A and **5**B. For example, the pitch D**1** of the first fin structures **120** may be about twice the pitch D**2** of the second fin structures **220**.

Referring to FIGS. **6**A and **6**B, the device isolation layer **60** surrounding the side surfaces of the lower portions of the first fin structure **120** and the side surfaces of the lower portions of the second fin structure **220** may be formed on the substrate **10**. For example, the device isolation layer **60** may be formed on the top surface of the substrate **10**, on side and top surfaces of the first fin structure **120**, and on side and top surfaces of the second fin structure **220**. Next, the device isolation layer **60** may be planarized to expose the top surface of the first fin structure **120** and the top surface of the second fin structure **220**. Next, the upper portion of the remaining device isolation layer **60** may be etched.

Referring to FIGS. **7**A and **7**B, first dummy gate structures **180** may be formed on the first fin structure **120**, and second dummy gate structures **280** may be formed on the second fin structures **220**. In some embodiments, the first dummy gate structures **180** may extend parallel to one another in the X direction and may be apart from one another in the Y direction. The second dummy gate structures **280** may extend parallel to one another in the X direction and may be apart from one another in the Y direction.

The first dummy gate structure **180** may include a first dummy gate insulation layer **181**, a first dummy gate electrode layer **182**, and a first dummy gate mask layer **183** that are sequentially stacked. The second dummy gate structure **280** may include a second dummy gate insulation layer **281**, a second dummy gate electrode layer **282**, and a second dummy gate mask layer **283** that are sequentially stacked. The first dummy gate insulation layer **181** and the second dummy gate insulation layer **281** may each include, for example, silicon oxide, silicon nitride, or a combination thereof. The first dummy gate electrode layer **182** and the second dummy gate electrode layer **282** may include a semiconductor material, for example. The first dummy gate mask layer **183** and the second dummy gate mask layer **283** may each include, for example, silicon oxide, silicon nitride, or a combination thereof.

For example, a dummy gate insulation layer, a dummy gate electrode layer, and a dummy gate mask layer are sequentially formed on the first fin structure **120** and the second fin structure **220**, and the dummy gate mask layer is patterned. The first dummy gate structure **180** and the second dummy gate structure **280** may be formed by sequentially etching the dummy gate electrode layer and the dummy gate insulation layer by using the dummy gate mask layer as an etching mask.

Referring to FIGS. **8**A and **8**B, a first recess **120**R may be formed in the first fin structure **120** by etching the upper portion of the first fin structure **120** by using the first dummy gate structure **180** as an etching mask. In some embodiments, a second recess **220**R may be formed in the second fin structure **220** by etching the upper portion of the second fin structure **220** by using the second dummy gate structure **280** as an etching mask.

Referring to FIGS. **9**A and **9**B, first gate spacers **142** on side surfaces of the first dummy gate structure **180**, first fin spacers **144** on the side surfaces of the first fin structure **120**, second gate spacers **242** on side surfaces of the second dummy gate structure **280**, and second fin spacers **244** on the side surfaces of the second fin structure **220** may be formed. For example, a spacer layer may be formed on all of the first dummy gate structure **180**, the first fin structure **120**, the second dummy gate structure **280**, the second fin structure **220**, and the device isolation layer **60**, and then the spacer layer may be anisotropically etched, thereby forming the first gate spacers **142**, the first fin spacers **144**, the second gate spacers **242**, and the second fin spacers **244**. In some embodiments, the first fin spacers **144** and the second fin spacers **244** may be removed.

Due to the first recess **120**R of the first fin structure **120**, the topmost portion **142**T of the bottom surface of the first gate spacer **142** may be formed lower than the topmost portion **120**T of the top surface of the first fin structure **120**. In some embodiments, due to the second recess **220**R of the second fin structure **220**, the topmost portion **242**T of the bottom surface of the second gate spacer **242** may be formed lower than the topmost portion **220**T of the top surface of the second fin structure **220**.

Referring to FIGS. **10**A and **10**B, after the spacer layers are formed, the first fin structure **120** may be further etched to extend the first recess **120**R in the vertical direction, such that the bottommost portion **120**B of the top surface of the first fin structure **120** becomes lower than the topmost portion **142**T of the bottom surface of the first gate spacer **142**. In some embodiments, the first fin structure **120** may be further etched in a horizontal direction (e.g., the Y direction), such that at least some of side surfaces of the first recess **120**R are formed closer to the first dummy gate structure **180** in the horizontal direction (the Y direction) than the outer side surface **142**O of the first gate spacer **142** is. In other words, a distance from at least some side surfaces of the first recess **120**R to the first dummy gate structure **180** may be smaller than a distance from the outer side surface **142**O of the first gate spacer **142** to the first dummy gate structure **180** in the horizontal direction. In other words, anisotropic etching and isotropic etching may be performed to the first recess **120**R.

Also, the second fin structure **220** may be further etched in the vertical direction, such that the bottommost portion **220**B of the top surface of the second fin structure **220** becomes lower than the topmost portion **242**T of the bottom surface of the second gate spacer **242**. In some embodiments, the second recess **220**R may be deeper than first recess **120**R. In other words, the bottommost portion **220**B of the top surface of the second fin structure **220** may be formed lower than the bottommost portion **120**B of the top surface of the first fin structure **120**. In some embodiments, the second fin structure **220** may be further etched in a horizontal direction (e.g., the Y direction), such that at least some of side surfaces of the second recess **220**R are formed closer to the second dummy gate structure **280** in the horizontal direction (the Y direction) than the outer side surface **242**O of the second gate spacer **242** is. In other words, a distance from at least some side surfaces of the second recess **220**R to the second dummy gate structure **280** may be smaller than a distance from the outer side surface **242**O of the second gate spacer **242** to the second dummy gate structure **280** in the horizontal direction. In other words, anisotropic etching and isotropic etching may be performed to the second recess **220**R.

Referring to FIGS. **11**A and **11**B, the first source/drain structure **150** in the first recess **120**R of the first fin structure **120** and the second source/drain structure **250** in the second recess **220**R of the second fin structure **220** may be formed through selective epitaxial growth (SEG). In some embodiments, the first source/drain structure **150** and the second source/drain structure **250** may be formed through a plurality of SEG operations. For example, a first source/drain layer **151** in the first recess **120**R and a first source/drain layer **251** in the second recess **220**R may be formed through a first SEG operation, a second source/drain layer **152** in the first recess **120**R and a second source/drain layer **252** in the second recess **220**R may be formed through a second SEG operation, and a third source/drain layer **153** in the first recess **120**R and a third source/drain layer **253** in the second recess **220**R may be formed through a third SEG operation.

Referring to FIG. **11**C, in some embodiments, the second source/drain structure **250** may be further grown through SEG. For example, a fourth source/drain layer **254** may be formed in the second recess **220**R of the second fin structure **220**, e.g., on the third source/drain layer **253**. Growth of the first source/drain structure **150** may be suppressed while the second source/drain structure **250** is being grown, that is, while the fourth source/drain layer **254** is being formed. For example, by using a source gas that does not include Cl (e.g., $SiH4$) as a Si source gas and using a relatively low flow rate carrier gas (e.g., $H2$ gas), growth of the first source/drain structure **150** may be suppressed while the second source/drain structure **250** is being grown. Therefore, the second source/drain structure **250** may be grown large to improve the performance of a semiconductor device, and the first source/drain structures **150** may be prevented from being overgrown and merged with one another.

Referring to FIGS. **12**A and **12**B, in some embodiments, the first source/drain structure **150** and the second source/drain structure **250** may be further grown through SEG. For example, a capping layer **155** in the first recess **120**R and a capping layer **255** in the second recess **220**R may be formed.

When the first source/drain structure **150** contacts the first gate spacer **120** during the growth of the first source/drain structure **150** described above with reference to FIGS. **11**A and **12**A, the growth of the first source/drain structure **150** may be suppressed. Therefore, the first source/drain structure **150** may be prevented from growing up above the topmost portion **142**T of the bottom surface of the first gate spacer **142**. Since the topmost portion **142**T of the bottom surface of the first gate spacer **142** is lower than the topmost portion **120**T of the top surface of the first fin structure **120**, the topmost portion **150**T of the top surface of the first source/drain structure **150** may be lower than the topmost portion **120**T of the top surface of the first fin structure **120**.

As shown in FIG. **2**, even when the topmost portion **150**T of the top surface of the first source/drain structure **150** grows higher than the topmost portion **142**T of the bottom surface of the first gate spacer **142**, the growth rate of the first source/drain structure **150** is significantly reduced after the topmost portion **150**T of the top surface of the drain structure **150** is grown to the topmost portion **142**T of the bottom surface of the first gate spacer **142**, and thus growth of the first source/drain structure **150** may stop before the topmost portion **150**T of the top surface of the first source/drain structure **150** reaches the topmost portion **120**T of the top surface of the first fin structure **120**. Therefore, the topmost portion **150**T of the top surface of the first source/drain structure **150** may be formed lower than the topmost portion **120**T of the top surface of the first fin structure **120**.

When the topmost portion **150**T of the top surface of the first source/drain structure **150** is formed lower than the topmost portion **120**T of the top surface of the first fin structure **120**, abnormal growth of the first source/drain structure **150** may be prevented, and the first source/drain structures **150** may be prevented from being merged with one another. Therefore, it is possible to prevent a defect of the semiconductor device that occurs as the first source/drain structures **150** are merged with one another.

In some embodiments, for example, when the topmost portion **242**T of the bottom surface of the second gate spacer **242** is formed lower than the topmost portion **220**T of the top surface of the second fin structure **220**, the topmost portion **250**T of the top surface of the second source/drain structure **250** may be formed lower than the topmost portion **220**T of the top surface of the second fin structure **220**. However, since the second recess **220**R is deeper than the first recess **120**R, the second source/drain structure **250** may be formed larger than the first source/drain structure **150** in the vertical direction and the horizontal direction (e.g., the X direction), and the pitch D**2** (refer to FIG. **5**B) of the second fin structures **220** is smaller than the pitch D**1** (refer to FIG. **5**A) of the first fin structures **120**. Therefore, portions of the second source/drain structure **250** respectively grown from each of the second fin structures **220** may be merged with one another. Although FIG. **11**B shows that merging occurs while the third source/drain layer **253** is being formed, merging may also occur while another source/drain layer is being formed. For example, merging may occur while the second source/drain layer **252** or the fourth source/drain layer **254** is being formed. By growing the second source/drain structure **250** largely to cause the merging of the second source/drain structure **250**, the mobility of charge carriers may be increased and the resistance and the contact resistance of the second source/drain structure **250** may be reduced. Therefore, a semiconductor device with improved performance may be manufactured.

Referring to FIGS. **13**A and **13**B, the interlayer insulation layer **90** may be formed on the first source/drain structure **150**, the second source/drain structure **250**, the first gate spacer **142**, the second gate spacer **242**, and the device isolation layer **60**. The interlayer insulation layer **90** may then be planarized to expose top surfaces of the first dummy gate electrode layer **182** of the first dummy gate structure **180** and the second dummy gate electrode layer **282** of the second dummy gate structure **280**. During the planarization, the first dummy gate mask layer **183** (refer to FIG. **12**A) and the second dummy gate mask layer **283** (refer to FIG. **12**B) may also be removed.

Referring to FIGS. **14**A and **14**B, a first opening OP**1** and a second opening OP**2** may be formed by removing the first dummy gate structure **180** (refer to FIG. **13**A) and the second dummy gate structure **280** (refer to FIG. **13**B), respectively. The first opening OP**1** may expose the first fin structure **120** and the inner side surface **142**I of the first gate spacer **142**. The second opening OP**2** may expose the second fin structure **220** and the inner side surface **242**I of the second gate spacer **242**.

The first gate structure **130** (refer to FIG. **2**B) may be formed in the first opening OP**1**, and the second gate structure **230** (refer to FIG. **2**C) may be formed in the second opening OP**2**. For example, gate insulation layers and gate electrode layers are sequentially formed on a portion of the first fin structure **120** and a portion of the inner side surface **142**I of the first gate spacer **142** that are exposed in the first opening OP**1** and a portion of the second fin structure and a portion of the inner side surface **242**I of the second gate spacer **242** that are exposed in the second opening OP**2** and the gate insulation layers and the gate electrode layers are planarized to expose the interlayer insulation layer **90**, and thus the first gate structure **130** (refer to FIG. **2**B) and the second gate structure **230** (refer to FIG. **2**C) may be formed.

According to the method described above with reference to FIGS. **5**A to **14**B, the semiconductor device **1000** described above with reference to FIGS. **1**B and **1**C or the semiconductor device **1000***a* described above with reference to FIG. **2** may be manufactured.

In some embodiments, the formation of the second recess **220**R in the second fin structure **220** shown in FIG. **8**B may be omitted before the formation of the second gate spacer **242** shown in FIG. **9**B. Therefore, as shown in FIG. **3**, the topmost portion **242**T of the bottom surface of the second gate spacer **242** may be formed at the same height as the topmost portion **220**T of the top surface of the second fin structure **220**. The topmost portion **242**T of the bottom surface of the second gate spacer **242** is formed at the same height as the topmost portion **220**T of the top surface of the second fin structure **220**, and thus, in some embodiments, the topmost portion **250**T of the second source/drain structure **250** may be formed at the same height as the topmost portion **220**T of the top surface of the second fin structure **220** or higher than the topmost portion **220**T of the top surface of the second fin structure **220**. In this regard, the semiconductor device **1000***b* described above with reference to FIG. **3** may be manufactured.

FIGS. **15**A to **26**B are diagrams showing a method of manufacturing a semiconductor device according to an embodiment.

Referring to FIGS. **15**A and **15**B, a first fin structure **120'** may be formed on the first region R**1** of the substrate **10**, and a second fin structure **220'** may be formed on the second region R**2** of the substrate **10**. The first fin structure **120'** may include a plurality of first channels **120***a* to **120***d* apart (i.e., separated) from one another in the vertical direction and a plurality of first sacrificial layers **184***a* to **184***c* respectively located between adjacent pairs of first channels **120***a* to **120***d*. The second fin structure **220'** may include a plurality of second channels **220***a* to **220***d* apart from one another in the vertical direction and a plurality of second sacrificial layers **284***a* to **284***c* respectively located between adjacent pairs of second channels **220***a* to **220***d*. The first channels **120***a* to **120***d* and the second channels **220***a* to **220***d* may include a semiconductor material, and the first sacrificial layers **184***a* to **184***c* and the second sacrificial layers **284***a* to **284***c* may include another semiconductor material. For example, the first channels **120***a* to **120***d* and the second channels **220***a* to **220***d* may include Si, whereas the first sacrificial layers **184***a* to **184***c* and the second sacrificial layers **284***a* to **284***c* may include SiGe.

For example, a plurality of sacrificial layers and a plurality of channel layers may be alternately stacked on the first region R**1** and the second region R**2** of the substrate **10** through epitaxial growth, and upper portions of the sacrificial layers, the channel layers, and the substrate **10** may be etched, thereby forming the first fin structure **120'** and the second fin structure **220'**.

Referring to FIGS. **16**A and **16**B, the device isolation layer **60** surrounding the side surfaces of the lower portions of the first fin structure **120'** and the side surfaces of the lower portions of the second fin structure **220'** may be formed on the substrate **10**. An operation for forming the device isolation layer **60** is the same as the operation described above with reference to FIGS. **6**A and **6**B.

Referring to FIGS. **17**A and **17**B, the first dummy gate structures **180** may be formed on the first fin structure **120'**, and the second dummy gate structures **280** may be formed on the second fin structures **220'**. Operations for forming the first dummy gate structures **180** and the second dummy gate structures **280** are the same as the operations described above with reference to FIGS. **7**A and **7**B.

Referring to FIGS. **18**A and **18**B, the first recess **120**R may be formed in a topmost first channel, that is, the first channel **120***d* by etching the upper portion of the topmost first channel, that is, the first channel **120***d* by using the first dummy gate structure **180** as an etching mask. In some embodiments, the second recess **220**R may be formed in a topmost second channel, that is, the second channel **220***d*, by etching the upper portion of the topmost second channel, that is, the second channel **220***d* by using the second dummy gate structure **280** as an etching mask. In another embodiment, the formation of the second recess **220**R may be omitted.

Referring to FIGS. **19**A and **19**B, the first gate spacers **142** on the side surfaces of the first dummy gate structure **180** and the second gate spacers **242** on the side surfaces of the second dummy gate structure **280** may be formed. For example, a spacer layer may be formed on the first dummy gate structure **180**, the first fin structure **120'**, the second dummy gate structure **280**, the second fin structure **220'**, and the device isolation layer **60**, and then the spacer layer may be anisotropically etched, thereby forming the first gate spacers **142** and the second gate spacers **242**. In some embodiments, first fin spacers on the side surfaces of the first fin structure **120'** and second fin spacers on the side surfaces of the second fin structure **220'** may be further formed.

Due to the first recess **120**R, the topmost portion **142**T of the bottom surface of the first gate spacer **142** may be formed lower than the topmost portion **120**T' of the top surface of the topmost first channel, that is, the first channel **120***d*. In some embodiments, due to the second recess **220**R, the topmost portion **242**T of the bottom surface of the second gate spacer **242** may be formed lower than the topmost portion **220**T' of the top surface of the topmost second channel, that is, the second channel **220***d*. In another embodiment where the formation of the second recess **220**R is omitted, the topmost portion **242**T of the bottom surface of the second gate spacer **242** may be formed at the same height as the topmost portion **220**T' of the top surface of the topmost second channel, that is, the second channel **220***d*.

Referring to FIGS. **20**A and **20**B, the first fin structure **120'** may be further etched in the vertical direction, such that the first recess **120**R extends to below the top surface of a bottommost first channel, that is, the first channel **120***a*. In some embodiments, the first fin structure **120'** may be further etched in a horizontal direction (e.g., the Y direction), such that at least some of side surfaces of the first recess **120**R are formed closer to the first dummy gate structure **180** in the horizontal direction (the Y direction) than the outer side surface **142**O of the first gate spacer **142** is. In other words, a distance from at least some side surfaces of the first recess **120**R to the first dummy gate structure **180** may be smaller than a distance from the outer side surface **142**O of the first gate spacer **142** to the first dummy gate structure **180** in the horizontal direction. In other words, anisotropic etching and isotropic etching may be performed to the first recess **120**R.

Also, the second fin structure **220'** may be further etched in the vertical direction, such that the second recess **220**R extends to below the top surface of a bottommost second channel, that is, the second channel **220***a*. In some embodiments, the second recess **220**R may be deeper than first recess **120**R. In other words, the second fin structure **220'** may be etched, such that the bottommost portion **220**B of the top surface of the second fin structure **220'** becomes lower than the bottommost portion **120**B of the top surface of the first fin structure **120'**. In some embodiments, the second fin structure **220'** may be further etched in a horizontal direction (e.g., the Y direction), such that at least some of side surfaces of the second recess **220**R are formed closer to the second dummy gate structure **280** in the horizontal direction (the Y direction) than the outer side surface **242**O of the second gate spacer **242** is. In other words, a distance from at least some side surfaces of the second recess **220**R to the second dummy gate structure **280** may be smaller than a distance from the outer side surface **242**O of the second gate spacer **242** to the second dummy gate structure **280** in the horizontal direction. In other words, anisotropic etching and isotropic etching may be performed to the second recess **220**R.

Referring to FIGS. **21**A and **21**B, a plurality of first openings exposing the top surfaces of first channels **120***a* to **120***c*, the bottom surfaces of first channels **120***b* to **120***d*, and the side surfaces of the first sacrificial layers **184***a* to **184***c* may be formed by etching side portions of the first sacrificial layers **184***a* to **184***c*, and first inner spacers **146** may be formed in the first openings, respectively. For example, a bottommost first opening from among the first openings may expose the top surface of the bottommost first channel, that is, the first channel **120***a*, the bottom surface of a first channel **120***b* adjacent to and above the bottommost first channel **120***a*, and the side surfaces of a bottommost first sacrificial layer, that is, a first sacrificial layer **184***a*. A topmost first opening from among the first openings may expose the bottom surface of the topmost first channel, that is, the first channel **120**_d_, the top surface of a first channel **120**_c_ adjacent to and below the topmost first channel, that is, the first channel **120**_d_, and the side surfaces of a topmost first sacrificial layer, that is, a first sacrificial layer **184**_c_.

In the same regard, a plurality of second openings exposing the top surfaces of second channels **220**_a_ to **220**_c_, the bottom surfaces of second channels **220**_b_ to **220**_d_, and the side surfaces of the second sacrificial layers **284**_a_ to **284**_c_ may be formed by etching side portions of the second sacrificial layers **284**_a_ to **284**_c_, and second inner spacers **246** may be formed in the second openings, respectively. For example, a bottommost second opening from among the second openings may expose the top surface of the bottommost second channel, that is, the second channel **220**_a_, the bottom surface of a second channel **220**_b_ adjacent to and above the bottommost second channel, that is, the second channel **220**_a_, and the side surfaces of a bottommost second sacrificial layer, that is, a second sacrificial layer **284**_a_. A topmost second opening from among the second openings may expose the bottom surface of the topmost second channel, that is, the second channel **220**_d_, that is, the second channel **220**_d_, the top surface of a second channel **220**_c_ adjacent to and below the topmost second channel, that is, the second channel **220**_d_, and the side surfaces of a topmost second sacrificial layer, that is, a second sacrificial layer **284**_c_.

Referring to FIGS. **22**A and **22**B, the first source/drain structure **150** in the first recess **120**R of the first fin structure **120'** and the second source/drain structure **250** in the second recess **220**R of the second fin structure **220'** may be formed through SEG. For example, the first to third source/drain layers **151** to **153** may be formed in the first recess **120**R, and the first to third source/drain layers **251** to **253** may be formed in the second recess **220**R.

Referring to FIG. **23**, in some embodiments, the second source/drain structure **250** may be further grown through SEG. For example, a fourth source/drain layer **254** may be formed in the second recess **220**R of the second fin structure **220'**, e.g., on the third source/drain layer **253**. Growth of the first source/drain structure **150** may be suppressed while the second source/drain structure **250** is being further grown.

Referring to FIGS. **24**A and **24**B, in some embodiments, the first source/drain structure **150** and the second source/drain structure **250** may be further grown through SEG. For example, a capping layer **155** in the first recess **120**R and a capping layer **255** in the second recess **220**R may be formed.

Since the topmost portion **142**T of the bottom surface of the first gate spacer **142** is lower than the topmost portion **120**T' of the top surface of the topmost first channel, that is, the first channel **120**_d_, the topmost portion **150**T of the top surface of the first source/drain structure **150** may be lower than the topmost portion **120**T' of the top surface of the topmost first channel, that is, the first channel **120**_d_. In some embodiments, for example, when the topmost portion **242**T of the bottom surface of the second gate spacer **242** is formed lower than the topmost portion **220**T' of the top surface of the topmost second channel, that is, the second channel **220**_d_, the topmost portion **250**T of the top surface of the second source/drain structure **250** may be formed lower than the topmost portion **220**T' of the top surface of the topmost second channel, that is, the second channel **220**_d_. In an embodiment in which the topmost portion **242**T of the bottom surface of the second gate spacer **242** is instead formed at the same height as the topmost portion **220**T of the top surface of the topmost second channel, that is, the second channel **220**_d_, the topmost portion **250**T of the second source/drain structure **250** may be formed at the same height as the topmost portion **220**T of the top surface of the topmost second channel, that is, the second channel **220**_d_ or higher than the topmost portion **220**T of the top surface of the topmost second channel, that is, the second channel **220**_d_. Operations for growing the first source/drain structure **150** and the second source/drain structure **250** are the same as the operations described above with reference to FIGS. **11**A to **12**B.

Referring to FIGS. **25**A and **25**B, the interlayer insulation layer **90** may be formed on the first source/drain structure **150**, the second source/drain structure **250**, the first gate spacer **142**, the second gate spacer **242**, and the device isolation layer **60**. While the interlayer insulation layer **90** is being formed, the first dummy gate mask layer **183** (refer to FIG. **24**A) and the second dummy gate mask layer **283** (refer to FIG. **24**B) may also be removed. An operation for forming the interlayer insulation layer **90** is the same as the operation described above with reference to FIGS. **13**A and **13**B.

Referring to FIGS. **26**A and **26**B, the first opening OP**1** may be formed by removing the first dummy gate structure **180** (refer to FIG. **25**A) and the first sacrificial layers **184**_a_ to **184**_c_ (refer to FIG. **25**A), and the second opening OP**2** may be formed by removing the second dummy gate structure **280** (refer to FIG. **25**B) and the second sacrificial layers **284**_a_ to **284**_c_ (refer to FIG. **25**B). The first opening OP**1** may expose the top surfaces of the first channels **120**_a_ to **120**_d_, the bottom surfaces of the first channels **120**_b_ to **120**_d_, the inner side surfaces **142**I of the first gate spacers **142**, and inner side surfaces **146**I of the first inner spacers **146**, and the second opening OP**2** may expose the top surfaces of the second channels **220**_a_ to **220**_d_, the bottom surfaces of the second channels **220**_b_ to **120**_d_, the inner side surfaces **242**I of the second gate spacers **242**, and inner side surfaces **246**I of the second inner spacers **246**.

The first gate structure **130** (refer to FIG. **4**A) may be formed in the first opening OP**1**, and the second gate structure **230** (refer to FIG. **4**B) may be formed in the second opening OP**2**. For example, the gate insulation layers and the gate electrode layers may be sequentially formed on the portions of the first channels **120**_a_ to **120**_d_, the portions of the first gate spacers **142**, and the inner side surfaces **146**I of the first inner spacers **146** that are exposed in the first opening OP**1** and the portions of the second channels **220**_a_ to **220**_d_, the portions of the second gate spacers **242**, and the inner side surfaces **246**I of the second inner spacers **246** that are exposed in the second opening OP**2** and the gate insulation layers and the gate electrode layers may be planarized to expose the interlayer insulation layer **90**, thereby forming the first gate structure **130** (refer to FIG. **4**A) and the second gate structure **230** (refer to FIG. **4**B).

According to the method described above with reference to FIGS. **15**A to **26**B, the semiconductor device **2000** described above with reference to FIGS. **4**A and **4**B may be manufactured.

While the disclosure has been particularly shown and described with reference to embodiments thereof, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the following claims.

What is claimed is:

1. A semiconductor device comprising:

- a substrate;
- a plurality of channels on the substrate apart from one another in a vertical direction;
- a gate structure contacting the plurality of channels;
- a gate spacer on at least one side surface of the gate structure; and

a source/drain structure contacting the plurality of channels, the source/drain structure comprising one of a source structure and a drain structure,

wherein a topmost portion of a bottom surface of the gate spacer is lower than a topmost portion of a top surface of a topmost channel from among the plurality of channels,

a topmost portion of a top surface of the source/drain structure is lower than the topmost portion of the top surface of the topmost channel, and

wherein the topmost portion of the bottom surface of the gate spacer contacts the source/drain structure.

2. The semiconductor device of claim **1**, wherein

the gate spacer comprises an inner side surface contacting the gate structure and an outer side surface opposite to the inner side surface, and

the source/drain structure comprises a portion such that a distance from the portion of the source/drain structure to the gate structure in a horizontal direction is smaller than a distance from the outer side surface of the gate spacer to the gate structure in the horizontal direction.

3. The semiconductor device of claim **1**, wherein

the topmost portion of the bottom surface of the gate spacer is higher than a bottommost portion of a top surface of a bottommost channel from among the plurality of channels.

4. The semiconductor device of claim **1**, wherein the source/drain structure is doped with a p-type dopant.

5. The semiconductor device of claim **1**, wherein

a bottom surface of the gate structure contacts the topmost portion of the top surface of the topmost channel.

6. The semiconductor device of claim **1**, wherein

the topmost portion of the bottom surface of the gate spacer is higher than a bottom surface of the topmost channel from among the plurality of channels.

7. A semiconductor device comprising:

a substrate comprising a first region and a second region;

a plurality of first channels on the first region apart from one another in a vertical direction;

a plurality of second channels on the second region apart from one another in the vertical direction;

a first gate structure contacting the plurality of first channels;

a second gate structure contacting the plurality of second channels;

a first gate spacer on at least one side surface of the first gate structure;

a second gate spacer on at least one side surface of the second gate structure;

a first source/drain structure contacting the plurality of first channels; and

a second source/drain structure contacting the plurality of second channels,

wherein a topmost portion of a bottom surface of the first gate spacer is lower than a topmost portion of a top surface of a topmost first channel from among the plurality of first channels,

wherein a topmost portion of a top surface of the first source/drain structure is lower than the topmost portion of the top surface of the topmost first channel, and

wherein the topmost portion of a bottom surface of the first gate spacer contacts the first source/drain structure.

8. The semiconductor device of claim **7**, wherein

the first source/drain structure comprises a first source/drain layer and a first capping layer directly on the first source/drain layer, and

the second source/drain structure comprises a second source/drain layer, a third source/drain layer on the second source/drain layer, and a second capping layer on the third source/drain layer.

9. The semiconductor device of claim **8**, wherein a Si concentration of the first source/drain layer is lower than a Si concentration of the first capping layer, and

wherein a Si concentration of the second source/drain layer is lower than a Si concentration of the second capping layer.

10. The semiconductor device of claim **8**, wherein

a Si concentration of the third source/drain layer is lower than a Si concentration of the second source/drain layer.

11. The semiconductor device of claim **8**, wherein

the first source/drain layer and the second source/drain layer comprise a substantially same first composition, and

the first capping layer and the second capping layer comprise a substantially same second composition.

12. The semiconductor device of claim **8**, wherein

the first source/drain layer, the second source/drain layer, and the third source/drain layer comprise SiGe.

13. The semiconductor device of claim **8**, wherein

the first source/drain layer, the second source/drain layer, and the third source/drain layer comprise a p-type dopant.

14. The semiconductor device of claim **7**, wherein

a distance from the topmost portion of the top surface of the topmost first channel to a bottommost portion of a top surface of a bottommost first channel from among the plurality of first channels in the vertical direction is less than a distance from a topmost portion of a top surface of a topmost second channel to a bottommost portion of a top surface of a bottommost second channel from among the plurality of second channels in the vertical direction.

15. The semiconductor device of claim **7**, wherein

a topmost portion of a bottom surface of the second gate spacer is lower than a topmost portion of a top surface of a topmost second channel from among the plurality of second channels.

16. The semiconductor device of claim **7**, wherein

a height of a topmost portion of a bottom surface of the second gate spacer is greater than or equal to a height of a bottommost portion of a top surface of a bottommost second channel from among the plurality of second channels.

17. A semiconductor device comprising:

a substrate comprising a first region and a second region;

a plurality of first channels on the first region apart from one another in a vertical direction;

a plurality of second channels on the first region apart from one another in the vertical direction;

a plurality of third channels on the second region apart from one another in the vertical direction;

a plurality of fourth channels on the second region apart from one another in the vertical direction;

a first gate structure contacting the plurality of first channels;

a second gate structure contacting the plurality of second channels;

a third gate structure contacting the plurality of third channels and the plurality of fourth channels;

a first gate spacer on a side surface of the first gate structure;

a second gate spacer on a side surface of the second gate structure;

a third gate spacer on a side surface of the third gate structure;

a first source/drain structure contacting the plurality of first channels;

a second source/drain structure contacting the plurality of second channels; and

a third source/drain structure contacting the plurality of third channels and the plurality of fourth channels,

wherein a topmost portion of a bottom surface of the first gate spacer is lower than a topmost portion of a top surface of a topmost first channel from among the plurality of first channels,

a topmost portion of a top surface of the first source/drain structure is lower than the topmost portion of the top surface of the topmost first channel, and

wherein the topmost portion of a bottom surface of the first gate spacer contacts the first source/drain structure.

18. The semiconductor device of claim **17**, wherein

the first source/drain structure and the second source/drain structure are separated from one another, and

the third source/drain structure contacts the plurality of third channels and the plurality of fourth channels.

19. The semiconductor device of claim **17**, wherein

a horizontal distance between the plurality of first channels and the plurality of second channels is greater than a horizontal distance between the plurality of third channels and the plurality of fourth channels.

20. The semiconductor device of claim **17**, wherein

a length of the first source/drain structure in the vertical direction is less than a length of the third source/drain structure in the vertical direction.

21. The semiconductor device of claim **17**, wherein

the first source/drain structure comprises a first predetermined number of layers, and

the third source/drain structure comprises a second predetermined number of layers, the second predetermined number being greater than the first predetermined number.

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