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(54) **METHOD OF FORMING STACKED TRENCH CONTACTS AND STRUCTURES FORMED THEREBY**

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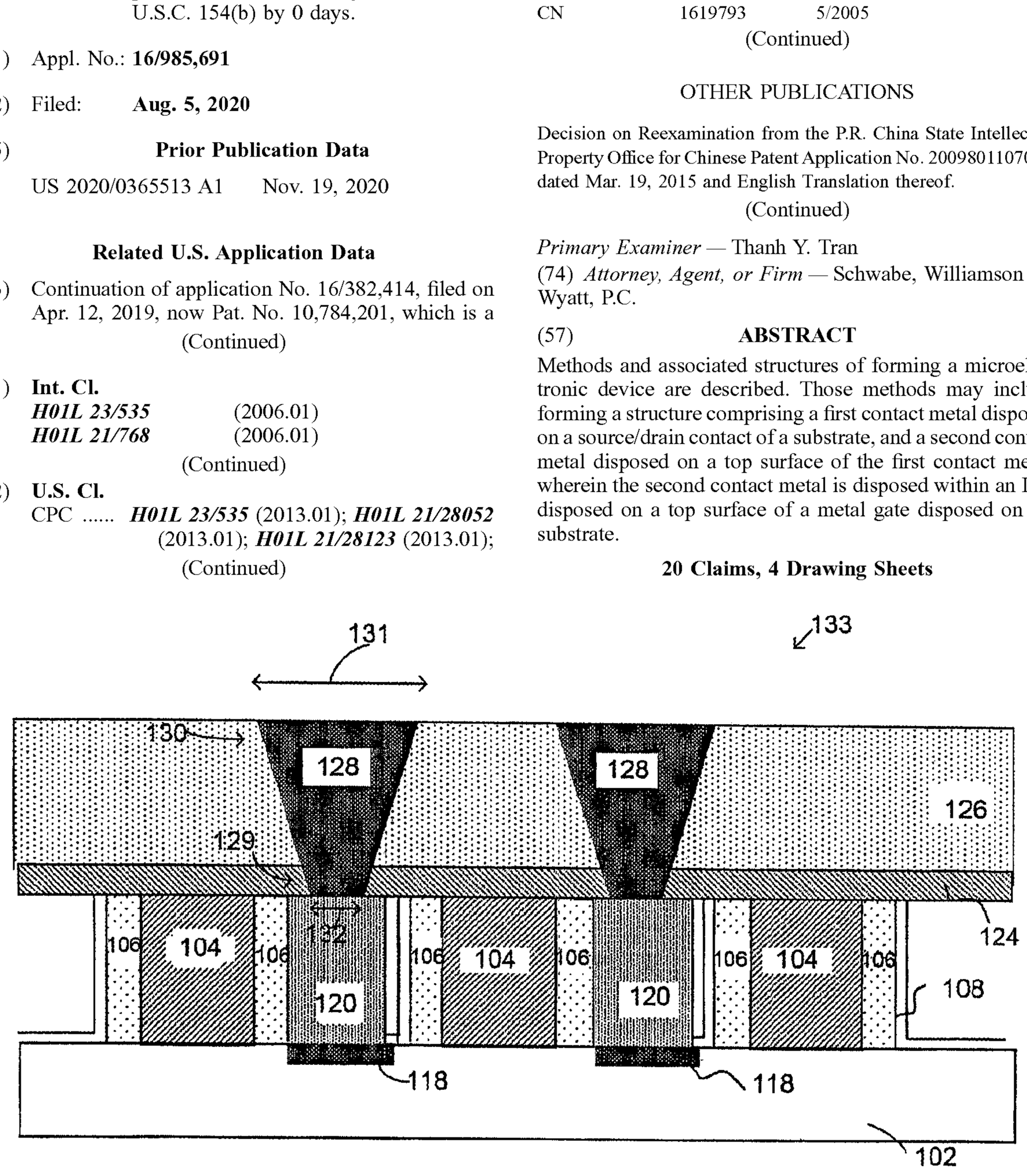
(57) **ABSTRACT**

Methods and associated structures of forming a microelectronic device are described. Those methods may include forming a structure comprising a first contact metal disposed on a source/drain contact of a substrate, and a second contact metal disposed on a top surface of the first contact metal, wherein the second contact metal is disposed within an ILD disposed on a top surface of a metal gate disposed on the substrate.

20 Claims, 4 Drawing Sheets



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continuation of application No. 15/925,151, filed on Mar. 19, 2018, now Pat. No. 10,297,549, which is a continuation of application No. 15/419,141, filed on Jan. 30, 2017, now Pat. No. 9,922,930, which is a continuation of application No. 15/220,270, filed on Jul. 26, 2016, now Pat. No. 9,559,060, which is a continuation of application No. 14/994,109, filed on Jan. 12, 2016, now Pat. No. 9,437,546, which is a continuation of application No. 14/581,498, filed on Dec. 23, 2014, now Pat. No. 9,252,267, which is a continuation of application No. 14/284,808, filed on May 22, 2014, now Pat. No. 9,293,579, which is a continuation of application No. 12/215,991, filed on Jun. 30, 2008, now Pat. No. 8,803,245.

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See application file for complete search history.

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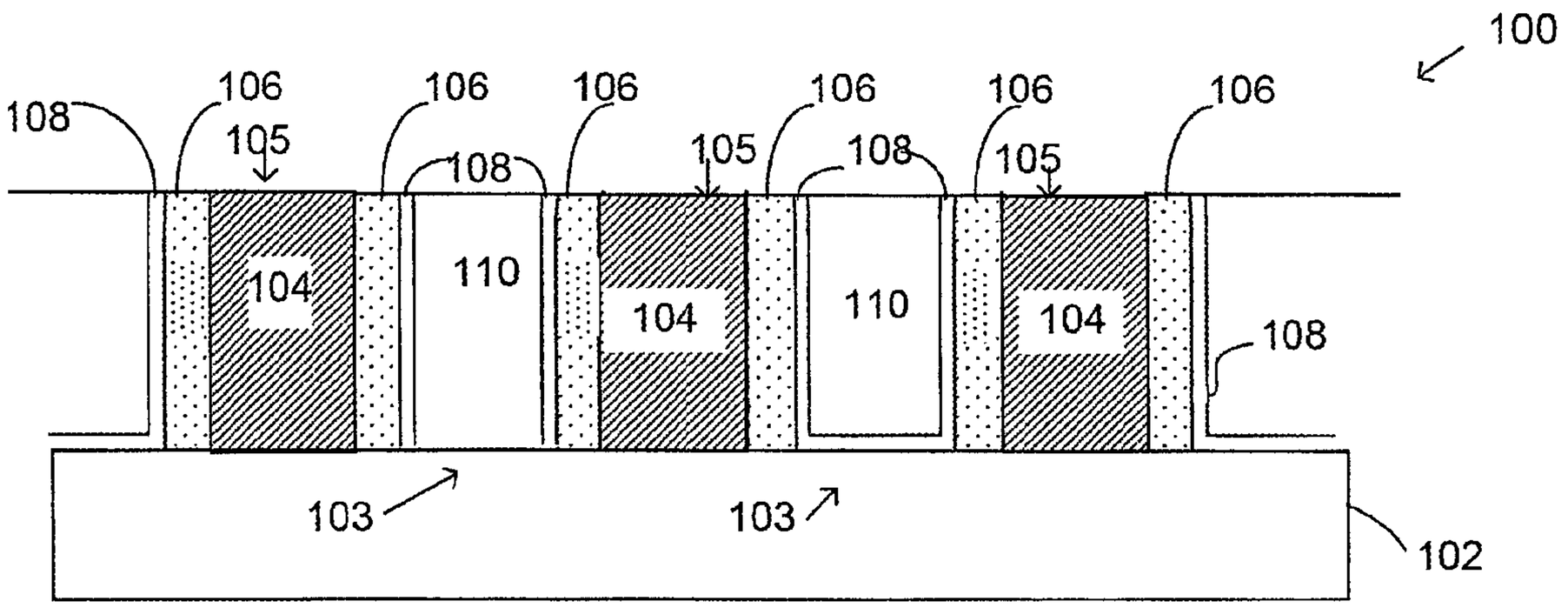

100
106
108
105
104
110
103
102

FIG. 1a

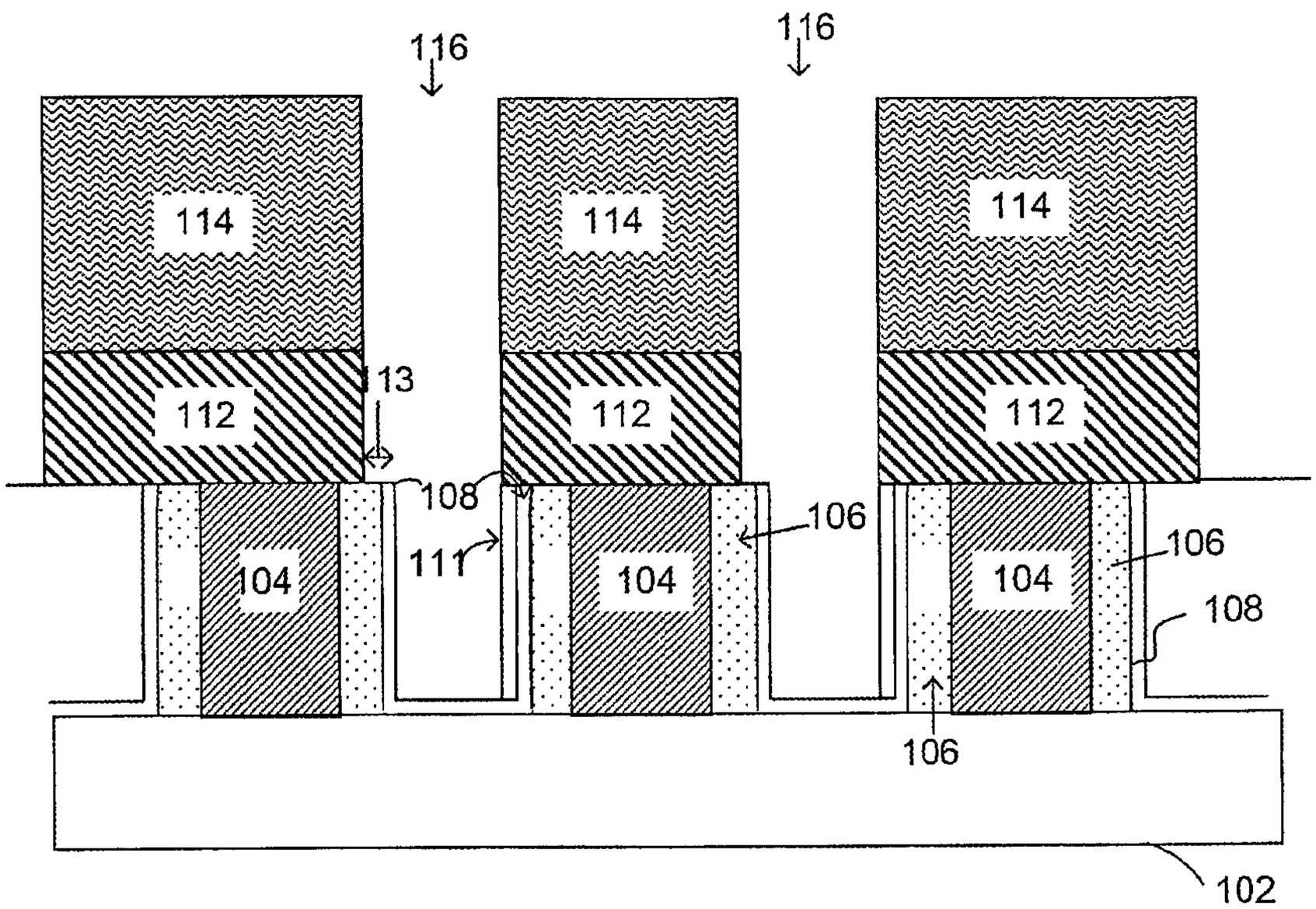
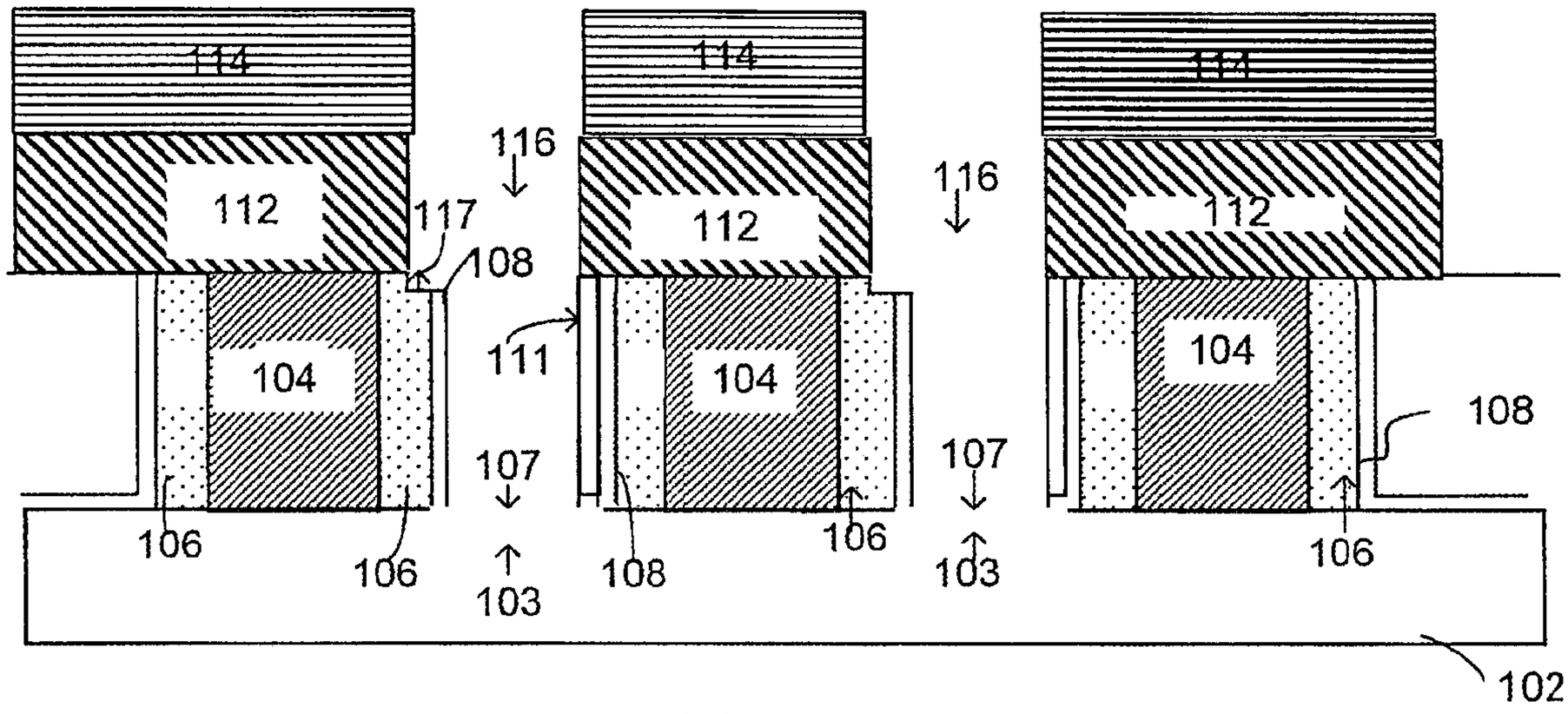

116
114
112
13
108
111
104
106
102

FIG. 1b


114
112
116
117
108
111
104
107
106
106
103
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106
103
114
112
116
104
108
106
102

FIG. 1c

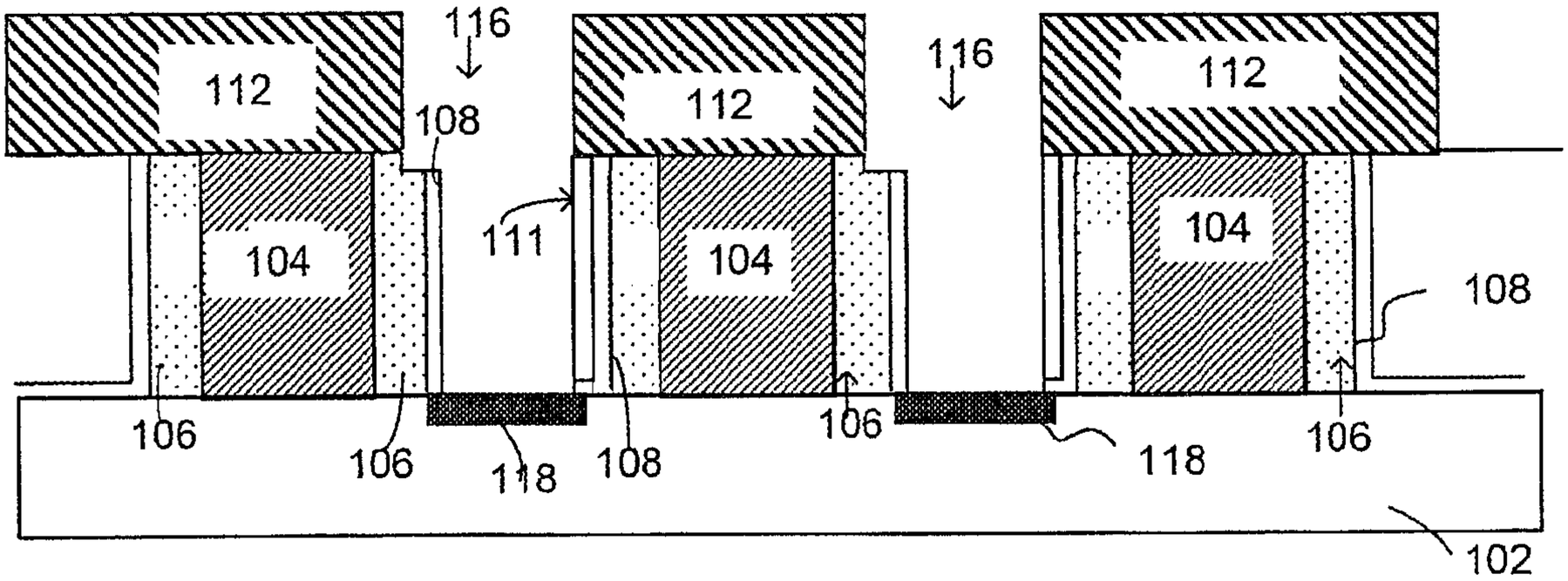
116
112
108
111
104
106
106
118
108
106
118
116
112
104
108
106
102

FIG. 1d

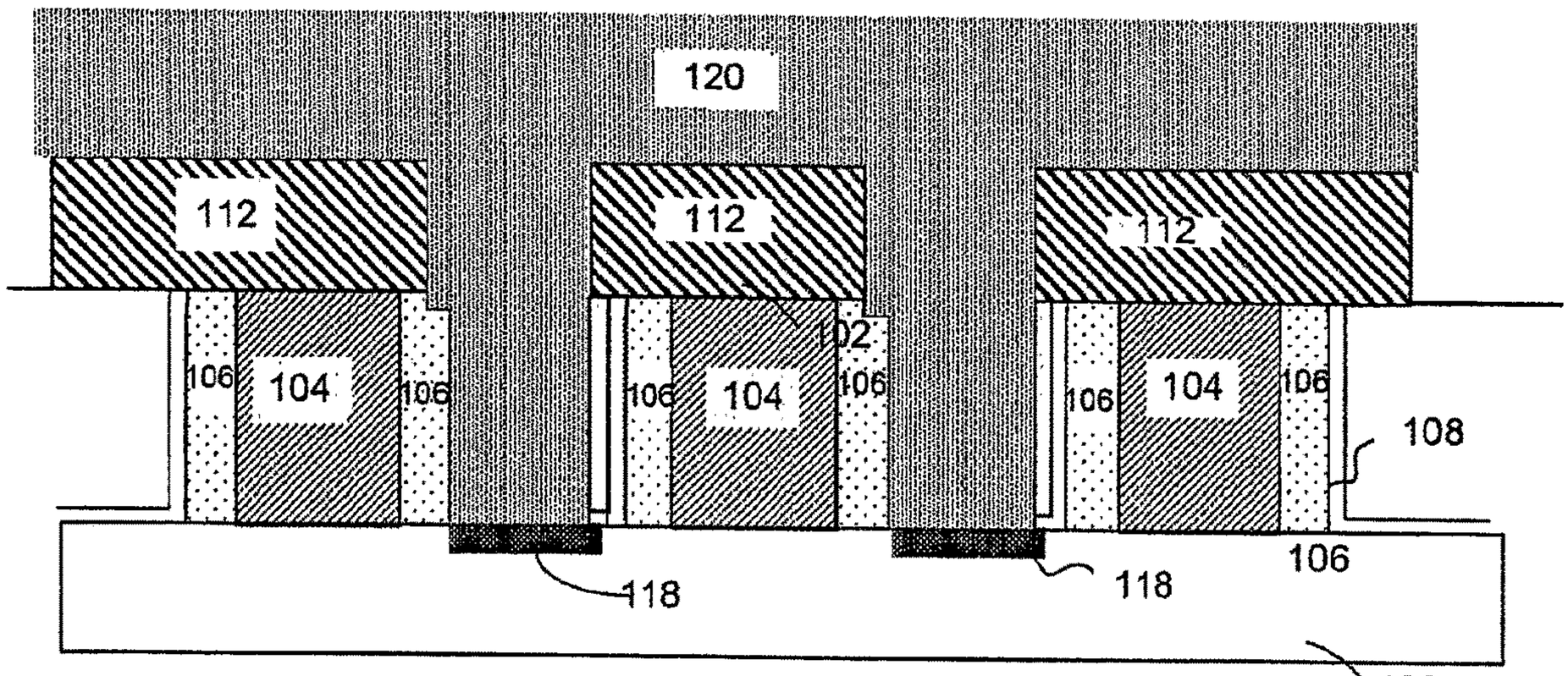
120
112
112
112
106
104
106
106
104
102
106
104
106
108
106
118
118
102

FIG. 1e

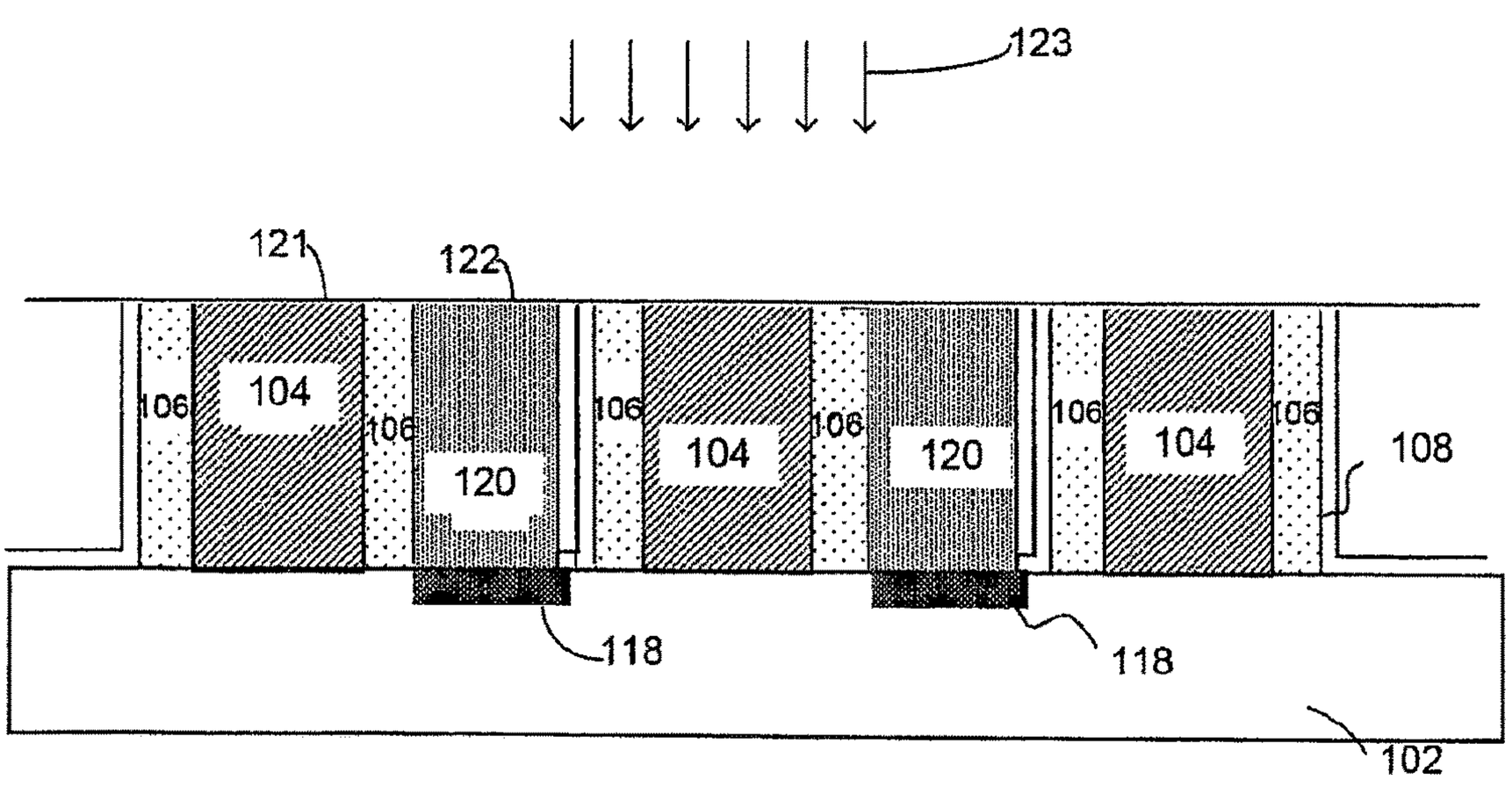
123
121
122
106
104
106
106
120
106
104
106
106
104
106
108
118
118
102

FIG. 1f

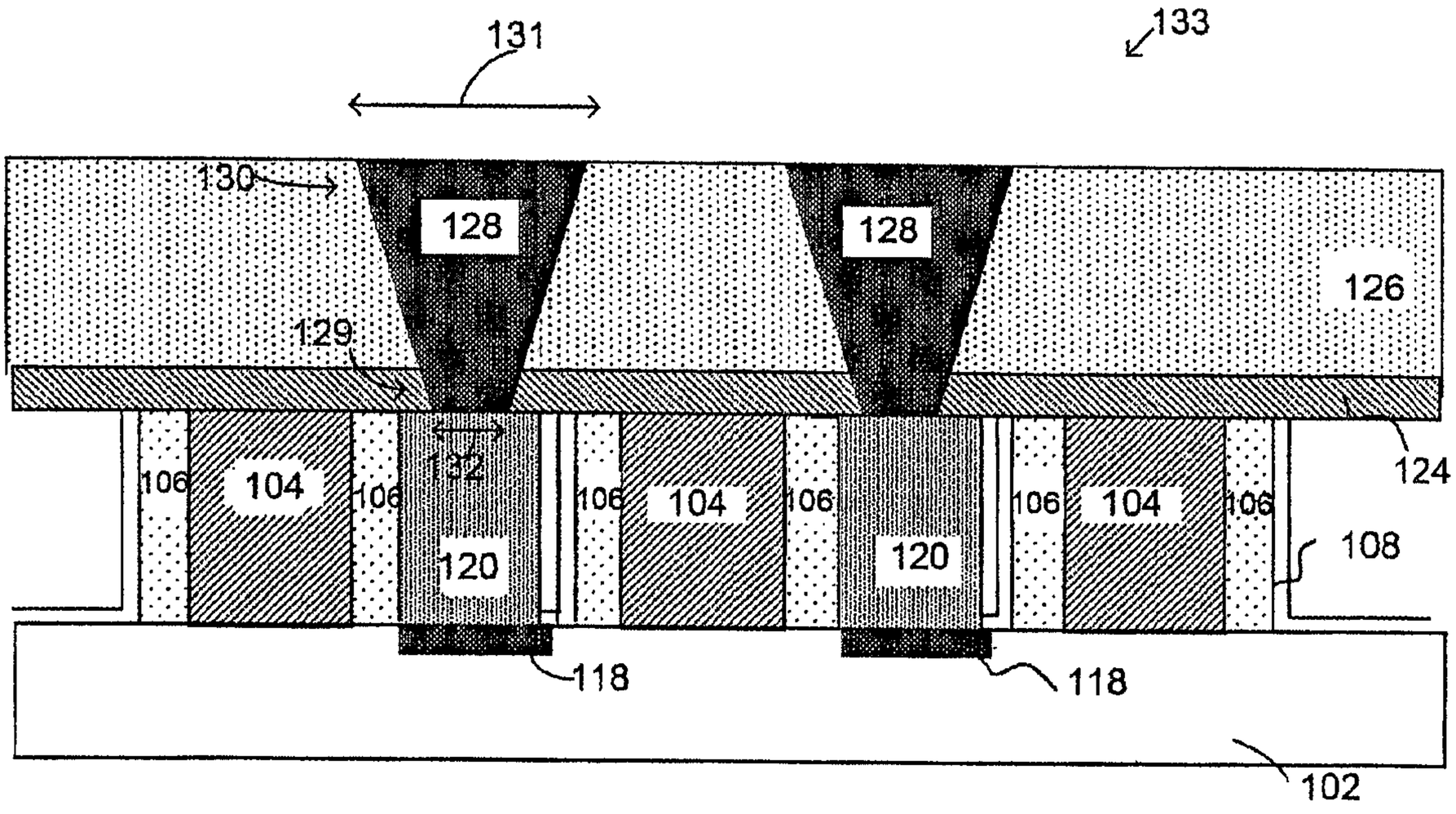
131
133
130
128
128
126
129
124
106
104
106
132
106
104
106
106
104
106
120
120
108
118
118
102

FIG. 1g

METHOD OF FORMING STACKED TRENCH CONTACTS AND STRUCTURES FORMED THEREBY

RELATED APPLICATIONS

This application is a continuation of application Ser. No. 16/382,414 filed Apr. 12, 2019, which is a continuation of application Ser. No. 15/925,151 filed Mar. 19, 2018, now U.S. Pat. No. 10,297,549, which is a continuation of application Ser. No. 15/419,141 filed Jan. 30, 2017, now U.S. Pat. No. 9,922,930, which is a continuation of application Ser. No. 15/220,270 filed Jul. 26, 2016, now U.S. Pat. No. 9,559,060, which is a continuation of application Ser. No. 14/994,109 filed Jan. 12, 2016, now U.S. Pat. No. 9,437,546, which is continuation of application Ser. No. 14/581,498 filed Dec. 23, 2014, now U.S. Pat. No. 9,252,267, which is a continuation of application Ser. No. 14/284,808 filed May 22, 2014, now U.S. Pat. No. 9,293,579, which is a continuation of application Ser. No. 12/215,991 filed Jun. 30, 2008, now U.S. Pat. No. 8,803,245. Each of these applications is incorporated herein by reference in its entirety.

BACKGROUND

Contact to gate shorts become an increasingly difficult problem for integrated circuits with scaled dimensions. While a metal gate process which forms a salicide through the contact hole may be beneficial in reducing such shorts, a contact process that increases the contact to gate registration margin is necessary to further reduce the contact to gate shorts to a manufacturable level.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIGS. **1***a*-**1***g* represents structures according to an embodiment of the present invention.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings that show, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that the various embodiments of the invention, although different, are not necessarily mutually exclusive. For example, a particular feature, structure, or characteristic described herein, in connection with one embodiment, may be implemented within other embodiments without departing from the spirit and scope of the invention. In addition, it is to be understood that the location or arrangement of individual elements within each disclosed embodiment may be modified without departing from the spirit and scope of the invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, appropriately interpreted, along with the full range of equivalents to which the claims are entitled. In the drawings, like numerals refer to the same or similar functionality throughout the several views.

Methods and associated structures of forming a microelectronic structure are described. Those methods may include forming a contact opening in a first ILD disposed on a substrate, wherein a source/drain contact area is exposed, forming a silicide on the source/drain contact area, forming a first contact metal in the contact opening to fill the contact opening, polishing the first contact metal to planarize a top surface of the first contact metal with a top surface of a gate disposed on the substrate, depositing a second ILD on the top surface of the gate, forming a second contact opening in the second ILD, and forming a second contact metal in the second contact opening, wherein the first and second contact openings are conductively coupled. Methods of the present invention increase the contact to gate registration margin and reduce contact to gate shorts.

Methods of the present invention are depicted in FIGS. **1***a*-**1***g*. FIG. **1***a* shows a cross section of a portion of a transistor structure **100** comprising a substrate **102**, and a gate **104**, which may comprise a metal gate in some embodiments, and may comprise such metal gate materials as hafnium, zirconium, titanium, tantalum, or aluminum, or combinations thereof, for example. The gate **104** may comprise a top surface **105**. The substrate **102** may be comprised of materials such as, but not limited to, silicon, silicon-on-insulator, germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, gallium antimonide, or combinations thereof.

The transistor structure **100** may further comprise a spacer material **106**, that may be adjacent and in direct contact with the gate **104**. The spacer material **106** may comprise a dielectric material in some cases, such as but not limited to silicon dioxide and/or silicon nitride materials. The transistor structure **100** may further comprise a nitride etch stop layer (nesl) **108**, that may be adjacent and in direct contact with the spacer material **106**. The nesl **108** may serve as an etch stop layer in some embodiments. The transistor structure **100** may further comprise a first interlayer dielectric (ILD) **110** that may serve as an isolation layer in some embodiments, and may be disposed adjacent to and in direct contact with the nesl **108** in some cases.

A sacrificial stopping layer **112** may be formed on the top surface **105** of the gate **104**, that may comprise a nitride and/or a silicon carbide material in some cases (FIG. **1***b*). A resist layer **114** may be formed on the stopping layer **112** utilizing any suitable patterning process, such as a photolithography process, for example. The resist layer **114** may be formed to define an opening **116**, such as a trench contact opening **115**, for a source/drain region **103** of the substrate **100**. A portion of the stopping layer **112** and a portion of the ILD **110** may be disposed on top surfaces of the gate **104**, the adjacent spacer material and on the adjacent nesl that are disposed on the substrate.

In an embodiment, a dry etch process may be utilized to form the opening **116**, in which portions of the stopping layer **112** and the first ILD **110** may be removed. In an embodiment, the etching process may comprise an oxide etch that may be selective to the nitride etch stop layer (nesl) **108** and to the spacer material **106**, and may remove the first ILD **110** in a substantially anisotropic manner, leaving the nesl **108** and the spacer material **106** substantially intact. In other words, the oxide ILD may etch at a much higher etch rate in the etch process chemistry than the spacer material **106** and the nesl **108**. In an embodiment, a portion of the stopping layer **112** and a portion of the ILD **110** may be removed that are disposed on top surfaces of the gate **104**, the an adjacent spacer **106**, and on the adjacent nesl **108**, to form the contact opening **116**.

The patterning process may result in a mis-registration of the resist layer **114**, wherein the resist layer **114** may be mis-aligned so that a portion **113** of the spacer material **106** may be exposed during the formation of the opening **115**, and a portion **111** of the first ILD **110** may remain covered with the resist layer **114**. The amount of mis-registration of the resist layer **114** may vary depending upon the particular application, but may become more significant as the aspect ratio of the opening **116** increases. For example, microelectronic devices comprising small geometries will be more likely to form a short between the contact and the gate due to resist layer **114** mis-alignment.

Subsequently, the nitride etch stop layer **108** may be removed that is disposed on a portion of the source/drain region **103** of the substrate **100** utilizing a nitride etching process, for example, so that a source/drain contact area **107** may be exposed (FIG. **1***c*). Alternatively, the nitride etch stop layer **108** may not be present on the substrate **102**, and thus the nesl **108** will not need to be removed. In another embodiment, the nesl etch may be optional, depending on the selectivity of the ILD removal process, such that when the ILD etch is selective to the substrate, the nesl etch does not need to be performed.

A depth **117** into the exposed portion **113** of the spacer material **106** may be formed by the nesl **108** etch and/or the ILD etch due to the mis-registration of the resist layer **114**. The depth **117** that may be created may vary depending upon the particular process parameters. In an embodiment, the depth **117** correlates/corresponds to an etch time of the contact etch (nesl and/or ILD etch). The resist layer **114** may then be removed and a salicide **118** may be formed on/in the source/drain contact area **107** using any suitable salicide process as are known in the art, such as but not limited to a nickel salicide process and/or other such salicide process (FIG. **1***d*).

A first contact metal **120** may be formed on the salicide **118** and may fill the opening **116** (FIG. **1***e*). In an embodiment, the first contact metal **120** may be formed utilizing a process possessing good gap fill properties to ensure that there are little to no voids formed in the contact opening **116**. Such a process may include a chemical vapor deposition (CVD) process, for example. A polishing process **123** may subsequently be performed, such as a chemical mechanical polishing (CMP) process, for example, to remove the first contact metal **120** (FIG. **1***f*) and the stopping layer **112**. The first contact metal may comprise at least one of tungsten, titanium, titanium nitride and titanium tungsten in some cases, but may comprise any suitable contact material, according to the particular application.

In an embodiment, the first contact metal **120** may be planarized with a planarized top surface **121** of the gate **104**, i.e., it may be polished by the polishing process **123** so that a top surface **122** of the first contact metal **120** may be planar with the planarized top surface **121** of the gate **104**. The polishing process **123** needs to comprise a sufficient amount of over-polish time so that any stringers that could connect the contact metal **120** with the gate **104** are removed. The polishing process **123** additionally removes the depth **117** of the exposed portion **113** of the spacer material **106** that was due to the mis-registration of the resist layer **114** (referring back to FIG. **1***c*). In an embodiment, the first contact metal **120** may comprise a non-tapered first contact metal **120**.

An additional gate etch stop layer **124** may be formed on the planarized top surface **121** of the gate **104**, and on the top surface **122** of the contact metal **120** (FIG. **1***g*). A second ILD **126** may be formed on the additional gate etch stop layer **124**. A second opening may be formed (not shown) that may be filled with a second contact metal **128**, that may be conductively coupled and may form an ohmic contact with the first contact metal **120**, and that may be disposed on the top surface **122** of the first contact metal. The second opening may be formed such that the second contact metal **128** can be tapered and a bottom portion **129** of the second contact metal **128** can be very small compared to a top portion **130** of the second contact metal **128**, since the salicide does not have to be formed through this second opening.

In an embodiment, the top portion **130** comprises a larger diameter **131** than a diameter **132** of the bottom portion **129** of the second contact metal **128**. The large taper of the second contact metal **128** may increase the contact-to-gate registration window significantly compared to prior art single contact processes. Thus, a stacked contact structure **133** may be formed that is higher than the gate **104**. The metal to metal contact of the first contact structure **120** and the second contact structure **128** affords much more flexibility on the shape of the stacked contact structure **133** (that may comprise a vertically stacked dual contact structure) within a transistor structure, thus increasing the amount of mis-registration error process window without creating the possibility of touching (shorting) the gate **104**.

Embodiments of the present invention enable a simple, unique method for integrating a stacked trench contact with a metal gate process, such as a dual metal gate process, for example, that increases contact to gate registration margin and decreases the aspect ratio of the contact during a salicide process. In an embodiment, the source drain trench contact structure consists of two vertically stacked contacts. The metal gate may be formed before the first source/drain contact, a salicide may be formed after the first source/drain contact is opened and before the second source/drain contact opening is formed. Prior art contact processes have used a single trench contact process, which may not be scalable to very small technology nodes.

Further advantages of this invention include the enabling of the formation of larger contacts with better contact to gate registration margin with relatively small process changes as compared with prior art processing. The embodiments of the present invention allow for an increased process window for contact mis-alignment that will not lead to a change in overlap capacitance of a microelectronic device, such as a transistor, fabricated according to the methods of the present invention.

Although the foregoing description has specified certain steps and materials that may be used in the method of the present invention, those skilled in the art will appreciate that many modifications and substitutions may be made. Accordingly, it is intended that all such modifications, alterations, substitutions and additions be considered to fall within the spirit and scope of the invention as defined by the appended claims. In addition, it is appreciated that certain aspects of microelectronic structures are well known in the art. Therefore, it is appreciated that the Figures provided herein illustrate only portions of exemplary microelectronic structures that pertain to the practice of the present invention. Thus the present invention is not limited to the structures described herein.

What is claimed is:

1. An integrated circuit structure comprising:

a gate structure having an uppermost surface;

a first region on a first side of the gate structure, and a second region on a second side of the gate structure, wherein the first region is one of a source region or a

drain region, and wherein the second region is the other of the source region or the drain region;

a first spacer and a second spacer, wherein the gate structure is at least partially between the first and second spacers, and wherein the first and second spacers have corresponding uppermost surfaces co-planar with the uppermost surface of the gate structure;

a nitride material, such that the first spacer is laterally between the nitride material and the gate structure, the nitride material compositionally different from the first spacer;

one or more layers comprising one or more dielectric materials above the gate structure, the first and second spacers, and the nitride layer, wherein one of the one or more layers is in contact with the uppermost surface of the gate structure and with the uppermost surfaces of the first and second spacers; and

a contact structure above the first region, the contact structure extending through the one or more layers, wherein at least a section of the contact structure extending through the one or more layers has a tapered shape, such that a horizontal width of an upper portion of at least the section of the contact structure is larger than a horizontal width of a lower portion of at least the section of the contact structure.

2. The integrated circuit structure of claim **1**, wherein at least the section of the contact structure extending through the one or more layers is a first section of the contact structure, wherein the contact structure comprises:

a second section that is below the one or more layers, wherein a smallest horizontal width of the second section is less than the horizontal width of the lower portion of the first section of the contact structure.

3. The integrated circuit structure of claim **2**, wherein the second section of the contact structure is either not tapered, or less tapered relative to the first section of the contact structure.

4. The integrated circuit structure of claim **2**, wherein the nitride material is laterally between at least a part of the second section of the contact structure and the first spacer.

5. The integrated circuit structure of claim **4**, wherein the nitride material is in direct contact with one or both the first spacer and/or at least the part of the second section of the contact structure.

6. The integrated circuit structure of claim **2**, wherein an interface between the first and second sections of the contact structure is free of silicide.

7. The integrated circuit structure of claim **1**, further comprising:

a region comprising silicide between the contact structure and the first region.

8. The integrated circuit structure of claim **1**, wherein the contact structure is a first contact structure, and wherein the integrated circuit structure further comprises:

a second contact structure over the second region, the second contact structure extending through the one or more layers, wherein at least a section of the second contact structure extending through the one or more layers has a tapered shape, such that a horizontal width of an upper portion of at least the section of the second contact structure is larger than a horizontal width of a lower portion of at least the section of the second contact structure.

9. The integrated circuit structure of claim **1**, wherein the one or more layers includes at least a first layer comprising a first dielectric material, and a second layer comprising a second dielectric material, the first layer below the second layer.

10. The integrated circuit structure of claim **9**, first dielectric material comprises another nitride material.

11. The integrated circuit structure of claim **9**, wherein the second dielectric material is compositionally different from the first dielectric material.

12. The integrated circuit structure of claim **1**, wherein the first and/or second spacers comprise silicon and one or more of nitrogen and oxygen.

13. The integrated circuit structure of claim **1**, wherein the nitride material has a first etch selectivity, and the first spacer has a second etch selectivity different from the first etch selectivity.

14. The integrated circuit structure of claim **1**, wherein the gate structure comprises one or more of hafnium, zirconium, titanium, tantalum, or aluminum.

15. The integrated circuit structure of claim **1**, wherein the contact structure comprises one or more of nitrogen, tungsten, titanium, or tungsten.

16. An integrated circuit structure comprising:

a gate structure;

a body comprising semiconductor material below the gate structure;

a first contact structure and a second contact structure;

a first dielectric material between the first contact structure and the gate structure, the first dielectric material also between the second contact structure and the gate structure; and

a second dielectric material comprising nitrogen and that is compositionally different from the first dielectric material, the second dielectric material laterally between the first dielectric material and the first contact structure, and not laterally between the first dielectric material and the second contact structure.

17. The integrated circuit structure of claim **16**, further comprising:

a first layer comprising a third dielectric material, the first layer above and in contact with top surfaces of the gate structure, the first dielectric material, and the second dielectric material; and

a second layer comprising a fourth dielectric material, the second layer above the first layer.

18. The integrated circuit structure of claim **17**, wherein:

the first contact structure comprises (i) a lower section that is below the first layer, and (ii) an upper section that extends through the first and second layers;

the upper section of the first contact structure is in contact with the lower section of the first contact structure;

the upper section is tapered relatively more than the lower section; and

a bottom surface of the upper section has a horizontal width that is less than a minimum horizontal width of the lower section.

19. An integrated circuit structure comprising:

a gate structure including a gate electrode and a high-k gate dielectric, the gate structure having an uppermost surface;

a source region;

a drain region;

a first spacer and a second spacer, the gate structure at least partially laterally between the first and second spacers, wherein the first and second spacers have corresponding uppermost surfaces co-planar with the uppermost surface of the gate structure;

a first contact structure over the source region;

a second contact structure above the first contact structure, the second contact structure having a top portion that is horizontally wider than a bottom portion of the second contact structure;

a third contact structure over the drain region;

a fourth contact structure above the third contact structure, the fourth contact structure having a top portion that is horizontally wider than a bottom portion of the fourth contact structure;

a first dielectric layer above the gate structure, the first spacer, and the second spacer, at least a portion of the first dielectric layer between the bottom portion of the second contact structure and the bottom portion of the fourth contact structure, wherein the first dielectric layer is in contact with the uppermost surface of the gate structure and with the uppermost surfaces of the first and second spacers; and

a second dielectric layer above the first dielectric layer, at least a portion of the second dielectric layer between the top portion of the second contact structure and the top portion of the fourth contact structure.

20. The integrated circuit structure of claim **19**, further comprising:

a nitride layer laterally between the first contact structure and the gate structure.

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