US011264454B2

(12) **United States Patent**
Yoon et al.

(10) **Patent No.: US 11,264,454 B2**
(45) **Date of Patent: Mar. 1, 2022**

(54) **INTEGRATED CIRCUIT DEVICE AND METHOD OF MANUFACTURING THE SAME**

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(73) Assignee: **SAMSUNG ELECTRONICS CO., LTD.**, Suwon-si (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 19 days.

(21) Appl. No.: **16/719,175**

(22) Filed: **Dec. 18, 2019**

(65) **Prior Publication Data**

US 2020/0135850 A1 Apr. 30, 2020

Related U.S. Application Data

(63) Continuation of application No. 15/881,863, filed on Jan. 29, 2018, now Pat. No. 10,541,302.

(30) **Foreign Application Priority Data**

May 31, 2017 (KR) 10-2017-0067634

(51) **Int. Cl.**
H01L 27/11573 (2017.01)
H01L 29/06 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 29/0649*** (2013.01); ***H01L 21/76232*** (2013.01); ***H01L 27/10894*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC ... H01L 21/762–765; H01L 21/823431; H01L 21/823878; H01L 27/108–10897;
(Continued)

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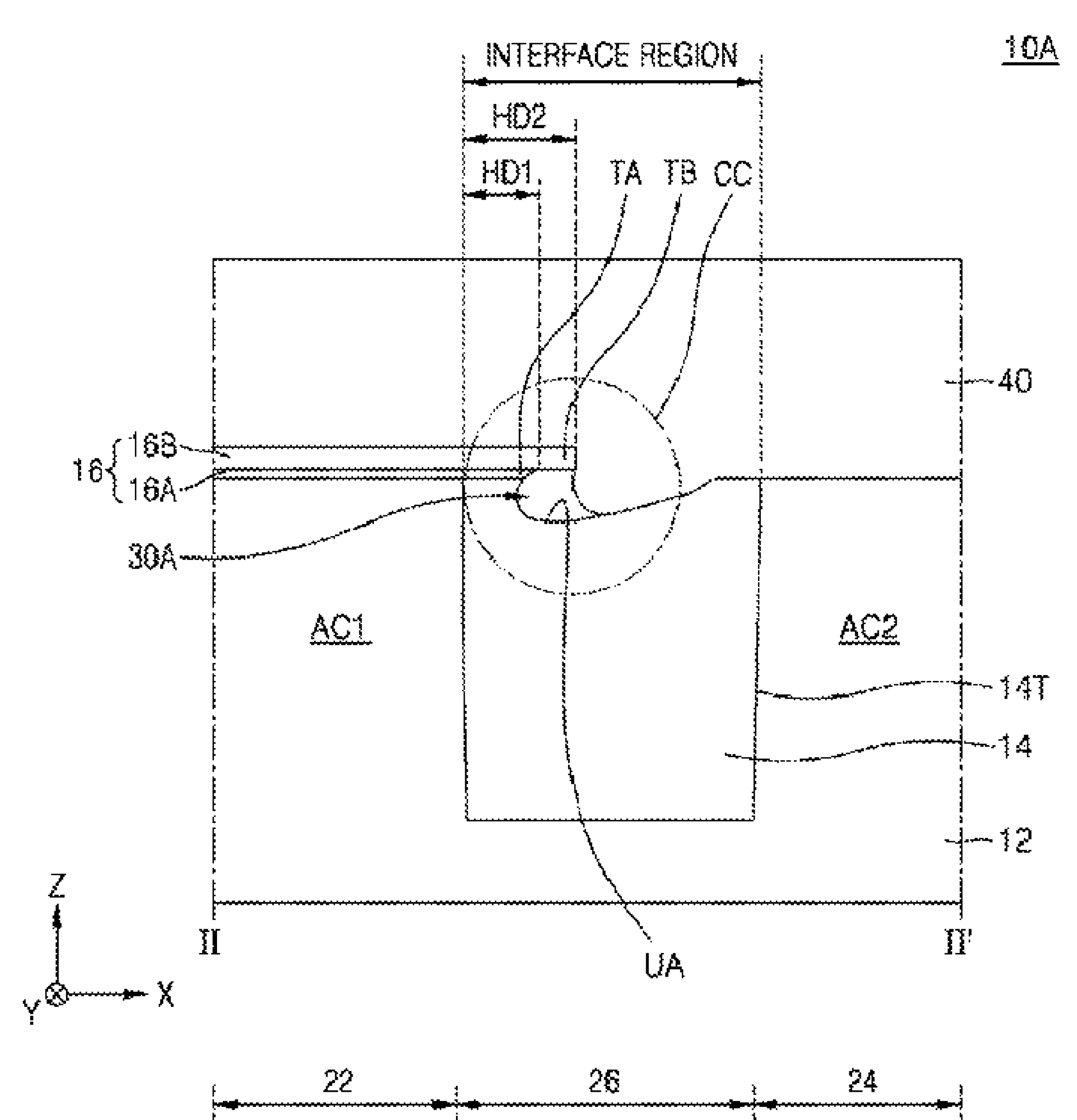
Primary Examiner — Eric A. Ward
(74) *Attorney, Agent, or Firm* — F. Chau & Associates, LLC

(57) **ABSTRACT**

An integrated circuit device includes a substrate having a first region and a second region separated from each other along a direction parallel to an upper surface of the substrate. An interface device isolation layer fills an interface trench in an interface region between the first region and the second region and defines a portion of a first active area positioned in the first region and a portion of a second active area positioned in the second region. An insulation pattern extends from the first region to an upper portion of the interface device isolation layer. The insulation pattern covers the first active area and at least a portion of the interface device isolation layer. The insulation pattern defines an undercut area on an upper surface of the interface device isolation layer. A buried pattern substantially fills the undercut region.

19 Claims, 31 Drawing Sheets



(51) **Int. Cl.**

H01L 21/762	(2006.01)
H01L 27/108	(2006.01)
G11C 11/408	(2006.01)

(52) **U.S. Cl.**
CPC ***H01L 27/10897*** (2013.01); *G11C 11/4085* (2013.01); *H01L 27/10814* (2013.01)

(58) **Field of Classification Search**
CPC H01L 29/0653; H01L 29/66681–66704; H01L 29/7816–7826; H01L 27/115–11597; H01L 21/761–76297; H01L 21/76224–76237; H01L 21/823481; H01L 27/10894; H01L 27/11526–11546; H01L 27/10897; H01L 29/0649–0653
See application file for complete search history.

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KR	1020150121767	10/2015

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FIG. 1

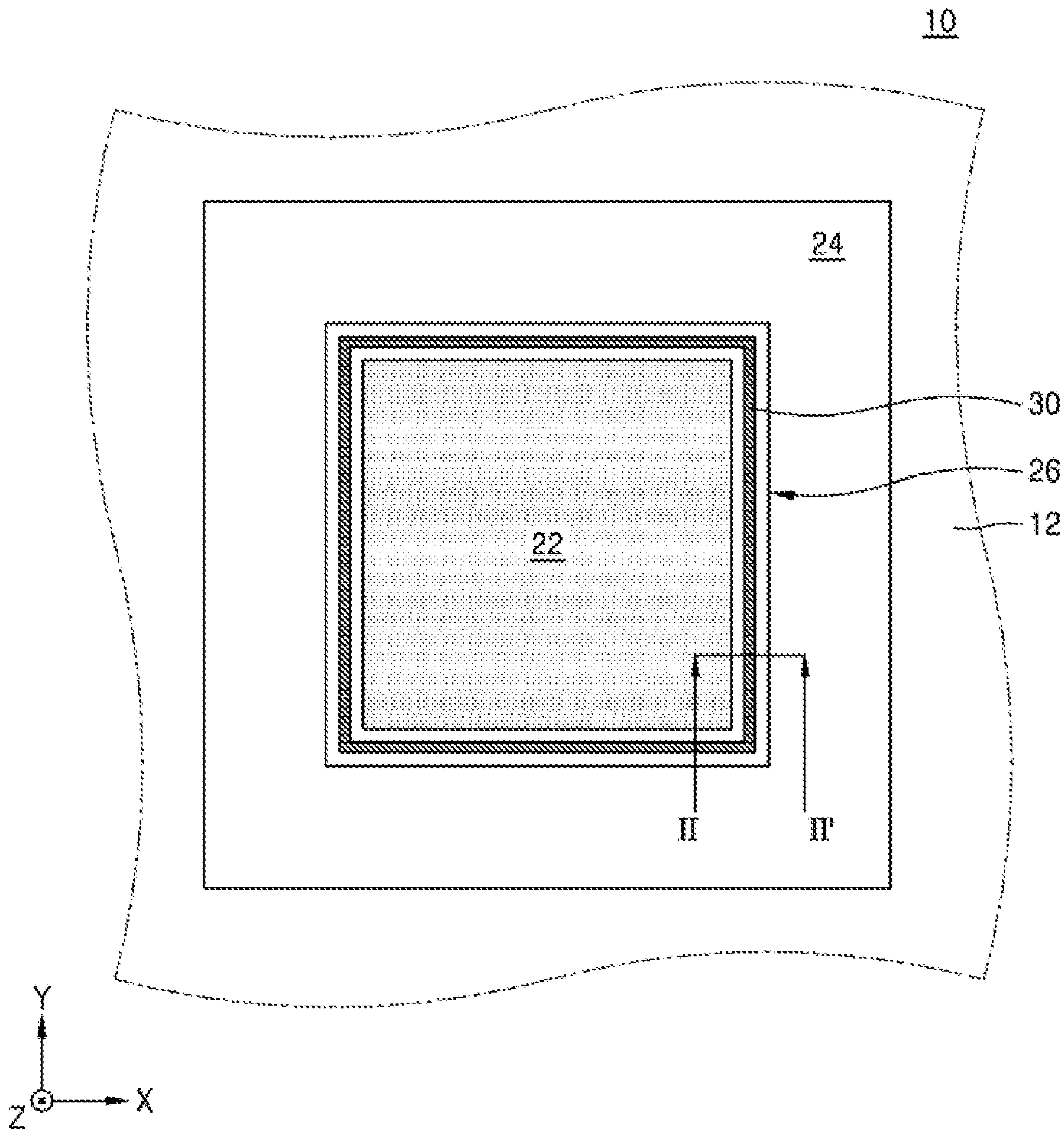


FIG. 2A

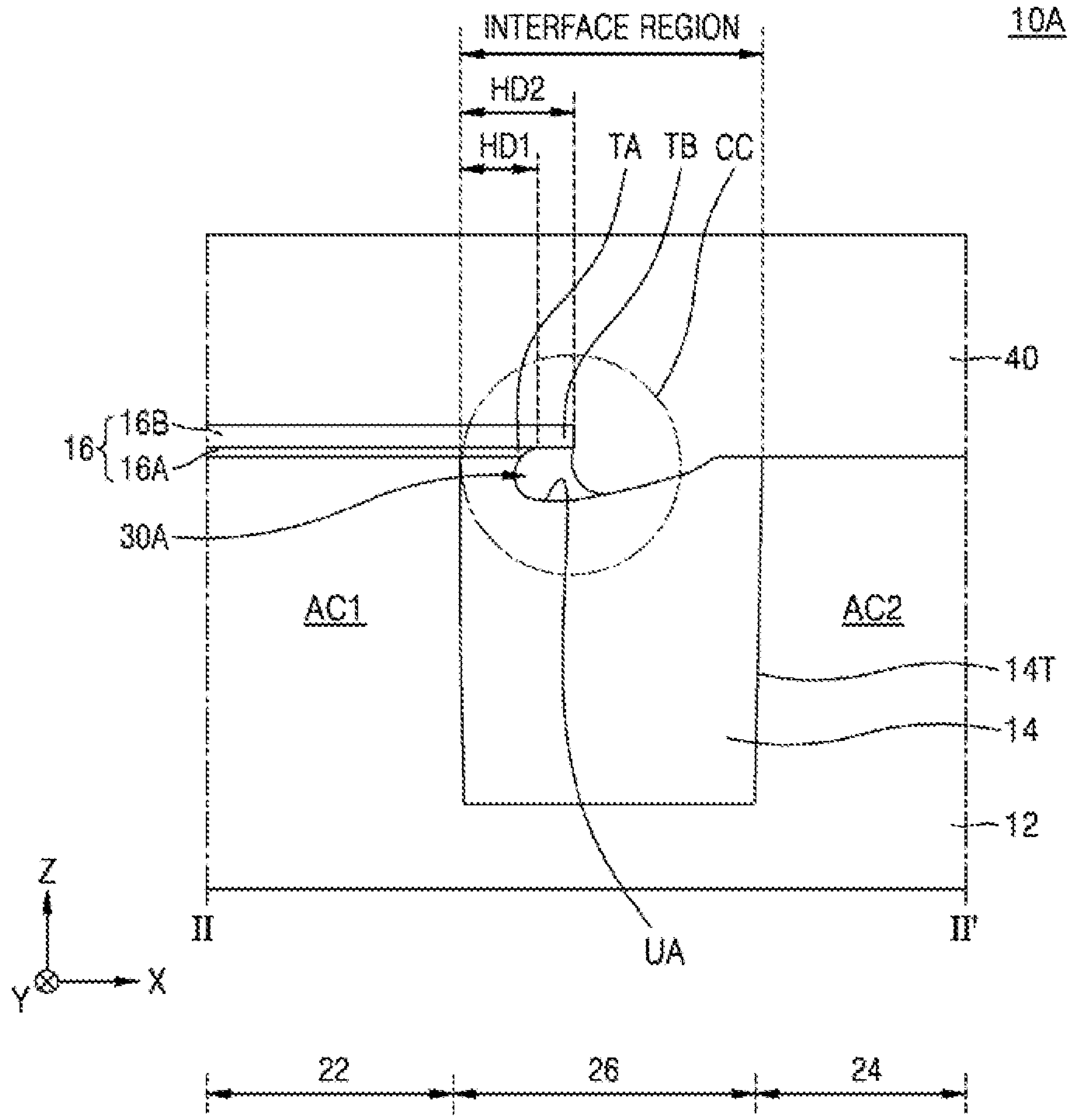

INTERFACE REGION
10A
HD2
HD1
TA
TB
CC
40
16
16B
16A
30A
AC1
AC2
14T
14
12
Z
Y
X
II
II'
UA
22
26
24

FIG. 2B

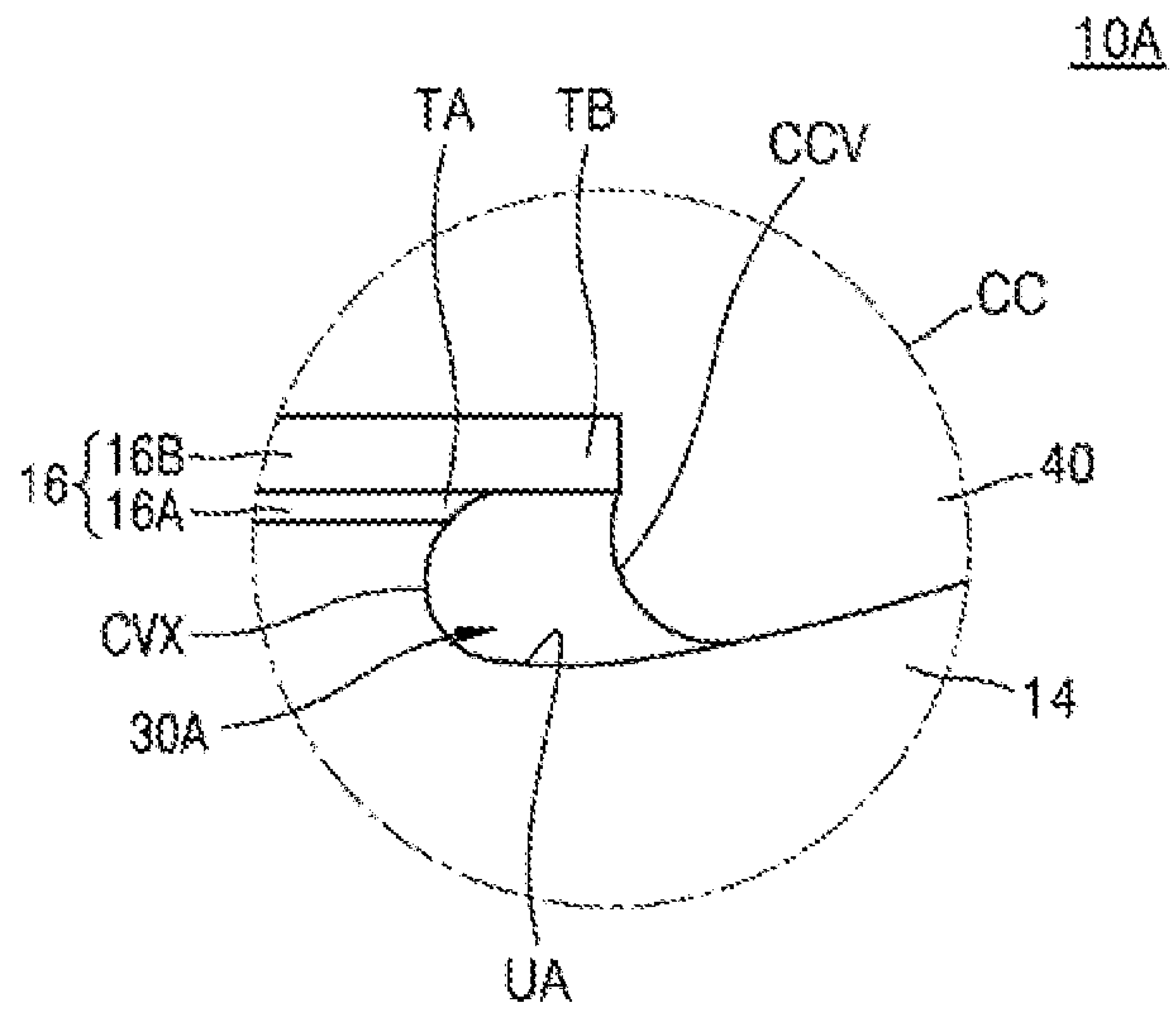

10A
TA
TB
CCV
CC
16
16B
16A
40
CVX
30A
14
UA

FIG. 3

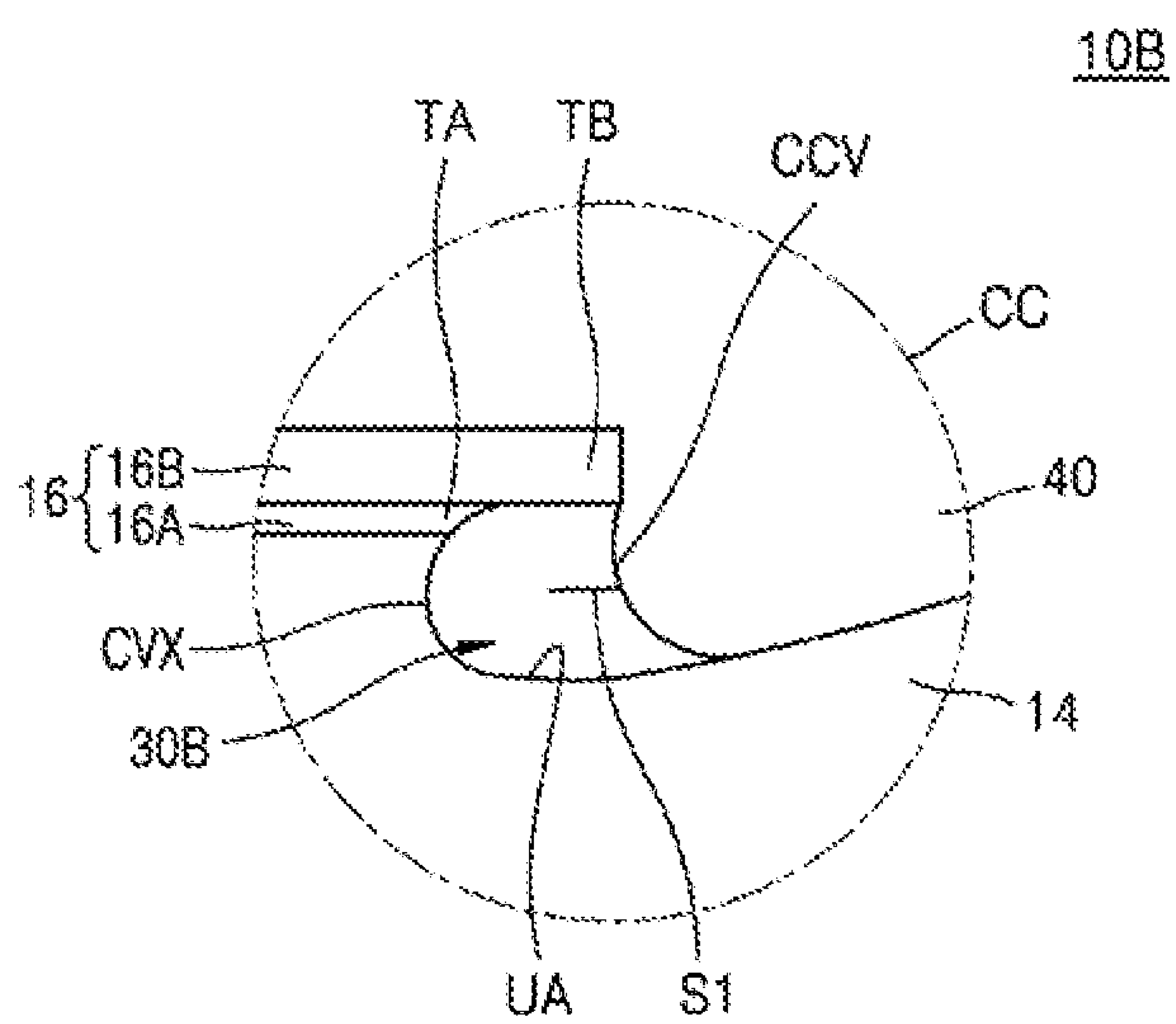

10B
TA
TB
CCV
CC
16
16B
16A
40
CVX
30B
14
UA
S1

FIG. 4

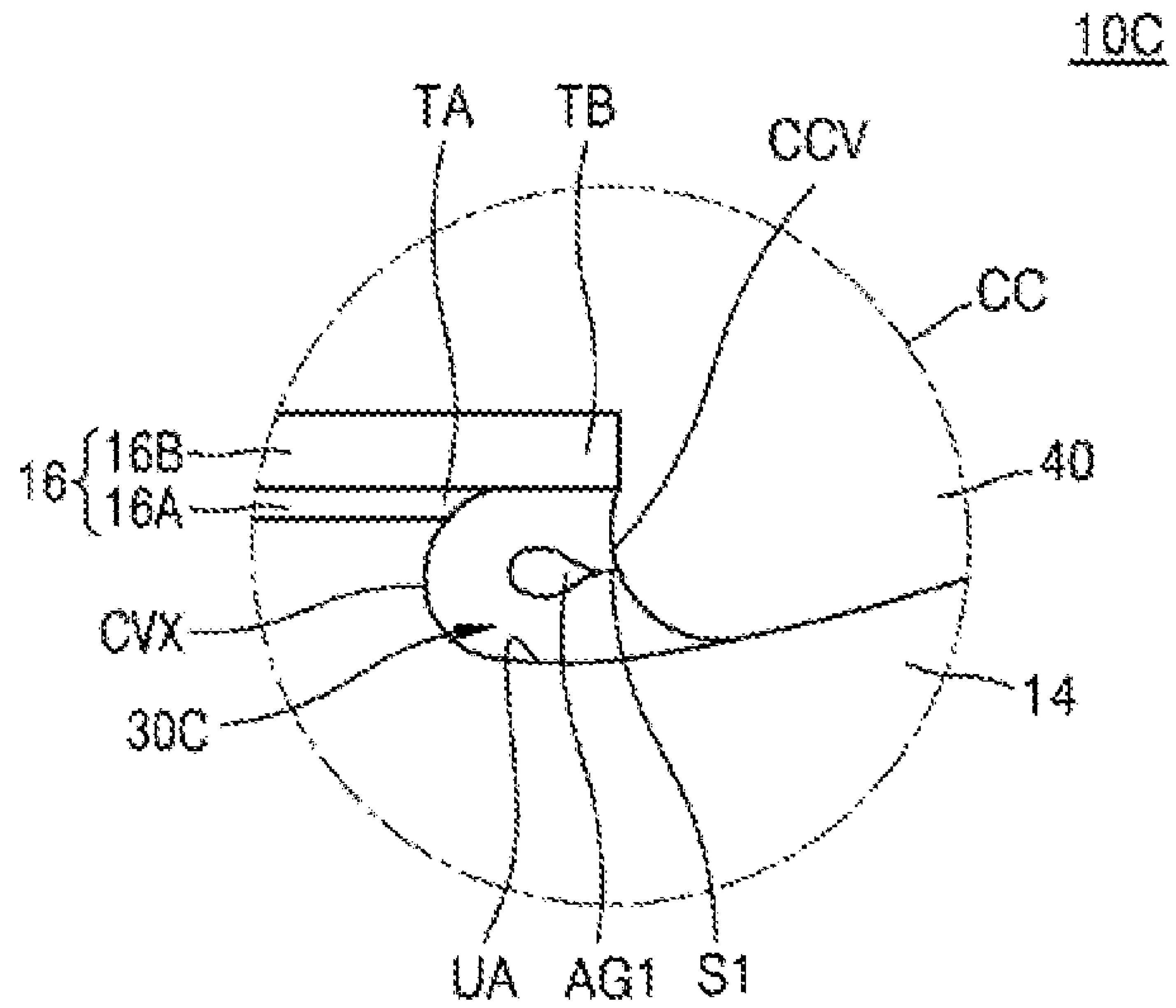

10C
TA
TB
CCV
CC
16
16B
16A
40
CVX
30C
14
UA
AG1
S1

FIG. 5

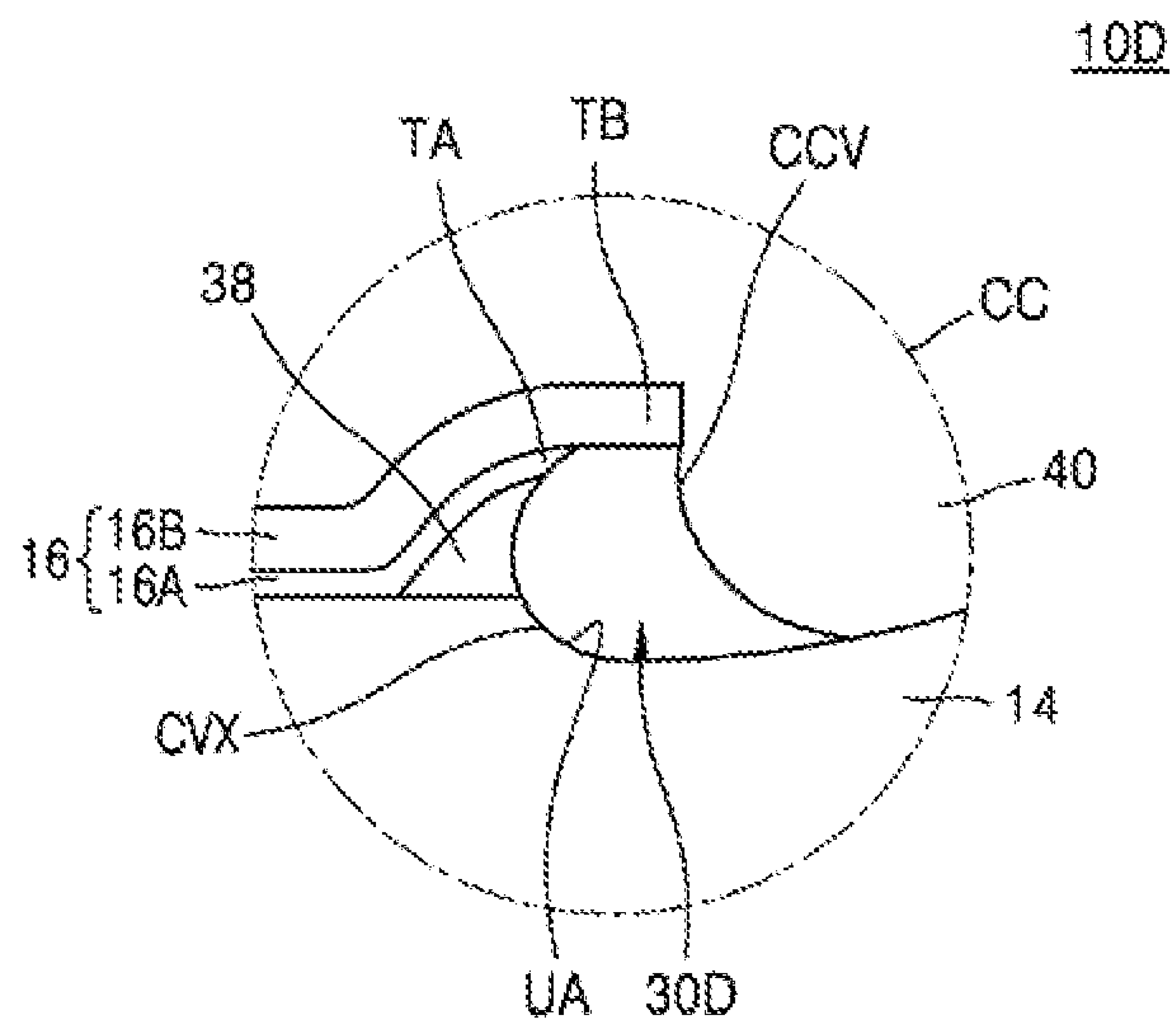

10D
TA
TB
CCV
38
CC
16
16B
16A
40
CVX
14
UA
30D

FIG. 6

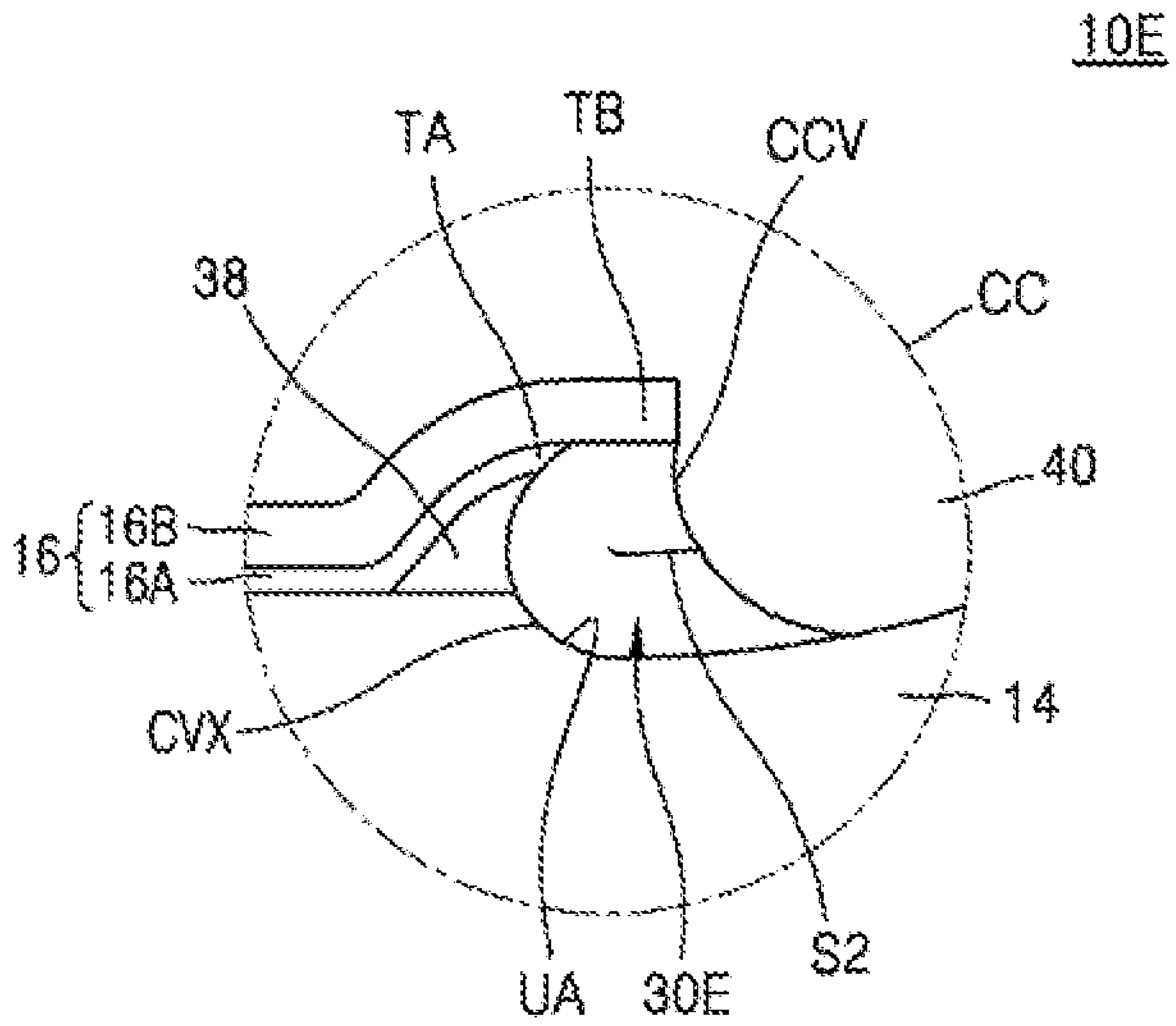

10E
TA
TB
CCV
38
CC
40
16
16B
16A
CVX
14
UA
30E
S2

FIG. 7

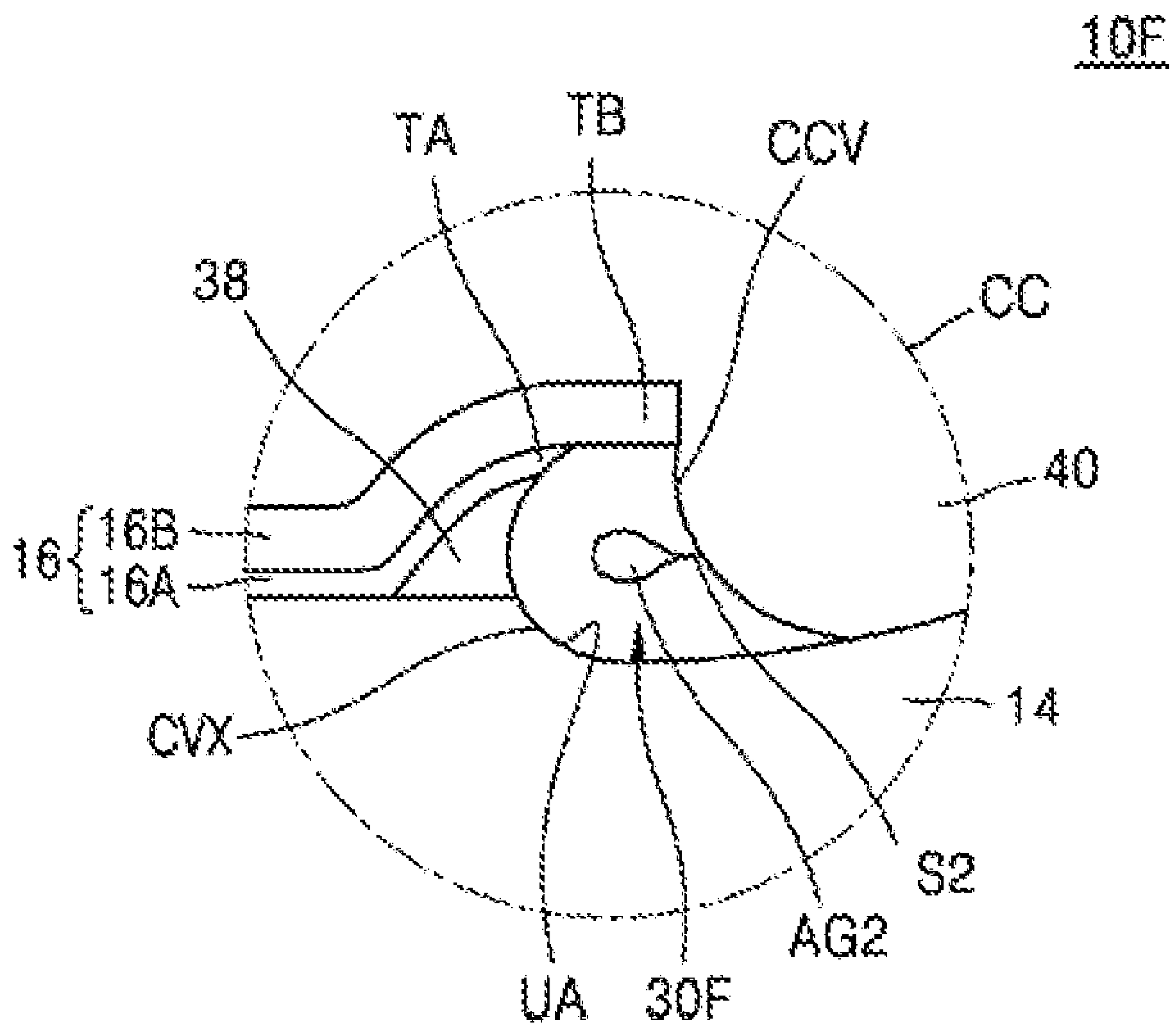

10F
TA
TB
CCV
38
CC
40
16
16B
16A
CVX
14
UA
30F
AG2
S2

FIG. 8

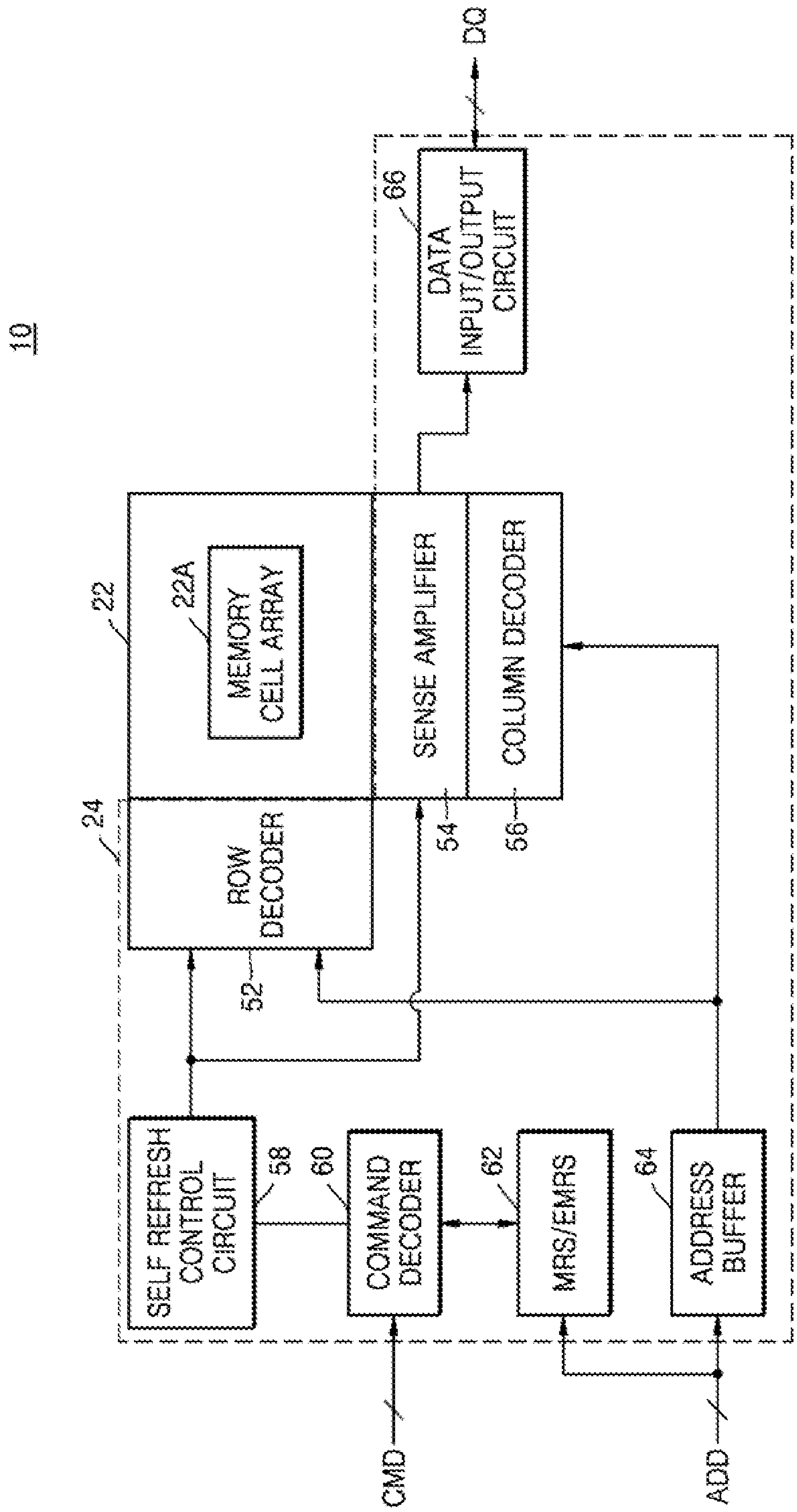

10
DQ
66
DATA INPUT/OUTPUT CIRCUIT
22
22A
MEMORY CELL ARRAY
SENSE AMPLIFIER
COLUMN DECODER
24
ROW DECODER
54
56
52
SELF REFRESH CONTROL CIRCUIT
58
60
COMMAND DECODER
62
MRS/EMRS
64
ADDRESS BUFFER
CMD
ADD

FIG. 9

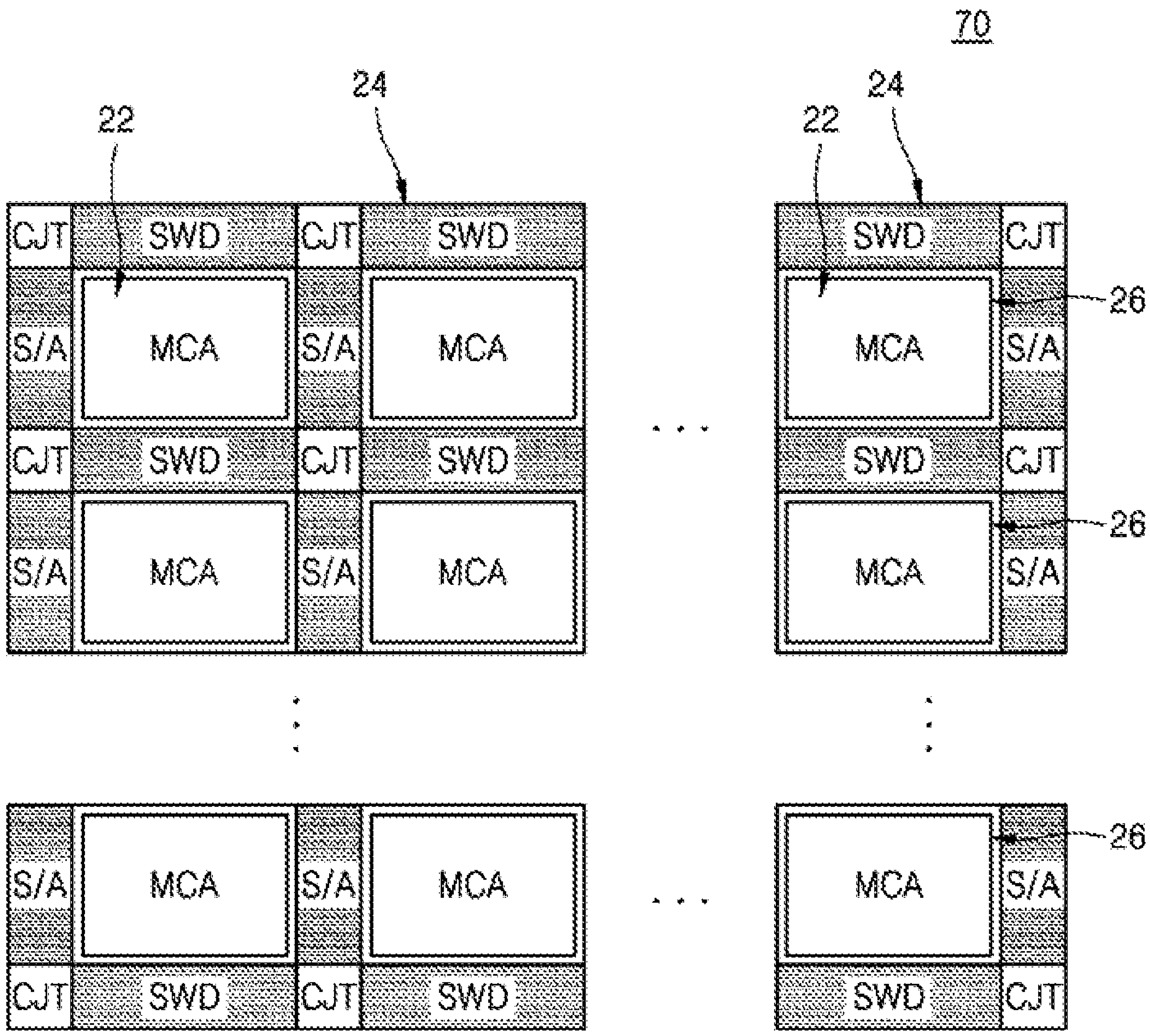

70
24
22
22
24
CJT
SWD
CJT
SWD
SWD
CJT
26
S/A
MCA
S/A
MCA
MCA
S/A
CJT
SWD
CJT
SWD
SWD
CJT
26
S/A
MCA
S/A
MCA
MCA
S/A
26
S/A
MCA
S/A
MCA
MCA
S/A
CJT
SWD
CJT
SWD
SWD
CJT

FIG. 10

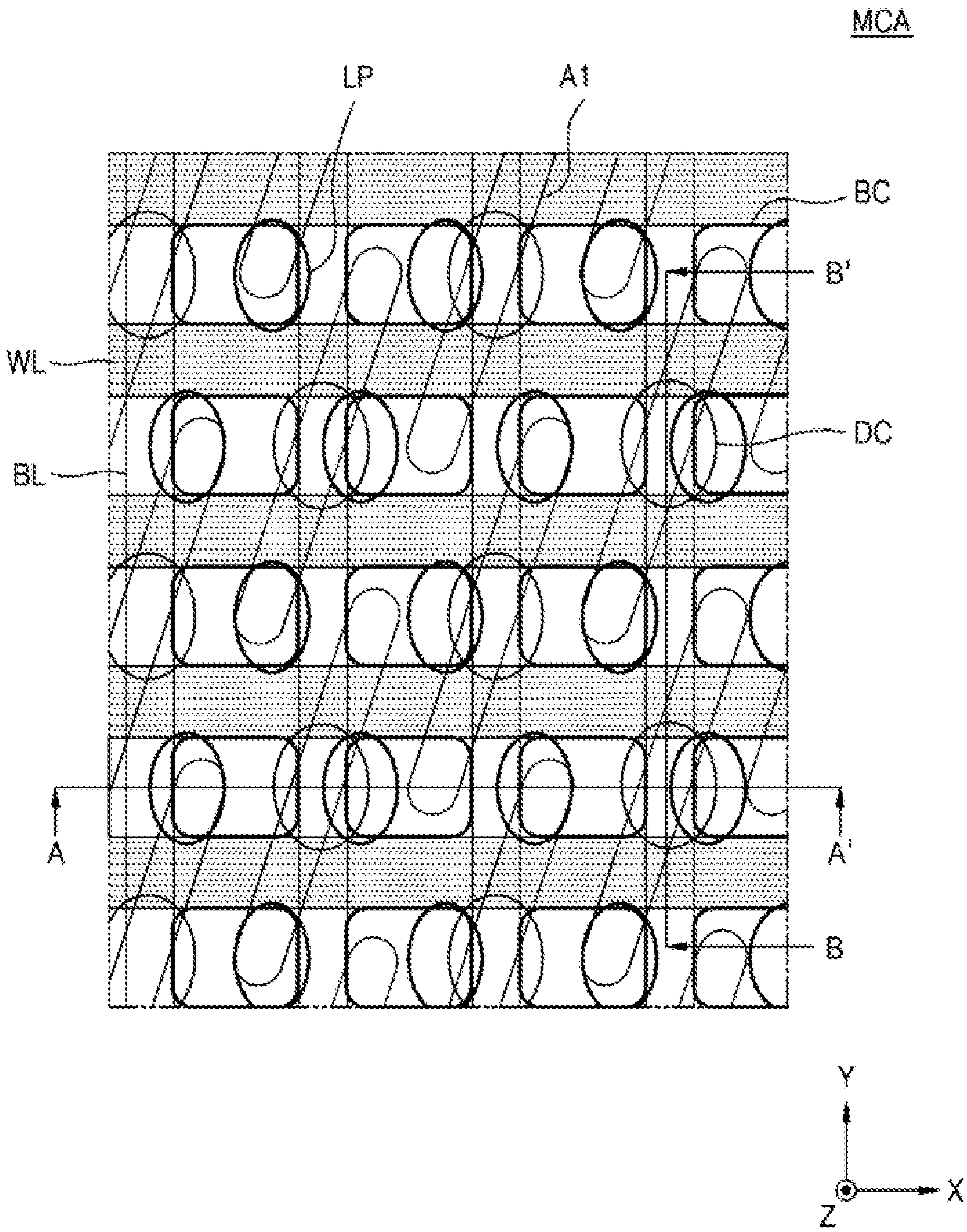


FIG. 11A

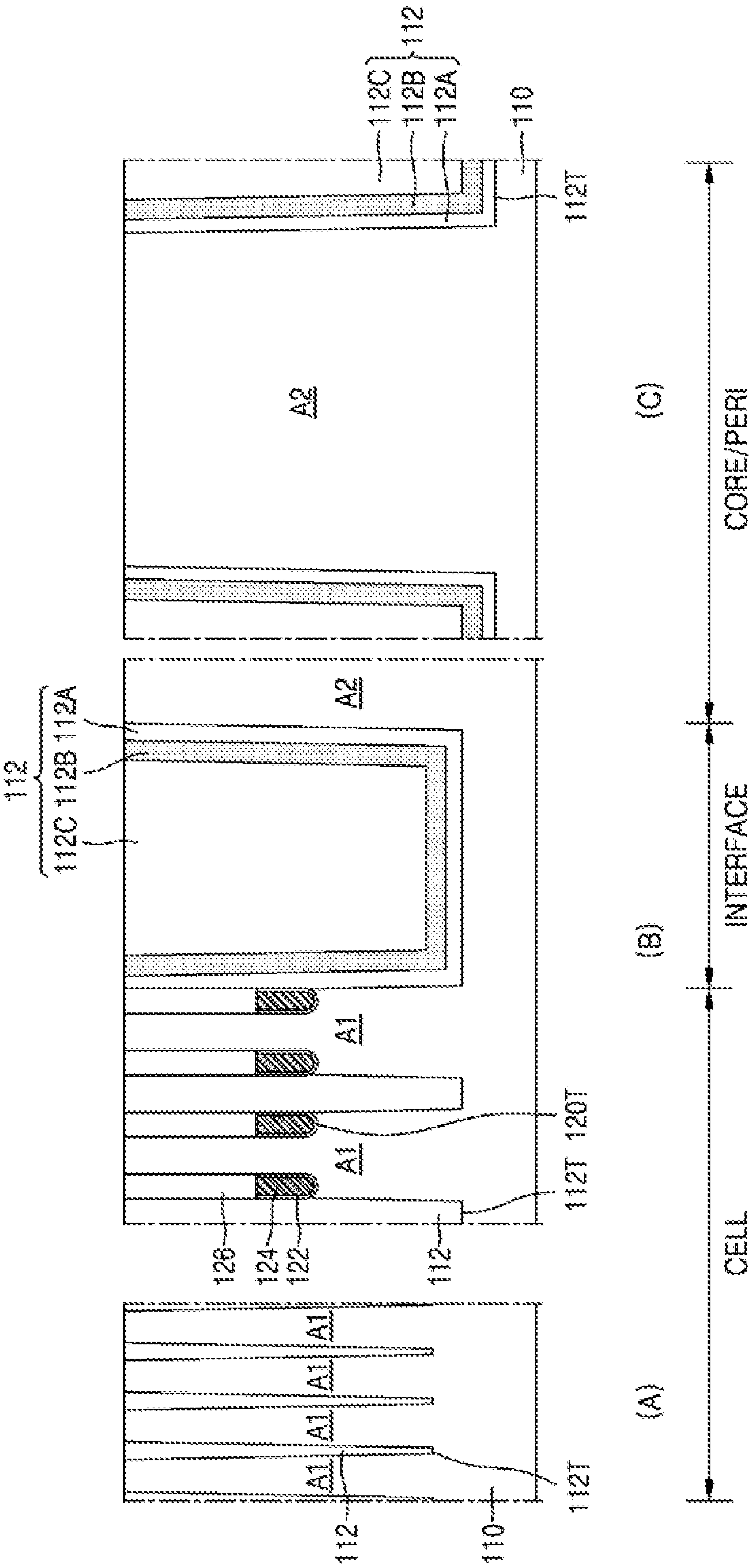

112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
112C
112B
112A
112
A2
INTERFACE
(B)
A1
120T
A1
112T
126
124
122
112
CELL
A1
A1
A1
A1
112
110
112T
(A)

FIG. 11B

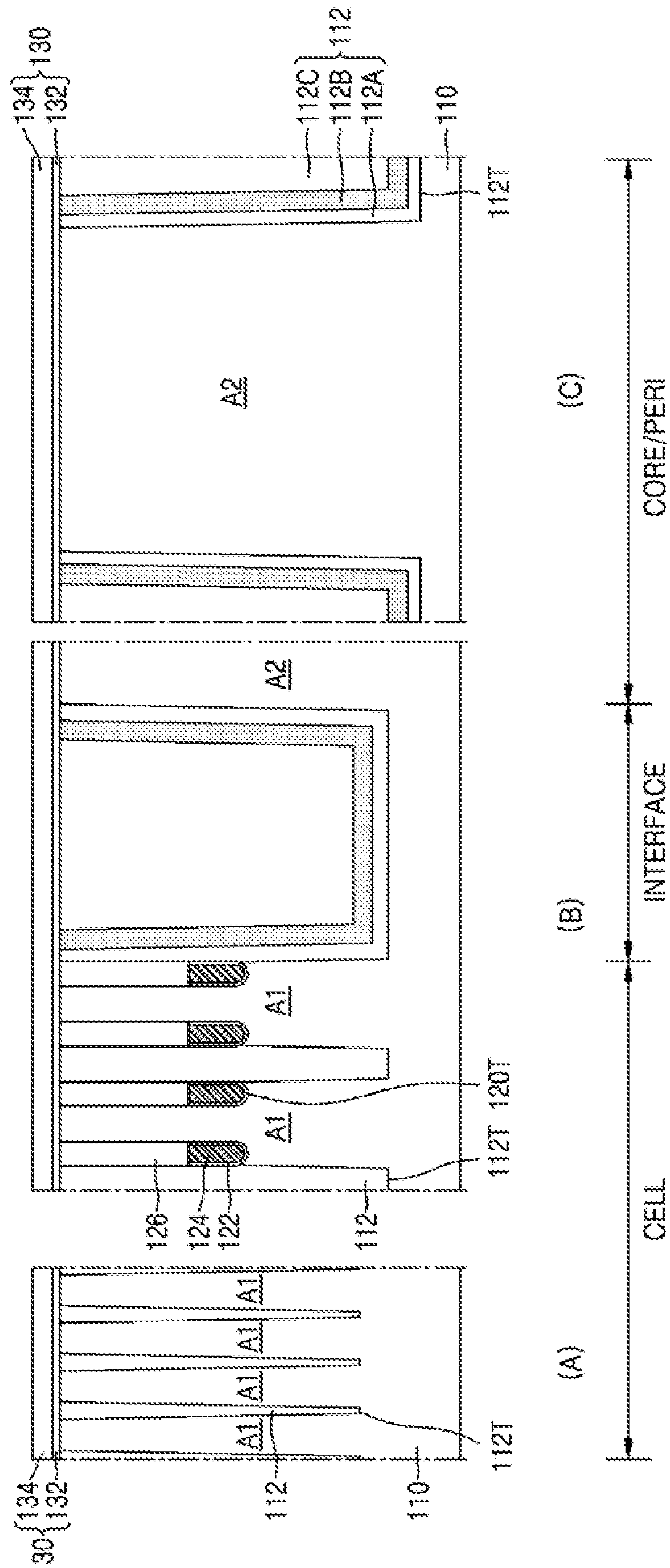
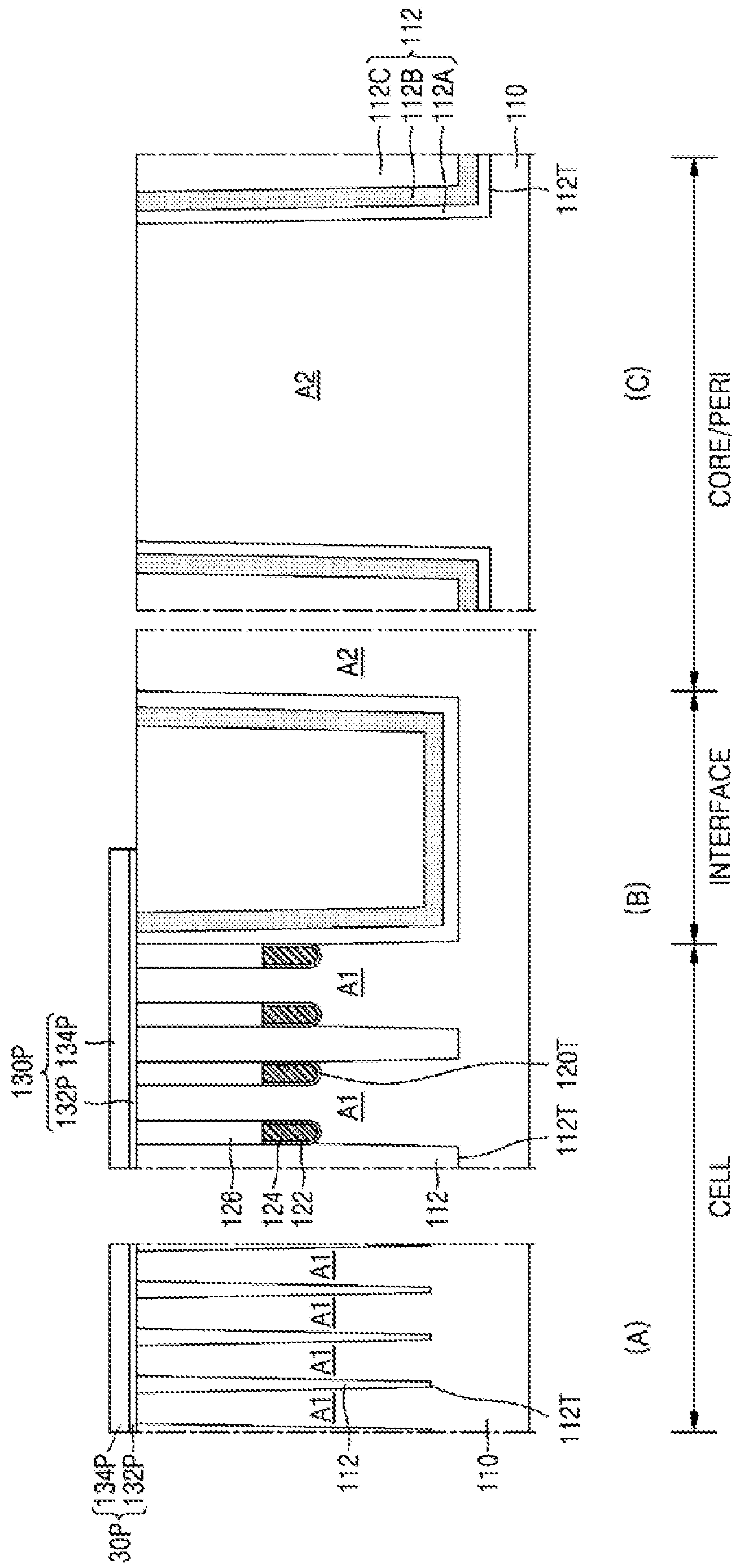
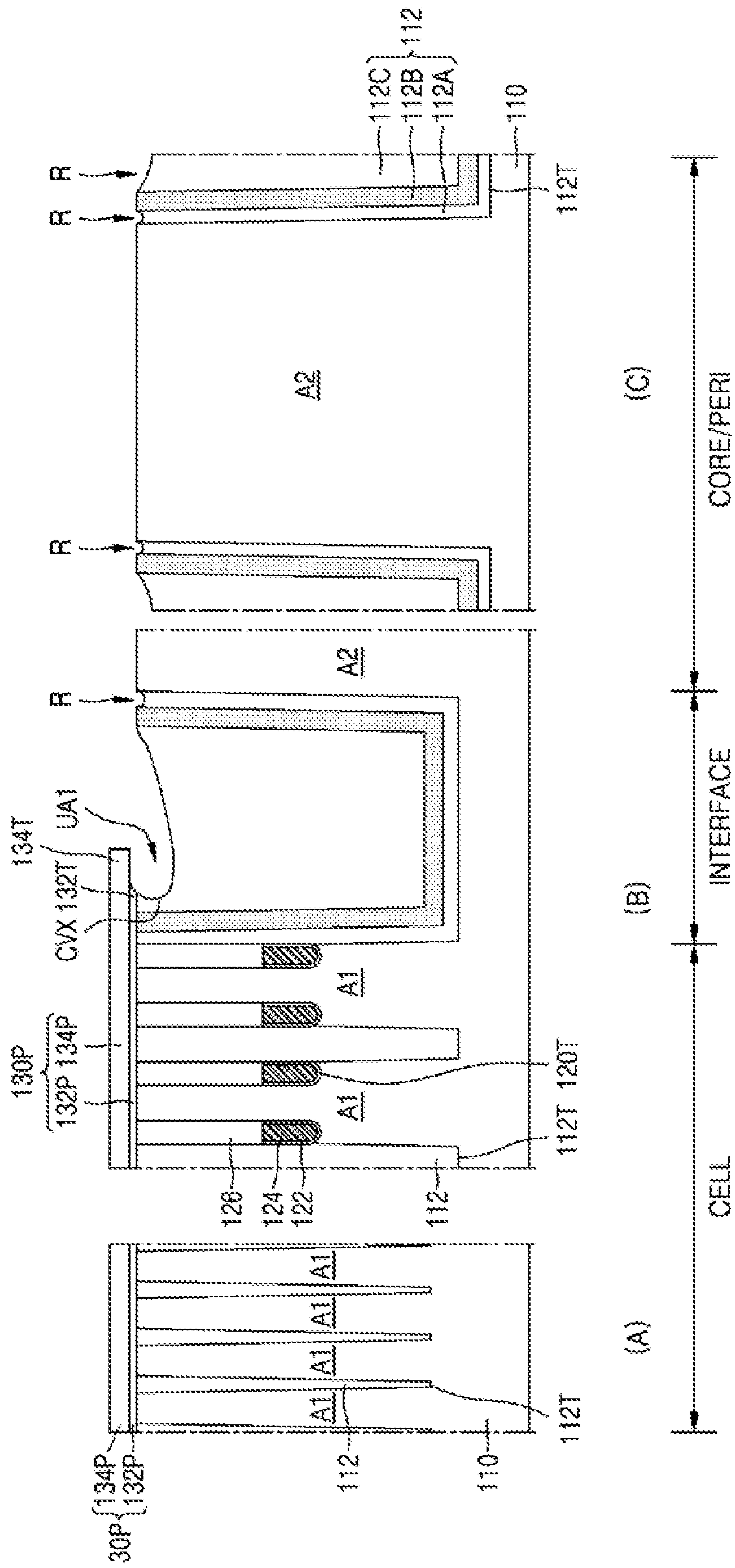

134
132
130
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
A2
INTERFACE
(B)
A1
A1
120T
112T
126
124
122
112
CELL
A1
A1
A1
A1
(A)
112T
110
112
134
132
130

FIG. 11C



130P
134P
132P
112
110
112T
A1
(A)
CELL
126
124
122
120T
(B)
INTERFACE
A2
(C)
CORE/PERI
112C
112B
112A

FIG. 11D



130P
134P
132P
112
110
112T
A1
126
124
122
120T
134T
132T
CVX
UA1
A2
R
112C
112B
112A
(A)
(B)
(C)
CELL
INTERFACE
CORE/PERI

FIG. 11E

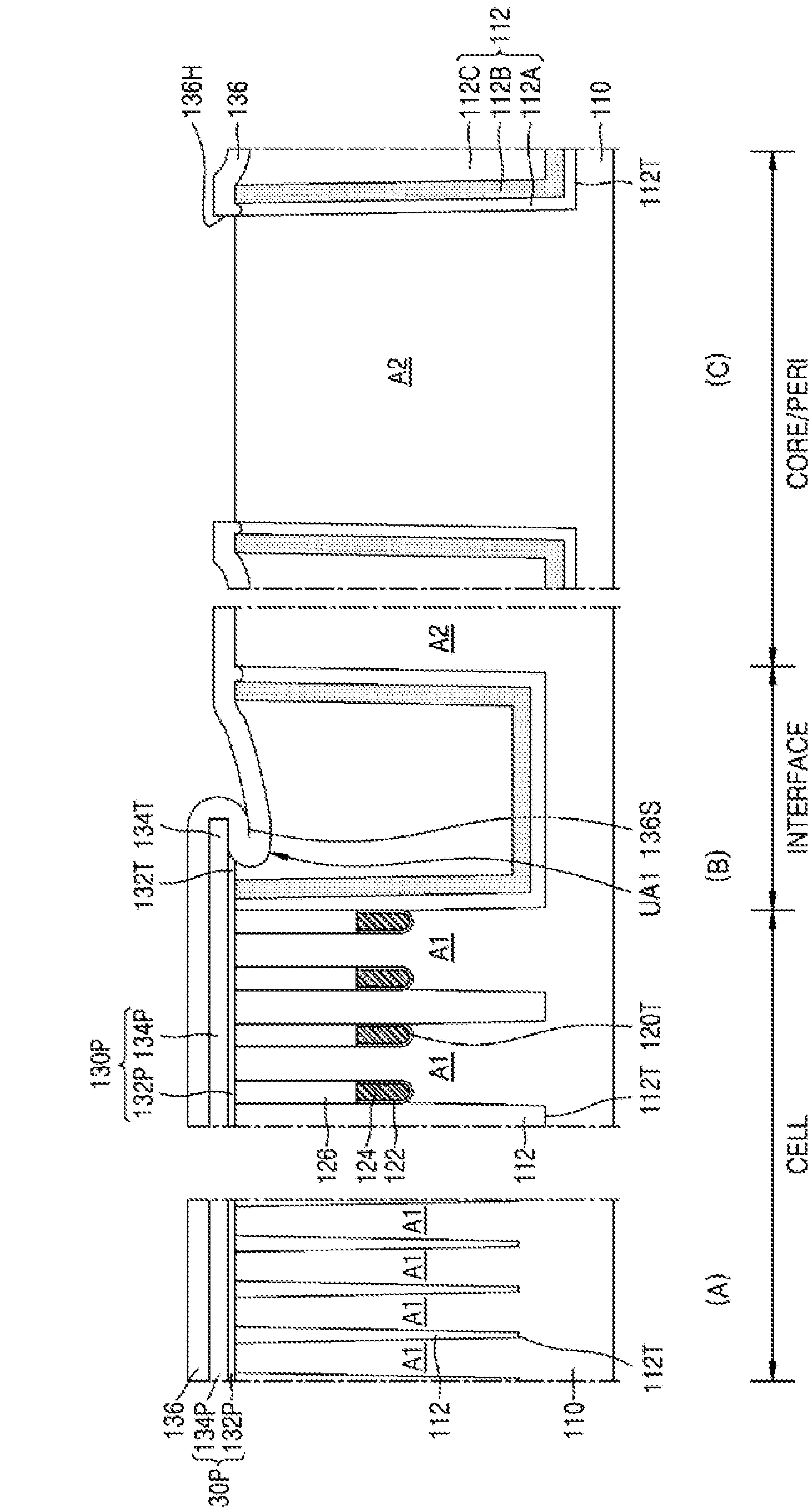
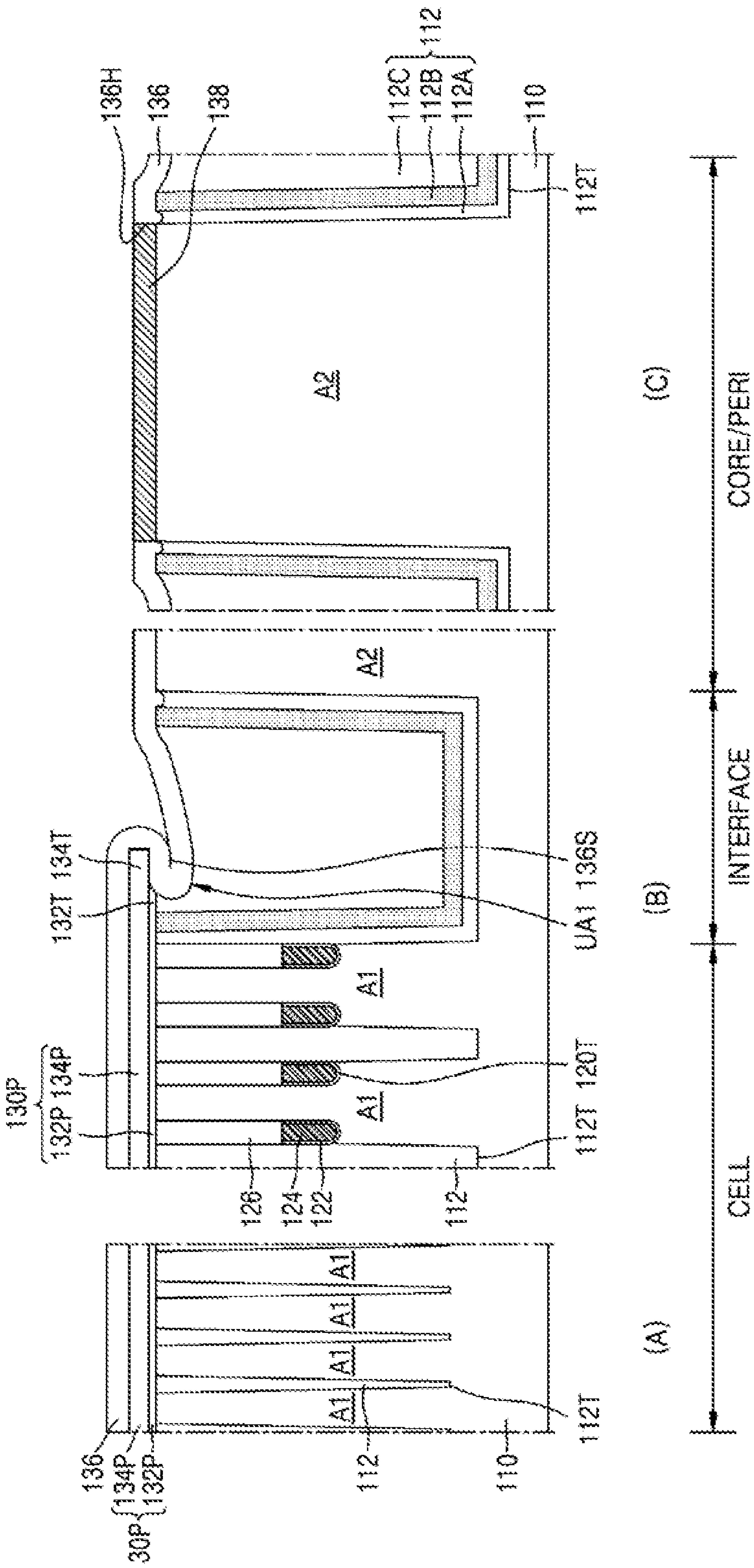

136H
136
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
A2
132T 134T
136S
UA1
(B)
INTERFACE
130P
132P 134P
120T
A1
A1
112T
126
124
122
112
CELL
(A)
136
134P
132P
130P
112
110
112T

FIG. 11F



136H
136
138
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
A2
INTERFACE
132T 134T
UA1 136S
(B)
130P
132P 134P
120T
A1
112T
126
124
122
112
CELL
A1
(A)
136
134P
132P
130P
110
112T

FIG. 11G

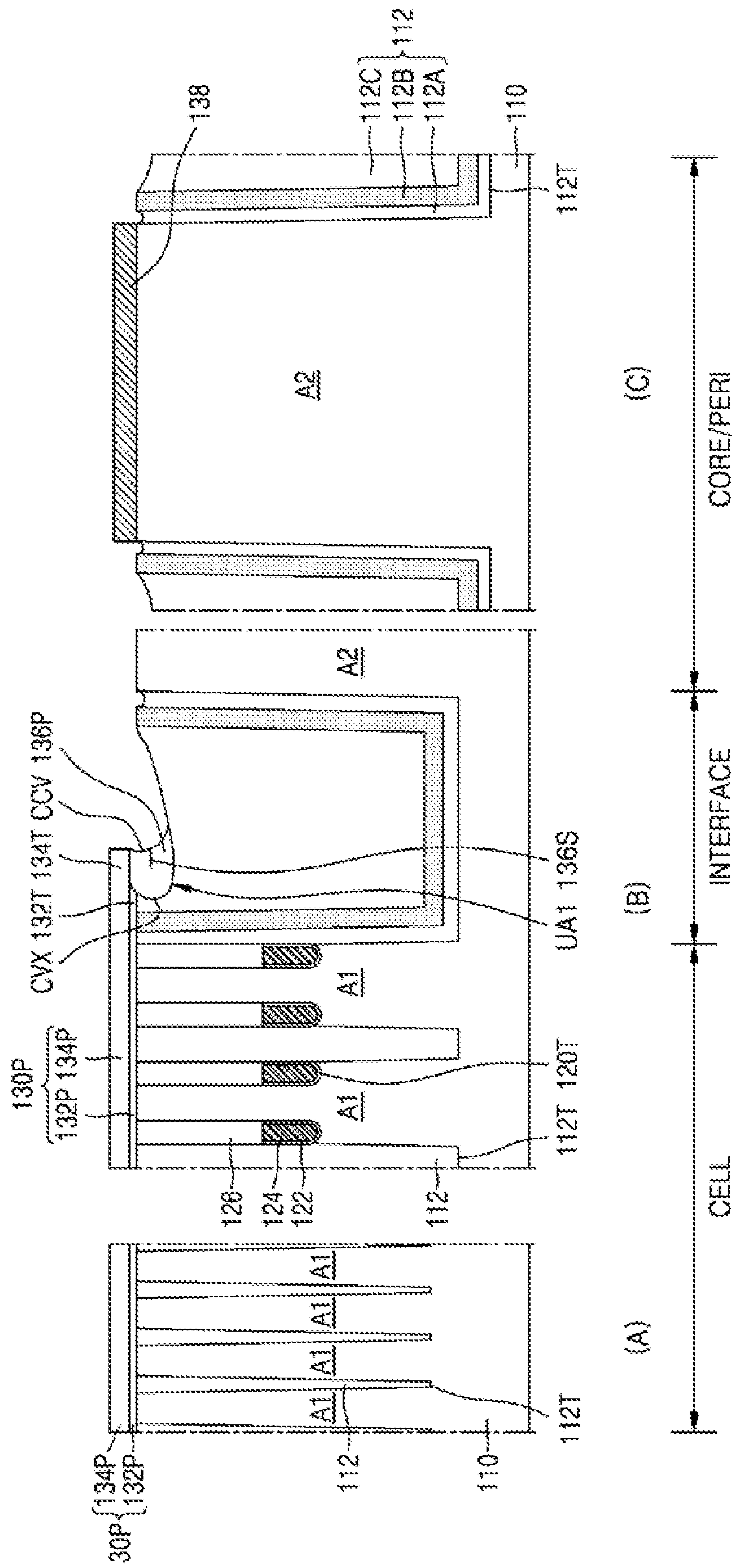

130P
134P
132P
112
110
112T
A1
(A)
CELL
126
124
122
120T
CVX
132T
134T
CCV
136P
UA1
136S
A2
(B)
INTERFACE
138
112C
112B
112A
(C)
CORE/PERI

FIG. 11H

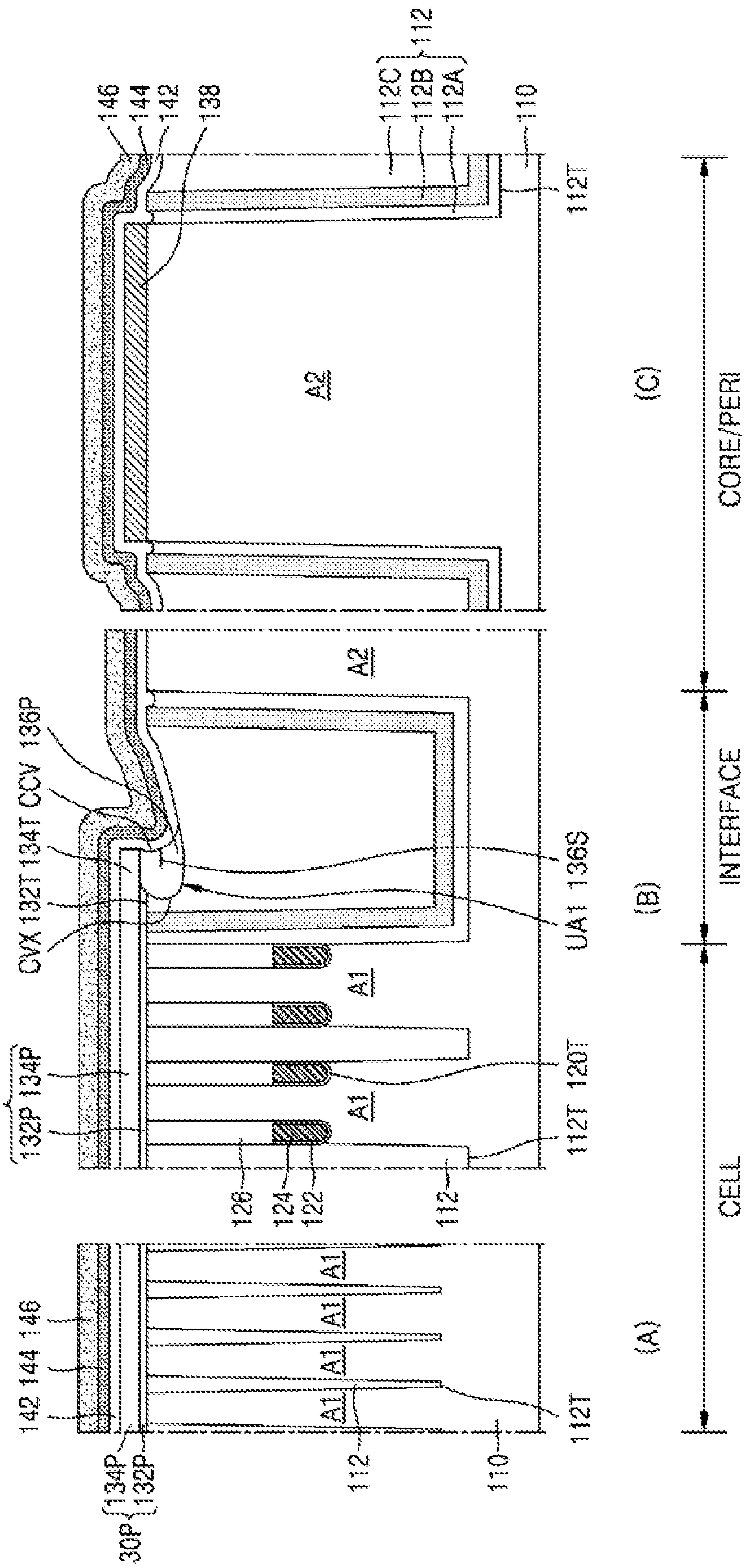
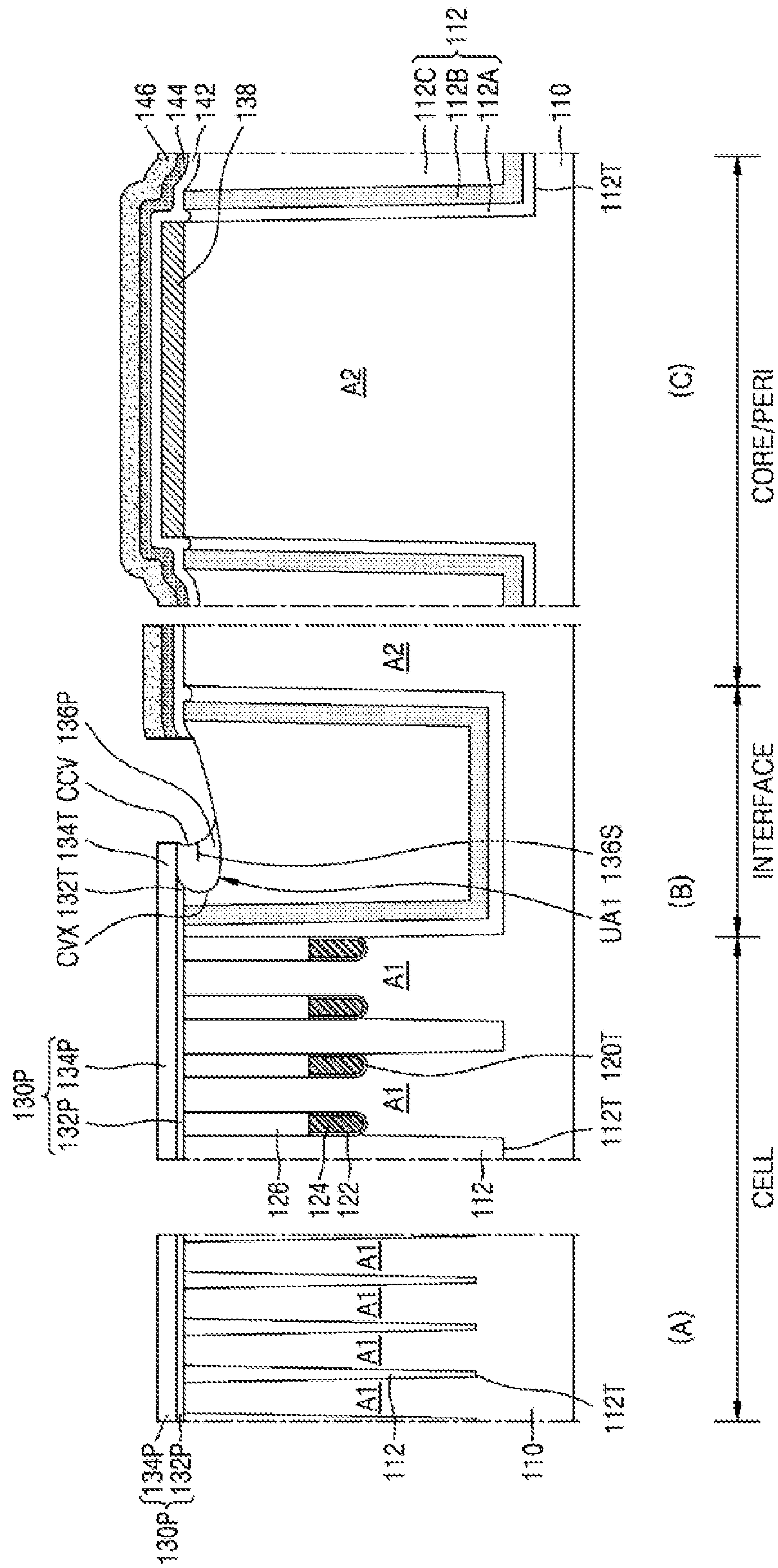

146
144
142
138
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
INTERFACE
CVX 132T 134T CCV 136P
UA1 136S
(B)
130P
132P 134P
112T 120T
A1
126
124
122
CELL
142 144 146
(A)
134P
132P

FIG. 11I



146
144
142
138
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
A2
CVX 132T 134T CCV 136P
136S
UA1
(B)
INTERFACE
130P
132P 134P
A1
120T
112T
126
124
122
112
CELL
A1
(A)
134P
132P
130P
110
112T

FIG. 11J

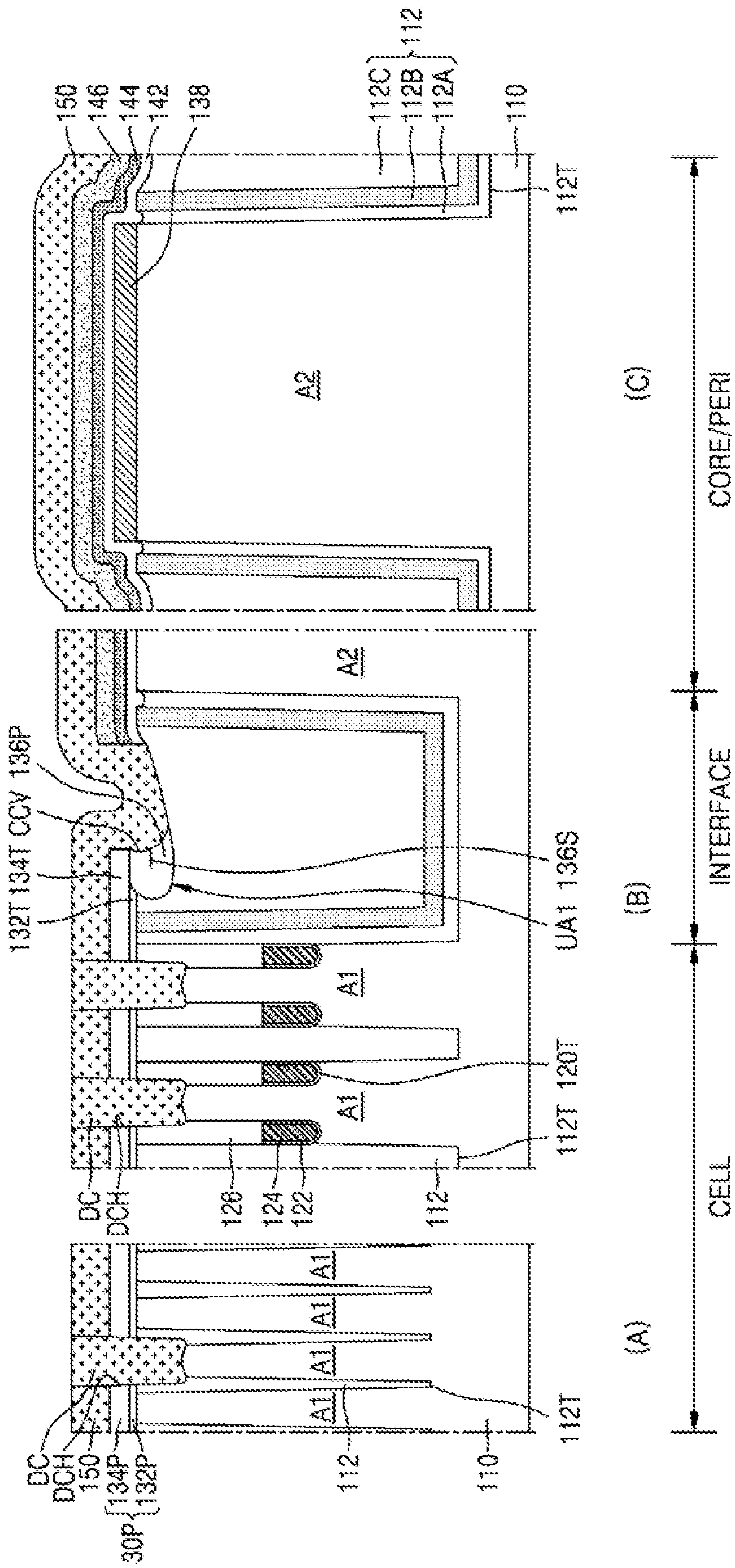

150
146
144
142
138
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
A2
132T 134T CCV 136P
136S
UA1
(B)
INTERFACE
A1
120T
A1
112T
DC
DCH
126
124
122
112
CELL
A1
A1
A1
A1
(A)
DC
DCH
150
134P
132P
130P
112
110
112T

FIG. 11K

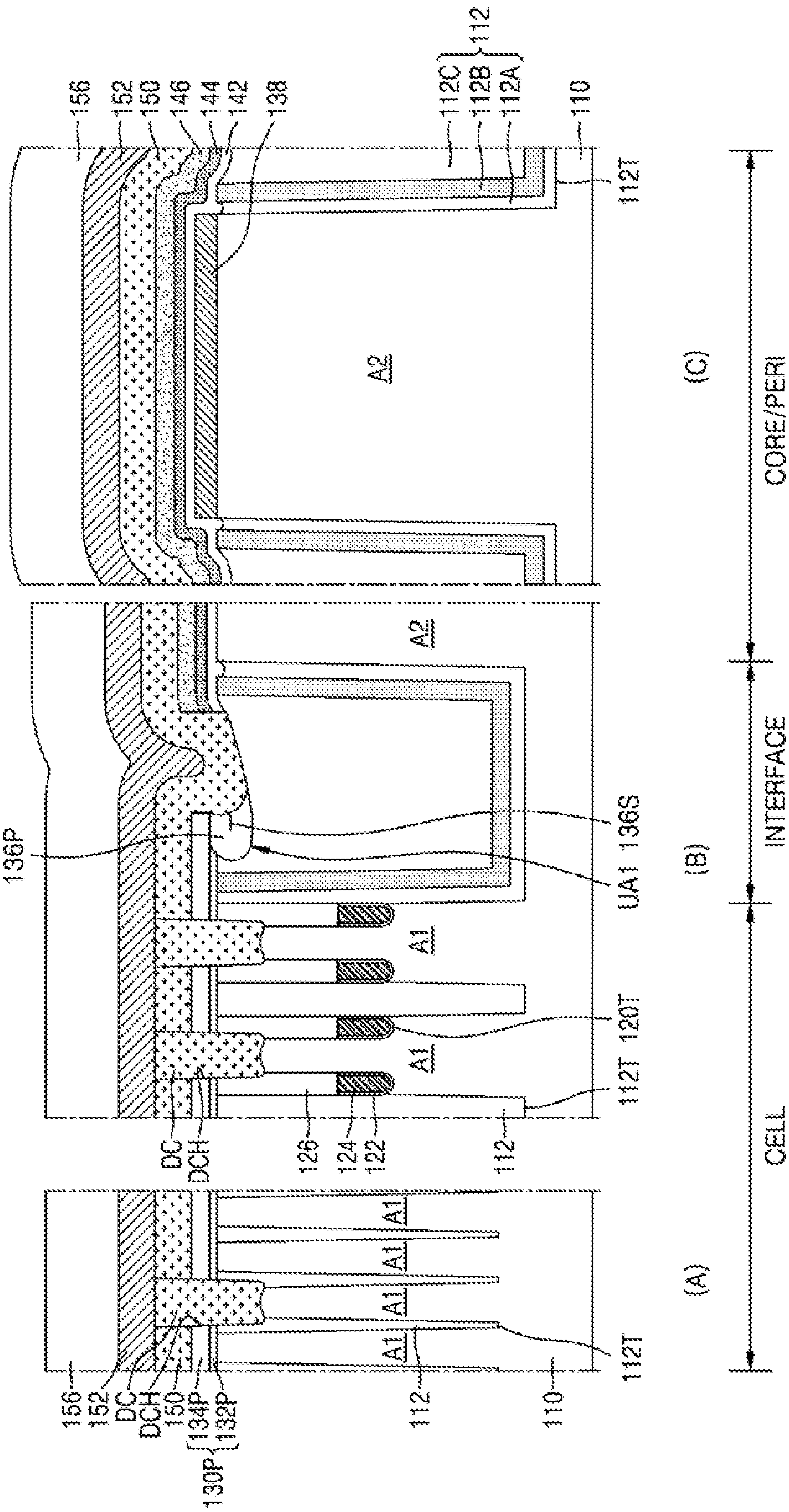
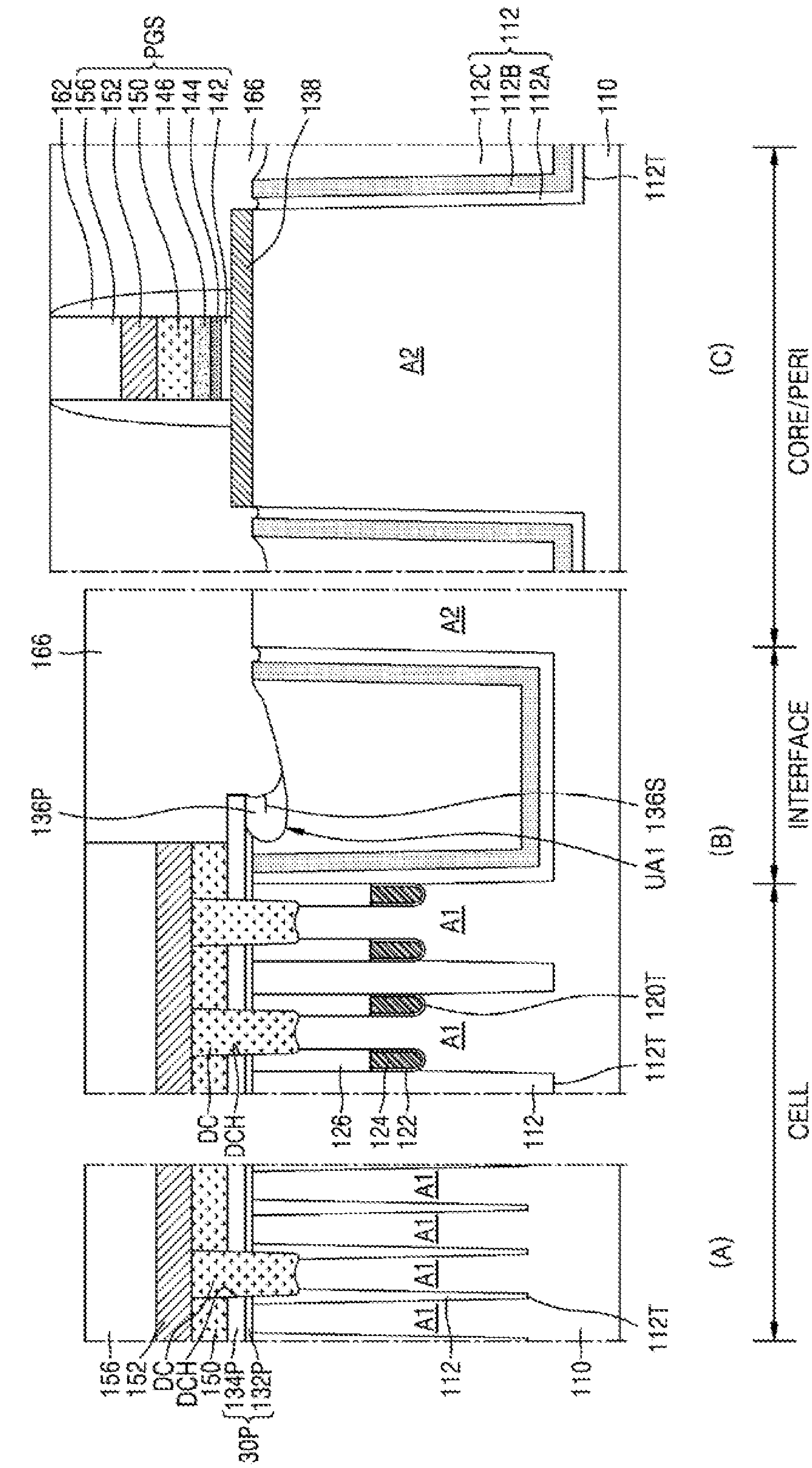
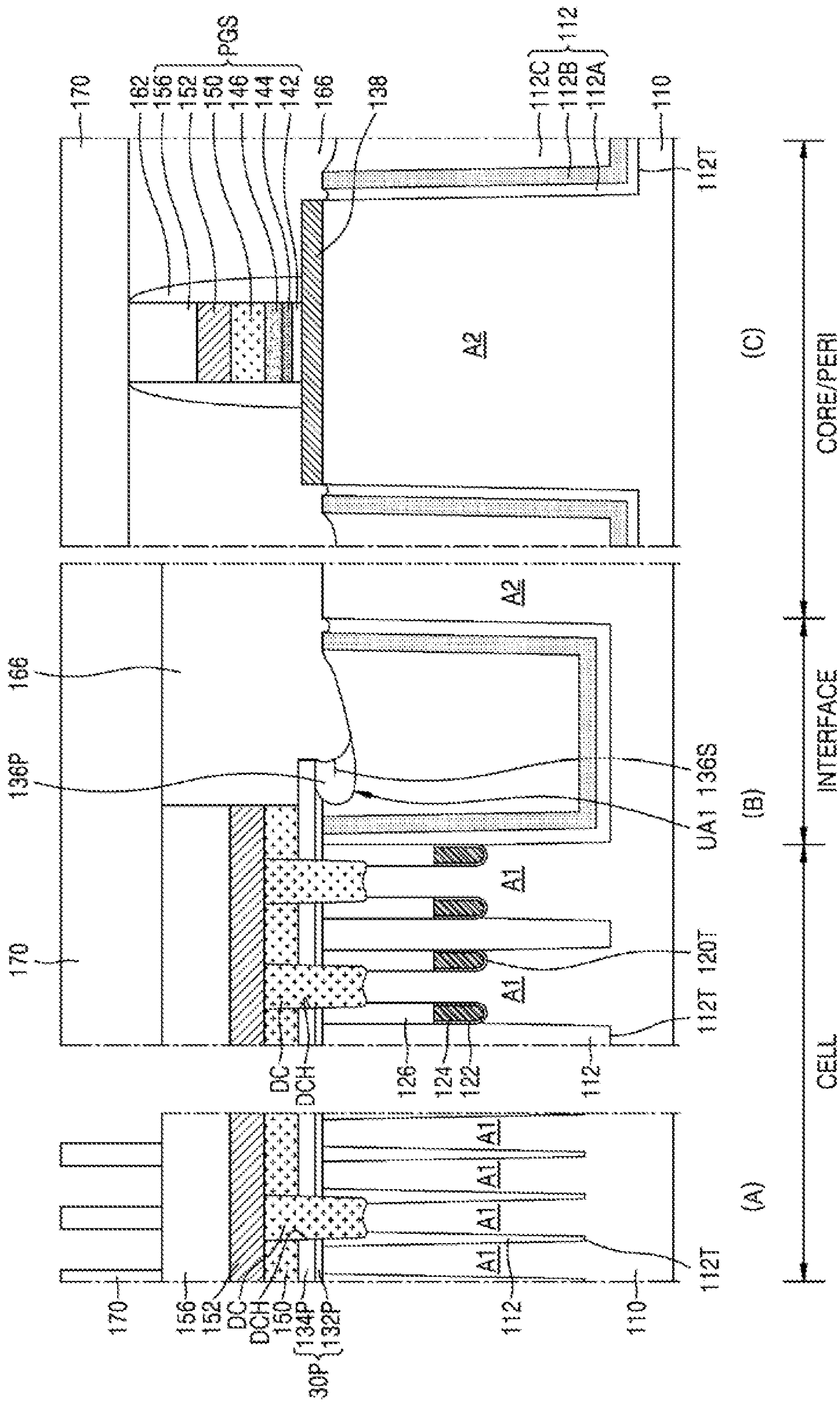

156
152
150
146
144
142
138
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
136P
136S
UA1
A2
(B)
INTERFACE
120T
112T
A1
DC
DCH
126
124
122
112
CELL
(A)
A1
156
152
DC
DCH
150
134P
132P
130P
112
110
112T

FIG. 11L



162
156
152
150
146
144
142
PGS
166
138
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
136P
UA1
136S
A1
120T
(B)
INTERFACE
DC
DCH
126
124
122
CELL
(A)
130P
132P
134P

FIG. 11M



170
162
156
152
150
146
144
142
PGS
166
138
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
166
136P
136S
UA1
(B)
INTERFACE
120T
112T
A1
DC
DCH
126
124
122
CELL
(A)
156
152
DC
DCH
150
134P
132P
130P

FIG. 11N

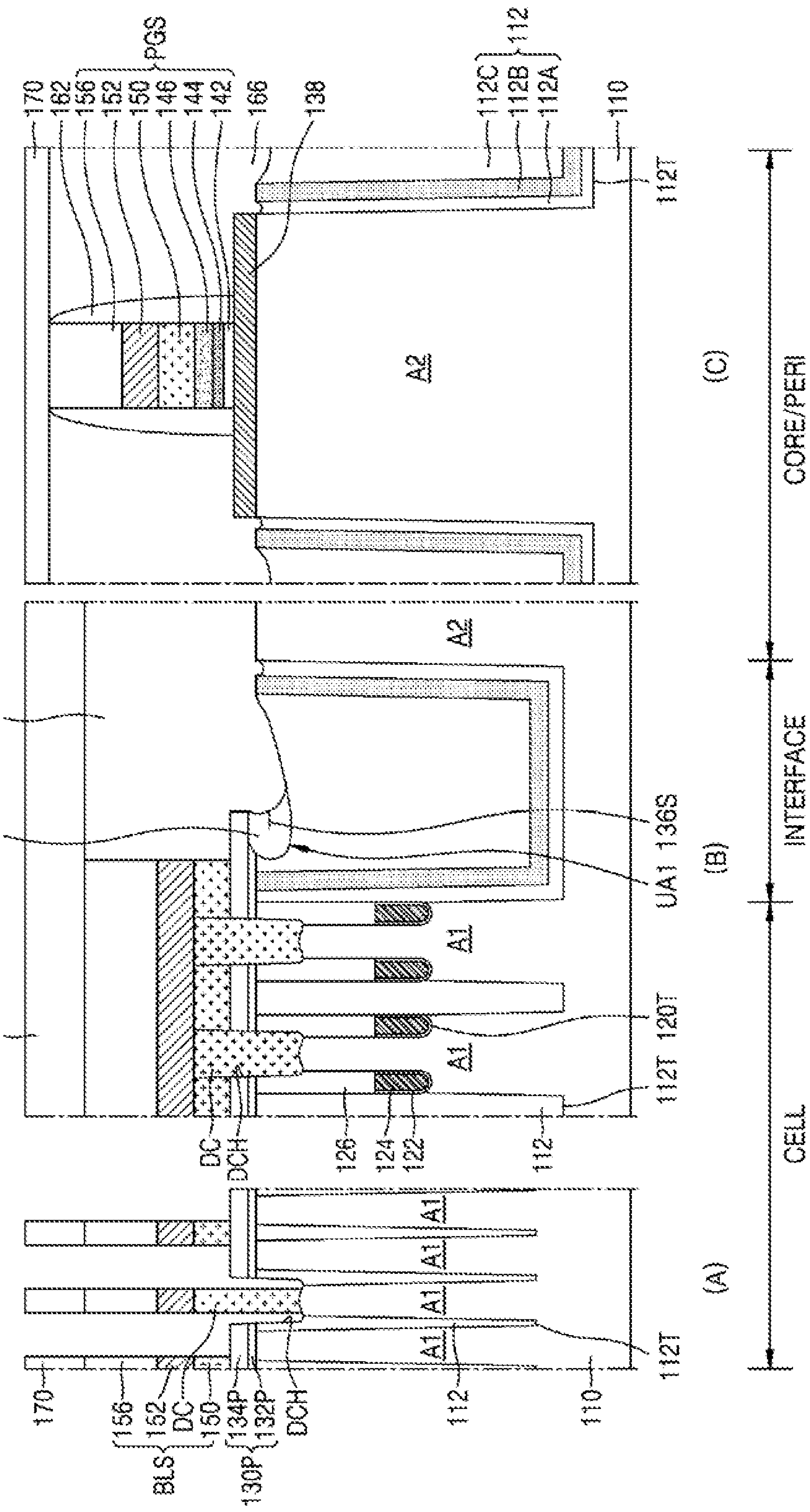
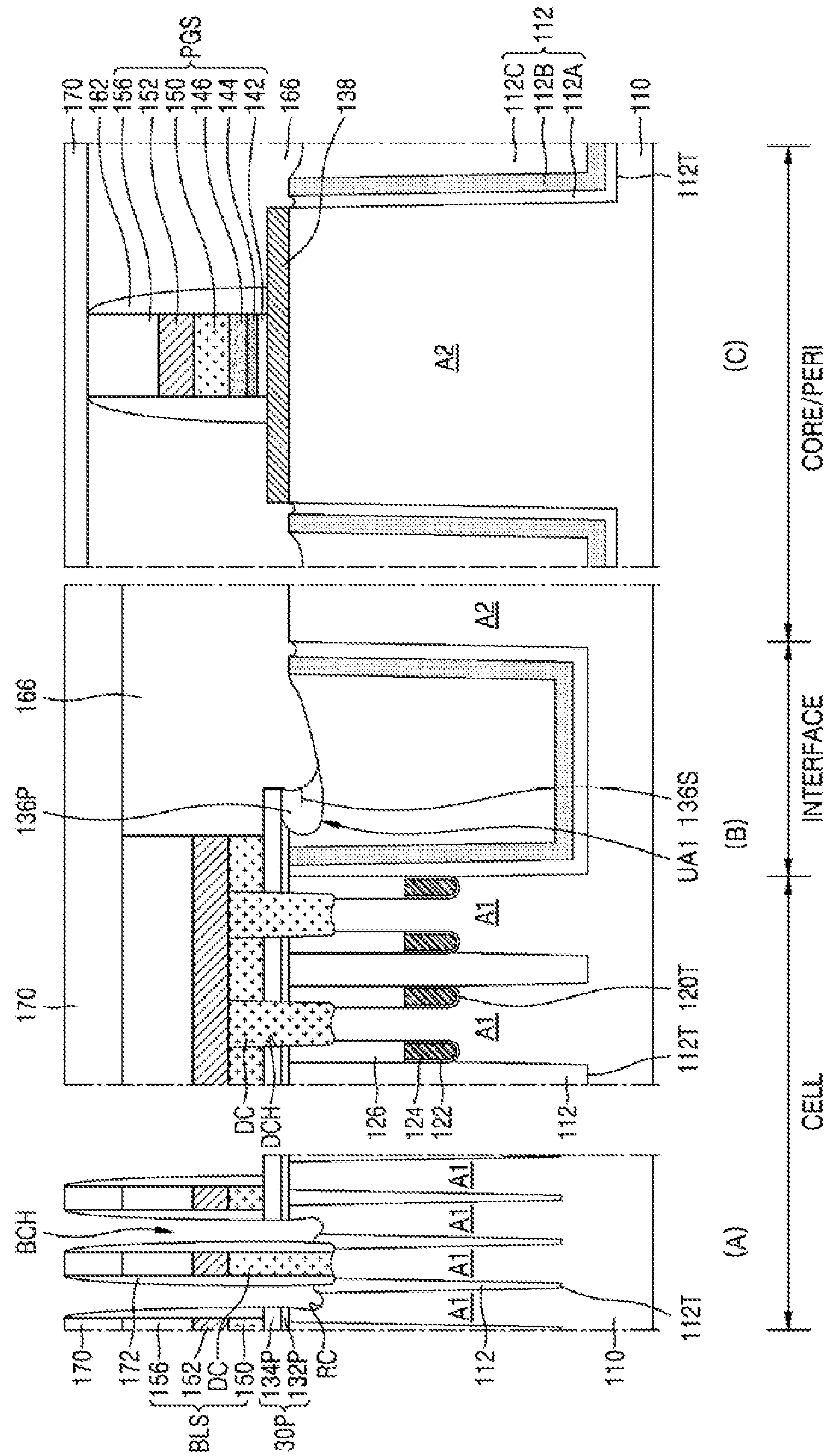

PGS
170
162
156
152
150
146
144
142
166
138
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
136P
136S
UA1
(B)
INTERFACE
120T
A1
126
124
122
DC
DCH
CELL
(A)
BLS
130P
134P
132P

FIG. 110



170
162
156
152
150
146
144
142
PGS
166
138
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
166
136P
136S
UA1
(B)
INTERFACE
170
120T
A1
112T
DC
DCH
126
124
122
112
CELL
BCH
(A)
172
156
152
DC
150
134P
132P
RC
BLS
130P
110

FIG. 11P

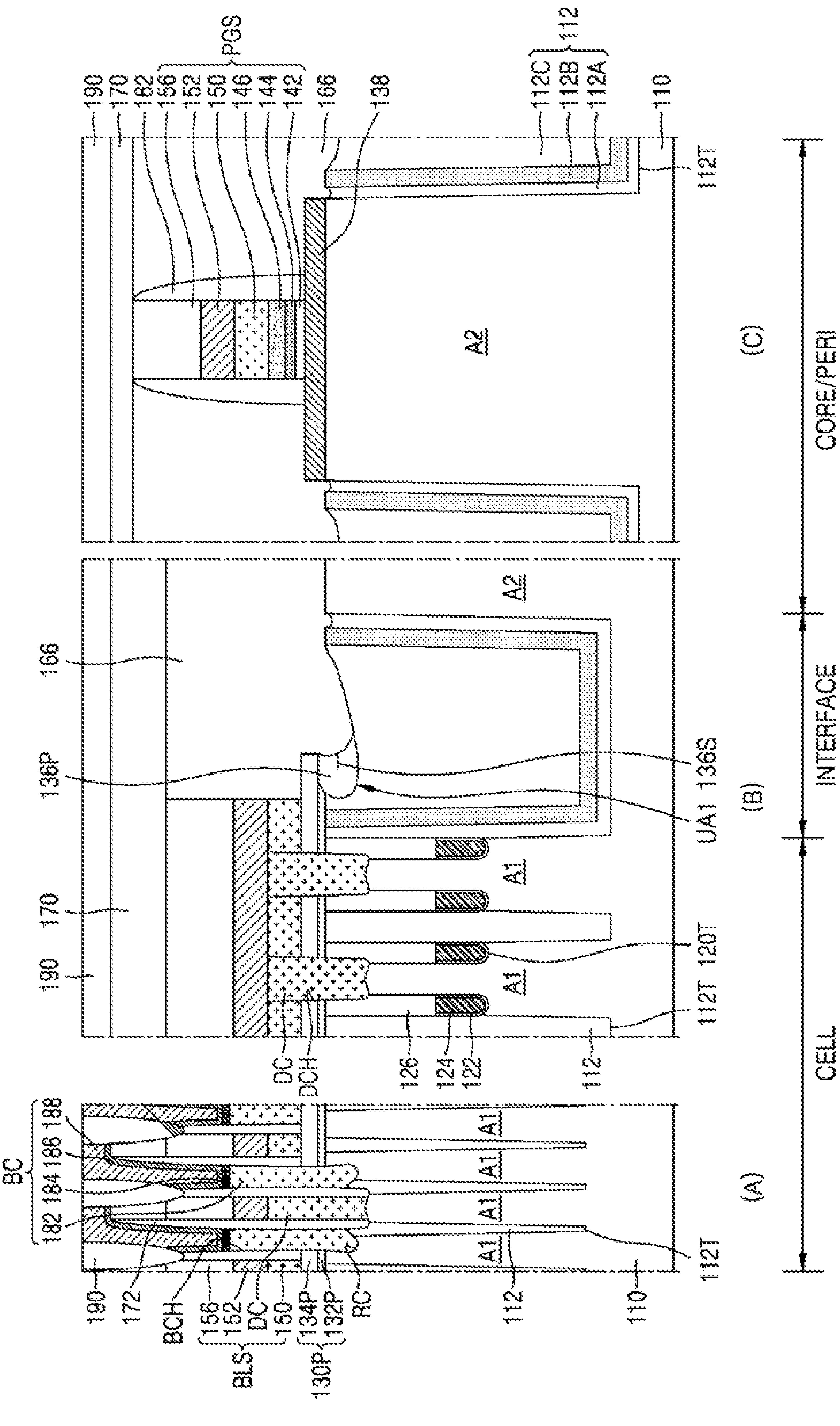
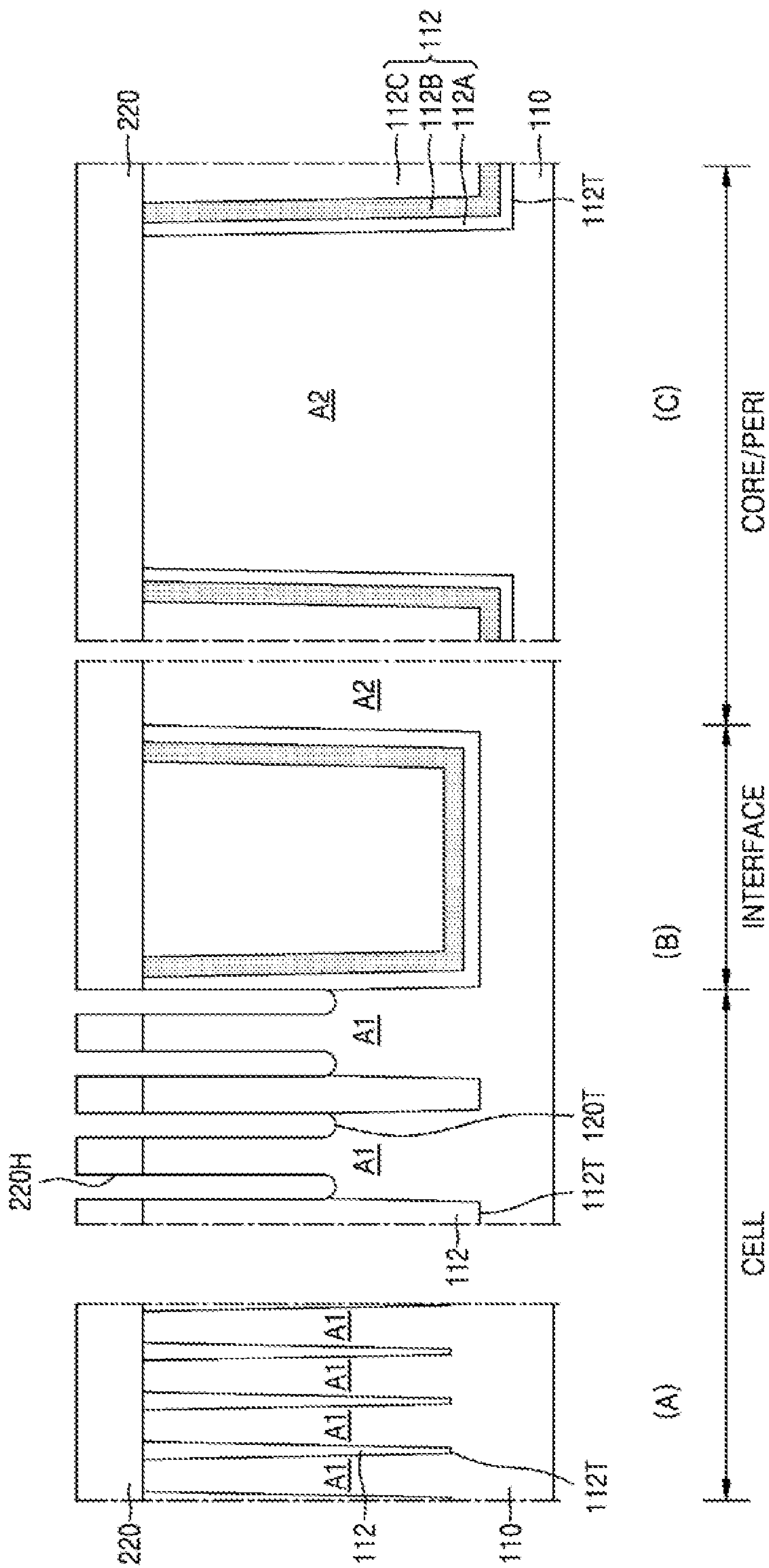

190
170
162
156
152
150
146
144
142
PGS
166
138
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
166
138P
136S
UA1
(B)
INTERFACE
170
190
120T
112T
A1
126
124
122
112
DC
DCH
CELL
BC
182
184
186
188
190
172
BCH
156
152
DC
150
134P
132P
RC
BLS
130P
112
110
112T
(A)

FIG. 12A



220
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
(B)
INTERFACE
A1
220H
120T
CELL
(A)

FIG. 12B

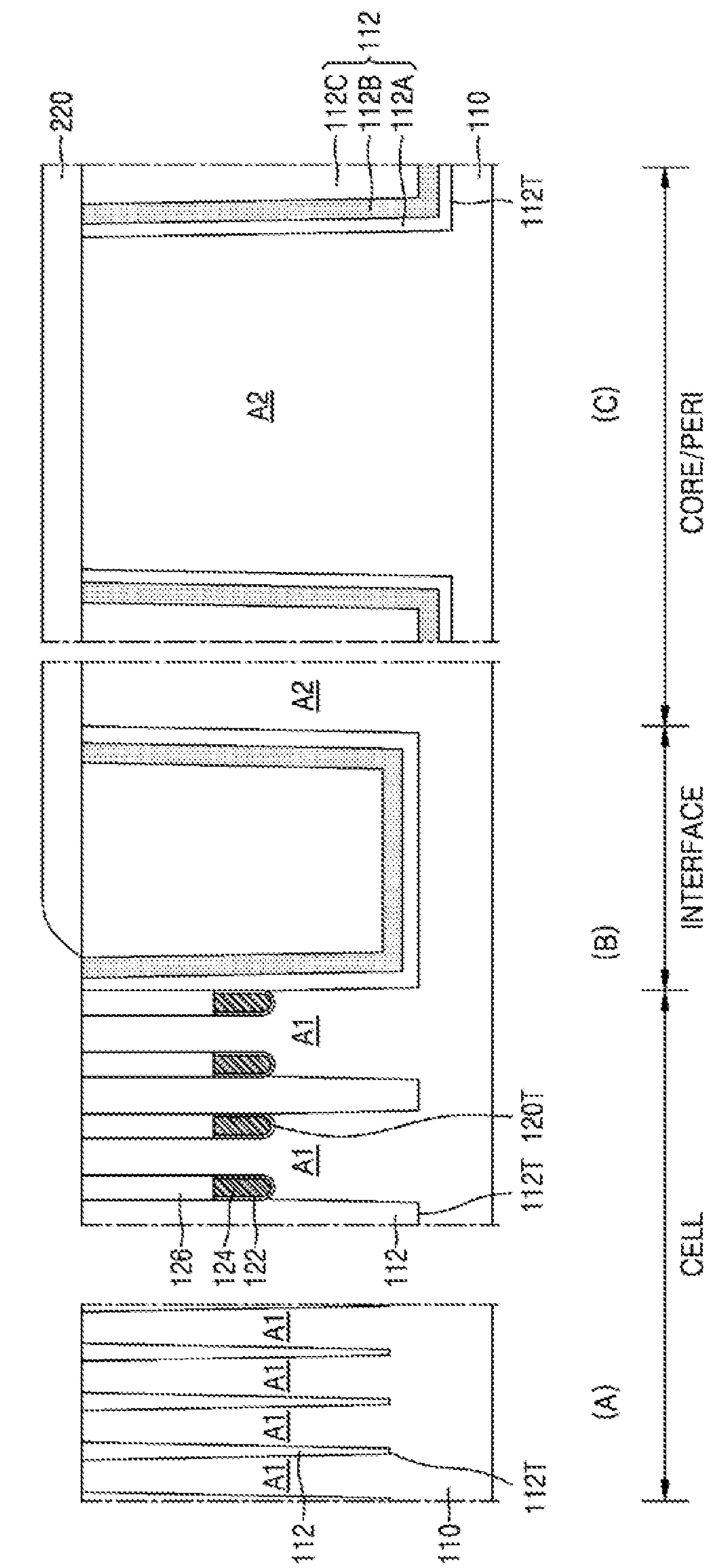
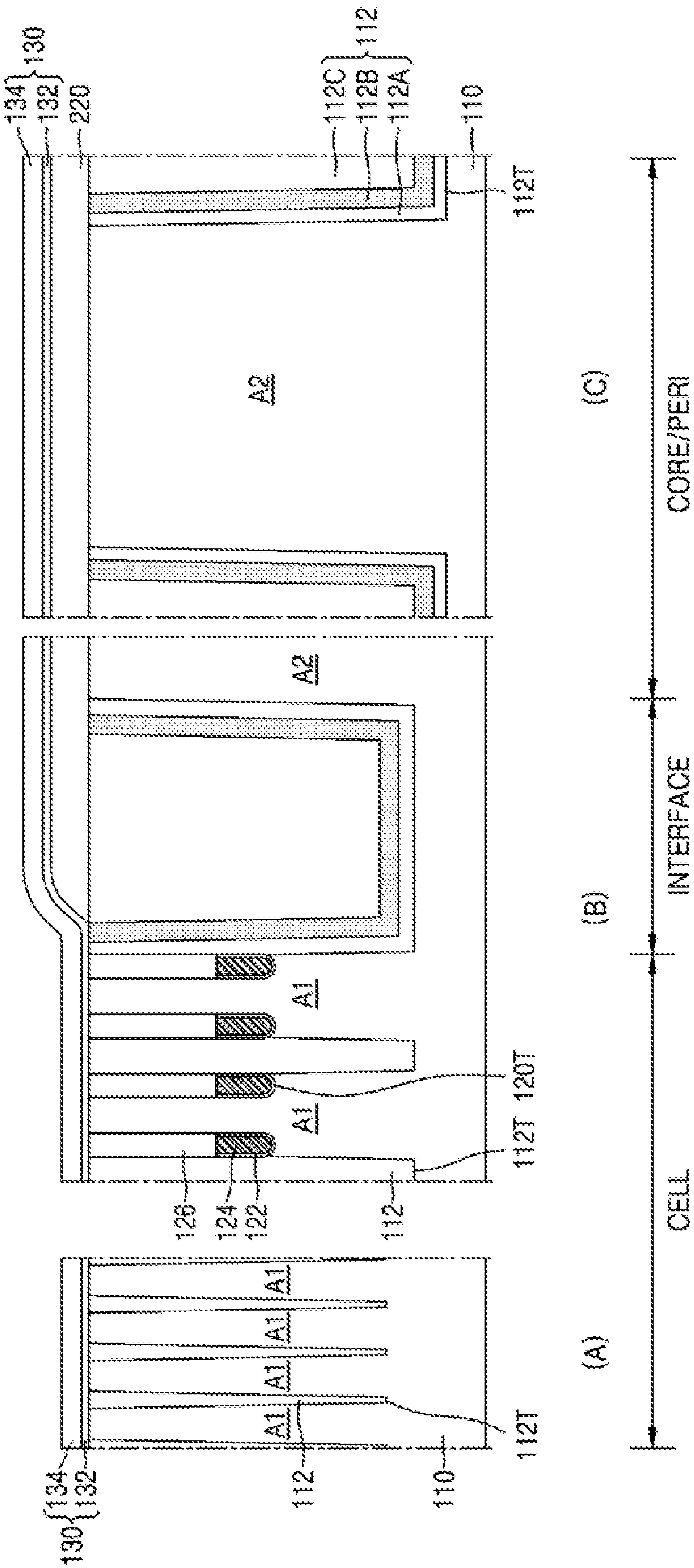
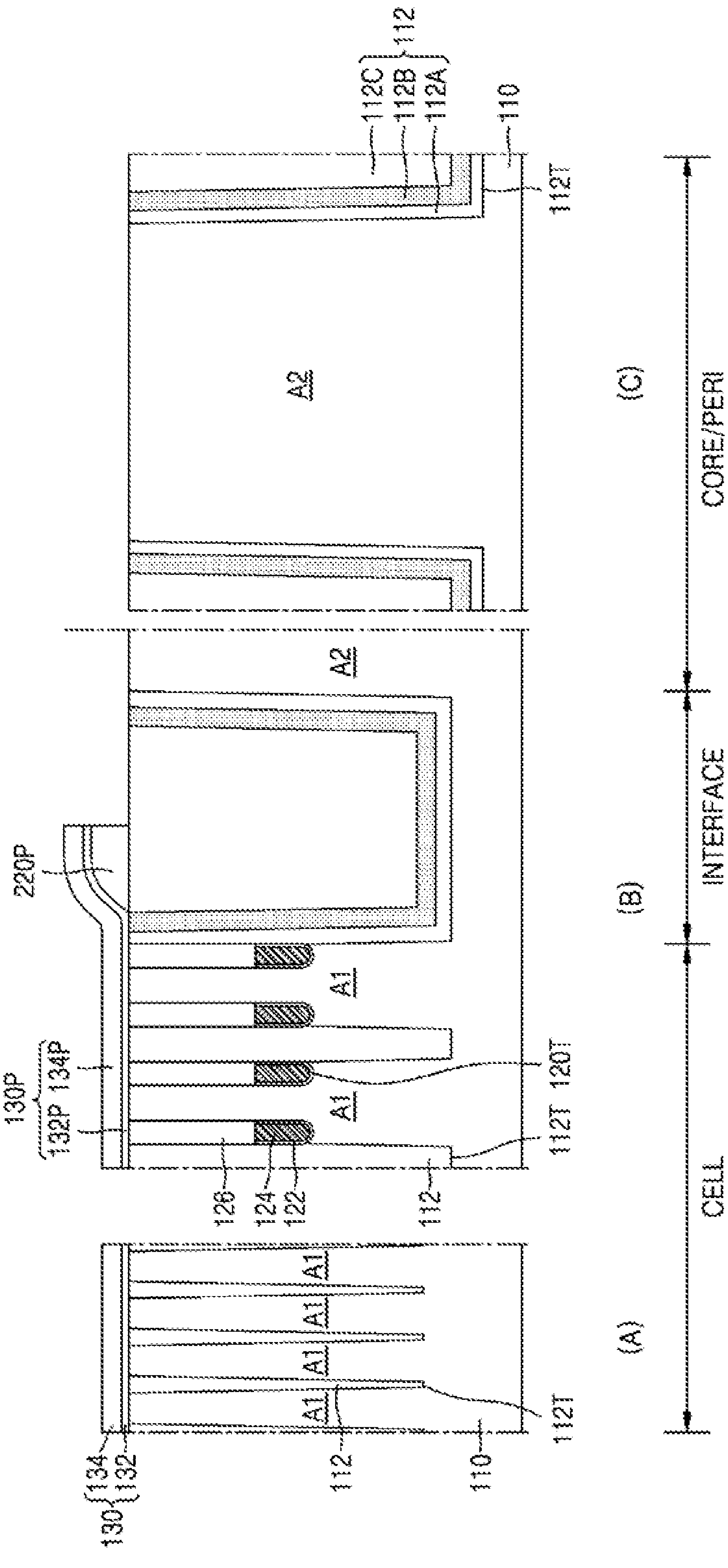

220
112C
112B
112A
112
110
112T
A2
A2
A1
A1
120T
112T
126
124
122
112
A1
A1
A1
A1
112
110
112T
(A)
(B)
(C)
CELL
INTERFACE
CORE/PERI

FIG. 12C



134
132
130
220
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
A2
(B)
INTERFACE
A1
120T
A1
112T
126
124
122
112
CELL
A1
A1
A1
A1
(A)
112T
134
132
130
112
110

FIG. 12D



130
134
132
112
110
112T
A1
126
124
122
130P
132P
134P
120T
220P
A2
112C
112B
112A
(A)
(B)
(C)
CELL
INTERFACE
CORE/PERI

FIG. 12E

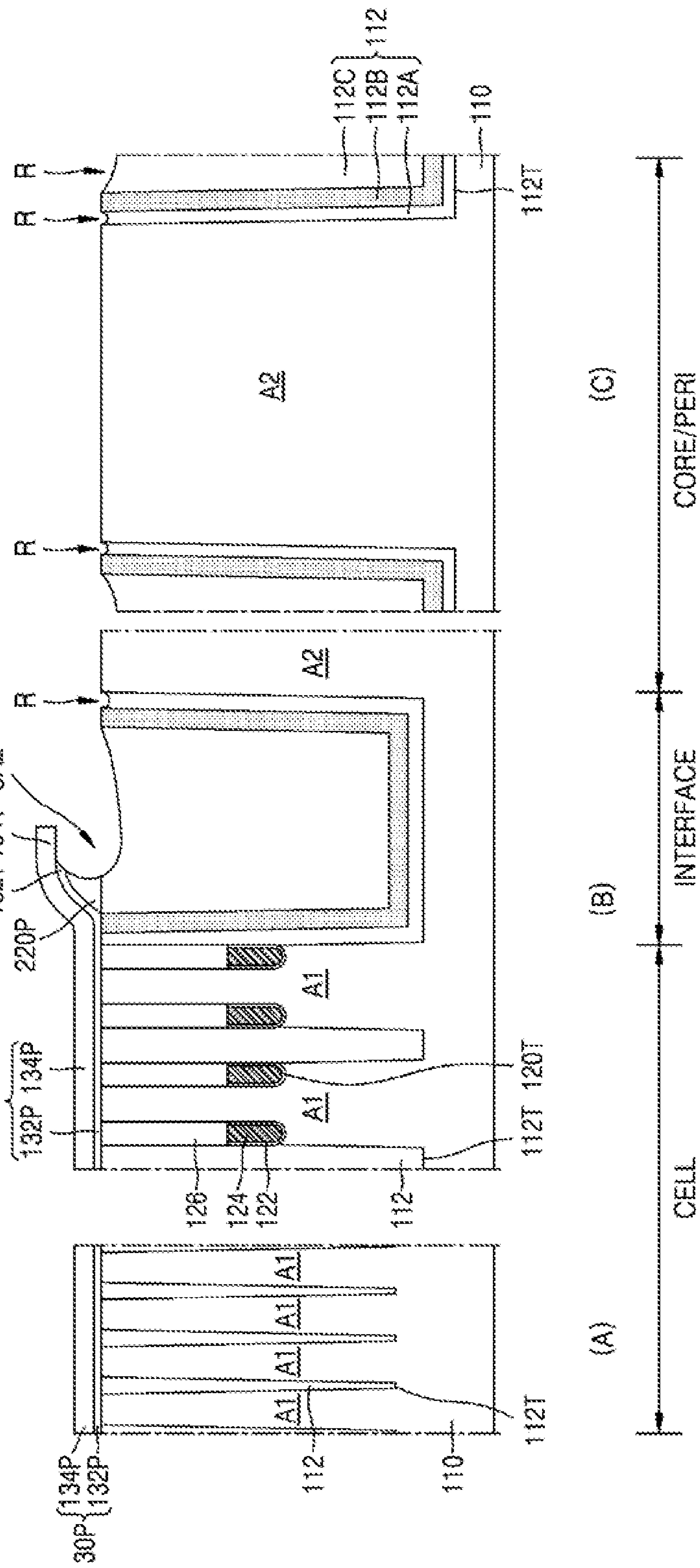

112C
112B
112A
112
110
112T
R
A2
(C)
CORE/PERI
A2
132T 134T UA2
220P
(B)
INTERFACE
130P
132P 134P
A1
120T
112T
126
124
122
112
CELL
(A)
A1
112
110
112T
130P
134P
132P

FIG. 12F

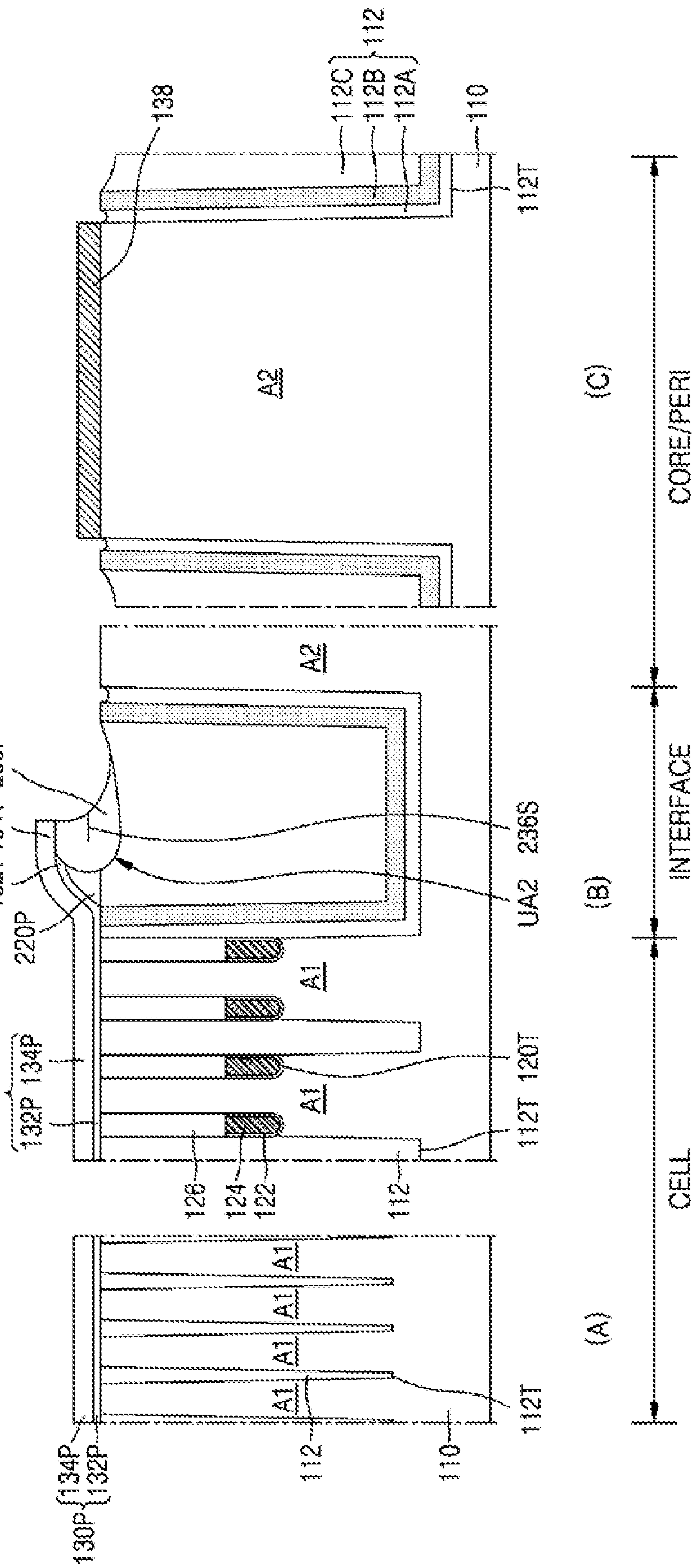
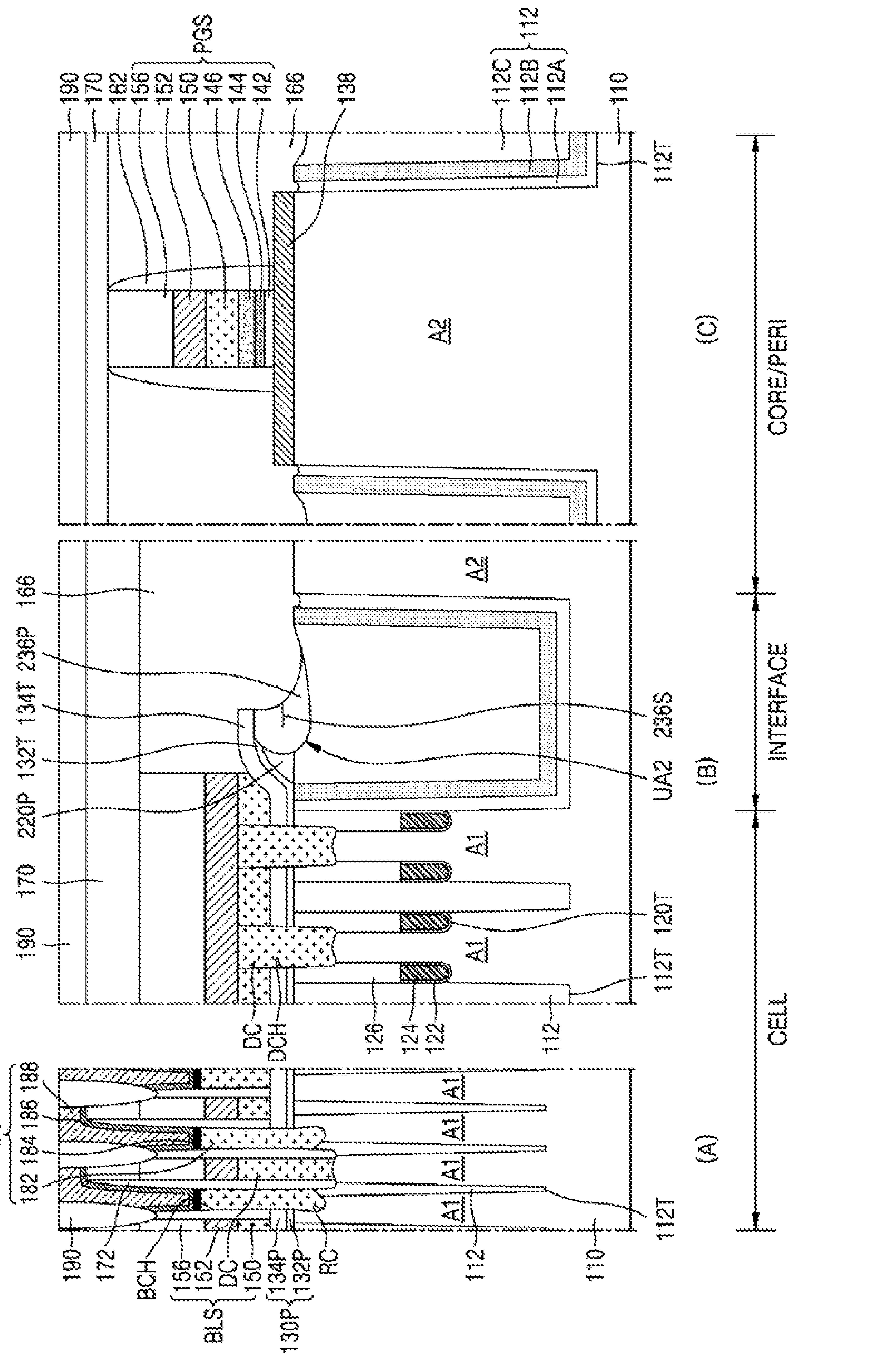

130P
134P
132P
112
110
112T
A1
(A)
CELL
126
124
122
132P
134P
120T
(B)
220P
132T
134T
236P
236S
UA2
A2
INTERFACE
138
112C
112B
112A
(C)
CORE/PERI

FIG. 12G



190
170
162
156
152
150
146
144
142
PGS
166
138
112C
112B
112A
112
110
112T
A2
(C)
CORE/PERI
166
236P
134T
132T
220P
236S
UA2
(B)
INTERFACE
170
190
120T
A1
112T
DC
DCH
126
124
122
112
CELL
BC
182
184
186
188
190
172
BCH
156
152
DC
150
134P
132P
RC
BLS
130P
110
(A)

INTEGRATED CIRCUIT DEVICE AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application is a Continuation of co-pending U.S. patent application Ser. No. 15/881,863, filed on Jan. 29, 2018, which claims priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2017-0067634, filed on May 31, 2017, in the Korean Intellectual Property Office, the disclosures of which are incorporated by reference herein in their entirety.

TECHNICAL FIELD

Exemplary embodiments of the present inventive concept relate to an integrated circuit device, and more particularly to a method of manufacturing the same.

DISCUSSION OF RELATED ART

With the development of electronic technology, down-scaling of integrated circuit devices has rapidly progressed, and integrated circuit devices are becoming more compact. Contamination by impurities such as metal particles during a manufacturing process of a compact integrated circuit device may reduce performance and yield of such integrated circuit devices.

SUMMARY

An exemplary embodiment of the present inventive concept provides an integrated circuit device in which contamination by impurities such as metal particles may be reduced or eliminated, thus increasing electric performance and reliability of the integrated circuit device.

An exemplary embodiment of the present inventive concept provides a method of manufacturing an integrated circuit device, in which, even when process tolerance is not sufficient due to the increased minuteness of patterns that are to be formed, contamination sources, for example, impurities such as metal particles, are reduced or eliminated, thus reducing or eliminating adverse effects by the impurities and increasing the yield and reliability of the integrated circuit device.

According to an exemplary embodiment of the present inventive concept, an integrated circuit device includes a substrate having a first region and a second region separated from each other along a direction parallel to an upper surface of the substrate. An interface device isolation layer fills an interface trench in an interface region between the first region and the second region and defines a portion of a first active area positioned in the first region and a portion of a second active area positioned in the second region. An insulation pattern extends from the first region to an upper portion of the interface device isolation layer. The insulation pattern covers the first active area and at least a portion of the interface device isolation layer. The insulation pattern defines an undercut area on an upper surface of the interface device isolation layer. A buried pattern substantially fills the undercut region.

According to an exemplary embodiment of the present inventive concept, an integrated circuit device includes a substrate comprising a cell array region including a cell active region and a peripheral circuit region including a peripheral circuit active region separated from each other along a direction parallel to an upper surface of the substrate. A first device isolation layer fills an interface trench extending in an interface region between the cell array region and the peripheral circuit region and defines a portion of the cell active region and a portion of the peripheral circuit active region. An insulation pattern extends from the cell array region to an upper portion of the first device isolation layer. The insulation pattern covers an upper surface of the cell active region and at least a portion of the first device isolation layer. The insulation pattern defines an undercut area on an upper surface of the first device isolation layer. A buried pattern substantially fills the undercut region.

According to an exemplary embodiment of the present inventive concept, a method of manufacturing an integrated circuit includes providing a substrate having a cell array region including a cell active region, a peripheral circuit region including a peripheral circuit active region separated from cell array region along a direction parallel to an upper surface of the substrate, and an interface region including a device isolation layer defining a portion of the cell active region and a portion of the peripheral circuit active region and positioned between the cell array region and the peripheral circuit region. The method includes forming an insulation pattern extending from the cell array region to an upper portion of the device isolation layer so as to cover an upper surface of the cell active region and at least a portion of the device isolation layer. The method includes forming an undercut area under the insulation pattern by removing a portion of the device isolation layer in the interface region. The method includes forming a buried pattern substantially filling the undercut area. The method includes forming an insulating layer covering the insulation pattern, the buried pattern, and the device isolation layer in the interface region.

The integrated circuit device according to an exemplary embodiment of the present inventive concept may have a structure in which the undercut region formed in the interface region is filled by a buried pattern so a metal contamination source may be prevented from remaining in the interface region. Thus, while dense and fine structures such as a plurality of bit line structures are formed in the cell array region, contamination of the minute structures by a metal contamination source may be reduced or eliminated, and degradation of electrical characteristics and reliability of the integrated circuit device to be manufactured may be prevented.

According to the method of manufacturing an integrated circuit device according to an exemplary embodiment of the present inventive concept, even when process tolerance is not sufficient due to the increased minuteness of patterns that are to be formed, contamination sources, for example, impurities such as metal particles, may be reduced or eliminated, thus preventing adverse effects due to the impurities during subsequent processes of forming minute patterns, and increasing the yield and reliability of the integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other features of the inventive concept will become more apparent by describing in detail exemplary embodiments thereof, with reference to the accompanying drawing, in which:

FIG. **1** is a plan view illustrating a schematic structure of an integrated circuit device according to an exemplary embodiment of the present inventive concept;

FIG. **2**A is a cross-sectional view of a schematic structure of an integrated circuit device according to an exemplary embodiment of the present inventive concept;

FIG. **2**B is an expanded cross-sectional view of a portion denoted as "CC" in FIG. **2**A;

FIGS. **3** through **7** are each cross-sectional views illustrating structures of an integrated circuit device according to an exemplary embodiment of the present inventive concept;

FIG. **8** is a structural block diagram of an integrated circuit device according to an exemplary embodiment of the present inventive concept;

FIG. **9** is a plan view of a schematic structure of an integrated circuit device according to an exemplary embodiment of the present inventive concept;

FIG. **10** is a schematic plan layout illustrating structures of a memory cell array region of an integrated circuit device according to an exemplary embodiment of the present inventive concept;

FIGS. **11**A through **11**P are cross-sectional views illustrating a method of manufacturing an integrated circuit device, according to an exemplary embodiment of the present inventive concept; and

FIGS. **12**A through **12**G are cross-sectional views illustrating a method of manufacturing an integrated circuit device, according to an exemplary embodiment of the present inventive concept.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Exemplary embodiments of the present inventive concept will be described below in more detail with reference to the accompanying drawings. In this regard, the exemplary embodiments may have different forms and should not be construed as being limited to the exemplary embodiments of the present inventive concept described herein. Like reference numerals may refer to like elements throughout the specification and drawings.

FIG. **1** is a plan view illustrating a schematic structure of an integrated circuit device according to an exemplary embodiment of the present inventive concept.

Referring to FIG. **1**, an integrated circuit device **10** may include a substrate **12** including a first region **22**, a second region **24** surrounding the first region **22**, and an interface region **26** positioned between the first region **22** and the second region **24** along a direction parallel to an upper surface of the substrate **12**.

The substrate **12** may include a semiconductor element such as Si or Ge or at least one compound semiconductor selected from SiGe, SiC, GaAs, InAs, or InP. The substrate **12** may include a conductive region such as an impurity-doped well or an impurity-doped structure.

In an exemplary embodiment of the present inventive concept, the first region **22** may be a memory cell region of the integrated circuit device **10**. The first region **22** may form a memory cell region of a volatile memory device or a memory cell region of a nonvolatile memory device. The memory cell region may be a memory cell region of a dynamic random-access memory (DRAM), a memory cell region of a magnetic RAM (MRAM), a memory cell region of a static RAM (SRAM), a memory cell region of a phase-change RAM (PRAM), or a memory cell region of a ferroelectric RAM (FRAM). The first region **22** may include any one type of memory cell selected from a DRAM memory cell, an MRAM memory cell, an SRAM memory cell, a PRAM memory cell, an RRAM memory cell, or a FRAM memory cell. The first region **22** may include a unit memory cell having a transistor and a capacitor, or a unit memory cell having a switching element and a variable resistor.

The second region **24** may be a core region or a peripheral circuit region (which may be referred to herein as a "peripheral circuit region"). Peripheral circuits driving memory cells in the first region **22** may be positioned in the second region **24**.

A plurality of conductive lines positioned to provide electrical connection between the first region **22** and the second region **24**, and insulating structures insulating between the first region **22** and the second region **24**, may be positioned in the interface region **26**.

In the interface region **26**, a buried pattern **30** may be formed to prevent unwanted residue from being deposited or remaining in the interface region **26**. The buried pattern **30** may have a planar shape surrounding the first region **22** (e.g., when viewed in a plan view). For example, the buried pattern **30** may have a closed loop shape surrounding the first region **22** along an X-Y plane. The buried pattern **30** may include at least one type of insulating material, or a combination of at least one type of insulating material and an air gap.

FIG. **2**A is a cross-sectional view of a schematic structure of an integrated circuit device according to an exemplary embodiment of the present inventive concept. The structure illustrated in FIG. **2**A is an example cross-section of a partial region of the integrated circuit device **10** illustrated in FIG. **1**, and may correspond to a cross-section cut along line II-II' of FIG. **1**.

Referring to FIG. **2**A, an interface trench **14**T extending along the interface region **26** between the first region **22** and the second region **24** may be formed in the substrate **12** of an integrated circuit device **10**A. The interface trench **14**T may be filled with an interface device isolation layer **14**. The interface device isolation layer **14** may include a silicon oxide layer, a silicon nitride layer, or a combination thereof.

The interface device isolation layer **14** may define a portion of a first active area AC**1** positioned in the first region **22** and a portion of a second active area AC**2** positioned in the second region **24**. The interface device isolation layer **14** may have a planar shape corresponding to a planar shape of the interface region **26** illustrated in FIG. **1**, so as to surround the first region **22** (e.g., in a plan view).

An insulation pattern **16** covering the first region **22** and the interface region **26** and extending in parallel to a main surface of the substrate **12** (X-Y plane) may be formed on the substrate **12**. The insulation pattern **16** may include a first insulation pattern **16**A and a second insulation pattern **16**B sequentially stacked on the substrate **12**. The first insulation pattern **16**A and the second insulation pattern **16**B may include different insulating materials from each other. For example, the first insulation pattern **16**A and the second insulation pattern **16**B may include different layers selected from an oxide layer and a nitride layer.

The first insulation pattern **16**A may extend to cover a portion of the first active area AC**1** and a portion of the interface device isolation layer **14**. The first insulation pattern **16**A may extend in the interface region **26** from the first region **22** toward the second region **24** to a first location that is a first horizontal distance HD**1** from the first region **22**.

The second insulation pattern **16**B may extend, with the first insulation pattern **16**A between the second insulation pattern **16**B and the first active region AC**1**, to cover a portion of the first active area AC**1** and a portion of the interface device isolation layer **14**. The second insulation pattern **16**B may extend in the interface region **26** from the first region **22** toward the second region **24**, to a second location at a second horizontal distance HD**2** from the first region **22** that is greater than the first horizontal distance HD**1**. The second location may be closer to the second region **24** than the first location is to the second region **24** along the direction parallel to the upper surface of the substrate **12**. Thus, a terminal portion TB of the second insulation pattern **168** may be closer to the second region **24** than a terminal portion TA of the first insulation pattern **16**A is to the second region **24** along the direction parallel to the upper surface of the substrate **12**.

In an exemplary embodiment of the present inventive concept, the first insulation pattern **16**A may be omitted, and the insulation pattern **16** may include only the second insulation pattern **16**B. In an exemplary embodiment of the present inventive concept, the insulation pattern **16** may include a multi-layer including at least three insulation patterns including the first insulation pattern **16**A and the second insulation pattern **16**B.

In the interface region **26**, an undercut area UA may be formed under the terminal portion TB of the second insulation pattern **16**B. The undercut area UA may be substantially filled with a buried pattern **30**A. A height of the buried pattern **30**A along a direction orthogonal to an upper surface of the substrate **12** may be defined by the interface device isolation layer **14** and the second insulation pattern **16**B. The buried pattern **30**A may include at least a portion of the buried pattern **30** described with reference to FIG. **1**.

As described above with respect to the buried pattern **30** with reference to FIG. **1**, the buried pattern **30**A may have a closed loop shape surrounding the first region **22** on the interface device isolation layer **14** along the X-Y plane. The buried pattern **30**A may include an insulating layer without a metal. For example, the buried pattern **30**A may include a silicon oxide, a silicon nitride, a silicon oxynitride (SiON), a silicon oxycarbonitride (SiOCN), polysilicon, or a combination thereof. The buried pattern **30**A may include a same material as one of the first insulation pattern **16**A and the second insulation pattern **16**B.

The first active area AC**1**, the second active area AC**2**, the interface device isolation layer **14**, the buried pattern **30**A, and the insulation pattern **16** may be covered by an insulating layer **40**. The insulating layer **40** may include an oxide layer, a nitride layer, or a combination thereof.

FIG. **2**B is an expanded cross-sectional view of a portion denoted as "CC" in FIG. **2**A.

Referring to FIGS. **2**A and **2**B, the buried pattern **30**A may include a convex surface CVX protruding toward the first region **22** and a concave surface CCV recessed toward a center of the buried pattern **30**A along the direction parallel to the upper surface of the substrate **12**. The concave surface CCV may face the second region **24**. In the interface region **26**, the convex surface CVX of the buried pattern **30**A may be in direct contact with the terminal portion TA of the first insulation pattern **16**A. In the interface region **26**, due to the convex surface CVX of the buried pattern **30**A, an interface between the interface device isolation layer **14** and the buried pattern **30**A may be a curved surface.

FIGS. **3** through **7** are each cross-sectional views illustrating structures of an integrated circuit device according to an exemplary embodiment of the present inventive concept. Integrated circuit devices **10**B, **10**C, **10**D, **10**E, and **10**F illustrated in FIGS. **3** through **7** are modified examples of the integrated circuit device **10**A illustrated in FIGS. **2**A and **2**B, and include modified structures of an area corresponding to the region denoted by "CC" of FIG. **2**A.

Referring to FIG. **3**, the integrated circuit device **10**B has substantially the same structure as the integrated circuit device **10**A illustrated in FIGS. **2**A and **2**B. For example, a buried pattern **30**B of the integrated circuit device **10**B has substantially the same structure as the buried pattern **30**A illustrated in FIGS. **2**A and **2**B. However, the buried pattern **30**B includes a seam line S**1** extending from the concave surface CCV facing the second region **24**, toward an inner portion of the buried pattern **30**B. The seam line S**1** may be formed during a deposition process in which the buried pattern **30**B is formed.

Referring to FIG. **4**, the integrated circuit device **10**C has substantially the same structure as the integrated circuit device **10**A illustrated in FIGS. **2**A and **2**B. For example, a buried pattern **30**C of the integrated circuit device **10**C has substantially the same structure as the buried pattern **30**A illustrated in FIGS. **2**A and **2**B. However, the buried pattern **30**C includes a seam line S**1** that extends from the concave surface CCV facing the second region **24**, toward an inner portion of the buried pattern **30**C, and an air gap AG**1** formed at an end of the seam line S**1**. The seam line S**1** and the air gap AG**1** may be formed during a deposition process in which the buried pattern **30**C is formed. The buried pattern **30**C may be at least a portion of the buried pattern **30** illustrated in FIG. **1**.

Referring to FIG. **5**, the integrated circuit device **10**D has substantially the same structure as the integrated circuit device **10**A illustrated in FIGS. **2**A and **2**B. For example, a buried pattern **30**D of the integrated circuit device **10**D has substantially the same structure as the buried pattern **30**A illustrated in FIGS. **2**A and **2**B. However, the integrated circuit device **10**D includes a local insulation pattern **38** positioned in the interface region **26** and surrounded by the interface device isolation layer **14**, the insulation pattern **16**, and the buried pattern **30**D. The local insulation pattern **38** may define a portion of the undercut area UA. The local insulation pattern **38** may be in direct contact with the convex surface CVX of the buried pattern **30**D. The local insulation pattern **38** may include a silicon oxide layer, a silicon nitride layer, or a combination thereof. The buried pattern **30**D may include at least a portion of the buried pattern **30** described with reference to FIG. **1**.

The first insulation pattern **16**A and the second insulation pattern **16**B may have a cross-sectional shape that is curved at a location adjacent to the local insulation pattern **38**. Portions of the first insulation pattern **16**A and the second insulation pattern **16**B that are in the first region **22** with respect to a point where the local insulation pattern **38** is positioned may extend in parallel to a main surface (X-Y plane) of the substrate **12** (see, e.g., FIG. **2**A), and portions of the first insulation pattern **16**A and the second insulation pattern **16**B on the local insulation pattern **38** may protrude upwards away from the interface device isolation layer **14** in a direction away from the first region **22** along the direction orthogonal to the upper surface of the substrate **12** so as to have a curved cross-sectional shape at the location adjacent to the local insulation pattern **38**. The terminal portions TA and TB of the first and second insulation patterns **16**A and **168** in the interface region **26** may be at a higher level than portions of the first insulation pattern **16**A and the second insulation pattern **16**B that are in the first region **22**. The term "level" used in the present specification refers to a height or a depth in a vertical direction with respect to the main surface of the substrate **12** (see FIG. **2**A) along the direction orthogonal to the upper surface of the substrate **12**. Thus, locations at the same level indicate those that are at a same height in a vertical upward direction from the main surface of the substrate **12** or those at a same depth into an inner portion of the substrate **12** from the main surface thereof. Locations at a lower level indicate those at a lower height in a vertical upward direction from the main surface of the substrate **12** or those at a deeper depth into the inner portion of the substrate **12** from the main surface thereof. Locations at a higher level indicate those at a higher height in a vertical upward direction from the main surface of the substrate **12** and those at a smaller depth into the inner portion of the substrate **12** from the main surface thereof.

Referring to FIG. **6**, the integrated circuit device **10**E has substantially the same structure as the integrated circuit device **10**D described with reference to FIG. **5**. For example, a buried pattern **30**E of the integrated circuit device **10**E has substantially the same structure as the buried pattern **30**D illustrated in FIG. **5**. However, the buried pattern **30**E includes a seam line S**2** extending from the concave surface CCV facing the second region **24**, toward an inner portion of the buried pattern **30**E. The seam line S**2** may be formed during a deposition process in which the buried pattern **30**E is formed. The buried pattern **30**E may include at least a portion of the buried pattern **30** described with reference to FIG. **1**.

Referring to FIG. **7**, the integrated circuit device **10**F has substantially the same structure as the integrated circuit device **10**D illustrated in FIG. **5**. For example, a buried pattern **30**F of the integrated circuit device **10**F has substantially the same structure as the buried pattern **30**D illustrated in FIG. **5**. However, the buried pattern **30**F includes a seam line S**2** extending from the concave surface CCV facing the second region **24**, toward an inner portion of the buried pattern **30**F, and an air gap AG**2** formed at an end of the seam line S**2**. The seam line S**2** and the air gap AG**2** may be formed during a deposition process in which the buried pattern **30**F is formed. The buried pattern **30**F may include at least a portion of the buried pattern **30** described with reference to FIG. **1**.

Referring to FIG. **1**, in an exemplary embodiment of the present inventive concept, the integrated circuit device **10** may be a DRAM device, and the first region **22** may be a memory cell region of the DRAM device.

FIG. **8** is a structural block diagram of an integrated circuit device according to an exemplary embodiment of the present inventive concept.

Referring to FIG. **8**, in the integrated circuit device **10**, the first region **22** may be a memory cell region of the DRAM device, and the second region **24** may be a peripheral circuit region of the DRAM device. The first region **22** may include a memory cell array **22**A. A plurality of memory cells for storing data in the memory cell array **22**A may be arranged in a row direction and a column direction. The plurality of memory cells may each include a cell capacitor and an access transistor. A gate of the access transistor may be connected to a corresponding word line from among a plurality of word lines arranged in the row direction, and one of a source and a drain of the access transistor may be connected to a bit line or a complementary bit line arranged in the column direction, and the other of the source and the drain may be connected to the cell capacitor.

The second region **24** may include a row decoder **52**, a sense amplifier **54**, a column decoder **56**, a self-refresh control circuit **58**, a command decoder **60**, a Mode Register Set/Extended Mode Register Set (MRS/EMRS) circuit **62**, an address buffer **64**, and a data input/output circuit **66**.

The sense amplifier **54** may sense and amplify data of a memory cell and store the data in the memory cell. The sense amplifier **54** may be implemented as a cross-coupled amplifier connected between a bit line and a complementary bit line included in the memory cell array **22**A.

Data DQ input through the data input/output circuit **66** may be written to the memory cell array **22**A based on an address signal ADD, and the data DQ read from the memory cell array **22**A based on the address signal ADD may be output to the outside through the data input/output circuit **66**. An address signal ADD may be input to the address buffer **64** so that a memory cell to or from which data is to be written or read may be designated. The address buffer **64** may temporarily store an address signal ADD that is input from an external source.

The row decoder **52** may decode a row address from among address signals ADD output from the address buffer **64**, in order to designate a word line connected to a memory cell to or from which data is to be input or output. For example, in a data write mode or a data read mode, the row decoder **52** may decode a row address output from the address buffer **64** and enable a corresponding word line. In a self-refresh mode, the row decoder **52** may decode a row address generated from an address counter and enable a corresponding word line.

The column decoder **56** may decode a column address from among address signals ADD output from the address buffer **64**, and thus may designate a bit line connected to the memory cell to or from which data is to be input or output. Data may be output from or written to a memory cell designated by row and column addresses or via the memory cell array **22**A.

The command decoder **60** may receive a command signal CMD applied from an external source, and may decode the signal to internally generate a decoded command signal such as a self-refresh entry command or a self-refresh exit command.

The MRS/EMRS circuit **62** may set an internal mode register in response to an MRS/EMRS command and an address signal ADD to designate an operation mode of the integrated circuit device **10**.

The integrated circuit device **10** may include a clock circuit that generates a clock signal or a power circuit that receives a power voltage applied from an external source and generates or distributes the internal voltage, or the like.

The self-refresh control circuit **58** may control a self-refresh operation of the integrated circuit device **10** in response to a command output from the command decoder **60**. The command decoder **60** may include an address counter, a timer, and a core voltage generator. In response to the self-refresh entry command output from the command decoder **60**, the address counter may generate a row address for designating a row address to self-refresh, and apply the row address to the row decoder **52**. The address counter may stop a counting operation in response to a self-refresh exit command output from the command decoder **60**.

FIG. **9** is a plan view of a schematic structure of an integrated circuit device according to an exemplary embodiment of the present inventive concept.

Referring to FIG. **9**, an integrated circuit device **70** may include a plurality of first regions **22**. The plurality of first regions **22** may each be surrounded by the second region **24** (e.g., when viewed in a plan view), with the interface region **26** therebetween. In the integrated circuit device **70**, the plurality of first regions **22** may each be a memory cell array region MCA of a DRAM device, and the second region **24** may be a peripheral circuit region of the DRAM device.

The memory cell array region MCA in the plurality of first regions **22** may include the memory cell array **22**A described with reference to FIG. **8**. The plurality of first regions **22** may be each surrounded by the interface region **26** (e.g., when viewed in a plan view). The buried pattern **30** described with reference to FIG. **1** may be formed in the interface region **26**. The buried pattern **30** may have a cross-section of at least one of the buried patterns **30**A, **30**B, **30**C, **30**D, **30**E, and **30**F described with reference to FIGS. **2**A through **7**.

The second region **24** may include a sub-word line driver block SWD, a sense amplifier block S/A, and a conjunction block CJT. In the second region **24**, a plurality of sub-word line driver blocks SWD may be arranged in a word line direction of the memory cell array region MCA, and a plurality of sense amplifier blocks S/A may be arranged in a bit line direction. A plurality of bit line sense amplifiers may be arranged in the sense amplifier blocks S/A. The conjunction block CJT may be arranged at a position where the sub-word line driver blocks SWD and the sense amplifier blocks S/A intersect with each other. In the conjunction block CJT, power drivers and ground drivers for driving the bit line sense amplifiers may be alternately arranged.

A peripheral circuit such as an inverter chain, or an input/output circuit may be further formed in the second region **24**.

FIG. **10** is a schematic plan layout illustrating structures of a memory cell array region of an integrated circuit device according to an exemplary embodiment of the present inventive concept.

Referring to FIG. **10**, the memory cell array region MCA may include a plurality of cell active regions A**1**. The plurality of cell active regions A**1** may be arranged to have a long axis in a diagonal direction with respect to a first direction (X direction) and a second direction (Y direction).

A plurality of word lines WL may extend in parallel to each other across the plurality of cell active regions A**1** and in the first direction (X direction). A plurality of bit lines BL may extend in parallel to each other above the plurality of word lines WL in the second direction (Y direction) crossing the first direction (X direction). The plurality of bit lines BL may be connected to the plurality of cell active regions A**1** via direct contacts DC.

A plurality of buried contacts BC may be formed between two adjacent bit lines from among the plurality of bit lines BL. The plurality of buried contacts BC may be arranged in a matrix in the first direction (X direction) and the second direction (Y direction). A plurality of landing pads LP may be formed on the plurality of buried contacts BC. The plurality of buried contacts BC and the plurality of landing pads LP may be used to connect, to the cell active regions A**1**, a bottom electrode of a capacitor that is formed on the plurality of bit lines BL. The plurality of landing pads LP may be arranged to each partially overlap the buried contacts BC along the direction orthogonal to the upper surface of the substrate **12**.

FIGS. **11**A through **11**P are cross-sectional views illustrating a method of manufacturing an integrated circuit device, according to an exemplary embodiment of the present inventive concept. A method of manufacturing an integrated circuit device including the DRAM device having the structure described with reference to FIGS. **8** through **10** will be described in more detail below with reference to FIGS. **11**A through **11**P.

FIGS. **11**A through **11**P illustrate cross-sectional structures of a cell array region CELL, a peripheral circuit region CORE/PERI, and an interface region INTERFACE. The cell array region CELL may include at least a portion of the first region **22** described with reference to FIGS. **1** and **9**. The interface region INTERFACE may include at least portion of the interface region **26** described with reference to FIGS. **1** and **9**. The peripheral circuit region CORE/PERI may include at least a portion of the second region **24** described with reference to FIGS. **1** and **9**. In FIGS. **11**A through **11**P, a cross-section denoted by (A) may correspond to a partial region of FIG. **10** along a cross-section taken along line A-A', and a cross-section denoted by (B) may correspond to a partial region of FIG. **10** along a cross-section taken along line B-B' and a partial region of the interface region INTERFACE adjacent to the above partial region.

Referring to FIG. **11**A, a substrate **110** including a cell array region CELL, a peripheral circuit region CORE/PERI, and an interface region INTERFACE positioned therebetween may be provided. The cell array region CELL and the peripheral circuit region CORE/PERI may be spaced apart from each other along a direction parallel to an upper surface of the substrate **110**. After forming a plurality of device isolation trenches **112**T in the substrate **110**, a plurality of device isolation layers **112** filling the plurality of device isolation trenches **112**T may be formed. A plurality of cell active regions A**1** may be defined on the substrate **110** in the cell array region CELL by the plurality of device isolation layers **112**, and a peripheral circuit active region A**2** may be defined in the peripheral circuit region CORE/PERI. The plurality of cell active regions A**1** may each have a relatively long and planar island-type shape having a short axis and a long axis (see, e.g., FIG. **10**). The interface region INTERFACE may be defined by a device isolation layer **112** positioned between the cell active region A**1** and the peripheral circuit active region A**2** from among the plurality of device isolation layers **112**. The device isolation layer **112** in the interface region INTERFACE may extend along a periphery of the cell array region CELL so as to have a shape surrounding the cell array region CELL when viewed from a plan view. From among the plurality of device isolation layers **112**, a width of the device isolation layer **112** arranged in the cell array region CELL may be smaller than a width of the device isolation layer **112** disposed in the interface region INTERFACE along a direction orthogonal to an upper surface of the substrate **110**.

The substrate **110** may have substantially the same structure as the substrate **12** described with reference to FIG. **2**A. The device isolation layer **112** may include a silicon oxide layer, a silicon nitride layer, or a combination thereof; however, exemplary embodiments of the present inventive concept are not limited thereto. The device isolation layer **112** may include a single layer including a single insulating material, or a dual layer including two layers each including a different insulating material, or a multi-layer including at least two layers each including a different insulating material.

In the peripheral circuit region CORE/PERI and the interface region INTERFACE, the device isolation layer **112** may include a first insulation liner **112**A and a second insulation liner **112**B sequentially formed on an internal wall of the device isolation trench **112**T, and a buried insulating layer **112**C on the second insulation liner **112**B and filling the device isolation trench **112**T. In an exemplary embodiment of the present inventive concept, the first insulation liner **112**A may include an oxide layer, the second insulation liner **112**B may include a nitride layer, and the buried insulating layer **112**C may include an oxide layer.

In an exemplary embodiment of the present inventive concept, an oxide layer included in the first insulation liner **112**A may be a medium temperature oxidation (MTO) layer, a high density plasma (HDP) oxide layer, a thermal oxide layer, a tetraethyl orthosilicate (TEOS) layer, or an undoped silicate glass (USG) layer. The second insulation liner **112**B may be a silicon nitride layer. In an exemplary embodiment of the present inventive concept, an oxide layer forming the buried insulating layer **112**C may be a Tonen silazane (TOSZ), an HDP oxide layer or a USG oxide layer. In an exemplary embodiment of the present inventive concept, an oxide layer forming the buried insulating layer **112**C may be silicate, siloxane, methyl silsesquioxane (MSQ), hydrogen silsesquioxane (HSQ), polysilazane, or a spin-on-glass (SOG) oxide layer including a combination thereof.

In the cell array region CELL, a plurality of word line trenches **120**T extending in parallel to each other may be formed in the substrate **110**. After cleaning a resultant product on which the plurality of word line trenches **120**T are formed, a gate dielectric layer **122**, a word line **124**, and a buried insulating layer **126** may be sequentially formed in each of the plurality of word line trenches **120**T. The plurality of word lines **124** may be the plurality of word lines WL described with reference to FIG. **10**.

A plurality of source/drain regions may be formed on an upper surface of the plurality of cell active regions A**1** by injecting impurity ions into both portions of the plurality of word lines **124** in the plurality of cell active regions A**1**. In an exemplary embodiment of the present inventive concept, the source/drain regions may also be formed before forming of the plurality of word lines **124**.

The plurality of gate dielectric layers **122** may include a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, an oxide/nitride/oxide (ONO) layer, or a high-k dielectric film having a higher dielectric constant than a silicon oxide layer. For example, the plurality of gate dielectric layers **122** may have a dielectric constant of from about 10 to about 25. In an exemplary embodiment of the present inventive concept, the plurality of gate dielectric layers **122** may include HfO_2, Al_2O_3, $HfAlO_3$, Ta_2O_3, or TiO_2. The plurality of word lines **124** may be formed of Ti, TiN, Ta, TaN, W, WN, TiSiN, WSiN, or a combination thereof. The plurality of buried insulating layers **126** may include a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, or a combination thereof.

Referring to FIG. **11**B, an insulating layer **130** may be formed on the substrate **110** in the cell array region CELL, the interface region INTERFACE, and the peripheral circuit region CORE/PERI. The insulating layer **130** may include a first insulating layer **132** and a second insulating layer **134** sequentially formed on the substrate **110**. The first insulating layer **132** and the second insulating layer **134** may each include different insulating materials. For example, the first insulating layer **132** may include an oxide layer, and the second insulating layer **134** may include a nitride layer; however, exemplary embodiments of the present inventive concept are not limited thereto.

Referring to FIG. **11**C, an insulation pattern **130**P may be formed by removing a portion of the insulating layer **130**. To form the insulation pattern **130**P, a first insulation pattern **132**P and a second insulation pattern **134**P may be formed by removing portions of the first insulating layer **132** and the second insulating layer **134**.

To form the first insulation pattern **132**P and the second insulation pattern **134**P, portions of the first insulating layer **132** and the second insulating layer **134** covering the peripheral circuit region CORE/PERI and a portion of the interface region INTERFACE may be removed. Thus, the first insulation pattern **132**P and the second insulation pattern **134**P covering the cell array region CELL and a portion of the interface region INTERFACE that is adjacent to the cell array region CELL may remain.

In an exemplary embodiment of the present inventive concept, to remove portions of the first insulating layer **132** and the second insulating layer **134**, a dry etching method, a wet etching method, or a combination thereof may be used. In an exemplary embodiment of the present inventive concept, the insulating layer **130** may be covered with a mask pattern, and then the mask pattern may be used as an etching mask to sequentially dry-etch the second insulating layer **134** and the first insulating layer **132** to thus form the second insulation pattern **134**P and the first insulation pattern **132**P. In an exemplary embodiment of the present inventive concept, a portion of the second insulating layer **134** may be dry-etched by using the mask pattern as an etching mask, to thus form the second insulation pattern **134**P exposing the first insulating layer **132**, and then the exposed first insulating layer **132** may be wet-etched to form the first insulation pattern **132**P.

After the first insulation pattern **132**P and the second insulation pattern **134**P are formed, an upper surface of the peripheral circuit active region A**2** may be exposed in the peripheral circuit region CORE/PERI.

Referring to FIG. **11**D, an undesired natural oxide layer on the peripheral circuit active region A**2** may be removed by cleaning an exposed surface of the peripheral circuit active region A**2** in the peripheral circuit region CORE/PERI. In an exemplary embodiment of the present inventive concept, a plasma dry cleaning operation may be used to clean the exposed surface of the peripheral circuit active region A**2**. During the plasma dry cleaning operation, a hydrogen gas may be used as a cleaning gas. By using the hydrogen gas, an undesired natural oxide layer on the peripheral circuit active region A**2** may be reduced or eliminated. For example, plasma may be generated by injecting a process gas including H_2 and SiH_2 into a plasma generator, and then a surface of the peripheral circuit active region A**2** may be cleaned using a radical activated by the generated plasma. In an exemplary embodiment of the present inventive concept, a wet cleaning operation may be used to clean the exposed surface of the peripheral circuit active region A**2**. The wet cleaning operation may be performed using an HF solution.

During the cleaning operation in which an undesired natural oxide layer is removed from the exposed surface of the peripheral circuit active region A**2**, a portion of the interface region INTERFACE and the peripheral circuit region CORE/PERI may be exposed to the cleaning atmosphere of the cleaning operation, and as a result, portions of the device isolation layer **112** that are in the interface region INTERFACE and the peripheral circuit region CORE/PERI and include an oxide may also be partially consumed by the cleaning atmosphere so as to form a recess R in an upper portion of each of the first insulation liner **112**A and the buried insulating layer **112**C. For example, in the interface region INTERFACE, the buried insulating layer **112**C of the device isolation layer **112** and the first insulation pattern **132**P may be consumed together by the cleaning atmosphere under a terminal portion **134**T of the second insulation pattern **134**P to form an undercut region UA**1** under the terminal portion **134**T of the second insulation pattern **134**P. The undercut region UA**1** may be defined by a convex surface CVX that extends convexly toward the cell array region CELL. The convex surface CVX may be defined by a terminal portion **132**T of the first insulation pattern **132**P and an upper surface of the buried insulating layer **112**C. The undercut region UA**1** may be formed to have an opening facing the peripheral circuit region CORE/PERI.

Referring to FIG. **11**E, a buried mask layer **136** burying the undercut region UA**1** may be formed on the substrate **110**. The buried mask layer **136** may be formed to have a thickness sufficient to fill the undercut region UA**1**.

The buried mask layer **136** may prevent epitaxial growth in undesired portions on the substrate **110**. The buried mask layer **136** may include a hole **136**H exposing a region of the peripheral circuit active region A**2** of the peripheral circuit region CORE/PERI that is formed by an epitaxial growth process of a semiconductor layer. While one hole **136**H is illustrated in FIG. **11**E, exemplary embodiments of the present inventive concept are not limited thereto, and a plurality of holes **136**H may be formed in the buried mask layer **136** to expose different regions of the peripheral circuit active areas A**2**.

In an exemplary embodiment of the present inventive concept, referring to FIG. **11**E, a seam portion **136**S having a line shape may be formed at a portion of the buried mask layer **136** that fills the undercut region UA**1**. The seam portion **136**S may be formed because layers used to form the buried mask layer **136** are continually built up from an inner surface of the undercut region UA**1** while facing each other during a process of forming the buried mask layer **136**, such that the layers end up contacting each other approximately in a center portion of the undercut region UA**1**. The seam portion **136**S may have a line shape extending toward the entrance of the undercut region UA**1** according to a cross-sectional view of the buried mask layer **136**.

In an exemplary embodiment of the present inventive concept, the seam portion **136**S or a seam portion having a similar shape need not be left in the undercut region UA**1** after the buried mask layer **136** is formed. In an exemplary embodiment of the present inventive concept, after forming the buried mask layer **136**, an air gap having a similar shape as the air gap AG**1** described with reference to FIG. **4** or the air gap AG**2** described with reference to FIG. **7** may be left in a region adjacent to the seam portion **136**S within the undercut region UA**1**.

The buried mask layer **136** may include an insulating film not including a metal. For example, the buried mask layer **136** may include a silicon oxide, a silicon nitride, a silicon oxynitride (SiON), a silicon oxynitride (SiOCN), polysilicon, or a combination thereof; however, exemplary embodiments of the present inventive concept are not limited thereto.

A chemical vapor deposition (CVD) process or an atomic layer deposition (ALD) process may be used to form the buried mask layer **136**; however, exemplary embodiments of the present inventive concept are not limited thereto.

Referring to FIG. **11**F, the buried mask layer **136** may be used as an epitaxial growth-preventing mask to perform a selective epitaxial growth process to grow a semiconductor material from a surface of the peripheral circuit active region A**2** exposed through the hole **136**H of the buried mask layer **136**, thus forming a semiconductor layer **138**.

The semiconductor layer **138** may include a compound semiconductor formed of a combination of elements of Group IV of the periodic table according to International Union of Pure and Applied Chemistry (IUPAC). For example, the semiconductor layer **138** may include SiGe. In an exemplary embodiment of the present inventive concept, the semiconductor layer **138** may have a thickness of about 20 Å to about 200 Å (e.g., along the direction orthogonal to the upper surface of the substrate **110**). When the semiconductor layer **138** includes SiGe, a Ge content in the semiconductor layer **138** may be about 10 atom % (at. %) to about 50 atom % (at. %).

In an exemplary embodiment of the present inventive concept, the device isolation layer **112** adjacent to the peripheral circuit active region A**2** may also be exposed through the hole **136**H of the buried mask layer **136**. In this case, during the selective epitaxial process, the semiconductor layer **138** may be formed only on a surface of the peripheral circuit active region A**2**, and need not be formed on the device isolation layer **112**.

Referring to FIG. **11**G, the buried mask layer **136** may be isotropically etched such that a portion of the buried mask layer **136** filling the undercut region UA**1** remains and the other portion of the buried mask layer **136** is removed. The portion of the buried mask layer **136** that fills the undercut region UA**1** may be left as a buried pattern **136**P. After the buried pattern **136**P is formed, the second insulation pattern **134**P may be exposed in the cell array region CELL, and an upper surface of the device isolation layer **112** may be exposed in the interface region INTERFACE and the peripheral circuit region CORE/PERI.

The buried pattern **136**P may extend along a periphery of the cell array region CELL to have a closed loop shape surrounding the cell array region CELL (e.g., when viewed in a plan view).

In an exemplary embodiment of the present inventive concept, the seam portion **136**S may be left in the buried pattern **136**P. In an exemplary embodiment of the present inventive concept, the seam portion **136**S need not be left in the buried pattern **136**P. In an exemplary embodiment of the present inventive concept, an air gap having a shape similar to the air gap AG**1** described with reference to FIG. **4** or the air gap AG**2** described with reference to FIG. **7** may be left in a region in the buried pattern **136**P adjacent to the seam portion **136**S. The buried pattern **136**P may include the convex surface CVX facing the cell array region CELL and the concave surface CCV recessed towards a center of the buried pattern **136**P. The concave surface CCV may face the peripheral circuit region CORE/PERI. In the interface region INTERFACE, the convex surface CVX of the buried pattern **136**P may be in direct contact with the terminal portion **132**T of the first insulation pattern **132**P. In the interface region INTERFACE, an interface between the device isolation layer **112** and the buried pattern **136**P may be a curved surface due to the convex surface CVX of the buried pattern **136**P.

In the interface region INTERFACE, as the undercut area UA**1** between the device isolation layer **112** and the second insulation pattern **134**P is filled with the buried pattern **136**P, undesirable contaminants, particularly, of metal particles, may be prevented from penetrating or remaining in the undercut region UA**1** during subsequent processes.

Referring to FIG. **11**H, a first dielectric layer **142**, a second dielectric layer **144**, and a work function controlling layer **146** including a metal may be sequentially formed on the substrate **110** in the cell array region CELL, the interface region INTERFACE, and the peripheral circuit region CORE/PERI of the substrate **110**.

The first dielectric layer **142** may include, for example, a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, or an oxide/nitride/oxide (ONO) layer. The first dielectric layer **142** may have a smaller thickness than the semiconductor layer **138** formed in the peripheral circuit region CORE/PERI (e.g., along the direction orthogonal to the upper surface of the substrate **110**). The first dielectric layer **142** may be formed using a CVD process or an ALD process.

The second dielectric layer **144** may include a high-k dielectric layer having a dielectric constant higher than a silicon oxide layer. The second dielectric layer **144** may have a higher dielectric constant than the first dielectric layer **142**. The second dielectric layer **144** may layer including metal and having a dielectric constant of from about 10 to about 25. For example, the second dielectric layer **144** may include HfO_2, Al_2O_3, $HfAlO_3$, Ta_2O_3, or TiO_2. The second dielectric layer **144** may have a smaller thickness than the first dielectric layer **142** (e.g., along the direction orthogonal to the upper surface of the substrate **110**).

The work function controlling layer **146** including a metal may include a metal, a conductive metal nitride, a conductive metal carbide, a conductor containing a metal atom, or a combination thereof. The work function controlling layer **146** including a metal may have a single-layered or multi-layered structure. The work function controlling layer **146** including a metal may include at least one material selected from Ti, Ta, Al, Ni, Co, La, Pd, Nb, Mo, Hf, Ir, Ru, Pt, Yb, Dy, Er, Pd, TiAl, HfSiMo, TiN, WN, TaN, RuN, MoN, TiAlN, TaC, TiC, or TaC. In an exemplary embodiment of the present inventive concept, the work function controlling layer **146** including a metal may include at least one stack structure selected from TiN/TiN, TiN/TiON, TiN/TiN, TaN/TiN, La/TiN, Al/TiN, Mg/TiN, or Sr/TiN. Here, TiN may be replaced by TaN, TaCN, TiCN, CoN, or CoCN, and La may be replaced by LaO or LaON.

Since the operations of forming the first dielectric layer **142**, the second dielectric layer **144**, and the work function controlling layer **146** including a metal are performed while the undercut region UA**1** is filled with the buried pattern **136**P, the first dielectric layer **142**, the second dielectric layer **144**, and the work function controlling layer **146** including a metal are not formed in the undercut region UA**1**.

Referring to FIG. **11**I, a portion of each of the first dielectric layer **142**, the second dielectric layer **144**, and the work function controlling layer **146** including a metal may be removed to expose the second insulation pattern **134**P and the buried pattern **136**P.

To expose the second insulation pattern **134**P and the buried pattern **136**P in the cell array region CELL and the interface region INTERFACE, an etching process may be performed to remove portions of the first dielectric layer **142**, the second dielectric layer **144**, and the work function controlling layers **146** including a metal that cover the cell array region CELL and a portion of the interface region INTERFACE adjacent to the cell array region CELL. Thus, remaining portions of the first dielectric layer **142**, the second dielectric layer **144**, and the work function controlling layer **146** including a metal may cover only the peripheral circuit region CORE/PERI and a portion of the interface region INTERFACE that is adjacent to the peripheral circuit region CORE/PERI.

While the first dielectric layer **142**, the second dielectric layer **144**, and the work function controlling layer **146** including a metal are being etched in the cell array region CELL and the interface region INTERFACE, metal elements included in the second dielectric layer **144** and/or the work function controlling layer **146** including a metal may remain on the substrate **110** as a by-product or residue to act as a metal contamination source. For example, if the undercut region UA**1** is not filled with the buried pattern **136**P, the metal contamination source may be deposited in the undercut region UA**1**. In this case, even if a cleaning process is performed to remove the metal contamination source, it may be difficult to remove the metal contamination source remaining in deep portions of the undercut region UAL. If a subsequent process is performed in a state where a metal contaminant remains in deep portions of the undercut region UA**1**, for example, during an etching process of forming a plurality of bit lines in the cell array region CELL in a subsequent process, or during an etching process of forming a plurality of contact plugs between a plurality of bits lines, the metal contamination source remaining in the deep portions of the undercut region UA**1** may be undesirably exposed, and this may degrade electric characteristics and reliability of a device to be manufactured.

However, according to the method of manufacturing an integrated circuit device according to an exemplary embodiment of the present inventive concept, the first dielectric layer **142**, the second dielectric layer **144**, and the second dielectric layer **144** may be etched while the undercut region UA**1** is filled with the buried pattern **136**P, and thus, when a metal contamination source remains in the interface region INTERFACE on the substrate **110** as a result of etching the first dielectric layer **142**, the second dielectric layer **144**, and the work function controlling layer **146** including a metal, the remaining metal contamination source may be relatively easily eliminated through a cleaning process. Thus, subsequent processes may be performed while an exposed surface of each of the second insulation pattern **134**P, the buried pattern **136**P, and the device isolation layer **112** exposed in the cell array region CELL and the interface region INTERFACE is not contaminated.

Referring to FIG. **11**J, a first conductive layer **150** extending on the substrate **110** in the cell array region CELL, the interface region INTERFACE, and the peripheral circuit region CORE/PERI may be formed, and then, in the cell array region CELL, a portion of each of the first conductive layer **150**, the second insulation pattern **134**P, and the first insulation pattern **132**P, and a portion of the substrate **110**, may be etched to form a plurality of direct contact holes DCH that pass through the first conductive layer **150**, the second insulation pattern **134**P, and the first insulation pattern **132**P to expose the cell active region A**1**. A plurality of direct contacts DC may be formed to fill the plurality of direct contact holes DCH.

The first conductive layer **150** may include doped polysilicon or a metal such as W, Mo, Au, Cu, Al, Ni, or Co. The first conductive layer **150** may include a single layer including one material selected from the above-described materials, or a multi-layer including at least two layers each respectively including a different one of the above-described materials from each other.

The direct contacts DC may include doped polysilicon or a metal such as W, Mo, Au, Cu, Al, Ni, or Co. In an exemplary embodiment of the present inventive concept, the direct contacts DC may include the same material as the material of the first conductive layer **150**.

In an exemplary embodiment of the present inventive concept, a metal silicide layer may be further formed between the substrate **110** and the direct contacts DC. For example, the metal silicide layer may include tungsten silicide, nickel silicide, or cobalt silicide; however, exemplary embodiments of the present inventive concept are not limited thereto.

Referring to FIG. **11**K, a second conductive layer **152** and an insulation capping layer **156** extending on the first conductive layer **150** in the cell array region CELL, the interface region INTERFACE, and the peripheral circuit region CORE/PERI may be formed.

The second conductive layer **152** may include TiSiN, TiN, TaN, CoN, a metal, a metal silicide, or a combination thereof. The metal and the metal silicide may include W, Mo, Au, Cu, Al, Ni, or Co.

The insulating capping layer **156** may include a silicon nitride layer.

Referring to FIG. **11**L, while the cell array region CELL and a portion of the interface region INTERFACE adjacent thereto may be protected using a mask pattern, a peripheral circuit stack structure including the first dielectric layer **142**, the second dielectric layer **144**, the work function controlling layer **146** including a metal, the first conductive layer **150**, the second conductive layer **152**, and the insulating capping layer **156** may be etched in the peripheral circuit area CORE/PERI and a periphery thereof to form a peripheral circuit gate structure PGS in the peripheral circuit region CORE/PERI.

While etching the peripheral circuit stack structure to form the peripheral circuit gate structure PGS in the peripheral circuit region CORE/PERI, the interface region INTERFACE may be exposed to the etching atmosphere of the peripheral circuit stack structure. If the undercut region UA**1** is not filled with the buried pattern **136**P and a metal contamination source remains in the undercut region UA**1**, the metal contamination source may be scattered in the etching atmosphere, and thus, the peripheral circuit gate structure PGS may be directly exposed to the metal contamination source such that it becomes contaminated. Alternatively, new metal contaminants may be deposited in the undercut region UA**1** while etching the peripheral circuit stack structure. However, according to the method of manufacturing an integrated circuit device according to an exemplary embodiment of the present inventive concept, while the etching process of the metal-containing layers as described with reference to FIG. **11**I and the etching process of the peripheral circuit stack structure as described with reference to FIG. **11**L are performed, since the undercut region UA**1** is filled with the buried pattern **136**P, the metal contamination source does not remain in the undercut region UA**1**. Thus, the peripheral circuit gate structure PGS is not contaminated by the metal contamination source, and a new metal contamination source is not deposited in the undercut region UA**1**.

After forming an insulating spacer **162** covering both sidewalls of the peripheral circuit gate structure PGS, an interlayer insulating layer **166** covering the peripheral circuit gate structure PGS and the insulating spacer **162** may be formed.

The insulating spacer **162** may include an oxide layer, a nitride layer, or a combination thereof. The insulating spacer **162** may include a single layer or multiple layers.

The interlayer insulating layer **166** may include an HDP oxide layer or a silicon oxide layer formed by a flowable CVD (FCVD) method.

Referring to FIG. **11**M, a mask pattern **170** may be formed above the substrate **110**. The peripheral circuit region CORE/PERI and the interface region INTERFACE may be protected by the mask pattern **170**, and an upper surface of the insulating capping layer **156** may be partially exposed in the cell array region CELL. The mask pattern **170** may include a silicon nitride layer.

Referring to FIG. **11**N, the cell stack structure including the direct contact DC, the first conductive layer **150**, the second conductive layer **152**, and the insulation capping layer **156** in the cell array region CELL may be etched using the mask pattern **170** as an etching mask to form a plurality of bit line structures BLS extending in parallel to each other in the cell array region CELL. The first conductive layer **150** and the second conductive layer **152** included in the plurality of bit line structures BLS may form the bit line BL (see, e.g., FIG. **10**).

While etching the cell stack structure to form the plurality of bit line structures BLS, the interface region INTERFACE surrounding the cell array region CELL may be exposed to the etching atmosphere of the cell stack structure. If the undercut region UA**1** is not filled with the buried pattern **136**P and a metal contamination source remains in the undercut region UA**1**, the metal contamination source remaining in the undercut region UA**1** may be scattered in the etching atmosphere, and thus, the plurality of bit line structures BLS may be directly exposed to the metal contamination source such that they become contaminated. However, according to the method of manufacturing an integrated circuit according to an exemplary embodiment of the present inventive concept, an etching operation for layers including metal, as described above with reference to FIG. **11**I, may be performed while the undercut region UA**1**, in which metal contamination sources may remain, is filled with the buried pattern **136**P, and an etching operation is performed to form a peripheral circuit stack structure as described with reference to FIG. **11**L. Thus, the cell stack structure may be etched in the cell array region CELL while no undesirable contamination sources remain in the undercut region UA**1**. Thus, even if the interface region INTERFACE is exposed to the etching atmosphere of the cell stack structure, the plurality of bit line structures BLS are not contaminated by metal contamination sources.

Referring to FIG. **11**O, a plurality of insulation spacers **172** covering both sidewalls of each of the plurality of bit line structures BLS in the cell array region CELL may be formed, and a portion of the substrate **110** and a portion of the device isolation layer **112** exposed through the plurality of insulation spacers **172** may be etched to form a plurality of recesses RC exposing the plurality of cell active regions A**1**. The plurality of recesses RC may each be communicatively connected to a buried contact hole BCH having a width that is defined by the pair of insulation spacers **172** between two adjacent bit lines structures BLS.

To form the plurality of insulation spacers **172** and the plurality of recesses RC, a spacer insulating layer covering the bit line structures BLS may be formed, and an operation of etching back of the spacer insulating layer and an operation of etching a portion of the substrate **110** and a portion of the device isolation layer **112** may be performed. Similar to the description referring to FIG. **11**N, as the etching operation of the layers including metal is performed while the undercut region UA**1** surrounding the cell array region CELL is filled with the buried pattern **136**P as described above with reference to FIG. **11**I, and the etching operation on the peripheral circuit stack structure is performed as described above with reference to FIG. **11**L, etching operations to form a plurality of insulation spacers **172** and a plurality of recesses RC may be performed while no contamination sources undesirably remain in the undercut region UA**1**. Thus, while performing the etching processes, even when the interface region INTERFACE is exposed to the etching atmosphere, the plurality of cell active regions A**1** exposed in the plurality of recesses RC are not contaminated by a metal contamination source.

Referring to FIG. **11**P, a buried conductive layer **182**, a metal silicide layer **184**, a conductive barrier layer **186**, and a conductive layer **188** may be formed, which are sequentially stacked in the plurality of buried contact holes BCH while filling the plurality of recesses RC between each of the plurality of bit line structures BLS. The conductive layer **182**, the metal silicide layer **184**, the conductive barrier layer **186**, and the conductive layer **188** may form a buried contact BC. Portions of the plurality of conductive layers **188** extending over an upper surface of the plurality of bit line structures BLS may be used as a plurality of landing pads, to which bottom electrodes of capacitors formed in a subsequent process may be connected, and may correspond to the plurality of landing pads LP described with reference to FIG. **10**.

A plurality of buried conductive layers **182** may be formed using a CVD process, a PVD process, or an epitaxial growth process. The plurality of buried conductive layers **182** may include an impurity-doped semiconductor material, a metal, a conductive metal nitride, a metal silicide, or a combination thereof.

The plurality of metal silicide layers **184** may include a cobalt silicide, a nickel silicide, or a manganese silicide. In an exemplary embodiment of the present inventive concept, the metal silicide layer **184** may be omitted.

The plurality of conductive barrier layers **186** may each be a Ti/TiN stack structures.

The plurality of conductive layers **188** may include doped polysilicon, a metal, a metal silicide, a conductive metal nitride, or a combination thereof. For example, the plurality of conductive layers **188** may include tungsten (W). While forming a plurality of conductive barrier layers **186** and a plurality of conductive layers **188** in the cell array region CELL, contact plugs that may be electrically connected to the peripheral circuit active region A**2** may be formed in the peripheral circuit region CORE/PERI. The plurality of conductive layers **188** may be electrically insulated from each other via an insulating layer **190** filling spaces around the conductive layers **188**.

In the cell array region CELL, a plurality of capacitor bottom electrodes that are electrically connectable to the plurality of conductive layers **188** may be formed on the insulating layer **190**.

FIGS. **12**A through **12**G are cross-sectional views illustrating a method of manufacturing an integrated circuit device, according to an exemplary embodiment of the present inventive concept. Similarly to FIGS. **11**A through **11**P, in FIGS. **12**A through **12**G, some exemplary configurations of the cell array region CELL, the peripheral circuit region CORE/PERI, and the interface region INTERFACE are illustrated. A method of manufacturing an integrated circuit device that further includes a local insulation pattern **220**P (see, e.g., FIG. **12**G) formed around an undercut region UA**2** will be described with reference to FIGS. **12**A through **12**G. In FIGS. **12**A through **12**G, reference numerals that are the same as those in FIGS. **11**A through **11**P denote like elements, and thus duplicative descriptions may be omitted below.

Referring to FIG. **12**A, by using substantially the same method as described with reference to FIG. **11**A, a plurality of device isolation trenches **112**T may be formed in the substrate **110**, and then a plurality of device isolation layers **112** filling the device isolation trenches **112**T may be formed. Then, a mask insulation pattern **220** covering a plurality of cell active regions A**1**, a plurality of peripheral circuit active regions A**2**, and the plurality of device isolation layers **112** may be formed above the substrate **10**. A plurality of openings **220**H exposing an area where a plurality of word line trenches **120**T are to be formed may be formed in the mask insulation pattern **220** in the cell array region CELL. By using the mask insulation pattern **220** as an etching mask, the substrate **110** and the device isolation layer **112** that are exposed through the plurality of openings **220**H may be etched to form a plurality of word line trenches **120**T. The mask insulation pattern **220** may include a silicon oxide layer, a silicon nitride layer, or a combination thereof.

Referring to FIG. **12**B, the gate dielectric layer **122**, the word line **124**, and the buried insulating layer **126** may be sequentially formed in each of the plurality of word line trenches **120**T in the cell array region CELL, and other layers remaining on the substrate **110** may be removed. Due to the plurality of openings **220**H formed in the mask insulation pattern **220**, the mask insulation pattern **220** is formed of portions having a relatively small width in the cell array region CELL, and thus, while removing the other layers on the substrate **110**, portions of the mask insulation pattern **220** above the substrate **110** may be removed relatively quickly due to three-dimensional etching effects. In the peripheral circuit region CORE/PERI and a portion of the interface region INTERFACE adjacent thereto, the mask insulation pattern **220** has a relatively large width unlike in the cell array region CELL, and thus, a rate of removal of the mask insulation pattern **220** may be relatively slow. Thus, when the mask insulation pattern **220** is completely removed in the cell array region CELL to expose an upper surface of the substrate **110**, in the peripheral circuit region CORE/PERI and a portion of the interface region INTERFACE adjacent thereto, the mask insulation pattern **220** of a reduced thickness may remain.

Referring to FIG. **12**C, in a similar manner as described with reference to FIG. **11**B, an insulating layer **130** may be formed above the substrate **110** in the cell array region CELL, the interface region INTERFACE, and the peripheral circuit region CORE/PERI. The insulating layer **130** may include a first insulating layer **132** and a second insulating layer **134**. In the peripheral circuit region CORE/PERI and a portion of the interface region INTERFACE adjacent thereto, the insulating layer **130** may cover the mask insulation pattern **220**.

Referring to FIG. **12**D, in a similar manner as described with reference to FIG. **11**C, a portion of the insulating layer **130** may be removed to form the insulation pattern **130**P, and a portion of the mask insulation pattern **220** exposed through the insulation pattern **130**P may be removed to form a local insulation pattern **220**P to expose the peripheral circuit active region A**2** in the peripheral circuit region CORE/PERI.

Referring to FIG. **12**E, in a similar manner as described with reference to FIG. **11**D, an exposed surface of the peripheral circuit active region A**2** in the peripheral circuit region CORE/PERI may be cleaned to remove an undesired natural oxide layer on the peripheral circuit active region A**2**. While performing a cleaning operation to remove a natural oxide layer, a portion of the interface region INTERFACE and the peripheral circuit region CORE/PERI may also be exposed to the cleaning atmosphere, and thus, portions of the device isolation layer **112** in the interface region INTERFACE and the peripheral circuit region CORE/PERI that include an oxide may be partially consumed by the cleaning atmosphere, such that a recess R is formed in each upper portion of the first insulation liner **112**A and the buried insulating layer **112**C in the peripheral circuit region CORE/PERI. In addition, a portion of the buried insulating layer **112**C forming the device isolation layer **112** under the terminal portion **134**T of the second insulation pattern **134**P in the interface region INTERFACE, a portion of the local insulation pattern **220**P, and a portion of the first insulation pattern **132**P may be consumed by the cleaning atmosphere so as to form the undercut region UA**2** under the terminal portion **134**T of the second insulation pattern **134**P.

Referring to FIG. **12**F, in a similar manner as described with reference to FIGS. **11**E through **11**G, the buried mask layer **136** (see, e.g., FIG. **11**E) may be formed on the substrate **110**, and, by using a selective epitaxial growth process, the semiconductor layer **138** may be formed from a surface of the peripheral circuit active region A**2** that is exposed through the hole **136**H of the buried mask layer **136**. Then, the buried mask layer **136** may be isotropically etched by leaving only a portion of the buried mask layer **136** that fills the undercut region UA**2**. The portion of the buried mask layer **136** filling the undercut region UA**2** may be left as a buried pattern **236**P.

The buried pattern **236**P may be extended along a periphery of the cell array region CELL such that the buried pattern **236**P has a closed loop shape surrounding the cell array region CELL (e.g., when viewed in a plan view). In an exemplary embodiment of the present inventive concept, a seam portion **236**S may be left in the buried pattern **236**P. In an exemplary embodiment of the present inventive concept, the seam portion **236**S need not be left in the buried pattern **236**P. In an exemplary embodiment of the present inventive concept, an air gap having a similar shape as the air gap AG**1** described with reference to FIG. **4** or the air gap AG**2** described with reference to FIG. **7** may be left in a portion of the buried pattern **236**P that is adjacent to the seam portion **236**S. Similarly to the buried pattern **136**P illustrated in FIG. **11**G, the buried pattern **236**P may include the convex surface CVX facing the cell array region CELL and a concave surface CCV facing the peripheral circuit region CORE/PERIL

In the interface region INTERFACE, as the undercut region UA**2** formed between the device isolation layer **112** and the second insulation pattern **134**P is filled with the buried pattern **236**P, while a subsequent process is being performed, undesired contamination sources, particularly, impurities such as metal particles, may be prevented from penetrating into or remaining in the undercut region UA**2**.

Referring to FIG. **12**G, the processes described with reference to FIGS. **11**H through **11**P may be performed on a resultant product of the embodiment of FIG. **12**F to form a plurality of bit line structures BLS and a plurality of direct contacts DC in the cell array region CELL, and a peripheral gate structure PGS in the peripheral circuit region CORE/PERI.

While the present inventive concept has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the present inventive concept.

What is claimed is:

1. A method of manufacturing an integrated circuit device, the method comprising:

forming a trench in a substrate;

forming a device isolation layer filling the trench;

forming an insulation pattern on the device isolation layer so as to cover a first portion of a top surface of the device isolation layer;

forming an undercut area under a terminal portion of the insulation pattern by removing a portion of the device isolation layer from a second portion of the top surface of the device isolation layer;

forming a buried pattern filling the undercut area; and

forming an interlayer insulating layer covering each of the device isolation layer, the insulation pattern, and the buried pattern,

wherein forming the insulation pattern includes forming a first insulation layer contacting the device isolation layer and forming a second insulation layer on top of the first insulation layer, and

wherein the undercut area is undercut with respect to both the first insulation layer and the second insulation layer, the buried pattern is disposed below both the first insulation layer and the second insulation layer, and a top-most surface of the buried pattern is disposed below the second insulation layer.

2. The method of claim **1**, wherein the forming of the buried pattern comprises forming a seam portion in the buried pattern, the seam portion being spaced apart from the device isolation layer and the insulation pattern.

3. The method of claim **1**, wherein in the forming of the buried pattern, the buried pattern is formed to have a closed loop shape.

4. The method of claim **1**, wherein the first insulating layer and the second insulating layer are formed including different insulating materials from each other, and portions of the first insulating layer and the second insulating layer are removed to form the insulation pattern.

5. The method of claim **1**, wherein the forming of the buried pattern comprises forming a buried layer burying the undercut area to have a thickness sufficient to fill the undercut area, the buried layer having a seam portion extending toward an entrance of the undercut area.

6. The method of claim **1**, wherein the forming, of the buried pattern comprises forming an air gap within the undercut area, the air gap surrounded by the buried pattern.

7. The method of claim **1**, wherein the buried pattern includes a silicon oxide, a silicon nitride, a silicon oxynitride (SiON), a silicon oxynitride (SiOCN), polysilicon, or a combination thereof.

8. A method of manufacturing an integrated circuit device, the method comprising:

forming a trench in a substrate;

forming a device isolation layer filling the trench;

forming a mask insulation pattern covering at least a portion of the device isolation layer;

forming an insulation layer on the device isolation layer with the mask insulation pattern interposed between the device isolation layer and the insulation layer;

forming am insulation pattern by removing a portion of the insulating layer to expose a portion of the mask insulation pattern overlying the device isolation layer;

forming a local insulation pattern by removing a portion of the mask insulation pattern exposed through the insulation pattern;

forming an undercut area under a terminal portion of the insulation pattern by removing a portion of the device isolation layer and a portion of the local insulation pattern to remain another portion of the local insulation pattern positioned under the insulation pattern, the another portion of the local insulation pattern exposed through the undercut area;

forming a buried pattern filling the undercut area, the buried pattern being in contact with the another portion of the local insulation within the undercut area; and

forming an interlayer insulating layer covering each of the device isolation layer, the insulation pattern, and the buried pattern.

9. The method of claim **8**, wherein the forming of the insulation layer comprises forming the insulation layer to have a convex surface overlying the device isolation layer, the convex surface being farther from the substrate than atop surface of the device isolation layer.

10. The method of claim **9**, wherein in the forming of the local insulation pattern, the local insulation pattern is in contact with the convex surface of the buried pattern.

11. The method of claim 8, wherein the forming of the insulation layer comprises:

forming a first insulating layer on the mask insulation pattern, the first insulating layer including a first insulating material; and

forming a second insulating layer on the first insulating layer, the second insulating layer including a second insulating material different form the first insulating material,

wherein in the forming of the buried pattern, the buried pattern is formed to be in contact with the first insulating layer and the second insulating layer.

12. The method of claim 11, wherein the first insulating layer includes an oxide layer, and the second insulating layer includes a nitride layer.

13. The method of claim 8, wherein the forming of the buried pattern comprises forming a buried layer burying the undercut area to have a thickness sufficient to fill the undercut area, the buried layer having a seam portion extending toward an entrance of the undercut area.

14. A method of manufacturing an integrated circuit device, the method comprising:

providing a substrate having a cell array region including a cell active region, a peripheral circuit region including a peripheral circuit active region separated from cell array region along a direction parallel to an upper surface of the substrate, and an interface region including a device isolation layer defining a portion of the cell active region and a portion of the peripheral circuit active region and positioned between the cell array region and the peripheral circuit region;

forming an insulation pattern extending from the cell array region to an upper portion of the device isolation layer so as to cover an upper surface of the cell active region and at least a portion of the device isolation layer;

forming an undercut area under the insulation pattern by removing a portion of the device isolation layer in the interface region;

forming a buried pattern substantially filling the undercut area; and

forming an insulating layer covering the insulation pattern, the buried pattern, and the device isolation layer in the interface region,

wherein the forming of the buried pattern comprises:

forming a buried mask layer that fills the undercut area and extends into the interface region so as to cover the insulation pattern and the device isolation layer, wherein the buried mask layer has a hole exposing an upper surface of the peripheral circuit active region;

forming a compound semiconductor layer covering the peripheral circuit active region exposed through the hole of the buried mask layer; and

isotropically etching the buried mask layer such that only a portion of the buried mask layer filling the undercut area remains.

15. The method of claim 14, wherein the forming of the insulation pattern comprises forming a first insulation pattern covering an upper surface of the cell array region and a second insulation pattern on an upper surface of the first insulation pattern, wherein the undercut area is undercut with respect to both the first insulation pattern and the second insulation pattern,

wherein the first insulation pattern covers at least a portion of the interface region adjacent to the cell array region,

wherein the first insulation pattern and the second insulation pattern include different materials from each other, and

wherein the forming of the undercut area comprises removing a portion of the device isolation layer and a portion of the first insulation pattern from a lower portion of a terminal portion of the second insulation pattern.

16. The method of claim 15, wherein the second insulation pattern and the device isolation layer each include a same material.

17. The method of claim 14, wherein in the forming of the undercut area, the undercut area is formed to be defined by a convex surface extending toward the cell array region and to have an entrance facing the peripheral circuit region along the direction parallel to the upper surface of the substrate.

18. The method of claim 14, wherein the forming of the buried pattern comprises forming a buried layer burying the undercut area to have a thickness sufficient to fill the undercut area, the buried layer having a seam portion extending toward an entrance of the undercut area.

19. The method of claim 14, wherein the forming of the buried pattern comprises forming an air gap within the undercut area, the air gap surrounded by the buried pattern.

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