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Biswas et al.

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(54) POWER GRID STRUCTURES AND METHOD OF FORMING THE SAME

(71) Applicant: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**, Hsinchu (TW)

(72) Inventors: **Hiranmay Biswas**, Hsinchu (TW); **Chi-Yeh Yu**, Hsinchu (TW); **Chung-Hsing Wang**, Baoshan Township (TW); **Kuo-Nan Yang**, Hsinchu (TW); **Stefan Rusu**, Sunnyvale, CA (US); **Chin-Shen Lin**, Taipei (TW)

(73) Assignee: **TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.**, Hsinchu (TW)

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Related U.S. Application Data

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(51) **Int. Cl.**

H01L 23/528	(2006.01)
H01L 21/768	(2006.01)

(Continued)

(52) **U.S. Cl.**

CPC ***H01L 23/5286*** (2013.01); ***H01L 21/76816*** (2013.01); ***H01L 21/76877*** (2013.01);

(Continued)

(58) **Field of Classification Search**

CPC H01L 23/5286; H01L 21/76816; H01L 21/6877

(Continued)

(56) **References Cited**

U.S. PATENT DOCUMENTS

7,260,442	B2	8/2007	Hwang et al.
8,421,205	B2	4/2013	Yang

(Continued)

FOREIGN PATENT DOCUMENTS

JP	9-293843	11/1997
JP	2004-186671	7/2004
JP	2015-15502	1/2015

OTHER PUBLICATIONS

Office Action dated Jun. 4, 2018 from corresponding application No. TW 106141047.

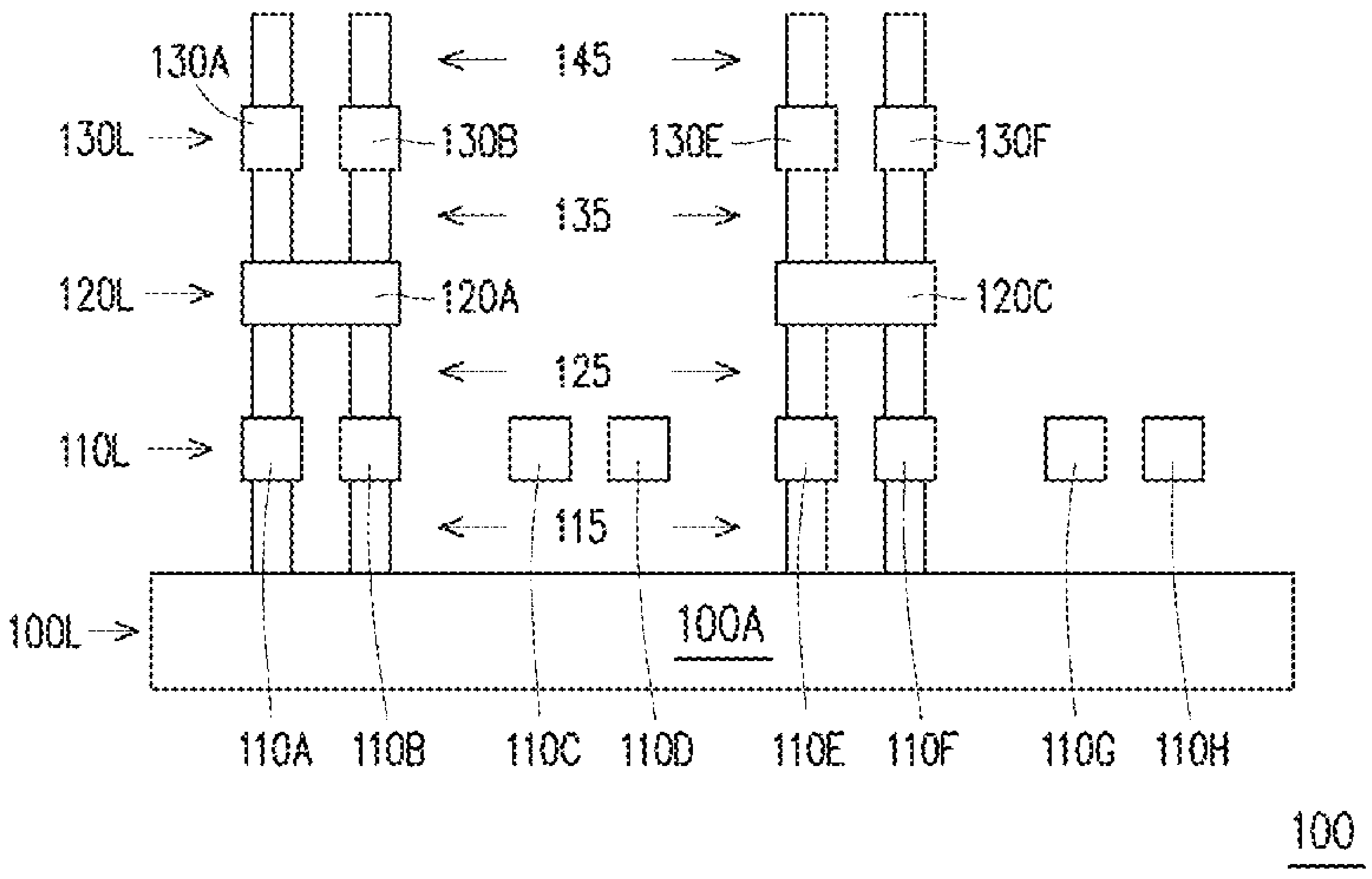
(Continued)

Primary Examiner — Thao X Le
Assistant Examiner — Xia L Cross
(74) *Attorney, Agent, or Firm* — Hauptman Ham, LLP

(57) **ABSTRACT**

An integrated circuit (IC) structure includes a power rail oriented in a power rail direction and first metal segments above the power rail, oriented in a first metal level direction perpendicular to the power rail direction. First vias positioned between the power rail and the first metal segments are positioned at locations where first metal segments overlap the power rail. A second metal segment is positioned above the first metal segments, overlaps the power rail, and is oriented in the power rail direction. Second vias are positioned above the first vias between the first metal segments and the second metal segments, and a power strap is positioned above the second metal segment. The power strap is electrically connected to the power rail, each first metal segment of the plurality of first metal segments has a

(Continued)



minimum width, and the power strap has a width greater than a minimum width.

20 Claims, 26 Drawing Sheets

(51) **Int. Cl.**

H01L 23/522	(2006.01)
G06F 30/394	(2020.01)

(52) **U.S. Cl.**
CPC ***H01L 23/5226*** (2013.01); ***H01L 23/5283*** (2013.01); *G06F 30/394* (2020.01)

(58) **Field of Classification Search**
USPC 257/774
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

8,661,389	B2	2/2014	Chern et al.	
8,698,205	B2	4/2014	Tzeng et al.	
8,826,212	B2	9/2014	Yeh et al.	
8,836,141	B2	9/2014	Chi et al.	
8,875,076	B2	10/2014	Lin et al.	
9,147,029	B2	9/2015	Ke et al.	
9,256,709	B2	2/2016	Yu et al.	
2004/0094820	A1	5/2004	Nishikawa et al.	
2008/0111158	A1	5/2008	Sherlekar et al.	
2013/0154128	A1*	6/2013	Wang	H01L 23/5286 257/786
2014/0040838	A1	2/2014	Liu et al.	
2014/0239406	A1	8/2014	Tsuda et al.	
2014/0264924	A1	9/2014	Yu et al.	
2014/0282289	A1	9/2014	Hsu et al.	
2015/0278429	A1	10/2015	Chang	
2015/0279453	A1	10/2015	Fujiwara et al.	
2015/0318241	A1	11/2015	Chang et al.	
2015/0347659	A1	12/2015	Chiang et al.	
2015/0357279	A1	12/2015	Fujiwara et al.	
2016/0012169	A1	1/2016	Chiang et al.	
2016/0211212	A1*	7/2016	Chao	H01L 23/5226

OTHER PUBLICATIONS

Office Action dated Nov. 14, 2018 from corresponding application No. KR 10-2017-0155642.

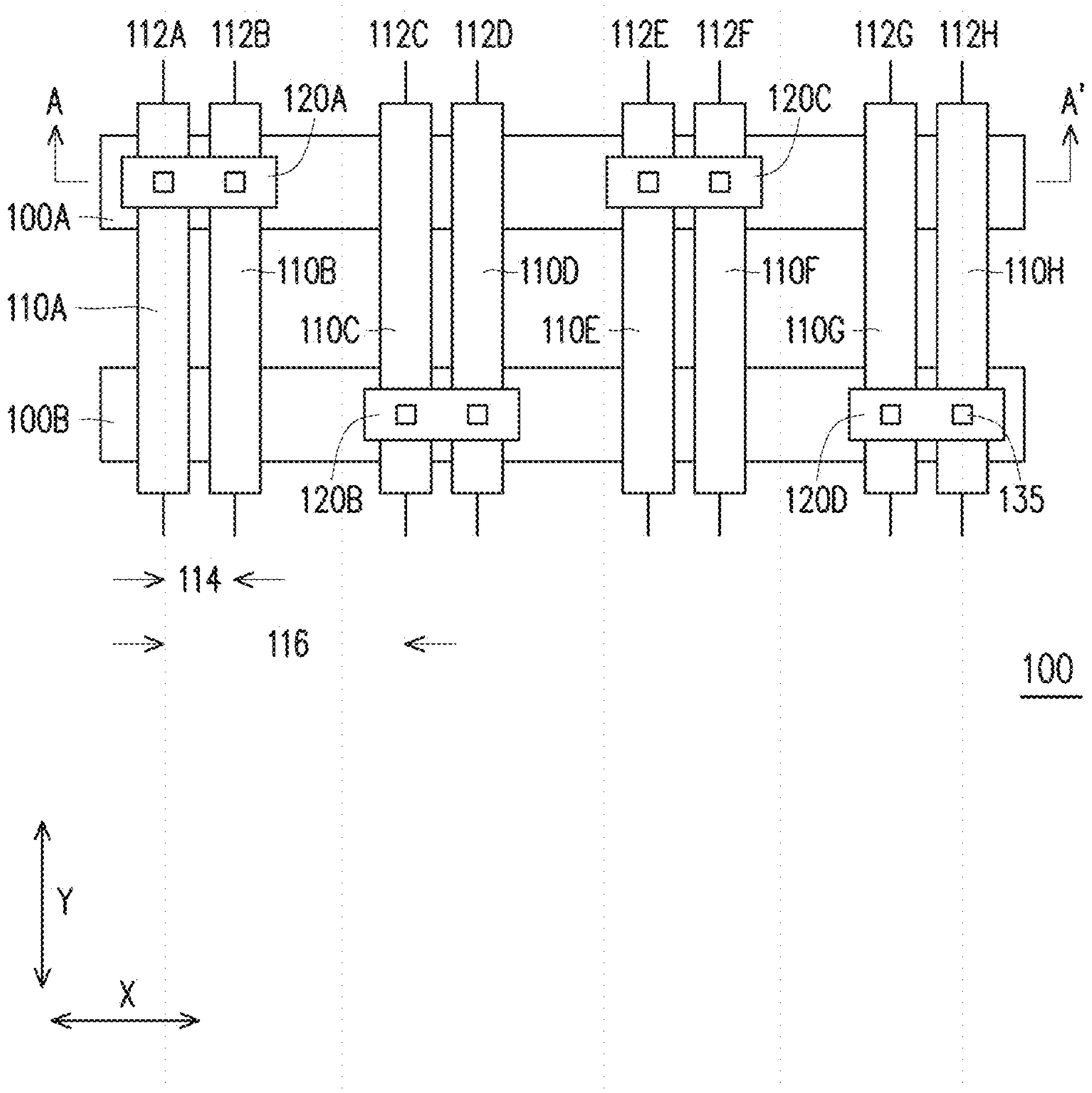
De Orio, Roberto Lacerda. "Electromigration Modeling and Simulation." Electromigration Modeling and Simulation, Vienna University of Technology, Faculty of Electrical Engineering and Information Technology, Aug. 31, 2015, http://www.iue.tuwien.ac.at/phd/orio/node21.html, Internet Archive https://web.archive.org/web/20150831223409/http://www.iue.tuwien.ac.at/phd/orio/node26.html.

"Blech length," University of Cambridge, Dissemination of IT for the Promotion of Materials Science (DoITPoMS), Oct. 22, 2015, https://www.doitpoms.ac.uk/tlplib/electromigration/blech_length.php, Internet Archive https://web.archive.org/web/20151022042201/https://www.doitpoms.ac.uk/tlplib/electromigration/blech_length.php#expand.

"What is Electromigration?," May 26, 2013, https://blog.intgckts.com/what-is-electromigration/.

J.R. Lloyd, "Electromigration for Designers: An Introduction for the Non-Specialist," Apr. 12, 2002, https://www.eetimes.com/electromigration-for-designers-an-introduction-for-the-non-specialist/#.

* cited by examiner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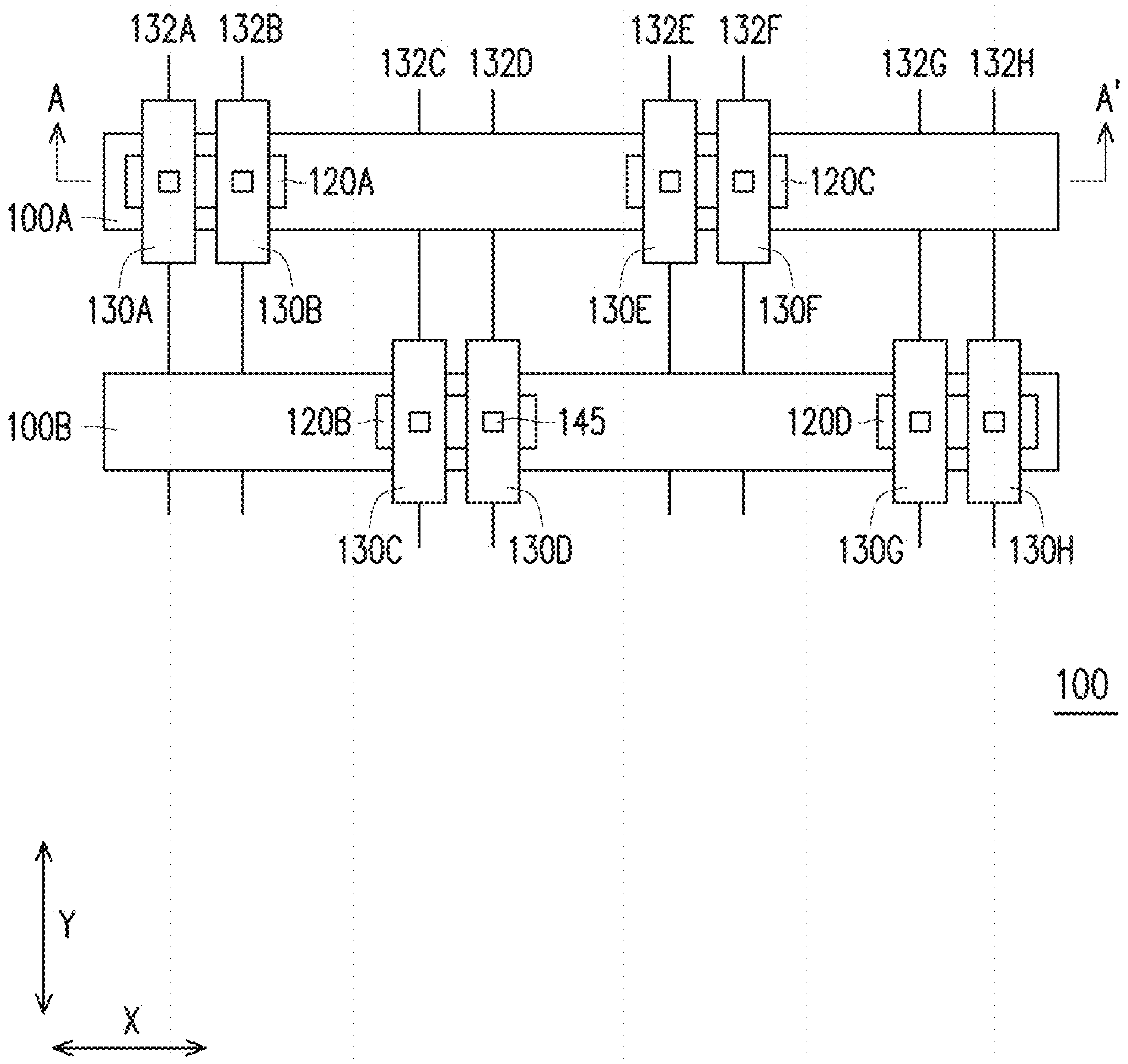
112B
112C
112D
112E
112F
112G
112H
A
120A
120C
A'
100A
110A
110B
110C
110D
110E
110F
110G
110H
100B
120B
120D
135
114
116
100
Y
X

FIG. 1A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132B
132C
132D
132E
132F
132G
132H
A
A'
120A
120C
100A
130A
130B
130E
130F
100B
120B
145
120D
130C
130D
130G
130H
100
Y
X

FIG. 1B

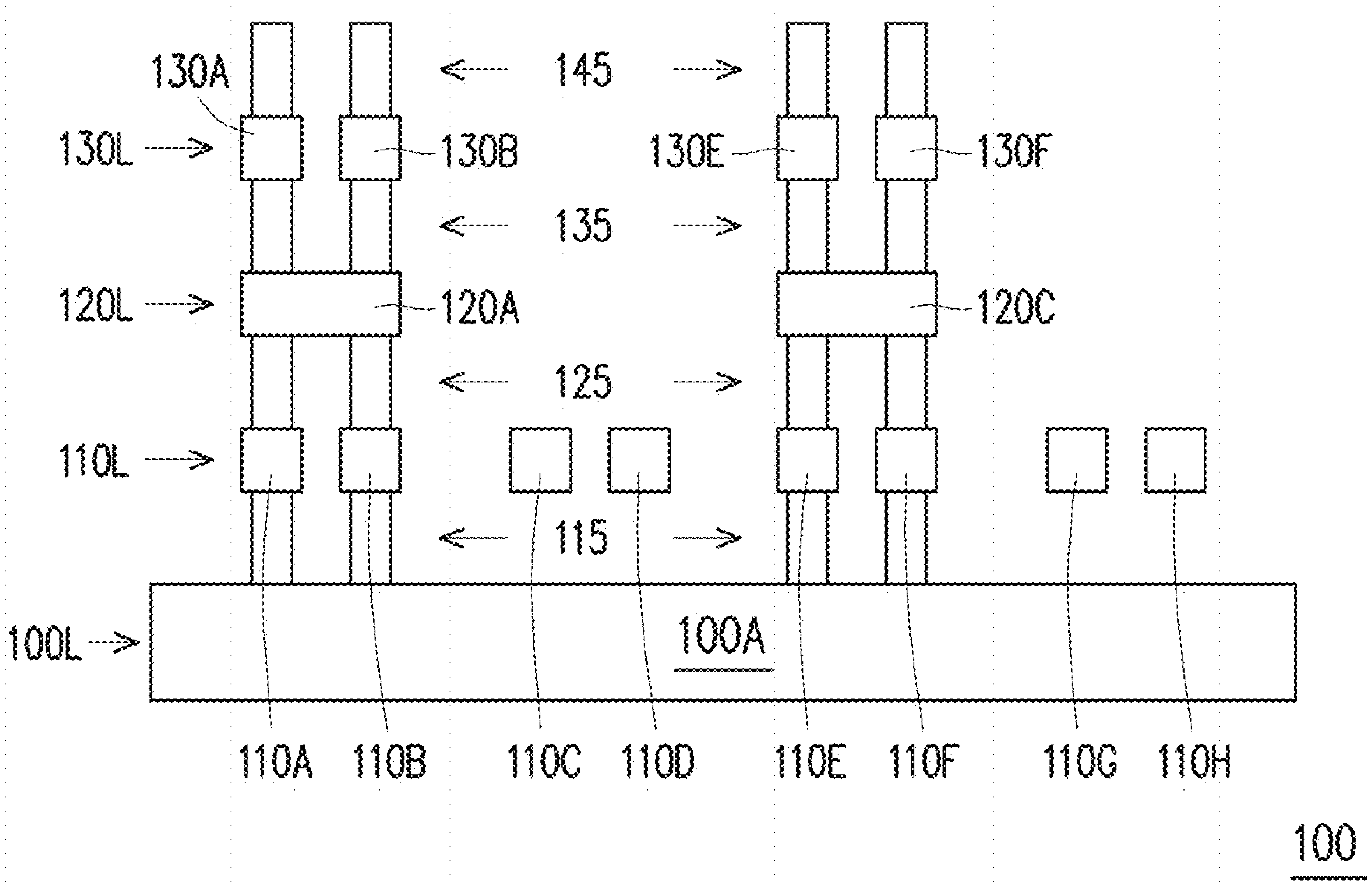
130A
130L
130B
145
130E
130F
135
120L
120A
120C
125
110L
115
100L
100A
110A
110B
110C
110D
110E
110F
110G
110H
100

FIG. 1C

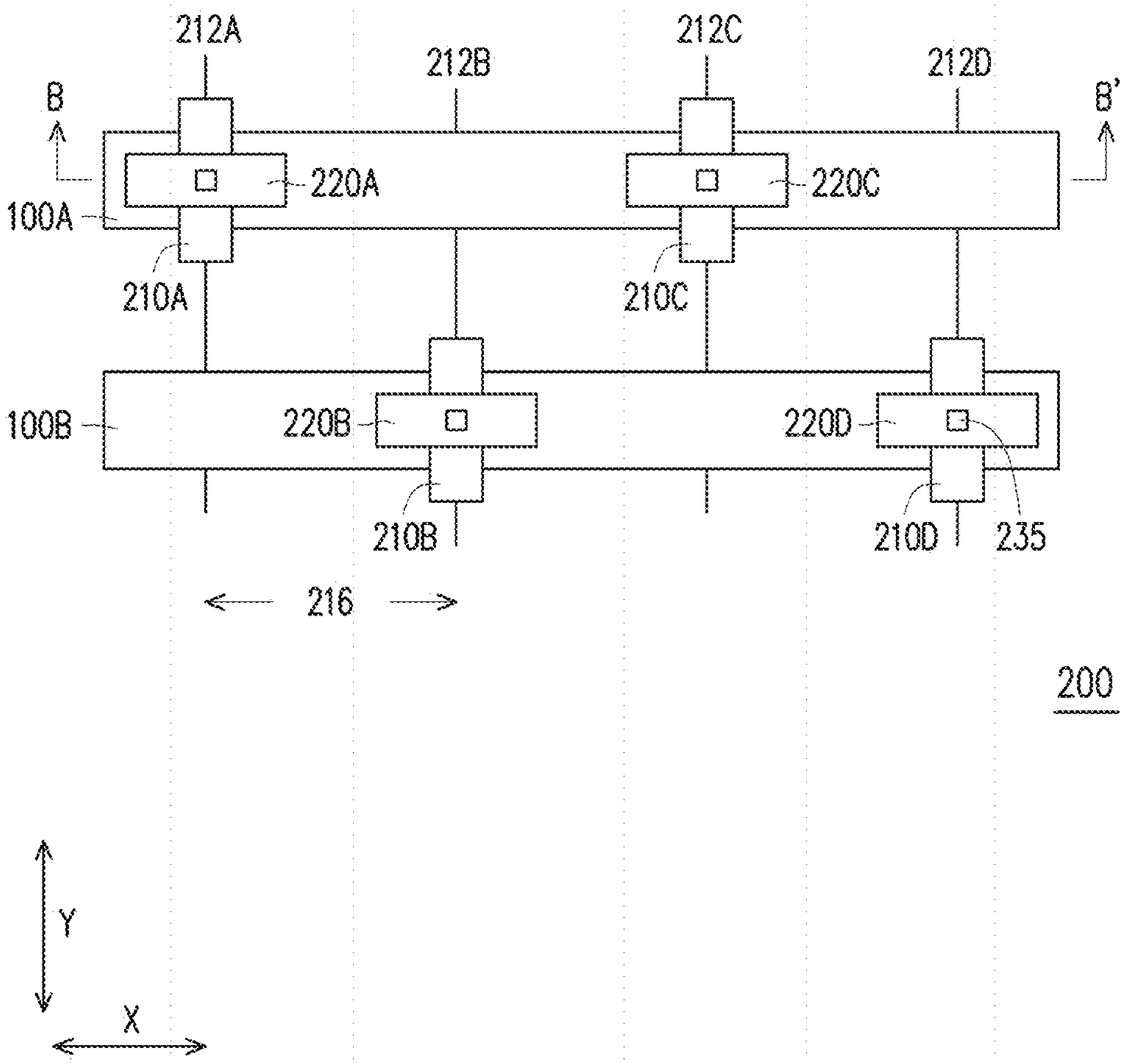
212A
212B
212C
212D
B
B'
220A
220C
100A
210A
210C
100B
220B
220D
210B
210D
235
216
200
Y
X

FIG. 2A

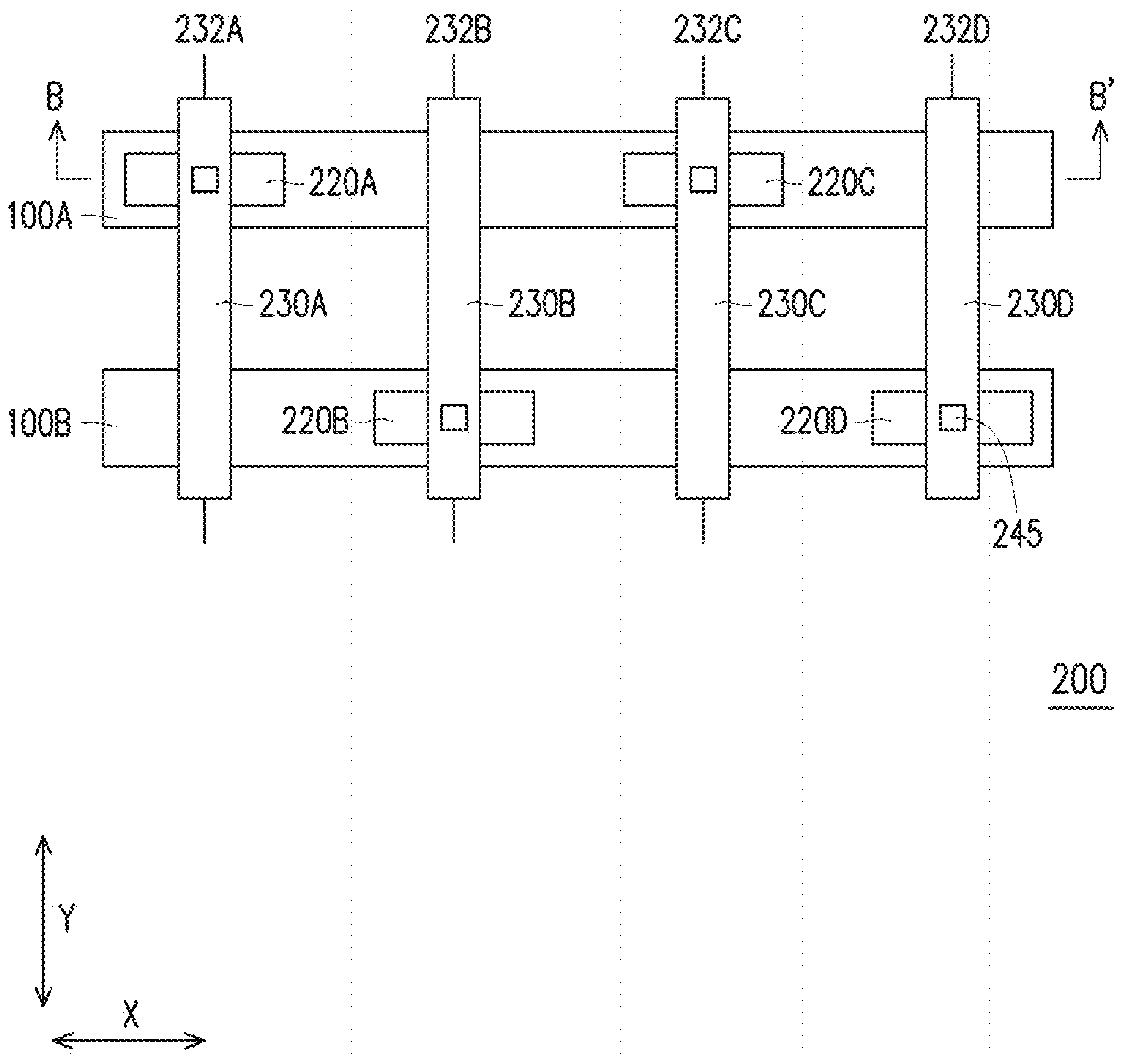
232A
232B
232C
232D
B
B'
220A
220C
100A
230A
230B
230C
230D
100B
220B
220D
245
200
Y
X

FIG. 2B

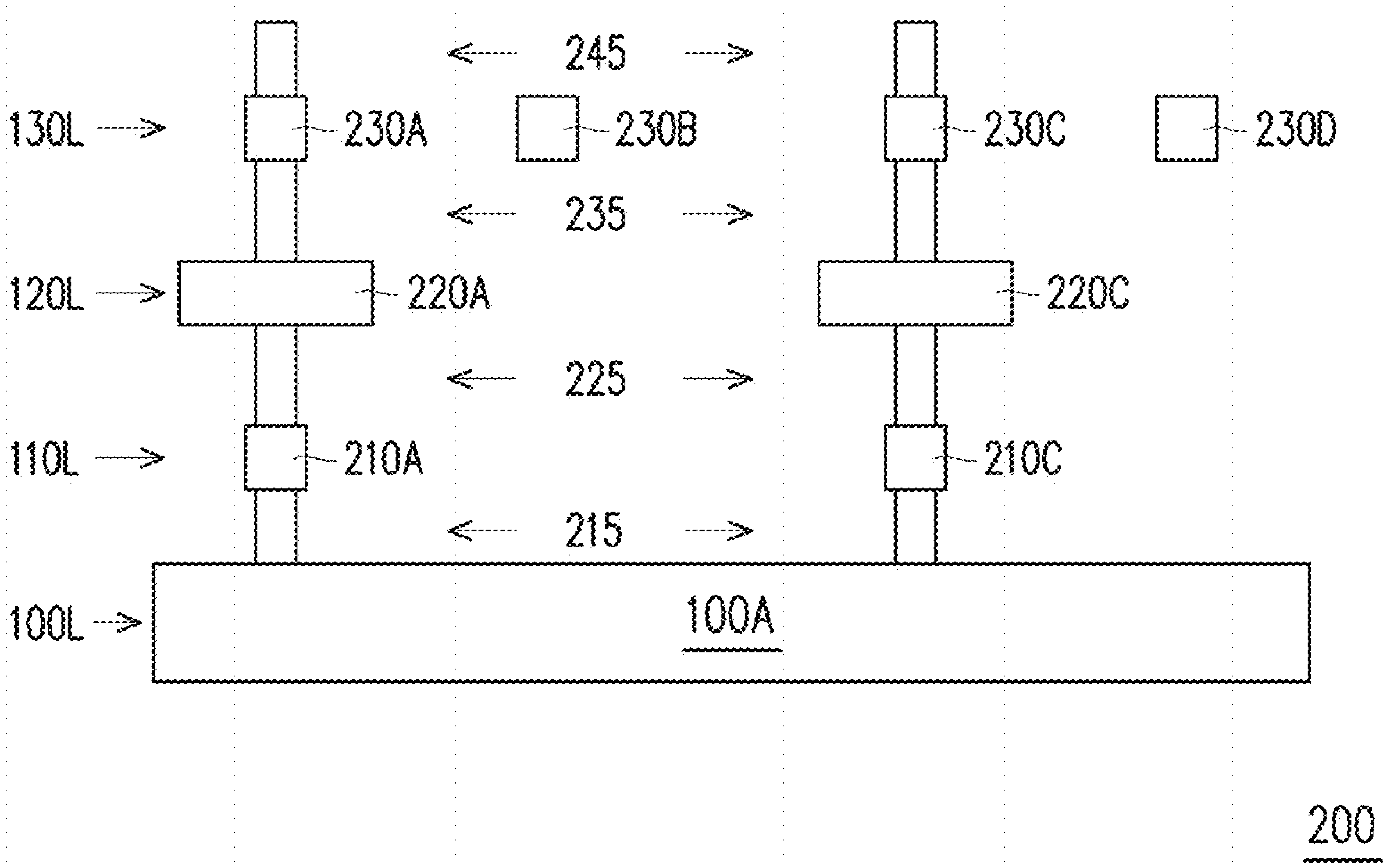
245
130L
230A
230B
230C
230D
235
120L
220A
220C
225
110L
210A
210C
215
100L
100A
200

FIG. 2C

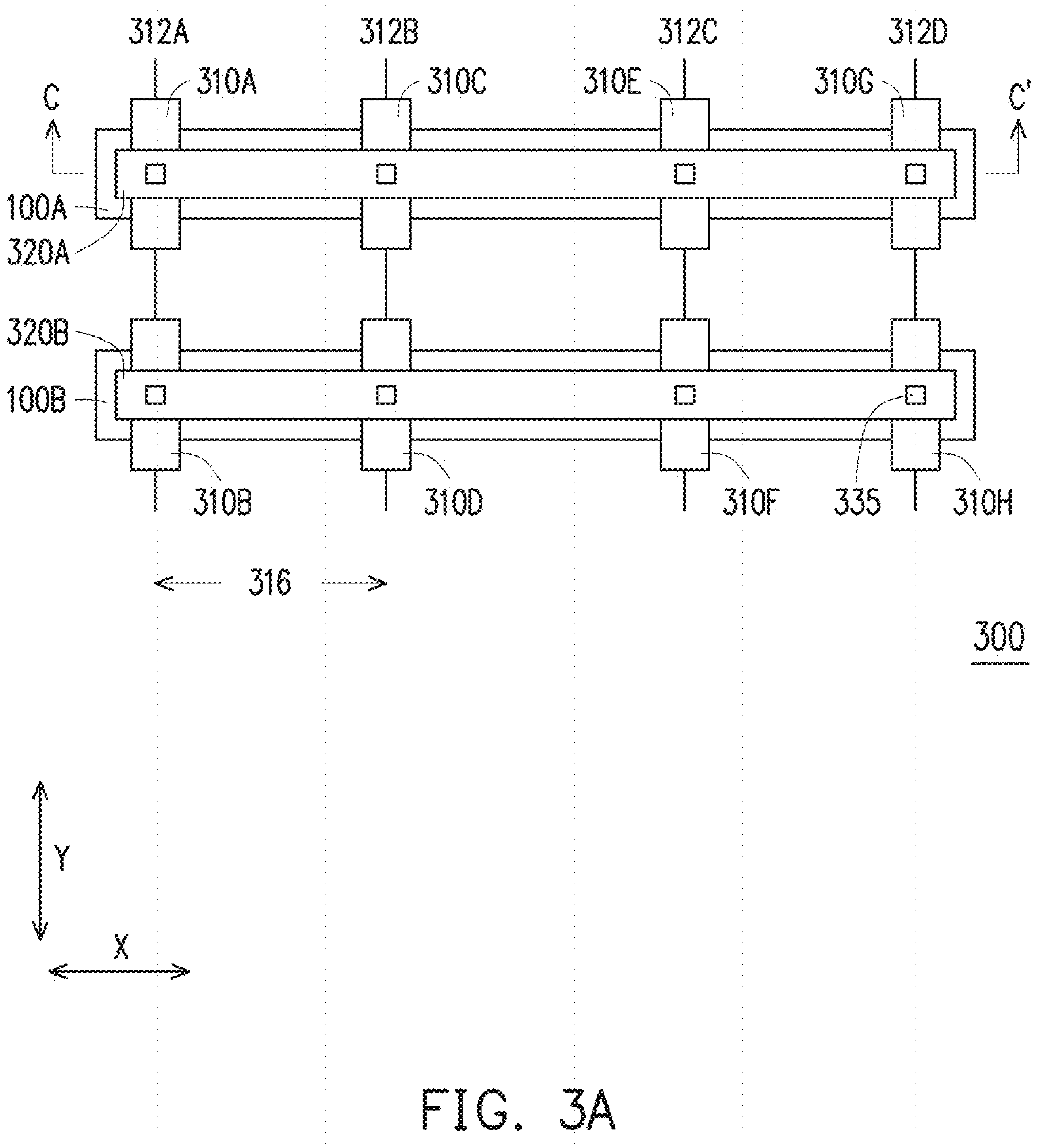
312A
312B
312C
312D
310A
310C
310E
310G
C
C'
100A
320A
320B
100B
310B
310D
310F
335
310H
316
300
Y
X

FIG. 3A

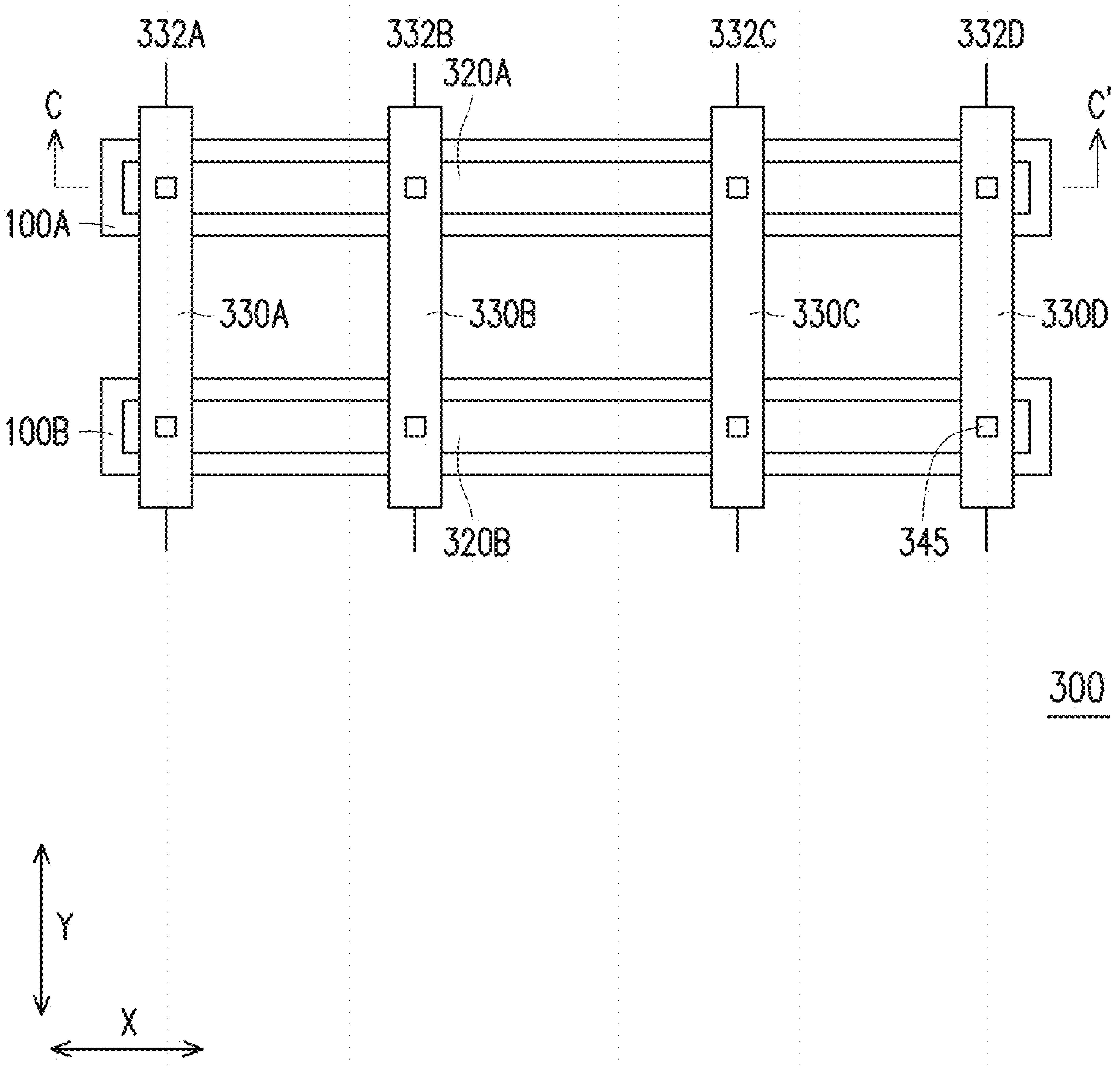
332A
332B
320A
332C
332D
C
C'
100A
330A
330B
330C
330D
100B
320B
345
300
Y
X

FIG. 3B

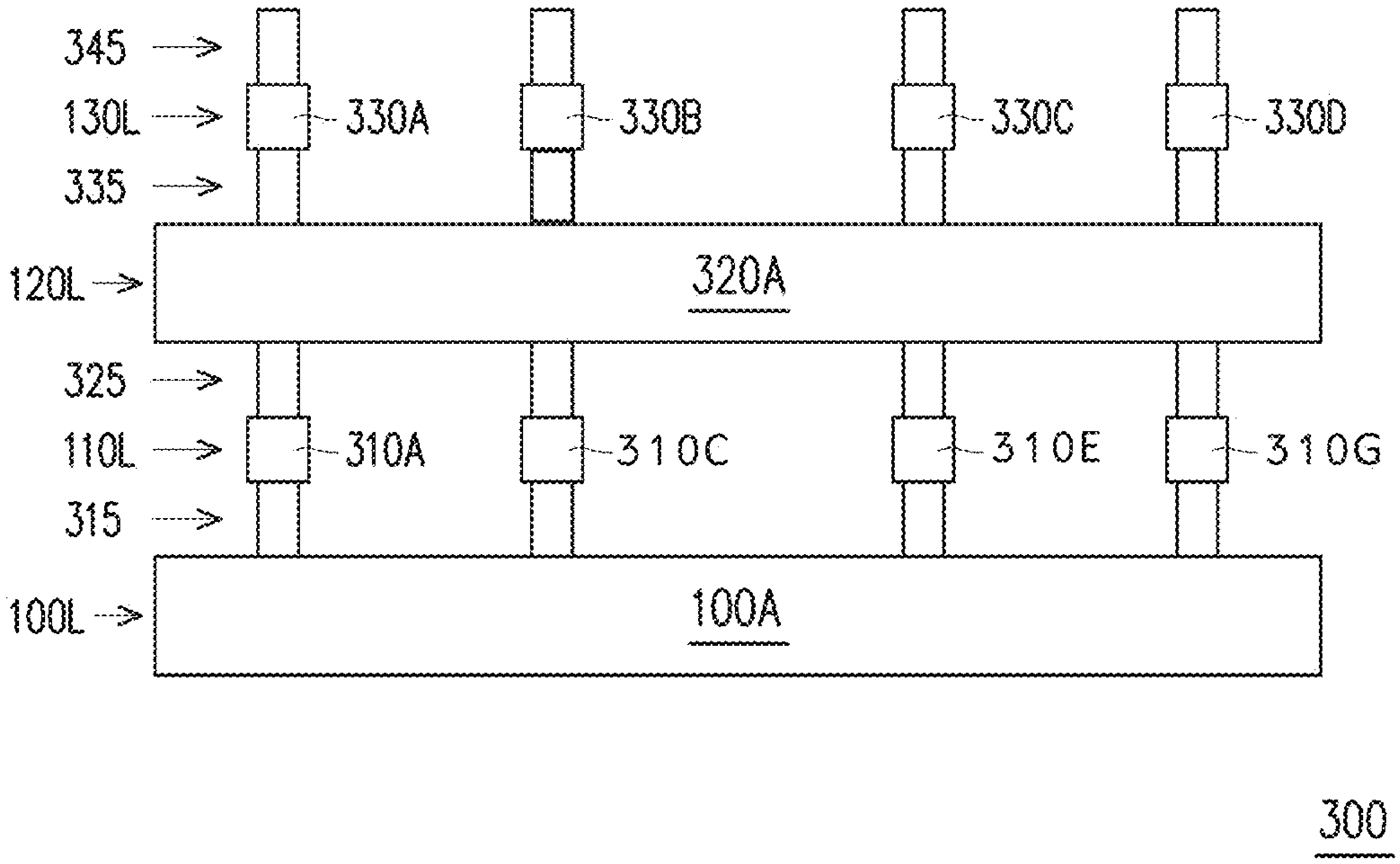
345
130L
335
120L
325
110L
315
100L
330A
330B
330C
330D
320A
310A
310C
310E
310G
100A
300

FIG. 3C

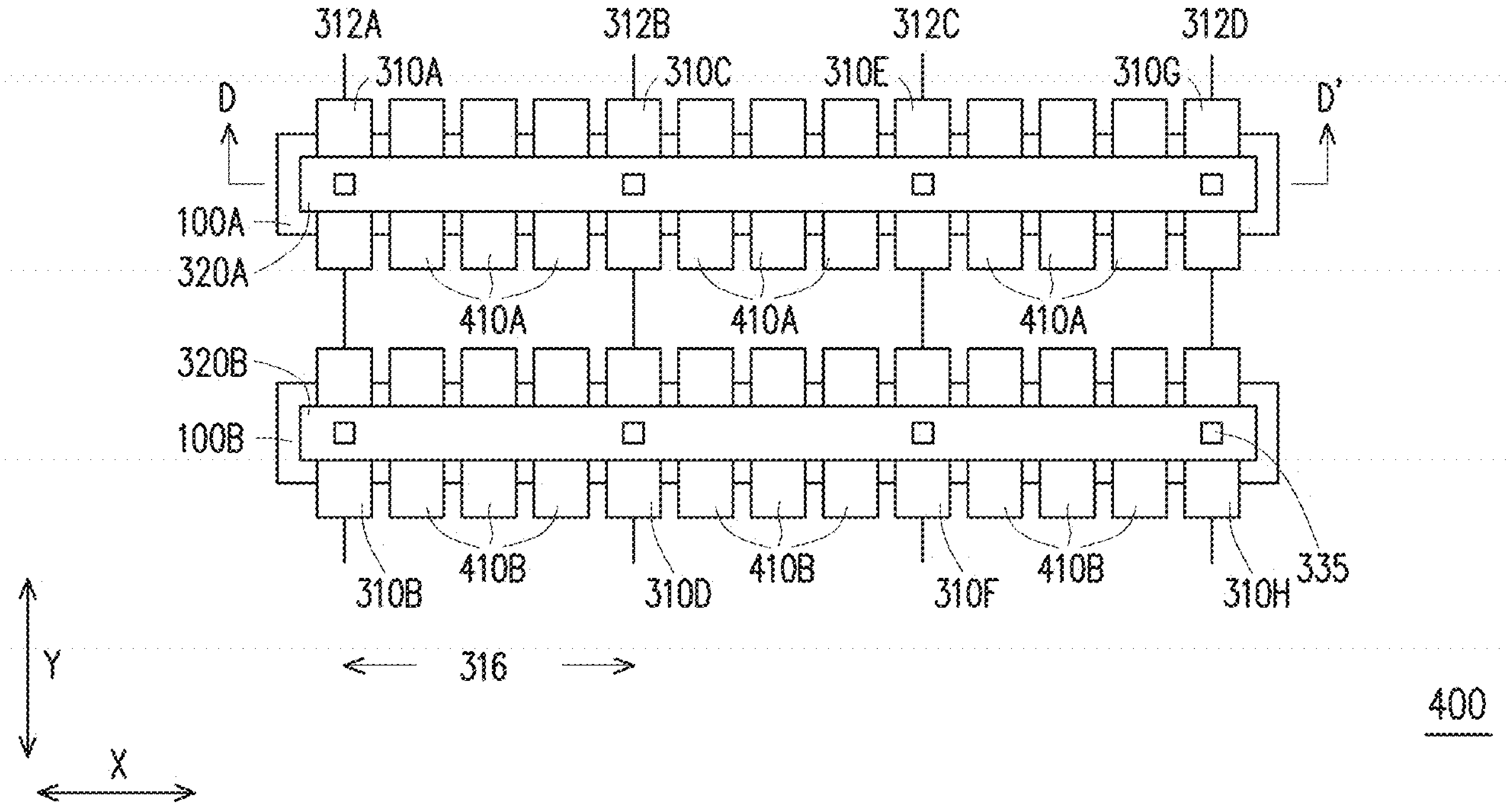
312A
312B
312C
312D
310A
310C
310E
310G
D
D'
100A
320A
410A
410A
410A
320B
100B
410B
410B
410B
310B
310D
310F
310H
335
Y
X
316
400

FIG. 4A

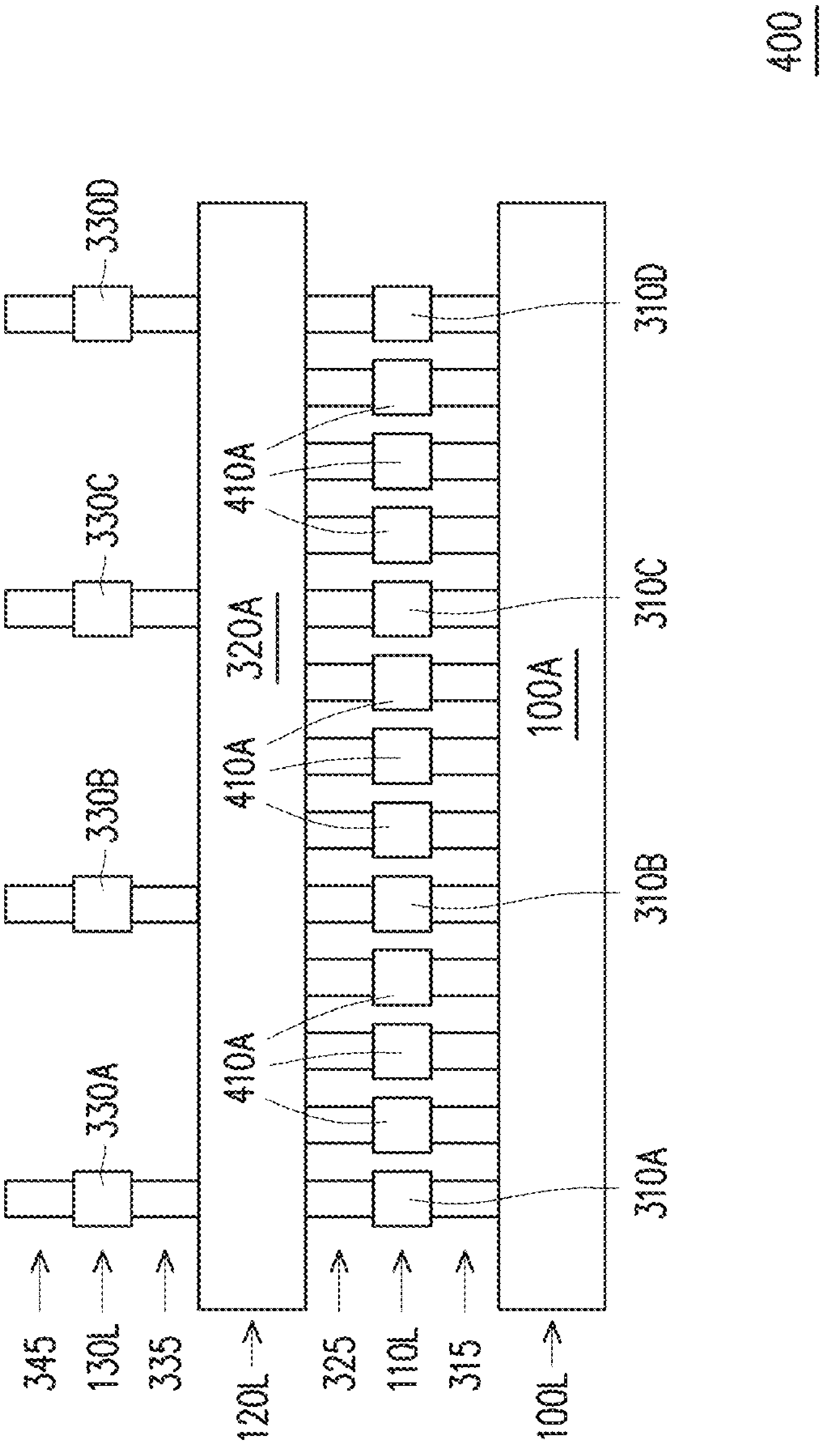
400
345
130L
335
120L
325
110L
315
100L
330A
330B
330C
330D
320A
410A
410A
410A
310A
310B
310C
310D
100A

FIG. 4B

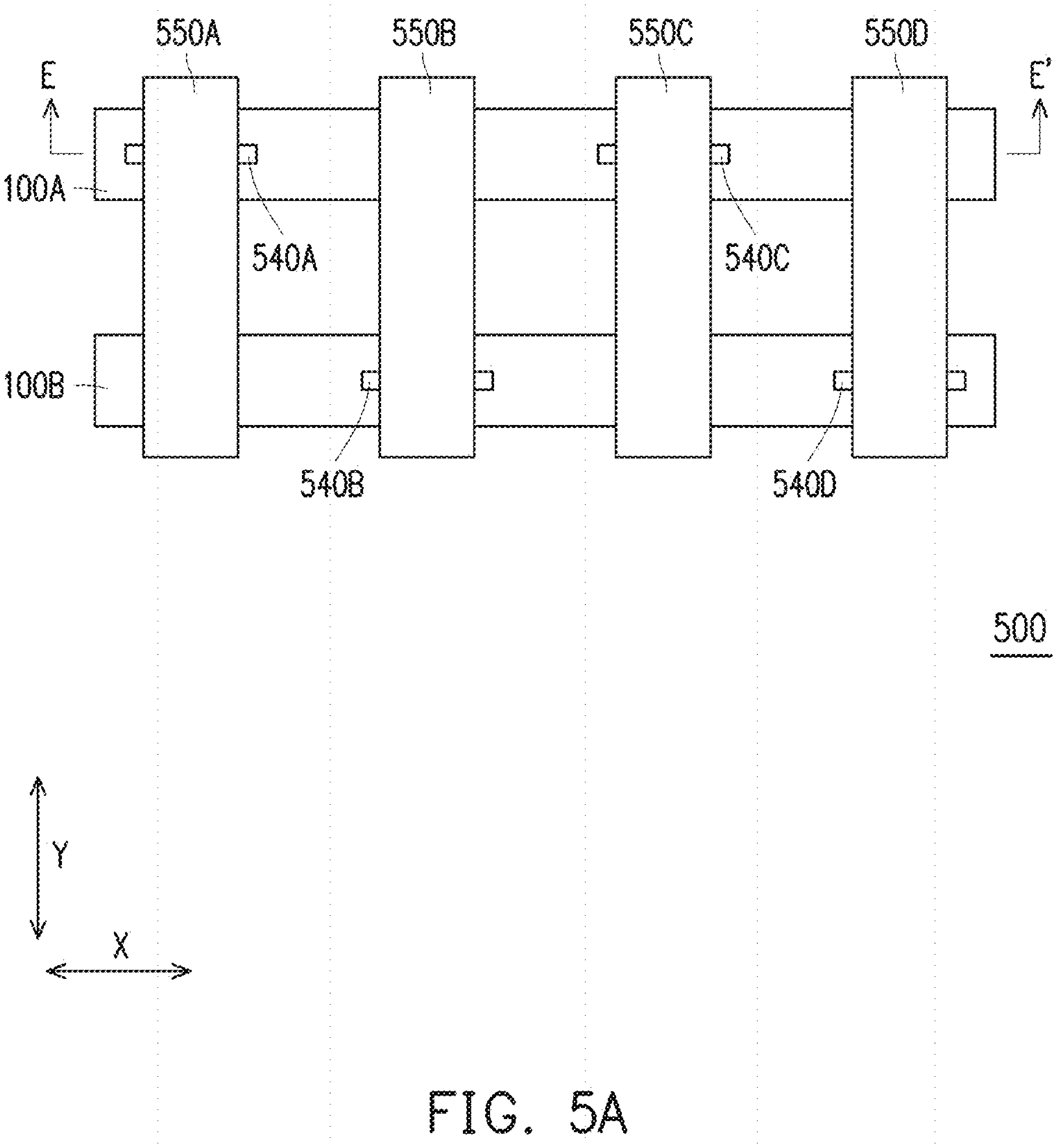

FIG. 5A

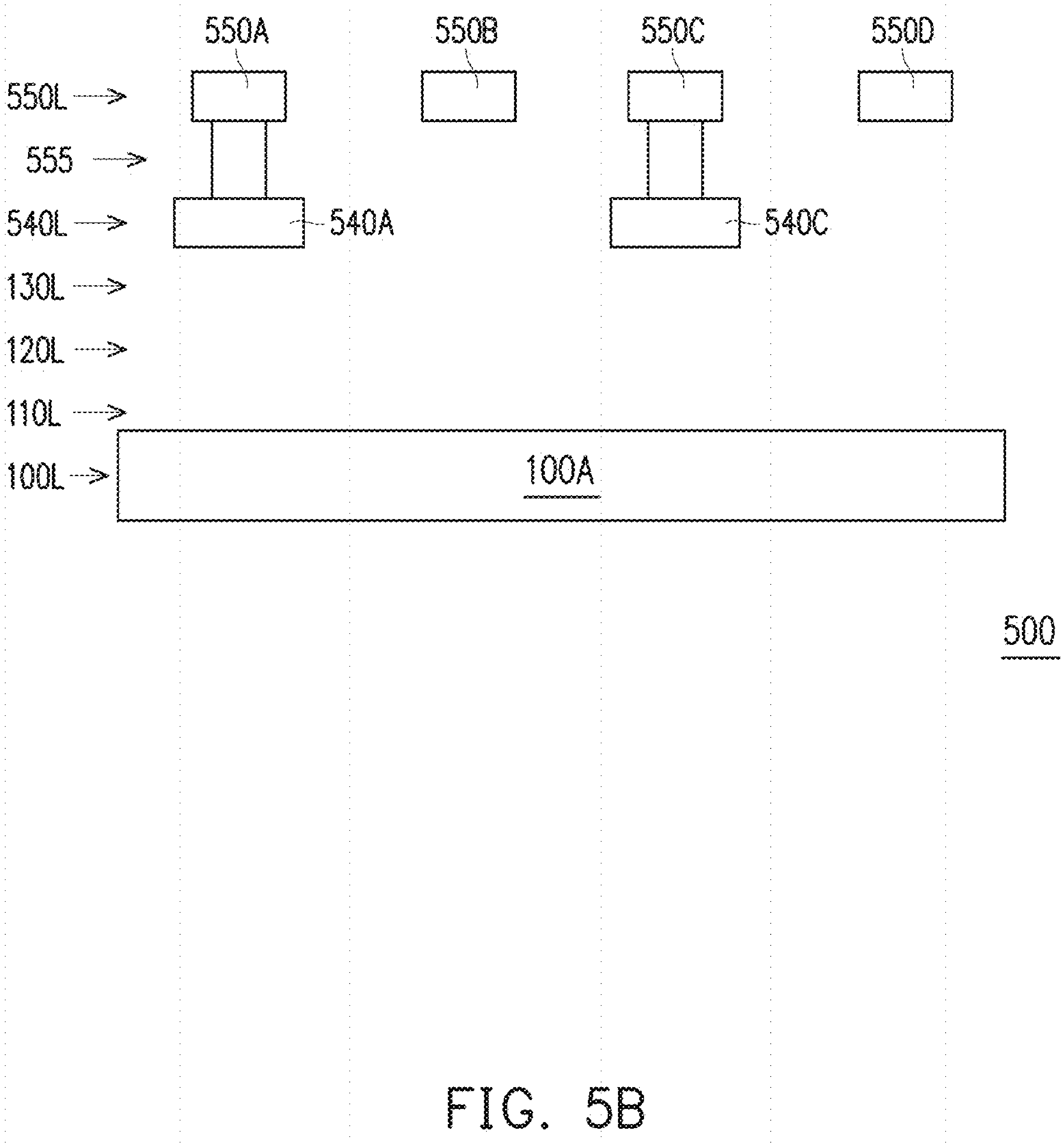
550A
550B
550C
550D
550L
555
540L
540A
540C
130L
120L
110L
100L
100A
500

FIG. 5B

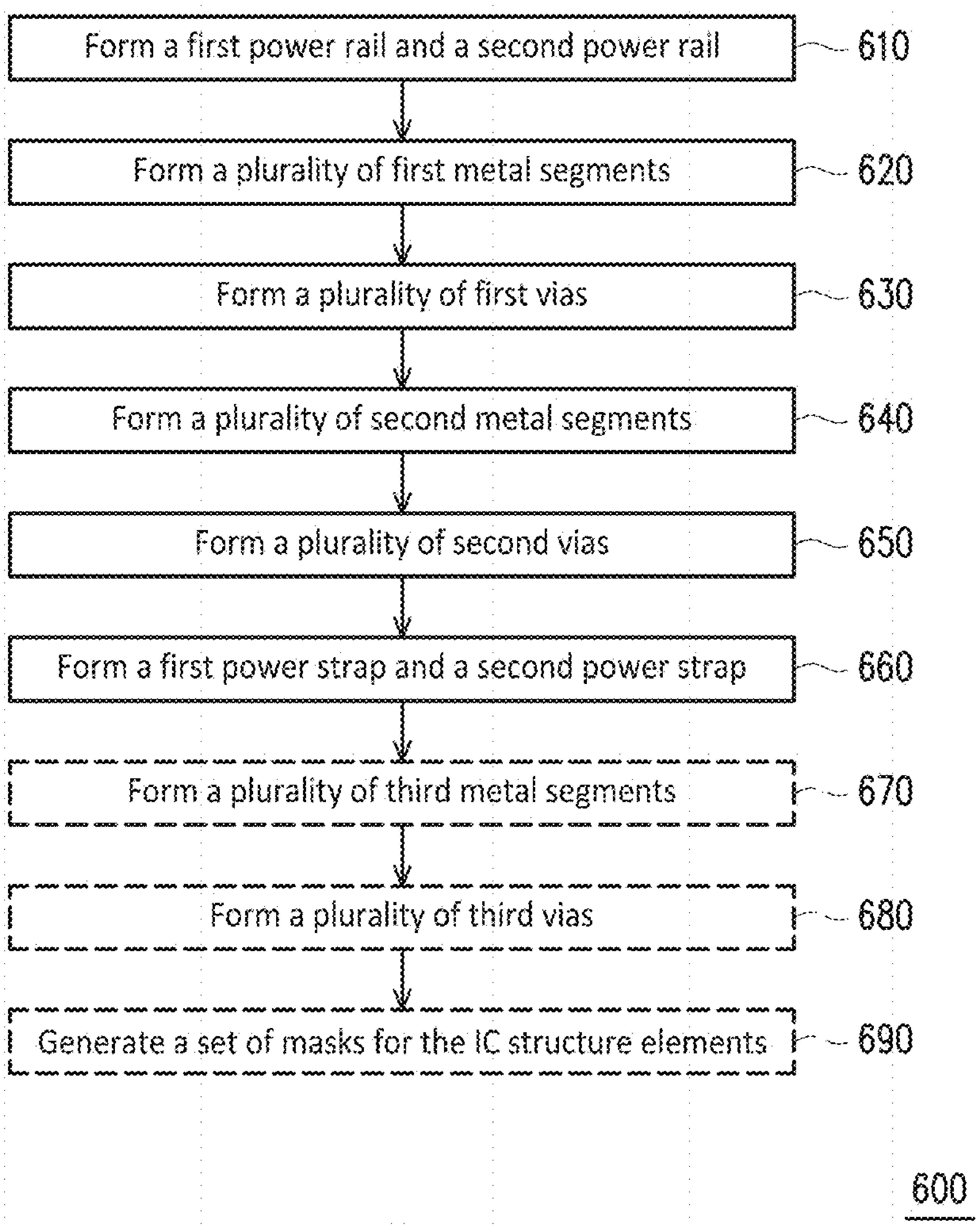
Form a first power rail and a second power rail
610
Form a plurality of first metal segments
620
Form a plurality of first vias
630
Form a plurality of second metal segments
640
Form a plurality of second vias
650
Form a first power strap and a second power strap
660
Form a plurality of third metal segments
670
Form a plurality of third vias
680
Generate a set of masks for the IC structure elements
690
600

FIG. 6

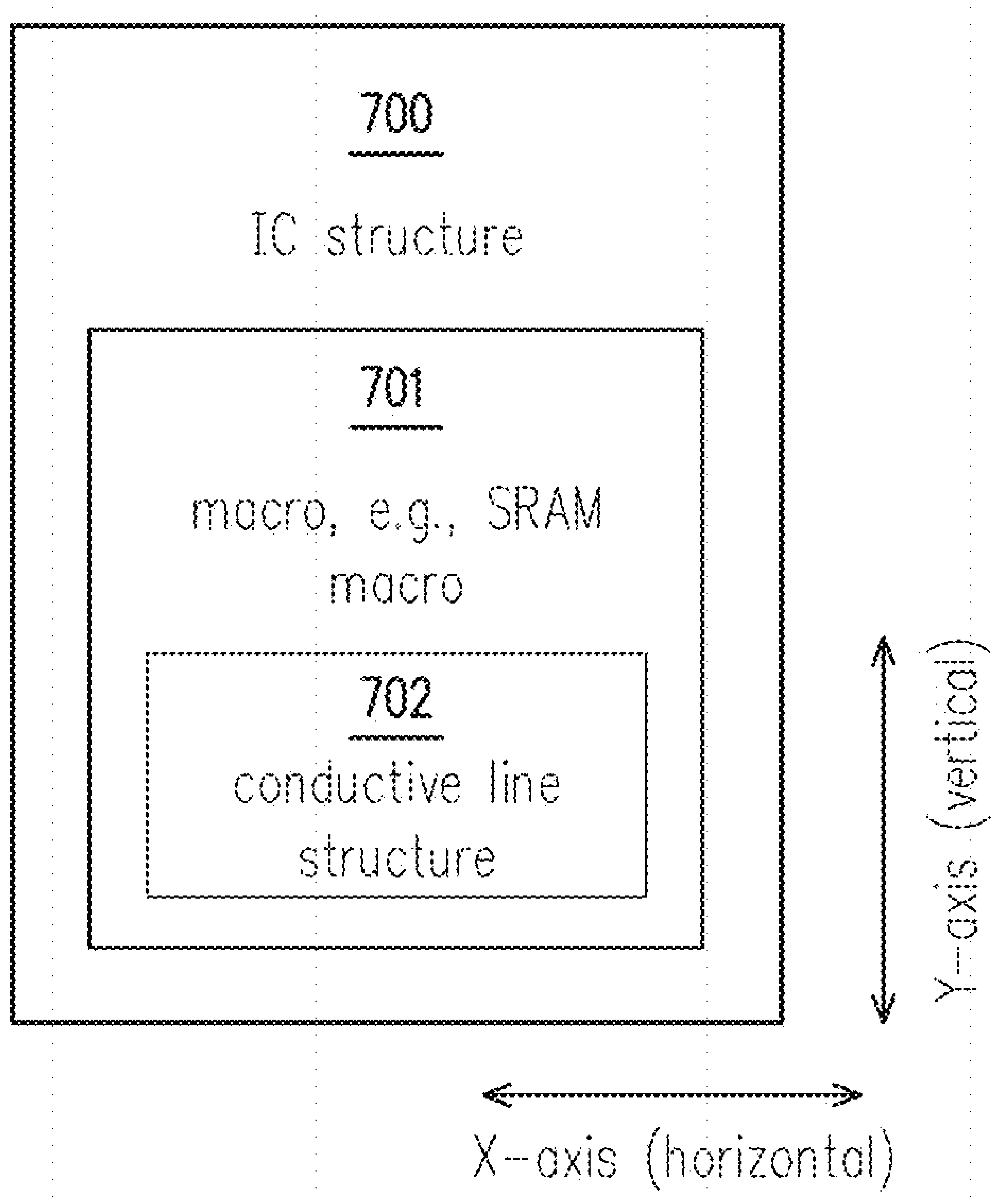
700
IC structure
701
macro, e.g., SRAM macro
702
conductive line structure
Y-axis (vertical)
X-axis (horizontal)

FIG. 7

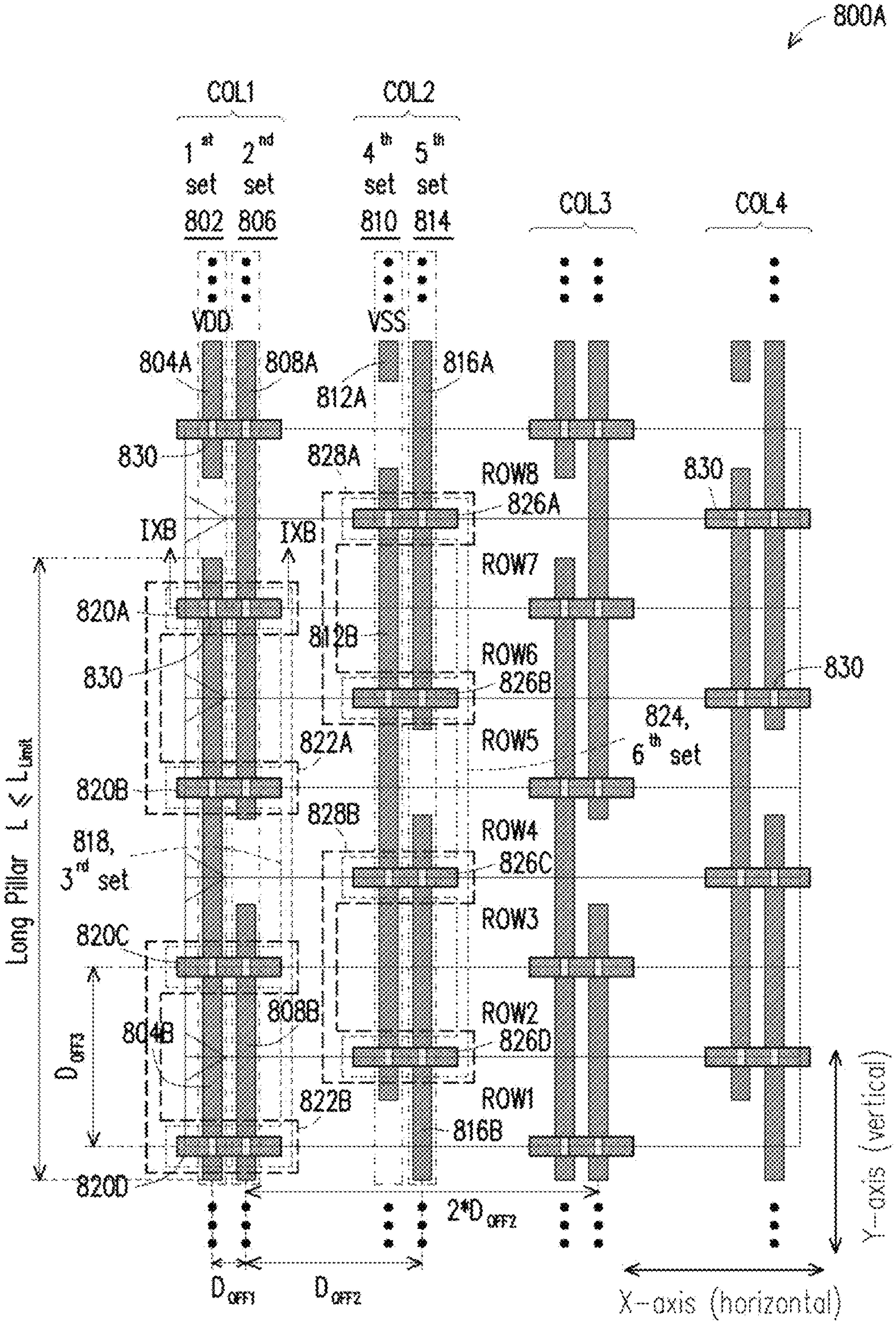
800A
COL1
COL2
1st set 802
2nd set 806
4th set 810
5th set 814
COL3
COL4
VDD
VSS
804A
808A
812A
816A
830
828A
ROW8
826A
IXB
IXB
820A
812B
ROW7
ROW6
826B
830
824, 6th set
ROW5
822A
820B
818, 3rd set
828B
ROW4
826C
ROW3
820C
808B
804B
ROW2
826D
822B
ROW1
816B
820D
Long Pillar L ≤ L_Limit
D_OFF3
2*D_OFF2
D_OFF1
D_OFF2
Y-axis (vertical)
X-axis (horizontal)

FIG. 8A

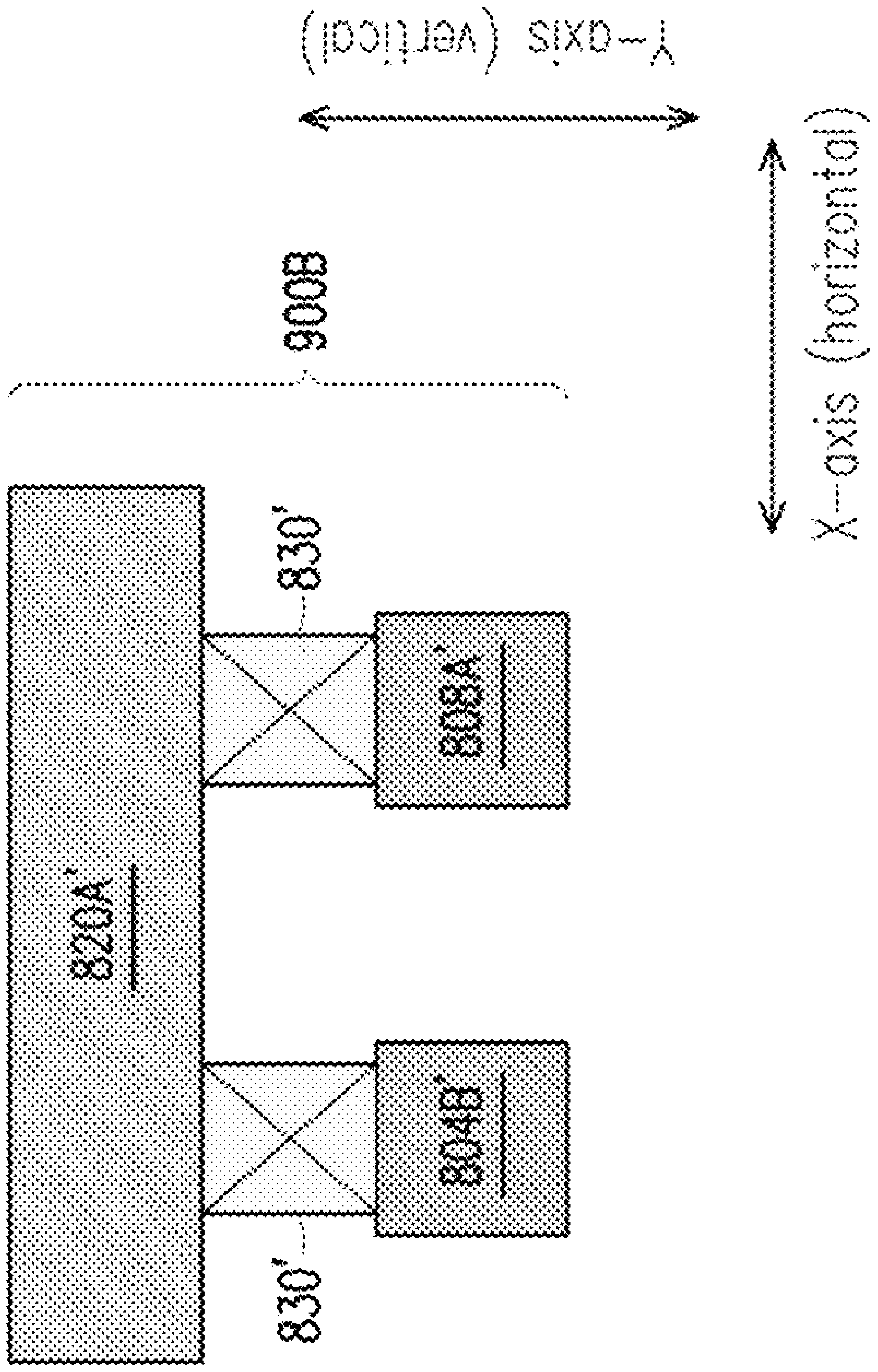
900B
820A'
830'
808A'
804B'
830'
Y-axis (vertical)
X-axis (horizontal)

FIG. 8B

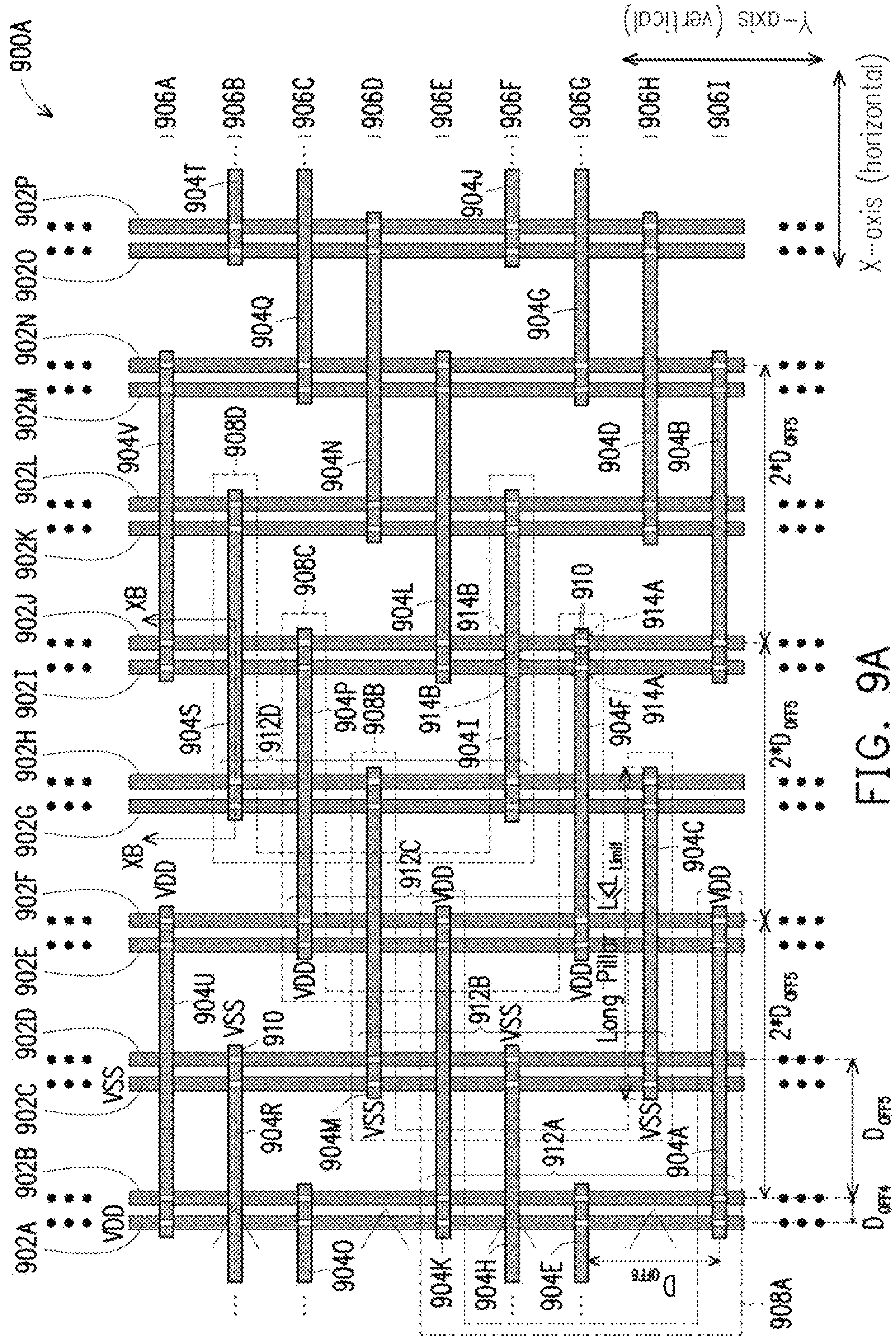
900A
906A
906B
906C
906D
906E
906F
906G
906H
906I
Y-axis (vertical)
X-axis (horizontal)
902A
902B
902C
902D
902E
902F
902G
902H
902I
902J
902K
902L
902M
902N
902O
902P
VDD
VSS
XB
904A
904B
904C
904D
904E
904F
904G
904H
904I
904J
904K
904L
904M
904N
904O
904P
904Q
904R
904S
904T
904U
904V
908A
908B
908C
908D
910
912A
912B
912C
912D
914A
914B
Long Pillar
L≤L_Limit
D_OFF3
D_OFF4
D_OFF5
2*D_OFF5

FIG. 9A

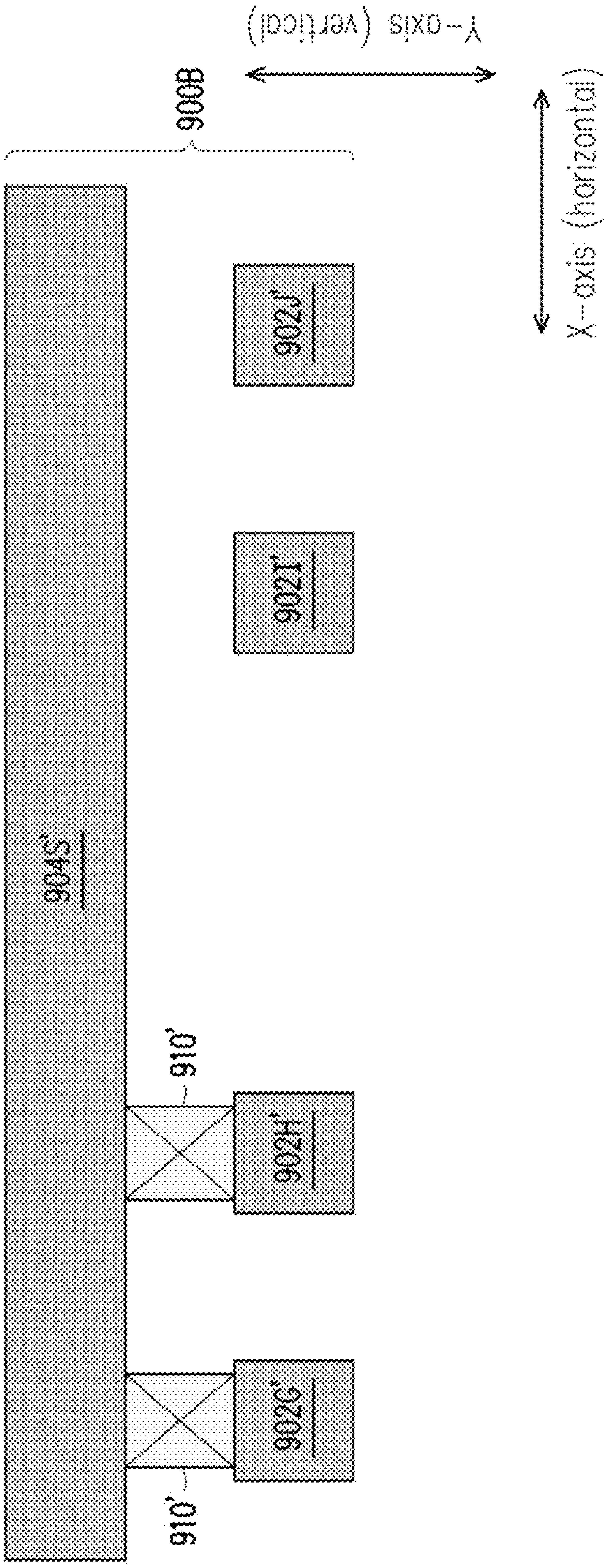
900B
Y-axis (vertical)
X-axis (horizontal)
904S'
902J'
902I'
902H'
902G'
910'
910'

FIG. 9B

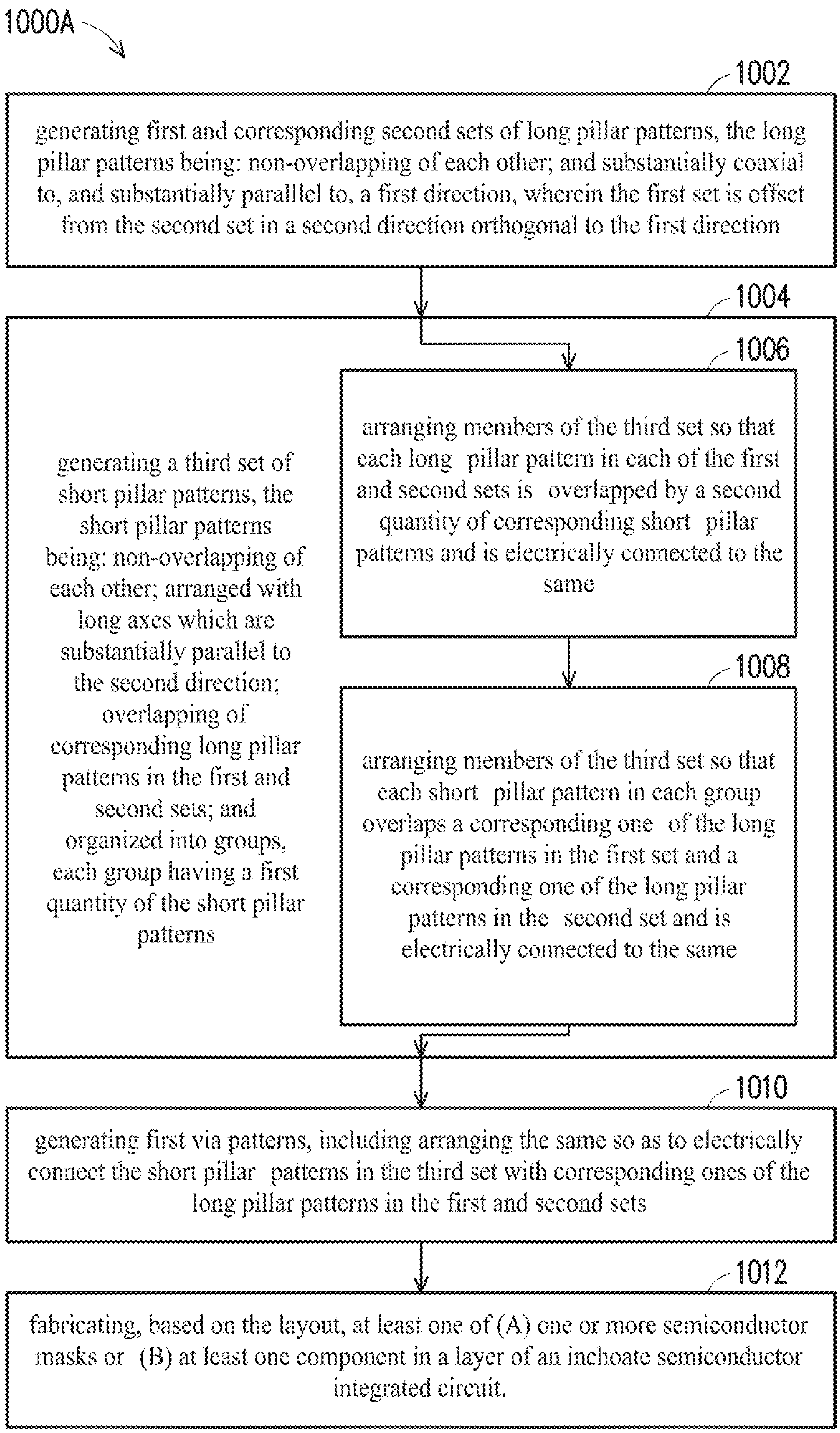
1000A
1002
generating first and corresponding second sets of long pillar patterns, the long pillar patterns being: non-overlapping of each other; and substantially coaxial to, and substantially paralllel to, a first direction, wherein the first set is offset from the second set in a second direction orthogonal to the first direction
1004
generating a third set of short pillar patterns, the short pillar patterns being: non-overlapping of each other; arranged with long axes which are substantially parallel to the second direction; overlapping of corresponding long pillar patterns in the first and second sets; and organized into groups, each group having a first quantity of the short pillar patterns
1006
arranging members of the third set so that each long pillar pattern in each of the first and second sets is overlapped by a second quantity of corresponding short pillar patterns and is electrically connected to the same
1008
arranging members of the third set so that each short pillar pattern in each group overlaps a corresponding one of the long pillar patterns in the first set and a corresponding one of the long pillar patterns in the second set and is electrically connected to the same
1010
generating first via patterns, including arranging the same so as to electrically connect the short pillar patterns in the third set with corresponding ones of the long pillar patterns in the first and second sets
1012
fabricating, based on the layout, at least one of (A) one or more semiconductor masks or (B) at least one component in a layer of an inchoate semiconductor integrated circuit.

FIG. 10A

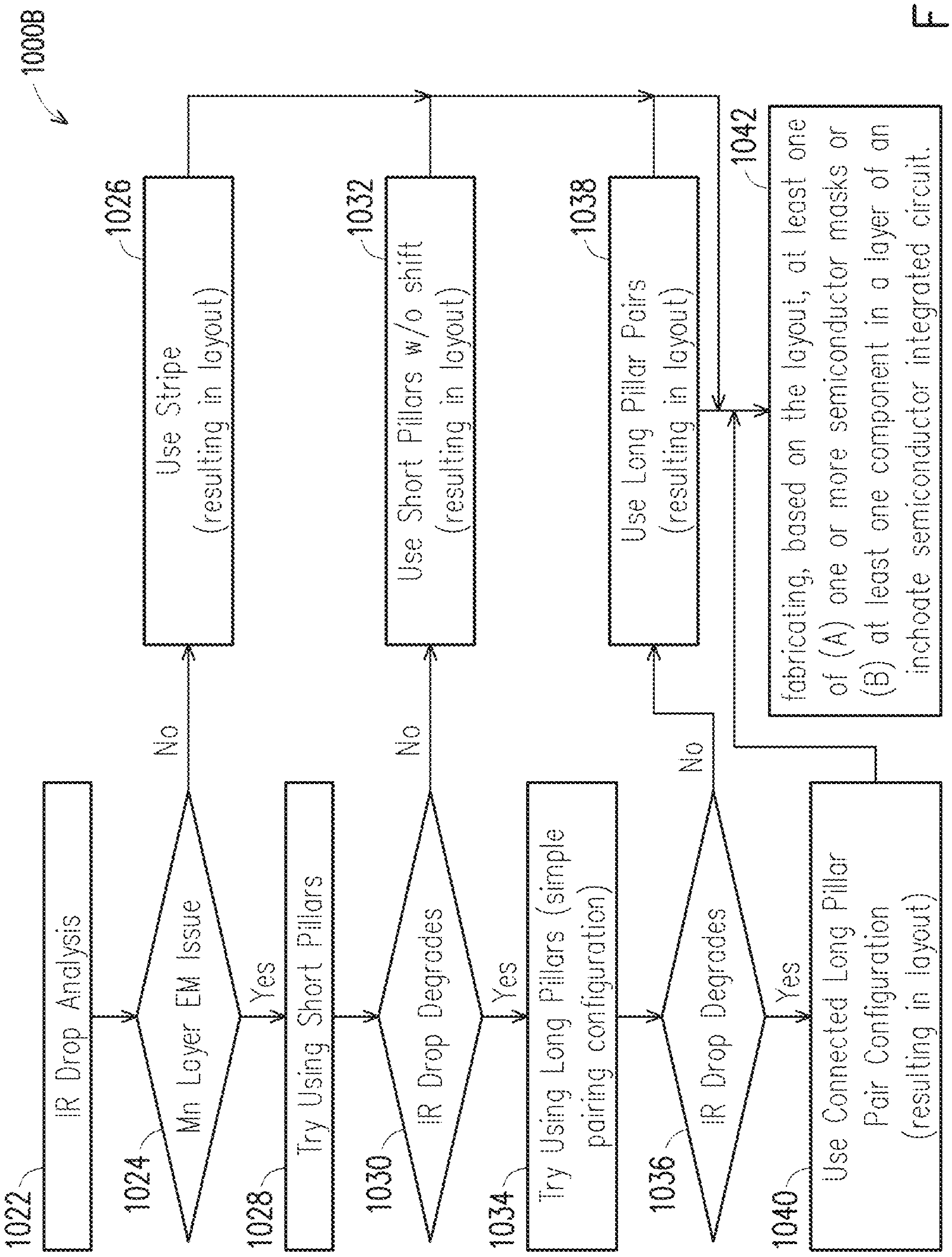
1000B
1022
IR Drop Analysis
1024
Mn Layer EM Issue
No
Yes
1026
Use Stripe (resulting in layout)
1028
Try Using Short Pillars
1030
IR Drop Degrades
No
Yes
1032
Use Short Pillars w/o shift (resulting in layout)
1034
Try Using Long Pillars (simple pairing configuration)
1036
IR Drop Degrades
No
Yes
1038
Use Long Pillar Pairs (resulting in layout)
1040
Use Connected Long Pillar Pair Configuration (resulting in layout)
1042
fabricating, based on the layout, at least one of (A) one or more semiconductor masks or (B) at least one component in a layer of an inchoate semiconductor integrated circuit.

FIG. 10B

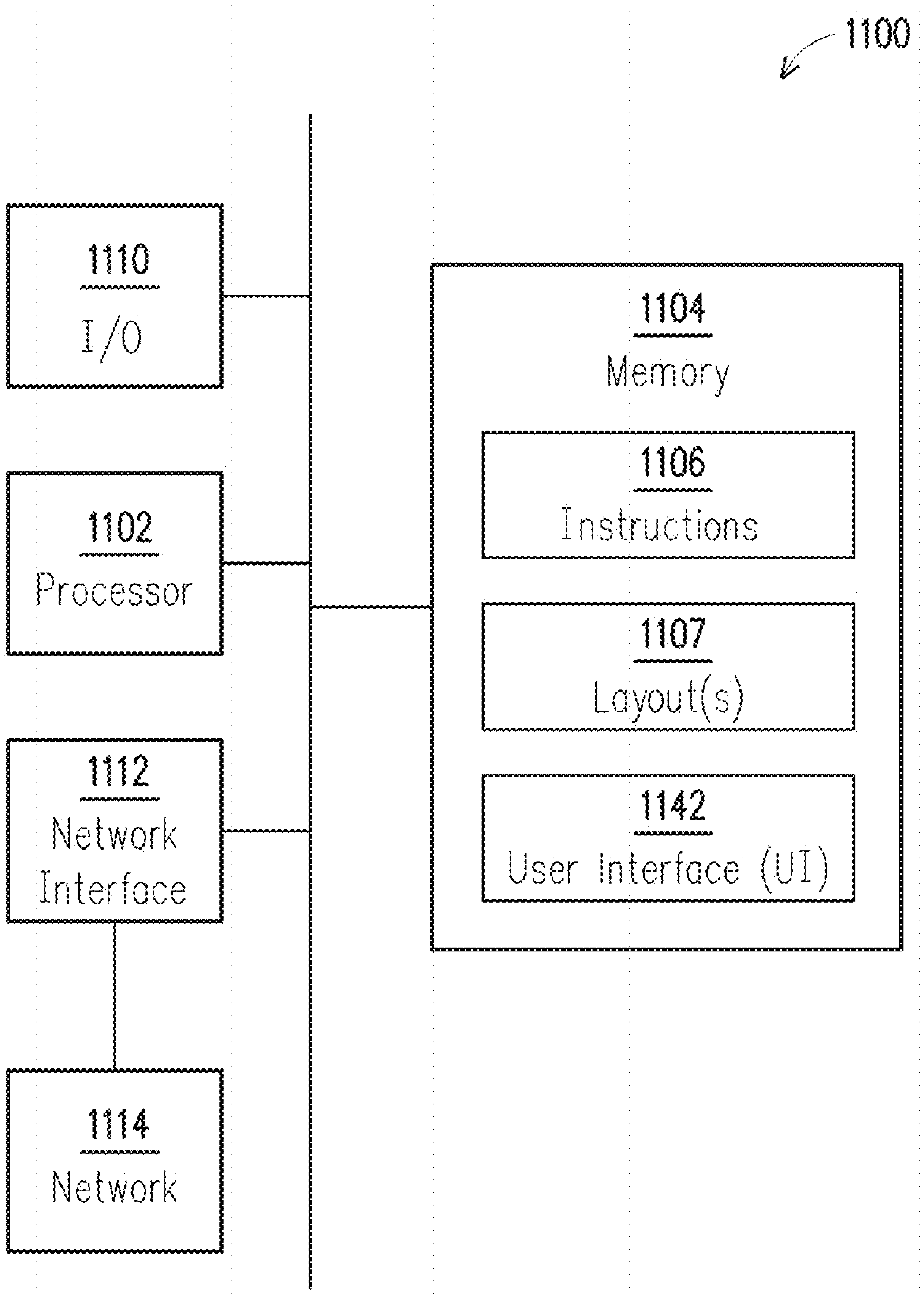
1100
1110
I/O
1102
Processor
1112
Network
Interface
1114
Network
1104
Memory
1106
Instructions
1107
Layout(s)
1142
User Interface (UI)

FIG. 11

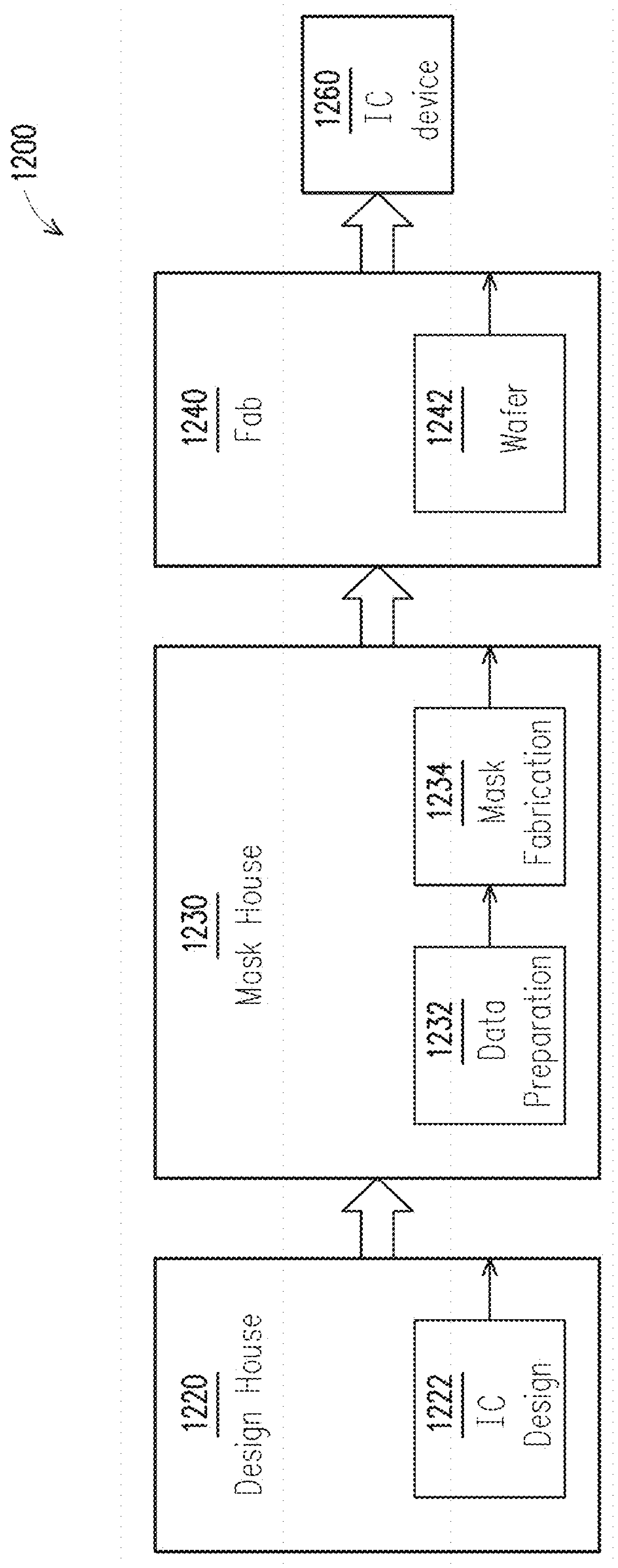
1200
1220
Design House
1222
IC
Design
1230
Mask House
1232
Data
Preparation
1234
Mask
Fabrication
1240
Fab
1242
Wafer
1260
IC
device

FIG. 12

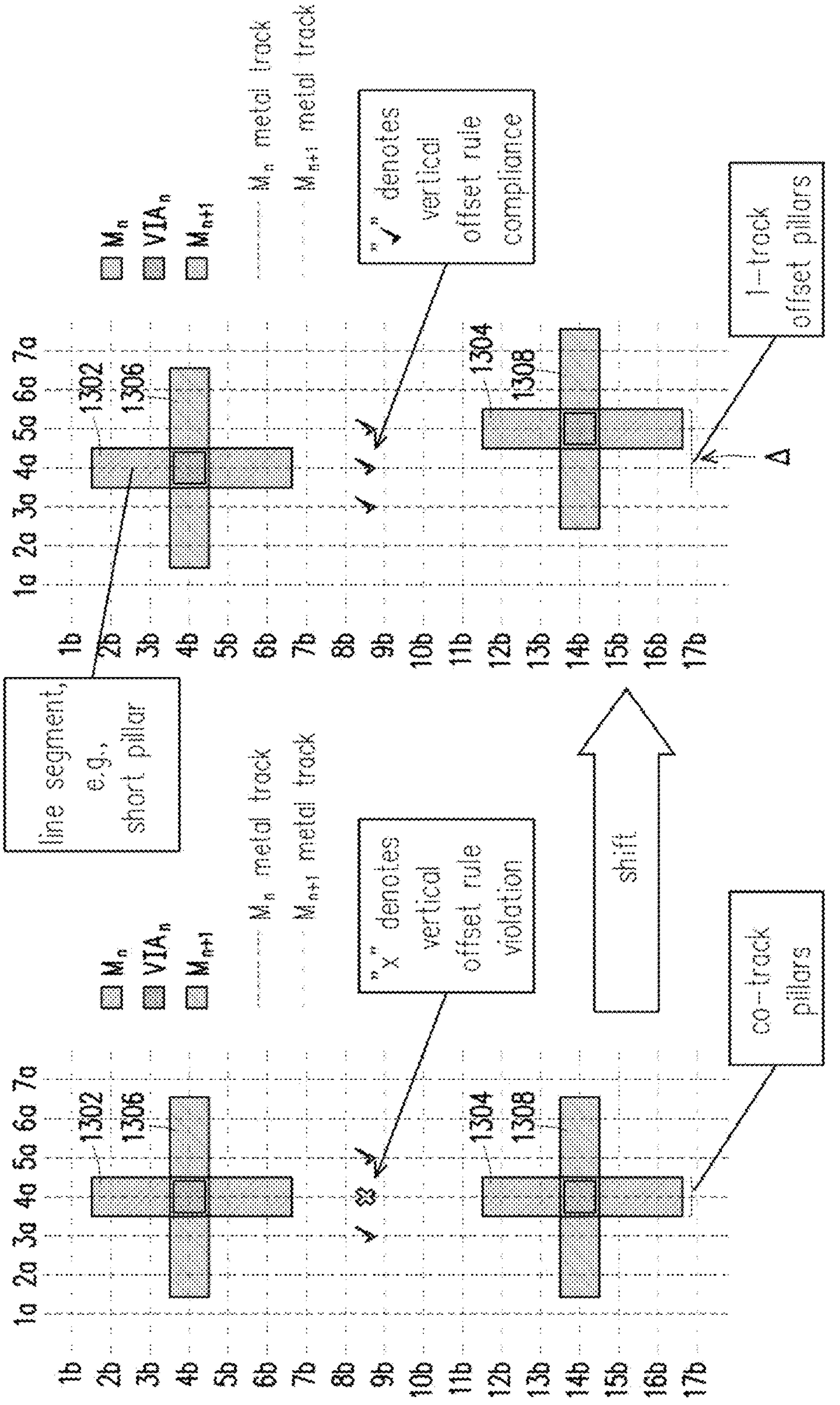

FIG. 13A

FIG. 13B

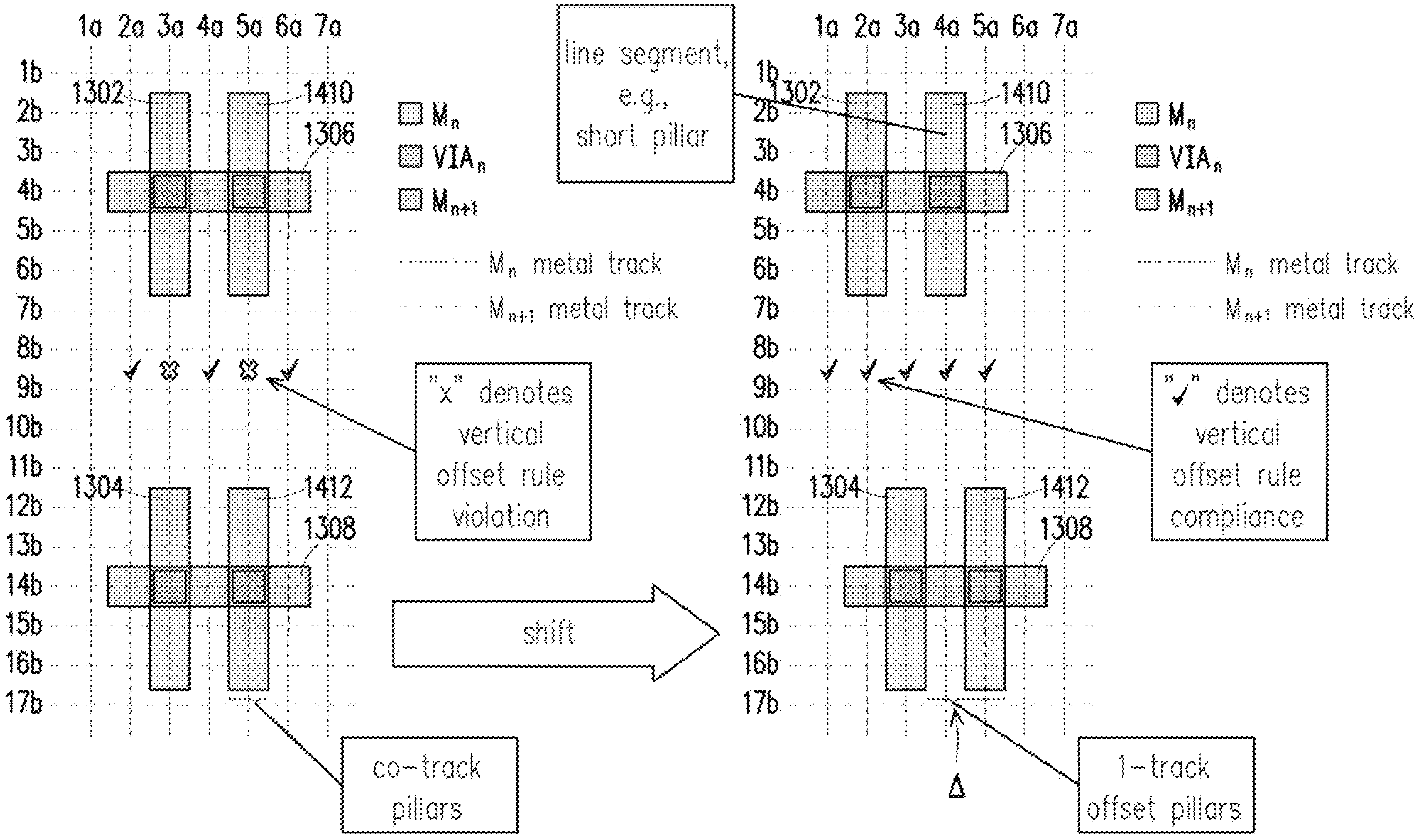

FIG. 14A

FIG. 14B

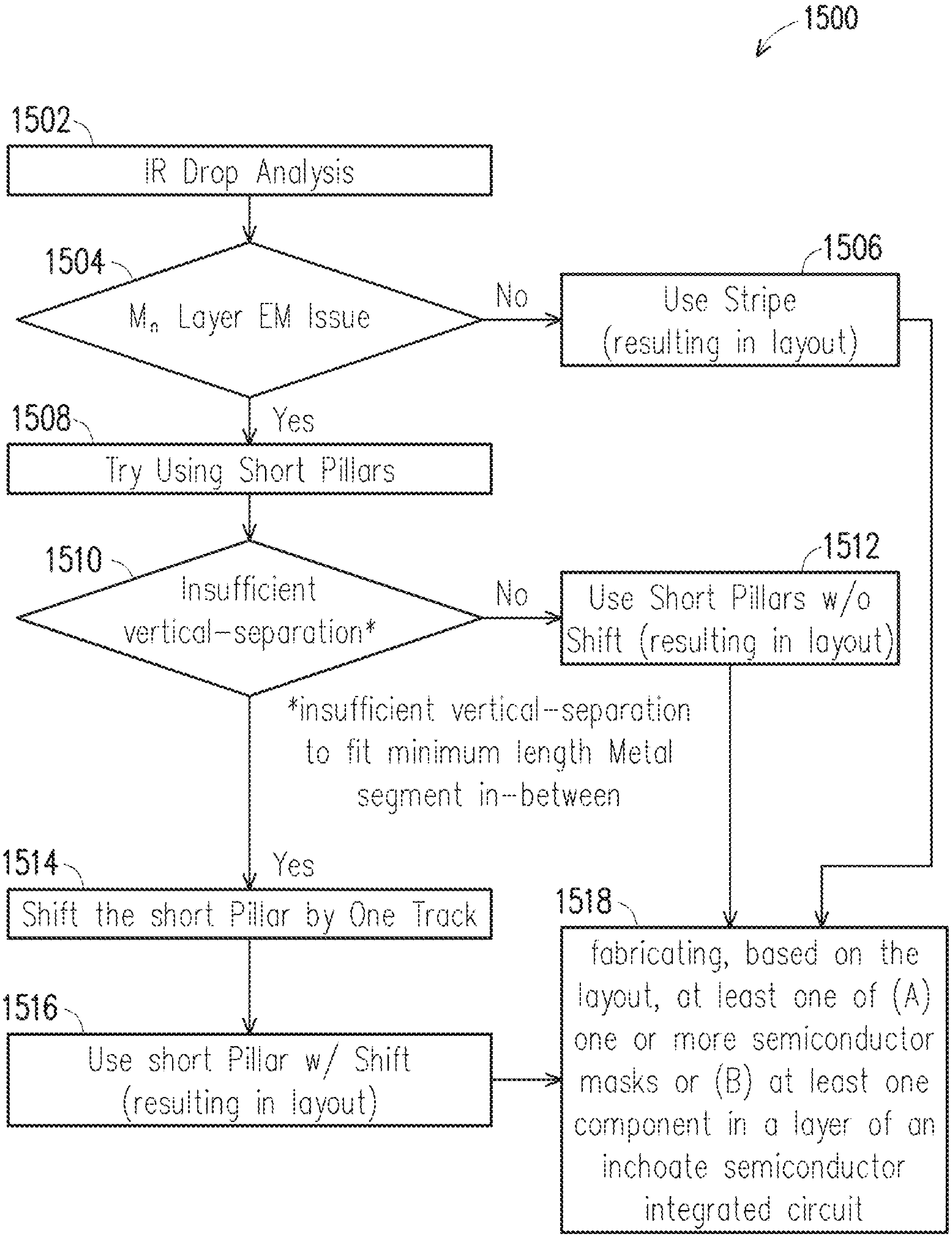
1500
1502
IR Drop Analysis
1504
M_n Layer EM Issue
No
1506
Use Stripe (resulting in layout)
Yes
1508
Try Using Short Pillars
1510
Insufficient vertical-separation*
No
1512
Use Short Pillars w/o Shift (resulting in layout)
*insufficient vertical-separation to fit minimum length Metal segment in-between
Yes
1514
Shift the short Pillar by One Track
1516
Use short Pillar w/ Shift (resulting in layout)
1518
fabricating, based on the layout, at least one of (A) one or more semiconductor masks or (B) at least one component in a layer of an inchoate semiconductor integrated circuit

FIG. 15

POWER GRID STRUCTURES AND METHOD OF FORMING THE SAME

The following application claims priority to U.S. provisional patent application No. 62/427,630 filed on Nov. 29, 2016, and is hereby incorporated by reference in its entirety.

BACKGROUND

In many integrated circuits (ICs), power rails are used to distribute power to functional circuit elements formed in a substrate. Power is often delivered to power rails using metal layers between the power rails and power straps at a level above the level of the power rails.

The resistance of an IC structure including such metal layers can affect the efficiency of power delivery, heat generation, and susceptibility to electromigration (EM). Routing of the metal layers can also impact the routing of additional electrical connections to the functional circuit elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIGS. **1**A, **1**B, and **1**C are diagrams of an IC structure, in accordance with some embodiments.

FIGS. **2**A, **2**B, and **2**C are diagrams of an IC structure, in accordance with some embodiments.

FIGS. **3**A, **3**B, and **3**C are diagrams of an IC structure, in accordance with some embodiments.

FIGS. **4**A and **4**B are diagrams of an IC structure, in accordance with some embodiments.

FIGS. **5**A and **5**B are diagrams of an IC structure, in accordance with some embodiments.

FIG. **6** is a flowchart of a method of forming an IC structure, in accordance with some embodiments.

FIG. **7** is a block diagram of an IC structure, in accordance with at least one embodiment of the present disclosure.

FIG. **8**A is a layout diagram of a conductive line structure of an IC structure, in accordance with at least one embodiment of the present disclosure.

FIG. **8**B is a cross-sectional diagram of a conductive line structure of an IC structure relating to the layout of FIG. **8**A, in accordance with at least one embodiment of the present disclosure.

FIG. **9**A is a layout diagram of a conductive line structure of an IC structure, in accordance with at least one embodiment of the present disclosure.

FIG. **9**B is a cross-sectional diagram of a conductive line structure of an IC structure relating to the layout of FIG. **9**A, in accordance with at least one embodiment of the present disclosure.

FIG. **10**A is a flowchart of a method of generating a layout of an IC structure, in accordance with some embodiments.

FIG. **10**B is a high level process flow of a method of shifting at least one pillar of an IC structure in a layout, in accordance with at least one embodiment of the present disclosure.

FIG. **11** is a block diagram of an electronic design automation (EDA) system, in accordance with at least one embodiment of the present disclosure.

FIG. **12** is a block diagram of an integrated circuit (IC) manufacturing system, and an IC manufacturing flow associated therewith, in accordance with at least one embodiment of the present disclosure.

FIGS. **13**A-**13**B are layout diagrams of a portion of a shifted pillar of an IC structure, in accordance with at least one embodiment of the present disclosure.

FIGS. **14**A-**14**B are layout diagrams of a portion of two shifted pillars of an IC structure, in accordance with at least one embodiment of the present disclosure.

FIG. **15** is a high level process flow of another method of shifting at least one pillar of an IC structure in a layout, in accordance with at least one embodiment of the present disclosure.

The patent or application file contains drawings/photographs executed in color. Copies of this patent with color drawing(s)/photograph(s) will be provided by the Office upon request and payment of the necessary fee.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components, values, operations, materials, arrangements, etc., are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. Other components, values, operations, materials, arrangements, etc., are contemplated. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

An IC structure includes a power rail and first metal segments above the power rail. The first metal segments are oriented in a first metal level direction perpendicular to a power rail direction and first vias are positioned between the power rail and the first metal segments at locations where first metal segments overlap the power rail. A second metal segment is positioned above the first metal segments, overlaps the power rail, and is oriented in the power rail direction. Second vias are positioned above the first vias between the first metal segments and the second metal segments. A power strap is positioned above the second metal segment and is electrically connected to the power rail by the first and second metal segments and the first and second vias. Each first metal segment of the plurality of first metal segments has a minimum width, and the power strap has a width greater than a minimum width. In some embodiments, a second power strap is electrically connected to a second power rail.

FIGS. **1**A, **1**B, and **1**C are diagrams of an IC structure **100**, in accordance with some embodiments. FIG. **1**A is a diagram based on a top view of a lower portion of IC structure **100**, FIG. **1**B is a diagram based on a top view of an upper portion of IC structure **100**, and FIG. **1**C is a diagram based on a cross-sectional view of IC structure **100** as intersected by plane A-A'.

As shown in FIG. **1**A, **1**C structure **100** includes power rails **100**A and **100**B, first metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H, and second metal segments **120**A, **120**B, **120**C, and **120**D. A first direction X and a second direction Y, perpendicular to first direction X, are indicated in FIG. **1**A. As shown in FIG. **1**B, **1**C structure **100** also includes third metal segments **130**A, **130**B, **130**C, **130**D, **130**E, **130**F, **130**G, and **130**H. For simplicity, the first metal segments **110**A-**110**H are omitted in FIG. **1**B.

As shown in FIG. **1**C (in part), power rails **100**A and **100**B are positioned at a power rail level **100**L, first metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H are positioned at a first metal level **110**L above power rail level **100**L, second metal segments **120**A, **120**B, **120**C, and **120**D are positioned at a second metal level **120**L above first metal level **110**L, and third metal segments **130**A, **130**B, **130**C, **130**D, **130**E, **130**F, **130**G, and **130**H are positioned at a third metal level **130**L above second metal level **120**L.

In some embodiments, first metal level **110**L is immediately above power rail level **100**L. In some embodiments, one or more metal levels (not shown) separate first metal level **110**L from power rail level **100**L and first metal level **110**L is not immediately above power rail level **100**L.

In some embodiments, second metal level **120**L is immediately above first metal level **110**L. In some embodiments, one or more metal levels (not shown) separate second metal level **120**L from first metal level **110**L and second metal level **120**L is not immediately above first metal level **110**L.

In some embodiments, third metal level **130**L is immediately above second metal level **120**L. In some embodiments, one or more metal levels (not shown) separate third metal level **130**L from second metal level **120**L and third metal level **130**L is not immediately above second metal level **120**L.

In some embodiments, power rail level **100**L is a metal zero layer of an IC process, first metal level **110**L is a metal one layer of the IC process, second metal level **120**L is a metal two layer of the IC process, and third metal level **130**L is a metal three layer of the IC process.

Each of power rails **100**A and **100**B, first metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H, second metal segments **120**A, **120**B, **120**C, and **120**D, and third metal segments **130**A, **130**B, **130**C, **130**D, **130**E, **130**F, **130**G, and **130**H comprises a conductive material such as a metal, a metal composite, or other suitable material that is formed in one or more metallization layers by one or more of a physical vapor deposition process, a chemical vapor deposition process, a plating process, or other suitable process.

Power rails **100**A and **100**B are electrically conductive line segments positioned in parallel at power rail level **100**L and oriented in first direction X. First direction X is also described as a power rail direction. In some embodiments, IC structure **100** includes only one of power rails **100**A or **100**B.

In some embodiments, power rails **100**A and **100**B are configured as outbound power rails for VDD and VSS of one or more functional circuit elements (not shown) positioned at and/or below power rail level **100**L. In some embodiments, one or more functional circuit elements are configured as cells (not shown) positioned between power rails **100**A and **100**B. The one or more functional circuit elements include a transistor, diode, resistor, inductor, capacitor, or other suitable device, or a combination of one or more such devices formed in a substrate.

First metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H are electrically conductive line segments positioned in parallel at first metal level **110**L and oriented in second direction Y. Second direction Y is also described as a first metal level direction.

Each of first metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H overlaps both power rail **100**A and power rail **100**B and is also described as a metal strap. First metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H are also described as a plurality of first metal segments or a plurality of metal straps. In some embodiments, first metal level **110**L corresponds to a metal strap level. In some embodiment, second direction Y corresponds to a metal strap direction.

In the embodiment shown in FIGS. **1**A, **1**B, and **1**C, a plurality of first metal segments includes eight first metal segments. In some embodiments, a plurality of first metal segments includes first metal segments (not shown) in addition to first metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G and **110**H. In some embodiments, a plurality of first metal segments includes a subset of first metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G and **110**H.

In some embodiments, each first metal segment of a plurality of first metal segments has a width corresponding to a predetermined minimum width for first metal level **110**L. In some embodiments, each first metal segment of a plurality of first metal segments has a width corresponding to a predetermined minimum width for a metal one layer of an IC process. Because of process variations, a width corresponding to a predetermined minimum width has a value within a tolerance range about the predetermined minimum width.

First metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H are positioned along tracks **112**A, **112**B, **112**C, **112**D, **112**E, **112**F, **112**G, and **112**H, respectively. First metal segments **110**A and **110**B are a pair of first metal segments having a pitch **114** defined as the distance between tracks **112**A and **112**B. Similarly, first metal segments **110**C and **110**D, **110**E and **110**F, and **110**G and **110**H are pairs of first metal segments having pitch **114** (not labelled). The spacing of pairs of first metal segments is shown in FIG. **1**A as pitch **116**, the distance between tracks **112**A and **112**C.

In some embodiments, pitch **114** corresponds to a poly pitch of an IC process. In some embodiments, pitch **114** corresponds to a metal one pitch of an IC process that is the same as a poly pitch of the IC process. In some embodiments, pitch **114** corresponds to a metal one pitch of an IC process that is different from a poly pitch of the IC process. In some embodiments, pitch **114** corresponds to a multiple of a metal one pitch of an IC process.

In some embodiments, pitch **116** is a multiple of pitch **114**. In some embodiments, pitch **116** is a multiple of pitch **114** that ranges from eight to 64. In some embodiments, pitch **116** is a multiple of pitch **114** that equals 16. In some embodiments, pitch **114** and pitch **116** are both multiples of a metal one pitch of an IC process.

First vias **115** are vias positioned between power rail level **100**L and first metal level **110**L at locations at which first metal segments **110**A, **110**B, **110**E, and **110**F overlap power rail **100**A and at locations at which first metal segments **110**C, **110**D, **110**G, and **110**H overlap first power rail **100**B. In some embodiments, first vias **115** are single vias positioned at the locations at which metal segments **110**C, **110**D, **110**G, and **110**H overlap first power rail **100**B. First vias **115** are not positioned at locations at which first metal segments **110**A, **110**B, **110**E, and **110**F overlap power rail **100**B or at locations at which metal segments **110**C, **110**D, **110**G, and **110**H overlap first power rail **100**A.

By this configuration, first vias **115** electrically connect first metal segments **110**A, **110**B, **110**E, and **110**F to power rail **100**A and are free from electrically connecting first metal segments **110**A, **110**B, **110**E, and **110**F to power rail **100**B. By this configuration, first vias **115** also electrically connect first metal segments **110**C, **110**D, **110**G, and **110**H to power rail **100**B and are free from electrically connecting first metal segments **110**C, **110**D, **110**G, and **110**H to power rail **100**A.

In accordance with this configuration, first metal segments **110**A, **110**B **110**E, and **110**F are described as a first set of pairs of first metal segments, and first metal segments **110**C, **110**D **110**G, and **110**H are described as a second set of pairs of first metal segments. In the embodiment shown in FIGS. **1**A, **1**B, and **1**C, a set of pairs of first metal segments includes two pairs of first metal segments. In some embodiments, a set of pairs of first metal segments includes pairs of first metal segments (not shown) in addition to first metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H.

Second metal segments **120**A, **120**B, **120**C, and **120**D are electrically conductive line segments oriented in first direction X. Second metal segment **120**A overlaps power rail **100**A at the locations at which first metal segments **110**A and **110**B overlap power rail **100**A, and second metal segment **120**C overlaps power rail **100**A at the locations at which first metal segments **110**E and **110**F overlap power rail **100**A. Second metal segment **120**B overlaps power rail **100**B at the locations at which first metal segments **110**C and **110**D overlap power rail **100**B, and second metal segment **120**D overlaps power rail **100**B at the locations at which first metal segments **110**G and **110**H overlap power rail **100**B.

Each of second metal segments **120**A and **120**C is free from overlapping first metal segments **110**C, **110**D, **110**G, or **110**H, and each of second metal segments **120**B and **120**D is free from overlapping first metal segments **110**A, **110**B, **110**E, or **110**F.

Second metal segments **120**A, **120**B, **120**C, and **120**D are also described as a plurality of second metal segments. In the embodiment shown in FIGS. **1**A, **1**B, and **1**C, a plurality of second metal segments includes four second metal segments. In some embodiments, a plurality of second metal segments includes second metal segments (not shown) in addition to second metal segments **120**A, **120**B, **120**C, and **120**D. In some embodiments, a plurality of second metal segments includes a subset of second metal segments **120**A, **120**B, **120**C, and **120**D.

In some embodiments, each second metal segment of a plurality of second metal segments has a width corresponding to a predetermined minimum width for second metal level **120**L. In some embodiments, each second metal segment of a plurality of second metal segments has a width corresponding to a predetermined minimum width for a metal two layer of an IC process.

Second vias **125** are vias positioned between first metal level **110**L and second metal level **120**L at locations above the locations at which first vias **115** are positioned. Thus, second vias **125** are positioned at the locations at which second metal segment **120**A overlaps first metal segments **110**A and **110**B, the locations at which second metal segment **120**B overlaps first metal segments **110**C and **110**D, the locations at which second metal segment **120**C overlaps first metal segments **110**E, and the locations at which second metal segment **120**D overlaps first metal segments **110**G and **110**H.

In some embodiments, second vias **125** are single vias positioned at the locations above the locations at which first vias **115** are positioned.

By this configuration, second metal segment **120**A is electrically connected to first metal segments **110**A and **110**B, second metal segment **120**B is electrically connected to first metal segments **110**C and **110**D, second metal segment **120**C is electrically connected to first metal segments **110**E and **110**F, and second metal segment **120**D is electrically connected to first metal segments **110**G and **110**H.

Third metal segments **130**A, **130**B, **130**C, **130**D, **130**E, **130**F, **130**G, and **130**H are electrically conductive line segments positioned in parallel at third metal level **130**L and oriented in second direction Y.

Each of third metal segments **130**A, **130**B, **130**C, **130**D, **130**E, **130**F, **130**G, and **130**H overlaps only one of power rail **100**A or power rail **100**B and is also described as a metal stub. In some embodiments, third metal level **130**L corresponds to a metal stub level.

Third metal segments **130**A and **130**B overlap second metal segment **120**A and power rail **100**A. Third metal segments **130**C and **130**D overlap second metal segment **120**B and power rail **100**B. Third metal segments **130**E and **130**F overlap second metal segment **120**C and power rail **100**A. Third metal segments **130**G and **130**H overlap second metal segment **120**D and power rail **100**B.

Third metal segments **130**A, **130**B, **130**C, **130**D, **130**E, **130**F, **130**G, and **130**H are also described as a plurality of third metal segments or a plurality of metal stubs. In the embodiment shown in FIGS. **1**A, **1**B, and **1**C, a plurality of third metal segments includes eight third metal segments. In some embodiments, a plurality of third metal segments includes third metal segments (not shown) in addition to third metal segments **130**A, **130**B, **130**C, **130**D, **130**E, **130**F, **130**G, and **130**H. In some embodiments, a plurality of third metal segments includes a subset of third metal segments **130**A, **130**B, **130**C, **130**D, **130**E, **130**F, **130**G, and **130**H.

Third metal segments **130**A, **130**B, **130**C, **130**D, **130**E, **130**F, **130**G, and **130**H are positioned along tracks **132**A, **132**B, **132**C, **132**D, **132**E, **132**F, **132**G, and **132**H, respectively. In some embodiments, tracks **132**A, **132**B, **132**C, **132**D, **132**E, **132**F, **132**G, and **132**H align with tracks **112**A, **112**B, **112**C, **112**D, **112**E, **112**F, **112**G, and **112**H, respectively. In some embodiments, each track of tracks **132**A, **132**B, **132**C, **132**D, **132**E, **132**F, **132**G, and **132**H does not align with a corresponding track of tracks **112**A, **112**B, **112**C, **112**D, **112**E, **112**F, **112**G, and **112**H, but is sufficiently close to a corresponding track so that a corresponding third metal segment of third metal segments **130**A, **130**B, **130**C, **130**D, **130**E, **130**F, **130**G, and **130**H overlaps a corresponding first metal segment of first metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H.

In some embodiments, each third metal segment of a plurality of third metal segments has a width corresponding to a predetermined minimum width for third metal level

130L. In some embodiments, each third metal segment of a plurality of third metal segments has a width corresponding to a predetermined minimum width for a metal three layer of an IC process.

Third vias **135** are vias positioned between second metal level **120**L and third metal level **130**L at locations above the locations at which second vias **125** are positioned. Thus, third vias are positioned at the locations at which third metal segments **130**A and **130**B overlap second metal segment **120**A, the locations at which third metal segments **130**C and **130**D overlap second metal segment **120**B, the locations at which third metal segments **130**E and **130**F overlap second metal segment **120**C, and the locations at which third metal segments **130**G and **130**H overlap second metal segment **120**D. In some embodiments, third vias **135** are single vias positioned at the locations above the locations at which second vias **125** are positioned. Third vias **135** are shown in FIG. **1**A, with one third via **135** labelled as an example.

By this configuration, third metal segments **130**A and **130**B are electrically connected to second metal segment **120**A, third metal segments **130**C and **130**D are electrically connected to second metal segment **120**B, third metal segments **130**E and **130**F are electrically connected to second metal segment **120**C, and third metal segments **130**G and **130**H are electrically connected to second metal segment **120**D.

Fourth vias **145** are vias positioned above third metal level **130**L at locations above the locations at which third vias **135** are positioned. As discussed below with respect to IC structure **500**, by this configuration, third metal segments **130**A and **130**B are electrically connected to a fourth metal segment **540**A, third metal segments **130**C and **130**D are electrically connected to a fourth metal segment **540**B, third metal segments **130**E and **130**F are electrically connected to a fourth metal segment **540**C, and third metal segments **130**G and **130**H are electrically connected to a fourth metal segment **540**D. In some embodiments, fourth vias **145** are single vias positioned at the locations above the locations at which third vias **135** are positioned. Fourth vias **145** are shown in FIG. **1**B, with one fourth via **145** labelled as an example.

The configuration of IC structure **100** in combination with IC structure **500** thereby establishes electrical connections between power straps positioned at upper metal layers and power rails at lower layers using minimum-width metal elements and, in some embodiments, single vias in the layers between the power straps and the power rails. By providing parallel paths having low resistance, one or more embodiments enable efficient power delivery, limited heat generation, and low susceptibility to EM.

In at least some embodiments, the double strap and extended pitch configuration of the sets of pairs of first metal segments also facilitates routing of various electrical connections to functional circuits powered via the power rails, e.g., by reducing an area/footprint impact of the power-grid (which increases space available for placement of other structure).

Compared to approaches that use metal elements wider than minimum-width metal elements and/or multiple vias at locations where metal elements overlap, one or more embodiments thereby provide power distribution to functional circuit elements with less impact on routing of other connections to those functional circuit elements.

FIGS. **2**A, **2**B, and **2**C are diagrams of an IC structure **200**, in accordance with some embodiments. FIG. **2**A is a diagram based on a top view of a lower portion of IC structure **200**, FIG. **2**B is a diagram based on a top view of an upper portion of IC structure **200**, and FIG. **2**C is a diagram based on a cross-sectional view of IC structure **200** as intersected by plane B-B'. Metallization levels shown in IC structure **200** include power rail level **100**L (at which power rails **100**A and **100**B are located), first metal level **110**L, second metal level **120**L, and third metal level **130**L, described above with respect to IC structure **100** and FIGS. **1**A, **1**B, and **1**C. First direction X and second direction Y, described above with respect to IC structure **100** and FIG. **1**A, are indicated in FIG. **2**A.

In addition to the elements of IC structure **100**, IC structure **200** includes first metal segments **210**A, **210**B, **210**C, and **210**D positioned at first level **110**L, second metal segments **220**A, **220**B, **220**C, and **220**D positioned at second metal level **120**L, and third metal segments **230**A, **230**B, **230**C, and **230**D positioned at third metal level **130**L.

Each of first metal segments **210**A, **210**B, **210**C, and **210**D, second metal segments **220**A, **220**B, **220**C, and **220**D, and third metal segments **230**A, **230**B, **230**C, and **230**D comprises a conductive material such as a metal, a metal composite, or other suitable material that is formed in one or more metallization layers by one or more of a physical vapor deposition process, a chemical vapor deposition process, a plating process, or other suitable process.

First metal segments **210**A, **210**B, **210**C, and **210**D are electrically conductive line segments positioned in parallel at first metal level **110**L and oriented in second direction Y. First metal segments **210**A and **210**C overlap power rail **100**A, and first metal segments **210**B and **210**D overlap power rail **100**B. Each of first metal segments **210**A, **210**B, **210**C, and **210**D therefore overlaps only one of power rail **100**A or power rail **100**B and is also described as a metal stub. In some embodiments, first metal level **110**L corresponds to a metal stub level.

First metal segments **210**A, **210**B, **210**C, and **210**D are also described as a plurality of first metal segments or a plurality of metal stubs. In the embodiment shown in FIGS. **2**A, **2**B, and **2**C, a plurality of first metal segments includes four first metal segments. In some embodiments, a plurality of first metal segments includes first metal segments (not shown) in addition to first metal segments **210**A, **210**B, **210**C, and **210**D. In some embodiments, a plurality of first metal segments includes a subset of first metal segments **210**A, **210**B, **210**C, and **210**D.

In some embodiments, each first metal segment of a plurality of first metal segments has a width corresponding to a predetermined minimum width for first metal level **110**L. In some embodiments, each first metal segment of a plurality of first metal segments has a width corresponding to a predetermined minimum width for a metal one layer of an IC process.

First metal segments **210**A, **210**B, **210**C, and **210**D are positioned along tracks **212**A, **212**B, **212**C, and **212**D, respectively. The spacing of first metal segments **210**A, **210**B, **210**C, and **210**D is shown in FIG. **2**A as pitch **216**, the distance between tracks **212**A and **212**B. In some embodiments, pitch **216** is a multiple of a metal one pitch of an IC process that is the same as a poly pitch of the IC process. In some embodiments, pitch **216** is a multiple of a metal one pitch of an IC process that is different from a poly pitch of the IC process. In some embodiments, pitch **216** is a multiple of a metal one pitch of an IC process that ranges from four to 16. In some embodiments, pitch **216** is a multiple of a metal one pitch of an IC process that equals eight.

First vias **215** are vias positioned between power rail level **100**L and first metal level **110**L at locations at which first metal segments **210**A and **210**C overlap power rail **100**A, and at locations at which metal segments **210**B and **210**D overlap first power rail **100**B. In some embodiments, first vias **215** are single vias positioned at the locations at which first metal segments **210**A and **210**C overlap power rail **100**A, and the locations at which metal segments **210**B and **210**D overlap first power rail **100**B. By this configuration, first vias **215** electrically connect first metal segments **210**A and **210**C to power rail **100**A and electrically connect first metal segments **210**B and **210**D to power rail **100**B.

Second metal segments **220**A, **220**B, **220**C, and **220**D are electrically conductive line segments oriented in first direction X. Second metal segment **220**A overlaps power rail **100**A at the location at which first metal segment **210**A overlaps power rail **100**A, second metal segment **120**B overlaps power rail **100**B at the location at which first metal segment **210**B overlaps power rail **100**B, second metal segment **120**C overlaps power rail **100**A at the location at which first metal segment **210**C overlaps power rail **100**A, and second metal segment **220**D overlaps power rail **100**B at the location at which first metal segment **210**D overlaps power rail **100**B.

Second metal segments **220**A, **220**B, **220**C, and **220**D are also described as a plurality of second metal segments. In the embodiment shown in FIGS. **2**A, **2**B, and **2**C, a plurality of second metal segments includes four second metal segments. In some embodiments, a plurality of second metal segments includes second metal segments (not shown) in addition to second metal segments **220**A, **220**B, **220**C, and **220**D. In some embodiments, a plurality of second metal segments includes a subset of second metal segments **220**A, **220**B, **220**C, and **220**D.

In some embodiments, each second metal segment of a plurality of second metal segments has a width corresponding to a predetermined minimum width for second metal level **120**L. In some embodiments, each second metal segment of a plurality of second metal segments has a width corresponding to a predetermined minimum width for a metal two layer of an IC process.

Second vias **225** are vias positioned between first metal level **110**L and second metal level **120**L at locations above the locations at which first vias **215** are positioned. Thus, second vias **225** are positioned at the locations at which second metal segment **220**A overlaps first metal segment **210**A, second metal segment **220**B overlaps first metal segment **210**B, second metal segment **220**C overlaps first metal segment **210**C, and second metal segment **220**D overlaps first metal segment **210**D. In some embodiments, second vias **225** are single vias positioned at the locations above the locations at which first vias **215** are positioned.

By this configuration, second metal segment **220**A is electrically connected to first metal segment **210**A, second metal segment **220**B is electrically connected to first metal segment **210**B, second metal segment **220**C is electrically connected to first metal segment **210**C, and second metal segment **220**D is electrically connected to first metal segment **210**D.

Third metal segments **230**A, **230**B, **230**C, and **230**D are electrically conductive line segments positioned in parallel at third metal level **130**L and oriented in second direction Y.

Each of third metal segments **230**A, **230**B, **230**C, and **230**D overlaps both power rail **100**A and power rail **100**B and is also described as a metal strap. Third metal segments **230**A, **230**B, **230**C, and **230**D are also described as a plurality of third metal segments or a plurality of metal straps. In some embodiments, third metal level **130**L corresponds to a metal strap level.

Third metal segment **230**A overlaps second metal segment **220**A and power rail **100**A. Third metal segment **230**B overlaps second metal segment **220**B and power rail **100**B. Third metal segment **230**C overlaps second metal segment **220**C and power rail **100**A. Third metal segment **230**D overlaps second metal segment **220**D and power rail **100**B.

In the embodiment shown in FIGS. **2**A, **2**B, and **2**C, a plurality of third metal segments includes four third metal segments. In some embodiments, a plurality of third metal segments includes third metal segments (not shown) in addition to third metal segments **230**A, **230**B, **230**C, and **230**D. In some embodiments, a plurality of third metal segments includes a subset of third metal segments **230**A, **230**B, **230**C, and **230**D.

Third metal segments **230**A, **230**B, **230**C, and **230**D are positioned along tracks **232**A, **232**B, **232**C, and **232**D, respectively. In some embodiments, tracks **232**A, **232**B, **232**C, and **232**D align with tracks **212**A, **212**B, **212**C, and **212**D, respectively. In some embodiments, each track of tracks **232**A, **232**B, **232**C, and **232**D does not align with a corresponding track of tracks **212**A, **212**B, **212**C, and **212**D, but is sufficiently close to a corresponding track so that a corresponding third metal segment of third metal segments **230**A, **230**B, **230**C, and **230**D overlaps a corresponding first metal segment of first metal segments **210**A, **210**B, **210**C, and **210**D.

In some embodiments, each third metal segment of a plurality of third metal segments has a width corresponding to a predetermined minimum width for third metal level **130**L. In some embodiments, each third metal segment of a plurality of third metal segments has a width corresponding to a predetermined minimum width for a metal three layer of an IC process.

Third vias **235** are vias positioned between second metal level **120**L and third metal level **130**L at locations above the locations at which second vias **225** are positioned. Thus, third vias are positioned at the locations at which third metal segment **230**A overlaps second metal segment **220**A, third metal segment **230**B overlaps second metal segment **220**B, third metal segment **230**C overlaps second metal segment **220**C, and third metal segment **230**D overlaps second metal segment **220**D. In some embodiments, third vias **235** are single vias positioned at the locations above the locations at which second vias **225** are positioned. Third vias **235** are shown in FIG. **2**A, with one third via **235** labelled as an example.

By this configuration, third metal segment **230**A is electrically connected to second metal segment **220**A, third metal segment **230**B is electrically connected to second metal segment **220**B, third metal segment **230**C is electrically connected to second metal segment **220**C, and third metal segment **230**D is electrically connected to second metal segment **220**D.

In accordance with this configuration, third metal segments **230**A and **230**C are described as a first set of third metal segments, and third metal segments **230**B and **230**D are described as a second set of third metal segments. In the embodiment shown in FIGS. **2**A, **2**B, and **2**C, a set of third metal segments includes two third metal segments. In some embodiments, a set of third metal segments includes third metal segments (not shown) in addition to third metal segments **230**A, **230**B, **230**C, and **230**D.

Fourth vias **245** are vias positioned above third metal level **130**L at locations above the locations at which third vias **235** are positioned. As discussed below with respect to IC structure **500**, by this configuration, third metal segment **230**A is electrically connected to a fourth metal segment

540A, third metal segment **230**B is electrically connected to a fourth metal segment **540**B, third metal segment **230**C is electrically connected to a fourth metal segment **540**C, and third metal segment **230**D is electrically connected to a fourth metal segment **540**D. In some embodiments, fourth vias **245** are single vias positioned at the locations above the locations at which third vias **235** are positioned. Fourth vias **245** are shown in FIG. 2B, with one fourth via **245** labelled as an example.

The configuration of IC structure **200** in combination with IC structure **500** thereby establishes electrical connections between power straps positioned at upper metal layers and power rails at lower layers using minimum-width metal elements and, in some embodiments, single vias in the layers between the power straps and the power rails. By providing parallel paths having low resistance, one or more embodiments enable efficient power delivery, limited heat generation, and low susceptibility to EM.

In at least some embodiments, alternating strap and extended pitch configuration of the sets of third metal segments also facilitates routing of various electrical connections to functional circuits powered via the power rails.

Compared to approaches that use metal elements wider than minimum-width metal elements and/or multiple vias at locations where metal elements overlap, one or more embodiments thereby provide power distribution to functional circuit elements with less impact on routing of other connections to those functional circuit elements.

FIGS. **3**A, **3**B, and **3**C are diagrams of an IC structure **300**, in accordance with some embodiments. FIG. **3**A is a diagram based on a top view of a lower portion of IC structure **300**, FIG. **3**B is a diagram based on a top view of an upper portion of IC structure **300**, and FIG. **3**C is a diagram based on a cross-sectional view of IC structure **300** as intersected by plane C-C'. Metallization levels shown in IC structure **300** include power rail level **100**L (at which are located power rails **100**A and **100**B), first metal level **110**L, second metal level **120**L, and third metal level **130**L, described above with respect to IC structure **100** and FIGS. **1**A, **1**B, and **1**C. First direction X and second direction Y, described above with respect to IC structure **100** and FIG. **1**A, are indicated in FIG. **3**A.

In addition to the elements of IC structure **100**, IC structure **300** includes first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H positioned at first level **110**L, second metal segments **320**A and **320**B positioned at second metal level **120**L, and third metal segments **330**A, **330**B, **330**C, and **330**D positioned at third metal level **130**L.

Each of first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H, second metal segments **320**A and **320**B, and third metal segments **330**A, **330**B, **330**C, and **330**D comprises a conductive material such as a metal, a metal composite, or other suitable material that is formed in one or more metallization layers by one or more of a physical vapor deposition process, a chemical vapor deposition process, a plating process, or other suitable process.

First metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H are electrically conductive line segments positioned in parallel at first metal level **110**L and oriented in second direction Y. First metal segments **310**A, **310**C, **310**E, and **310**G overlap power rail **100**A, and first metal segments **310**B, **310**D, **310**F, and **310**H overlap power rail **100**B. Each of first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H therefore overlaps only one of power rail **100**A or power rail **100**B and is also described as a metal stub. In some embodiments, first metal level **110**L corresponds to a metal stub level.

First metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H are also described as a plurality of first metal segments or a plurality of metal stubs. In the embodiment shown in FIGS. **3**A, **3**B, and **3**C, a plurality of first metal segments includes eight first metal segments. In some embodiments, a plurality of first metal segments includes first metal segments (not shown) in addition to first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H. In some embodiments, a plurality of first metal segments includes a subset of first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H.

In some embodiments, each first metal segment of a plurality of first metal segments has a width corresponding to a predetermined minimum width for first metal level **110**L. In some embodiments, each first metal segment of a plurality of first metal segments has a width corresponding to a predetermined minimum width for a metal one layer of an IC process.

First metal segments **310**A and **310**B are positioned along track **312**A, first metal segments **310**C and **310**D are positioned along track **312**B, first metal segments **310**E and **310**F are positioned along track **312**C, and first metal segments **310**G and **310**H are positioned along track **312**D. The spacing of first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H is shown in FIG. **3**A as pitch **316**, the distance between tracks **312**A and **312**B. In some embodiments, pitch **316** is a multiple of a metal one pitch of an IC process that is the same as a poly pitch of the IC process. In some embodiments, pitch **316** is a multiple of a metal one pitch of an IC process that is different from a poly pitch of the IC process. In some embodiments, pitch **316** is a multiple of a metal one pitch of an IC process that ranges from four to 16. In some embodiments, pitch **316** is a multiple of a metal one pitch of an IC process that equals eight. In some embodiments, pitch **316** is a multiple of a metal one pitch of an IC process that equals twelve.

First vias **315** are vias positioned between power rail level **100**L and first metal level **110**L at locations at which first metal segments **310**A, **310**C, **310**E, and **310**G overlap power rail **100**A, and at locations at which metal segments **310**B, **310**D, **310**F, and **310**H overlap first power rail **100**B. In some embodiments, first vias **315** are single vias positioned at the locations at which first metal segments **310**A, **310**C, **310**E, and **310**G overlap power rail **100**A, and the locations at which first metal segments **310**B, **310**D, **310**F, and **310**H overlap first power rail **100**B. By this configuration, first vias **315** electrically connect first metal segments **310**A, **310**C, **310**E, and **310**G to power rail **100**A and electrically connect first metal segments **310**B, **310**D, **310**F, and **310**H to power rail **100**B.

Second metal segments **320**A and **320**B are electrically conductive line segments oriented in first direction X. Second metal segment **320**A overlaps power rail **100**A at the locations at which first metal segments **310**A, **310**C, **310**E, and **310**G overlap power rail **100**A, and second metal segment **320**B overlaps power rail **100**B at the locations at which first metal segments **310**B, **310**D, **310**F, and **310**H overlap power rail **100**B. Second metal segments **320**A and **320**B are also described as a plurality of second metal segments.

In some embodiments, each second metal segment of a plurality of second metal segments has a width corresponding to a predetermined minimum width for second metal level **120**L. In some embodiments, each second metal segment of a plurality of second metal segments has a width corresponding to a predetermined minimum width for a metal two layer of an IC process.

In some embodiments, each second metal segment of a plurality of second metal segments has a width greater than a predetermined minimum width for second metal level **120**L. In some embodiments, each second metal segment of a plurality of second metal segments has a width corresponding to two times a predetermined minimum width for second metal level **120**L.

In some embodiments, each second metal segment of a plurality of second metal segments has a width greater than a predetermined minimum width for a metal two layer of an IC process. In some embodiments, each second metal segment of a plurality of second metal segments has a width corresponding to two times a predetermined minimum width for a metal two layer of an IC process.

Second vias **325** are vias positioned between first metal level **110**L and second metal level **120**L at locations above the locations at which first vias **315** are positioned. Thus, second vias **325** are positioned at the locations at which second metal segment **320**A overlaps first metal segments **310**A, **310**C, **310**E, and **310**G, and at the locations at which second metal segment **320**B overlaps first metal segments **310**B, **310**D, **310**F, and **310**H. In some embodiments, second vias **325** are single vias positioned at the locations above the locations at which first vias **315** are positioned.

By this configuration, second metal segment **320**A is electrically connected to first metal segments **310**A, **310**C, **310**E, and **310**G, and second metal segment **320**B is electrically connected to first metal segments **310**B, **310**D, **310**F, and **310**H.

Third metal segments **330**A, **330**B, **330**C, and **330**D are electrically conductive line segments positioned in parallel at third metal level **130**L and oriented in second direction Y.

Each of third metal segments **330**A, **330**B, **330**C, and **330**D overlaps both of power rails **100**A and **100**B, both of second metal segments **320**A and **320**B, and is also described as a metal strap. Third metal segments **330**A, **330**B, **330**C, and **330**D are also described as a plurality of third metal segments or a plurality of metal straps. In some embodiments, third metal level **130**L corresponds to a metal strap level.

In the embodiment shown in FIGS. **3**A, **3**B, and **3**C, a plurality of third metal segments includes four third metal segments. In some embodiments, a plurality of third metal segments includes third metal segments (not shown) in addition to third metal segments **330**A, **330**B, **330**C, and **330**D. In some embodiments, a plurality of third metal segments includes a subset of third metal segments **330**A, **330**B, **330**C, and **330**D.

Third metal segments **330**A, **330**B, **330**C, and **330**D are positioned along tracks **332**A, **332**B, **332**C, and **332**D, respectively. In some embodiments, tracks **332**A, **332**B, **332**C, and **332**D align with tracks **312**A, **312**B, **312**C, and **312**D, respectively. In some embodiments, each track of tracks **332**A, **332**B, **332**C, and **332**D does not align with a corresponding track of tracks **312**A, **312**B, **312**C, and **312**D, but is sufficiently close to a corresponding track so that a corresponding third metal segment of third metal segments **330**A, **330**B, **330**C, and **330**D overlaps a corresponding pair of first metal segments of first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H.

The location at which third metal segment **330**A overlaps second metal segment **320**A corresponds to the location at which second metal segment **320**A overlaps first metal segment **310**A, the location at which third metal segment **330**B overlaps second metal segment **320**B corresponds to the location at which second metal segment **320**B overlaps first metal segment **310**D, the location at which third metal segment **330**C overlaps second metal segment **320**A corresponds to the location at which second metal segment **320**A overlaps first metal segment **310**E, and the location at which third metal segment **330**D overlaps second metal segment **320**B corresponds to the location at which second metal segment **320**B overlaps first metal segment **310**F.

In some embodiments, each third metal segment of a plurality of third metal segments has a width corresponding to a predetermined minimum width for third metal level **130**L. In some embodiments, each third metal segment of a plurality of third metal segments has a width corresponding to a predetermined minimum width for a metal three layer of an IC process.

Third vias **335** are vias positioned between second metal level **120**L and third metal level **130**L at locations above a subset of the locations at which second vias **325** are positioned. Accordingly, third vias are positioned at the locations at which third metal segment **330**A overlaps second metal segment **320**A, third metal segment **330**B overlaps second metal segment **320**B, third metal segment **330**C overlaps second metal segment **320**A, and third metal segment **330**D overlaps second metal segment **320**B. In some embodiments, third vias **335** are single vias positioned at the locations above a subset of the locations at which second vias **325** are positioned. Third vias **335** are shown in FIG. **3**A, with one third via **335** labelled as an example.

By this configuration, third metal segments **330**A and **330**C are electrically connected to second metal segment **320**A, and third metal segments **330**B and **330**D are electrically connected to second metal segment **320**B.

In accordance with this configuration, third metal segments **330**A and **330**C are described as a first set of third metal segments, and third metal segments **330**B and **330**D are described as a second set of third metal segments. In the embodiment shown in FIGS. **3**A, **3**B, and **3**C, a set of third metal segments includes two third metal segments. In some embodiments, a set of third metal segments includes third metal segments (not shown) in addition to third metal segments **330**A, **330**B, **330**C, and **330**D.

Fourth vias **345** are vias positioned above third metal level **130**L at locations above the locations at which third vias **335** are positioned. As discussed below with respect to IC structure **500**, by this configuration, third metal segment **330**A is electrically connected to a fourth metal segment **540**A, third metal segment **330**B is electrically connected to a fourth metal segment **540**B, third metal segment **330**C is electrically connected to a fourth metal segment **540**C, and third metal segment **330**D is electrically connected to a fourth metal segment **540**D. In some embodiments, fourth vias **345** are single vias positioned at the locations above the locations at which third vias **335** are positioned. Fourth vias **345** are shown in FIG. **3**B, with one fourth via **345** labelled as an example.

The configuration of IC structure **300** in combination with IC structure **500** thereby establishes electrical connections between power straps positioned at upper metal layers and power rails at lower layers using minimum-width metal stubs and straps and, in some embodiments, single vias in the layers between the power straps and the power rails. By providing parallel paths having low resistance, particularly between power rails and second metal segments, one or more embodiments enable efficient power delivery, limited heat generation, and low susceptibility to EM.

In at least some embodiments, alternating strap and extended pitch configuration of the sets of third metal segments also facilitates routing of various electrical connections to functional circuits powered via the power rails.

Compared to approaches that use metal elements wider than minimum-width metal elements and/or multiple vias at locations where metal elements overlap, one or more embodiments thereby provide power distribution to functional circuit elements with less impact on routing of other connections to those functional circuit elements.

FIGS. **4**A and **4**B are diagrams of an IC structure **400**, in accordance with some embodiments. FIG. **4**A is a diagram based on a top view of a lower portion of IC structure **400** and FIG. **4**B is a diagram based on a cross-sectional view of IC structure **400** as intersected by plane D-D'. IC structure **400** includes power rails **100**A and **100**B, power rail level **100**L, first metal level **110**L, second metal level **120**L, and third metal level **130**L, described above with respect to IC structure **100** and FIGS. **1**A, **1**B, and **1**C. IC structure **400** also includes first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H, second metal segments **320**A and **320**B, and third metal segments **330**A, **330**B, **330**C, and **330**D, described above with respect to IC structure **300** and FIGS. **3**A, **3**B, and **3**C. First direction X and second direction Y, described above with respect to IC structure **100** and FIG. **1**A, are indicated in FIG. **4**A.

In addition to the elements of IC structures **100** and **300**, IC structure **400** includes first metal segments **410**A and **410**B positioned at first level **110**L. Each of first metal segments **410**A and **410**B comprises a conductive material such as a metal, a metal composite, or other suitable material that is formed in one or more metallization layers by one or more of a physical vapor deposition process, a chemical vapor deposition process, a plating process, or other suitable process.

First metal segments **410**A are electrically conductive line segments positioned at first metal level **110**L in parallel with and between first metal segments **310**A, **310**C, **310**E, and **310**G. First metal segments **410**A overlap power rail **100**A and do not overlap power rail **100**B.

First metal segments **410**B are electrically conductive line segments positioned at first metal level **110**L in parallel with and between first metal segments **310**B, **310**D, **310**F, and **310**H. First metal segments **410**B overlap power rail **100**B and do not overlap power rail **100**A.

First metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, **310**H, **410**A, and **410**B are also described as a plurality of first metal segments or a plurality of metal stubs. In the embodiment shown in FIGS. **4**A and **4**B, a plurality of first metal segments includes three first metal segments **410**A between each of two first metal segments **310**A, **310**C, **310**E, and **310**G, and three first metal segments **410**B between each of two first metal segments **310**B, **310**D, **310**F, and **310**H.

In some embodiments, a plurality of first metal segments includes fewer than three first metal segments **410**A between each of two first metal segments **310**A, **310**C, **310**E, and **310**G. In some embodiments, a plurality of first metal segments includes greater than three first metal segments **410**A between each of two first metal segments **310**A, **310**C, **310**E, and **310**G.

In some embodiments, a plurality of first metal segments includes fewer than three first metal segments **410**B between each of two first metal segments **310**B, **310**D, **310**F, and **310**H. In some embodiments, a plurality of first metal segments includes greater than three first metal segments **410**B between each of two first metal segments **310**B, **310**D, **310**F, and **310**H.

The locations at which third metal segments **330**A and **330**C overlap second metal segment **320**A are a subset of the locations at which second metal segment **320**A overlaps first metal segments **310**A, **310**C, **310**E, **310**G, and **410**A, and the locations at which third metal segments **330**B and **330**D overlap second metal segment **320**B are a subset of the locations at which second metal segment **320**B overlaps first metal segments **310**B, **310**D, **310**F, **310**H, and **410**B.

In some embodiments, each first metal segment of a plurality of first metal segments has a width corresponding to a predetermined minimum width for first metal level **110**L. In some embodiments, each first metal segment of a plurality of first metal segments has a width corresponding to a predetermined minimum width for a metal one layer of an IC process.

First vias **315** are vias positioned between power rail level **100**L and first metal level **110**L at locations at which first metal segments **310**A, **310**C, **310**E, **310**G, and **410**A overlap power rail **100**A, and at locations at which metal segments **310**B, **310**D, **310**F, **310**H, and **410**B overlap first power rail **100**B. In some embodiments, first vias **315** are single vias positioned at the locations at which first metal segments **310**A, **310**C, **310**E, **310**G, and **410**A overlap power rail **100**A, and the locations at which metal segments **310**B, **310**D, **310**F, **310**H, and **410**B overlap first power rail **100**B. By this configuration, first vias **315** electrically connect first metal segments **310**A, **310**C, **310**E, **310**G, and **410**A to power rail **100**A and electrically connect first metal segments **310**B, **310**D, **310**F, **310**H, and **410**B to power rail **100**B.

Second vias **325** are vias positioned between first metal level **110**L and second metal level **120**L at locations above the locations at which first vias **315** are positioned. Thus, second vias **325** are positioned at the locations at which second metal segment **420**A overlaps first metal segments **310**A, **310**C, **310**E, **310**G, and **410**A, and at the locations at which second metal segment **420**B overlaps first metal segments **310**B, **310**D, **310**F, **310**H, and **410**B. In some embodiments, second vias **325** are single vias positioned at the locations above the locations at which first vias **315** are positioned.

By this configuration, second metal segment **420**A is electrically connected to first metal segments **310**A, **310**C, **310**E, **310**G, and **410**A, and second metal segment **420**B is electrically connected to first metal segments **310**B, **310**D, **310**F, **310**H, and **410**B.

The configuration of IC structure **400** in combination with IC structure **500** thereby establishes electrical connections between power straps positioned at upper metal layers and power rails at lower layers using minimum-width metal stubs and straps and, in some embodiments, single vias in the layers between the power straps and the power rails. By providing parallel paths having low resistance, particularly between power rails and second metal segments, one or more embodiments enable efficient power delivery, limited heat generation, and low susceptibility to EM.

In at least some embodiments, alternating strap and extended pitch configuration of the sets of third metal segments also facilitates routing of various electrical connections to functional circuits powered via the power rails.

Compared to approaches that use metal elements wider than minimum-width metal elements and/or multiple vias at locations where metal elements overlap, one or more embodiments thereby provide power distribution to functional circuit elements with less impact on routing of other connections to those functional circuit elements.

FIGS. **5**A and **5**B are diagrams of an IC structure **500**, in accordance with some embodiments. FIG. **5**A is a diagram based on a top view of IC structure **500**, and FIG. **5**B is a diagram based on a cross-sectional view of IC structure **500** as intersected by plane E-E'. IC structure **500** includes power rails **100**A and **100**B, power rail level **100**L, first metal level **110**L, second metal level **120**L, and third metal level **130**L, described above with respect to IC structure **100** and FIGS. **1**A, **1**B, and **1**C. First direction X and second direction Y, described above with respect to IC structure **100** and FIG. **1**A, are indicated in FIG. **5**A.

In addition to the elements of IC structure **100**, IC structure **500** includes fourth metal segments **540**A, **540**B, **540**C, and **540**D positioned at a fourth metal level **540**L and power straps **550**A, **550**B, **550**C, and **550**D positioned at a power strap level **550**L.

In some embodiments, fourth metal level **540**L is immediately above third metal level **130**L. In some embodiments, one or more metal levels (not shown) separate fourth metal level **540**L from third metal level **130**L and fourth metal level **540**L is not immediately above third metal level **130**L.

In some embodiments, power strap level **550**L is immediately above fourth metal level **540**L. In some embodiments, one or more metal levels (not shown) separate power strap level **550**L from fourth metal level **540**L and power strap level **550**L is not immediately above fourth metal level **540**L.

Each of fourth metal segments **540**A, **540**B, **540**C, and **540**D and power straps **550**A, **550**B, **550**C, and **550**D comprises a conductive material such as a metal, a metal composite, or other suitable material that is formed in one or more metallization layers by one or more of a physical vapor deposition process, a chemical vapor deposition process, a plating process, or other suitable process.

Fourth metal segments **540**A, **540**B, **540**C, and **540**D are electrically conductive line segments positioned in parallel at fourth metal level **540**L and oriented in first direction X. Fourth metal segments **540**A and **540**C overlap power rail **100**A, and fourth metal segments **540**B and **540**D overlap power rail **100**B.

Fourth metal segments **540**A, **540**B, **540**C, and **540**D are also described as a plurality of fourth metal segments. In the embodiment shown in FIGS. **5**A and **5**B, a plurality of fourth metal segments includes four fourth metal segments. In some embodiments, a plurality of fourth metal segments includes fourth metal segments (not shown) in addition to fourth metal segments **540**A, **540**B, **540**C, and **540**D. In some embodiments, a plurality of fourth metal segments includes a subset of fourth metal segments **540**A, **540**B, **540**C, and **540**D.

In some embodiments, each fourth metal segment of a plurality of fourth metal segments has a width corresponding to a predetermined minimum width for fourth metal level **540**L. In some embodiments, each fourth metal segment of a plurality of fourth metal segments has a width corresponding to a predetermined minimum width for a metal four layer of an IC process.

In some embodiments, fourth metal segment **540**A overlaps third metal segments **130**A and **130**B, fourth metal segment **540**B overlaps third metal segments **130**C and **130**D, fourth metal segment **540**C overlaps third metal segments **130**E and **130**F, and fourth metal segment **540**D overlaps third metal segments **130**G and **130**H, described above with respect to IC structure **100** and FIGS. **1**A, **1**B, and **1**C. In this configuration, fourth vias **145** electrically connect fourth metal segment **540**A to third metal segments **130**A and **130**B, fourth metal segment **540**B to third metal segments **130**C and **130**D, fourth metal segment **540**C to third metal segments **130**E and **130**F, and fourth metal segment **540**D to third metal segments **130**G and **130**H.

In some embodiments, fourth metal segment **540**A overlaps third metal segment **230**A, fourth metal segment **540**B overlaps third metal segment **230**B, fourth metal segment **540**C overlaps third metal segment **230**C, and fourth metal segment **540**D overlaps third metal segment **230**D, described above with respect to IC structure **200** and FIGS. **2**A, **2**B, and **2**C. In this configuration, fourth vias **245** electrically connect fourth metal segment **540**A to third metal segment **230**A, fourth metal segment **540**B to third metal segment **230**B, fourth metal segment **540**C to third metal segment **230**C, and fourth metal segment **540**D to third metal segment **230**D.

In some embodiments, fourth metal segment **540**A overlaps third metal segment **330**A, fourth metal segment **540**B overlaps third metal segment **330**B, fourth metal segment **540**C overlaps third metal segment **330**C, and fourth metal segment **540**D overlaps third metal segment **330**D, described above with respect to IC structure **300** and FIGS. **3**A, **3**B, and **3**C. In this configuration, fourth vias **345** electrically connect fourth metal segment **540**A to third metal segment **330**A, fourth metal segment **540**B to third metal segment **330**B, fourth metal segment **540**C to third metal segment **330**C, and fourth metal segment **540**D to third metal segment **330**D.

Power straps **550**A, **550**B, **550**C, and **550**D are electrically conductive line segments oriented in second direction Y. Power strap **550**A overlaps power rail **100**A at the location at which fourth metal segment **540**A overlaps power rail **100**A, power strap **550**B overlaps power rail **100**B at the location at which fourth metal segment **540**B overlaps power rail **100**B, power strap **550**C overlaps power rail **100**A at the location at which fourth metal segment **540**C overlaps power rail **100**A, and power strap **550**D overlaps power rail **100**B at the location at which fourth metal segment **540**D overlaps power rail **100**B.

Power straps **550**A, **550**B, **550**C, and **550**D are also described as a plurality of power straps. In the embodiment shown in FIGS. **5**A and **5**B, a plurality of power straps includes four power straps. In some embodiments, a plurality of power straps includes power straps (not shown) in addition to power straps **550**A, **550**B, **550**C, and **550**D. In some embodiments, a plurality of power straps includes a subset of power straps **550**A, **550**B, **550**C, and **550**D.

In some embodiments, each power strap of a plurality power straps has a width corresponding to two times a predetermined minimum width for power strap level **550**L. In some embodiments, each power strap of a plurality power straps has a width greater than two times a predetermined minimum width for power strap level **550**L

In some embodiments, each power strap of a plurality of power straps has a width corresponding to two times a predetermined minimum width for a metal five layer of an IC process. In some embodiments, each power strap of a plurality of power straps has a width greater than two times a predetermined minimum width for a metal five layer of an IC process.

Fifth vias **555** are vias positioned between fourth metal level **540**L and power strap level **550**L at the locations at which power strap **550**A overlaps fourth metal segment **540**A, power strap **550**B overlaps fourth metal segment **540**B, power strap **550**C overlaps fourth metal segment **540**C, and power strap **550**D overlaps fourth metal segment **540**D. In some embodiments, fifth vias **555** are single vias positioned at the locations at which power strap **550**A overlaps fourth metal segment **540**A, power strap **550**B overlaps fourth metal segment **540**B, power strap **550**C overlaps fourth metal segment **540**C, and power strap **550**D overlaps fourth metal segment **540**D.

By this configuration, power strap **550**A is electrically connected to fourth metal segment **540**A, power strap **550**B is electrically connected to fourth metal segment **540**B, power strap **550**C is electrically connected to fourth metal segment **540**C, and power strap **550**D is electrically connected to fourth metal segment **540**D.

By the configuration of IC structure **500** in combination with any one of IC structure **100**, IC structure **200**, IC structure **300**, or IC structure **400**, power strap **550**A is electrically connected to power rail **100**A, power strap **550**B is electrically connected to power rail **100**B, power strap **550**C is electrically connected to power rail **100**A, and power strap **550**D is electrically connected to power rail **100**B.

FIG. **6** is a flowchart of a method **600** of forming an IC structure, in accordance with one or more embodiments. Method **600** is implemented to one or more of manufacture or design an IC structure such as one or more of IC structures **100**, **200**, **300**, **400**, and **500**, discussed above. If method **600** is performed to design an IC structure, method **600** is implemented by a processor configured to execute a set of computer-readable instructions that interface with a circuit design system to design and render a layout of an IC structure having the features discussed herein.

The sequence in which the operations of method **600** are depicted in FIG. **6** is for illustration only; the operations of method **600** are capable of being executed in sequences that differ from that depicted in FIG. **6**. In some embodiments, operations in addition to those depicted in FIG. **6** are performed before, between and/or after the operations depicted in FIG. **6**.

At operation **610**, a first power rail and a second power rail are formed. The first power rail and the second power rail are positioned in parallel at a power rail level and are oriented in a power rail direction.

In some embodiments, forming a first power rail and a second power rail includes forming first power rails **100**A and **100**B, discussed above with respect to IC structures **100**, **200**, **300**, and **400**.

At operation **620**, a plurality of first metal segments is formed at a first metal level immediately above the power rail level. The plurality of first metal segments includes first metal segments oriented in a first metal direction perpendicular to the power rail direction. Each first metal segment of the plurality of first metal segments overlaps one or both of the first power rail or the second power rail. Forming the plurality of first metal segments comprises forming each first metal segment of the plurality of first metal segments having a width corresponding to a predetermined minimum width for the first metal level.

In some embodiments, forming a plurality of first metal segments includes forming first metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H, discussed above with respect to IC structure **100**. In some embodiments, forming a plurality of first metal segments includes forming first metal segments **210**A, **210**B, **210**C, and **210**D, discussed above with respect to IC structure **200**. In some embodiments, forming a plurality of first metal segments includes forming first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H, discussed above with respect to IC structure **300**. In some embodiments, forming a plurality of first metal segments includes forming first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, **310**H, **410**A, and **410**B, discussed above with respect to IC structure **400**.

At operation **630**, a plurality of first vias is formed between the power rail level and the first metal level. Each via of the plurality of first vias is a single via positioned at a location where a corresponding first metal segment of the plurality of first metal segments overlaps the first power rail or the second power rail.

In some embodiments, forming a plurality of first vias includes forming plurality of first vias **115** between power rails **100**A and **100**B and first metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H, discussed above with respect to IC structure **100**. In some embodiments, forming a plurality of first vias includes forming plurality of first vias **215** between power rails **100**A and **100**B and first metal segments **210**A, **210**B, **210**C, and **210**D, discussed above with respect to IC structure **200**. In some embodiments, forming a plurality of first vias includes forming plurality of first vias **315** between power rails **100**A and **100**B and first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H, discussed above with respect to IC structure **300**. In some embodiments, forming a plurality of first vias includes forming plurality of first vias **315** between power rails **100**A and **100**B and first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, **310**H, **410**A, and **410**B, discussed above with respect to IC structure **400**.

At operation **640**, a plurality of second metal segments is formed at a second metal level immediately above the first metal level. Each second metal segment of the plurality of second metal segments is oriented in the power rail direction, at least one second metal segment of the plurality of second metal segments overlaps the first power rail, and at least one second metal segment of the plurality of second metal segments overlaps the second power rail.

In some embodiments, forming a plurality of second metal segments comprises forming second metal segments **120**A, **120**B, **120**C, and **120**D, discussed above with respect to IC structure **100**. In some embodiments, forming a plurality of second metal segments comprises forming second metal segments **220**A, **220**B, **220**C, and **220**D, discussed above with respect to IC structure **200**. In some embodiments, forming a plurality of second metal segments comprises forming second metal segments **320**A and **320**B, discussed above with respect to IC structures **300** and **400**.

At operation **650**, a plurality of second vias is formed between the first metal level and the second metal level. Each second via of the plurality of second vias is a single via formed at a location above a corresponding first via of the plurality of first vias.

In some embodiments, forming a plurality of second vias includes forming plurality of second vias **125** between first metal segments **110**A, **110**B, **110**C, **110**D, **110**E, **110**F, **110**G, and **110**H and second metal segments **120**A, **120**B, **120**C, and **120**D, discussed above with respect to IC structure **100**. In some embodiments, forming a plurality of second vias includes forming plurality of second vias **225** between first metal segments **210**A, **210**B, **210**C, and **210**D and second layer of metal segments **220**A, **220**B, **220**C, and **220**D, discussed above with respect to IC structure **200**. In some embodiments, forming a plurality of second vias includes forming plurality of second vias **325** between first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, and **310**H and second layer of metal segments **320**A and **320**B, discussed above with respect to IC structure **300**. In some embodiments, forming a plurality of second vias includes forming plurality of second vias **325** between first metal segments **310**A, **310**B, **310**C, **310**D, **310**E, **310**F, **310**G, **310**H, **410**A, and **410**B and second layer of metal segments **320**A and **320**B, discussed above with respect to IC structure **400**.

At operation **660**, a first power strap and a second power strap are formed at a power strap level above the second metal level. Forming the first power strap comprises forming the first power strap having a width greater than a predetermined minimum width for the power strap level. Forming the second power strap comprises forming the second power strap having the width greater than the predetermined minimum width for the power strap level. In some embodiments, forming a first power strap and a second power strap includes forming power straps **550**A, **550**B, **550**C, and **550**D, discussed above with respect to IC structure **500**.

Operations **610**-**660** thereby establish an electrical connection from the first power strap to the first power rail and from the second power strap to the second power rail. In some embodiments, establishing an electrical connection from the first power strap to the first power rail and from the second power strap to the second power rail includes operations in addition to operations **610**-**660**.

In some embodiments, at operation **670**, a plurality of third metal segments is formed at a third metal level immediately above the second metal level. The plurality of third metal segments is oriented in the first metal level direction. In some embodiments, a plurality of third metal segments includes a first set of third metal segments alternating with a second set of third metal segments.

In some embodiments, forming a plurality of third metal segments comprises forming third metal segments **130**A, **130**B, **130**C, **130**D, **130**E, **130**F, **130**G, and **130**H, discussed above with respect to IC structure **100**. In some embodiments, forming a plurality of third metal segments comprises forming third layer of metal segments **230**A, **230**B, **230**C, and **230**D, discussed above with respect to IC structure **200**. In some embodiments, forming a plurality of third metal segments comprises forming third layer of metal segments **330**A, **330**B, **330**C, and **330**D, discussed above with respect to IC structures **300** and **400**.

In some embodiments, operation **680** includes forming a plurality of third vias. In some embodiments, a plurality of third vias electrically connects a first set of third metal segments to at least one second metal segment of a plurality of second metal segments overlapping a first power rail and electrically connects a second set of third metal segments to at least one second metal segment of the plurality of second metal segments overlapping a second power rail. In some embodiments, at operation **690**, a new set of masks is generated based on the results of operations **610**-**680**.

In some embodiments, forming a plurality of third vias includes forming third vias **135**, discussed above with respect to IC structure **100**. In some embodiments, forming a plurality of third vias includes forming third vias **235**, discussed above with respect to IC structure **200**. In some embodiments, forming a plurality of third vias includes forming third vias **335**, discussed above with respect to IC structures **300** and **400**.

Each of the various embodiments thereby establishes electrical connections between components of the power grid (which include power straps positioned at upper metal layers and power rails at lower layers using minimum-width metal elements and single vias in the layers between the power straps and the power rails) and thereby reduces IR losses, reduces an area/footprint impact of the power-grid (which increases space available for placement of other structures), or the like. By providing parallel paths having low resistance, one or more embodiments enable efficient power delivery, limited heat generation, and low susceptibility to EM.

Compared to approaches that use metal elements wider than minimum-width metal elements and/or multiple vias at locations where metal elements overlap, one or more embodiments provide power distribution to functional circuit elements with less impact on routing of other connections to those functional circuit elements.

FIG. **7** is a block diagram of an IC structure **700**, in accordance with at least one embodiment of the present disclosure.

In FIG. **7**, IC structure **700** includes, among other things, a circuit macro/module **701**. In some embodiments, circuit macro/module **701** is understood in the context of an analogy to the architectural hierarchy of modular programming in which subroutines/procedures are called by a main program (or by other subroutines) to carry out a given computational function. In this context, IC structure **700** uses circuit macro/module **701** to form one or more given functions. Accordingly, in this context and in terms of architectural hierarchy, IC structure **700** is analogous to the main program and circuit macro/module (hereinafter, macro) **701** is analogous to subroutines/procedures. In some embodiments, macro **701** is a soft macro. In some embodiments, macro **701** is a hard macro. In some embodiments, macro **701** is a soft macro which is described/couched in register-transfer level (RTL) code. In some embodiments, synthesis, placement and routing have yet to have been performed on macro **701** such that the soft macro can be synthesized, placed and routed for a variety of process nodes. In some embodiments, macro **701** is a hard macro which is described/couched in a binary file format (e.g., Graphic Database System II (GDSII) stream format), where the binary file format represents planar geometric shapes, text labels, other information and the like of one or more layout diagrams of macro **701** in hierarchical form. In some embodiments, synthesis, placement and routing have been performed on macro **701** such that the hard macro is specific to a particular process node.

In some embodiments, macro **701** is an SRAM macro. In some embodiments, macro **701** is another macro such as another type of RAM, a ROM, phase lock loops (PLLs), special function circuits, or the like. Macro **701** includes, among other things, a conductive line region **702**. In some embodiments, region **702** corresponds to a part of or an entirety of an instance of a standard cell structure, where the standard cell structure is included in a library of various standard cell structures.

FIG. **8**A is a layout diagram **800**A of a conductive line structure **800**A of an IC structure, in accordance with at least one embodiment of the present disclosure. In some embodiments, the IC structure is IC structure **700** of FIG. **7**. Layout diagram **800**A includes an example of a connected long pillar pair configuration.

In terms of arrangement, FIG. **8**A is arranged into an array of rows (including rows ROW**1**-ROW**8**) and columns (including COL**1**-COL**4**). Each of the rows is arranged to be substantially parallel to a first direction. Relative to a second direction (which is substantially perpendicular to the first direction), each of rows ROW**1**-ROW**8** has a height H_{ROW}. In FIG. **8**A, the first and second directions are the corresponding vertical and horizontal. In some embodiments, the first and second directions are corresponding directions other than the vertical and horizontal directions. In some embodiments, each of the rows includes a predetermined number of the reference lines/tracks (not shown in FIG. **8**A). In some embodiments, odd-numbered rows have a first conductivity and even-numbered rows have a second conductivity. In some embodiments, the odd-numbered rows are configured for PMOS technology and the even-numbered rows are configured for NMOS technology. In some embodiments, the odd-numbers rows are configured for NMOS technology and the even-numbered rows are configured for PMOS technology.

Layout diagram **800**A includes sets of long pillar patterns, sets of short pillar patterns; and first via patterns **830**. In particular, the sets of long pillar patterns include: first set **802** of long pillar patterns **804**A-**804**B; a second set **806** of long pillar patterns **808**A-**808**B; a fourth set **810** of long pillar patterns **812**A-**812**B; and a fifth set **814** of long pillar patterns **816**A-**816**B. In particular, the short pillar patterns include: a third **818** of short pillar patterns **820**A-**820**D; and a sixth set **824** of short pillar patterns **826**A-**826**D. In FIG. **8**A, each column is shown as a group of sets which includes two sets. For example, column COL**1** includes first set **802** of long pillar patterns **804**A-**804**B and second set **806** of long pillar patterns **808**A-**808**B, and column COL**2** includes fourth set **810** of long pillar patterns **812**A-**812**B and fifth set **814** of long pillar patterns **816**A-**816**B. In some embodiments, each column includes a group of sets which has a number of sets other than two. Via patterns **830** electrically connect short pillar patterns **820**A-**820**D and **826**A-**826**D of corresponding third **818** and sixth **824** sets with corresponding ones of long pillar patterns **804**A-**804**B, **808**A-**808**B, **812**A-**812**B and **816**A-**816**B of corresponding first set **802**, second **806** set, fourth set **810** and fifth set **814**.

Members of first set **804**, second set **806**, fourth set **810**, fifth set **814**, and the like are located in a M(i) metallization layer, where i is a non-negative integer. Members of third set **818**, sixth set **824**, and the like are located in an M(i+1) metallization layer. In some embodiments, i=0. In some embodiments, i=1. In some embodiments, values of i other than i=0 or i=1 are contemplated.

Regarding members of each of first set **802**, second set **806**, fourth set **810** and fifth set **814** of long pillar patterns, they: are substantially the same length; are non-overlapping of each other; and have long axes which are substantially coaxial and substantially parallel to the first direction. In some embodiments, the first direction is the vertical direction. In some embodiments, amongst the long pillars (including long pillars **804**A-**804**B, **808**A-**808**B, **812**A-**812**B and **816**A-**816**B, not all of the long pillars are substantially the same length.

In terms of offsets, offsets shown in FIG. **8**A include paired-set offsets in the second/horizontal direction, paired-set offsets in the first/vertical direction and intra-column offsets in the first/vertical direction. A paired-set offset in the second/horizontal direction occurs between horizontally-adjacent sets of long pillars. A paired-set offset in the first/vertical direction occurs between horizontally-adjacent sets. An inter-column offset in the first direction occurs between the sets of long pillars in a first column and the sets of long pillars in an adjacent second column.

An example of the paired-set offset in the second/horizontal direction is that second set **806** is offset in the second direction relative to first set **802** by an offset distance, D_{OFF1}. Fifth set **814** is offset in the second direction relative to fourth set **810** by the offset distance, D_{OFF1}. In some embodiments, offset distance D_{OFF1} is the poly pitch, P_{POLY}, for the corresponding process node, where $D_{OFF1}=P_{POLY}$. In some embodiments, other values of D_{OFF1} are contemplated. Also, pairs of first set **802** & fourth set **810**, second set **806** & fourth set **814**, and the like, are offset in the second direction relative to each other by an offset distance, D_{OFF2}. Adjacent columns are offset in the second direction relative to each other by an offset distance, D_{OFF2}. In FIG. **8**A, offset distance D_{OFF2} is an approximately six times multiple of offset distance D_{OFF1} such that $D_{OFF2}\approx 6*D_{OFF1}$. In some embodiments, offset distance D_{OFF2} is approximate multiple of offset distance D_{OFF1} other than an approximately six time multiple. In some embodiments, D_{OFF2} is one-half of the power pitch, P_v, between adjacent power rails or stripes for the corresponding process node, where $D_{OFF2}=\frac{1}{2}P_v$. In some embodiments, other values of D_{OFF2} are contemplated.

In terms of sizes shown in FIG. **8**A, each of long pillar patterns **804**A-**804**B, **808**A-**808**B, **810**A-**810**B, **816**A-**816**B and the like has a length, L, less than or equal to a predetermined length, L_{LIMIT}, where $L\leq L_{LIMIT}$. In some embodiments, L_{LIMIT} is substantially equal to, albeit without being greater than, the Blech length, L_{Blech}, where $L_{LIMIT}\approx L_{Blech}$ AND $L_{LIMIT}\leq L_{Blech}$. It is noted that L_{Blech} represents a length of conductor below which substantially no electromigration occurs. In some embodiments, L_{LIMIT} is a length other than Blech length, L_{Blech}.

An example of the paired-set offset in the first/vertical direction between horizontally-adjacent sets of long pillar patterns is that second set **806** (which is horizontally-adjacent to first set **802**) is offset in the first/vertical direction by a vertical-separation distance of substantially one row height H_{ROW} relative to first set **802**. More particularly regarding the example, long pillar pattern **804**B in first set **802** is offset by a vertical-separation distance of substantially four row heights H_{ROW} relative to long pillar pattern **808**A in second set **806**. In some embodiments, the paired-set offset in the first/vertical direction has vertical-separation distance different than one row height H_{ROW}.

An example of an inter-column offset in the first/vertical direction between the sets of long pillars in a first column and the sets of long pillar patterns in an adjacent second column is that is first set **802** and second set **806** of long pillar patterns in column COL**1** are offset in the first/vertical direction by a vertical-separation distance of substantially one row height H_{ROW} relative to fourth set **810** and fifth set **814** of long pillar patterns in column COL**2**. More particularly regarding the example, long pillar pattern **812**B in fourth set **810** of column COL**2** is offset by a vertical-separation distance of substantially one row height H_{ROW} relative to long pillar pattern **804**B in first set **802** of column COL**1**, and long pillar pattern **816**A in fifth set **814** of column COL**2** is offset by a vertical-separation distance of substantially one row height H_{ROW} relative to long pillar pattern **808**A in second set **806** of column COL**1**. In some embodiments, the inter-column offset in the first/vertical direction has vertical-separation distance different than one row height H_{ROW}.

In FIG. **8**A, the short pillar patterns **820**A-**820**D, **826**A-**826**D and the like are organized into according to rows ROW**1**-ROW**8** and the like. Regarding members of each of third set third set **818** and sixth set **824** of short pillar patterns, they: are non-overlapping of each other; have long axes which are substantially parallel to the second direction; are overlapping of corresponding long pillar patterns **804**A-**804**B, **808**A-**808**B, **812**A-**812**B and **816**A-**816**B in corresponding first set **802**, second set **806**, fourth set **810** and fifth set **814**; and are organized into groups. Members of third set **818** are aligned with each other relative to the first direction. Members of sixth set **824** are aligned with each other relative to the first direction. Adjacent members of third set **818** are offset in the first direction relative to each other by an offset distance, D_{OFF3}. In FIG. **8**A, D_{OFF3} is the size in the first direction of two rows. In some embodiments, D_{OFF3} is a multiple of the size, D_{SS}, in the first direction of a standard cell, where $D_{OFF3}=\alpha*D_{SS}$, and where α is a positive real number. In some embodiments, other values of D_{OFF3} are contemplated.

Furthermore, third set **818** of short pillar patterns is organized into groups **822**A-**822**B, and sixth set **824** of short pillar patterns is organized into groups **828**A-**828**B. Each of groups **822**A-**822**B and **828**A-**828**B has the same quantity, Q_{822}, of short pillar patterns **820**A-**820**D. In FIG. **8**A, for simplicity of illustration, quantity Q_{822} of short pillar patterns is shown as two, $Q_{822}=2$. In some embodiments, other values for Q_{822} are contemplated, where Q_{822} is a positive integer and Q**822**>2.

Each group **822**A-**822**B of third set **818** overlaps and is electrically connected between a corresponding pair of one of long pillar patterns **804**A-**804**B in first set **802** and a corresponding one of long pillar patterns **808**A-**808**B in second set **806**. An example of such a pair is long pillar pattern **804**B in first set **802** and long pillar pattern **808**A in second set **806**. Accordingly, in each of groups **822**A-**822**B, each of corresponding short pillar patterns **820**A-**820**D overlaps and is electrically connected between the corresponding pair of long pillar pattern **804**B in first set **802** and long pillar pattern **808**A in second set **806**. In FIG. **8**A, relative to the first/vertical direction, each short pillar pattern is located: substantially at a stub-distance from an end of one of the long pillar patterns which the short pillar pattern overlaps; and at a middle region of the other of the long pillar pattern which the short pillar pattern overlaps. As an example, short pillar pattern **820**A is located at substantially a stub-distance from the end of long pillar pattern **804**B and at a middle region of long pillar pattern **808**A. A stub-distance ensures a sufficient amount of overlap between the end of the long pillar and the short pillar, and is dependent upon the alignment tolerance of the corresponding process node used to manufacture structures corresponding to the short pillar patterns, long pillar patterns, or the like.

In FIG. **8**A, each of long pillar patterns **804**A-**804**B in first set **802**, and each of long pillar patterns **808**A-**808**B in second set **806**, is overlapped by a quantity Q_{818} of corresponding short pillar patterns **820**A-**820**D in third set **818**, and is electrically connected to the same. In FIG. **8**A, vertically-aligned and vertically-adjacent ones of long pillar patterns, including corresponding ones of long pillar patterns **804**A-**804**B and **808**A-**808**B, have a vertical separation distance of substantially one row height H_{ROW}. For example, vertically-aligned and vertically-adjacent long pillar patterns **808**A and **808**B have a vertical separation of substantially one row height H_{ROW}. In some embodiments, vertically-aligned and vertically-adjacent long pillar patterns have a vertical separation distance different than one row height H_{ROW}. In FIG. **8**A, for simplicity of illustration, quantity Q_{818} of short pillar patterns is shown as four, $Q_{818}=4$. In some embodiments, other values for Q_{818} are contemplated, where Q_{818} is a positive integer and $Q_{818}>3$. Quantity Q_{818} is greater than quantity Q_{822}, where $Q_{822}<$ where Q_{818}.

FIG. **8**B is a cross-sectional diagram of a conductive line structure **800**B of an IC structure, in accordance with at least one embodiment of the present disclosure. In some embodiments, the IC structure is IC structure **700** of FIG. **7**. In some embodiments, conductive line structure **800**B is fabricated at least in part according to layout **800**A of FIG. **8**A.

In FIG. **8**B, conductive line structure **800**B includes: long pillars **804**B' and **808**A'; vias **830**'; and a short pillars **820**A'. Long pillars **804**B' and **808**A' are conductive and correspond to long pillar patterns **804**B and **808**A of FIG. **8**A. Vias **830**' are conductive and correspond to via patterns **830** of FIG. **8**A. Short pillar **820**A' is conductive and corresponds to short pillar pattern **820**A of FIG. **8**A.

Advantages of using a connected long pillar pair configuration such as layout **800**A of FIG. **8**A include at least one of: a more robust grid (as contrasted with, e.g., a configuration of simple stripes according to another approach) without negatively impacting, e.g., routability or the like; reduced electromigration susceptibility, (as contrasted with, e.g., a configuration of simple stripes according to another approach) without negatively impacting, e.g., routability or the like; being appropriate/suitable to any metallization layer; or the like.

FIG. **9**A is a layout diagram of a conductive line structure **900**A of an IC structure, in accordance with at least one embodiment of the present disclosure. In some embodiments, the IC structure is IC structure **700** of FIG. **7**. Layout diagram **900**A includes an example of a connected long pillar pair configuration.

Layout diagram **900**A includes line patterns **902**A-**902**P, long pillar patterns **904**A-**904**V, and via patterns **910**. Via patterns **910** electrically connect long pillar patterns **904**A-**904**V with corresponding ones of line patterns **902**A-**902**P. Line patterns **902**A-**902**P are located in an M(i) metallization layer, where i is a non-negative integer. Long pillar patterns **904**A-**904**V are located in an M(i+1) metallization layer. In some embodiments, i=0. In some embodiments, i=1. In some embodiments, values of i other than i=0 or i=1 are contemplated.

Regarding line patterns **902**A-**902**P, they: are non-overlapping of each other; have long axes which are substantially parallel to a first direction. In some embodiments, the first direction is the vertical direction. Line patterns **902**A-**902**P are offset in a second direction relative to each other, the second direction being orthogonal to the first direction. In some embodiments, the second direction is the horizontal direction.

Within each cluster, members of the cluster, e.g., line patterns **902**A & **902**B, are offset in the second direction relative to each other by an offset distance, D_{OFF4}. In some embodiments, offset distance D_{OFF4} is the poly pitch, P_{POLY}, for the corresponding process node, where $D_{OFF4}=P_{POLY}$. In some embodiments, other values of D_{OFF4} are contemplated. Adjacent clusters are offset in the second direction relative to each other by an offset distance, D_{OFF5}. For example, line pattern **902**B of the cluster **902**A & **902**B is offset from line pattern **902**D of the cluster **902**C & **902**D by the distance D_{OFF5}. In some embodiments, D_{OFF5} is the one-half of the power pitch, Pv, between adjacent power rails or stripes for the corresponding process node, where $D_{OFF5}=\frac{1}{2}Pv$. In some embodiments, other values of D_{OFF5} are contemplated.

Long pillar patterns **904**A-**904**V are organized into sets **906**A-**9061**, for which the long pillar pattern members of each set: are non-overlapping of each other; have long axes which are substantially coaxial and substantially parallel to the second direction; are offset in the second direction relative to each other; and are overlapping of corresponding ones of line patterns **902**A-**902**P. Long pillar patterns **904**A-**904**V also are organized into groups **908**A-**908**D and the like. A collection of groups is referred to as a unit. Each unit includes F groups, where F is a positive integer. In FIG. **9**A, F=4. In some embodiments, values of F other than 4 are contemplated. Regarding groups **908**A-**908**D and the like, they: are offset in the first direction relative to each other;

and each have a same quantity of the long pillar patterns. For each of groups **908**A-**908**D and the like, member long pillar patterns of the group: are non-overlapping of each other; and are offset, and aligned, in the first direction relative to each other.

Line patterns **902**A-**902**P are arranged into bunches, each bunch including J clusters, with the clusters being offset in the second direction from each other, where J is a positive integer. Each cluster includes K ones of line patterns **902**A-**902**P, where K is a positive integer. In FIG. **9**A, J is four, J=4, and K is two, K=2. In some embodiments, values of J other than four are contemplated. In some embodiments, values of K other than two are contemplated. The clusters of line patterns **902**A-**902**P include the clusters of line patterns **902**A & **902**B, **902**C & **902**D, **902**E & **902**F, and the like. In FIG. **9**A, examples of a bunch include the following: a bunch including clusters of line patterns of line patterns **902**A & **902**B, **902**C & **902**D, **902**E & **902**F and **902**G & **902**H; a bunch including clusters of line patterns of line patterns **902**C & **902**D, **902**E & **902**F, **902**G & H and **902**I & **902**J; and the like. For each of sets **906**A-**9061** of long pillar patterns, each of the long pillar pattern members thereof overlaps J-1 clusters. Accordingly, in FIG. **9**A, for each of sets **906**A-**9061** of long pillar patterns, each of the long pillar pattern members thereof overlaps J-1=4-1=3 clusters. Also for each of sets **906**A-**9061** of long pillar patterns, each of the long pillar pattern members thereof is electrically connected to each of the members of J-2 clusters. Accordingly, in FIG. **9**A, for each of sets **906**A-**9061** of long pillar patterns, each of the long pillar pattern members thereof is electrically connected to each of the members of J-2=4-2=2 clusters.

Where long pillar pattern patterns **904**A-**904**V cross over corresponding portions of line patterns **902**A-**902**P, two types of intersections are described, namely a functional intersection **914**A and a flyover intersection **914**B. Regarding a conductive line structure that will be fabricated at least in part according to layout **800**A, and for a functional intersection **914**A, corresponding ones of long pillar pattern patterns **904**A-**904**V will be functionally connected (electrically connected) to corresponding ones of underlying line patterns **902**A-**902**P through corresponding via patterns **910**. Regarding a conductive line structure that will be fabricated at least in part according to layout **800**A, and for a flyover intersection **914**B, corresponding ones of long pillar pattern patterns **904**A-**904**V will NOT be functionally connected (electrically connected) to corresponding ones of underlying line patterns **902**A-**902**P because no via patterns **910** are present at flyover intersections **914**B.

For a reference portion **912**A-**912**B and the like of each of line patterns **902**A-**902**P, a number, Q1, of the long pillar patterns which overlaps the reference portion is greater than a second number, Q2, of long pillar patterns which are electrically connected to the reference portion (or which intersect in the form of functional intersections rather than flyover intersections). In FIG. **9**A, Q2=Q1−1. In some embodiments, other relations between Q2 and Q1 are contemplated.

As an example, consider reference portion **912**B of each of line patterns **902**C and **902**D. Long pillar patterns **904**C, **904**H, **904**K and **904**M overlap reference portion **912**B of line patterns **902**C and **902**D. In the example, the first number of long pillar patterns **904**A-**904**V which overlaps reference portion **912**B of each of line patterns **902**C and **902**D is four, Q1=4. Of the overlapping ones of the long pillar patterns, long pillar patterns **904**C, **904**H and **904**M overlap reference portion **912**B of line patterns **902**C and **902**D in the form of functional intersections **914**A. By contrast, long pillar pattern **904**K overlaps reference portion **912**B of line patterns **902**C and **902**D in the form of a flyover intersection **914**B. Accordingly, in the example, the second number of long pillar patterns which are electrically connected to reference portion **912**B of each of line patterns **902**C and **902**D is three, Q2=3 such that (Q2=3)<(Q1=4). Furthermore, in the example, the number F of groups in a unit is Q1, where F=Q1=4, and such that Q2=F−1=3.

FIG. **9**B is a cross-sectional diagram of a conductive line structure **900**B of an IC structure, in accordance with at least one embodiment of the present disclosure. In some embodiments, the IC structure is IC structure **700** of FIG. **7**. In some embodiments, conductive line structure **900**B is fabricated at least in part according to layout **900**A of FIG. **9**A.

In FIG. **9**B, conductive line structure **900**B includes: lines **902**G', **902**H', **902**I' and **902**J'; vias **910**'; and a long pillar **904**S'. Lines **902**G', **902**H', **902**I' and **902**J' are conductive and correspond to line patterns **902**G, **902**H, **902**I and **902**J. Vias **910**' are conductive and correspond to via patterns **910** of FIG. **9**A. Long pillar **904**S' is conductive and corresponds to long pillar pattern **904**S of FIG. **9**A.

Advantages of using a connected long pillar pair configuration such as layout **900**A of FIG. **9**A include at least one of: a more robust grid (as contrasted with, e.g., a configuration of simple stripes according to another approach) without negatively impacting, e.g., routability or the like; reduced electromigration susceptibility, (as contrasted with, e.g., a configuration of simple stripes according to another approach) without negatively impacting, e.g., routability or the like; being appropriate/suitable to any metallization layer; or the like.

FIG. **10**A is a flowchart of a method **1000**A of generating a layout of an IC structure, in accordance with some embodiments. In some embodiments, method **1000** is used to generate an instance of layout diagram **800**A of conductive line structure **800**B of an IC structure.

In FIG. **10**A, the flowchart of method **1000**A includes blocks **1002**-**1012**. At least one of blocks **1002**, **1004** (which includes blocks **1006**-**1008**) or **1010** is executed by a processor of a computer. An example of the processor is a processor **1102** of FIG. **11** (discussed below). An example of the computer is an electronic design automation (EDA) system **1100** of FIG. **11** (discussed below). In some embodiments, each of blocks **1002**-**1010** is executed by the processor of the computer. In some embodiments, the layout generated by method **1000** is stored on a non-transitory computer-readable medium. An example of the non-transitory computer-readable medium is layout **1107** of FIG. **11** (discussed below).

At block **1002**, first and corresponding second sets of long pillar patterns are generated. Examples of the first and second sets of long pillar patterns are first set **802** of long pillar patterns **804**A-**804**B of FIG. **8**A and corresponding second set **806** of long pillar patterns **808**A-**808**B of FIG. **8**A. Such long pillar patterns are: non-overlapping of each other; and substantially coaxial to, and substantially parallel to, a first direction. The first set is offset from the second set in a second direction orthogonal to the first direction. From block **1002**, flow proceeds to block **1004**.

At block **1004**, a third set of short pillar patterns is generated. An example of the third set of short pillar patterns is set **818** of short pillar patterns **820**A-**820**D of FIG. **8**A. Such short pillar patterns are: non-overlapping of each other; arranged with long axes which are substantially parallel to the second direction; overlapping of corresponding long pillar patterns in the first and second sets; and organized into groups. Examples of such a group are groups **822**A-**822**B of FIG. **8**A. Each such group has a first quantity of the short pillar patterns. In the example of FIG. **8**A, the first quantity Q_{822} is two, where $Q_{822}=2$. In some embodiments, other values for Q_{822} are contemplated, where Q_{822} is a positive integer and Q**822**>2.

Again, block **1004** includes blocks **1006**-**1008**. Within block **1004**, flow proceeds to block **1006**. At block **1006**, members of the third set are arranged so that each long pillar pattern in each of the first and second sets is overlapped by a second quantity of corresponding short pillar patterns and is electrically connected to the same. In the example of FIG. **8**A, the second quantity Q_{818} is three, where $Q_{818}=3$, and where Q_{818} is greater than Q_{822} such that where $Q_{822}<Q_{818}$. From block **1006**, flow proceeds to block **1008**.

At block **1008**, members of the third set are arranged so that each short pillar pattern in each group overlaps a corresponding one of the long pillar patterns in the first set and a corresponding one of the long pillar patterns in the second set and is electrically connected to the same. In the example of FIG. **8**A, e.g., long pillar pattern **804**B is overlapped by short pillar patterns **820**A-**820**D through corresponding via patterns **830**. From block **1008**, flow exits block **1004** and proceeds to block **1010**.

At block **1010**, first via patterns are generated, which includes arranging the same so as to electrically connect the short pillar patterns in the third set with corresponding ones of the long pillar patterns in the first and second sets. In the example of FIG. **8**A, e.g., Via patterns **830** electrically connect long pillar pattern **804**B to short pillar patterns **820**A-**820**D. From block **1010**, flow proceeds to block **1012**. At block **1012**, based on the layout, at least one of (A) one or more semiconductor masks is fabricated (see FIG. **12**, discussed below) or (B) at least one component in a layer of an inchoate semiconductor integrated circuit is fabricated (again, see FIG. **12**, discussed below).

FIG. **10**B is a high level process flow of a method **1000**B of shifting at least one pillar of an IC structure in a layout, in accordance with at least one embodiment of the present disclosure.

In FIG. **10**B, the flowchart of method **1000**B includes blocks **1022**-**1042**. At least one of blocks **1022**-**1040** is executed by a processor of a computer. An example of the processor is a processor **1102** of FIG. **11** (discussed above). An example of the computer is an electronic design automation (EDA) system **1100** of FIG. **11** (discussed below). In some embodiments, each of blocks **1022**-**1040** is executed by the processor of the computer. In some embodiments, the layout generated by method **1000**B is stored on a non-transitory computer-readable medium. An example of the non-transitory computer-readable medium is layout **1107** stored in memory **1104** of FIG. **11** (discussed below).

At block **1022**, an IR drop analysis is executed for conductive segments in a layer M_n. For the IR drop analysis of block **1022**, an attempt is made to use stripes, wherein a stripe is a conductive line which is longer than a long pillar (where a length of a long pillar is related to the Blech length, L_{Blech}, discussed above). For block **1022**, it is assumed that an IR drop exhibited by the stripes satisfies is less than or equal to a corresponding maximum reference value. From block **1022**, flow proceeds to block **1024** wherein a determination is made whether there is an electromigration issue in any of one or more stripes in the M_n layer. In some embodiments, the determination of an whether there is an electromigration issue is based on test data, details of the grain structure for the conductors under consideration, the metal deposition process used to form the conductors under consideration, or the like.

If the result of block **1024** is negative, then the process flow proceeds to block **1026** in which a stripe is used into the layout, resulting in the layout. In some embodiments, a stripe is a conductive line which is longer than a long pillar (where a length of a long pillar is related to the Blech length, L_{Blech}, discussed above). From block **1026**, the process flow then proceeds to block **1042** where, based on the layout, at least one of (A) one or more semiconductor masks is fabricated (see FIG. **12**, discussed below) or (B) at least one component in a layer of an inchoate semiconductor integrated circuit is fabricated (again, see FIG. **12**, discussed below).

If the result of block **1024** is positive, i.e., an electromigration issue is determined in the layout, then the process flow proceeds to block **1028**. At block **1028**, an attempt is made to use short pillars. Execution of block **1028** causes the insertion of short pillars into the layout in replacement of corresponding stripe(s) having the electromigration issue. An example of the short pillars are short pillars **1302** and **1304** of FIG. **13**A (discussed below). The process flow then proceeds to block **1030** in which a determination is made whether an IR drop exhibited by the short pillars (which were introduced as replacements of the corresponding stripe(s) at block **1028**) has degraded beyond a corresponding threshold relative to the IR drop(s) of the corresponding stripe(s). If the result of block **1030** is negative, then the process flow proceeds to block **1032** in which the short pillars (see block **1028**) are used, resulting in the layout. At block **1032**, the short pillars are used without having to shift track-aligned positions of one or more of the short pillars such that the short pillars remain co-track aligned (for shifting, e.g., see **1514** of FIG. **15**, discussed below). From block **1032**, the process flow then proceeds to block **1042** (discussed above).

If the result of block **1030** is positive, then the process flow proceeds to block **1034** which tries to use long pillars in a simple pairing configuration. Execution of block **1034** causes the insertion of long pillars in a simple pairing configuration into the layout in replacement of corresponding stripe(s) which were determined in block **1024** as having the electromigration issue. In the simple pairing configuration of long pillars, direct electrical connections are made between two members of a first pair of long pillars (intra-pair connections), but no direct electrical connection is made between the first pair of long pillars and a second pair of long pillars.

From block **1034**, the process flow then proceeds to block **1036** in which a determination is made whether an IR drop exhibited by the simple pairing configuration of long pillars (which was introduced as replacements of the corresponding stripe(s) at block **1034**) has degraded beyond a corresponding threshold relative to the IR drop(s) of the corresponding stripe(s). If the result of block **1036** is negative, then the process flow proceeds to block **1038** in which the simple pairing configuration of long pillars is used, resulting in the layout. From block **1038**, the process flow then proceeds to block **1042** (discussed above).

If the result of block **1036** is positive, then the process flow proceeds to block **1040** which uses a connected long pillar pair configuration, resulting in the layout. In the connected long pillar pair configuration of long pillars, intra-pair connections are made and inter-pair connections are made. An example of a first pair of long pillar patterns having intra-pair and inter-pair connections is the pair of long pillar pattern **804**B and long pillar pattern **808**A of FIG. **8**A, which: are intra-pair connected by short pillar patterns **820**A and **820**B as well as corresponding via patterns **830**; and for which member long pillar pattern **804**B is inter-pair connected by short pillar patterns **820**C and **820**D as well as corresponding via patterns **830** to long pillar pattern **808**B, where long pillar pattern **808**B is a member of a second pair. Another example of a first pair of long pillar patterns having intra-pair and inter-pair connections is the pair of long pillar pattern **904**F and long pillar pattern **904**P of FIG. **9**A, which: are intra-pair connected by line patterns **902**E, **902**F, **902**I and **902**J as well as corresponding via patterns **910**; and are inter-pair connected by line patterns **902**E, **902**F, **902**I and **902**J as well as corresponding via patterns **910** to at least long pillar patterns **904**A and **904**K, where long pillar patterns **904**A and **904**K are members of a second pair. In FIG. **9**A, the noted second pair is included in a corresponding second group of long pillar patterns which includes not only long pillar patterns **904**A and **904**K but also long pillar pattern **904**U. In some embodiments, the second group further includes other corresponding long pillar patterns which are vertically-aligned with long pillar patterns **904**A, **904**K and **904**U, where the other corresponding long pillar patterns are not shown in FIG. **9**A but are suggested by the ellipses at the top and bottom of FIG. **9**A. In some embodiments, the noted first pair is included in a corresponding first group which further includes other corresponding long pillar patterns which are vertically-aligned with long pillar patterns **904**F and **904**P, where the other corresponding long pillar patterns are not shown in FIG. **9**A but are suggested by the ellipses at the top and bottom of FIG. **9**A. From block **1040**, the process flow then proceeds to block **1042** (discussed above).

FIG. **11** is a block diagram of an electronic design automation (EDA) system **1100**, in accordance with at least one embodiment of the present disclosure.

In some embodiments, EDA system **1100** includes an APR system. The method of the flowcharts of FIGS. **6** and **10**A-**10**B are implemented, for example, using EDA system **1100**, in accordance with some embodiments.

In some embodiments, EDA system **1100** is a general purpose computing device including a hardware processor **1102** and a non-transitory, computer-readable storage medium **1104**. Storage medium **1104**, amongst other things, is encoded with, i.e., stores, computer program code **1106**, i.e., a set of executable instructions. Execution of instructions **1106** by hardware processor **1102** represents (at least in part) an EDA tool which implements a portion or all of, e.g., the methods of FIGS. **6** and **10**A-**10**B, in accordance with one or more embodiments (hereinafter, the noted processes and/or methods).

Processor **1102** is electrically coupled to computer-readable storage medium **1104** via a bus **1108**. Processor **1102** is also electrically coupled to an I/O interface **1110** by bus **1108**. A network interface **1112** is also electrically connected to processor **1102** via bus **1108**. Network interface **1112** is connected to a network **1114**, so that processor **1102** and computer-readable storage medium **1104** are capable of connecting to external elements via network **1114**. Processor **1102** is configured to execute computer program code **1106** encoded in computer-readable storage medium **1104** in order to cause system **1100** to be usable for performing a portion or all of the noted processes and/or methods. Computer-readable storage medium **1104** also includes one or more layouts **1107** generated according to a portion or all of the noted processes and/or methods. In one or more embodiments, processor **1102** is a central processing unit (CPU), a multi-processor, a distributed processing system, an application specific integrated circuit (ASIC), and/or a suitable processing unit.

In one or more embodiments, computer-readable storage medium **1104** is an electronic, magnetic, optical, electromagnetic, infrared, and/or a semiconductor system (or apparatus or device). For example, computer-readable storage medium **1104** includes a semiconductor or solid-state memory, a magnetic tape, a removable computer diskette, a random access memory (RAM), a read-only memory (ROM), a rigid magnetic disk, and/or an optical disk. In one or more embodiments using optical disks, computer-readable storage medium **1104** includes a compact disk-read only memory (CD-ROM), a compact disk-read/write (CD-R/W), and/or a digital video disc (DVD).

In one or more embodiments, storage medium **1104** stores computer program code **1106** configured to cause system **1100** (where such execution represents (at least in part) the EDA tool) to be usable for performing a portion or all of the noted processes and/or methods. In one or more embodiments, storage medium **1104** also stores information which facilitates performing a portion or all of the noted processes and/or methods. In one or more embodiments, storage medium **1104** stores a library (not shown) of standard cells.

EDA system **1100** includes I/O interface **1110**. I/O interface **1110** is coupled to external circuitry. In one or more embodiments, I/O interface **1110** includes a keyboard, keypad, mouse, trackball, trackpad, touchscreen, and/or cursor direction keys for communicating information and commands to processor **1102**.

Again, EDA system **1100** includes network interface **1112**. Network interface **1112** includes wireless network interfaces such as BLUETOOTH, WIFI, WIMAX, GPRS, or WCDMA; or wired network interfaces such as ETHERNET, USB, or IEEE-1364. In one or more embodiments, a portion or all of noted processes and/or methods, is implemented in two or more systems **1100**.

System **1100** is configured to receive information through I/O interface **1110**. The information received through I/O interface **1110** includes one or more of instructions, data, design rules, libraries of standard cells, and/or other parameters for processing by processor **1102**. The information is transferred to processor **1102** via bus **1108**. EDA system **1100** is configured to receive information related to a UI through I/O interface **1110**. The information is stored in computer-readable medium **1104** as user interface (UI) **1142**.

In some embodiments, a portion or all of the noted processes and/or methods is implemented as a standalone software application for execution by a processor. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a software application that is a part of an additional software application. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a plug-in to a software application. In some embodiments, at least one of the noted processes and/or methods is implemented as a software application that is a portion of an EDA tool. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a software application that is used by EDA system **1100**. In some embodiments, a layout is generated using a tool such as VIRTUOSO® available from CADENCE DESIGN SYSTEMS, Inc., or another suitable layout generating tool.

In some embodiments, the processes are realized as functions of a program stored in a non-transitory computer readable recording medium. Examples of a non-transitory computer readable recording medium include, but are not limited to, external/removable and/or internal/built-in storage or memory unit, e.g., one or more of an optical disk, such as a DVD, a magnetic disk, such as a hard disk, a semiconductor memory, such as a ROM, a RAM, a memory card, and the like.

FIG. **12** is a block diagram of an integrated circuit (IC) manufacturing system **1200**, and an IC manufacturing flow associated therewith, in accordance with at least one embodiment of the present disclosure.

In FIG. **12**, IC manufacturing system **1200** includes entities, such as a design house **1220**, a mask house **1230**, and an IC manufacturer/fabricator ("fab") **1240**, that interact with one another in the design, development, and manufacturing cycles and/or services related to manufacturing an IC device **1260**. The entities in system **1200** are connected by a communications network. In some embodiments, the communications network is a single network. In some embodiments, the communications network is a variety of different networks, such as an intranet and the Internet. The communications network includes wired and/or wireless communication channels. Each entity interacts with one or more of the other entities and provides services to and/or receives services from one or more of the other entities. In some embodiments, two or more of design house **1220**, mask house **1230**, and IC fab **1240** is owned by a single larger company. In some embodiments, two or more of design house **1220**, mask house **1230**, and IC fab **1240** coexist in a common facility and use common resources.

Design house (or design team) **1220** generates an IC design layout **1222**. IC design layout **1222** includes various geometrical patterns designed for an IC device **1260**. The geometrical patterns correspond to patterns of metal, oxide, or semiconductor layers that make up the various components of IC device **1260** to be fabricated. The various layers combine to form various IC features. For example, a portion of IC design layout **1222** includes various IC features, such as an active region, gate electrode, source and drain, metal lines or vias of an interlayer interconnection, and openings for bonding pads, to be formed in a semiconductor substrate (such as a silicon wafer) and various material layers disposed on the semiconductor substrate. Design house **1220** implements a proper design procedure to form IC design layout **1222**. The design procedure includes one or more of logic design, physical design or place and route. IC design layout **1222** is presented in one or more data files having information of the geometrical patterns. For example, IC design layout **1222** can be expressed in a GDSII file format or DFII file format.

Mask house **1230** includes mask data preparation **1232** and mask fabrication **1234**. Mask house **1230** uses IC design layout **1222** to manufacture one or more masks to be used for fabricating the various layers of IC device **1260** according to IC design layout **1222**. Mask house **1230** performs mask data preparation **1232**, where IC design layout **1222** is translated into a representative data file ("RDF"). Mask data preparation **1232** provides the RDF to mask fabrication **1234**. Mask fabrication **1234** includes a mask writer. A mask writer converts the RDF to an image on a substrate, such as a mask (reticle) or a semiconductor wafer. The design layout is manipulated by mask data preparation **1232** to comply with particular characteristics of the mask writer and/or requirements of IC fab **1240**. In FIG. **12**, mask data preparation **1232** and mask fabrication **1234** are illustrated as separate elements. In some embodiments, mask data preparation **1232** and mask fabrication **1234** can be collectively referred to as mask data preparation.

In some embodiments, mask data preparation **1232** includes optical proximity correction (OPC) which uses lithography enhancement techniques to compensate for image errors, such as those that can arise from diffraction, interference, other process effects and the like. OPC adjusts IC design layout **1222**. In some embodiments, mask data preparation **1232** includes further resolution enhancement techniques (RET), such as off-axis illumination, sub-resolution assist features, phase-shifting masks, other suitable techniques, and the like or combinations thereof. In some embodiments, inverse lithography technology (ILT) is also used, which treats OPC as an inverse imaging problem.

In some embodiments, mask data preparation **1232** includes a mask rule checker (MRC) that checks the IC design layout that has undergone processes in OPC with a set of mask creation rules which contain certain geometric and/or connectivity restrictions to ensure sufficient margins, to account for variability in semiconductor manufacturing processes, and the like. In some embodiments, the MRC modifies the IC design layout to compensate for limitations during mask fabrication **1234**, which may undo part of the modifications performed by OPC in order to meet mask creation rules.

In some embodiments, mask data preparation **1232** includes lithography process checking (LPC) that simulates processing that will be implemented by IC fab **12501240** to fabricate IC device **1260**. LPC simulates this processing based on IC design layout **1222** to create a simulated manufactured device, such as IC device **1260**. The processing parameters in LPC simulation can include parameters associated with various processes of the IC manufacturing cycle, parameters associated with tools used for manufacturing the IC, and/or other aspects of the manufacturing process. LPC takes into account various factors, such as aerial image contrast, depth of focus ("DOF"), mask error enhancement factor ("MEEF"), other suitable factors, and the like or combinations thereof. In some embodiments, after a simulated manufactured device has been created by LPC, if the simulated device is not close enough in shape to satisfy design rules, OPC and/or MRC are be repeated to further refine IC design layout **1222**.

It should be understood that the above description of mask data preparation **1232** has been simplified for the purposes of clarity. In some embodiments, mask data preparation **1232** includes additional features such as a logic operation (LOP) to modify the IC design layout according to manufacturing rules. Additionally, the processes applied to IC design layout **1222** during mask data preparation **1232** may be executed in a variety of different orders.

After mask data preparation **1232** and during mask fabrication **1234**, a mask or a group of masks are fabricated based on the modified IC design layout. In some embodiments, an electron-beam (e-beam) or a mechanism of multiple e-beams is used to form a pattern on a mask (photomask or reticle) based on the modified IC design layout. The mask can be formed in various technologies. In some embodiments, the mask is formed using binary technology. In some embodiments, a mask pattern includes opaque regions and transparent regions. A radiation beam, such as an ultraviolet (UV) beam, used to expose the image sensitive material layer (e.g., photoresist) which has been coated on a wafer, is blocked by the opaque region and transmits through the transparent regions. In one example, a binary mask includes a transparent substrate (e.g., fused quartz) and an opaque material (e.g., chromium) coated in the opaque regions of the mask. In another example, the mask is formed using a phase shift technology. In the phase shift mask

(PSM), various features in the pattern formed on the mask are configured to have proper phase difference to enhance the resolution and imaging quality. In various examples, the phase shift mask can be attenuated PSM or alternating PSM. The mask(s) generated by mask fabrication **1234** is used in a variety of processes. For example, such a mask(s) is used in an ion implantation process to form various doped regions in the semiconductor wafer, in an etching process to form various etching regions in the semiconductor wafer, and/or in other suitable processes.

IC fab **1240** is an IC fabrication business that includes one or more manufacturing facilities for the fabrication of a variety of different IC products. In some embodiments, IC Fab **1240** is a semiconductor foundry. For example, there may be a manufacturing facility for the front end fabrication of a plurality of IC products (front-end-of-line (FEOL) fabrication), while a second manufacturing facility may provide the back end fabrication for the interconnection and packaging of the IC products (back-end-of-line (BEOL) fabrication), and a third manufacturing facility may provide other services for the foundry business.

IC fab **1240** uses the mask (or masks) fabricated by mask house **1230** to fabricate IC device **1260**. Thus, IC fab **1240** at least indirectly uses IC design layout **1222** to fabricate IC device **1260**. In some embodiments, a semiconductor wafer **1242** is fabricated by IC fab **1240** using the mask (or masks) to form IC device **1260**. Semiconductor wafer **1242** includes a silicon substrate or other proper substrate having material layers formed thereon. Semiconductor wafer further includes one or more of various doped regions, dielectric features, multilevel interconnects, and the like (formed at subsequent manufacturing steps).

Details regarding an integrated circuit (IC) manufacturing system (e.g., system **1200** of FIG. **12**), and an IC manufacturing flow associated therewith are found, e.g., in U.S. Pat. No. 9,256,709, granted Feb. 9, 2016, U.S. Pre-Grant Publication No. 20150278429, published Oct. 1, 2015, U.S. Pre-Grant Publication No. 20140040838, published Feb. 6, 2014, and U.S. Pat. No. 7,260,442, granted Aug. 21, 2007, the entireties of each of which are hereby incorporated by reference.

FIGS. **13**A and **13**B are layout diagrams of a portion of a shifted pillar of an IC structure, in accordance with at least one embodiment of the present disclosure.

In FIG. **13**A, a conductive line structure, in an IC, includes first line segment **1302**, second line segment **1304**, third line segment **1306** and fourth line segment **1308** which are arranged with respect to a grid. The grid includes tracks **1***a*-**7***a* which are parallel to a first direction, and tracks **1***b*-**17***b* which are parallel to a second direction, the second direction being substantially perpendicular to the first direction. In FIG. **13**A, the first direction is vertical and the second direction is horizontal. In some embodiments, the first and second directions are directions other than the corresponding vertical and horizontal directions.

The first **1302** and second **1304** line segments: are conductive; are non-overlapping of each other; and have long axes which are substantially parallel to a first direction. The third **1306** and fourth **1308** line segments: are conductive; are non-overlapping of each other; have long axes which are substantially parallel to a second direction, the second direction being orthogonal to the first direction; and overlap the corresponding first **1302** and second **1304** line segments. The second **1304** and fourth **1308** line segments offset in the second direction relative to the corresponding first **1302** and third **1306** line segments. First **1302** and second **1304** line segments are coaxial with track **4***a*. Third **1306** and fourth **1308** line segments are coaxial with corresponding tracks **4***b* and **14***b*. In some embodiments, line segments **1302**-**1308** are short pillars.

In FIG. **13**A, first line segment **1302** and second line segment **1304** are substantially aligned along track **4***a*. As indicated by the X symbol on track **4***a*, the vertical-separation between first line segment **1302** and second line segment **1304** is less than a design-rule-permitted minimum offset, MIN_{COAX}, between vertically-adjacent co-track/coaxial line segments such that FIG. **13**A does not comply with the design rule. In some embodiments, a purpose of the design rule is to ensure a vertical-separation which is sufficiently large enough to accommodate minimum length conductive segment between first line segment **1302** and second line segment **1304**.

As shown in FIG. **13**B, to increase the vertical-separation between vertically-adjacent co-track/coaxial line segments, second line segment **1304** is shifted by a shift-amount, Δ, in the first direction relative to the first line segment **1302** such that second line segment **1304** is aligned with track **5***a*. In FIG. **13**B, the shift-amount A is one track width. In some embodiments, the shift-amount A is a multiple of one track width. In some embodiments, the offset in the amount delta is equal to an offset between neighboring ones of tracks **1***a*-**7***a*. The resultant vertical-separation along track **5***a* is equal to or greater than the design-rule-permitted minimum offset MIN_{COAX} between vertically-adjacent co-track/coaxial line segments such that FIG. **13**B complies with the design-rule. In FIG. **13**B, second line segment **1304** is shifted to the right. In some embodiments, second line segment **1304** is shifted to the left.

In some embodiments the conducting line structure of FIG. **13**A includes a fifth line segment (not depicted) and a sixth line segment (not depicted) which are arranged with respect to the grid such that: the fifth line segment also is aligned along track **4***a*; the sixth line segment is substantially aligned along a track **24***b* (not shown); the fifth and sixth line segments overlap similarly to how first **1302** and second **1304** line segments overlap with corresponding third **1306** and fourth **1308** line segments; the vertical-separation between second line segment **1304** and the fifth line segment is less than the design-rule-permitted minimum offset MIN_{COAX} between vertically-adjacent co-track/coaxial line segments. Accordingly, in some embodiments, the fifth and sixth line segments are shifted similarly to how second line segment **1304** and fourth line segment **1308** are shifted in FIG. **13**B such that the fifth line segment is shifted by the shift-amount A in the first direction relative to second line segment **1304** such that fifth line segment (again, now shown) becomes aligned with track **6***a*. In some embodiments, in contrast to how second line segment **1304** and fourth line segment **1308** are shifted in FIG. **9**B, the fifth and sixth line segments are not shifted relative to first line segment **1302** because the shift of second line segment **1304** and fourth line segment **1308** relative to first line segment **1302** not only achieves adequate vertical-separation (between vertically-adjacent co-track/coaxial line segments) along track **5***a* but also does so for track **4***a* (that latter being between first line segment **1302** and the fifth line segment).

Accordingly, an advantage of FIG. **13**B is that a layout incorporating such pillar-shifting has a reduced consumption of routing-resources such that the layout incorporating the conducting line structure is denser. In some embodiments, the portion of track **4***a* below first line segment **1302** (which is otherwise occupied by second line segment **1304** in FIG. **13**A) is used for signal routing. In some embodiments, a layout incorporating such a conducting line structure is denser by two or more instances of the first reference line relative to a power pitch. In some embodiments, the power pitch is a distance between a line segment having a voltage level of a first reference voltage and a line segment having a voltage level of a second reference voltage. In some embodiments, the first reference voltage is VDD and the second reference voltage is VSS.

FIGS. **14**A and **14**B are layout diagrams of a portion of two shifted pillars of an IC structure, in accordance with at least one embodiment of the present disclosure.

FIGS. **14A-14**B are a variation of FIGS. **13A-13**B such that FIGS. **14A-14**B further include fifth line segment **1410** and sixth line segment **1412** which: are conductive; are non-overlapping of each other; have long axes which are substantially parallel to the first direction; and are overlapped by the corresponding third and fourth line segments. The fifth and sixth line segments are offset in the second direction relative to the corresponding first and second line segments. The sixth line segment is offset by the amount delta, Δ, in the first direction relative to the fifth line segment. In some embodiments in which line segments **1302-1308** are short pillars, line segments **1410** and **1412** also are short pillars.

The conductive line structure, and method for generating a layout of such a conductive line structure, arise in the context of a process node for a given semiconductor technology. In some embodiments, the offset in the amount delta is equal to a poly pitch of the process node.

In some embodiments, the first and second line segments are long pillars. In some embodiments, the third and fourth line segments are long pillars. In some embodiments, the first through fourth line segments are long pillars. In some embodiments, the line segments which are long pillars have a length, L_L, less than or equal to a predetermined length, L_{LIMIT}, where $L_L \leq L_{LIMIT}$. In some embodiments, L_{LIMIT} is substantially equal to, albeit without being greater than, the Blech length, L_{Blech}, where $L_{LIMIT} \approx L_{Blech}$ AND $L_{LIMI}T \leq L_{Blech}$. It is noted that L_{Blech} represents a length of conductor below which substantially no electromigration occurs. In some embodiments, L_{LIMIT} is a length other than Blech length, L_{Blech}.

In some embodiments, the first and second line segments are short pillars. In some embodiments, the third and fourth line segments are short pillars. In some embodiments, the first through fourth line segments are short pillars. In some embodiments, the line segments which are short pillars have a length, L_S, less than the predetermined length, L_{LIMIT}, where $L_S < L_{LIMIT}$.

FIG. **15** is a high level process flow of a method **1500** of shifting at least one pillar of an IC structure in a layout, in accordance with at least one embodiment of the present disclosure.

In FIG. **15**, the flowchart of method **1500** includes blocks **1502-1518**. At least one of blocks **1502-1516** is executed by a processor of a computer. An example of the processor is a processor **1102** of FIG. **11** (discussed above). An example of the computer is an electronic design automation (EDA) system **1100** of FIG. **11** (discussed above). In some embodiments, each of blocks is executed by the processor of the computer. In some embodiments, the layout generated by method **1500** is stored on a non-transitory computer-readable medium. An example of the non-transitory computer-readable medium is layout **1107** stored in memory **1104** of FIG. **11** (discussed above).

At block **1502**, an IR drop analysis is executed for conductive segments in a layer M_n. Assuming that the conductive segments in the M_n layer satisfy the IR drop analysis of block **1502**, the process flow then proceeds to block **1504** wherein a determination is made whether there is an electromigration issue in any of one or more stripes in the M_n layer. If the result of block **1504** is negative, then the process flow proceeds to block **1506** in which a stripe is used into the layout, resulting in the layout. In some embodiments, a stripe is a conductive line which is longer than a long pillar (where a length of a long pillar is related to the Blech length, L_{Blech}, discussed above). From block **1506**, the process flow then proceeds to block **1518** where, based on the layout, at least one of (A) one or more semiconductor masks is fabricated (see FIG. **12**, discussed above) or (B) at least one component in a layer of an inchoate semiconductor integrated circuit is fabricated (again, see FIG. **12**, discussed above).

If the result of block **1504** is positive, i.e., an electromigration issue is determined in the layout, then the process flow proceeds to block **1508** which tries to use short pillars. Execution of block **1508** causes the insertion of short pillars into the layout in replacement of corresponding stripe(s) having the electromigration issue. An example of the short pillars are short pillars **1302** and **1304** of FIG. **13**A. The process flow then proceeds to block **1510** in which a determination is made whether there is insufficient vertical-separation in which to fit a minimum length metal segment in between two given pillars of the IC structure. If the result of block **1510** is negative, the process flow proceeds to block **1512** in which a pillar is used without a shift in position/track-alignment, resulting in the layout such that the two given pillars remain co-track aligned. From block **1512**, the process flow then proceeds to block **1518** (discussed above).

If the result of block **1510** is positive, the process flow proceeds to block **1514** in which the pillar position is shifted by one track in a direction perpendicular to the direction in which the insufficient space was determined. The process flow then proceeds to block **1516** in which the shifted pillar is used, resulting in the layout. From block **1516**, the process flow then proceeds to block **1518** (discussed above).

An aspect of the present disclosure is directed to an IC structure comprises a power rail positioned at a power rail level and oriented in a power rail direction, and a plurality of first metal segments positioned at a first metal level above the power rail level, the plurality of first metal segments being oriented in a first metal level direction perpendicular to the power rail direction. The IC structure further comprises a plurality of first vias between the power rail level and the first metal level, each first via of the plurality of first vias being positioned at a location where a corresponding first metal segment of the plurality of first metal segments overlaps the power rail. The IC structure further comprises a second metal segment positioned at a second metal level above the first metal level, the second metal segment overlapping the power rail and being oriented in the power rail direction. The IC structure further comprises a plurality of second vias between the first metal level and the second metal level, each second via of the plurality of second vias being positioned at a location above a corresponding first via of the plurality of first vias, and a power strap positioned at a power strap level above the second metal level. The IC structure is configured to electrically connect the power strap to the power rail, each first metal segment of the plurality of first metal segments has a width corresponding to a predetermined minimum width for the first metal level, and the power strap has a width greater than a predetermined minimum width for the power strap level.

Regarding the aspect of the present disclosure, the power strap is one power strap of a plurality of power straps oriented in the first metal level direction, and the IC structure further includes: a plurality of third metal segments at a third metal level above the second metal level, the plurality of third metal segments being oriented in the first metal level direction; a plurality of third vias between the second metal level and the third metal level, each third via of the plurality of third vias being positioned at a location at which a third metal segment of the plurality of third metal segments overlaps the power rail; a plurality of fourth metal segments at a fourth metal level above the third metal level and below the power strap level, the plurality of fourth metal segments being oriented in the power rail direction; a plurality of fourth vias between the third metal level and the fourth metal level, each fourth via of the plurality of fourth vias being positioned at a location above a corresponding third via of the plurality of third vias; and a plurality of fifth vias between the fourth metal level and the power strap level, each fifth via of the plurality of fifth vias being positioned at a location at which a power strap of the plurality of power straps overlaps a corresponding fourth metal segment of the plurality of fourth metal segments. Each third metal segment of the plurality of third metal segments has a width corresponding to a predetermined minimum width for the third metal level. Each fourth metal segment of the plurality of fourth metal segments has a width corresponding to a predetermined minimum width for the fourth metal level.

Regarding the aspect of the present disclosure, the plurality of first metal segments includes: a first set of pairs of first metal segments alternating with a second set of pairs of first metal segments. The plurality of first vias electrically connects the first set of pairs of first metal segments to the power rail and is free from electrically connecting the second set of pairs of first metal segments to the power rail. The second metal segment is one second metal segment of a plurality of second metal segments. Each second metal segment of the plurality of second metal segments overlaps the power rail at locations at which a corresponding pair of the first set of pairs of first metal segments overlap the power rail and is free from overlapping the power rail at locations at which the second set of pairs of first metal segments overlap the power rail. Each second metal segment of the plurality of second metal segments has a width corresponding to a predetermined minimum width for the second metal level. Also regarding the first aspect of the present disclosure, each pair of first metal segments of the first set of pairs of first metal segments and of the second set of pairs of first metal segments has a first pitch. The pairs of first metal segments of the first set of pairs of first metal segments and the pairs of first metal segments of the second set of pairs of first metal segments have a second pitch. The second pitch is a multiple of the first pitch.

Regarding the aspect of the present disclosure, the first vias of the plurality of first vias are positioned at each location where corresponding first metal segments of the plurality of first metal segments overlap the power rail. The IC structure further comprises: a plurality of third metal segments positioned at a third metal level above the second metal level, the plurality of third metal segments being oriented in the first metal level direction and including a first set of third metal segments alternating with a second set of third metal segments; and a plurality of third vias, each third via of the plurality of third vias being positioned at a location where a corresponding third metal segment of the first set of third metal segments overlaps the power rail. Each third metal segment of the plurality of third metal segments has a width corresponding to a predetermined minimum width for the third metal level. Also regarding the first aspect of the present disclosure, the second metal segment is one second metal segment of a plurality of second metal segments. Each second metal segment of the plurality of second metal segments electrically connects a corresponding second via of the plurality of second vias to a corresponding third via of the plurality of third vias. Each second metal segment of the plurality of second metal segments has a width corresponding to a predetermined minimum width for the second metal level. Furthermore regarding the first aspect of the present disclosure, the second metal segment electrically connects the plurality of second vias to the plurality of third vias. The second metal segment has a width greater than a predetermined minimum width for the second metal level.

Another aspect of the present disclosure is directed to an IC structure comprises a first power rail positioned at a power rail level and oriented in a power rail direction, a second power rail positioned at the power rail level and oriented in the power rail direction, and a first metal segment positioned at a metal segment level above the power rail level, the first metal segment overlapping the first power rail and being oriented in the power rail direction. The IC structure further comprises a second metal segment positioned at the metal segment level, the second metal segment overlapping the second power rail and being oriented in the power rail direction, a plurality of metal straps positioned at a metal strap level above the power rail level, each metal strap of the plurality of metal straps overlapping the first power rail and the second power rail and being oriented in a metal strap direction perpendicular to the power rail direction, and a plurality of metal stubs positioned at a metal stub level above the power rail level, each metal stub of the plurality of metal stubs overlapping either the first power rail or the second power rail and being oriented in the metal strap direction. A first power strap is positioned at a power strap level above the metal segment level, the metal strap level, and the metal stub level, and a second power strap is positioned at the power strap level. The IC structure further comprises a plurality of via arrays, the number of via arrays being one less than a total number of metal levels, each via array comprising vias positioned at locations at which metal elements of corresponding adjacent metal levels overlap. The IC structure is configured to electrically connect the first power strap to the first power rail and to separately electrically connect the second power strap to the second power rail, each metal strap of the plurality of metal straps has a width corresponding to a predetermined minimum width for the metal strap level, each metal stub of the plurality of metal stubs has a width corresponding to a predetermined minimum width for the metal stub level, and each of the first power strap and the second power strap has a width greater than a predetermined minimum width for the power strap level.

Regarding the another aspect of the present disclosure, the first power strap is one first power strap of a plurality of first power straps oriented in the first metal strap direction. The second power strap is one second power strap of a plurality of second power straps oriented in the first metal level direction. The IC structure further comprises: a plurality of metal islands at a metal island level above the metal segment level, the metal strap level, and the metal stub level, and below the power strap level, the plurality of metal islands being oriented in the power rail direction. Each metal segment of the plurality of metal islands has a width corresponding to a predetermined minimum width for the metal island level.

Regarding the another aspect of the present disclosure, the metal segment level is a level above the metal strap level, and the metal stub level is a level above the metal segment level. The plurality of metal straps includes: a first set of pairs of metal straps alternating with a second set of pairs of metal straps. The first metal segment is one first metal segment of a plurality of first metal segments. Each first metal segment of the plurality of first metal segments overlaps the power rail at locations at which a corresponding pair of the first set of pairs of metal straps overlap the first power rail. The second metal segment is one second metal segment of a plurality of second metal segments. Each second metal segment of the plurality of second metal segments overlaps the power rail at locations at which a corresponding pair of the second set of pairs of metal straps overlap the second power rail. Each first metal segment of the plurality of first metal segments and each second metal segment of the plurality of second metal segments has a width corresponding to a predetermined minimum width for the metal segment level. Also regarding the second aspect of the present disclosure, each pair of metal straps of the first set of pairs of metal straps and the second set of pairs of metal straps has a first pitch. The pairs of metal straps of the first set of pairs of metal straps and the pairs of metal straps of the second set of pairs of metal straps have a second pitch. The second pitch is a multiple of the first pitch.

Regarding the another aspect of the present disclosure, the metal stub level is a level above the power rail level, the metal segment level is a level above the metal stub level, and the metal strap level is a level above the metal segment level. The first metal segment is one first metal segment of a plurality of first metal segments overlapping the first power rail. The second metal segment is one second metal segment of a plurality of second metal segments overlapping the second power rail. Each first metal segment of the plurality of first metal segments and each second metal segment of the plurality of second metal segments has a width corresponding to a predetermined minimum width for the metal segment level. The plurality of metal straps includes: a first set of metal straps alternating with a second set of metal straps. Each metal strap of the first set of metal straps overlaps a corresponding first metal segment of the plurality of first metal segments. Each metal strap of the second set of metal straps overlaps a corresponding second metal segment of the plurality of second metal segments.

Regarding the another aspect of the present disclosure, the metal segment level is a level above the metal stub level, and the metal strap level is a level above the metal segment level. The plurality of metal straps includes: a first set of metal straps alternating with a second set of metal straps. Each metal strap of the first set of metal straps is electrically connected to the first metal segment. Each metal strap of the second set of metal straps is electrically connected to the second metal segment. Each of the first metal segment and the second metal segment overlaps multiple metal stubs of the plurality of metal stubs and has a width wider than a predetermined minimum width for the metal segment level. Also regarding the second aspect of the present disclosure, each of the locations at which the first metal segment or the second metal segment overlaps the metal stubs of the plurality of metal stubs corresponds to a location at which a metal strap of the plurality of metal straps overlaps the first metal segment or the second metal segment. Furthermore regarding the second aspect of the present disclosure, the locations at which the metal straps of the plurality of metal straps overlap the first metal segment or the second metal segment correspond to a subset of the locations at which the first metal segment or the second metal segment overlap the metal stubs of the plurality of metal stubs.

A further aspect of the present disclosure is directed to a method of forming an IC structure comprises forming a first power rail and a second power rail at a power rail level, the first power rail and the second power rail being oriented in a power rail direction, and forming a plurality of first metal segments at a first metal level above the power rail level, the plurality of first metal segments being oriented in a first metal level direction perpendicular to the power rail direction, each first metal segment of the plurality of first metal segments overlapping one or both of the first power rail or the second power rail. The method further comprises forming a plurality of first vias between the power rail level and the first metal level, each first via of the plurality of first vias being positioned at a location where a corresponding first metal segment of the plurality of first metal segments overlaps the first power rail or the second power rail, and forming a plurality of second metal segments at a second metal level above the first metal level, each second metal segment of the plurality of second metal segments being oriented in the power rail direction, at least one second metal segment of the plurality of second metal segments overlapping the first power rail, and at least one second metal segment of the plurality of second metal segments overlapping the second power rail. The method further comprises forming a plurality of second vias between the first metal level and the second metal level, each second via of the plurality of second vias being positioned at a location above a corresponding first via of the plurality of first vias, forming a first power strap at a power strap level above the second metal level, and forming a second power strap at the power strap level. Forming the IC structure comprises configuring the IC structure to electrically connect the first power strap to the first power rail and to electrically connect the second power strap to the second power rail, forming the plurality of first metal segments comprises forming each first metal segment of the plurality of first metal segments having a width corresponding to a predetermined minimum width for the first metal level, forming the first power strap comprises forming the first power strap having a width greater than a predetermined minimum width for the power strap level, and forming the second power strap comprises forming the second power strap having the width greater than the predetermined minimum width for the power strap level.

Regarding the further aspect of the present disclosure, the forming the plurality of first metal segments includes: forming a first set of pairs of first metal segments alternating with a second set of pairs of first metal segments. Each pair of first metal segments of the first set of pairs of first metal segments and of the second set of pairs of first metal segments has a first pitch. The pairs of first metal segments of the first set of pairs of first metal segments and the pairs of first metal segments of the second set of pairs of first metal segments have a second pitch. The second pitch is a multiple of the first pitch. The forming the plurality of second metal segments includes: forming a first set of second metal segments overlapping the first set of pairs of first metal segments and the first power rail; forming a second set of second metal segments overlapping the second set of pairs of first metal segments and the second power rail; and forming each second metal segment of the plurality of second metal segments having a width corresponding to a predetermined minimum width for the second metal level.

Regarding the further aspect of the present disclosure, the forming the plurality of second metal segments includes: forming a first set of second metal segments overlapping corresponding first metal segments of the plurality of first metal segments and the first power rail; forming a second set of second metal segments overlapping corresponding first metal segments of the plurality of first metal segments and the second power rail; and forming each second metal segment of the plurality of second metal segments having a width corresponding to a predetermined minimum width for the second level. The forming the IC structure further includes: forming a plurality of third metal segments at a third metal level above the second metal level, the plurality of third metal segments being oriented in the first metal level direction and including a first set of third metal segments alternating with a second set of third metal segments. The forming the first set of third metal segments includes: forming third metal segments overlapping corresponding second metal segments of the first set of second metal segments. The forming the second set of third metal segments includes: forming third metal segments overlapping corresponding second metal segments of the second set of second metal segments. The forming the plurality of third metal segments includes: forming each third metal segment of the plurality of third metal segments having a width corresponding to a predetermined minimum width for the third metal level.

Regarding the further aspect of the present disclosure, the forming the plurality of first vias includes: forming a via at each location where the first metal segments of the plurality of first metal segments overlap the first power rail and at each location where the first metal segments of the plurality of first metal segments overlap the second power rail. The forming the plurality of second metal segments includes: forming each second metal segment overlapping multiple first metal segments of the plurality of first metal segments and having a width wider than a predetermined minimum width for the second metal segment level. The forming the IC structure further includes: forming a plurality of third metal segments at a third metal level immediately above the second metal level, the plurality of third metal segments being oriented in the first metal level direction and including a first set of third metal segments alternating with a second set of third metal segments. The forming the plurality of third metal segments includes: forming each third metal segment of the plurality of third metal segments overlapping the first power rail and the second power rail and having a width corresponding to a predetermined minimum width for the third metal level; and forming a plurality of third vias, the plurality of third vias electrically connecting the first set of third metal segments to the at least one second metal segment of the plurality of second metal segments overlapping the first power rail and electrically connecting the second set of third metal segments to the at least one second metal segment of the plurality of second metal segments overlapping the second power rail.

Yet another aspect of the present disclosure is directed to a conductive line structure in an integrated circuit (IC), the conductive line structure comprising: first and corresponding second sets of long pillars; a third set of short pillars; and first vias. Members of each of the first and second sets: are non-overlapping of each other; and have long axes which are substantially coaxial and substantially parallel to a first direction. The second set is offset in a second direction relative to the first set, the second direction being orthogonal to the first direction. Members of the third set of short pillars: are non-overlapping of each other; have long axes which are substantially parallel to the second direction; are overlapping of corresponding long pillars in the first and second sets; and are organized into groups. Each group has a first quantity of the short pillars in the third set. The first vias electrically connect the short pillars in the third set with corresponding ones of the long pillars in the first and second sets. Each group of the third set overlaps and is electrically connected between a corresponding pair of one of the long pillars in the first set and a corresponding one of the long pillars in the second set such that, in each group, each short pillar overlaps and is electrically connected between the corresponding pair. Each long pillar in each of the first and second sets is overlapped by a second quantity of corresponding short pillars in the third set and is electrically connected to the same. The first quantity is less than the second quantity.

Regarding the yet another aspect of the present disclosure, members of the third set are aligned in the first direction. The conductive line structure further comprises: fourth and corresponding fifth sets of long pillars; a sixth set of short pillars; and second vias. Members of each of the fourth and fifth sets: are non-overlapping of each other; and have long axes which are substantially coaxial and substantially parallel to the first direction. The fifth set is offset in the second direction relative to the fourth set. Members of the sixth set of short pillars: are non-overlapping of each other; have long axes which are substantially parallel to the second direction; are overlapping of corresponding long pillars in the fourth and fifth sets; and are organized into groups, each group having the first quantity of the short pillars in the sixth set. The second vias electrically connect the short pillars in the sixth set with corresponding ones of the long pillars in the fourth and fifth sets. Each long pillar in each of the fourth and fifth sets is overlapped by the second quantity of corresponding short pillars in the sixth set and is electrically connected to the same. Each short pillar in each group of the sixth set overlaps a corresponding one of the long pillars in the fourth set and a corresponding one of the long pillars in the fifth set and is electrically connected to the same. The fourth set is offset in the second direction by a first distance relative to the first set. The fifth set is offset in the second direction by the first distance relative to the second set. The sixth set is offset in the first direction by a second distance relative to the third set.

Regarding the yet another aspect of the present disclosure, the second set is offset in the second direction by a third distance relative to the first set. The fifth set is offset in the second direction by the third distance relative to the fourth set. The third distance is less than the first distance. Members of the first and second sets are located in a M(i) metallization layer of the IC, where i is a non-negative integer. Members of the third set are located in a M(i+1) metallization layer of the IC.

A still further aspect of the present disclosure is directed to a conductive line structure in an integrated circuit (IC), the conductive line structure comprising: lines; long pillars; and vias. Regarding the lines, they: are conductive; are non-overlapping of each other; and have long axes which are substantially parallel to a first direction; and are offset in a second direction relative to each other, the second direction being orthogonal to the first direction The long pillars organized into sets, wherein members of each set: are non-overlapping of each other; have long axes which are substantially coaxial and substantially parallel to the second direction; are offset in the second direction relative to each other; and are overlapping of corresponding ones of the lines. The long pillars also are organized into groups, wherein the groups: are offset in the first direction relative to each other; and each have a same quantity of the long pillars. For each group, member long pillars of the group: are non-overlapping of each other; and are offset, and aligned, in the first direction relative to each other. The vias electrically connect the long pillars with corresponding ones of the lines. For a reference portion of each of the lines, a first number of the long pillars which overlaps the reference portion is greater than a second number of long pillars which are electrically connected to the reference portion.

Regarding the still further aspect of the present disclosure, the members of each set are aligned in the first direction. The sets are offset in the second direction relative to each other. The lines are organized into bunches, each bunch including a J clusters, each cluster including K lines, J and K being positive integers. Adjacent clusters are offset from each other in the second direction by a first distance. Adjacent lines in each of the clusters are offset from each other in the second direction by a second distance, the second distance being less than the first distance. For each of the sets of long pillars, each of the long pillar members thereof overlaps J-1 clusters. For each of the sets, each of the long pillar members thereof is electrically connected to each of the members of J-2 clusters.

Regarding the still further aspect of the present disclosure, the lines in the first set are organized into first and second clusters of the lines. Adjacent members of the first cluster are offset from each other in the second direction by a first distance. Adjacent members of the second cluster are offset from each other in the second direction by the first distance. Members of the second cluster are offset in the second direction by a second distance relative to corresponding members of the first cluster. The second distance is less than the first distance. Members of the first set are located in a M(i) metallization layer of the IC, where i is a non-negative integer; and members of the F sets are located in a M(i+1) metallization layer of the IC. A total number of the groups is F, F being a positive integer, and wherein: the first number of long pillars is F; and the second number of long pillars is F−1.

An additional aspect of the present disclosure is directed to a method of generating a layout of a conductive line structure for an integrated circuit (IC), the layout being stored on a non-transitory computer-readable medium. Such a method includes: generating first and corresponding second sets of long pillar patterns; generating a third set of short pillars patterns; and generating first via patterns. The generating first and corresponding second sets of long pillar patterns includes arranging members of each of the first and second sets so as: to be non-overlapping of each other; to have long axes which are substantially coaxial to, and substantially parallel to, a first direction; and to have the second set be offset in a second direction relative to the first set, the second direction being orthogonal to the first direction. The generating a third set of short pillars patterns includes arranging members of the third set so as: to be non-overlapping of each other; to have long axes which are substantially parallel to the second direction; to be overlapping of corresponding long pillar patterns in the first and second sets; and to be organized into groups, each group having a first quantity of the short pillar patterns. The generating first via patterns includes arranging the first via patterns so as to electrically connect the short pillar patterns in the third set with corresponding ones of the long pillar patterns in the first and second sets. The generating a third set further includes: arranging members of the third set so that each short pillar pattern in each group of the third set overlaps a corresponding one of the long pillar patterns in the first set and a corresponding one of the long pillar patterns in the second set and is electrically connected to the same; arranging members of the third set so that each long pillar pattern in each of the first and second sets is overlapped by a second quantity of corresponding short pillar patterns and is electrically connected to the same; and setting the first quantity to be less than the second quantity. At least one of the generating first and corresponding second sets, the generating a third set or the generating first via patterns is executed by a processor of a computer.

Regarding the additional aspect of the present disclosure, the method further includes: fabricating, based on the layout, at least one of (A) one or more semiconductor masks or (B) at least one component in a layer of an inchoate semiconductor integrated circuit. The generating a third set of short pillar patterns further includes: arranging members of the third set to be aligned in the first direction.

Regarding the additional aspect of the present disclosure, the method further includes: generating fourth and corresponding fifth sets of long pillar patterns; generating a sixth set of short pillar patterns; and generating fourth via patterns. The generating fourth and corresponding fifth sets of long pillar patterns includes arranging members of each of the fourth and fifth sets so as: to be non-overlapping of each other; to have long axes which are substantially coaxial and substantially parallel to a fourth direction; and to have the fifth set be offset in a fifth direction relative to the fourth set, the fifth direction being orthogonal to the fourth direction. The generating a sixth set of short pillar patterns includes arranging members of the sixth set so as: to be non-overlapping of each other; to have long axes which are substantially parallel to the fifth direction; to be overlapping of corresponding long pillar patterns in the fourth and fifth sets; and to be organized into groups, each group having the first quantity of the short pillar patterns in the sixth set. The generating fourth via patterns includes arranging the fourth via patterns so as: to electrically connect the short pillar patterns in the sixth set with corresponding ones of the long pillar patterns in the fourth and fifth sets. The generating a sixth set further includes: arranging members of the sixth set so that each long pillar pattern in each of the fourth and fifth sets is overlapped by the second quantity of corresponding short pillar patterns in the sixth set and is electrically connected to the same; and arranging members of the sixth set so that each short pillar pattern in each group of the sixth set overlaps a corresponding one of the long pillar patterns in the fourth set and a corresponding one of the long pillar patterns in the fifth set and is electrically connected to the same. The generating fourth and corresponding fifth sets includes: offsetting the fourth set in the second direction by a first distance relative to the first set; offsetting the fifth set in the second direction by the first distance relative to the second set. The generating a sixth set yet further includes: offsetting the sixth set in the first direction by a second distance relative to the third set.

Regarding the additional aspect of the present disclosure, the generating first and corresponding second sets includes: offsetting the second set in the second direction by a third distance relative to the first set; and setting the third distance to be less than the first distance. The generating fourth and corresponding fifth sets includes: offsetting the fifth set in the second direction by the third distance relative to the fourth set. The generating first and corresponding second sets includes: locating members of the first and second sets in a M(i) metallization layer of the IC, where i is a non-negative integer; and the generating a third set of short pillar patterns further includes: locating members of the third set in a M(i+1) metallization layer of the IC.

Another still further aspect of the present disclosure is directed to a conductive line structure in an integrated circuit (IC). The conductive line structure includes first and second line segments which: are conductive; are non-overlapping of each other; and have long axes which are substantially parallel to a first direction. The conductive line structure also includes third and fourth line segments which: are conductive; are non-overlapping of each other; have long axes which are substantially parallel to a second direction, the second direction being orthogonal to the first direction; and overlap the corresponding first and second line segments. The second and fourth line segments are offset in the second direction relative to the corresponding first and third line segments; the second line segment is offset by an amount delta, Δ, in the first direction relative to the first line segment; and delta is less than a permitted minimum offset between neighboring coaxial line segments, MIN_{COAX}, such that $\Delta<\mathrm{MIN}_{COAX}$.

Regarding the another still further aspect of the present disclosure, the fourth line segment is offset in the second direction relative to the third line segment. The first and second line segments are short pillars. The third and fourth line segments are short pillars. Relative to a grid which includes instances of a first reference line and instances of a second reference line which are parallel to the corresponding first and second directions: the first and second line segments are coaxial with corresponding instances of the first reference line; and the third and fourth line segments are coaxial with corresponding instances of the second reference line; and the offset in the amount delta is equal to an offset between neighboring instances of first reference line. The conductive line structure arises in the context of a process node for a given semiconductor technology; and the offset in the amount delta is equal to a poly pitch of the process node. The first direction is the vertical direction; and the second direction is the horizontal direction. The another still further aspect of the present disclosure further includes fifth and sixth line segments which: are conductive; are non-overlapping of each other; have long axes which are substantially parallel to the first direction; and are overlapped by the corresponding third and fourth line segments; wherein the fifth and sixth line segments offset in the second direction relative to the corresponding first and second third line segments; wherein the sixth line segment is offset by the amount delta, Δ, in the first direction relative to the fifth line segment. The conductive line structure arises in the context of a process node for a given semiconductor technology; the offset in the amount delta is equal to a poly pitch of the process node. The fifth line and sixth line segments are offset by an amount of twice delta, 2*Δ, in the first direction relative to the corresponding first and second line segments.

Another aspect of the present disclosure is directed to a method of generating a layout of a conductive line structure for an integrated circuit (IC), the layout being stored on a non-transitory computer-readable medium. The method includes: generating first and second line segment patterns which: are conductive; are non-overlapping of each other; and have long axes which are substantially parallel to a first direction; generating third and fourth line segment patterns which: are conductive; are non-overlapping of each other; have long axes which are substantially parallel to a second direction, the second direction being orthogonal to the first direction; and overlap the corresponding first and second line segment patterns; offsetting the second and fourth line segment patterns in the second direction relative to the corresponding first and third line segment patterns; and offsetting the second line segment pattern by an amount delta, Δ, in the first direction relative to the first line segment pattern. Delta is less than a permitted minimum offset between neighboring coaxial line segment patterns, MIN_{COAX}, such that $\Delta<\mathrm{MIN}_{COAX}$.

Regarding the another aspect of the present disclosure, the method further includes: fabricating, based on the layout, at least one of (A) one or more semiconductor masks or (B) at least one component in a layer of an inchoate semiconductor integrated circuit. The method further includes offsetting the fourth line segment pattern in the second direction relative to the third line segment pattern. The first and second line segment patterns are short pillars. The third and fourth line segment patterns are short pillars. Relative to a grid which includes instances of a first reference line and instances of a second reference line which are parallel to the corresponding first and second directions, the method further includes: arranging the first and second line segment patterns to be coaxial with corresponding instances of the first reference line; and arranging the third and fourth line segment patterns to be coaxial with corresponding instances of the second reference line; and wherein the offset in the amount delta is equal to an offset between neighboring instances of first reference line. The conductive line structure arises in the context of a process node for a given semiconductor technology; and the offset in the amount delta is equal to a poly pitch of the process node. The first direction is the vertical direction; and the second direction is the horizontal direction. Fifth and sixth line segment patterns which: are conductive; are non-overlapping of each other; have long axes which are substantially parallel to the first direction; and are overlapped by the corresponding third and fourth line segment patterns; wherein the fifth and sixth line segment patterns offset in the second direction relative to the corresponding first and second third line segment patterns; wherein the sixth line segment pattern is offset by the amount delta, Δ, in the first direction relative to the fifth line segment pattern. The conductive line structure arises in the context of a process node for a given semiconductor technology; the offset in the amount delta is equal to a poly pitch of the process node. The fifth line and sixth line segment patterns are offset by an amount of twice delta, 2*Δ, in the first direction relative to the corresponding first and second line segment patterns.

A further aspect of the present disclosure is directed to a non-transitory, computer-readable medium comprising computer-executable instructions for carrying out a method of generating a layout of a conductive line structure for an integrated circuit (IC), the layout being stored on a non-transitory computer-readable medium. The method includes: generating first and second line segment patterns which: are conductive; are non-overlapping of each other; and have long axes which are substantially parallel to a first direction; generating third and fourth line segment patterns which: are conductive; are non-overlapping of each other; have long axes which are substantially parallel to a second direction, the second direction being orthogonal to the first direction; and overlap the corresponding first and second line segment patterns; offsetting the second and fourth line segment patterns in the second direction relative to the corresponding first and third line segment patterns; and offsetting the second line segment pattern by an amount delta, Δ, in the first direction relative to the first line segment pattern. Delta is less than a permitted minimum offset between neighboring coaxial line segment patterns, MIN_{COAX}, such that $\Delta<\mathrm{MIN}_{COAX}$.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. An integrated circuit (IC) structure comprising:

a first power rail positioned at a power rail level and oriented in a power rail direction;

a second power rail positioned at the power rail level and oriented in the power rail direction;

a plurality of first metal segments positioned at a first metal level above the power rail level, the plurality of first metal segments being oriented in a first metal level direction perpendicular to the power rail direction, the plurality of first metal segments including:

a first set of pairs of first metal segments alternating with a second set of pairs of first metal segments;

relative to the power rail direction, each pair of the first set of pairs of first metal segments is separated from another pair of the first set of pairs of first metal segments by a corresponding pair of the second set of pairs of first metal segments; and

relative to the power rail direction, each pair of the second set of pairs of first metal segments is separated from another pair of the second set of pairs of first metal segments by a corresponding pair of the first set of pairs of first segments;

a plurality of first vias between the power rail level and the first metal level, each first via of the plurality of first vias being positioned at a location where a corresponding first metal segment of the plurality of first metal segments correspondingly overlaps the first or second power rails;

a plurality of second metal segments positioned at a second metal level above the first metal level, the plurality of second metal segment being oriented in the power rail direction;

the plurality of second metal segments being organized into a first set and second set;

each second metal segment in the first set overlapping the first power rail but being free from overlapping the second power rail;

each second metal segment in the second set overlapping the second power rail but being free from overlapping the first power rail;

relative to the power rail direction, the first set of pairs of second metal segments alternating with the second set of pairs of second metal segments;

each member of the first set of pairs of second metal segments is electrically connected to a corresponding member of the first set of pairs of first metal segments;

each member of the second set of pairs of second metal segments is electrically connected to a corresponding member of the second set of pairs of first metal segments;

a plurality of second vias between the first metal level and the second metal level, each second via of the plurality of second vias being positioned at a location above a corresponding first via of the plurality of first vias;

a plurality of third metal segments at a third metal level above the second metal level, the plurality of third metal segments being oriented in the first metal level direction;

the plurality of third metal segments being arranged as a first set of pairs of third metal segments alternating with a second set of pairs of third metal segments;

relative to the power rail direction, each pair of the first set of pairs of third metal segments being separated from another pair of the first set of pairs of third metal segments by a corresponding pair of the second set of pairs of third metal segments; and

relative to the power rail direction, each pair of the second set of pairs of third metal segments being separated from another pair of the second set of pairs of third metal segments by a corresponding pair of the first set of pairs of third metal segments;

a plurality of third vias between the second metal level and the third metal level, each third via of the plurality of third vias being positioned at a location at which a third metal segment of the plurality of third metal segments correspondingly overlaps the first or second power rails;

one or more power straps positioned at a power strap level above the third metal level;

wherein:

the IC structure is configured to electrically connect the one or more power straps correspondingly to the first or second power rails;

each first metal segment of the plurality of first metal segments has a width corresponding to a predetermined minimum width for the first metal level;

the power strap has a width greater than a predetermined minimum width for the power strap level;

the plurality of third vias substantially overlap the plurality of first vias and the plurality of second vias;

the first set of pairs of first metal segments and the first set of pairs of third metal segments are electrically connected with the first power rail, but not electrically connected with the second power rail; and

the second set of pairs of first metal segments and the second set of pairs of third metal segments are electrically connected with the second power rail, but not electrically connected with the first power rail.

2. The IC structure of claim **1**, wherein:

the power strap is one power strap of a plurality of power straps oriented in the first metal level direction;

the IC structure further comprises:

a plurality of fourth metal segments at a fourth metal level above the third metal level and below the power strap level, the plurality of fourth metal segments being oriented in the power rail direction;

a plurality of fourth vias between the third metal level and the fourth metal level, each fourth via of the plurality of fourth vias being positioned at a location above a corresponding third via of the plurality of third vias; and

a plurality of fifth vias between the fourth metal level and the power strap level, each fifth via of the plurality of fifth vias being positioned at a location at which a power strap of the plurality of power straps overlaps a corresponding fourth metal segment of the plurality of fourth metal segments;

each third metal segment of the plurality of third metal segments has a width corresponding to a predetermined minimum width for the third metal level; and each fourth metal segment of the plurality of fourth metal segments has a width corresponding to a predetermined minimum width for the fourth metal level.

3. The IC structure of claim 1, wherein:

the plurality of first vias is organized into first sets and second sets which correspondingly electrically connect the first set of pairs of first metal segments to the first power rail and the second set of pairs of first metal segments to the second power rail; and

each second metal segment of the plurality of second metal segments has a width corresponding to a predetermined minimum width for the second metal level.

4. The IC structure of claim 3, wherein:

each pair of first metal segments of the first set of pairs of first metal segments and of the second set of pairs of first metal segments has a first pitch;

the pairs of first metal segments of the first set of pairs of first metal segments and the pairs of first metal segments of the second set of pairs of first metal segments have a second pitch; and

the second pitch is a multiple of the first pitch.

5. The IC structure of claim 1,

wherein each third metal segment of the plurality of third metal segments has a width corresponding to a predetermined minimum width for the third metal level.

6. The IC structure of claim 5, wherein:

each second metal segment of the plurality of second metal segments electrically connects a corresponding second via of the plurality of second vias to a corresponding third via of the plurality of third vias; and

each second metal segment of the plurality of second metal segments has a width corresponding to a predetermined minimum width for the second metal level.

7. The IC structure of claim 5, wherein:

the second metal segments correspondingly electrically connect the plurality of second vias to the plurality of third vias; and

each second metal segment has a width greater than a predetermined minimum width for the second metal level.

8. The IC structure of claim 1, wherein:

the plurality of first metal segments are configured as long pillars;

the plurality of second metal segments are configured as short pillars;

the plurality of third metal segments are configured as short pillars; and

each long pillar has a length less than or equal to Blech length.

9. The IC structure of claim 1, wherein:

each pair of the first set of pairs of first metal segments and of the second set of pairs of first metal segments has an intra-pair pitch;

the pairs of the first set of pairs of first metal segments and the pairs of the second set of pairs of first metal segments have an inter-pair pitch;

the inter-pair pitch is greater than the intra-pair pitch; and

the inter-pair pitch is a multiple of the intra-pair pitch.

10. An integrated circuit (IC) structure comprising:

a first power rail positioned at a power rail level and oriented in a power rail direction;

a second power rail positioned at the power rail level and oriented in the power rail direction;

a plurality of first metal segments overlapping the first power rail, the plurality of first metal segments being positioned at a metal segment level above the power rail level, the plurality of first metal segments being oriented perpendicular to the power rail direction;

a plurality of second metal segments overlapping the second power rail, the plurality of second metal segments being positioned at the metal segment level, the plurality of second metal segments being oriented perpendicular to the power rail direction;

a plurality of metal straps positioned at a metal strap level above the metal segment level, each metal strap of the plurality of metal straps overlapping the first power rail or the second power rail and being oriented in the power rail direction;

the plurality of metal straps includes:

a first set of metal straps alternating with a second set of metal straps;

each member of the first set of metal straps overlaps a corresponding one of the plurality of first metal segments; and

each member of the second set of metal straps overlaps a corresponding one of the plurality of second metal segments;

a plurality of metal stubs positioned at a metal stub level above the metal strap level, each metal stub of the plurality of metal stubs overlapping both the first power rail and the second power rail and being oriented perpendicular to a metal strap direction;

relative to the power rail direction, the plurality of metal stubs being arranged as a first set of metal stubs alternating with a second set of metal stubs;

each member of the first set of metal stubs electrically connected to the first set of metal straps;

each member of the second set of metal stubs electrically connected to the second set of metal straps;

a first power strap positioned at a power strap level above the metal stub level;

a second power strap positioned at the power strap level; and

a plurality of via arrays, a number of the via arrays being one less than a total number of metal levels, each via array including vias positioned at locations at which metal elements of corresponding adjacent metal levels overlap; and

wherein:

the IC structure is configured to electrically connect the first power strap to the first power rail and to separately electrically connect the second power strap to the second power rail;

each metal strap of the plurality of metal straps has a width corresponding to a predetermined minimum width for the metal strap level;

each metal stub of the plurality of metal stubs has a width corresponding to a predetermined minimum width for the metal stub level;

the plurality of first metal segments overlap the first power rail but are free from overlapping the second power rail;

the plurality of second metal segments overlap the second power rail but are free from overlapping the first power rail;

each of the first power strap and the second power strap has a width greater than a predetermined minimum width for the power strap level; and

the plurality of via arrays include a first via array between the power rail level and the metal segment level, a second via array between the metal segment level and the metal strap level, a third via array between the metal strap level and the metal stub level, the third via array substantially overlapping the first via array and the second via array.

11. The IC structure of claim **10**, wherein:

the first power strap is one first power strap of a plurality of first power straps oriented in the metal strap direction;

the second power strap is one second power strap of a plurality of second power straps oriented in the metal strap direction; and

the IC structure further comprises:

a plurality of metal islands at a metal island level above the metal stub level and below the power strap level, the plurality of metal islands being oriented in the power rail direction; each metal island of the plurality of metal islands having a width corresponding to a predetermined minimum width for the metal island level.

12. The IC structure of claim **10**, wherein:

each first metal segment of the plurality of first metal segments and each second metal segment of the plurality of second metal segments has a width corresponding to a predetermined minimum width for the metal segment level.

13. The IC structure of claim **10**, wherein:

each member of the first set of metal straps is electrically connected to the plurality of first metal segments;

each member of the second set of metal straps is electrically connected to the plurality of second metal segments; and

each of the plurality of first metal segments and the plurality of second metal segments has a width wider than a predetermined minimum width for the metal segment level.

14. The IC structure of claim **13**, wherein:

each corresponding location at which the plurality of first metal segments or the plurality of second metal segments overlap the plurality of metal stubs corresponds to a location at which a metal strap of the plurality of metal straps overlaps the plurality of first metal segments or the plurality of second metal segments.

15. An integrated circuit (IC) structure comprising:

a first power rail positioned at a power rail level and oriented in a power rail direction;

a second power rail positioned at the power rail level and oriented in the power rail direction;

first metal segments, configured as long pillars, and positioned at a first metal level above the power rail level, the first metal segments being oriented in a first metal direction perpendicular to the power rail direction;

the first metal segments including a first set of pairs of first metal segments alternating with a second set of pairs of first metal segments;

relative to the power rail direction, each pair of the first set of pairs of first metal segments is separated from another pair of the first set of pairs of first metal segments by a corresponding pair of the second set of pairs of first metal segments;

each member of the first set of pairs of first metal segments overlapping the first power rail;

each member of the second set of pairs of first metal segments overlapping the second power rail; and

relative to the power rail direction, each pair of the second set of pairs of first metal segments is separated from another pair of the second set of pairs of first metal segments by a corresponding pair of the first set of pairs of first metal segments;

first vias between the power rail level and the first metal level, the first vias being positioned at locations where corresponding ones of the first metal segments overlap the first power rail;

second metal segments, configured as short pillars, and positioned at a second metal level above the first metal level, the second metal segments overlapping the first power rail or the second power rail and being oriented in the power rail direction;

the second metal segments including:

relative to the power rail direction, a first set of second metal segments alternating with a second set of second metal segments;

each member of the first set of second metal segments overlapping and electrically connected to a corresponding member of the first set of first metal segments, but being free from overlapping the second power rail;

each member of the second set of second metal segments overlapping and electrically connected to a corresponding member of the second set of first metal segments, but being free from overlapping the first power rail;

second vias between the first metal level and the second metal level, the second vias being positioned at locations above corresponding ones of the first vias;

third metal segments, configured as short pillars, and positioned at a third metal level above the second metal level, the third metal segments correspondingly overlapping the second metal segments and being oriented in the first metal direction;

the third metal segments being arranged as a first set of pairs of third metal segments alternating with a second set of pairs of third metal segments;

relative to the power rail direction, each pair of the first set of pairs of third metal segments being separated from another pair of the first set of pairs of third metal segments by a corresponding pair of the second set of pairs of third metal segments;

relative to the power rail direction, each pair of the second set of pairs of third metal segments being separated from another pair of the second set of pairs of third metal segments by a corresponding pair of the first set of pairs of third metal segments;

third vias between the second metal level and the third metal level, each third via of the third vias being positioned at a location at which a third metal segment of the third metal segments correspondingly overlaps the first or second power rails; and

one or more power straps positioned at a power strap level above the third metal level;

wherein:

the IC structure is configured to electrically connect the first or second power rails to the one of more power straps;

the third vias substantially overlap the first vias and the second vias;

the first set of pairs of first metal segments and the first set of pairs of third metal segments are electrically connected with the first power rail, but not electrically connected with the second power rail;

the second set of pairs of first metal segments and the second set of pairs of third metal segments are electrically connected with the second power rail, but not electrically connected with the first power rail;

a long axis of each long pillar has a length less than Blech length;

a long axis of each short pillar is substantially shorter than a shortest long axis of the long pillars.

16. The IC structure of claim **15**, wherein:

the first vias electrically connects the first set of pairs of first metal segments to the first power rail and the second set of pairs of first metal segments to the second power rail; and

each one of the second metal segments overlaps the first and second power rails at locations at which a corresponding pair of the first set of pairs of first metal segments overlap the first power rail and a corresponding pair of the second set of pairs of first metal segments overlap the second power rail.

17. The IC structure of claim **15**, wherein:

each pair of the first set of pairs of first metal segments has a first pitch;

the pairs of the first set of first metal segments and of the second set of first metal segments have a second pitch; and

the second pitch is a multiple of the first pitch.

18. The IC structure of claim **15**, wherein:

the first vias are organized into first sets and second sets which correspondingly electrically connect the first set of pairs of first metal segments to the first power rail and the second set of pairs of first metal segments to the second power rail; and

each second metal segment of the second metal segments has a width corresponding to a predetermined minimum width for the second metal level.

19. The IC structure of claim **18**, wherein:

each pair of first metal segments of the first set of pairs of first metal segments and of the second set of pairs of first metal segments has a first pitch;

the pairs of first metal segments of the first set of pairs of first metal segments and the pairs of first metal segments of the second set of pairs of first metal segments have a second pitch; and

the second pitch is a multiple of the first pitch.

20. The IC structure of claim **15**, wherein each third metal segment of the third metal segments has a width corresponding to a predetermined minimum width for the third metal level.

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