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(54) **LEAKAGE RESISTANT RRAM/MIM STRUCTURE**

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H01L 45/00 (2006.01)

H01L 49/02 (2006.01)

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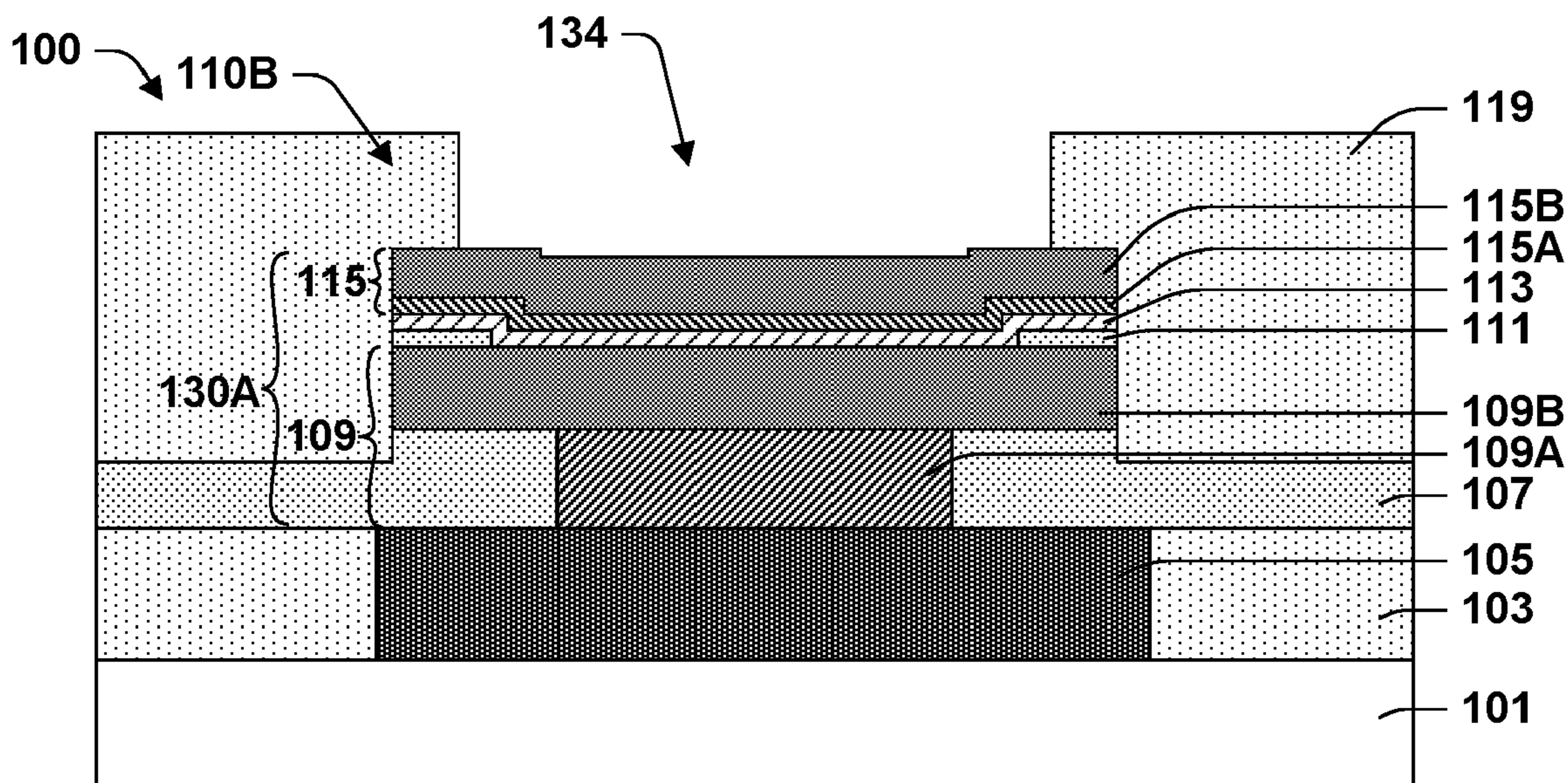
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(57) **ABSTRACT**

In some methods, a contact is formed over a substrate, and a bottom electrode layer is formed over the contact. A first dielectric layer is formed to cover a peripheral portion of the bottom electrode layer but not a central portion of the bottom electrode layer. A second dielectric layer is formed over the first dielectric layer. The second dielectric layer includes a central dielectric region that contacts the central portion of the bottom electrode layer, and a peripheral dielectric region over the peripheral portion of the bottom electrode. A step dielectric region connects the central and peripheral dielectric regions. A top electrode layer is formed over the second dielectric layer. The top electrode layer includes a central top electrode region, a peripheral top electrode region, and a step top electrode region directly above the central dielectric region, the peripheral dielectric region, and the step dielectric region, respectively.

20 Claims, 7 Drawing Sheets



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division of application No. 14/261,526, filed on Apr. 25, 2014, now Pat. No. 9,728,719.

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(52) **U.S. Cl.**

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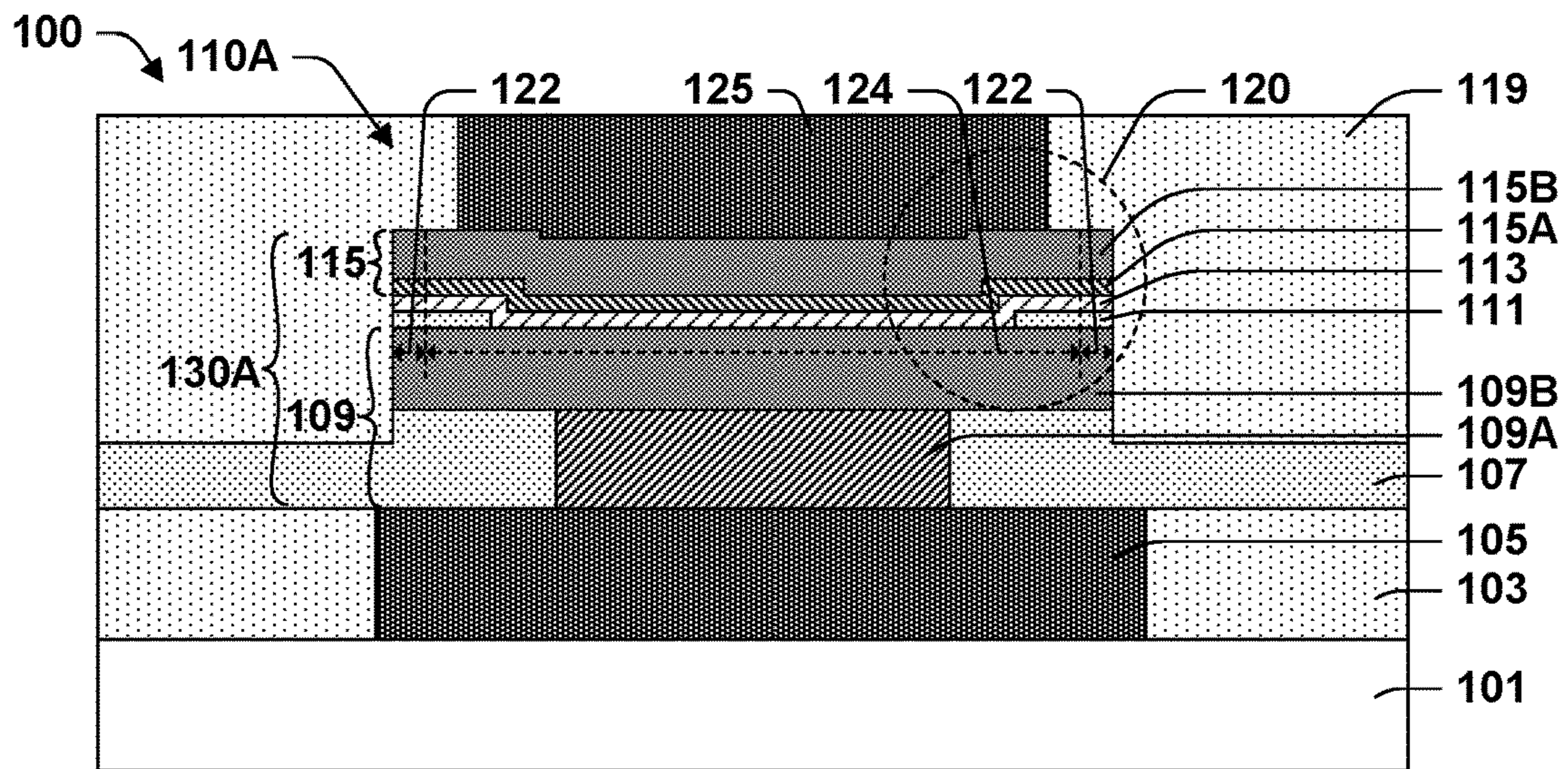


Fig. 1

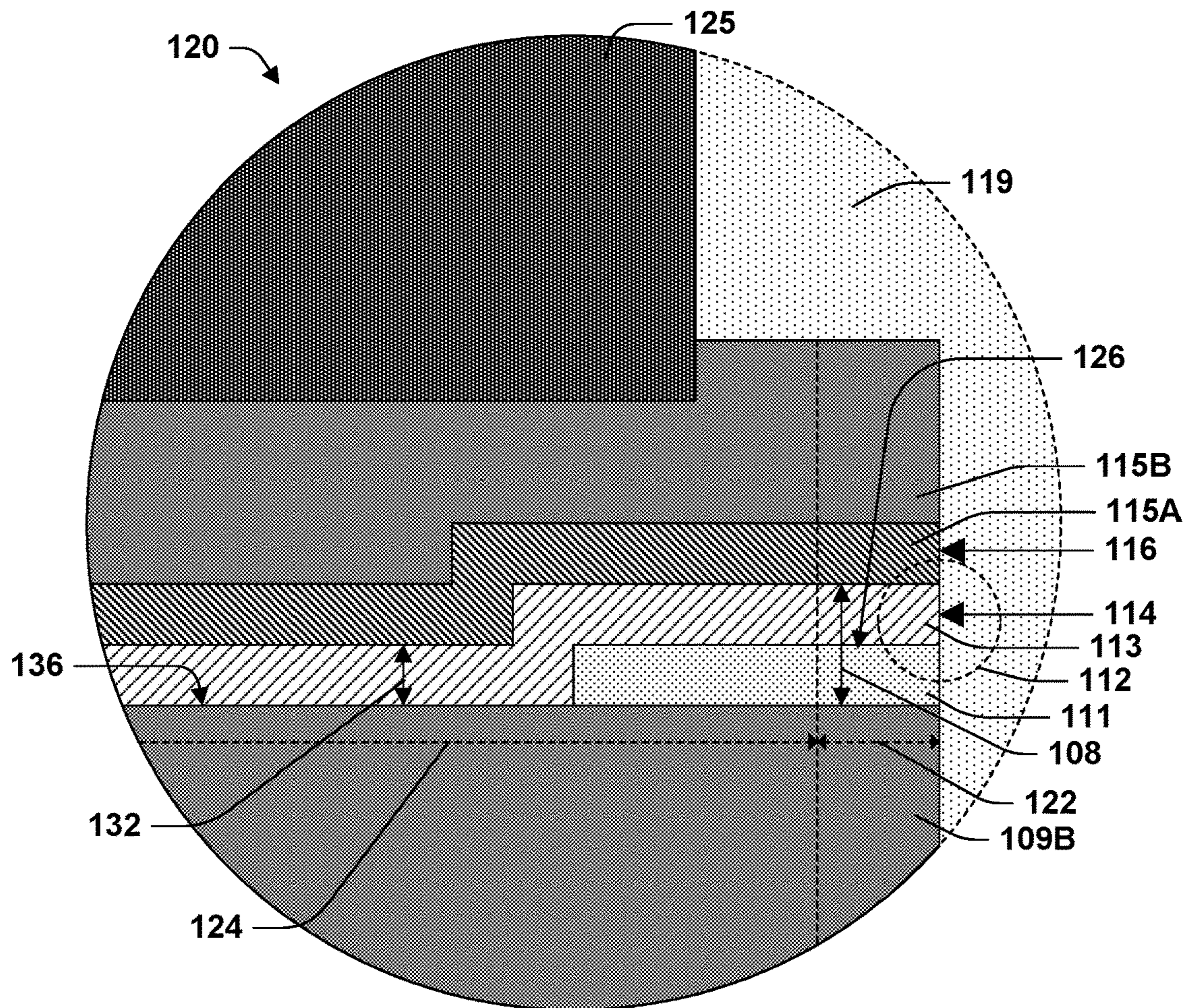


Fig. 2

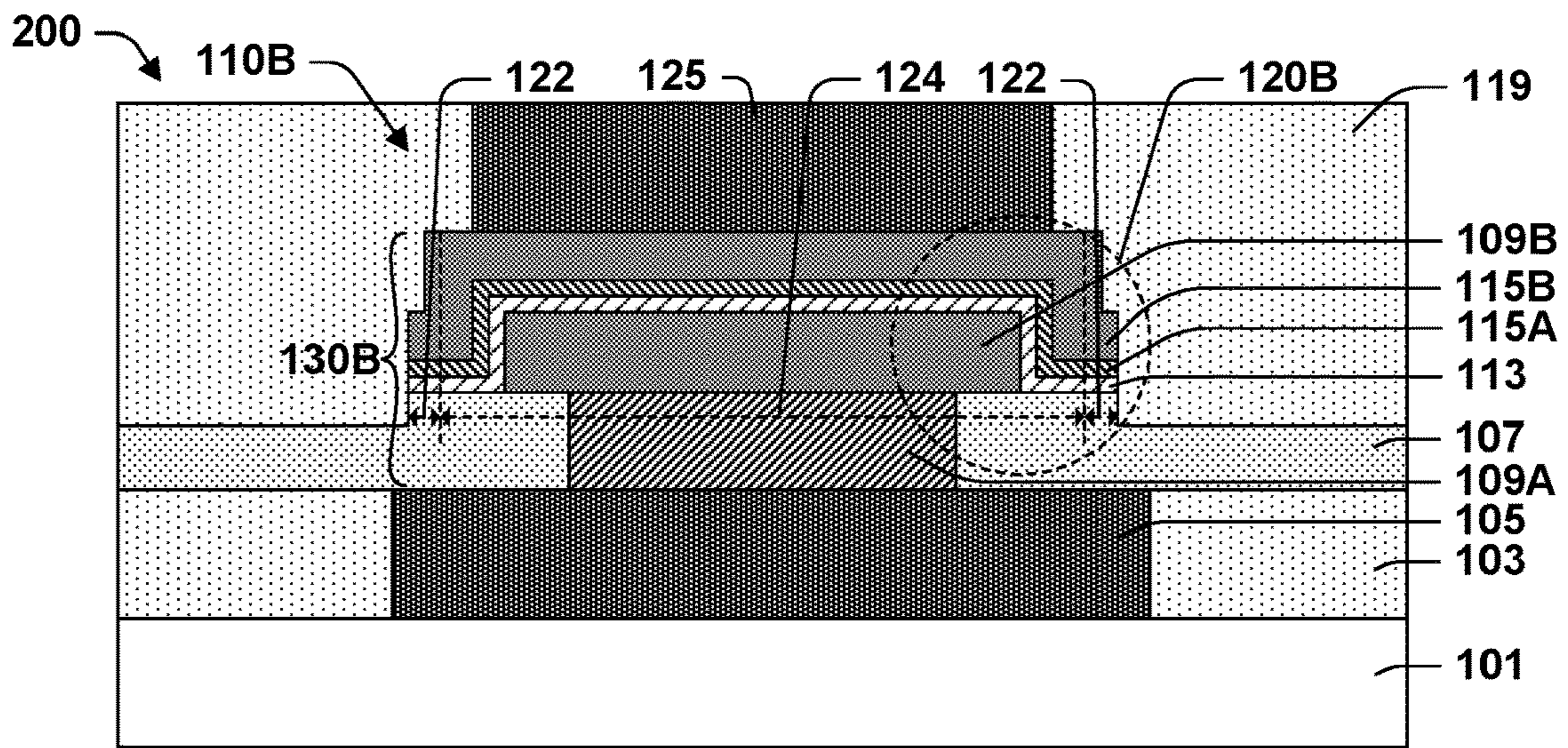


Fig. 3

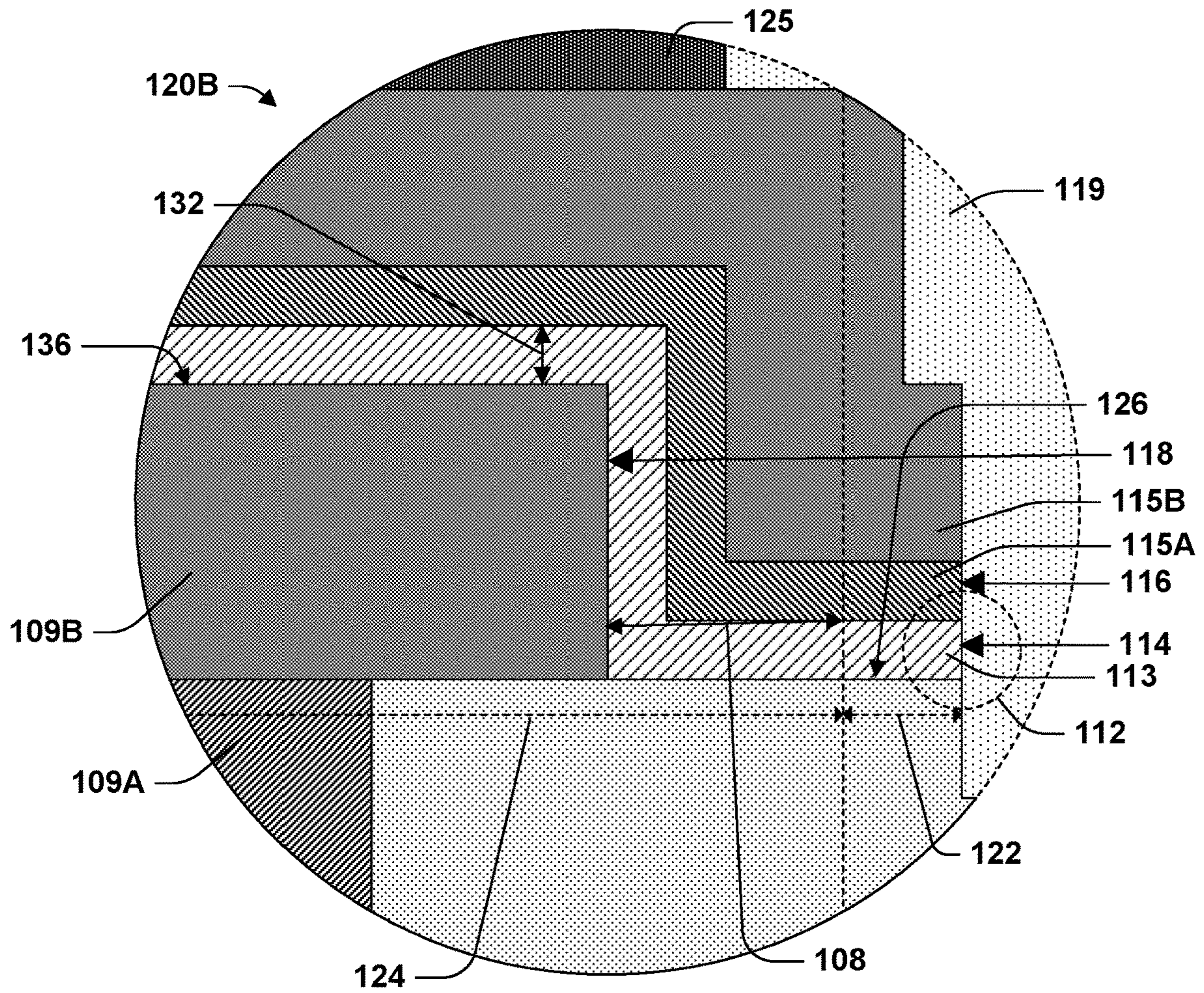


Fig. 4

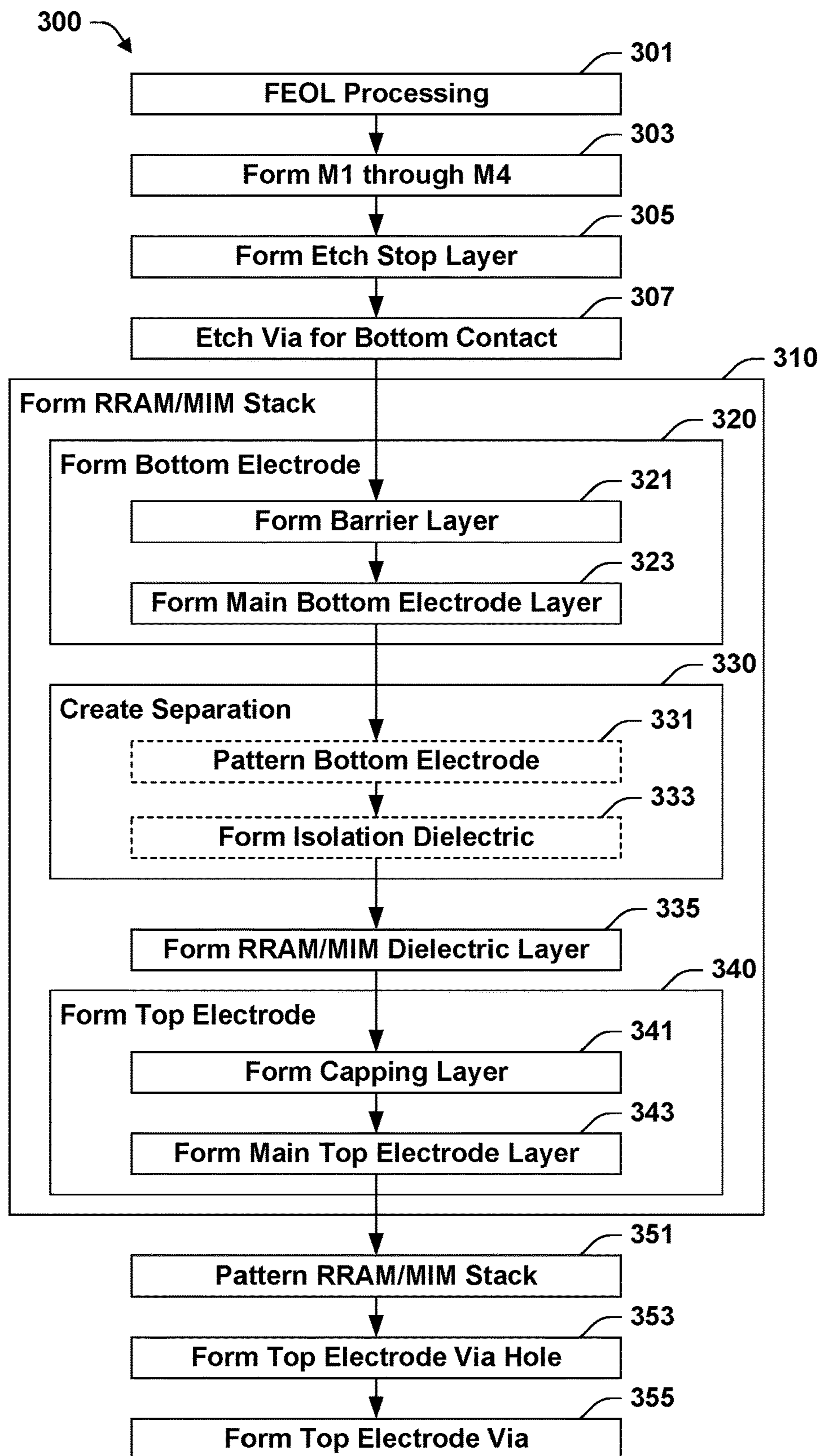


Fig. 5

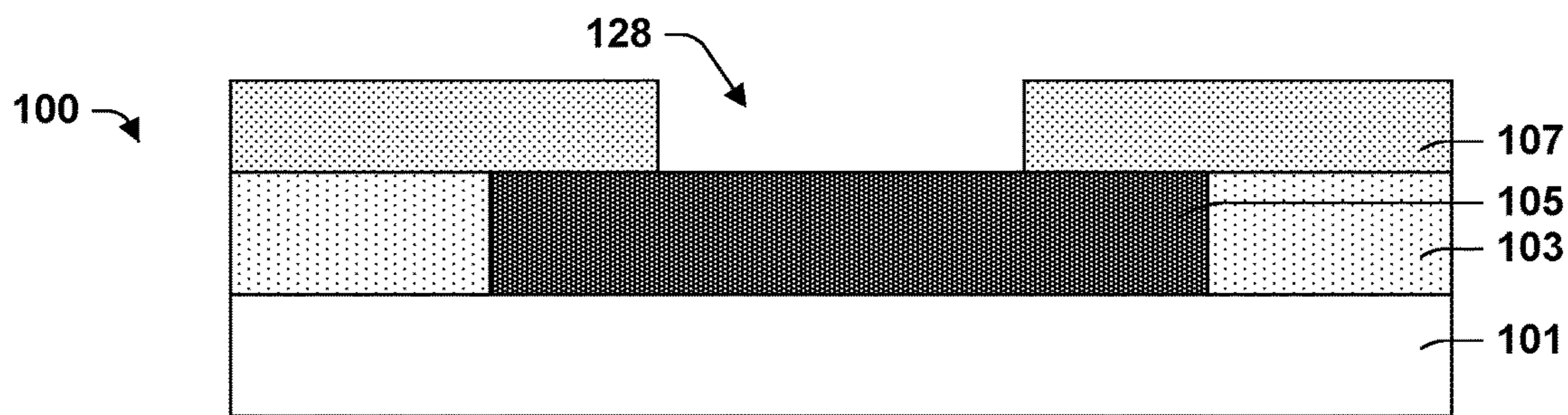


Fig. 6

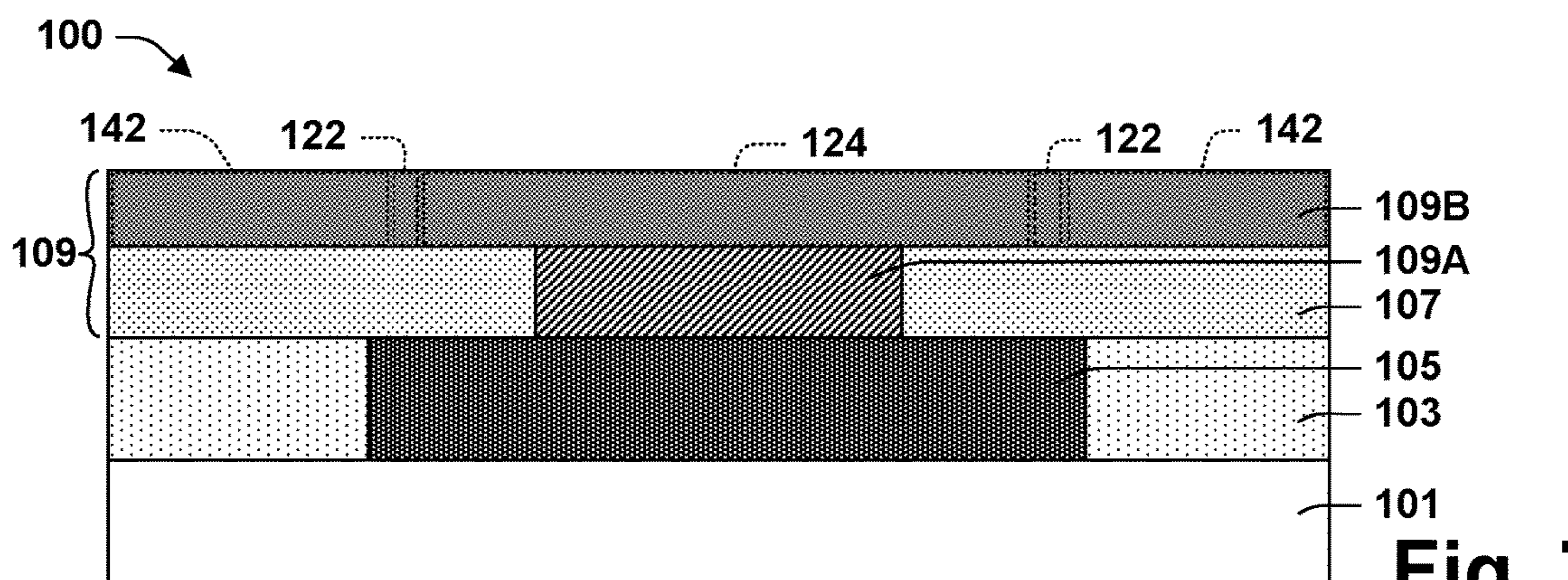


Fig. 7A

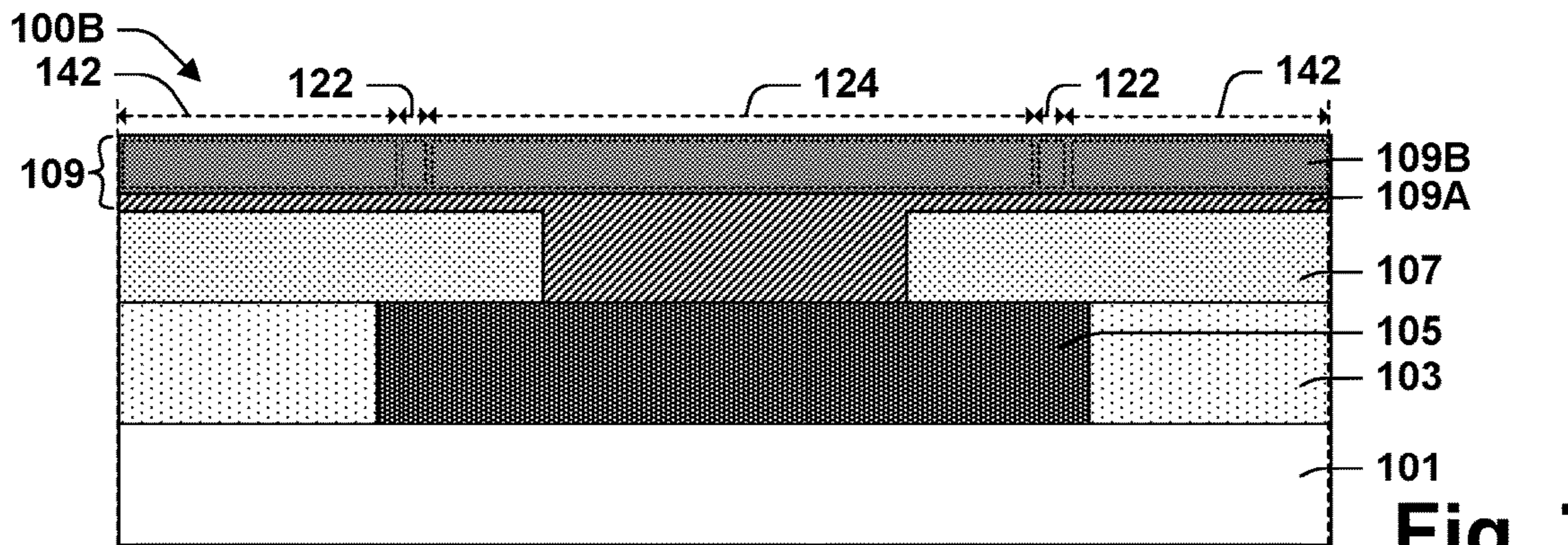


Fig. 7B

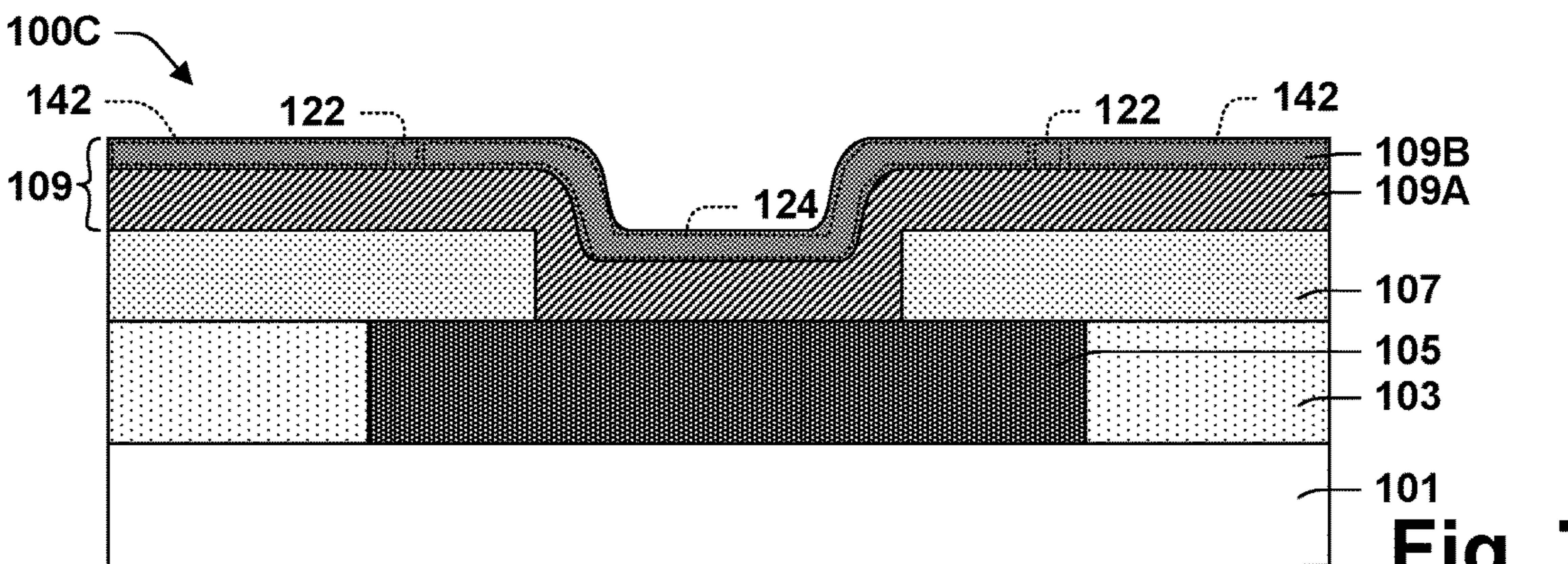


Fig. 7C

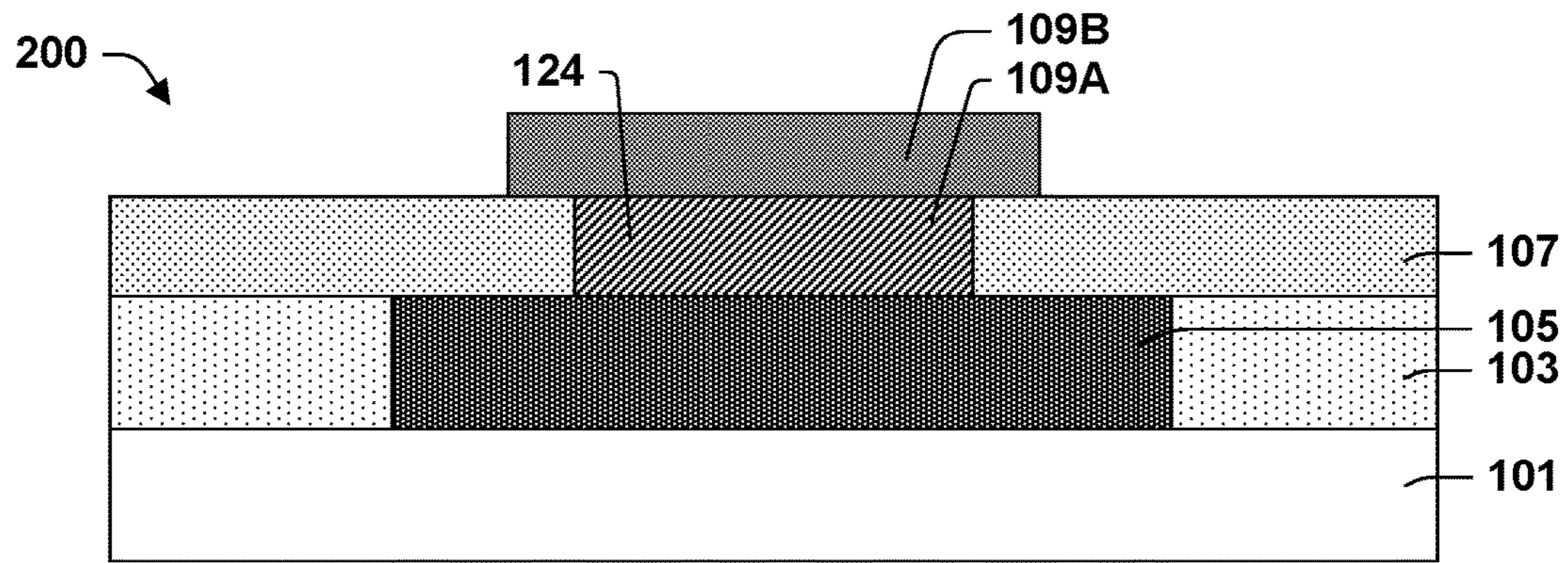


Fig. 8

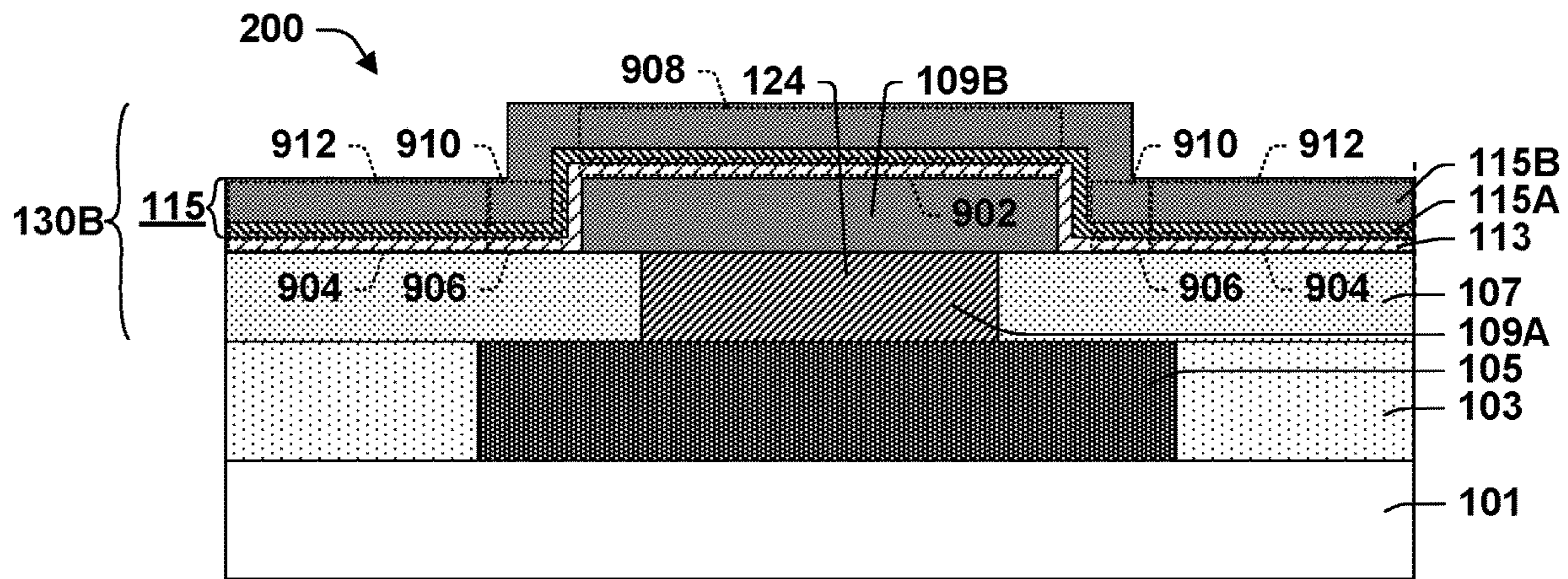


Fig. 9

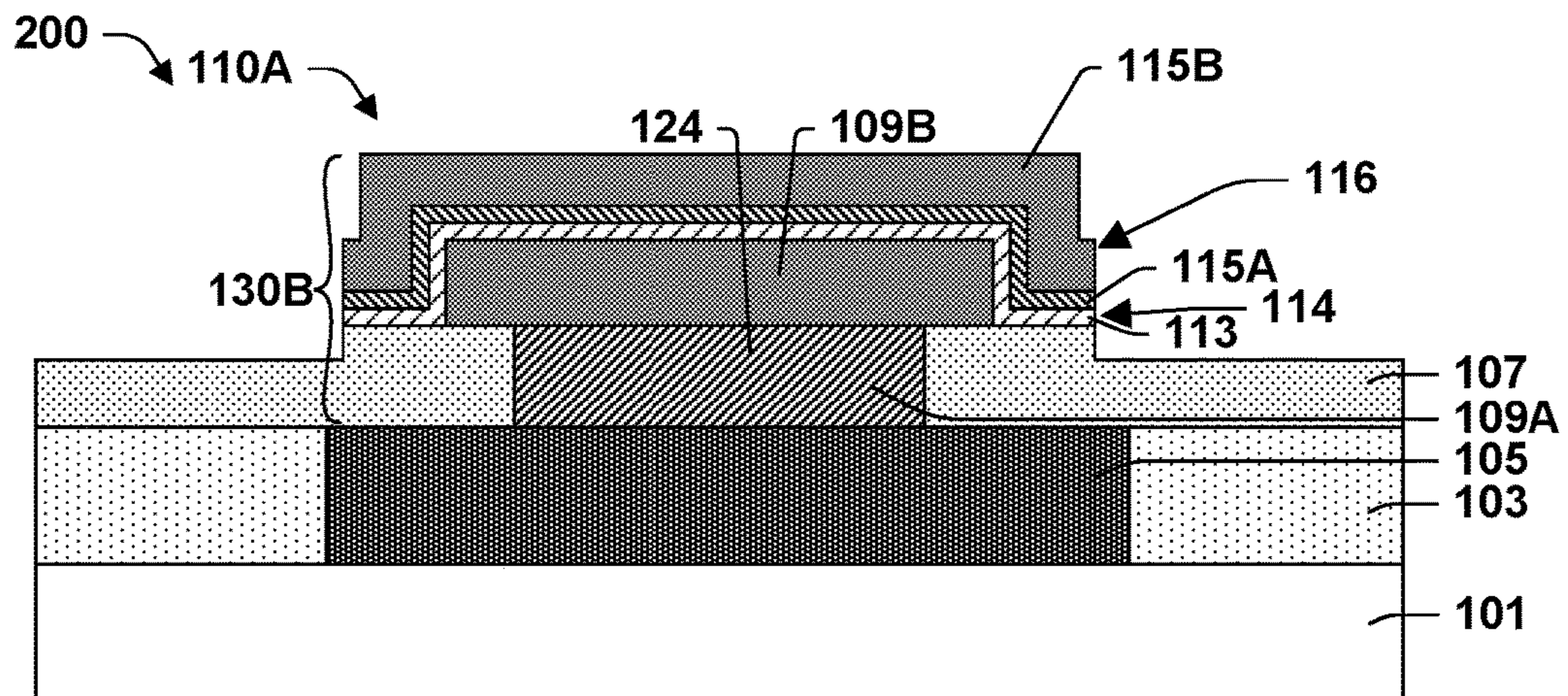


Fig. 10

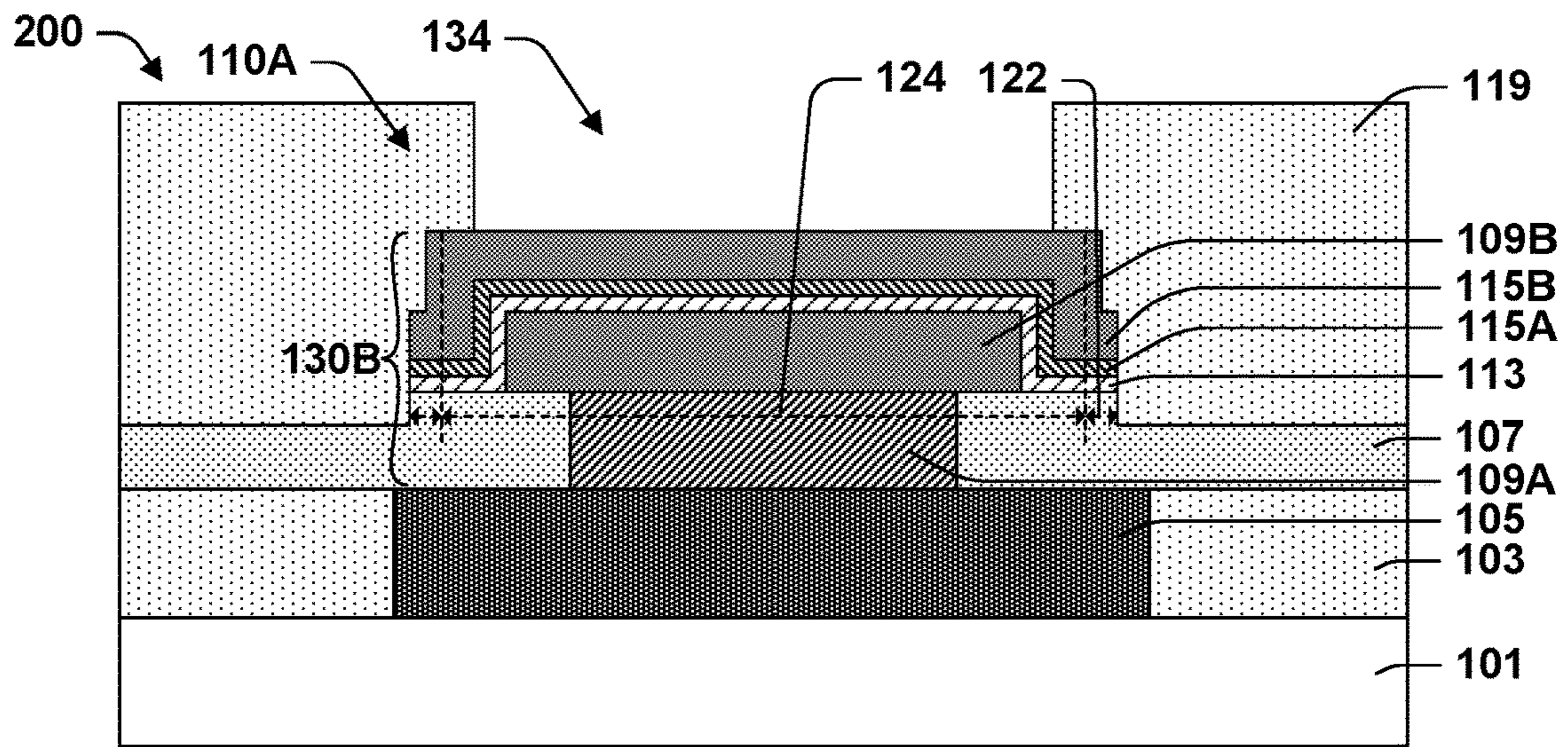


Fig. 11

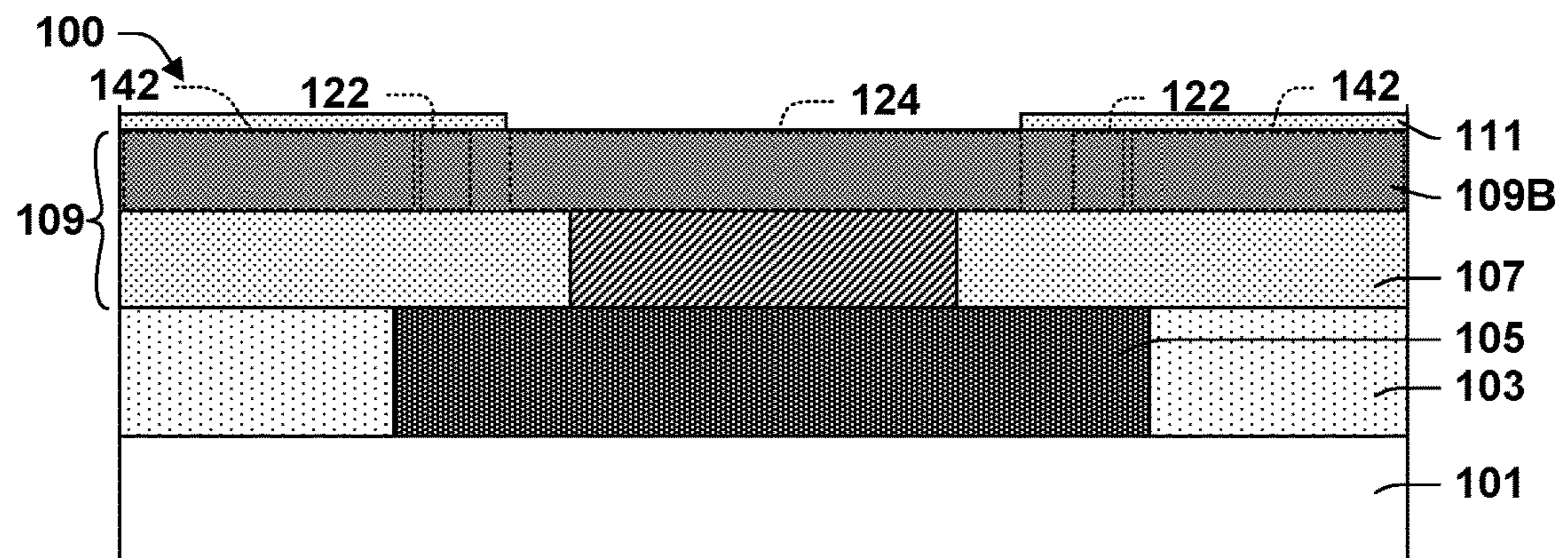


Fig. 12

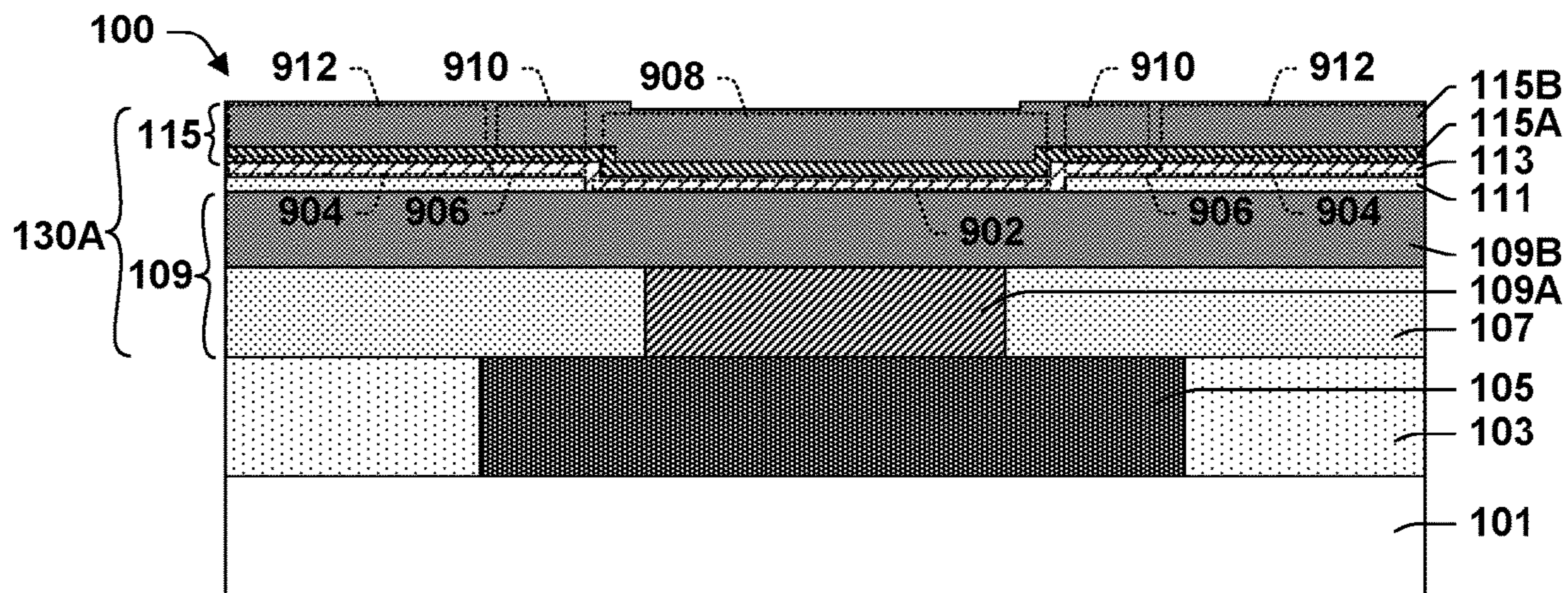


Fig. 13

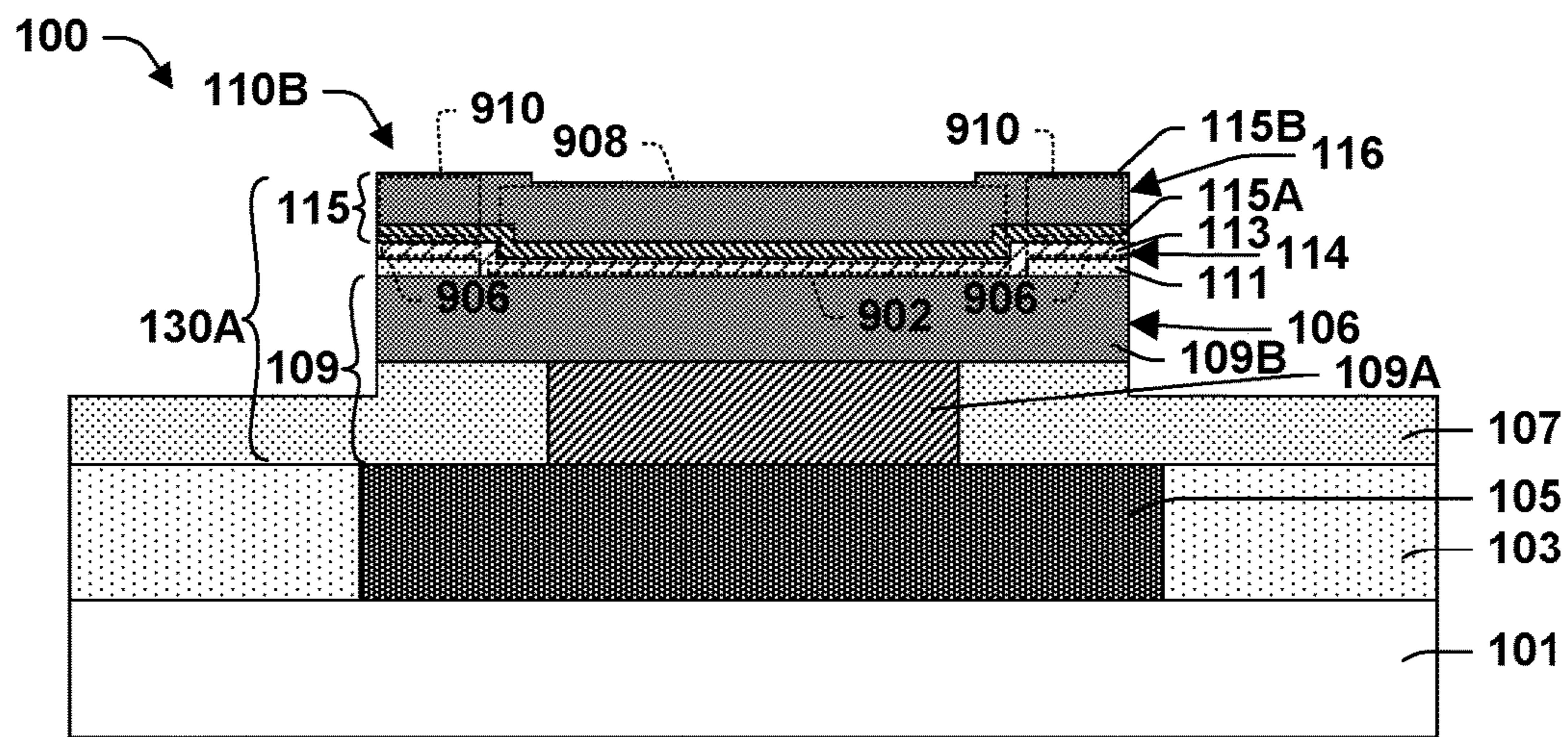


Fig. 14

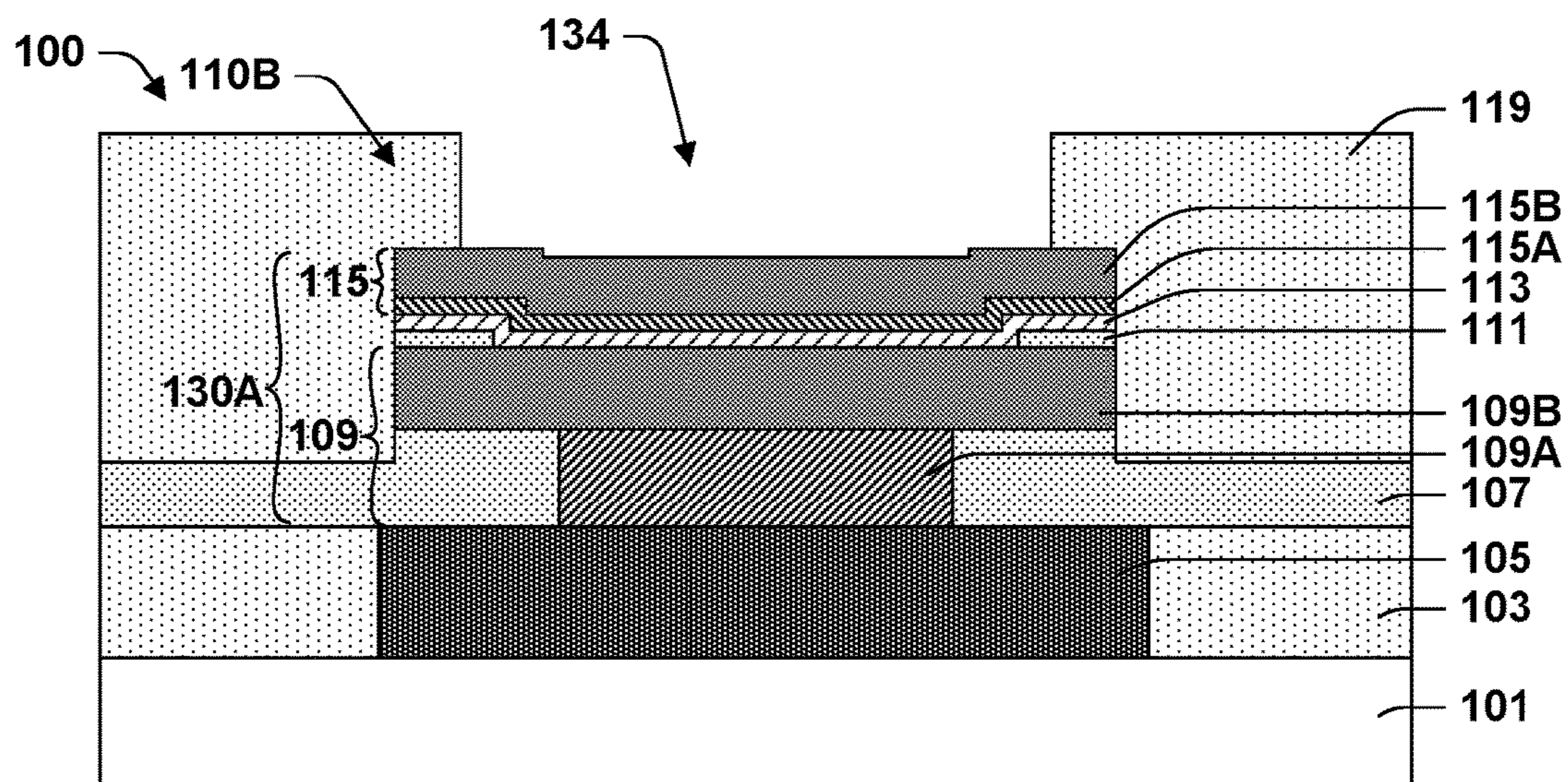


Fig. 15

1**LEAKAGE RESISTANT RRAM/MIM
STRUCTURE**

REFERENCE TO RELATED APPLICATIONS

This Application is a Divisional of U.S. application Ser. No. 15/647,579, filed on Jul. 12, 2017, which is a Divisional of U.S. application Ser. No. 14/261,526, filed on Apr. 25, 2014 (now U.S. Pat. No. 9,728,719, issued on Aug. 8, 2017). The contents of the above-referenced Patent Applications are hereby incorporated by reference in their entirety.

BACKGROUND

The present disclosure relates to integrated circuit devices with resistive random access memory or metal-insulator-metal capacitors, methods of making such devices, and methods of operating such devices.

Resistive random access memory (RRAM) has a simple structure, low operating voltage, high-speed, good endurance, and CMOS process compatibility. RRAM is a promising alternative to provide a downsized replacement for traditional flash memory and is finding wide application in devices such as optical disks and non-volatile memory arrays.

An RRAM cell stores data within a layer of material that can be induced to undergo a phase change. The phase change can be induced within all or part of the layer to switch between a high resistance state and a low resistance state. The resistance state can be queried and interpreted as representing either a "0" or a "1".

In a typical RRAM cell, the data storage layer includes an amorphous metal oxide. Upon application of a sufficient voltage, a metallic bridge is induced to form across the data storage layer, which results in the low resistance state. The metallic bridge can be disrupted and the high resistance state restored by applying a short high current density pulse that melts or otherwise breaks down all or part of the metallic structure. The data storage layer quickly cools and remains in the high resistance state until the low resistance state is induced again. RRAM cells are typically formed after front-end-of-line (FEOL) processing. In a typical design, an array of RRAM cells is formed between a pair of metal interconnect layers.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. 1 is an illustration of an integrated circuit device providing an example in accordance with a first group of embodiments provided by the present disclosure.

FIG. 2 is an expanded view of a portion of FIG. 1.

FIG. 3 is an illustration of an integrated circuit device providing an example in accordance with a second group of embodiments provided by the present disclosure.

FIG. 4 is an expanded view of a portion of FIG. 3.

FIG. 5 is a flow chart of a method, which is an example in accordance with some embodiments of the present disclosure.

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FIGS. 6 and 7A illustrate a device, which can be the device of FIG. 1 or the device of FIG. 3, as it begins manufacture according to the process of FIG. 5.

FIGS. 7B-7C illustrate alternative structures for the bottom electrode and provide alternative embodiments within either the group of embodiments represented by the device of FIG. 1 or the group of embodiments represented by the device of FIG. 3.

FIGS. 8 to 11 illustrate the device of FIG. 1 as it undergoes further processing according to the method of FIG. 5.

FIGS. 12 to 15 illustrate the device of FIG. 3 as it undergoes further processing according to the method of FIG. 5.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

It has been observed that an RRAM dielectric can be damaged or contaminated by etching and that this can lead to leakage currents through a peripheral region adjacent an outer edge of the RRAM dielectric layer. The present disclosure provides a method and resulting structures in which such leakage does not occur. The method modifies the structure of the RRAM cell stack to cause the separation between the top electrode and the bottom electrode to be substantially greater about a peripheral region of the top electrode in comparison to a minimum separation that occurs in a central region. In a first group of embodiments, the additional separation is created by forming an extra layer of dielectric in the peripheral region. In a second group of embodiments, the additional separation is created by cutting off the bottom electrode short of the peripheral region. In alternate embodiments these method and structures are applied to form metal-insulator-metal (MIM) capacitors, which are generally similar in structure to RRAM cells.

FIGS. 1 and 2 illustrate a metal-insulator-metal structure 110A in an integrated circuit device 100, which is an example within the first group of embodiments provided by the present disclosure. The metal-insulator-metal structure

110A is typically one cell in an array of similar cells. In some embodiments, the metal-insulator-metal structure 110A is an RRAM cell. In some other embodiments, the metal-insulator-metal structure 110A is an MIM capacitor. The device 100 includes a substrate 101 over which is formed a contact 105 within a matrix of dielectric 103. In most embodiments substrate 101 includes one or more metal interconnect layers formed over a semiconductor body.

Contact 105 can connect to a switching device for selecting metal-insulator-metal structure 110A. A switching device can be formed on the semiconductor body within substrate 101. In some embodiments the switching device is a transistor and the structure 110A is one in an array of RRAM cells having the 1T1R architecture. In some embodiments, the switching device is a diode and the structure 110A is one in an array of RRAM cells having the 1D1R architecture. In some embodiments, the switching device is a bipolar junction transistor and the structure 110A is one in an array of RRAM cells having the 1BJT1R architecture. In some embodiments, the switching device is a bipolar switch and the structure 110A is one in an array of RRAM cells having the 1S1R architecture. In some embodiments, there is no switching device and the structure 110A is one in an array of RRAM cells having the 1R architecture.

An RRAM/MIM (RRAM cell or MIM capacitor) stack 130A is formed over the contact 105. Contact 105 and dielectric 103 can be part of a metal interconnect layer formed over the substrate 101. In some embodiments, the structure 110A is an RRAM cell and contact 105 and dielectric 103 are part of the fourth (M4) metal interconnect layer. In some embodiments, an etch stop layer 107 is formed over the metal interconnect layer that includes contact 105. In those embodiments, etch stop layer 107 can include an opening over contact 105 that allows RRAM/MIM stack 130A to interface with contact 105.

RRAM/MIM stack 130A includes bottom electrode 109, a dielectric layer 113, which can be an RRAM dielectric, top electrode 115, and an additional dielectric layer 111. Bottom electrode 109 can include diffusion barrier layer 109A and main bottom electrode layer 109B. Top electrode 115 can include capping layer 115A and main top electrode layer 115B. RRAM/MIM stack 130A includes a central region 124 and a peripheral region 122. Additional dielectric layer 111 extends through peripheral region 122, but not through central region 124.

Top electrode 115 covers an upper surface of dielectric layer 113. Dielectric layer 113 covers an upper surface of bottom electrode 109. In some embodiments, top electrode 115 is coextensive with dielectric layer 113. In some embodiments, top electrode 115 and bottom electrode 109 shadow the same area of substrate 101.

FIG. 2 provides an expanded view of the region 120 identified in FIG. 1. As shown in FIG. 2, the distance 108, which is the shortest distance between any point on top electrode 115 within peripheral region 122 and any point on bottom electrode 109, is much greater than the shortest distance 132 between any point on top electrode 115 within central region 122 and bottom electrode 109. In some embodiments, the distance 108 is at least about twice the distance 132. In most embodiments, dielectric layer 111 has a lower dielectric constant than the material of dielectric layer 113. In most embodiments, the resistance along the shortest path 108 from top electrode 115 in peripheral region 122 to bottom electrode 109 is more than twice the resistance along the shortest path 132 from top electrode 115 in central region 124 to bottom electrode 109.

Dielectric layer 113 may be damaged or contaminated as a result of etching near an edge 114. Any such damage or contamination is restricted to an area 112 proximate edge 114 and will not significantly affect the performance of the device 100. The area 112 is entirely within peripheral region 122. Because of the greater electrode separation along pathways through peripheral region 122, leakage will not occur to any significant degree through peripheral region 122. In embodiments where structure 110A is an RRAM cell, conductive bridges will ordinarily not form through any portion of dielectric layer 113 that is in peripheral region 122. Conductive bridges will form exclusively within central region 124.

FIGS. 3 and 4 illustrate a metal-insulator-metal structure 110B in an integrated circuit device 200, which is an example within the second group of embodiments provided by the present disclosure. In some embodiments, the metal-insulator-metal structure 110B is an RRAM cell. In some other embodiments, the metal-insulator-metal structure 110B is an MIM capacitor. The description of integrated circuit device 100 and its embodiments applies to integrated circuit device 200 with two differences: additional dielectric layer 111 can be absent from metal-insulator-metal structure 110B and in metal-insulator-metal structure 110B, bottom electrode 109 is cut off short of peripheral region 122. As a consequence, in metal-insulator-metal structure 110B bottom electrode 109 lies exclusively within central region 124 and bottom electrode 109 shadows a smaller area of substrate 101 than top electrode 115. In most of these embodiments, dielectric 113 covers an edge surface 118 of bottom electrode as shown in FIG. 4.

FIG. 4 provides an expanded view of the region 120B identified in FIG. 3. As shown in FIG. 4, shortest distance 108 between top electrode 115 in peripheral region 122 and any point on bottom electrode 109 lies in a different direction for device 200 as compared to device 100, but distance 108 is still much greater than the shortest distance 132 within central region 122. Accordingly, device 200 achieves the same results as device 100.

As shown in FIGS. 2 and 4, in both structure 110A and 110B, the base 136 of dielectric layer 113 within central region 124 contacts bottom electrode 109, but the base 126 of dielectric layer 113 within peripheral region 122 does not. In embodiments represented by structure 110A, this is because additional dielectric layer 111 separates dielectric layer 113 from bottom electrode 109 in peripheral region 122. In embodiments represented by structure 110B, this is because bottom electrode 109 is absent beneath dielectric layer 113 in peripheral region 122. In both groups of embodiments, a shortest-distance path from top electrode 115 to bottom electrode 109 is not found in region 112 where dielectric layer 113 may be damaged by etching that forms edge 114.

FIG. 5 provides a flow chart of a method 300, which is an example according to another embodiment of the present disclosure. The method 300 can be used to form the device 100 or the device 200. Some embodiments of manufacturing methods are described below with reference to FIGS. 6-15, which depict incremental manufacturing steps as a series of cross-sectional views. More particularly FIGS. 6-11 show one manufacturing methodology embodiment for manufacturing device 200 while FIGS. 12-15 show another manufacturing methodology embodiment for manufacturing device 100.

In FIG. 6, process 300 begins with optional acts of completing front-end-of-line (FEOL) processing (FIG. 5, act 301 and act 303) in which first (M1) through fourth (M4), contact 105, and dielectric layer 103 are formed. An etch

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stop layer 107 is then formed over the metal interconnect layer on substrate 101 (FIG. 5, act 305) and a hole 128 is formed through etch stop layer 107 to expose contact 105 as show in FIG. 6.

Process 300 continues with a series of acts 310 that form RRAM/MIM stack 130 (RRAM/MIM stack 130A or RRAM/MIM stack 130B). An example of how this RRAM/MIM stack 130A is now described below.

FIGS. 7A-7C shows several different ways to form bottom electrode 109 (FIG. 5, act 320), which can include one or more layers. For example, in the illustrated embodiments of FIGS. 7A-7C, a diffusion barrier layer 109A can be formed (FIG. 5, act 321), and a main bottom electrode layer 109B is then formed thereover (FIG. 5, act 323). Diffusion barrier layer 109A can be included to prevent contamination of main bottom electrode layer 109B by material from underlying contact 105. In some embodiments contact 105 is copper and diffusion barrier layer 109A is a material TiN for example, that provides an effective barrier to copper diffusion. In general, diffusion barrier layer 109A can have any suitable composition. In most embodiments, diffusion barrier layer 109A is a conductive oxide, nitride, or oxynitride of a metal selected from the group consisting of Al, Mn, Co, Ti, Ta, W, Ni, Sn, Mg, and combinations thereof. Diffusion barrier layer 109A can have any suitable thickness. A suitable thickness is large enough to provide an effective diffusion barrier while not being so large as to cause excessive resistance. In most embodiments, the thickness of diffusion barrier layer 109A is in the range from 20 Å to 300 Å. In some embodiments, the thickness of diffusion barrier layer 109A is in the range from 100 Å to 300 Å, for example, 200 Å.

Main bottom electrode layer 109B can have any suitable composition. Examples of compositions that can be suitable include, without limitation, metals, metal nitrides, and doped polysilicon. In some embodiments, bottom electrode layer 109B is a metal. The metal can be, for example, Al, Ti, Ta, Au, Pt, W, Ni, Ir, Cu, or a combination thereof. In some embodiments, bottom electrode layer 109B is a metal nitride. The metal nitride can be, for example, TaN. In some embodiments, bottom electrode layer 109B is a doped polysilicon. A doped polysilicon can be either a p+ doped polysilicon or an n+ doped polysilicon. In most embodiments, the thickness of bottom electrode layer 109B is in the range from 20 Å to 200 Å. In some embodiments, the thickness of bottom electrode layer 109B is in the range from 50 Å to 150 Å, for example, 100 Å.

The bottom electrode layers 109A and 109B can be formed by any suitable processes. In FIG. 7A, for example, bottom electrode layer 109A is deposited (act 321, FIG. 5) to fill hole (FIG. 6, 128) and is then chemically mechanically polished down to etch stop layer 107, whereby bottom electrode layer 109A just fills hole 128. Main bottom electrode layer 109B is then deposited (act 323) to form a structure as shown in FIG. 7A. In FIG. 7B, CMP is not performed on the deposited diffusion barrier layer 109A (or CMP is performed, but for less time than in FIG. 7A), such that some remaining amount of diffusion barrier layer 109A is allowed to cover the surface of etch stop layer 107. In FIG. 7C, the layers of bottom electrode 109 conform to the surface over which they are deposited. In this later situation, the shapes of all layers in RRAM/MIM stack 130 are affected by the shape of hole 128 over which the RRAM/MIM stack 130 is formed. Any of the structures as shown in FIGS. 7A-7C can be used in conjunction with embodiments exemplified by device 100 of FIGS. 1 and 2 or device 200 of FIGS. 3 and 4.

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FIGS. 8-11 illustrate intermediate stages of device 200 as one or more acts 330 that create separation between peripheral top electrode region 115 and peripheral bottom electrode region 109. These can include either or both of act 331, patterning to remove bottom electrode 109 from peripheral region 122, and act 333, forming additional dielectric layer 111 and patterning to remove a portion of additional dielectric layer 111 lying within central region 124. Act 331 results in devices such as device 200 illustrated by FIGS. 3-4. FIGS. 8-11 illustrate intermediate stages of device 200 as it undergoes manufacture by the process 300 when act 331 is employed. FIG. 8 (act 331, FIG. 5, patterning to remove bottom electrode 109 from peripheral region 122 and outer region 142), generally includes photolithography to form a mask (not shown) that covers central bottom electrode 124 while exposing peripheral bottom electrode region 122 and outer bottom electrode region 142. With this mask in place, an etch is performed to remove the exposed peripheral and outer bottom electrode regions 122, 142. The mask is then stripped to form a structure as shown in FIG. 8, in which only the central bottom electrode region 124 remains in place. In most embodiments, the etch can include dry and/or wet etching for which etch stop layer 107 provides an etch stop. The dry etch can be, for example, a plasma etch using a fluorine-based gas or Ar. The wet etch can be, for example, a wet etch using HF or a similar acid.

In FIG. 9 an RRAM dielectric layer 113 is formed (act 335, FIG. 5), and a top electrode 115 is formed thereover (acts 340, FIG. 5). The dielectric layer 113, which can be referred to in some embodiments as a first dielectric layer, includes a central dielectric region 902 that is in direct contact with at least an upper surface of the bottom electrode layer 109B. The dielectric layer 113 also includes an outer dielectric region 904 spaced apart from the bottom electrode layers 109, and a peripheral dielectric region 906 connecting the central and outer dielectric regions. The peripheral dielectric region 906 is spaced apart from the bottom electrode layers 109.

In RRAM device embodiments, dielectric 113 can be any material suitable for the data storage layer of an RRAM cell. A material suitable for the data storage layer of an RRAM cell is one that can be induced to undergo a reversible phase change between a high resistance state and a low resistance state. In some embodiments, the phase change is between an amorphous state and a metallic state. The phase change can be accompanied by or associated with a change in chemical composition. For example, an amorphous metal oxide may lose oxygen as it undergoes a phase change to a metallic state. The oxygen may be stored in a portion of dielectric 113 that remains in the amorphous state or in an adjacent layer, especially capping layer 115A. Although described as a dielectric, only the low resistance state need be a dielectric. In most RRAM embodiments, dielectric 113 is a high-k dielectric while in the low resistance state. In some RRAM embodiments, dielectric 113 is a transitional metal oxide. Examples of high-k dielectric materials that can be suitable for dielectric 113 in RRAM devices include, without limitation, NiO_x , Ta_yO_x , TiO_x , HfO_x , Ta_yO_x , WO_x , ZrO_x , Al_yO_x , SrTiO_x and combinations thereof. In most RRAM embodiments, the thickness of dielectric 113 is in the range from 20 Å to 100 Å. In some RRAM embodiments, the thickness of dielectric 113 is in the range from 30 Å to 70 Å, for example, 50 Å.

In MIM capacitor embodiments, dielectric 113 can be any material suitable for the insulating layer of an MIM capacitor. In some MIM capacitor embodiments, dielectric layer 113 is silicon oxynitride or silicon nitride. In most MIM

capacitor embodiments, dielectric layer **113** is a high-k dielectric. In some MIM capacitor embodiments, dielectric layer **113** is a hafnium compound. Examples of hafnium compounds include hafnium oxide (HfO₂), hafnium silicon oxide (HfSiO), hafnium silicon oxynitride, (HfSiON), hafnium tantalum oxide (HfTaO), hafnium titanium oxide (HfTiO), hafnium Zirconium oxide (HfZrO), and combinations thereof. Dielectric layer **113** can include multiple layers of various dielectrics. In most MIM capacitor embodiments, the thickness of dielectric **113** is in the range from 50 Å to 300 Å. In some MIM capacitor embodiments, especially those in which dielectric **113** is a high-k dielectric, the thickness of dielectric **113** is in the range from 50 Å to 100 Å.

When dielectric layer **113** is formed over a bottom electrode **109** shaped as illustrated for the device **100C** shown in FIG. **7C**, it is possible that a deposition process will result in dielectric layer **113** being slightly thicker in peripheral region **222** as compared to a minimum thickness of dielectric layer **113** occurring in central region **224**. A slightly greater separation between bottom electrode **109** and top electrode **115** in peripheral region **222** resulting solely from that thickness variation would not be considered substantial as that term is used in the present disclosure. By contrast, the difference in separation resulting from either act **331** or act **333** would be considered substantial.

As shown in FIG. **9**, top electrode **115** when initially formed includes a central top electrode region **908**, a peripheral top electrode region **910**, and an outer top electrode region **912**. Top electrode **115** can include one or more layers. Top electrode **115** includes a main top electrode layer **115B** of conductive material. In some embodiments, especially the RRAM embodiments, top electrode **115** also includes capping layer **115A**. For RRAM embodiments, capping layer **115A** can provide an oxygen storage function that facilitates the setting and resetting of the RRAM cell formed by metal-insulator-metal structure **110**.

Capping layer **115A** can have any suitable composition. In some RRAM embodiments, capping layer **115A** is a metal or a metal oxide that is relatively low in oxygen concentration. Examples of metals that can be suitable for capping layer **115A** in RRAM embodiments include Ti, Hf, Pt, Al or a combination thereof. Examples of metal oxides that can be suitable for capping layer **115A** include TiO_x, HfO_x, ZrO_x, GeO_x, CeO_x, or a combination thereof. Capping layer **115A** can have any suitable thickness. In most RRAM embodiments, the thickness of capping layer **115A** is in the range from 20 Å to 100 Å. In some RRAM embodiments, the thickness of capping layer **115A** is in the range from 30 Å to 70 Å, for example, 50 Å.

Main top electrode layer **115B** can have any of the compositions identified as suitable for main bottom electrode layer **109B**. Top electrode layer **115B** can have any suitable thickness. In most embodiments, the thickness of top electrode layer **115B** is in the range from 100 Å to 400 Å. In some embodiments, the thickness of top electrode layer **115B** is in the range from 150 Å to 300 Å, for example 250 Å.

In FIG. **10**, the RRAM/MIM stack is patterned to form metal-insulator-metal structure **110A** (act **351**, FIG. **5**). To form the structure of FIG. **10**, photolithography is typically used to form a mask (not shown) over the top electrode layer **115B**. This mask exposes outer top electrode regions **912**, while covering the central and peripheral top electrode regions **908**, **910**. With the mask in place, an etch process (Act **351**, FIG. **5**) etches through at least top electrode layers **115** and dielectric layer **113** and removes the outer top

electrode regions **912** and outer dielectric regions **904**, while leaving the central and peripheral top electrode and dielectric regions (**902**, **906**, **908**, **910**) in place. In most embodiments, the etch is a plasma etch for which etch stop layer **107** provides an etch stop. The etch can be carried out in one or more stages to etch through the various layer of RRAM/MIM stack **130**. The individual stages can be, for example, plasma etches based on one or more of Cl₂, BCl₂, Ar, and F. In most embodiments, act **351** uses a single mask.

As shown in FIG. **10**, for example, act **351** forms edge **116** of top electrode **115** and edge **114** of dielectric layer **113**. In most embodiments, act **351** leaves edge **116** and edge **114** flush as shown in FIGS. **2** and **4**. Edges **114** and **116** are at the periphery of metal-insulator-metal structure **110**, abut peripheral region **122**, and are distal to central region **124**. Capping layer **115A** may be damaged or contaminated near edge **116**. Dielectric layer **113** may be damaged or contaminated near edge **114**. Any such damage or contamination does not affect the performance of metal-insulator-metal structure **110** provided by the present disclosure. In some embodiments, act **351** includes etching through bottom electrode **109** and leaves an edge **106** of bottom electrode **109** also flush with edge **114** of dielectric **113** as shown in FIG. **14**.

Process **300** continues with acts that encapsulate metal-insulator-metal structures **110** in dielectric **119** and form a top electrode via **125** for connecting metal-insulator-metal structures **110** to bit lines (not shown) or the like. Act **353** deposits dielectric **119**. Act **355** forms an opening **134** in dielectric **119** as shown in FIG. **11** for device **200** and FIG. **15** for device **100**. Act **357** fills opening **134** with conductive material to form via **125** resulting in a structure as shown in FIG. **1** for device **100** and FIG. **3** for device **200**. In most embodiments, dielectric **119** is a low-k dielectric. In some embodiments, dielectric **119** is an extremely low-k dielectric. Via **125** can be formed from any suitable conductor. In some embodiments, via **125** is copper.

FIGS. **12-15** illustrate an alternate manufacturing embodiment to form devices such as device **100** illustrated in FIGS. **1-2**. Many acts in manufacturing device **100** are the same as described above with regards to manufacturing device **200**, and are therefore not repeated for purposes of clarity and conciseness. Act **333** of FIG. **5** is present, however, and was not previously described in FIGS. **6-11**. FIGS. **12-15** illustrate intermediate stages of device **100** as it undergoes manufacture by the process **300** when act **333** is employed.

In FIG. **12** (Act **333**, forming additional dielectric layer **111**), generally includes photolithography to form a mask (not shown) that exposes a central region of additional dielectric layer **111**, while covering peripheral and outer regions of the additional dielectric layer **111**. An etch is carried out with the mask in place to remove the exposed central portion of additional dielectric layer **111**, and the mask is then stripped to form a structure as shown in FIG. **12**. As shown in FIG. **12**, act **333** leaves peripheral dielectric region **122** and outer dielectric region **142**. Additional dielectric layer **111** can have any suitable composition and can be formed by any suitable process. Examples of suitable compositions for additional dielectric layer **111** include, without limitation, SiO₂, SiN, and SiON.

Additional dielectric layer **111** can have any suitable thickness. Additional dielectric layer **111** is sufficiently thick to perform its function but is generally not so thick as to excessively increase the height of RRAM/MIM stack **130A**. In most embodiments, the thickness of additional dielectric layer **111** is in the range from 10 Å to 200 Å. In some embodiments, the thickness of additional dielectric layer **111**

is in the range from 20 Å to 100 Å, for example, 50 Å. As shown in FIGS. 13-14, a MIM/RRAM dielectric 113 and top electrode layers 115 are then conformally formed over the dielectric layer. Etching is then performed to remove outer regions of the layers while leaving peripheral and central regions in place, as shown in FIG. 14.

The present disclosure provides an integrated circuit device that includes a metal-insulator-metal structure. The structure can form a resistive random access memory (RRAM) cell or an MIM capacitor. The metal-insulator-metal structure includes a dielectric layer between a top conductive layer and a bottom conductive layer. The dielectric layer includes a peripheral region adjacent an edge of the dielectric layer where the dielectric layer has been cut off by etching and a central region surrounded by the peripheral region. The top conductive layer abuts and is above dielectric layer. The bottom conductive layer abuts and is below the dielectric layer in the central region. The bottom conductive layer does not abut the dielectric layer in the peripheral region of the dielectric layer.

This structure causes pathways between the top conductive layer and the bottom conductive layer to be substantially greater along pathways passing through the peripheral region of the dielectric layer in comparison to pathways passing through the central region. This inhibits formation of conductive bridges or leakage currents through areas of the dielectric layer that may have been damaged or contaminated by etching near the edge of the dielectric layer. In a first group of embodiments, the bottom conductive layer is prevented from abutting the dielectric in the peripheral region by an extra layer of dielectric in the peripheral region. In a second group of embodiments, the bottom conductive layer is prevented from abutting the dielectric in the peripheral region by cutting off the bottom conductive layer short of the peripheral region.

The present disclosure also provides an integrated circuit device that includes a metal-insulator-metal structure formed over the substrate. The metal-insulator-metal structure is either a resistive random access memory (RRAM) cell or an MIM capacitor. The metal-insulator-metal structure includes a bottom electrode, a first dielectric layer, and a top electrode. There is a minimum distance between the bottom electrode and the top electrode. The first dielectric layer is positioned between the bottom electrode and the top electrode where they are separated by the minimum distance. The bottom electrode and the top electrode are configured whereby the shortest path starting from a point on the perimeter of the top electrode and continuing to the bottom electrode is greater than the minimum distance. In a first group of embodiments, the distance between the electrodes is increased in the peripheral region by an extra layer of dielectric in the peripheral region. In a second group of embodiments, the distance between the electrodes is made greater in the peripheral region by the bottom electrode being cut off short of the peripheral region.

The present disclosure provides a method of manufacturing an integrated circuit device that includes forming a contact on a substrate and forming one or more bottom electrode layers directly over the contact. A first dielectric layer is formed over the one or more bottom electrode layers. The first dielectric layer includes a central dielectric region in direct contact with the bottom electrode layers, an outer dielectric region spaced apart from the bottom electrode layers, and a peripheral dielectric region that is also spaced apart from the bottom electrode layers. The peripheral dielectric region connects the central and outer dielectric regions. One or more top electrode layers is then

conformally formed over the first dielectric layer. The one or more top electrode layers include a central top electrode region, an outer top electrode region, and a peripheral top electrode region. These are formed over the central dielectric region, the outer dielectric region, and the peripheral dielectric region, respectively. The one or more top electrode layers and the first dielectric layer are then patterned to form a cell having a patterned top electrode and a patterned first dielectric. The patterning removes the outer top electrode region and the outer dielectric region while leaving the central and peripheral top electrode regions and the central and peripheral dielectric regions.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method of manufacturing an integrated circuit device, comprising:

forming a contact over a substrate;

forming one or more bottom electrode layers over the contact;

forming a first dielectric layer over the one or more bottom electrode layers;

patterning the first dielectric layer to form an opening in the first dielectric layer, wherein the opening is arranged over the contact;

forming an additional dielectric layer such that a first base region of the additional dielectric layer extends through the opening to contact the one or more bottom electrode layers and a second base region of the additional dielectric layer extends over the first dielectric layer to be spaced apart from the one or more bottom electrode layers;

forming one or more top electrode layers over the additional dielectric layer; and

patterning by etching through the one or more top electrode layers and by etching through the additional dielectric layer to form a metal-insulator-metal structure, wherein the patterning removes a portion of the second base region that directly overlies the one or more bottom electrode layers, but does not remove the first base region.

2. The method of claim 1, wherein the first dielectric layer comes between the second based region of the additional dielectric layer and the one or more bottom electrode layers.

3. The method of claim 1, wherein the patterning comprises:

forming a mask over the one or more top electrode layers;

etching through the one or more top electrode layers through openings in the mask; and

etching through the additional dielectric layer using the mask.

4. The method of claim 3, wherein the patterning further comprises etching through the one or more bottom electrode layers using the same mask used to etch through the one or more top electrode layers and the additional dielectric layer.

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5. The method of claim 1, wherein the additional dielectric layer is a high-k dielectric layer and the metal-insulator-metal structure is a resistive random access memory (RRAM) cell.

6. The method of claim 1, further comprising:
prior to forming the one or more bottom electrode layers, forming an etch stop layer, wherein the one or more bottom electrode layers are formed to overhang and contact a top surface of the etch stop layer.

7. The method of claim 6, wherein the patterning of the one or more top electrode layers and the additional dielectric layer also removes a portion of the etch stop layer, such that a bottom surface of the one or more bottom electrode layers is even with the top surface of the etch stop layer.

8. A method of manufacturing an integrated circuit device, comprising:

forming a contact over a substrate;

forming one or more bottom electrode layers over the contact;

forming a first dielectric layer that covers a peripheral portion of the one or more bottom electrode layers and does not cover a central portion of the one or more bottom electrode layers, wherein an outermost sidewall of the first dielectric layer is aligned with an outermost sidewall of the one or more bottom electrode layers; and

forming a second dielectric layer over the first dielectric layer, wherein the second dielectric layer comprises: a central dielectric region extending through the first dielectric layer to contact the central portion of the one or more bottom electrode layers, a peripheral dielectric region spaced apart from the peripheral portion of the one or more bottom electrode layers by the first dielectric layer; and a step dielectric region connecting the central dielectric region and the peripheral dielectric region; and

conformally forming one or more top electrode layers over the second dielectric layer, wherein the one or more top electrode layers include a central top electrode region, a peripheral top electrode region, and a step top electrode region directly above the central dielectric region, the peripheral dielectric region, and the step dielectric region, respectively.

9. The method of claim 8, further comprising:

patterning the one or more top electrode layers and the second dielectric layer to form a cell having a patterned top electrode and a patterned second dielectric, wherein the patterning removes the peripheral top electrode region and the peripheral dielectric region while leaving the central top electrode region, the step top electrode region, the central dielectric region, and the step dielectric region in place.

10. The method of claim 9, wherein the patterning comprises:

forming a mask over the one or more top electrode layers; etching through the one or more top electrode layers through openings in the mask; and

etching through the first dielectric layer using the same mask.

11. The method of claim 10, wherein the patterning further comprises etching through the one or more bottom electrode layers using the same mask used to etch through the one or more top electrode layers and the second dielectric layer.

12. The method of claim 8, wherein the first dielectric layer has a uniform thickness from an inner edge of the first dielectric layer to an outer edge of the first dielectric layer,

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the uniform thickness being measured perpendicular to a top surface of the one or more bottom electrode layers.

13. The method of claim 8, wherein the first dielectric layer and the second dielectric layer have different compositions from one another.

14. The method of claim 8, wherein the peripheral top electrode region extends to a first height as measured perpendicularly from a top surface of the one or more bottom electrode layers, and the central top electrode region extends to a second height as measured perpendicularly from the top surface of the one or more bottom electrode layers, the first height being greater than the second height.

15. A method of manufacturing an integrated circuit device, comprising:

forming a contact over a substrate;

forming an etch stop layer over the contact, wherein the etch stop layer comprises inner sidewalls disposed directly above the contact;

forming one or more bottom electrode layers over the contact and between the inner sidewalls of the etch stop layer;

forming a first dielectric layer that covers a peripheral portion of the one or more bottom electrode layers and does not cover a central portion of the one or more bottom electrode layers; and

forming a second dielectric layer over the first dielectric layer, wherein the second dielectric layer comprises: a central dielectric region extending through the first dielectric layer to contact the central portion of the one or more bottom electrode layers, a peripheral dielectric region spaced apart from the peripheral portion of the one or more bottom electrode layers by the first dielectric layer; and a step dielectric region connecting the central dielectric region and the peripheral dielectric region;

conformally forming a conductive capping layer over the second dielectric layer and conformally forming a conductive main electrode layer over the conductive capping layer, wherein the conductive capping layer and the conductive main electrode layer each include a central top electrode region, a peripheral top electrode region, and a step top electrode region directly above the central dielectric region, the peripheral dielectric region, and the step dielectric region, respectively; and

patterning the conductive capping layer, the conductive main electrode layer, and the second dielectric layer to form a cell having a patterned top electrode and a patterned second dielectric, wherein the patterning removes the peripheral top electrode region and the peripheral dielectric region while leaving the central top electrode region, the step top electrode region, the central dielectric region, and the step dielectric region in place, such that outer sidewalls of the step top electrode region, outer sidewalls of the step dielectric region, outer sidewalls of the one or more bottom electrode layers, and outer sidewalls of the etch stop layer are aligned along a substantially vertical axis.

16. The method of claim 15, wherein the patterning comprises:

forming a mask over the conductive main electrode layer; etching through the conductive capping layer and the conductive main electrode layer through openings in the mask; and

etching through the first dielectric layer using the mask.

17. The method of claim 15, wherein the first dielectric layer has a uniform thickness from an inner edge of the first dielectric layer to an outer edge of the first dielectric layer,

the uniform thickness being measured perpendicular to a top surface of the one or more bottom electrode layers.

18. The method of claim **15**, wherein forming the one or more bottom electrode layers over the contact comprises:

forming a diffusion barrier layer over the contact; and 5

forming a bottom conductive layer over the diffusion barrier layer, wherein the diffusion barrier layer and the bottom conductive layer collectively have a T-shaped profile.

19. The method of claim **15**, wherein the conductive 10 capping layer comprises no more than one material.

20. The method of claim **15**, further comprising:

forming a dielectric structure over and surrounding the patterned top electrode such that a bottom surface of the dielectric structure contacts a top surface of the 15 patterned top electrode, and an inner sidewall of the dielectric structure contacts the outer sidewalls of the step top electrode region, the outer sidewalls of the step dielectric region, and the outer sidewalls of the etch stop layer. 20

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