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Lee

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(54) **CHALCOGENIDE MATERIAL AND ELECTRONIC DEVICE INCLUDING THE SAME**

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H01L 45/00 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 45/143*** (2013.01); ***C01G 28/002*** (2013.01); ***H01L 45/1253*** (2013.01); *C01P 2006/40* (2013.01)

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See application file for complete search history.

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Primary Examiner — Edward Chin

(57) **ABSTRACT**

A chalcogenide material and an electronic device are provided. The chalcogenide material may include 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium. The electronic device may include a switching element including a chalcogenide material, the chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium. The electronic device may further include a first electrode electrically coupled to the switching element and a second electrode electrically coupled to the switching element.

19 Claims, 10 Drawing Sheets

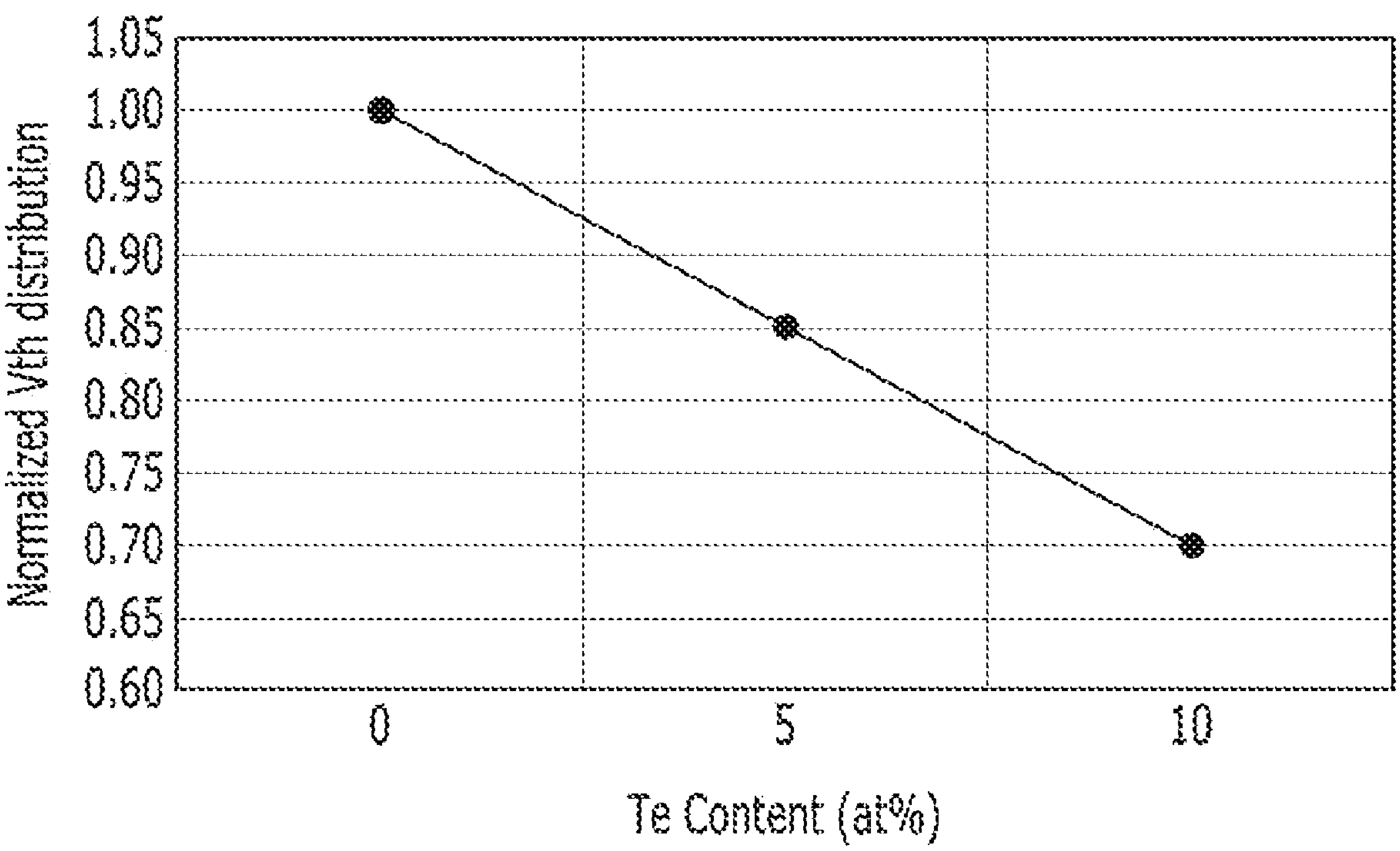


FIG. 1

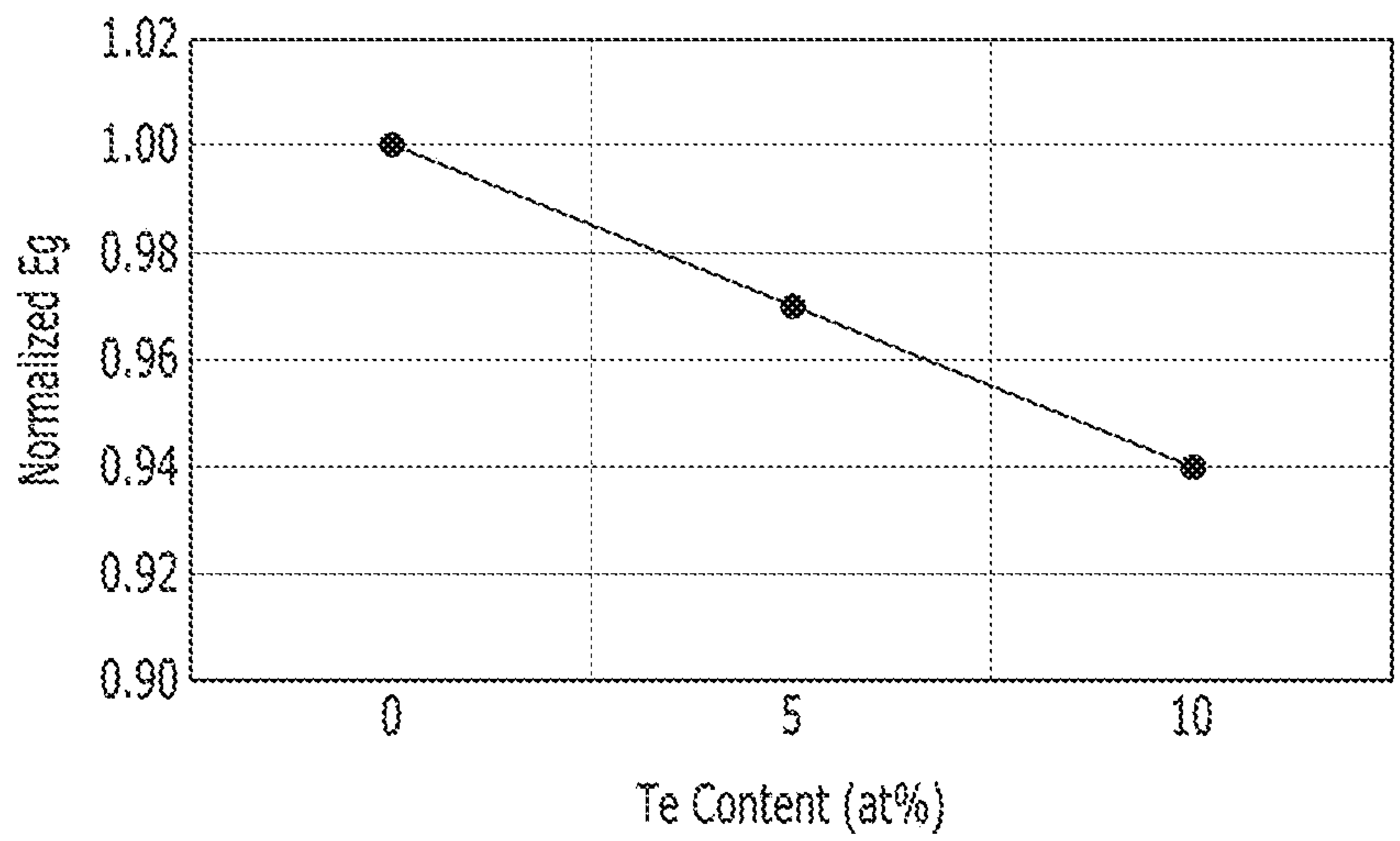

1.02
1.00
0.98
0.96
0.94
0.92
0.90
Normalized Eg
0
5
10
Te Content (at%)

FIG. 2

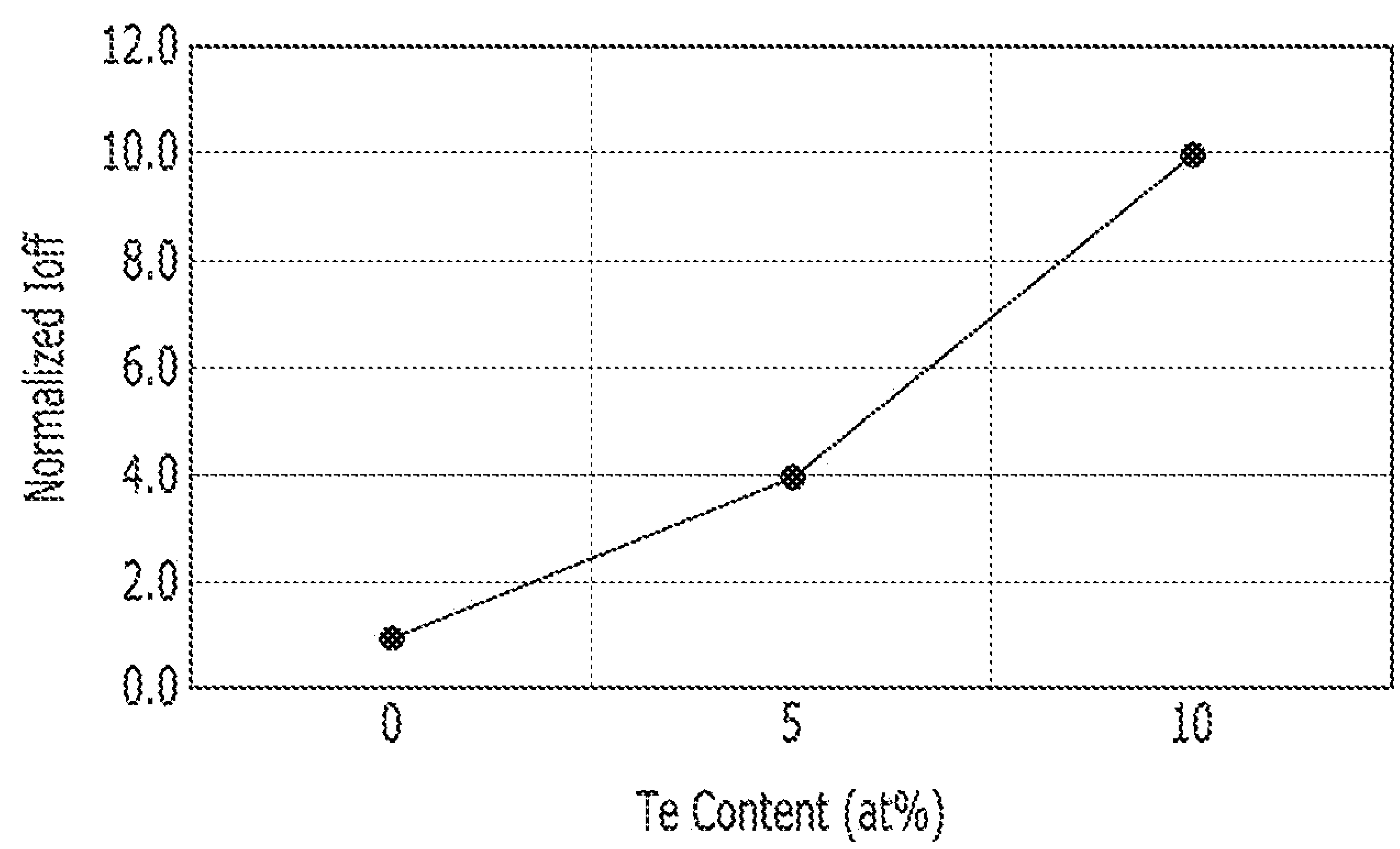

12.0
10.0
8.0
6.0
4.0
2.0
0.0
Normalized Ioff
0
5
10
Te Content (at%)

FIG. 3

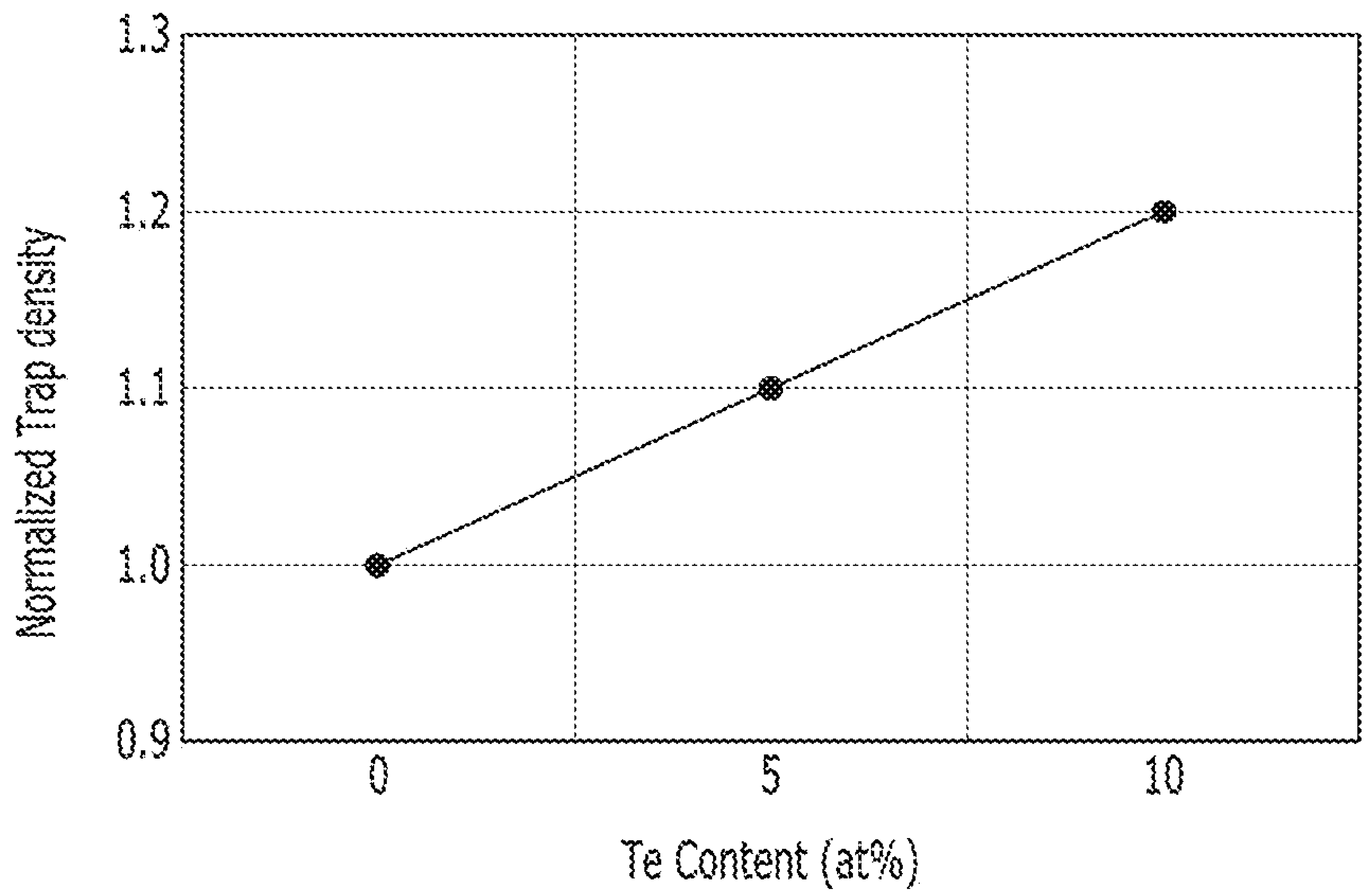

1.3
1.2
1.1
1.0
0.9
Normalized Trap density
0
5
10
Te Content (at%)

FIG. 4

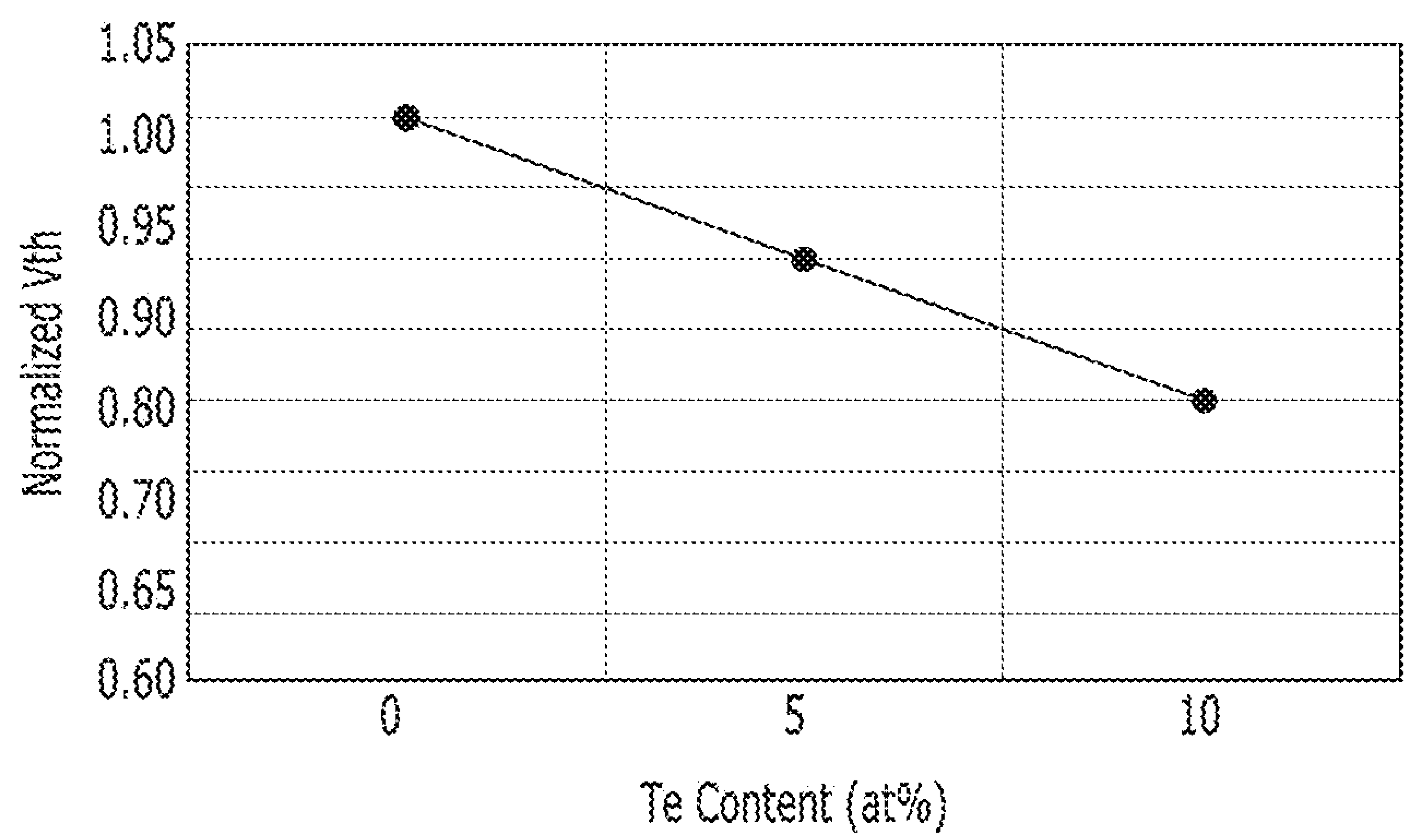
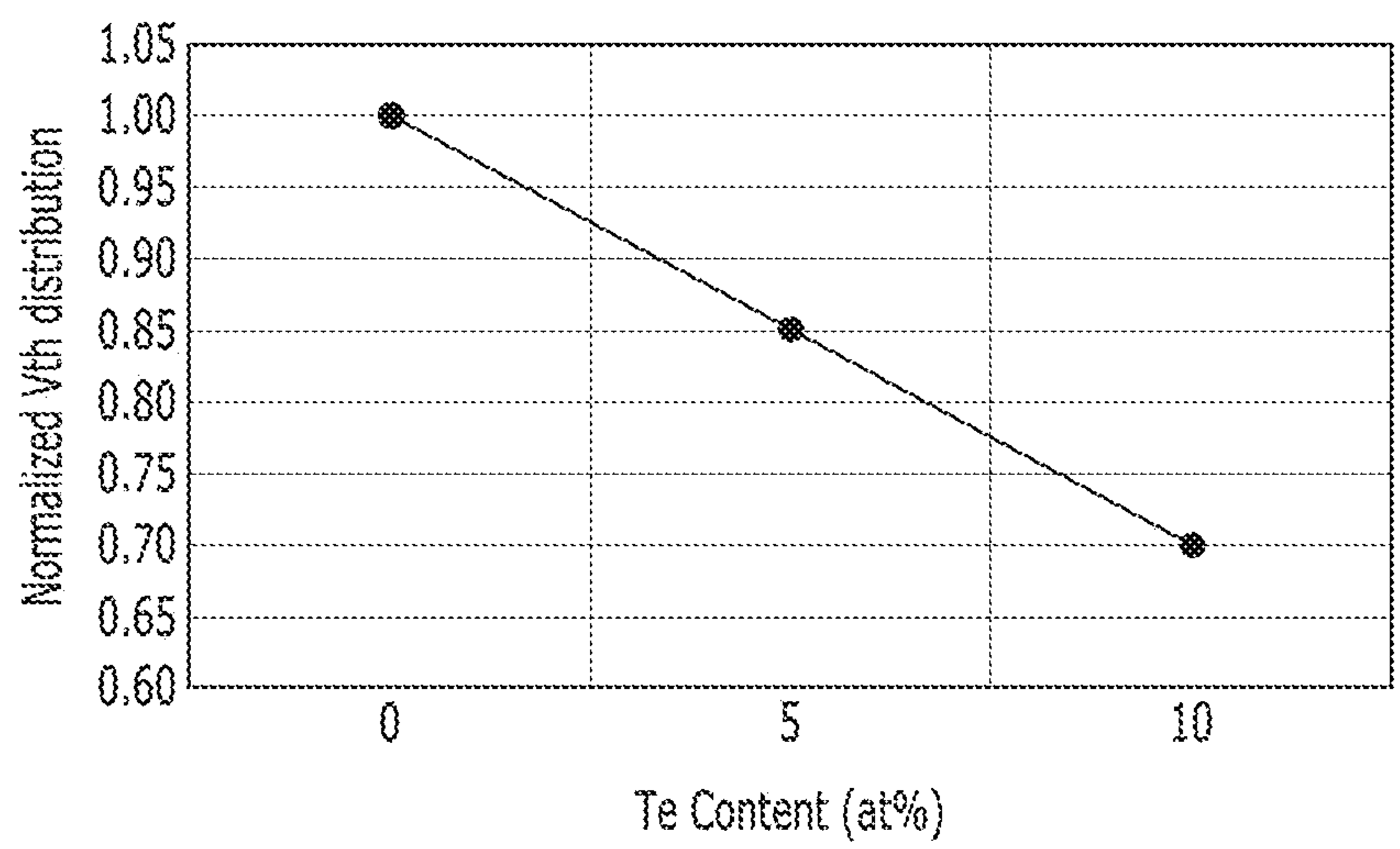

1.05
1.00
0.95
0.90
0.80
0.70
0.65
0.60
Normalized Vth
0
5
10
Te Content (at%)

FIG. 5



1.05
1.00
0.95
0.90
0.85
0.80
0.75
0.70
0.65
0.60
Normalized Vth distribution
0
5
10
Te Content (at%)

FIG. 6

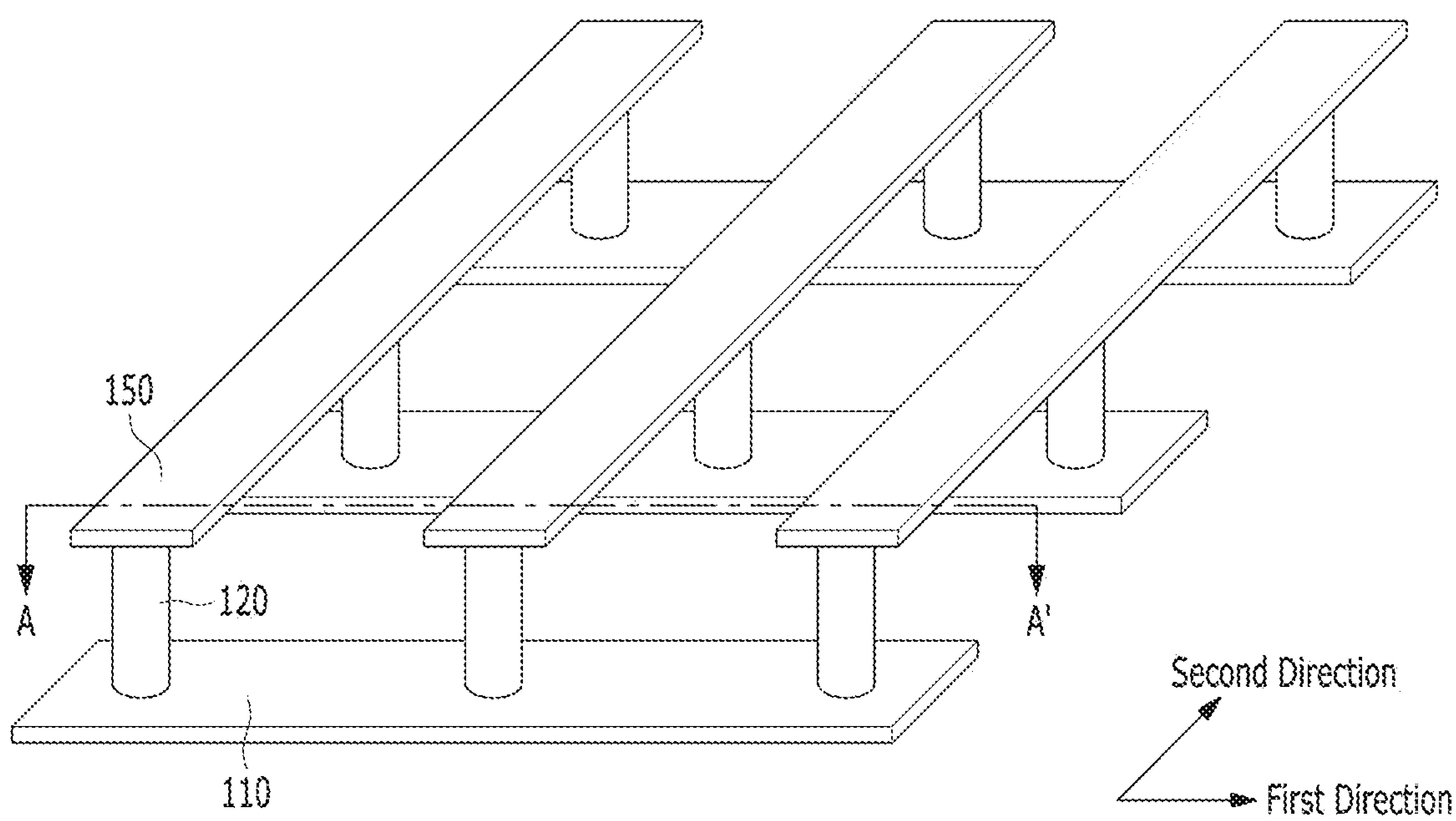


FIG. 7A

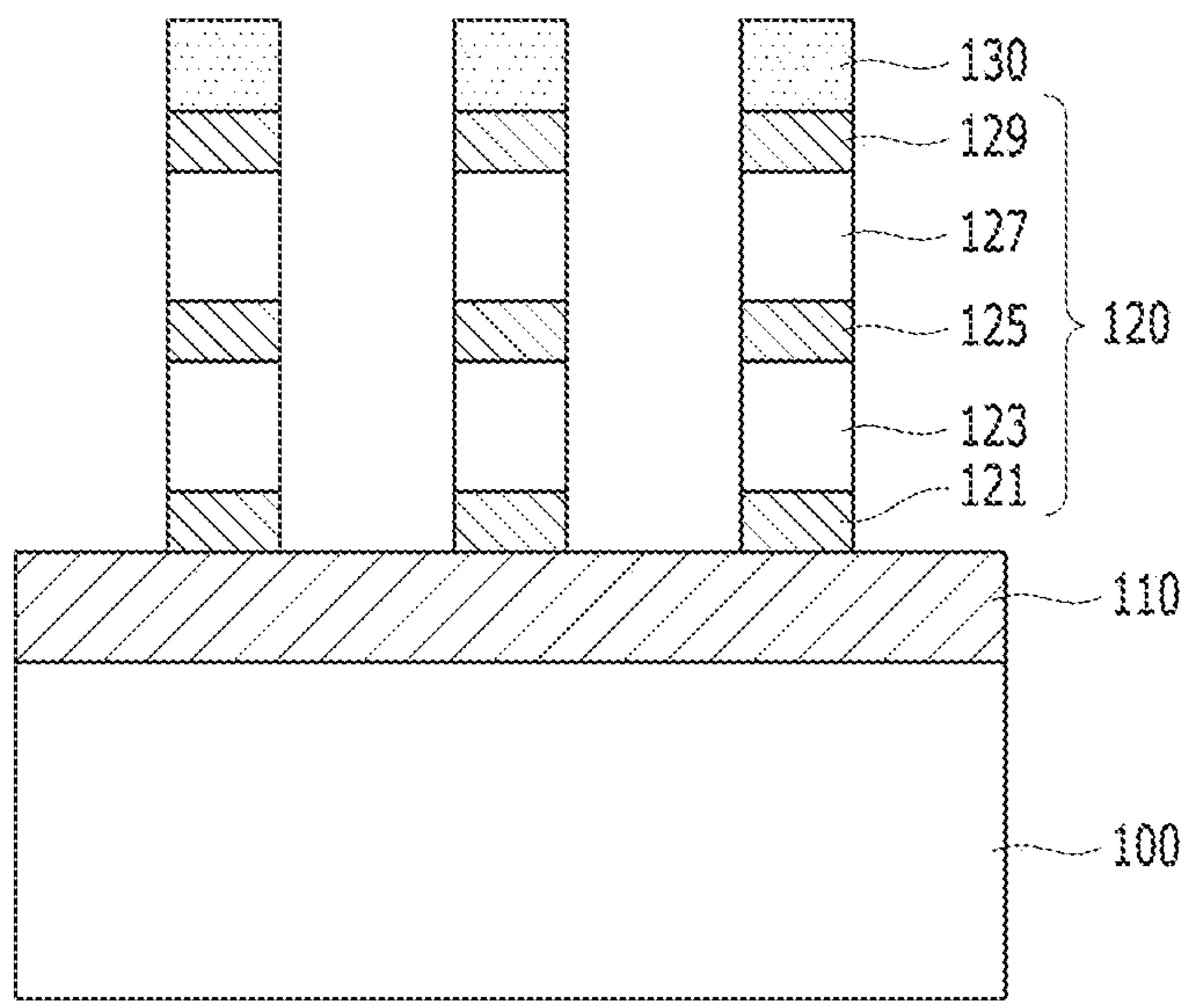

130
129
127
125
120
123
121
110
100

FIG. 7B

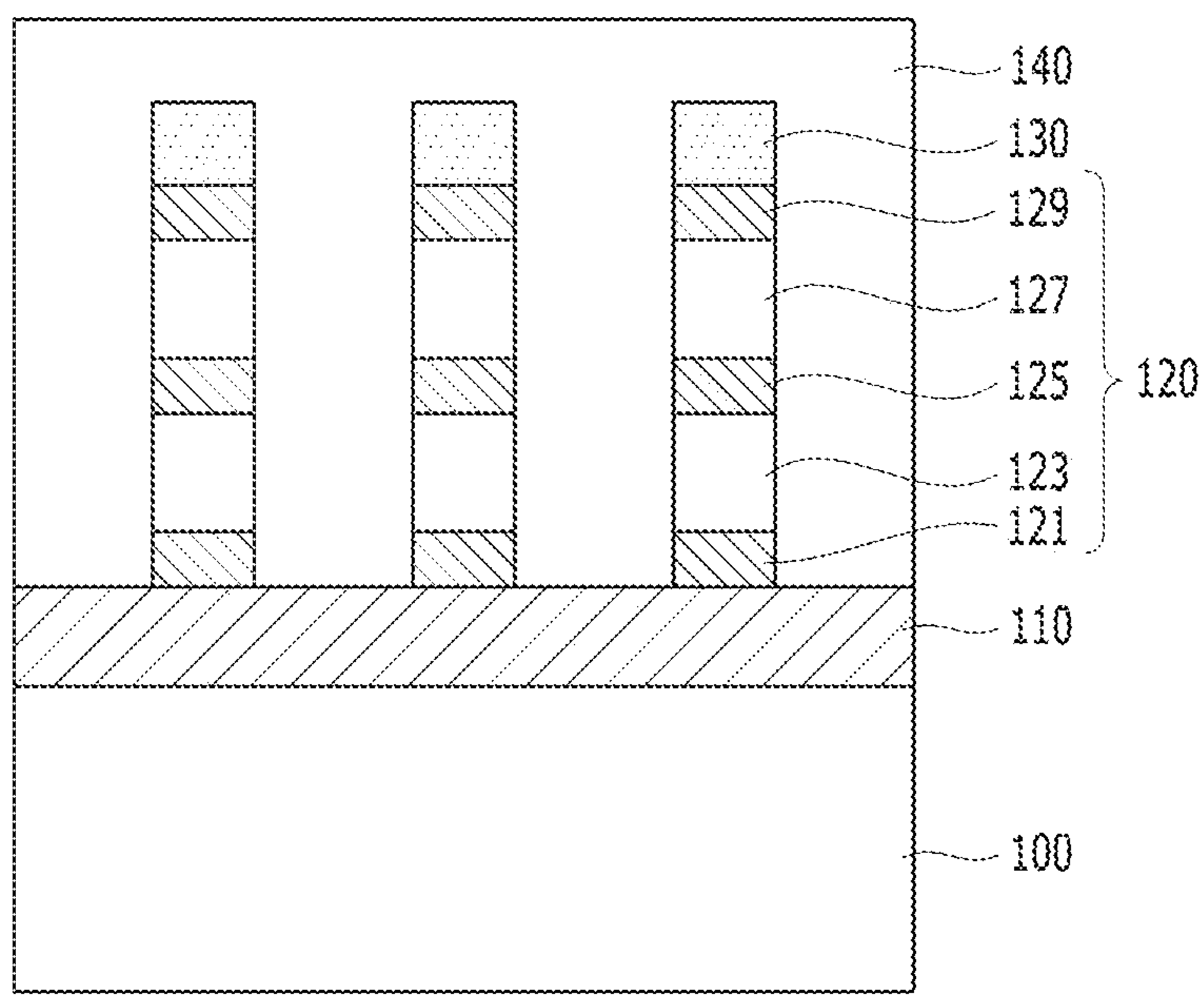

140
130
129
127
125
120
123
121
110
100

FIG. 7C

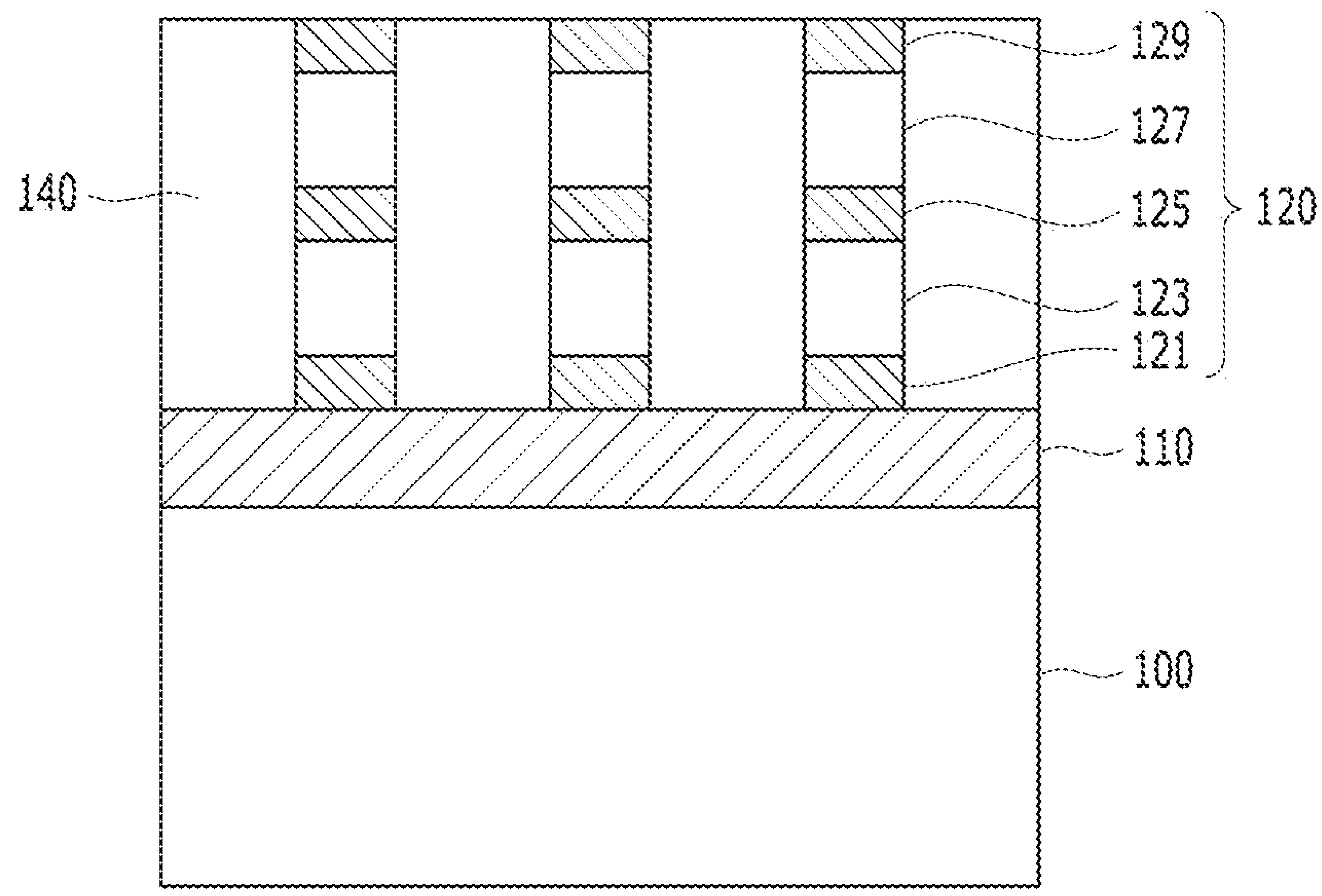

129
127
140
125
120
123
121
110
100

FIG. 7D

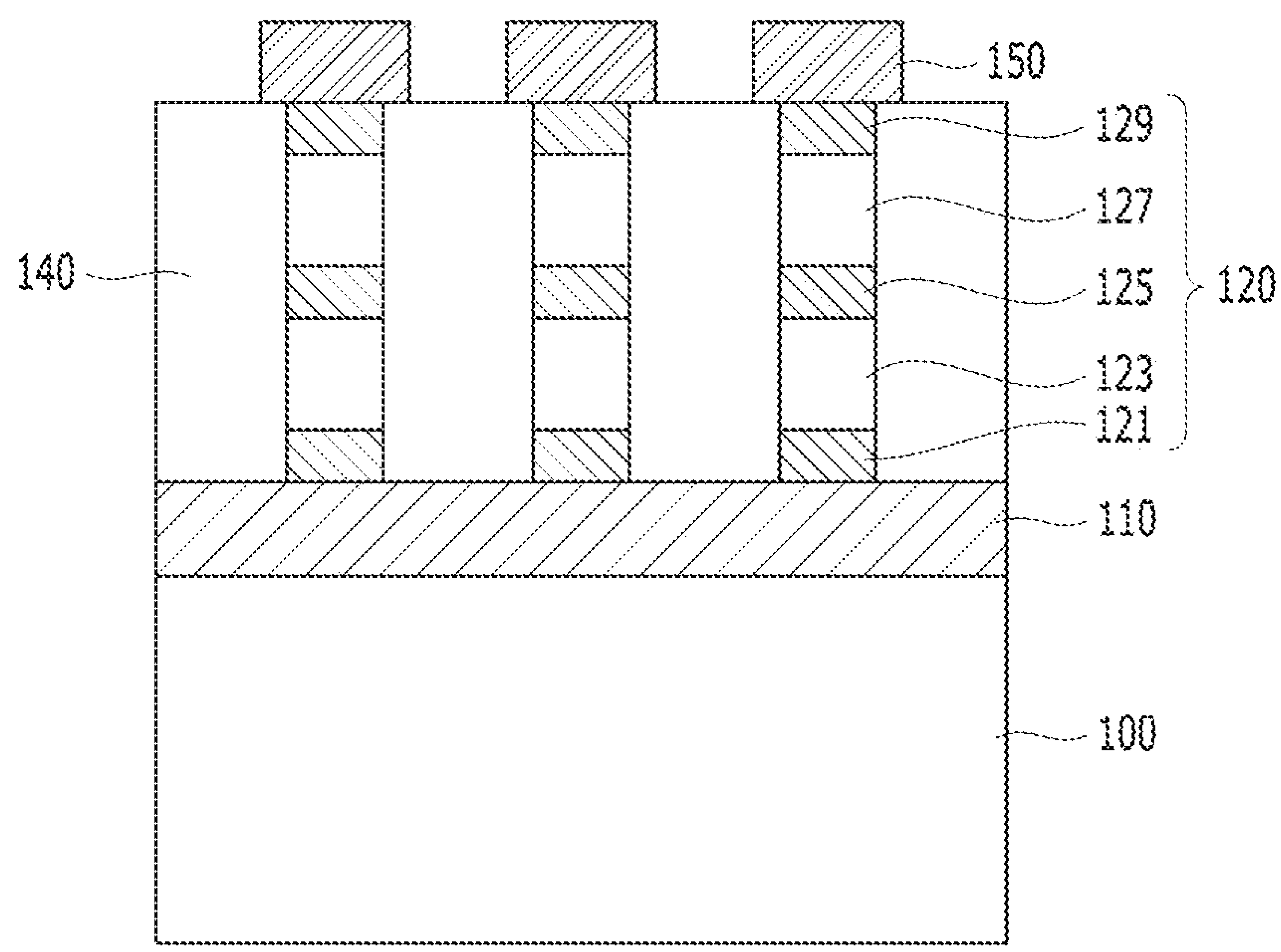

150
129
127
140
125
120
123
121
110
100

FIG. 8

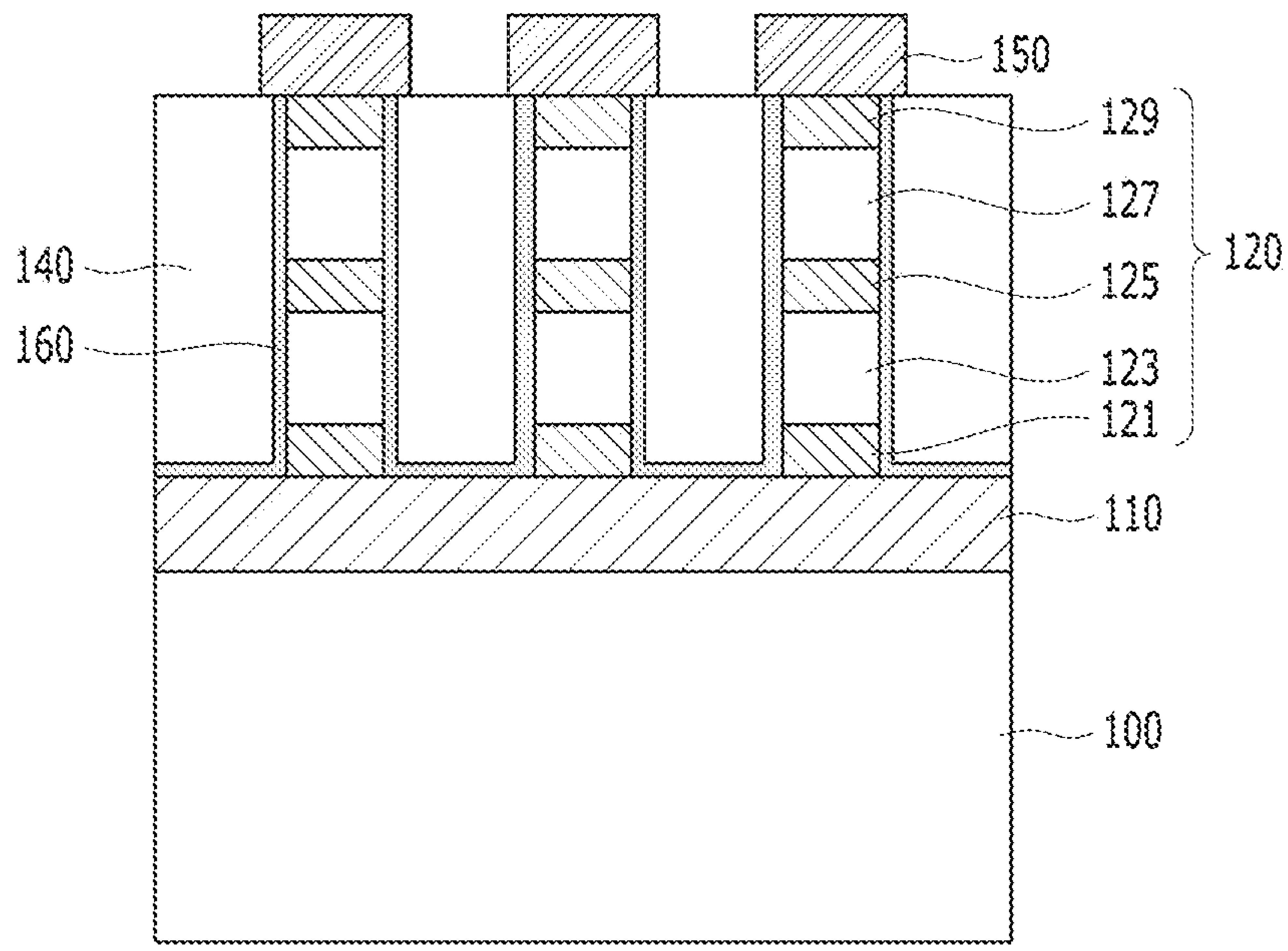

150
129
127
125
120
123
121
140
160
110
100

FIG. 9

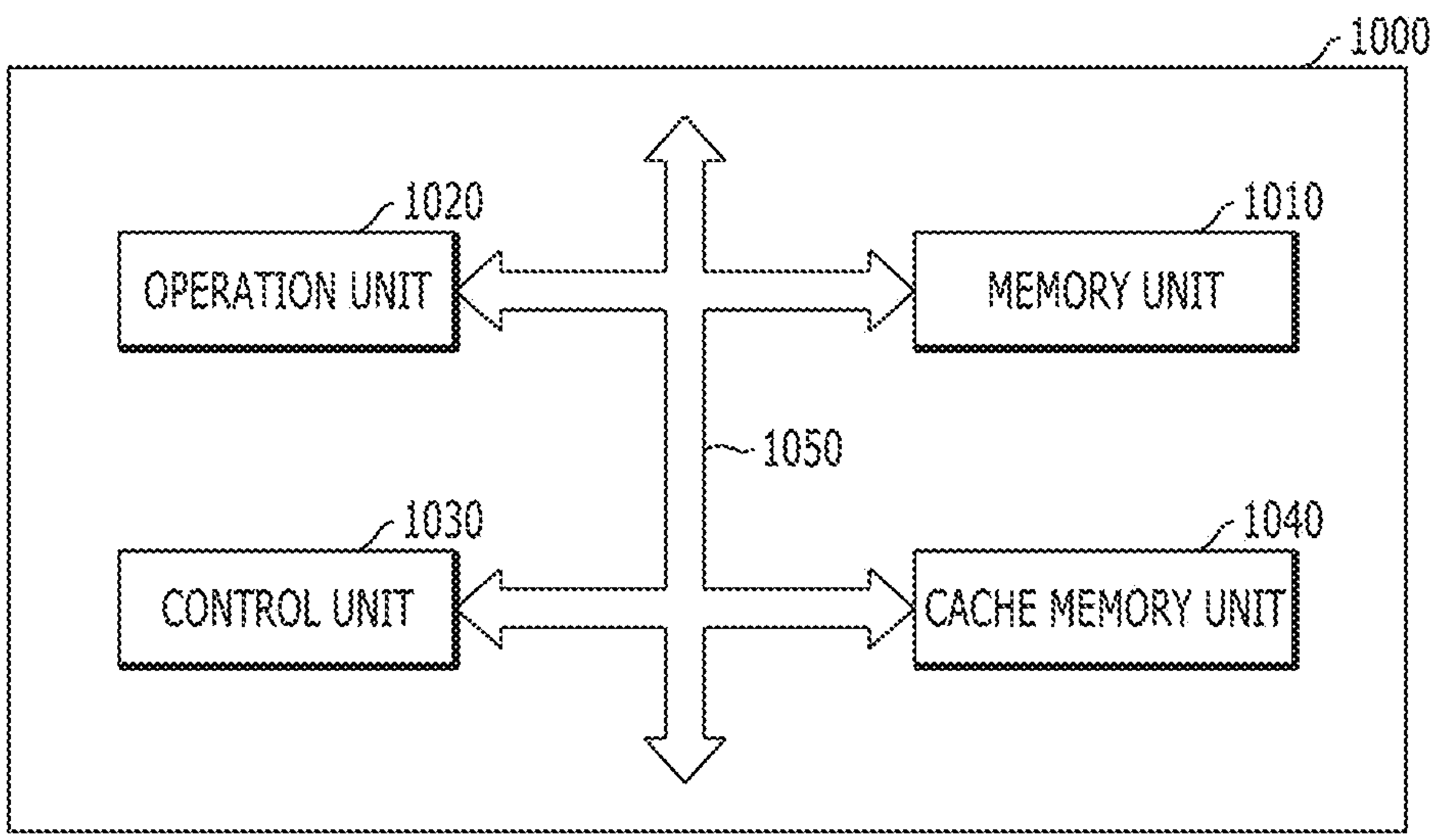

1000
1020
OPERATION UNIT
1010
MEMORY UNIT
1050
1030
CONTROL UNIT
1040
CACHE MEMORY UNIT

FIG. 10

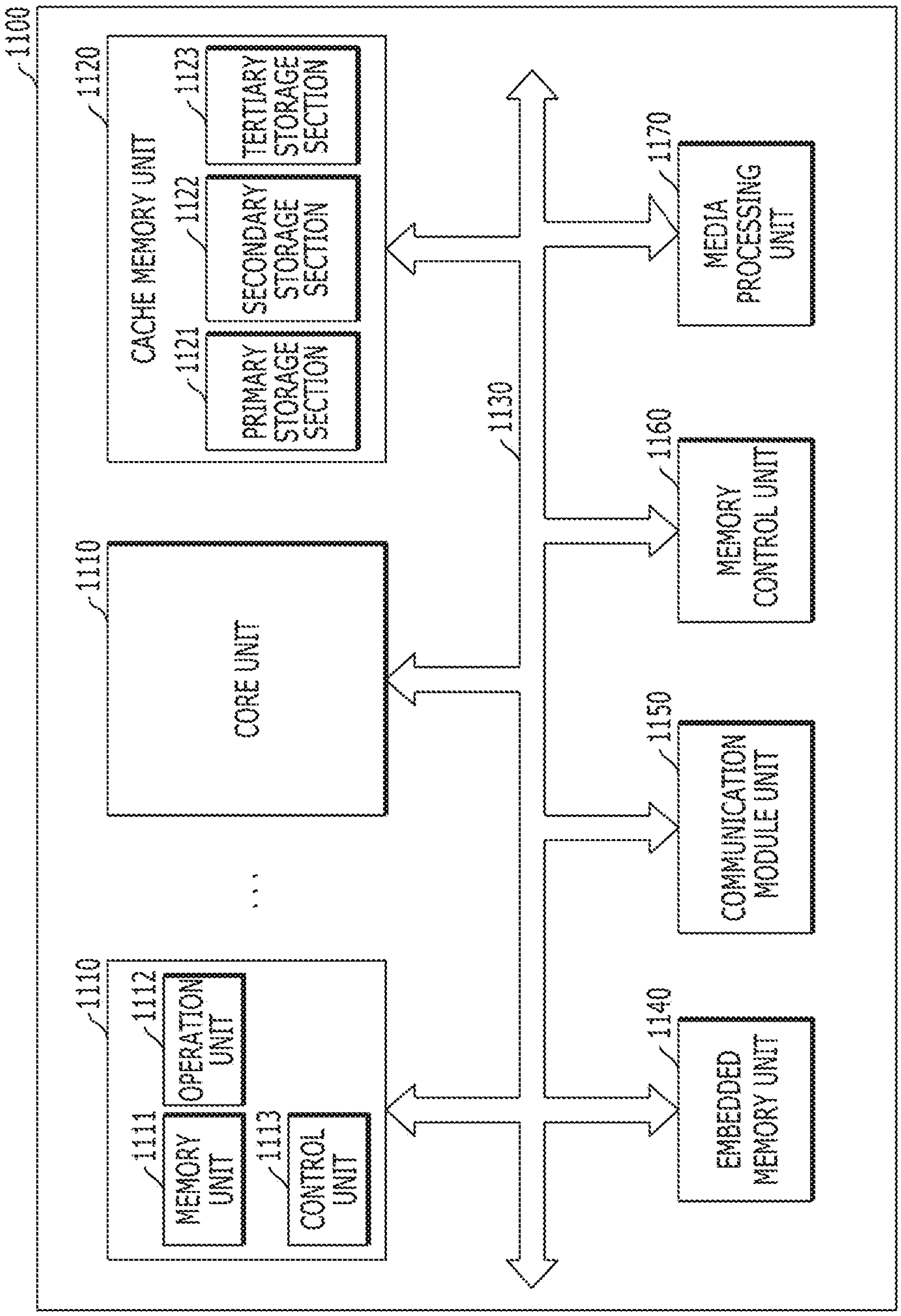

1100
1120
CACHE MEMORY UNIT
1121
PRIMARY STORAGE SECTION
1122
SECONDARY STORAGE SECTION
1123
TERTIARY STORAGE SECTION
1110
CORE UNIT
1130
1110
1111
MEMORY UNIT
1112
OPERATION UNIT
1113
CONTROL UNIT
1140
EMBEDDED MEMORY UNIT
1150
COMMUNICATON MODULE UNIT
1160
MEMORY CONTROL UNIT
1170
MEDIA PROCESSING UNIT

FIG. 11

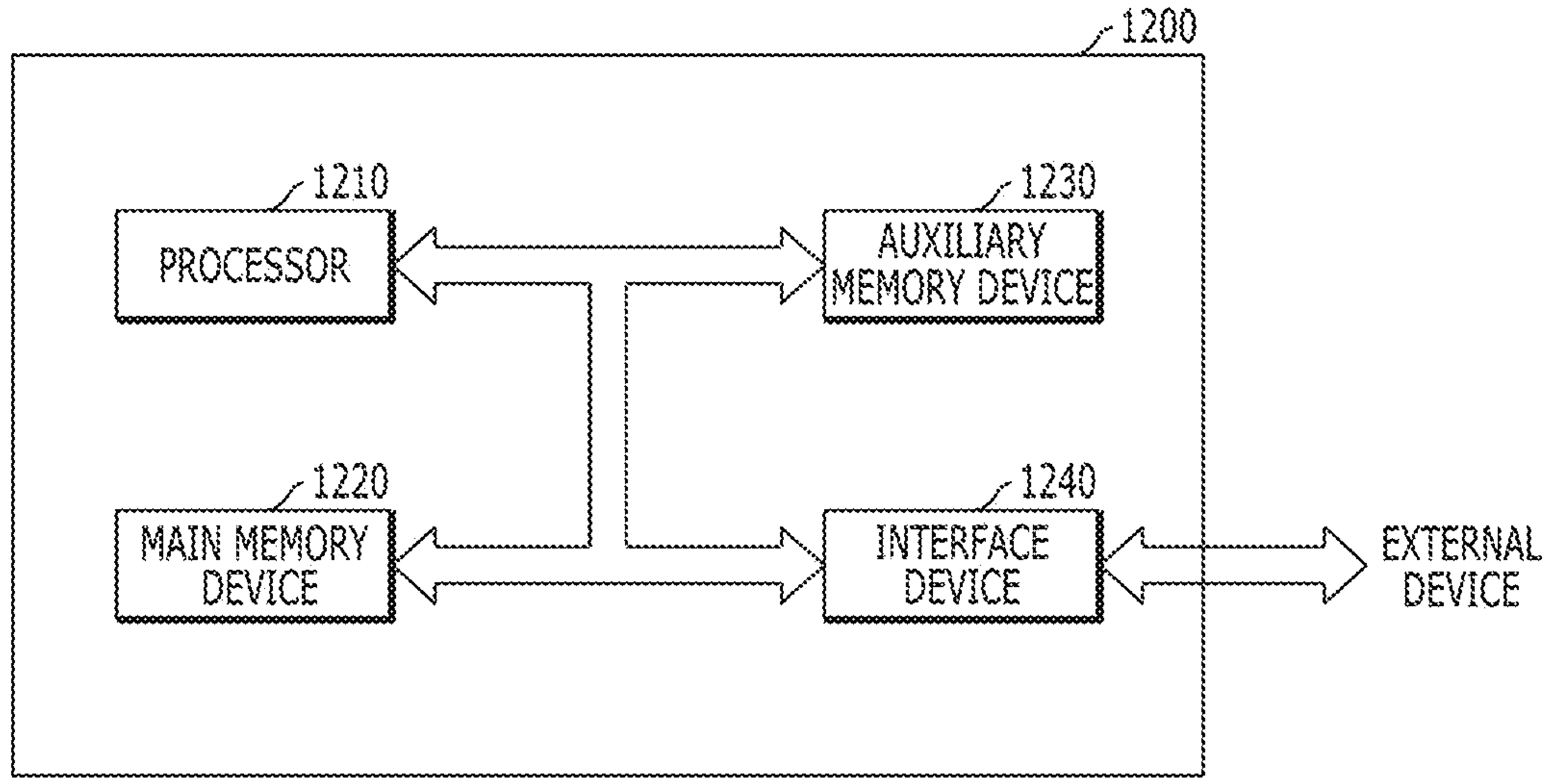

1200
1210
PROCESSOR
1230
AUXILIARY MEMORY DEVICE
1220
MAIN MEMORY DEVICE
1240
INTERFACE DEVICE
EXTERNAL DEVICE

FIG. 12

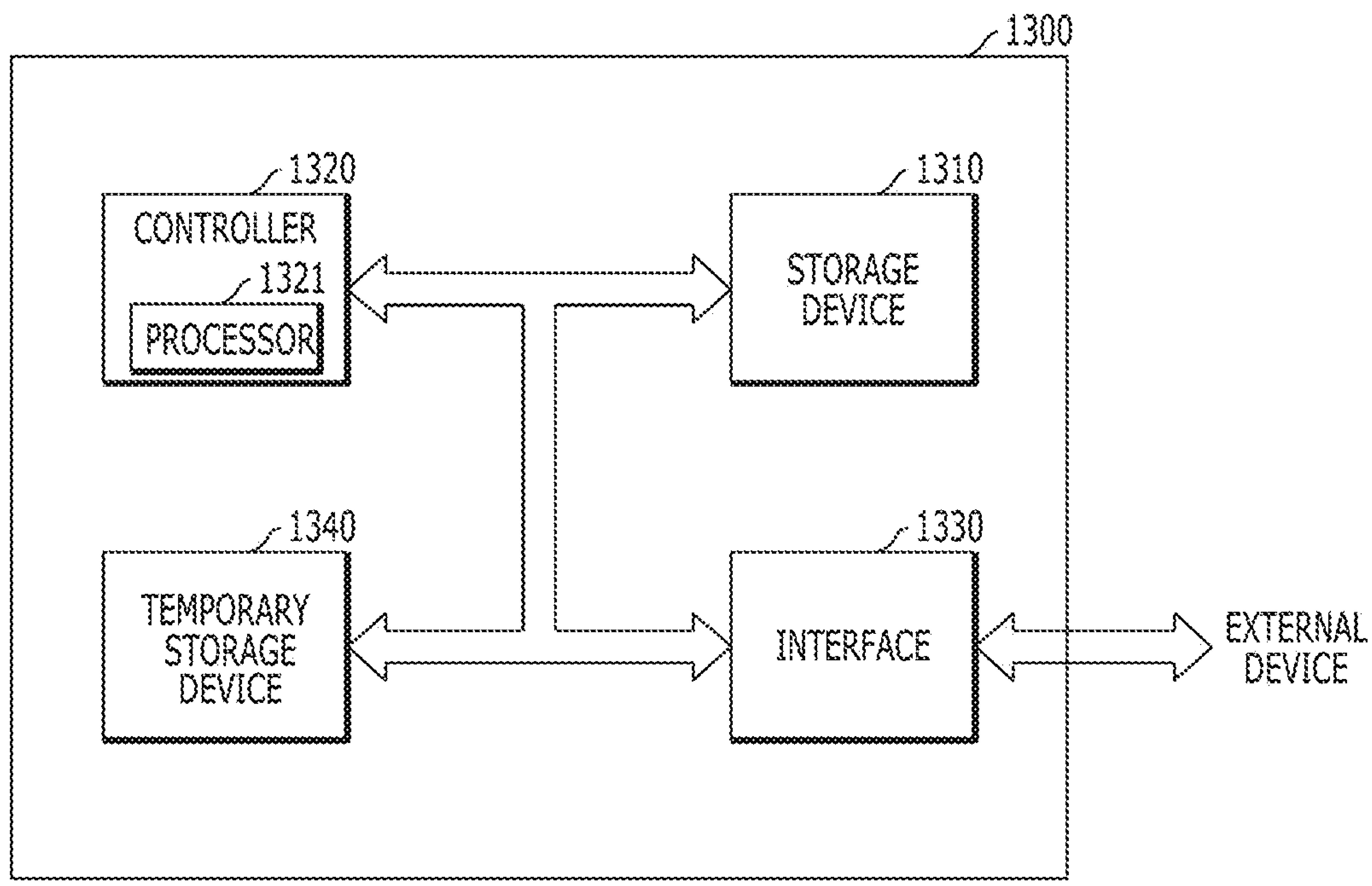
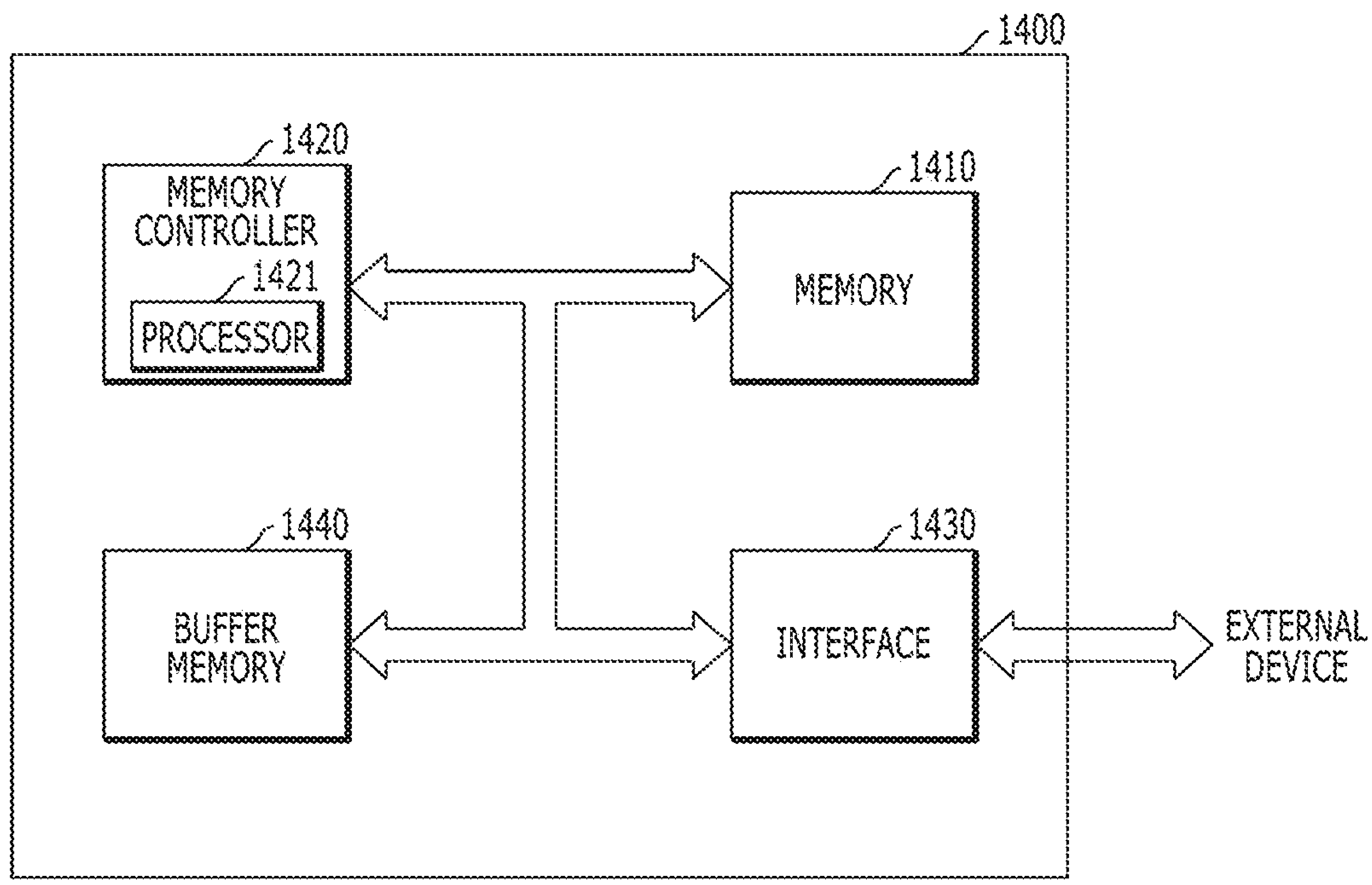

1300
1320
CONTROLLER
1321
PROCESSOR
1310
STORAGE DEVICE
1340
TEMPORARY STORAGE DEVICE
1330
INTERFACE
EXTERNAL DEVICE

FIG. 13


1400
1420
MEMORY CONTROLLER
1421
PROCESSOR
1410
MEMORY
1440
BUFFER MEMORY
1430
INTERFACE
EXTERNAL DEVICE

CHALCOGENIDE MATERIAL AND ELECTRONIC DEVICE INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This patent document claims priority to Korean Patent Application No. 10-2018-0096780, entitled "CHALCOGENIDE MATERIAL AND ELECTRONIC DEVICE INCLUDING THE SAME" and filed on Aug. 20, 2018, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

This patent document relates to memory circuits or devices and their applications in electronic devices or systems.

BACKGROUND

Recently, as electronic devices or appliances trend toward miniaturization, low power consumption, high performance, multi-functionality, and so on, there is a demand for electronic devices capable of storing information in various electronic devices or appliances such as a computer, a portable communication device, and so on, and research and development for such electronic devices have been conducted. Examples of such electronic devices include electronic devices which can store data using a switching characteristic between different resistance states according to an applied voltage or current, and can be implemented in various configurations, for example, an RRAM (resistive random access memory), a PRAM (phase change random access memory), an FRAM (ferroelectric random access memory), an MRAM (magnetic random access memory), an E-fuse, etc.

SUMMARY

The disclosed technology in this patent document includes memory circuits or devices and their applications in electronic devices or systems and various implementations of an electronic device, in which an electronic device includes a semiconductor memory (or a semiconductor memory device) which can improve characteristics of a selection element.

In one aspect, a chalcogenide material may include 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium and 1-10 at % of tellurium.

Implementations of the above chalcogenide material may include one or more the following.

Content of silicon may be 1-5 at %. Content of germanium may be 15-20 at %. Content of arsenic may be 25-30 at %. Content of selenium may be 42-47 at %. Content of tellurium may be 2-8 at %. A sum of content of silicon and the content of germanium may be 20 at % or more.

In another aspect, an electronic device may include a switching element including a chalcogenide material, the chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium and 1-10 at % of tellurium; a first electrode electrically coupled to the switching element; and a second electrode electrically coupled to the switching element.

Implementations of the above electronic device may include one or more the following.

Content of silicon may be 1-5 at %. Content of germanium may be 15-20 at %. Content of arsenic may be 25-30 at %. Content of selenium may be 42-47 at %. Content of tellurium may be 2-8 at %. A sum of content of silicon and the content of germanium may be 20 at % or more.

In further another aspect, an electronic device may include a semiconductor memory device, wherein the semiconductor memory device may include a first memory cell including a switching element, wherein the first switching element may include a chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium and 1-10 at % of tellurium.

Implementations of the above electronic device may include one or more the following.

The semiconductor memory device may further include a second memory cell including a second switching element, the second switching element having a chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium, and the first memory cell and the second memory cell may further include a first memory layer and a second memory layer, respectively, each of the first and second memory layers switching between different resistance states according to a voltage or a current applied thereto. The first switching element and the second switching element may control access to the first memory layer and the second memory layer, respectively. The semiconductor memory device may include a plurality of memory cells including the first memory cell, wherein the semiconductor device may further include: a plurality of first lines disposed between a substrate and the plurality of memory cells, each of the plurality of first lines extending in a first direction; and a plurality of second lines disposed over the plurality of memory cells, each of the plurality of second lines extending in a second direction that crosses the first direction, and wherein the plurality of memory cells are disposed at respective intersections of the first lines and the second lines. The semiconductor memory device may further include a capping layer disposed over at least side surfaces of the first memory cell. Content of silicon may be 1-5 at %. Content of germanium may be 15-20 at %. Content of arsenic may be 25-30 at %. Content of selenium may be 42-47 at %. Content of tellurium may be 2-8 at %. A sum of content of silicon and the content of germanium may be 20 at % or more.

The electronic device may further include a microprocessor which includes: a control unit configured to receive a signal including a command from an outside of the microprocessor, and performs extracting, decoding of the command, or controlling input or output of a signal of the microprocessor; an operation unit configured to perform an operation based on a result that the control unit decodes the command; and a memory unit configured to store data for performing the operation, data corresponding to a result of performing the operation, or an address of data for which the operation is performed, wherein the semiconductor memory is part of the memory unit in the microprocessor.

The electronic device may further include a processor which includes: a core unit configured to perform, based on a command inputted from an outside of the processor, an operation corresponding to the command, by using data; a cache memory unit configured to store data for performing the operation, data corresponding to a result of performing the operation, or an address of data for which the operation is performed; and a bus interface connected between the core unit and the cache memory unit, and configured to transmit data between the core unit and the cache memory unit, wherein the semiconductor memory is part of the cache memory unit in the processor.

The electronic device may further include a processing system which includes: a processor configured to decode a command received by the processor and control an operation for information based on a result of decoding the command; an auxiliary memory device configured to store a program for decoding the command and the information; a main memory device configured to call and store the program and the information from the auxiliary memory device such that the processor can perform the operation using the program and the information when executing the program; and an interface device configured to perform communication between at least one of the processor, the auxiliary memory device and the main memory device and the outside, wherein the semiconductor memory is part of the auxiliary memory device or the main memory device in the processing system.

The electronic device may further include a data storage system which includes: a storage device configured to store data and conserve stored data regardless of power supply; a controller configured to control input and output of data to and from the storage device according to a command inputted from an outside; a temporary storage device configured to temporarily store data exchanged between the storage device and the outside; and an interface configured to perform communication between at least one of the storage device, the controller and the temporary storage device and the outside, wherein the semiconductor memory is part of the storage device or the temporary storage device in the data storage system.

The electronic device may further include a memory system which includes: a memory configured to store data and conserve stored data regardless of power supply; a memory controller configured to control input and output of data to and from the memory according to a command inputted from an outside; a buffer memory configured to buffer data exchanged between the memory and the outside; and an interface configured to perform communication between at least one of the memory, the memory controller and the buffer memory and the outside, wherein the semiconductor memory is part of the memory or the buffer memory in the memory system.

In still further another aspect, an electronic device may include a semiconductor memory device, wherein the semiconductor memory device may include: a substrate; a plurality of first lines disposed over the substrate and each extending in a first direction; a plurality of second lines each extending in a second direction that crosses the first direction; and a plurality of memory cells disposed at respective intersections of the plurality of first lines and the plurality of second lines, wherein each of the plurality of memory cells may include: a variable resistance layer switching between different resistance states according to a voltage or a current applied thereto; and a selection element layer controlling access to the variable resistance layer, and wherein the selection element layer may include a chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium and 1-10 at % of tellurium.

Implementations of the above method may include one or more the following.

The variable resistance layer may include any one of a metal oxide, a phase change material, a ferroelectric material, a ferromagnetic material, and a combination thereof. The selection element layer may have either one of a single-layered structure and a multi-layered structure. Each of the plurality of memory cells may further include: a lower electrode layer coupled to a lowermost portion of each of the plurality of memory cells and functioning as a transmission path of a voltage or a current between a corresponding one of the plurality of first lines and a portion other than the lowermost portion of each of the memory cells; a middle electrode layer physically separating the selection element layer from the variable resistance layer and electrically coupling the selection element layer to the variable resistance layer; and an upper electrode layer coupled to an uppermost portion of each of the plurality of memory cells and functioning as a transmission path of a voltage or a current between a corresponding one of the plurality of second lines and a portion other than the uppermost portion of each of the memory cells. The semiconductor memory device may further include a capping layer disposed over at least side surfaces of the plurality of memory cells. Content of silicon may be 1-5 at %. Content of germanium may be 15-20 at %. Content of arsenic may be 25-30 at %. Content of selenium may be 42-47 at %. Content of tellurium may be 2-8 at %. A sum of content of silicon and the content of germanium may be 20 at % or more.

These and other aspects, implementations and associated advantages are described in greater detail in the drawings, the description and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a normalized band gap energy (Eg) according to Te content in a chalcogenide material in accordance with an implementation of the disclosed technology.

FIG. **2** illustrates a normalized off current (Ioff) according to Te content in a chalcogenide material in accordance with an implementation of the disclosed technology.

FIG. **3** illustrates a normalized trap density according to Te content in a chalcogenide material in accordance with an implementation of the disclosed technology.

FIG. **4** illustrates a normalized threshold voltage (Vth) according to Te content in a chalcogenide material in accordance with an implementation of the disclosed technology.

FIG. **5** illustrates a normalized threshold voltage (Vth) distribution according to the Te content in a chalcogenide material.

FIG. **6** is a perspective view of a semiconductor memory in accordance with an implementation of the disclosed technology.

FIGS. **7**A to **7**D are cross-sectional views illustrating an exemplary semiconductor memory and a method for fabricating the same in accordance with an implementation of the disclosed technology.

FIG. **8** is a cross-sectional view illustrating a semiconductor memory in accordance with an implementation of the disclosed technology.

FIG. **9** is an example of configuration diagram of a microprocessor implementing memory circuitry based on an implementation of the disclosed technology.

FIG. **10** is an example of configuration diagram of a processor implementing memory circuitry based on an implementation of the disclosed technology.

FIG. **11** is an example of configuration diagram of a system implementing memory circuitry based on an implementation of the disclosed technology.

FIG. **12** is an example of configuration diagram of a data storage system implementing memory circuitry based on an implementation of the disclosed technology.

FIG. **13** is an example of configuration diagram of a memory system implementing memory circuitry based on an implementation of the disclosed technology.

DETAILED DESCRIPTION

Various examples and implementations of the disclosed technology are described below in detail with reference to the accompanying drawings.

The drawings may not be necessarily to scale and in some instances, proportions of at least some of substrates in the drawings may have been exaggerated to illustrate certain features of the described examples or implementations. In presenting a specific example in a drawing or description having two or more layers in a multi-layer substrate, the relative positioning relationship of such layers or the sequence of arranging the layers as shown reflects a particular implementation for the described or illustrated example and a different relative positioning relationship or sequence of arranging the layers may be possible.

In accordance with implementations of the present disclosure, a chalcogenide material which is useful for a switching element may be provided. A chalcogenide is a chemical compound consisting of at least one chalcogen anion and one or more electropositive materials. The chalcogenide material may be used as a phase change material or a switching element depending on a combination of constituent elements and the contents thereof.

In an implementation of the disclosed technology, a chalcogenide material may include 1-10 atomic percent (at %) of silicon (Si), 10-20 at % of germanium (Ge), 25-35 at % of arsenic (As), 40-50 at % of selenium (Se), and 1-10 at % of tellurium (Te). In another implementation of the disclosed technology, a chalcogenide material may include 1-5 at % of silicon (Si), 15-20 at % of germanium (Ge), 25-30 at % of arsenic (As), 42-47 at % of selenium (Se), and 2-8 at % of tellurium (Te). In further another implementation of the disclosed technology, a chalcogenide material may include about 1.5 at % (e.g., 1.4-1.6 at %, 1.45-1.55 at %, 1.47-1.53 at %, or 1.49-1.51 at %) of silicon (Si), about 19.5 at % (e.g., 19.4-19.6 at %, 19.45-19.55 at %, 19.47-19.53 at %, or 19.49-19.51 at %) of germanium (Ge), about 29.0 at % (e.g., 28.9-29.1 at %, 28.95-29.05 at %, 28.97-29.03 at %, or 28.99-29.01 at %) of arsenic (As), about 45.0 at % (e.g., 44.9-45.1 at %, 44.95-45.05 at %, 44.97-45.03 at %, or 44.99-45.01 at %) of selenium (Se) and 5.0 at % (e.g., 4.9-5.1 at %, 4.95-5.05 at %, 4.97-5.03 at %, or 4.99-5.01 at %) of tellurium (Te).

In implementations of the disclosed technology, each constituent element and its content in the chalcogenide material may be selected such that an electronic device including the chalcogenide material can exhibit overall optimal effects in terms of voltage drift, a threshold voltage (Vth), an off current (Ioff), Vth distribution, endurance, and the like. Although it is possible to improve an individual characteristic among the above characteristics by suitably selecting any one constituent element and its content, other characteristics can be deteriorated. Therefore, it is desirable to select optimum constituent elements and adjust their contents, which can lead to the optimum effect in consideration of the above characteristics together. In implementations of the disclosed technology, each constituent element and its content contained in the chalcogenide material may be determined in consideration of balancing various aspects of the device performances.

In the chalcogenide material, silicon (Si) and germanium (Ge) may affect voltage drift (or threshold voltage drift) and thermal stability. The voltage drift may represent a change in a threshold voltage (Vth) of a selection element according to a delay time (or a device delay time) of a device that includes the selection element. For example, the device delay time is a delay between an input pulse applied to a first end of the device and an output pulse generated at a second end of the device in response to the input pulse, the device including the selection element and a variable resistance element that are coupled to each other in series. As a value of the voltage drift is decreased, the device can exhibit better characteristics. For example, if the device according to an implementation has a difference between a first threshold voltage at a first device delay time and a second threshold voltage at a second given delay time and the difference is smaller than that of a conventional device, the device performs better than the conventional device. Silicon (Si) may function to substantially suppress an occurrence of voltage drift acceleration, which indicates an increased difference between threshold voltages especially when the device delay time is relatively long (e.g., 100 ms or longer). However, a degree of voltage drift acceleration may not be decreased in proportion to an increased amount of the silicon (Si) content. Rather, when the silicon (Si) content is increased, other device characteristics may be deteriorated. Therefore, the silicon (Si) content may be determined in such a range as to reduce deterioration of other device characteristics while reducing the voltage drift and enhancing the thermal stability.

In implementations of the disclosed technology, the silicon (Si) content in a chalcogenide material may be 1-10 at %, or 1-5 at %. When the silicon (Si) content is less than 1 at %, the Vth change according to the device delay time may be nonlinearly and significantly increased so that the voltage drift may be accelerated. When the silicon (Si) content in the chalcogenide material is greater than 10 at %, other device characteristics may be deteriorated. For example, deterioration of the endurance due to an increase in hard fail and an increase in a reduction amount of the Vth, an increase in the voltage drift, an increase in the Ioff, and an increase in Vth distribution may occur.

Germanium (Ge) included in the chalcogenide material may affect voltage drift and thermal stability together with silicon (Si). Germanium (Ge) may function to substantially suppress voltage drift acceleration (e.g., acceleration of a Vth increase) and control the voltage drift, especially when the device delay time is relatively short (e.g., 100 ms or shorter). The germanium (Ge) content may be determined in such a range as to reduce deterioration of other device characteristics while reducing the voltage drift and enhancing the thermal stability.

In implementations of the disclosed technology, the germanium (Ge) content in a chalcogenide material may be 10-20 at %, or 15-20 at %. When the germanium (Ge) content is less than 15 at %, the silicon (Si) content may be increased, thereby resulting in deterioration of one or more device characteristics. For example, deterioration of the endurance due to an increase in hard fail and an increase in a reduction amount of the Vth, an increase in the voltage drift, an increase in the Ioff, and an increase in the Vth distribution may occur. When the germanium (Ge) content is greater than 20 at %, the thermal stability may be increased, but the voltage drift may be accelerated.

Meanwhile, the silicon (Si) content and the germanium (Ge) content may influence the thermal stability of the chalcogenide material. As the thermal stability is increased, it is possible to increase a margin in a subsequent process and stabilize the one or more device characteristics.

In an implementation, in consideration of the thermal stability, the sum of the silicon (Si) content and the germanium (Ge) content is preferably 20 at % or more. When the sum of the silicon (Si) content and the germanium (Ge) content is 20 at % or more, it is possible to obtain stable characteristics in a process at a relatively high temperature, for example, about 320° C. In this implementation, the chalcogenide material may exhibit stable characteristics when the sum of the silicon (Si) content and the germanium (Ge) content is 20 at % or more. However, in another implementation, the chalcogenide material may exhibit stable characteristics by suitably controlling one or more process variables such as a process temperature, a pressure, and the like, even when the sum of the silicon (Si) content and the germanium (Ge) content is less than 20 at %.

Arsenic (As) included in the chalcogenide material may contribute to forming an amorphous structure of the chalcogenide material.

In implementations of the disclosed technology, the arsenic (As) content may be 25-35 at %, or 25-30 at %. When the arsenic (As) content is less than 25 at %, a switching operation of a device including the chalcogenide material may become unstable. When the arsenic (As) content is greater than 35 at %, content of each of other constituent elements may become relatively low due to the excessive arsenic (As) content, thereby resulting in deterioration of the device characteristics. Therefore, it is desirable to select the optimum content of arsenic (As) by considering these aspects together.

Selenium (Se) included in the chalcogenide material may have an influence on a band gap energy of the device to control a sneak current. Also, selenium (Se) may affect the voltage determination. As the band gap energy is increased, the off current (Ioff) may be decreased, thereby reducing the sneak current.

In implementations of the disclosed technology, the selenium (Se) content in a chalcogenide material may be 40-50 at %, or 42-47 at %. When the selenium (Se) content is less than 40 at %, the device may not function properly due to the excessively low voltage. When the selenium (Se) content is greater than 50 at %, a decrease rate of the Vth according to the cycle is increased, thereby deteriorating the endurance. Therefore, it is desirable to select the optimum content of selenium (Se) considering these aspects together.

Tellurium (Te) may affect voltage distribution (e.g., threshold voltage Vth distribution) of a device and improve voltage instability in response to a current injected into the device.

In implementations of the disclosed technology, the tellurium (Te) content may be 1-10 at %, or 2-8 at %. When the tellurium (Te) content is less than 1 at %, the Vth distribution may not be sufficiently improved. When the tellurium (Te) content is greater than 10 at %, a leakage current may be excessively increased and a threshold voltage may be excessively reduced. Therefore, it is desirable to select the optimum content of tellurium (Te) considering these aspects together, as will be explained below in more detail with reference to FIGS. **1** to **5**.

FIGS. **1** to **5** show effects of content of tellurium (Te) in chalcogenide materials on the device characteristics. The chalcogenide materials shown in each of FIGS. **1** to **5** include content of tellurium (Te) of 0 at %, 5 at %, and 10 at %, respectively. When the content of tellurium (Te) is 10 at %, expected values for the device characteristics are shown. For example, the values of the device characteristics shown in FIGS. **1** to **5** may be calculated by extrapolating two or more values at respective atomic percentages that are greater than 5 at % and less than 10 at %.

Referring to FIG. **1**, the effect of content of tellurium (Te) in each of chalcogenide materials on a band gap energy of a device including a corresponding chalcogenide material will be explained.

FIG. **1** illustrates a normalized band gap energy (Eg) according to Te content in a chalcogenide material in accordance with an implementation of the disclosed technology. In FIG. **1**, the vertical axis represents a normalized band gap energy (Eg) and the horizontal axis represents the Te content. For example, values of band gap energy (Eg) at the Te content of 0 at %, 5 at % and 10 at % are each normalized by a value of band gap energy (Eg) at the Te content of 0 at %.

Referring to FIG. **1**, as the Te content is increased, As_2Te_3 bonding is increased and the level of band gap energy (Eg) is decreased, which may lead to an increase in a leakage current. Therefore, the maximum content of tellurium (Te) may be determined in consideration of deterioration of one or more device characteristics due to the increase in the leakage current.

FIG. **2** illustrates a normalized off current (Ioff) according to Te content in a chalcogenide material in accordance with an implementation of the disclosed technology. In FIG. **2**, the vertical axis represents a normalized off current (Ioff) and the horizontal axis represents the Te content. For example, magnitudes of the off current (Ioff) at the Te content of 0 at %, 5 at % and 10 at % are each normalized by a magnitude of the off current (Ioff) at the Te content of 0 at %.

The off current (Ioff) may refer to an electric current in an off state and affect a sneak current. The sneak current may refer to an electric current that flows in one or more paths other than a desirable path. For example, the sneak current may include a current flowing through an unselected memory cell, rather than a selected memory cell. In most cases, the sneak current may be undesirable, because, for example, the sneak current may cause read margin degradation and increase power consumption. When the off current is increased, the sneak current is also increased, and thus it may be desirable to decrease the off current in order to improve the device characteristics.

Referring to FIG. **2**, as the Te content is increased, the off current is increased. Therefore, the maximum Te content may be determined in consideration of deterioration of one or more device characteristics due to the increase in the off current.

FIG. **3** illustrates a normalized trap density according to Te content in a chalcogenide material in accordance with an implementation of the disclosed technology. In FIG. **3**, the vertical axis represents a normalized trap density and the horizontal axis represents the Te content. For example, values of the trap density at the Te content of 0 at %, 5 at % and 10 at % are each normalized by a value of the trap density at the Te content of 0 at %.

Referring to FIG. **3**, as the Te content is increased, the trap density is increased.

FIG. **4** illustrates a normalized threshold voltage (Vth) according to the Te content in a chalcogenide material in accordance with an implementation of the disclosed technology. In FIG. **4**, the vertical axis represents a normalized Vth and the horizontal axis represents the Te content. For example, levels of the threshold voltages at the Te content of 0 at %, 5 at % and 10 at % are each normalized by a level of the threshold voltage at the Te content of 0 at %.

The Vth should be adjusted to an appropriate level for a stable operation of a device including the chalcogenide material. Specifically, if the Vth is excessively decreased, such a device may not function properly.

Referring to FIG. **4**, as the Te content is increased, the Vth is decreased. This is because the Eg is decreased as the Te content is increased as shown in FIG. **1**. Therefore, the maximum content of tellurium (Te) may be determined in consideration of prohibiting the Vth from being excessively decreased and keeping the Vth at a sufficiently high level to ensure a stable operation.

FIG. **5** illustrates normalized Vth distribution according to Te content in a chalcogenide material in accordance with an implementation of the disclosed technology. In FIG. **5**, the vertical axis represents the normalized Vth distribution and the horizontal axis represents the Te content.

The Vth distribution may represent a degree of change in the Vth according to repeated measurements of the Vth. For example, a value of the Vth distribution may be a variance of threshold voltages in a plurality of selection elements after a given number of switching operations are performed. Each of the plurality of selection elements may include a chalcogenide material with specific Te content. Values of the Vth distribution at the Te content of 0 at %, 5 at % and 10 at % may be normalized by a value of the Vth distribution at the Te content of 0 at %. In order to improve the device characteristics, it may be desirable to decrease the degree of the Vth change.

Referring to FIG. **5**, as the Te content is increased, the Vth distribution is decreased. Without intending to be limited by theory, it is believed that Te doping makes the phonon frequency relatively low to decrease irregular collisions, thereby decreasing the Vth distribution.

When the Te content is increased, the Vth distribution is improved, but the off current may be increased and the Vth may be excessively decreased. As a result, it may be difficult to secure a stable operation of the device. Therefore, it is desirable to determine the Te content in consideration of overall characteristics of the device. For example, the Te content may be selected to exhibit the beneficial effect of improving the Vth distribution and decrease deterioration of other device characteristics.

The chalcogenide material in accordance with the above-described implementations may include silicon (Si), germanium (Ge), arsenic (As), selenium (Se), and tellurium (Te) as constituent elements, wherein the content of each constituent element may be selected to exhibit the optimum effect in consideration of balancing the overall characteristics of the device. For example, the silicon (Si) content may be selected to substantially inhibit the voltage drift acceleration and reduce deterioration of other device characteristics. And, the tellurium (Te) content may be selected to exhibit the beneficial effect of improving the Vth distribution and decrease deterioration of other device characteristics.

The chalcogenide material may be prepared by various methods such as physical vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer deposition (ALD), ion implantation, and the like.

In an implementation, a Si—Ge—As—Se—Te chalcogenide material may be formed through a physical deposition process by using a SiGeAsSeTe alloy target, for example, a sputtering process.

In another implementation, a Si—Ge—As—Se—Te chalcogenide material may be formed through a physical deposition process by using a Te target and a SiGeAsSe alloy target, for example, a co-sputtering process.

In further another implementation, a Si—Ge—As—Se—Te chalcogenide material may be formed by incorporating Te into a Si—Ge—As—Se material using a sputtering process, an ion implantation process, or both.

In still another implementation, a Si—Ge—As—Se—Te chalcogenide material may be formed by depositing a Te layer and a SiGeAsSe layer and performing a heat treatment to cause a reaction between the Te layer and the SiGeAsSe layer.

In still further another implementation, a Si—Ge—As—Se—Te chalcogenide material may be formed by depositing a plurality of Te layers and a plurality of SiGeAsSe layers and performing a heat treatment to cause a reaction between the Te layers and the SiGeAsSe layers.

An element including a chalcogenide material in accordance with an implementation may function as a switching element according to types and composition of constituent elements. The switching element using the chalcogenide may include an ovonic memory switching (OMS) element and an ovonic threshold switching (OTS) element. For the OMS element, when a pulse is applied to the OMS element, the phase of a material is changed. When a pulse is applied to the OTS element, the electrical characteristic is changed from a nonconductor state to a conductor state in a single phase (usually an amorphous phase), and when the pulse is removed, it returns to its original nonconductor state. The OTS element may have a high resistance in response to a voltage less than a given threshold voltage (Vth). When a voltage greater than the Vth is applied, a current flows through the OTS element at a relatively low voltage that is substantially constant and the OTS element exhibits a low impedance. When the current through the OTS element becomes lower than a holding current, the OTS element returns to a high-impedance condition. This I-V characteristics of the OTS element may be substantially symmetrical.

Hereinafter, an electronic device including a switching element including the chalcogenide material in accordance with the above-described implementations will be explained.

FIG. **6** is a perspective view of a semiconductor memory in accordance with an implementation of the disclosed technology.

The semiconductor memory in accordance with the implementation in FIG. **8** of the present disclosure may have a cross-point structure which includes first lines **110** each extending in a first direction, second lines **150** located over the first lines **110** and each extending in a second direction crossing the first direction, and memory cells **120** located between the first lines **110** and the second lines **150**. The memory cells **120** are disposed at respective intersections of the first lines **110** and the second lines **150**.

FIGS. **7**A to **7**D are cross-sectional views illustrating a semiconductor memory and a method for fabricating the semiconductor memory in accordance with an implementation of the disclosed technology.

FIG. **7**D is a cross-sectional view of a portion of the semiconductor device taken along line A-A' of FIG. **6**.

Referring to FIG. **7**A, a substrate **100** including given structures (not shown) may be provided. For example, the given structures may include one or more transistors for controlling the first lines **110**, the second lines **150**, or the first and second lines **110** and **150** of FIGS. **6** and **7**D, which are formed over the substrate **100**.

Then, the first lines **110** each extending in a first direction (e.g., a horizontal direction in FIG. **7**A) may be formed over the substrate **100**. The first lines **110** may have a single-layered structure or a multi-layered structure, and may include a conductive material such as a metal, a metal nitride, etc. The first lines **110** may be formed by depositing a layer that includes the conductive material and patterning the deposited layer. Spaces between the first lines **110** may be filled with an insulating material (not shown).

Then, a plurality of memory cells **120** may be formed over the first lines **110**. In the implementation shown in FIG. **7**A, each of the plurality of memory cells **120** may have a pillar shape. The plurality of memory cells **120** may be arranged in a matrix having rows and columns. The rows each extend along the first direction and the columns extend along a second direction crossing the first direction. The memory cells **120** may be disposed in respective intersection regions between the first lines **110** and second lines **150**. An intersection region between one of the first lines **110** and one of the second lines **150** is defined, for example, as a three-dimensional region where the first line **110** and the second line **150** overlap each other in a third direction (e.g., a vertical direction in FIG. **7**A) that crosses the first and second directions. In an implementation, each of the memory cells **120** may have a size that is substantially equal to or smaller than that of the intersection region between each corresponding pair of the first lines **110** and the second lines **150**. In another implementation, each of the memory cells **120** may have a size that is larger than that of the intersection region between each corresponding pair of the first lines **110** and the second lines **150**.

The memory cells **120** may be formed by depositing a plurality of material layers (not shown) over a structure including the first lines **110** and the insulating material (not shown), forming a plurality of hard mask patterns **130** over the plurality of material layers, and etching the material layers using the hard mask patterns **130** as an etching barrier. Therefore, each of the hard mask patterns **130** has sidewalls substantially aligned with sidewalls of each of the corresponding memory cells **120**.

The hard mask patterns **130** may function as an etching barrier during etching the material layers (not shown) for forming the memory cells **120** and include one or more of various materials having etch selectivity with respect to the memory cells **120**. For example, each of the hard mask patterns **130** may have a single-layered structure or a multi-layered structure and include an insulating material such as a silicon oxide, a silicon nitride, a silicon oxynitride, etc.

Also, in this implementation of FIG. **7**A, each of the plurality of memory cells **120** may include a lower electrode layer **121**, a selection element layer **123**, a middle electrode layer **125**, a variable resistance layer **127**, and an upper electrode layer **129**, which are sequentially stacked.

Specifically, the lower electrode layer **121** may be located at a lowermost portion of each of the memory cells **120** and function as a transmission path of a voltage or a current between a corresponding one of the first lines **110** and the remaining portion (e.g., the elements **123**, **125**, **127**, and **129**) of each of the memory cells **120**. The middle electrode layer **125** may physically separate the selection element layer **123** from the variable resistance layer **127**, and electrically couple the selection element layer **123** to the variable resistance layer **127**. For example, a current flow through the selection element layer **123**, the middle electrode layer **125**, and the variable resistance layer **127**, when a voltage level across the selection element layer **123** is equal to or greater than a given threshold voltage. The upper electrode layer **129** may be located at an uppermost portion of each of the memory cells **120** and function as a transmission path of a voltage or a current between the remaining portion (e.g., the elements **121**, **123**, **125**, and **127**) of each of the memory cells **120** and a corresponding one of the second lines **150** of FIG. **7**D. Each of the lower electrode layer **121**, the middle electrode layer **125**, and the upper electrode layer **129** may have a single-layered structure or a multi-layered structure and include a conductive material such as a metal, a metal nitride, a conductive carbon material, etc.

The selection element layer **123** may control access to the variable resistance layer **127**. That is, the selection element layer **123** may function as a switching element and have a selection element characteristic, which substantially prevents a current from passing through the selection element layer **123** when a magnitude of an applied voltage or an applied current is lower than a critical value (or a threshold value), and causes a current to pass through the selection element layer **123** when a magnitude of the applied voltage or the applied current is substantially equal to or greater than the critical value. For example, a magnitude of the current passing through the selection element layer **123** is proportional to a magnitude of the voltage or current applied to the selection element layer **123**. The selection element layer **123** may have a single-layered structure, or a multi-layered structure that exhibits the selection element characteristic using a combination of two or more layers.

For example, the selection element layer **123** may include the chalcogenide material in accordance with the above-described implementations. Specifically, in an implementation of the disclosed technology, the selection element layer **123** may include a chalcogenide material including 1-10 at % of silicon (Si), 10-20 at % of germanium (Ge), 25-35 at % of arsenic (As), 40-50 at % of selenium (Se), and 1-10 at % of tellurium (Te). Moreover, in an implementation of the disclosed technology, the selection element layer **123** may include a chalcogenide material including 1-5 at % of silicon (Si), 15-20 at % of germanium (Ge), 25-30 at % of arsenic (As), 42-47 at % of selenium (Se), and 3-7 at % of tellurium (Te). Further, in an implementation of the disclosed technology, the selection element layer **123** may include a chalcogenide material including about 1.5 at % of silicon (Si), about 19.5 at % of germanium (Ge), about 29.0 at % of arsenic (As), about 45.0 at % of selenium (Se), and about 5.0 at % of tellurium (Te). Such a chalcogenide material has been explained in detail in the above implementations, the detailed explanation for the chalcogenide material is omitted for the interest of brevity.

As described above, the chalcogenide material included in the selection element layer **123** may include silicon (Si), germanium (Ge), arsenic (As), selenium (Se), and tellurium (Te) as constituent elements, wherein the content of each constituent element may be selected to exhibit the optimum effect in consideration of balancing the overall characteristics of the device. For example, the silicon (Si) content may be selected to substantially inhibit the voltage drift acceleration and reduce deterioration of other device characteristics. And, the tellurium (Te) content may be selected to improve the Vth distribution and reduce deterioration of other device characteristics. Therefore, it is possible to effectively suppress the voltage drift acceleration at a relatively long delay time as well as a relatively short delay time, effectively improve the Vth distribution, and substantially prevent deterioration of other device characteristics, resulting in superior device characteristics and improved reliability of the device.

The variable resistance layer **127** may switch between different resistance states according to a voltage or a current applied to the variable resistance layer **127** through the upper electrode layer **129** and the middle electrode layer **125**, thereby storing data having different values. For example, when the variable resistance layer **127** is in a low resistance state, data having a first logic value of '1' may be stored in the variable resistance layer **127**. On the other hand, when the variable resistance layer **127** is in a high resistance state, data having a second logic value of '0' may be stored in the variable resistance layer **127**. The variable resistance layer **127** may include one or more of various materials that are used in RRAM, PRAM, FRAM, MRAM, or the like. For example, the variable resistance layer **127** may include any of metal oxides, such as transition metal oxides or perovskite-based materials; phase-change materials, such as chalcogenide-based materials; ferroelectric materials, ferromagnetic materials; and the like. The variable resistance layer **127** may have a single-layered structure, or a multi-layered structure that shows a variable resistance characteristic by a combination of two or more layers. However, other implementations are also possible. For example, the memory cells **120** may include a memory layer, which can store data in different ways than the above-described variable resistance layer **127**.

In the implementation shown in FIG. **7**A, each of the memory cells **120** includes the lower electrode layer **121**, the selection element layer **123**, the middle electrode layer **125**, the variable resistance layer **127**, and the upper electrode layer **129**. However, implementations of the present patent document are not limited thereto, and the memory cells **120** may have various structures. In some implementations, one or more of the lower electrode layer **121**, the middle electrode layer **125**, and the upper electrode layer **129** may be omitted. In some implementations, the stacked order of the selection element layer **123** and the variable resistance layer **127** may be reversed with respect to the orientation shown in FIG. **7**A, such that the selection element layer **123** may be disposed over the variable resistance layer **127**. In some implementations, in addition to the layers **121**, **123**, **125**, **127**, and **129** shown in FIG. **7**A, the memory cells **120** may further include one or more layers (not shown) for enhancing characteristics of the memory cells **120**, improving fabricating processes, or both.

A neighboring pair of the plurality of memory cells **120** may be spaced apart from each other at a given interval, and trenches may be present between the plurality of memory cells **120**. In an implementation, the given interval is a predetermined interval, and a trench between a neighboring pair of the plurality of memory cells **120** may have a height to width ratio (or an aspect ratio) in a range from 1:1 to 40:1, from 10:1 to 40:1, from 10:1 to 20:1, from 5:1 to 10:1, from 10:1 to 15:1, from 1:1 to 25:1, from 1:1 to 30:1, from 1:1 to 35:1, or from 1:1 to 45:1.

In some implementations, the trench may have sidewalls that are substantially perpendicular to an upper surface of the substrate **100**. In some implementations, neighboring trenches may be spaced substantially equidistant from each other. For example, a first pair of trenches neighboring each other in a first direction (e.g., the first direction of FIG. **6**) may be spaced apart from each other by substantially the same distance as a second pair of trenches neighboring each other in a second direction (e.g., the second direction of FIG. **6**). In some implementations, distances between the neighboring trenches may vary.

Referring to FIG. **7**B, an interlayer dielectric layer **140** may be formed over the structure illustrated in FIG. **7**A. The interlayer dielectric layer **140** may include various insulating materials such as a silicon oxide, a silicon nitride, a silicon oxynitride and the like. Moreover, the interlayer dielectric layer **140** may be formed along a lower profile. For example, the interlayer dielectric layer **140** is formed over the first lines **110**, sidewalls of the memory cells **120**, and upper surfaces and sidewalls of the hard mask patterns **130**.

Referring to FIG. **7**C, a planarization process may be performed on the interlayer dielectric layer **140** until the upper electrode **129** is exposed. The planarization process may be performed by a chemical mechanical polishing (CMP) process, an etch process, a cleaning process, or any suitable planarization process. Since the planarization process is performed until upper surfaces of the upper electrode layers **129** of the memory cells **120** are exposed, the hard mask pattern **130** may be removed by the planarization process.

Referring to FIG. **7**D, a plurality of second lines **150** may be formed over the memory cells **120** and the interlayer dielectric layer **140**. The plurality of second lines **150** may be respectively coupled to the upper surfaces of the memory cells **120**. Each of the plurality of second lines **150** extend in the second direction crossing the first direction. For example, the second direction may be perpendicular to the line A-A' of FIG. **6**. Each of the second lines **150** may have a single-layer structure or a multi-layer structure, and include a conductive material, such as any of a metal, a metal nitride, and the like. The second lines **150** may be formed by depositing a conductive material and patterning the deposited material. Spaces between neighboring second lines **150** may be filled with an insulating material (not shown).

Through the processes as described above, the semiconductor memory shown in FIG. **7**D may be fabricated.

In the implementation shown in to FIG. **7**D, the semiconductor memory (or the semiconductor memory device) may include the memory cells **120** disposed at intersection regions between the first lines **110** each extending in the first direction and the second lines **150** each extending in the second direction. In an implementation, the selection element layer **123** of the memory cells **120** may include a chalcogenide material including 1-10 at % of silicon (Si), 10-20 at % of germanium (Ge), 25-35 at % of arsenic (As), 40-50 at % of selenium (Se), and 1-10 at % of tellurium (Te). In an implementation, the selection element layer **123** of the memory cells **120** may include a chalcogenide material including 1-5 at % of silicon (Si), 15-20 at % of germanium (Ge), 25-30 at % of arsenic (As), 42-47 at % of selenium (Se), and 2-8 at % of tellurium (Te).

The memory cells **120** may store data having different values according to a voltage or current that is applied thereto through the first lines **110** and the second lines **150**. In particular, when the memory cells **120** each include variable resistance elements, each of the memory cells **120** may store data by switching between different resistance states.

One or more of the first lines **110** each may function as a word line and one or more of the second lines **150** each may function as a bit line, and vice versa.

In the semiconductor memory of FIG. **9**D fabricated by a method according to an implementation of the present disclosure, the selection element layer **123** of the memory cells **120** includes the chalcogenide material having specific composition of four components so that the optimum effects can be exhibited in terms of various aspects of device characteristics such as voltage drift, a Vth, a VFF, an Ioff, Vth distribution, endurance, and the like.

FIG. **8** is a cross-sectional view illustrating a semiconductor memory in accordance with an implementation of the disclosed technology. Detailed descriptions of parts that are substantially the same as those of the implementation described above with reference to FIGS. 7A to 7D will be omitted for the interest of brevity.

Referring to FIG. 8, a capping layer 160 may be further formed on sidewalls of the memory cells 120 and over the first lines 110. The capping layer 160 may function to protect the memory cells 120 and have a single-layered structure or a multi-layered structure including various insulating materials such as a silicon nitride and the like.

The capping layer 160 may be formed by forming a material layer for the capping layer 160 over the structure of FIG. 7A, for example, on sidewalls of the memory cells 120 and sidewalls and upper surfaces of the hard mask pattern 130, and then performing the processes of FIGS. 7B to 7D.

As a result, the first lines 110 each extending in a first direction (e.g., the first direction of FIG. 6) and the second lines 150 each extending in a second direction (e.g., the second direction of FIG. 6) are formed over the substrate 100 and the memory cells 120 may be disposed in respective intersection regions between the first lines 110 and the second lines 150. In an implementation, the selection element layer 123 of each of the memory cells 120 may include the chalcogenide material including 1-10 at % of Si, 10-20 at % of Ge, 25-35 at % of As, 40-50 at % of Se, and 1-10 at % of Te. In an implementation, the selection element layer 123 of each of the memory cells 120 may include a chalcogenide material including 1-5 at % of silicon (Si), 15-20 at % of germanium (Ge), 25-30 at % of arsenic (As), 42-47 at % of selenium (Se), and 2-8 at % of tellurium (Te).

The sidewalls of the memory cells 120 may be in direct contact with the capping layer 160. The capping layer 160 may include an insulating material and function to protect the memory cells 120.

In the implementations shown in FIGS. 6 to 8, the semiconductor memory having a single-layer cross-point structure has been described. However, in another implementation, a semiconductor memory may have a multi-layer cross-point structure in which two or more cross-point structures may be stacked. Each of the cross-point structures may include first lines 110, second lines 150, and memory cells 120 located at respective intersections between the first lines 110 and the second lines 150.

Memory circuits or semiconductor devices in accordance with implementations based on the disclosed technology can be used in a range of devices or systems. FIGS. 9 to 13 provide some examples of devices or systems that can implement the memory circuits disclosed herein.

FIG. 9 is an example of configuration diagram of a microprocessor implementing memory circuitry based on the disclosed technology.

Referring to FIG. 9, a microprocessor 1000 may perform tasks for controlling and tuning a series of processes of receiving data from various external devices, processing the data, and outputting processing results to external devices. The microprocessor 1000 may include a memory unit 1010, an operation unit 1020, a control unit 1030, and so on. The microprocessor 1000 may be various data processing units such as a central processing unit (CPU), a graphic processing unit (GPU), a digital signal processor (DSP) and an application processor (AP).

The memory unit 1010 is a part which stores data in the microprocessor 1000, as a processor register, register or the like. The memory unit 1010 may include a data register, an address register, a floating point register and so on. Besides, the memory unit 1010 may include various registers. The memory unit 1010 may perform the function of temporarily storing data for which operations are to be performed by the operation unit 1020, result data of performing the operations and addresses where data for performing of the operations are stored.

The memory unit 1010 may include one or more of the above-described semiconductor devices in accordance with the implementations. For example, the memory unit 1010 may include a plurality of memory cells each including a switching element, wherein the switching element may include a chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium. Through this, data storage characteristics of the memory unit 1010 may be improved. As a consequence, operating characteristics of the microprocessor 1000 may be improved.

The operation unit 1020 may perform four arithmetical operations or logical operations according to results that the control unit 1030 decodes commands. The operation unit 1020 may include at least one arithmetic logic unit (ALU) and so on.

The control unit 1030 may receive signals from the memory unit 1010, the operation unit 1020 and an external device of the microprocessor 1000, perform extraction, decoding of commands, and controlling input and output of signals of the microprocessor 1000, and execute processing represented by programs.

The microprocessor 1000 according to this implementation may additionally include a cache memory unit 1040 which can temporarily store data to be inputted from an external device other than the memory unit 1010 or to be outputted to an external device. In this case, the cache memory unit 1040 may exchange data with the memory unit 1010, the operation unit 1020 and the control unit 1030 through a bus interface 1050.

FIG. 10 is an example of configuration diagram of a processor implementing memory circuitry based on an implementation of the disclosed technology.

Referring to FIG. 10, a processor 1100 may improve performance and realize multi-functionality by including various functions other than those of a microprocessor which performs tasks for controlling and tuning a series of processes of receiving data from various external devices, processing the data, and outputting processing results to external devices. The processor 1100 may include a core unit 1110 which serves as the microprocessor, a cache memory unit 1120 which serves to storing data temporarily, and a bus interface 1130 for transferring data between internal and external devices. The processor 1100 may include various system-on-chips (SoCs) such as a multi-core processor, a graphic processing unit (GPU) and an application processor (AP).

The core unit 1110 of this implementation is a part which performs arithmetic logic operations for data inputted from an external device, and may include a memory unit 1111, an operation unit 1112 and a control unit 1113.

The memory unit 1111 is a part which stores data in the processor 1100, as a processor register, a register or the like. The memory unit 1111 may include a data register, an address register, a floating point register and so on. Besides, the memory unit 1111 may include various registers. The memory unit 1111 may perform the function of temporarily storing data for which operations are to be performed by the operation unit 1112, result data of performing the operations and addresses where data for performing of the operations are stored. The operation unit 1112 is a part which performs operations in the processor 1100. The operation unit 1112 may perform four arithmetical operations, logical operations, according to results that the control unit **1113** decodes commands, or the like. The operation unit **1112** may include at least one arithmetic logic unit (ALU) and so on. The control unit **1113** may receive signals from the memory unit **1111**, the operation unit **1112** and an external device of the processor **1100**, perform extraction, decoding of commands, controlling input and output of signals of processor **1100**, and execute processing represented by programs.

The cache memory unit **1120** is a part which temporarily stores data to compensate for a difference in data processing speed between the core unit **1110** operating at a high speed and an external device operating at a low speed. The cache memory unit **1120** may include a primary storage section **1121**, a secondary storage section **1122** and a tertiary storage section **1123**. In general, the cache memory unit **1120** includes the primary and secondary storage sections **1121** and **1122**, and may include the tertiary storage section **1123** in the case where high storage capacity is required. As the occasion demands, the cache memory unit **1120** may include an increased number of storage sections. That is to say, the number of storage sections which are included in the cache memory unit **1120** may be changed according to a design. The speeds at which the primary, secondary and tertiary storage sections **1121**, **1122** and **1123** store and discriminate data may be the same or different. In the case where the speeds of the respective storage sections **1121**, **1122** and **1123** are different, the speed of the primary storage section **1121** may be largest. At least one storage section of the primary storage section **1121**, the secondary storage section **1122** and the tertiary storage section **1123** of the cache memory unit **1120** may include one or more of the above-described semiconductor devices in accordance with the implementations. For example, the cache memory unit **1120** may include a plurality of memory cells each including a switching element, wherein the switching element may include a chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium. Through this, data storage characteristics of the cache memory unit **1120** may be improved. As a consequence, operating characteristics of the processor **1100** may be improved.

Although it was shown in FIG. **10** that all the primary, secondary and tertiary storage sections **1121**, **1122** and **1123** are configured inside the cache memory unit **1120**, it is to be noted that all the primary, secondary and tertiary storage sections **1121**, **1122** and **1123** of the cache memory unit **1120** may be configured outside the core unit **1110** and may compensate for a difference in data processing speed between the core unit **1110** and the external device. Meanwhile, it is to be noted that the primary storage section **1121** of the cache memory unit **1120** may be disposed inside the core unit **1110** and the secondary storage section **1122** and the tertiary storage section **1123** may be configured outside the core unit **1110** to strengthen the function of compensating for a difference in data processing speed. In another implementation, the primary and secondary storage sections **1121**, **1122** may be disposed inside the core units **1110** and tertiary storage sections **1123** may be disposed outside core units **1110**.

The bus interface **1130** is a part which connects the core unit **1110**, the cache memory unit **1120** and external device and allows data to be efficiently transmitted.

The processor **1100** according to this implementation may include a plurality of core units **1110**, and the plurality of core units **1110** may share the cache memory unit **1120**. The plurality of core units **1110** and the cache memory unit **1120** may be directly connected or be connected through the bus interface **1130**. The plurality of core units **1110** may be configured in the same way as the above-described configuration of the core unit **1110**. In the case where the processor **1100** includes the plurality of core unit **1110**, the primary storage section **1121** of the cache memory unit **1120** may be configured in each core unit **1110** in correspondence to the number of the plurality of core units **1110**, and the secondary storage section **1122** and the tertiary storage section **1123** may be configured outside the plurality of core units **1110** in such a way as to be shared through the bus interface **1130**. The processing speed of the primary storage section **1121** may be larger than the processing speeds of the secondary and tertiary storage section **1122** and **1123**. In another implementation, the primary storage section **1121** and the secondary storage section **1122** may be configured in each core unit **1110** in correspondence to the number of the plurality of core units **1110**, and the tertiary storage section **1123** may be configured outside the plurality of core units **1110** in such a way as to be shared through the bus interface **1130**.

The processor **1100** according to this implementation may further include an embedded memory unit **1140** which stores data, a communication module unit **1150** which can transmit and receive data to and from an external device in a wired or wireless manner, a memory control unit **1160** which drives an external memory device, and a media processing unit **1170** which processes the data processed in the processor **1100** or the data inputted from an external input device and outputs the processed data to an external interface device and so on. Besides, the processor **1100** may include a plurality of various modules and devices. In this case, the plurality of modules which are added may exchange data with the core units **1110** and the cache memory unit **1120** and with one another, through the bus interface **1130**.

The embedded memory unit **1140** may include not only a volatile memory but also a nonvolatile memory. The volatile memory may include a DRAM (dynamic random access memory), a mobile DRAM, an SRAM (static random access memory), and a memory with similar functions to above mentioned memories, and so on. The nonvolatile memory may include a ROM (read only memory), a NOR flash memory, a NAND flash memory, a phase change random access memory (PRAM), a resistive random access memory (RRAM), a spin transfer torque random access memory (STTRAM), a magnetic random access memory (MRAM), a memory with similar functions.

The communication module unit **1150** may include a module capable of being connected with a wired network, a module capable of being connected with a wireless network and both of them. The wired network module may include a local area network (LAN), a universal serial bus (USB), an Ethernet, power line communication (PLC) such as various devices which send and receive data through transmit lines, and so on. The wireless network module may include Infrared Data Association (IrDA), code division multiple access (CDMA), time division multiple access (TDMA), frequency division multiple access (FDMA), a wireless LAN, Zigbee, a ubiquitous sensor network (USN), Bluetooth, radio frequency identification (RFID), long term evolution (LTE), near field communication (NFC), a wireless broadband Internet (Wibro), high speed downlink packet access (HSDPA), wideband CDMA (WCDMA), ultra wideband (UWB) such as various devices which send and receive data without transmit lines, and so on.

The memory control unit **1160** is to administrate and process data transmitted between the processor **1100** and an external storage device operating according to a different communication standard. The memory control unit **1160** may include various memory controllers, for example, devices which may control IDE (Integrated Device Electronics), SATA (Serial Advanced Technology Attachment), SCSI (Small Computer System Interface), RAID (Redundant Array of Independent Disks), an SSD (solid state disk), eSATA (External SATA), PCMCIA (Personal Computer Memory Card International Association), a USB (universal serial bus), a secure digital (SD) card, a mini secure digital (mSD) card, a micro secure digital (micro SD) card, a secure digital high capacity (SDHC) card, a memory stick card, a smart media (SM) card, a multimedia card (MMC), an embedded MMC (eMMC), a compact flash (CF) card, and so on.

The media processing unit **1170** may process the data processed in the processor **1100** or the data inputted in the forms of image, voice and others from the external input device and output the data to the external interface device. The media processing unit **1170** may include a graphic processing unit (GPU), a digital signal processor (DSP), a high definition audio device (HD audio), a high definition multimedia interface (HDMI) controller, and so on.

FIG. **11** is an example of configuration diagram of a system implementing memory circuitry based on an implementation of the disclosed technology.

Referring to FIG. **11**, a system **1200** as an apparatus for processing data may perform input, processing, output, communication, storage, etc. to conduct a series of manipulations for data. The system **1200** may include a processor **1210**, a main memory device **1220**, an auxiliary memory device **1230**, an interface device **1240**, and so on. The system **1200** of this implementation may be various electronic systems which operate using processors, such as a computer, a server, a PDA (personal digital assistant), a portable computer, a web tablet, a wireless phone, a mobile phone, a smart phone, a digital music player, a PMP (portable multimedia player), a camera, a global positioning system (GPS), a video camera, a voice recorder, a telematics, an audio visual (AV) system, a smart television, and so on.

The processor **1210** may decode inputted commands and processes operation, comparison, etc. for the data stored in the system **1200**, and controls these operations. The processor **1210** may include a microprocessor unit (MPU), a central processing unit (CPU), a single/multi-core processor, a graphic processing unit (GPU), an application processor (AP), a digital signal processor (DSP), and so on.

The main memory device **1220** is a storage which can temporarily store, call and execute program codes or data from the auxiliary memory device **1230** when programs are executed and can conserve memorized contents even when power supply is cut off. The main memory device **1220** may include a plurality of memory cells each including a switching element, wherein the switching element may include a chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium. Through this, data storage characteristics of the main memory device **1220** may be improved. As a consequence, operating characteristics of the system **1200** may be improved.

Also, the main memory device **1220** may further include a static random access memory (SRAM), a dynamic random access memory (DRAM), and so on, of a volatile memory type in which all contents are erased when power supply is cut off. Unlike this, the main memory device **1220** may not include the semiconductor devices according to the implementations, but may include a static random access memory (SRAM), a dynamic random access memory (DRAM), and so on, of a volatile memory type in which all contents are erased when power supply is cut off.

The auxiliary memory device **1230** is a memory device for storing program codes or data. While the speed of the auxiliary memory device **1230** is slower than the main memory device **1220**, the auxiliary memory device **1230** can store a larger amount of data. The auxiliary memory device **1230** may include one or more of the above-described semiconductor devices in accordance with the implementations. For example, the auxiliary memory device **1230** may include a plurality of memory cells each including a switching element, wherein the switching element may include a chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium. Through this, data storage characteristics of the auxiliary memory device **1230** may be improved. As a consequence, operating characteristics of the system **1200** may be improved.

Also, the auxiliary memory device **1230** may further include a data storage system (see the reference numeral **1300** of FIG. **12**) such as a magnetic tape using magnetism, a magnetic disk, a laser disk using optics, a magneto-optical disc using both magnetism and optics, a solid state disk (SSD), a USB memory (universal serial bus memory), a secure digital (SD) card, a mini secure digital (mSD) card, a micro secure digital (micro SD) card, a secure digital high capacity (SDHC) card, a memory stick card, a smart media (SM) card, a multimedia card (MMC), an embedded MMC (eMMC), a compact flash (CF) card, and so on. Unlike this, the auxiliary memory device **1230** may not include the semiconductor devices according to the implementations, but may include data storage systems (see the reference numeral **1300** of FIG. **12**) such as a magnetic tape using magnetism, a magnetic disk, a laser disk using optics, a magneto-optical disc using both magnetism and optics, a solid state disk (SSD), a USB memory (universal serial bus memory), a secure digital (SD) card, a mini secure digital (mSD) card, a micro secure digital (micro SD) card, a secure digital high capacity (SDHC) card, a memory stick card, a smart media (SM) card, a multimedia card (MMC), an embedded MMC (eMMC), a compact flash (CF) card, and so on.

The interface device **1240** may be to perform exchange of commands and data between the system **1200** of this implementation and an external device. The interface device **1240** may be a keypad, a keyboard, a mouse, a speaker, a mike, a display, various human interface devices (HIDs), a communication device, and so on. The communication device may include a module capable of being connected with a wired network, a module capable of being connected with a wireless network and both of them. The wired network module may include a local area network (LAN), a universal serial bus (USB), an Ethernet, power line communication (PLC), such as various devices which send and receive data through transmit lines, and so on. The wireless network module may include Infrared Data Association (IrDA), code division multiple access (CDMA), time division multiple access (TDMA), frequency division multiple access (FDMA), a wireless LAN, Zigbee, a ubiquitous sensor network (USN), Bluetooth, radio frequency identification (RFID), long term evolution (LTE), near field communication (NFC), a wireless broadband Internet (Wibro), high speed downlink packet access (HSDPA), wideband CDMA

(WCDMA), ultra wideband (UWB), such as various devices which send and receive data without transmit lines, and so on.

FIG. **12** is an example of configuration diagram of a data storage system implementing memory circuitry based on an implementation of the disclosed technology.

Referring to FIG. **12**, a data storage system **1300** may include a storage device **1310** which has a nonvolatile characteristic as a component for storing data, a controller **1320** which controls the storage device **1310**, an interface **1330** for connection with an external device, and a temporary storage device **1340** for storing data temporarily. The data storage system **1300** may be a disk type such as a hard disk drive (HDD), a compact disc read only memory (CDROM), a digital versatile disc (DVD), a solid state disk (SSD), and so on, and a card type such as a USB memory (universal serial bus memory), a secure digital (SD) card, a mini secure digital (MSD) card, a micro secure digital (micro SD) card, a secure digital high capacity (SDHC) card, a memory stick card, a smart media (SM) card, a multimedia card (MMC), an embedded MMC (eMMC), a compact flash (CF) card, and so on.

The storage device **1310** may include a nonvolatile memory which stores data semi-permanently. The nonvolatile memory may include a ROM (read only memory), a NOR flash memory, a NAND flash memory, a phase change random access memory (PRAM), a resistive random access memory (RRAM), a magnetic random access memory (MRAM), and so on.

The controller **1320** may control exchange of data between the storage device **1310** and the interface **1330**. To this end, the controller **1320** may include a processor **1321** for performing an operation for, processing commands inputted through the interface **1330** from an outside of the data storage system **1300** and so on.

The interface **1330** is to perform exchange of commands and data between the data storage system **1300** and the external device. In the case where the data storage system **1300** is a card type, the interface **1330** may be compatible with interfaces which are used in devices, such as a USB memory (universal serial bus memory), a secure digital (SD) card, a mini secure digital (MSD) card, a micro secure digital (micro SD) card, a secure digital high capacity (SDHC) card, a memory stick card, a smart media (SM) card, a multimedia card (MMC), an embedded MMC (eMMC), a compact flash (CF) card, and so on, or be compatible with interfaces which are used in devices similar to the above mentioned devices. In the case where the data storage system **1300** is a disk type, the interface **1330** may be compatible with interfaces, such as IDE (Integrated Device Electronics), SATA (Serial Advanced Technology Attachment), SCSI (Small Computer System Interface), eSATA (External SATA), PCMCIA (Personal Computer Memory Card International Association), a USB (universal serial bus), and so on, or be compatible with the interfaces which are similar to the above mentioned interfaces. The interface **1330** may be compatible with one or more interfaces having a different type from each other.

The temporary storage device **1340** can store data temporarily for efficiently transferring data between the interface **1330** and the storage device **1310** according to diversifications and high performance of an interface with an external device, a controller and a system. The temporary storage device **1340** for temporarily storing data may include one or more of the above-described semiconductor devices in accordance with the implementations. The temporary storage device **1340** may include a plurality of memory cells each including a switching element, wherein the switching element may include a chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium. Through this, data storage characteristics of the storage device **1310** or the temporary storage device **1340** may be improved. As a result, operating characteristics and data storage characteristics of the data storage system **1300** may be improved.

FIG. **13** is an example of configuration diagram of a memory system implementing memory circuitry based on an implementation of the disclosed technology.

Referring to FIG. **13**, a memory system **1400** may include a memory **1410** which has a nonvolatile characteristic as a component for storing data, a memory controller **1420** which controls the memory **1410**, an interface **1430** for connection with an external device, and so on. The memory system **1400** may be a card type such as a solid state disk (SSD), a USB memory (universal serial bus memory), a secure digital (SD) card, a mini secure digital (MSD) card, a micro secure digital (micro SD) card, a secure digital high capacity (SDHC) card, a memory stick card, a smart media (SM) card, a multimedia card (MMC), an embedded MMC (eMMC), a compact flash (CF) card, and so on.

The memory **1410** for storing data may include one or more of the above-described semiconductor devices in accordance with the implementations. For example, the memory **1410** may include a plurality of memory cells each including a switching element, wherein the switching element may include a chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium. Through this, data storage characteristics of the memory **1410** may be improved. As a consequence, operating characteristics and data storage characteristics of the memory system **1400** may be improved.

Also, the memory **1410** according to this implementation may further include a ROM (read only memory), a NOR flash memory, a NAND flash memory, a phase change random access memory (PRAM), a resistive random access memory (RRAM), a magnetic random access memory (MRAM), and so on, which have a nonvolatile characteristic.

The memory controller **1420** may control exchange of data between the memory **1410** and the interface **1430**. To this end, the memory controller **1420** may include a processor **1421** for performing an operation for and processing commands inputted through the interface **1430** from an outside of the memory system **1400**.

The interface **1430** is to perform exchange of commands and data between the memory system **1400** and the external device. The interface **1430** may be compatible with interfaces which are used in devices, such as a USB memory (universal serial bus memory), a secure digital (SD) card, a mini secure digital (MSD) card, a micro secure digital (micro SD) card, a secure digital high capacity (SDHC) card, a memory stick card, a smart media (SM) card, a multimedia card (MMC), an embedded MMC (eMMC), a compact flash (CF) card, and so on, or be compatible with interfaces which are used in devices similar to the above mentioned devices. The interface **1430** may be compatible with one or more interfaces having a different type from each other.

The memory system **1400** according to this implementation may further include a buffer memory **1440** for efficiently transferring data between the interface **1430** and the memory **1410** according to diversification and high performance of an interface with an external device, a memory controller and a memory system. For example, the buffer memory **1440** for temporarily storing data may include one or more of the above-described semiconductor devices in accordance with the implementations. The buffer memory **1440** may include a plurality of memory cells each including a switching element, wherein the switching element may include a chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium. Through this, data storage characteristics of the buffer memory **1440** may be improved. As a consequence, operating characteristics and data storage characteristics of the memory system **1400** may be improved.

Moreover, the buffer memory **1440** according to this implementation may further include an SRAM (static random access memory), a DRAM (dynamic random access memory), and so on, which have a volatile characteristic, and a phase change random access memory (PRAM), a resistive random access memory (RRAM), a spin transfer torque random access memory (STTRAM), a magnetic random access memory (MRAM), and so on, which have a nonvolatile characteristic. Unlike this, the buffer memory **1440** may not include the semiconductor devices according to the implementations, but may include an SRAM (static random access memory), a DRAM (dynamic random access memory), and so on, which have a volatile characteristic, and a phase change random access memory (PRAM), a resistive random access memory (RRAM), a spin transfer torque random access memory (STTRAM), a magnetic random access memory (MRAM), and so on, which have a nonvolatile characteristic.

Features in the above examples of electronic devices or systems in FIGS. **9-13** based on the memory devices disclosed in this document may be implemented in various devices, systems or applications. Some examples include mobile phones or other portable communication devices, tablet computers, notebook or laptop computers, game machines, smart TV sets, TV set top boxes, multimedia servers, digital cameras with or without wireless communication functions, wrist watches or other wearable devices with wireless communication capabilities.

While this patent document contains many specifics, these should not be construed as limitations on the scope of any invention or of what may be claimed, but rather as descriptions of features that may be specific to particular embodiments of particular inventions. Certain features that are described in this patent document in the context of separate embodiments can also be implemented in combination in a single embodiment. Conversely, various features that are described in the context of a single embodiment can also be implemented in multiple embodiments separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

Similarly, while operations are depicted in the drawings in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Moreover, the separation of various system components in the embodiments described in this patent document should not be understood as requiring such separation in all embodiments.

Only a few implementations and examples are described. Other implementations, enhancements and variations can be made based on what is described and illustrated in this patent document.

What is claimed is:

1. A chalcogenide material comprising 1-5 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium.

2. The chalcogenide material of claim **1**, wherein content of germanium is 15-20 at %.

3. The chalcogenide material of claim **1**, content of arsenic is 25-30 at %.

4. The chalcogenide material of claim **1**, wherein content of selenium is 42-47 at %.

5. The chalcogenide material of claim **1**, wherein content of tellurium is 2-8 at %.

6. The chalcogenide material of claim **1**, wherein a sum of content of silicon and content of germanium is 20 at % or more.

7. An electronic device comprising:

a switching element including a chalcogenide material, the chalcogenide material including 1-5 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium;

a first electrode electrically coupled to the switching element; and

a second electrode electrically coupled to the switching element.

8. The electronic device of claim **7**, wherein content of germanium is 15-20 at %.

9. The electronic device of claim **7**, wherein content of arsenic is 25-30 at %.

10. The electronic device of claim **7**, wherein content of selenium is 42-47 at %.

11. The electronic device of claim **7**, wherein content of tellurium is 2-8 at %.

12. The electronic device of claim **7**, wherein a sum of content of silicon and content of germanium is 20 at % or more.

13. An electronic device comprising a semiconductor memory device, the semiconductor memory device including a first memory cell including a first switching element,

wherein the first switching element includes a chalcogenide material including 1-5 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium.

14. The electronic device of claim **13**, wherein the semiconductor memory device further includes:

a second memory cell including a second switching element, the second switching element having a chalcogenide material including 1-10 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium, and

wherein the first memory cell and the second memory cell further include a first memory layer and a second memory layer, respectively, each of the first and second memory layers switching between different resistance states according to a voltage or a current applied thereto.

15. The electronic device of claim **14**, wherein the first switching element and the second switching element control access to the first memory layer and the second memory layer, respectively.

16. The electronic device of claim **13**, wherein the semiconductor memory device includes a plurality of memory cells including the first memory cell,

wherein the semiconductor memory device further includes:

a plurality of first lines disposed between a substrate and the plurality of memory cells, each of the plurality of first lines extending in a first direction; and

a plurality of second lines disposed over the plurality of memory cells, each of the plurality of second lines extending in a second direction that crosses the first direction, and

wherein the plurality of memory cells are disposed at respective intersections of the first lines and the second lines.

17. The electronic device of claim **13**, wherein the semiconductor memory device further includes a capping layer disposed over at least side surfaces of the first memory cell.

18. The electronic device of claim **13**, wherein a sum of content of silicon and content of germanium is 20 at % or more.

19. The electronic device of claim **14**, wherein the chalcogenide material of the second switching element includes 1-5 atomic percent (at %) of silicon, 10-20 at % of germanium, 25-35 at % of arsenic, 40-50 at % of selenium, and 1-10 at % of tellurium.

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