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Malechek

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(54) **CONTROLLING OPERATION OF A VOLTAGE CONVERTER BASED ON TRANSISTOR DRAIN VOLTAGES**

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G05F 1/575	(2006.01)
H02M 3/156	(2006.01)
H02M 3/155	(2006.01)

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CPC ***H02M 3/33546*** (2013.01); ***G05F 1/575*** (2013.01); ***H02M 3/156*** (2013.01); ***H02M 3/33592*** (2013.01); *H02M 2003/1552* (2013.01)

(58) **Field of Classification Search**
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USPC 327/168; 363/17, 21.01, 21.02
See application file for complete search history.

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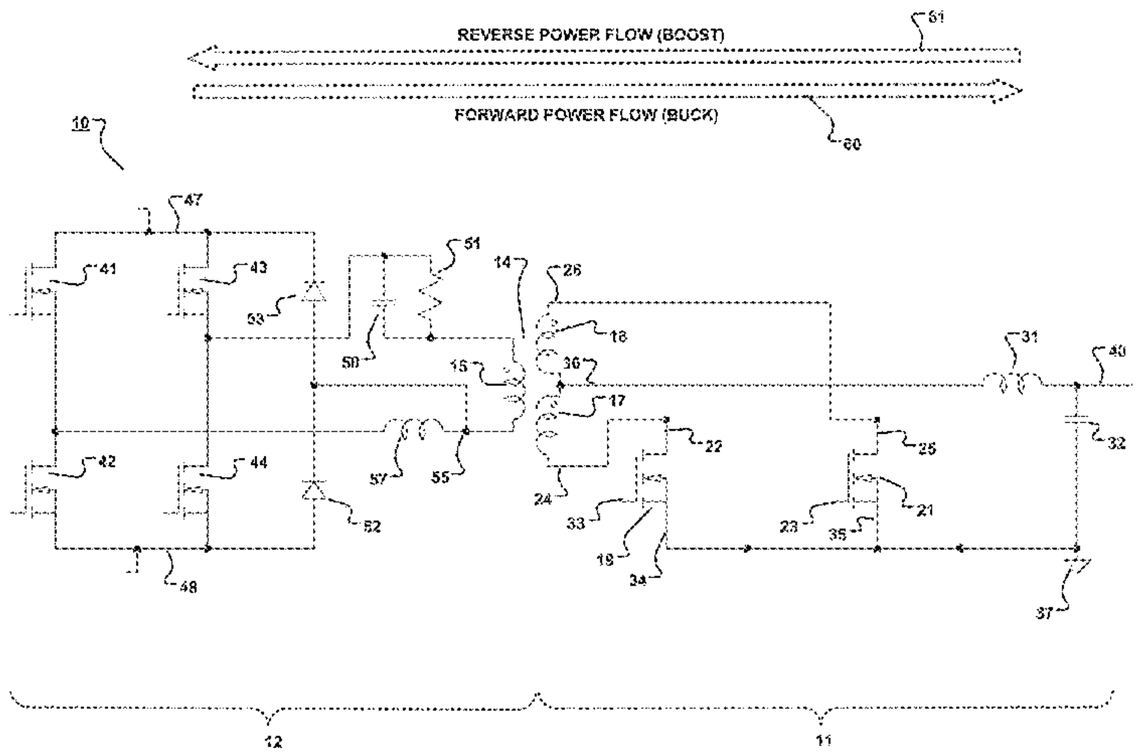
(57) **ABSTRACT**

An example voltage converter includes a transformer having a primary winding, a first secondary winding, and a second secondary winding; a first transistor connected between a first terminal of the first secondary winding and electrical ground, where the first transistor has a first drain; a second transistor connected between a second terminal of the second secondary winding and electrical ground, where the second transistor has a second drain; and a capacitor connectable along a current path to the transformer via at least one of the first transistor or the second transistor. A control system detects a first voltage at the first drain and a second voltage at the second drain, and generates pulse-width modulated control signals based at least on the first and second voltages to control operation of the first and second transistors to produce voltage at the primary winding based on a voltage across the capacitor.

20 Claims, 4 Drawing Sheets



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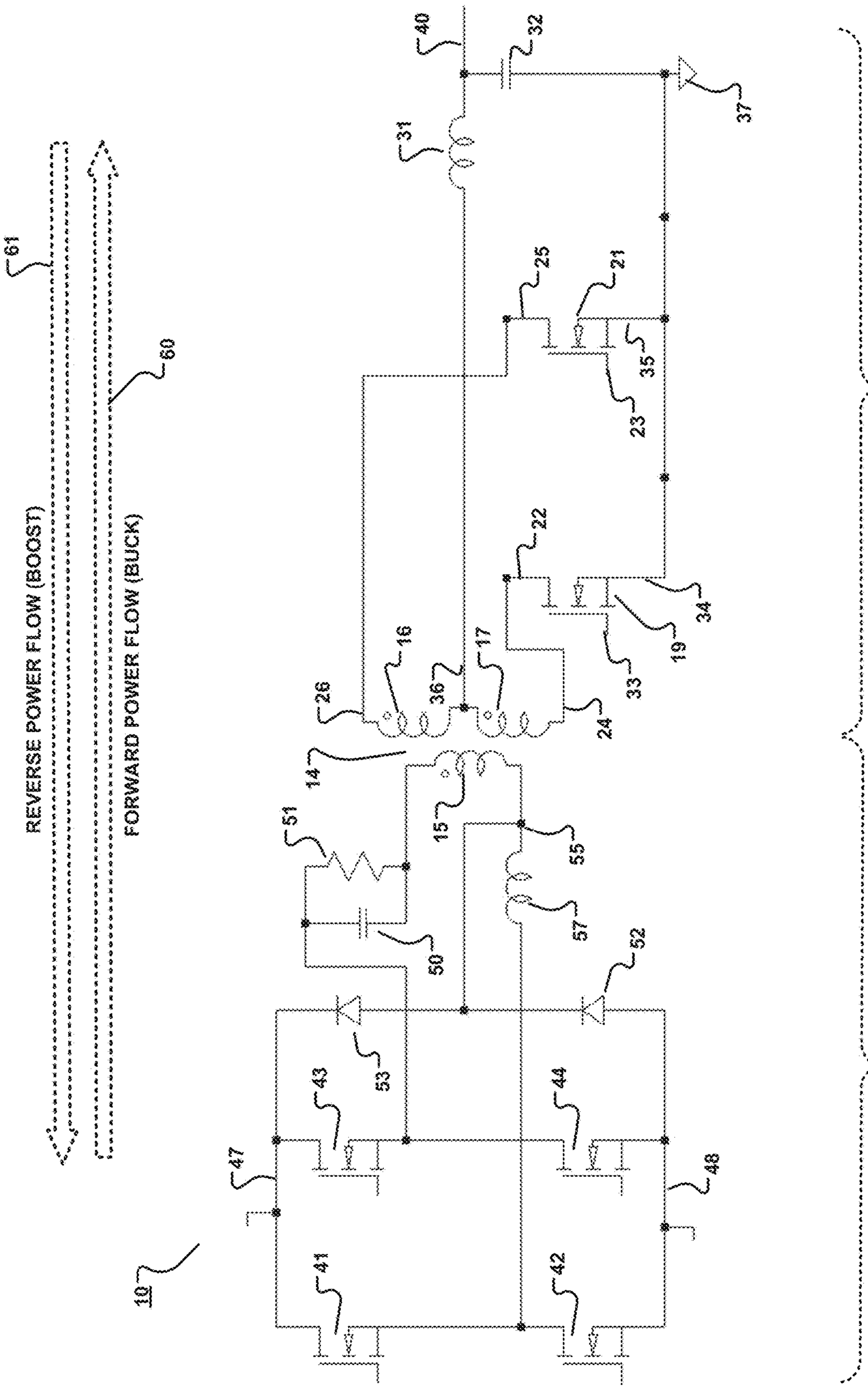
REVERSE POWER FLOW (BOOST)
FORWARD POWER FLOW (BUCK)
61
60
40
32
31
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25
21
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23
22
34
19
33
16
36
17
26
24
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FIG. 1

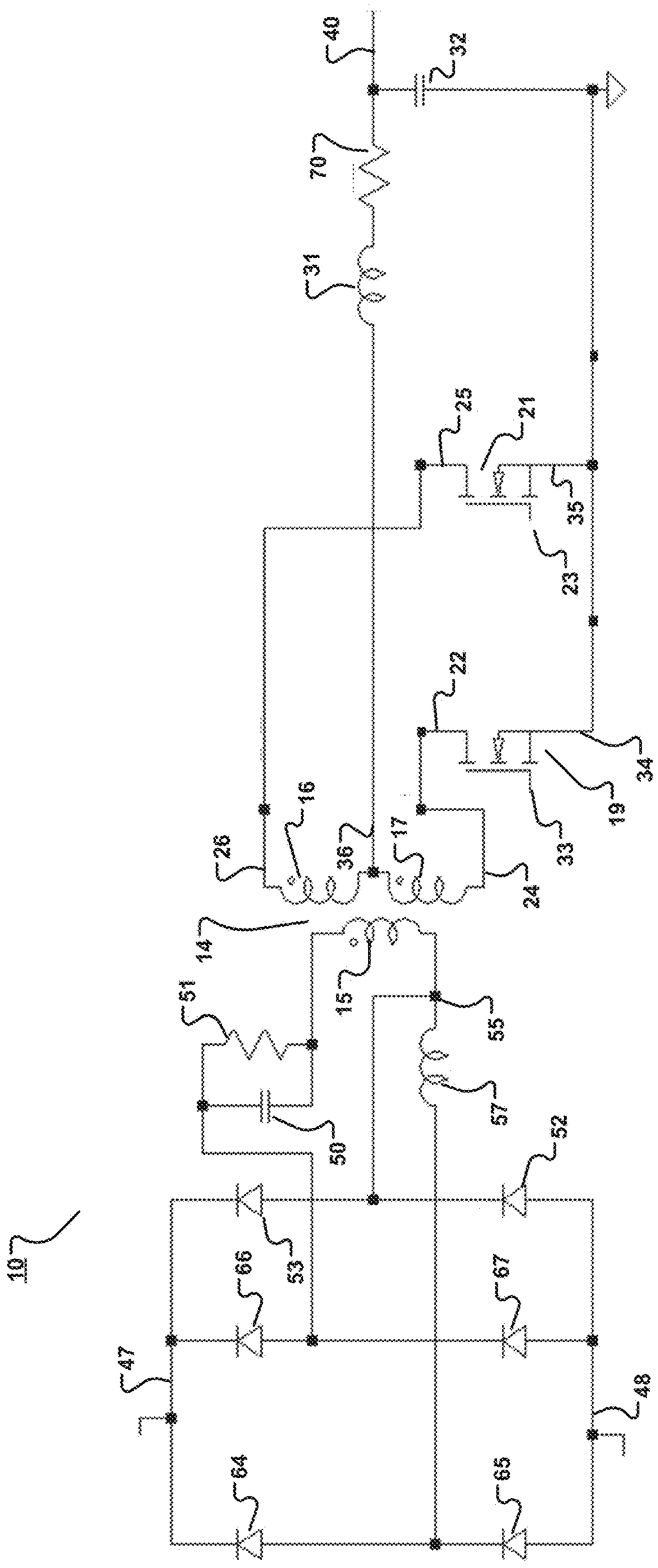
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FIG. 2

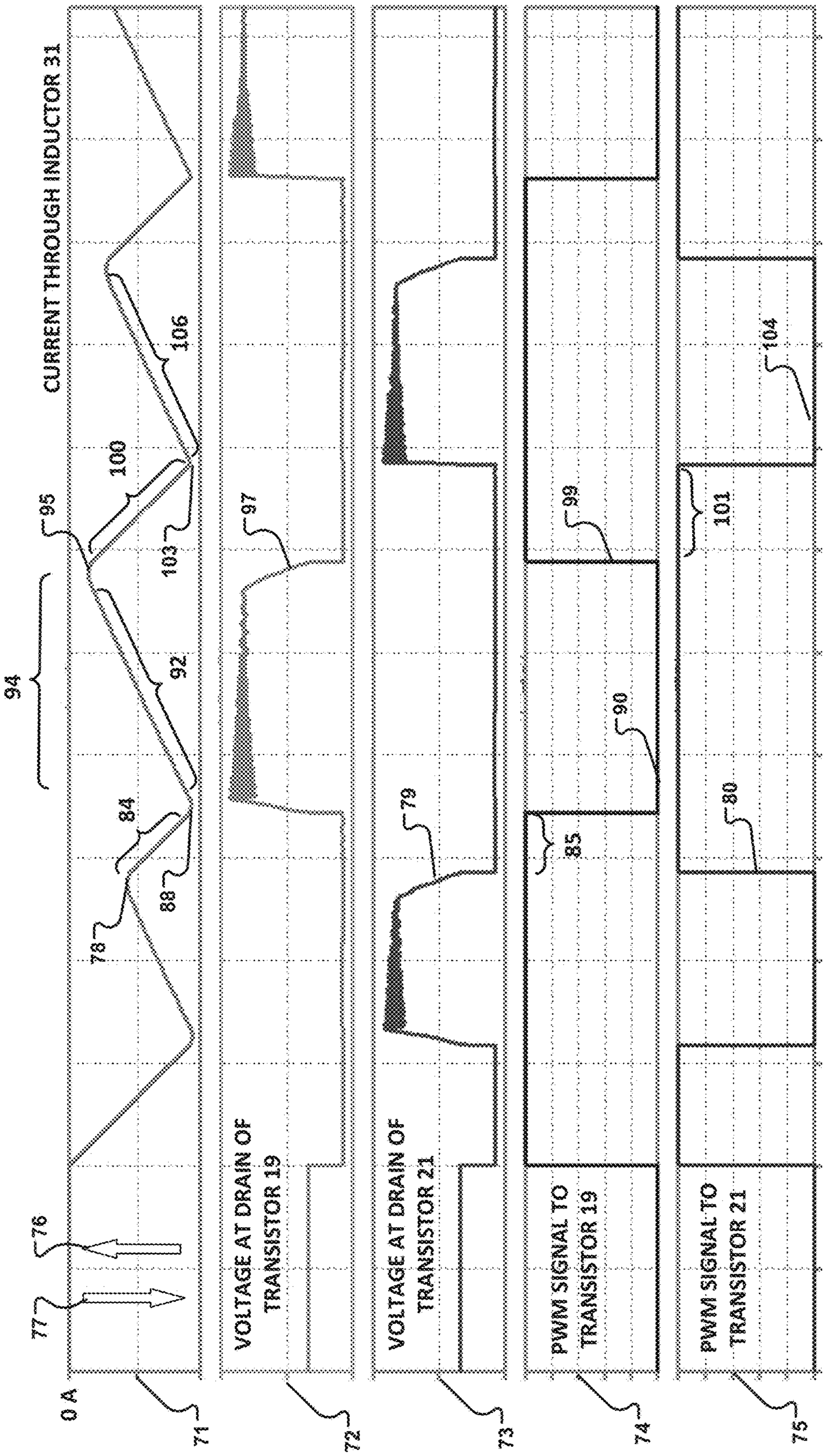
CURRENT THROUGH INDUCTOR 31
94
95
100
103
106
92
84
88
78
97
79
99
90
85
101
104
80
0A
77
76
VOLTAGE AT DRAIN OF TRANSISTOR 19
VOLTAGE AT DRAIN OF TRANSISTOR 21
PWM SIGNAL TO TRANSISTOR 19
PWM SIGNAL TO TRANSISTOR 21
71
72
73
74
75

FIG. 3

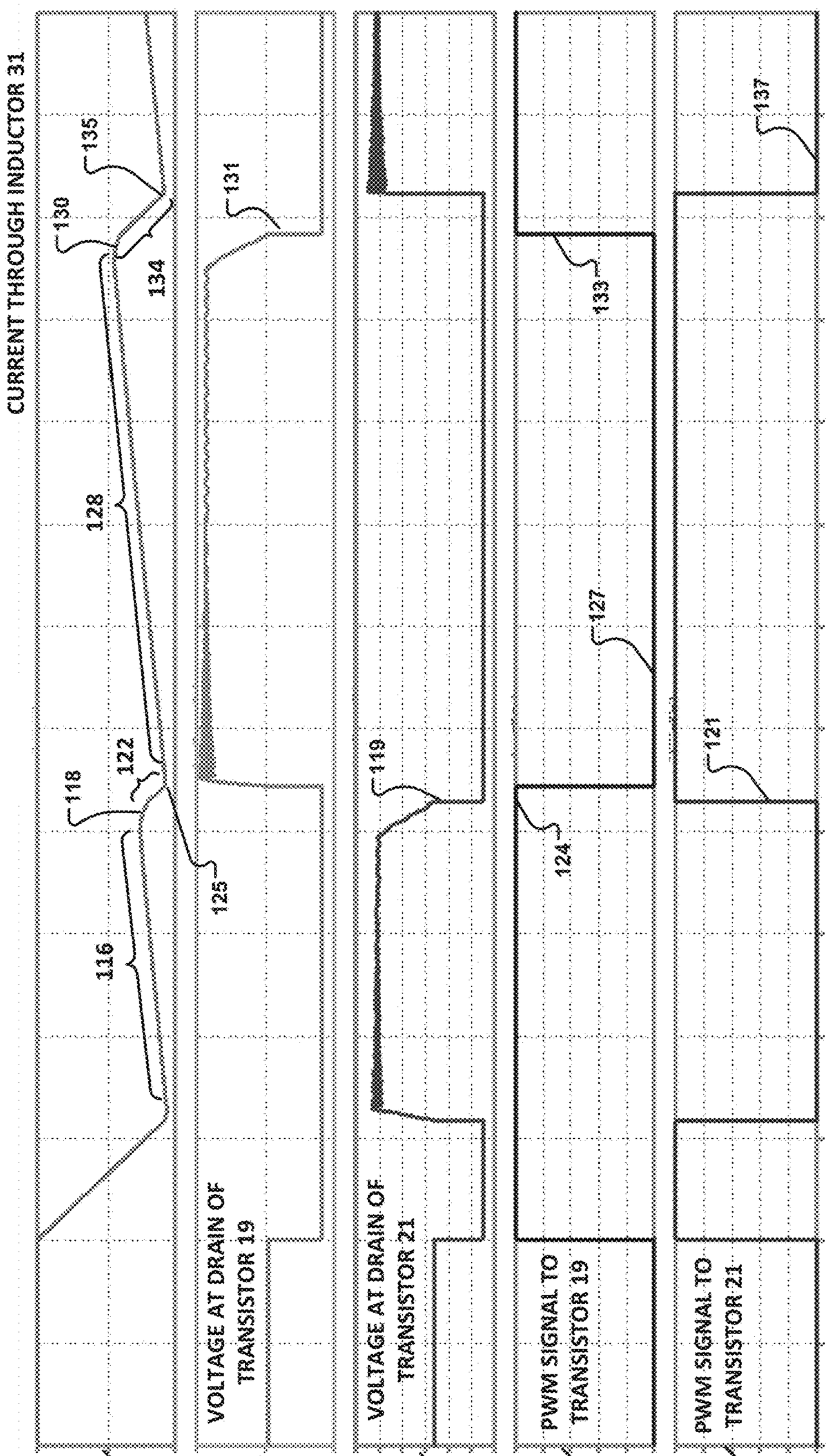
CURRENT THROUGH INDUCTOR 31
130
135
134
131
133
137
128
118
122
125
116
119
124
127
121
VOLTAGE AT DRAIN OF TRANSISTOR 19
VOLTAGE AT DRAIN OF TRANSISTOR 21
PWM SIGNAL TO TRANSISTOR 19
PWM SIGNAL TO TRANSISTOR 21
110
111
112
113
114

FIG. 4

CONTROLLING OPERATION OF A VOLTAGE CONVERTER BASED ON TRANSISTOR DRAIN VOLTAGES

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

This invention was made with government support under government contract N00019-16-C-0002 awarded by the US Naval Air Systems Command. The government has certain rights in the invention.

TECHNICAL FIELD

This specification describes examples of step-down converters that are controllable to operate as step-up converters.

BACKGROUND

A voltage converter changes the magnitude of a voltage from its input to its output. A step-down converter is a type of voltage converter that reduces the magnitude of a voltage from its input to its output. An example of a step-down converter is a buck converter. A step-up converter is a type of voltage converter that increases the magnitude of a voltage from its input to its output. An example of a step-up converter is a boost converter.

SUMMARY

An example voltage converter includes a transformer having a primary winding, a first secondary winding, and a second secondary winding; a first transistor connected between a first terminal of the first secondary winding and electrical ground, where the first transistor includes a first drain; a second transistor connected between a second terminal of the second secondary winding and electrical ground, where the second transistor includes a second drain; and a capacitor that is connectable along a current path to the transformer via at least one of the first transistor or the second transistor. A control system is configured to detect a first voltage at the first drain and a second voltage at the second drain, and also to generate pulse-width modulated control signals based at least on the first voltage and the second voltage. The pulse-width modulated control signals are for controlling operation of the first transistor and the second transistor to produce voltage at the primary winding based on a voltage across the capacitor. The voltage converter may include one or more of the following features, either alone or in combination.

The voltage converter may include an output terminal to connect to a load. The voltage converter may include an inductor connected in series with the capacitor and the output terminal and connected at a center tap of the transformer between the first secondary winding and the second secondary winding. The pulse-width modulated control signals may be based also on current through the inductor to the transformer. The pulse-width modulated control signals may control operation of the first transistor and the second transistor to enable discharge of the capacitor via the inductor.

The first transistor may include a first gate and the second transistor may include a second gate. The control system may be configured to apply the pulse-width modulated control signals to the first gate and to the second gate. Detecting the first voltage may include detecting when the first voltage decreases. The control system may be configured to generate a first pulse-width modulated control signal to apply to the first gate in response to the first voltage decreasing. The first pulse-width modulated control signal may have a pulse width that is based also on the current through the inductor. Detecting the second voltage may include identifying when the second voltage decreases. The control system may be configured to generate a second pulse-width modulated control signal to apply to the second gate in response to the second voltage decreasing. The second pulse-width modulated control signal may have a pulse width that is based also on the current through the inductor. A time when the first voltage decreases may correspond to a minimum current through the transformer. The minimum current through the transformer may correspond to current circulation on a primary voltage side or the primary winding the transformer.

The voltage converter may include input transistors connected electrically to the primary winding. The control system may be configured to apply control signals to gates of the input transistors to cause the input transistor to operate as diodes. The voltage converter may possibly include clamping diodes connected between voltages rails on a primary winding side of the transformer. The clamping diodes may be configured to reduce voltage ringing on a secondary voltage side of the transformer.

The control system may include comparators to compare the first voltage and the second voltage to reference voltages. The voltage converter may possibly include an inductor connected in series with the primary winding. The inductor may provide storage for a phase-shifted full bridge to operate in a zero voltage switched (ZVS) mode of operation.

The voltage converter may be a buck converter. Controlling operation of the first transistor and the second transistor to produce voltage at the primary winding based on a voltage across the capacitor may include controlling the buck converter to operate as a boost converter. The primary winding may be configured to support a higher voltage than a combined voltage of the first secondary winding and the second secondary winding multiplied by a turns ratio of the transformer.

The voltage converter may include an output terminal to connect to a load; an inductor connected in series with the capacitor and the output terminal and connected at a center tap of the transformer between the first secondary winding and the second secondary winding; and circuitry to detect current through the inductor to the transformer. Each pulse-width modulated control signal may have a rising edge that corresponds to a decrease in the first voltage or the second voltage and has a falling edge that corresponds to a predefined current through the inductor.

An example method of controlling a voltage converter may include detecting a first voltage at a first drain of a first transistor that is connected between a first secondary winding of a transformer and electrical ground; detecting a second voltage at a second drain of a second transistor that is connected between a second secondary winding of the transformer and electrical ground; detecting a current through an inductor connected at a center tap between the first secondary winding and the second secondary winding, where the inductor is connected in series with a capacitor that is connected to electrical ground; generating pulse-width modulated control signals based on the first voltage, the second voltage, and the current through the inductor; and controlling operation of the first transistor and the second transistor based on the pulse-width modulated control signals to cause the capacitor to discharge current through the inductor towards the transformer and thereby produce a

voltage at a primary winding of the transformer. The method may include one or more of the following features, either alone or in combination.

Each pulse-width modulated control signal may have a rising edge that corresponds to a decrease in the first voltage or the second voltage and may have a falling edge that corresponds to the current through the inductor. The current through the inductor may include a predefined maximum current through the inductor, where the predefined maximum current is based at least in part on the transformer. The voltage converter may be a step-down converter. Controlling operation of the first transistor and the second transistor based on the pulse-width modulated control signals to cause the capacitor to discharge current through the inductor and thereby produce a voltage at a primary winding of the transformer may include controlling the step-down converter to operate as a step-up converter. Operation of the first transistor and the second transistor may be controlled until the capacitor discharges in whole or in part.

Any two or more of the features described in this specification, including in this summary section, may be combined to form implementations not specifically described in this specification.

At least part of the circuitry and processes described in this specification may be configured or controlled by executing, on one or more processing devices, instructions that are stored on one or more non-transitory machine-readable storage media. Examples of non-transitory machine-readable storage media include read-only memory, an optical disk drive, memory disk drive, and random access memory. At least part of the circuitry and processes described in this specification may be configured or controlled using a computing system comprised of one or more processing devices and memory storing instructions that are executable by the one or more processing devices to perform various control operations.

The details of one or more implementations are set forth in the accompanying drawings and the following description. Other features and advantages will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF THE DRAWINGS

FIG. **1** is a circuit diagram of an example voltage converter.

FIG. **2** is a circuit diagram of the example voltage converter configured to operate in a step-up, or boost, mode.

FIG. **3** shows example timing diagrams that illustrate operation of the example voltage converter in step-up, or boost, mode.

FIG. **4** shows another example of timing diagrams that illustrate operation of the example voltage converter in step-up, or boost, mode.

Like reference numerals in different figures indicate like elements.

DETAILED DESCRIPTION

Described herein are example implementations of a step-down voltage converter that is not designed to operate as a step-up converter, but that is controllable to operate as a step-up voltage converter. In an example, the step-down voltage converter is a buck converter having a phase-shifted full bridge (PSFB) topology. The buck converter is a direct current (DC) to DC voltage converter that uses synchronous rectification to perform the switching required to produce the voltage provided at its output to a load. To implement this switching, the buck converter includes transistor-based switches. These switches are controllable to direct current through an inductor connected in series with an output terminal and one or more capacitors, which are referred to herein as a capacitor bank, connected in parallel with the output terminal. The capacitor bank is arranged as it is, and sized, to reduce voltage transients at the output.

When the buck converter is shut-down, the capacitor bank may be discharged. However, in some cases, the size of the capacitor bank is such that it can take on the order of minutes to discharge to a zero voltage. In addition, in some cases, due to this discharge duration, the voltage in the system can remain at a non-zero value for too long resulting in damage to the converter. To decrease the time it takes to discharge the capacitor bank, the buck converter may be controlled to operate as a boost converter. That is, the buck converter may be operated to generate a voltage output in a reverse direction using the voltage across the capacitor bank. The resulting voltage output is generated using the charge stored in the capacitor bank and, during output, the capacitor bank is continually depleted until the capacitor bank is discharged. This active discharge of the capacitor bank can reduce the time it takes for the capacitor bank to discharge. For example, the time it takes for the voltage across the capacitor bank to reach zero volts can be reduced.

In some implementations, a control system is configured—for example, programmed—to generate pulse-width modulated (PWM) control signals to control operation of the transistor-based switches to operate the buck converter as a boost converter and thereby discharge its capacitor bank. The control signals may be generated based on drain voltages produced at the transistor-based switches and based on a current through the inductor. For example, the current through the inductor may be monitored to generate part of the PWM control signals that produce a controlled and rapid discharge of the capacitor bank. The drain voltages on the transistor-based switches may be monitored to generate another part of the PWM control signals that produce the controlled and rapid discharge of the capacitor bank. For example, as explained below, each PWM control signal may include a rising edge that corresponds to a decrease in drain voltage on a transistor-based switch and may include a falling edge that corresponds to maximum negative current through the inductor.

FIG. **1** shows an example implementation of a buck converter **10** having a PSFB topology that may be controlled to operate as a boost converter. Converter **10** includes a low voltage side **11** and a high voltage side **12**. The low voltage side is so named because it receives and/or outputs a low voltage and the high voltage side is so named because it receives and/or outputs a high voltage. "High" and "low" have no specific numerical connotations, but rather are meant only to indicate that the voltage on the high voltage side is greater than the voltage on the low voltage side. In some examples, the high voltage side is referred to as the primary side and the low voltage side is referred to as the secondary side.

A transformer **14** operates as the electrical interface between the low voltage side **11** and the high voltage side **12**. In this example, transformer **14** includes a primary winding **15** and two secondary windings **16** and **17**. Converter **10** also include transistors **19** and **21**. In this example, the transistors are power metal oxide field-effect (MOSFET) transistors, which are controllable to operate as synchronous rectification switches to control the operation of converter **10**. As shown, drain **22** of transistor **19** is connected to terminal **24**

of secondary winding **17** and drain **25** of transistor **21** is connected to terminal **26** of secondary winding **16**.

As shown, inductor **31** is connected to the center tap of transformer **14** between secondary windings **16** and **17**. As also shown, inductor **31** is connected in series with capacitor bank **32** and the output terminal **40** of converter **10**. A load (not shown)—for example, a device to be driven by the voltage output of the buck converter—may be connected to the output terminal. Depending on how the transistors are switched, a square wave voltage is generated and applied through inductor **31**. Capacitor bank **32** is connected in parallel between the load and electrical ground **37**. Inductor **31**, in combination with capacitor bank **32**, filters that square wave voltage to limit ripple in the voltage provided to the load. Sources **34** and **35** of respective transistors **19** and **21** are also connected to electrical ground in this example.

During normal operation—for example, to step-down an input voltage—PWM control signals are applied to the gates of transistors **19** and **21** (and also to transistors **41**, **42**, **43**, and **44** discussed below) to charge the capacitor bank to produce a stepped-down output voltage. In this example, a high voltage input is provided to primary winding **15** and is stepped-down to produce a lower voltage at secondary windings **16** and **17**. When a PWM control signal is applied to the gate of transistor **19**, transistor **19** conducts. During at least part of the time that transistor **19** is conducting, no control signal (e.g., zero volts) is applied to transistor **21**. As a result, transistor **21** does not conduct during this time. While transistor **19** is conducting, current from terminal **36** (the center tap) of secondary winding **17** flows toward output terminal **40** to charge inductor **31** and capacitor bank **32**, thereby generating the output voltage across capacitor bank **32**. At some time during operation, a PWM signal is applied to the gate of transistor **21**, thereby causing transistor **21** to conduct. During at least part of the time that transistor **21** is conducting, no control signal is applied to transistor **19**. As a result, transistor **19** does not conduct during this time. During this period of time, the current through inductor **31** discharges to maintain the voltage across the load. This cycle repeats to maintain the stepped-down voltage across the load.

The high voltage side **12** of converter **10** includes transistors **41**, **42**, **43**, and **44**, Transistors **41**, **42**, **43**, and **44** form the PSFB, which is configured and controllable to switch a DC input voltage at voltage rails **47** and **48** to produce an alternating DC voltage or square wave DC voltage at primary winding **15** of transformer **14**. Capacitor **50** is a blocking capacitor that is used to ensure that transformer **14** does not become unbalanced. For example, when the voltages on either side of transformer **14** are reversed, excessive flux can develop in one direction that may cause the transformer to saturate and not operate normally. Capacitor **50** limits the passage of unbalanced DC current to the transformer and prevents or reduces saturation of the transformer. Resistor **51** is sized to ensure that capacitor **50** balances and discharges within an acceptable timeframe.

The high voltage side also includes clamp diodes **52**, **53**. In some implementations, clamp diodes **52**, **53** are not included, Clamp diodes **52** and **53** clamp the high-frequency ringing voltage at node **55** between primary winding **15** (a leakage inductance of transformer **14**), the capacitance of transistors **19** and **21** on the low voltage side, and the resonant inductor **57** to the input voltage rails **47** and **48**. This reduces the current through the transformer windings and resonant inductor **57**, which may alleviate or prevent voltage ringing on the low voltage side of the transformer on the drains of transistors **19** and **21**. Resonant inductor **57** provides energy storage for the PSFB to operate in a zero voltage switched (ZVS) mode of operation.

As explained previously, converter **10** is controllable to operate in a boost mode—for example, to discharge capacitor bank **32** through transformer **14**. As shown in FIG. **1**, during forward (buck) operation, power flows in the direction of arrow **60**, whereas in boost mode, power flows in the direction of arrow **61**. Accordingly, when converter **10** is operated in boost mode, the charge stored in capacitor bank **32** is used to produce a voltage output at the primary winding **15** of transformer **14**.

During the boost mode of operation, there may be no control inputs to the gates of transistors **41**, **42**, **43**, and **44** that form the PSFB; for example, zero volts may be applied to the gates of these transistors. In this regard, as noted, in some implementations, transistors **41**, **42**, **43**, and **44** include MOSFETs. When zero volts is applied to their gates, the MOSFETs operate as diodes due to their internal body diodes. Accordingly, during boost mode, converter **10** may be modeled as shown in FIG. **2**. That is, transistors **41**, **42**, **43**, and **44** are modeled as respective diodes **64**, **65**, **66**, and **67**. The remaining features of FIG. **2** are the same as those of FIG. **1**, except that an additional resistor **70** may be added to measure inductor current.

To operate converter **10** in boost mode, transistors **19** and **21** are controlled by applying PWM signals to their respective gates. Transistors **19** and **21** are controlled to connect the capacitor bank along a current path to the transformer that runs through at least one of the transistors to enable the capacitor bank to discharge through the transformer. The PWM signals are generated based, at least in part, on current from the low voltage side **11** to the high voltage side **12**. For example, the PWM signals are generated to regulate that current so that the current does not exceed the current limit of the converter and thereby cause damage to the buck converter circuitry. In this regard, an example of a traditional operation of synchronous rectification transistors in a voltage converter includes applying, to the gates of the synchronous rectification transistors, signals that have the same period and that are out-of-phase. When operating converter **10** in boost mode, this would cause transistors **19** and **21** to conduct for equal but different time periods, with no overlap in conduction. This operation of transistors **19** and **21** could cause the current flow from the low voltage side to the high voltage side to become increasingly negative until the current exceeds the current limit of the converter. In boost mode, the systems and processes described herein detect the current flowing from the low voltage side **11** to the high voltage side **12** and control transistors **19** and **21** to regulate that current flow. In boost mode, the systems and processes described herein also detect the drain voltage to sense the path of the current flow on the primary winding and control transistors **19** and **21** to regulate the current flow based on that information.

FIG. **3** includes timing diagrams **71**, **72**, **73**, **74**, and **75** that illustrate an example operation of converter **10** in boost mode. In each timing diagram, the X-axis includes time and the Y-axis includes current or voltage as indicated below. Timing diagram **71** shows the current through inductor **31**. The current is depicted as negative (less than zero amperes ("0 A" in the figure)), since the current is flowing in the direction of arrow **61** in FIG. **1**. That is, negative current is designated as current flowing away from the capacitor bank or load and towards transformer **14**, whereas positive current is designated as current flowing away from transformer **14** and towards the capacitor bank or load. For the purposes of the following explanation, since the current through inductor

31 is considered negative, current changing in the direction of arrow 76 is referred to as decreasing (that is, less negative current) and current changing the direction of arrow 77 is referred to as increasing (that is, more negative current).

Timing diagram 72 shows the voltage on the drain 22 of transistor 19, and timing diagram 73 shows the voltage on the drain 25 of transistor 21. Timing diagram 74 shows the PWM control signal applied to the gate of transistor 19; and timing diagram 75 shows the PWM control signal applied to the gate of transistor 21. As depicted in timing diagrams 71, 72, and 73, in each instance, a positive peak in the negative current through inductor 31 coincides with a change in voltage at the drain of the synchronous rectification transistor that is not conducting. In this regard, a positive peak 78 indicates a change in slope—that is, a decrease followed by an increase—in current through inductor 31. Also, by way of example, as shown in timing diagram 73, positive peak 78 coincides with a decrease in voltage 79 at the drain of non-conducting transistor 21.

At approximately the positive peak, the current through the inductor approaches or reaches zero. Accordingly, each positive peak represents a local minimum current through the inductor. The minimum is characterized as local because it may fluctuate from cycle-to-cycle. Also at approximately the positive peak, the current begins to circulate internally within the high voltage side of the transformer or on the primary winding of the transformer and is not transferred out to the input at nodes 47 and 48. That current, if unchecked, can cause damage to the converter. Accordingly, when a decrease in voltage 79 is detected at the drain of non-conducting transistor 21, transistor 21 is driven to conduction by applying a non-zero voltage 80 to its gate 23. This produces a controlled increase 84 in current through inductor 31. As noted, the drain voltages on the synchronous rectification transistors provide information about how current is transferring on the primary side of the transformer. Accordingly, use of the drain voltages on the synchronous rectification transistors enables control over the converter based on the current in the primary winding and how power flows into the input at 47 and 48 without directly measuring that current. As explained above, that control causes a synchronous rectification transistor to switch once the current stops flowing out of the converter into the input.

As shown in timing diagram 74, transistor 19 remains conductive temporarily 85 while transistor 21 is driven to conduction. In this regard, use of a center-tapped secondary winding may require that transistors 19 and 21 always have some temporary conduction overlap in order to keep secondary voltage spikes down. For example, as shown in timing diagrams 74 and 75, there is always a temporary overlap, such as overlap 85, in operation between transistors 19 and 21. In the configuration of FIGS. 1 and 2, if both of transistors 19 and 21 are non-conductive at the same time, all of the energy from the transformer may instantly transfer to those transistors as a high voltage spike. This could damage the transistors. The temporary overlap in conduction between transistors 19 and 21 may reduce the chances that this type of damage will occur.

At some time following conduction of transistor 21, a maximum negative current through the transformer is detected. This maximum negative current is represented by negative peak 88 in timing diagram 71. The maximum negative current may have a predefined magnitude that is based on operational characteristics of the transformer and other circuitry used to implement the buck converter. Exceeding the maximum negative current could result in damage to the circuitry. Accordingly, at that time, transistor 19, which is already conducting as shown in timing diagram 74, is made non-conductive by applying a zero voltage 90 to its gate 33. This produces a controlled decrease 92 in current through the inductor, as shown in timing diagram 71. In this regard, by using current through inductor 31 to start a switching cycle 94 and a transistor drain voltage to end the switching cycle, the system may be able automatically to adjust for variations in input and output voltage, temperature, and component value variations.

The controlled decrease 92 in current continues until another positive peak 95 occurs. At this time, the voltage 97 on the drain 22 of transistor 19 decreases, as shown in timing diagram 72. In response, transistor 19—the previously non-conductive transistor—is driven to conduction by applying a non-zero voltage 99 to its gate 33. This produces a controlled increase 100 in current through inductor 31. As shown in timing diagram 75, transistor 21 remains temporarily conductive 101 while transistor 19 is driven to conduction. At some time following conduction of transistor 19, a maximum negative current through the inductor is detected. This maximum negative current is represented by negative peak 103 in timing diagram 71. Accordingly, at that time, transistor 21, which is already conducting as shown in timing diagram 75, is made non-conductive by applying a zero voltage 104 to its gate 23. This produces a controlled decrease 106 in current through the inductor, as shown in timing diagram 71.

The foregoing process repeats to provide controlled current flow from the low voltage side of the buck converter to the high voltage side of the buck converter. In the examples described herein, the foregoing process repeats until the capacitor bank is discharged to zero volts or substantially zero volts.

The example circuitry of FIGS. 1 and 2 also includes components (not shown) to detect voltages on the drains of transistors 19 and 21 and negative peaks of the inductor current. For example, the circuitry may include multiple analog comparators. One or more comparators may be used to detect voltages on the drains of transistors 19 and 21. For example, a first comparator may be used to detect the voltage on the drain 22 of transistor 19 and a second, different comparator may be used to detect the voltage on the drain 25 of transistor 21. For example, a single comparator may be used to detect the voltage on the drain 22 of transistor 19 and to detect the voltage on the drain 25 of transistor 21, In this example, detection of drain voltage on a single transistor, such as transistor 19, is performed every other clock cycle.

In some implementations, components to detect the negative peak of the inductor current include one or more of the analog comparators. For example, an analog comparator compares the inductor current to a predefined threshold. When that threshold is reached, the maximum negative current is detected. Resistor 70 may also be included to detect the current through inductor 31.

The detected drain voltages and the time at which the maximum negative current (the negative peak) is detected may be digitized and transmitted to the control system. The control system uses the resulting data to control the gates of transistors 19 and 21 in the manner described with respect to timing diagrams 74 and 75.

FIG. 4 includes timing diagrams 110, 111, 112, 113, and 114 that illustrate another example operation of converter 10 in boost mode. Comparing FIG. 4 to FIG. 3, it is evident that the decreasing inductor current—for example, decreases 92 and 116—occurs at a lower rate in FIG. 4 than in FIG. 3. This is due to characteristics of the transformer and con-

verter operating point such as input and output voltage at an instant in time. In the example of FIG. **3**, the turns ratio of the transformer can support an input voltage that is greater than the voltage that can be generated by the low voltage side of the converter. In the example of FIG. **4**, the turns ratio of the transformer can support an input voltage that is greater than the voltage that can be generated by the low voltage side of the converter, but not as great as the voltage that can be supported by the transformer turns ratio in the example of FIG. **3**. In this regard, if the primary winding cannot support the voltage generated by on the low voltage side, then the converter may not be operable as a boost converter or may be operable as a boost converter over a limited input and output voltage range only. Accordingly, to operate in boost mode, the transformer turns ratio is configured to support a higher voltage than a combined voltage of the first secondary winding and the second secondary winding taking into account a turns ratio of the transformer. For example, a transformer having appropriate numbers of windings and ratios may be selected. For example, the primary winding may be configured to support a higher voltage than a combined voltage of the first secondary winding and the second secondary winding multiplied by a turns ratio of the transformer.

Notwithstanding the foregoing differences, as explained below, the basic operation depicted in FIG. **4** is the same as the basic operation depicted in FIG. **3**. As was the case previously, in FIG. **4**, timing diagram **110** shows the current through inductor **31** of FIGS. **1** and **2**. As above, the current is depicted as negative, since it is flowing in the direction of arrow **61** in FIG. **1**.

Timing diagram **111** shows the voltage on the drain **22** of transistor **19**, and timing diagram **112** shows the voltage on the drain **25** of transistor **21**. Timing diagram **113** shows the PWM control signal applied to the gate of transistor **19**; and timing diagram **14** shows the PWM control signal applied to the gate of transistor **21**. As was the case above, a positive peak in the negative current through inductor **31** coincides with a change in voltage at the drain of the synchronous rectification transistor that is not conducting. For example, positive peak **118** coincides with a decrease in voltage **119** at drain **25** of transistor **21**, as shown in timing diagram **112**. At approximately the positive peak, current stops flowing out of the input and begins to recirculate in the primary side which, if unchecked, can cause damage to the converter. Accordingly, transistor **21** is driven to conduction by applying a non-zero voltage **121** to its gate **23**. This produces a controlled increase **122** in current through inductor **31**. As shown in timing diagram **113**, transistor **19** remains conductive for a time **124** while transistor **21** is driven to conduction.

At some time following conduction of transistor **21**, a maximum negative current through the transformer occurs. This maximum negative current is represented by negative peak **125** in timing diagram **110**. Accordingly, at that time, transistor **19**, which is already conducting as shown in timing diagram **113**, is made non-conductive by applying a zero voltage **127** to its gate **33**. This produces a controlled decrease **128** in current through the inductor, as shown in timing diagram **110**.

The controlled decrease **128** continues until positive peak **130** is detected. At this time, the voltage **131** on the drain **22** of transformer **19** decreases, as shown in timing diagram **111**. In response, transistor **19**—the previously non-conductive transistor—is driven to conduction by applying a non-zero voltage **133** to its gate **33**. This produces a controlled increase **134** in current through inductor **31**. As shown in timing diagram **114**, transistor **21** remains conductive while transistor **19** is driven to conduction. At some time following conduction of transistor **19**, a maximum negative current through the transformer is detected. This maximum negative current is represented by negative peak **135** in timing diagram **110**. Accordingly, at that time, transistor **21** which is already conducting as shown in timing diagram **113**, is made non-conductive by applying a zero voltage **137** to its gate **23**. This produces a controlled decrease in current through the inductor, as shown in timing diagram **110**.

The foregoing process repeats to provide controlled current from the low voltage side of the converter to the high voltage side of the converter. In the examples described herein, the foregoing process repeats until the capacitor bank is discharged to zero volts or substantially zero volts.

The example systems and processes described herein may be used in any appropriate electronic system. For example, the systems and processes may be used in DC/DC converters within radar systems, antenna systems, or radar and antenna systems. For example, the systems and processes may be used in power supply systems in any appropriate technological context.

All or part of the systems and processes described in this specification and their various modifications may be configured or controlled at least in part by a control system that includes one or more computers executing one or more computer programs tangibly embodied in one or more information carriers, such as in one or more non-transitory machine-readable storage media. For example, the PWM signals may be generated by one or more computers using one or more computer programs based on voltages detected on the synchronous rectification transistors' drains and the maximum negative current detected in the inductor. A computer program can be written in any form of programming language, including compiled or interpreted languages, and it can be deployed in any form, including as a stand-alone program or as a module, part, subroutine, or other unit suitable for use in a computing environment. A computer program can be deployed to be executed on one computer or on multiple computers at one site or distributed across multiple sites and interconnected by a network.

Actions associated with configuring or controlling the systems and processes can be performed by one or more programmable processors executing one or more computer programs to control all or some of the well formation operations described previously. All or part of the systems and processes can be configured or controlled by special purpose logic circuitry, such as, an FPGA (field programmable gate array) and/or an ASIC (application-specific integrated circuit).

Processors suitable for the execution of a computer program include, by way of example, both general and special purpose microprocessors, and any one or more processors of any kind of digital computer. Generally, a processor will receive instructions and data from a read-only storage area or a random access storage area or both. Elements of a computer include one or more processors for executing instructions and one or more storage area devices for storing instructions and data. Generally, a computer will also include, or be operatively coupled to receive data from, or transfer data to, or both, one or more machine-readable storage media, such as mass storage devices for storing data, such as magnetic, magneto-optical disks, or optical disks. Non-transitory machine-readable storage media suitable for embodying computer program instructions and data include all forms of non-volatile storage area, including by way of example, semiconductor storage area devices, such as

EPROM (erasable programmable read-only memory), EEPROM (electrically erasable programmable read-only memory), and flash storage area devices; magnetic disks, such as internal hard disks or removable disks; magneto-optical disks; and CD-ROM (compact disc read-only memory) and DVD-ROM (digital versatile disc read-only memory).

Elements of different implementations described may be combined to form other implementations not specifically set forth previously, Elements may be left out of the systems described previously without adversely affecting their operation or the operation of the system in general. Furthermore, various separate elements may be combined into one or more individual elements to perform the functions described in this specification.

Other implementations not specifically described in this specification are also within the scope of the following claims.

What is claimed is:

1. A voltage converter comprising:

a transformer comprising a primary winding, a first secondary winding, and a second secondary winding;

a first transistor connected between a first terminal of the first secondary winding and electrical ground, the first transistor comprising a first drain;

a second transistor connected between a second terminal of the second secondary winding and electrical ground, the second transistor comprising a second drain;

a capacitor that is connectable along a current path to the transformer via at least one of the first transistor or the second transistor;

an inductor connected in series with the capacitor and connected at a center tap of the transformer between the first secondary winding and the second secondary winding; and

a control system to detect a first voltage at the first drain, a second voltage at the second drain, and a current through the inductor, and to generate pulse-width modulated control signals based at least on the first voltage, the second voltage, and the current through the inductor, the pulse-width modulated control signals to control operation of the first transistor and the second transistor to produce voltage at the primary winding based on a voltage across the capacitor.

2. The voltage converter of claim **1**, further comprising:

an output terminal to connect to a load.

3. The voltage converter of claim **2**, wherein the pulse-width modulated control signals control operation of the first transistor and the second transistor to enable discharge of the capacitor via the inductor.

4. The voltage converter of claim **2**, wherein the first transistor comprises a first gate and the second transistor comprises a second gate; and

wherein the control system is configured to apply the pulse-width modulated control signals to the first gate and to the second gate.

5. The voltage converter of claim **4**, wherein detecting the first voltage comprises detecting when the first voltage decreases; and

wherein the control system is configured to generate a first pulse-width modulated control signal to apply to the first gate in response to the first voltage decreasing, the first pulse-width modulated control signal having a pulse width that is based also on the current through the inductor.

6. The voltage converter of claim **5**, wherein detecting the second voltage comprises identifying when the second voltage decreases; and

wherein the control system is configured to generate a second pulse-width modulated control signal to apply to the second gate in response to the second voltage decreasing, the second pulse-width modulated control signal having a pulse width that is based also on the current through the inductor.

7. The voltage converter of claim **5**, wherein a time when the first voltage decreases corresponds to a minimum current through the transformer.

8. The voltage converter of claim **7**, wherein the minimum current through the transformer corresponds to current circulation on a primary voltage side or the primary winding the transformer.

9. The voltage converter of claim **1**, further comprising:

input transistors connected electrically to the primary winding;

wherein the control system is configured to apply control signals to gates of the input transistors to cause the input transistor to operate as diodes.

10. The voltage converter of claim **1**, further comprising:

clamping diodes connected between voltages rails on a primary winding side of the transformer, the clamping diodes being configured to reduce voltage ringing on a secondary voltage side of the transformer.

11. The voltage converter of claim **1**, wherein the control system comprises comparators to compare the first voltage and the second voltage to reference voltages.

12. The voltage converter of claim **1**, further comprising:

a second inductor connected in series with the primary winding, the second inductor to provide storage for a phase-shifted full bridge to operate in a zero voltage switched (ZVS) mode of operation.

13. The voltage converter of claim **1**, wherein the voltage converter comprises a buck converter; and

wherein controlling operation of the first transistor and the second transistor to produce voltage at the primary winding based on a voltage across the capacitor comprises controlling the buck converter to operate as a boost converter.

14. The voltage converter of claim **1**, wherein the primary winding is configured to support a higher voltage than a combined voltage of the first secondary winding and the second secondary winding multiplied by a turns ratio of the transformer.

15. The voltage converter of claim **1**, further comprising:

an output terminal to connect to a load; and

circuitry to detect current through the inductor to the transformer;

wherein each pulse-width modulated control signal has a rising edge that corresponds to a decrease in the first voltage or the second voltage and has a falling edge that corresponds to a predefined current through the inductor.

16. A method of controlling a voltage converter comprising:

detecting a first voltage at a first drain of a first transistor that is connected between a first secondary winding of a transformer and electrical ground;

detecting a second voltage at a second drain of a second transistor that is connected between a second secondary winding of the transformer and electrical ground;

detecting a current through an inductor connected at a center tap between the first secondary winding and the

second secondary winding, the inductor being connected in series with a capacitor that is connected to electrical ground;

generating pulse-width modulated control signals based on the first voltage, the second voltage, and the current through the inductor; and

controlling operation of the first transistor and the second transistor based on the pulse-width modulated control signals to cause the capacitor to discharge current through the inductor towards the transformer and thereby produce a voltage at a primary winding of the transformer.

17. The method of claim **16**, wherein each pulse-width modulated control signal has a rising edge that corresponds to a decrease in the first voltage or the second voltage and has a falling edge that corresponds to the current through the inductor.

18. The method of claim **16**, wherein the current through the inductor comprises a predefined maximum current through the inductor, the predefined maximum current being based at least in part on the transformer.

19. The method of claim **16**, wherein the voltage converter comprises a step-down converter; and

wherein controlling operation of the first transistor and the second transistor based on the pulse-width modulated control signals to cause the capacitor to discharge current through the inductor and thereby produce a voltage at a primary winding of the transformer comprises controlling the step-down converter to operate as a step-up converter.

20. The method of claim **16**, wherein operation of the first transistor and the second transistor is controlled until the capacitor discharges.

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