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(54) **MULTILEVEL CONVERTER CIRCUIT AND METHOD**

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H02M 7/5395	(2006.01)
H02M 7/64	(2006.01)
H02M 7/49	(2007.01)

(52) **U.S. Cl.**

CPC ***H02M 7/483*** (2013.01); ***H02M 1/00*** (2013.01); ***H02M 7/49*** (2013.01); ***H02M 7/5395*** (2013.01); ***H02M 7/64*** (2013.01); *H02M 2001/007* (2013.01); *H02M 2001/0009* (2013.01)

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See application file for complete search history.

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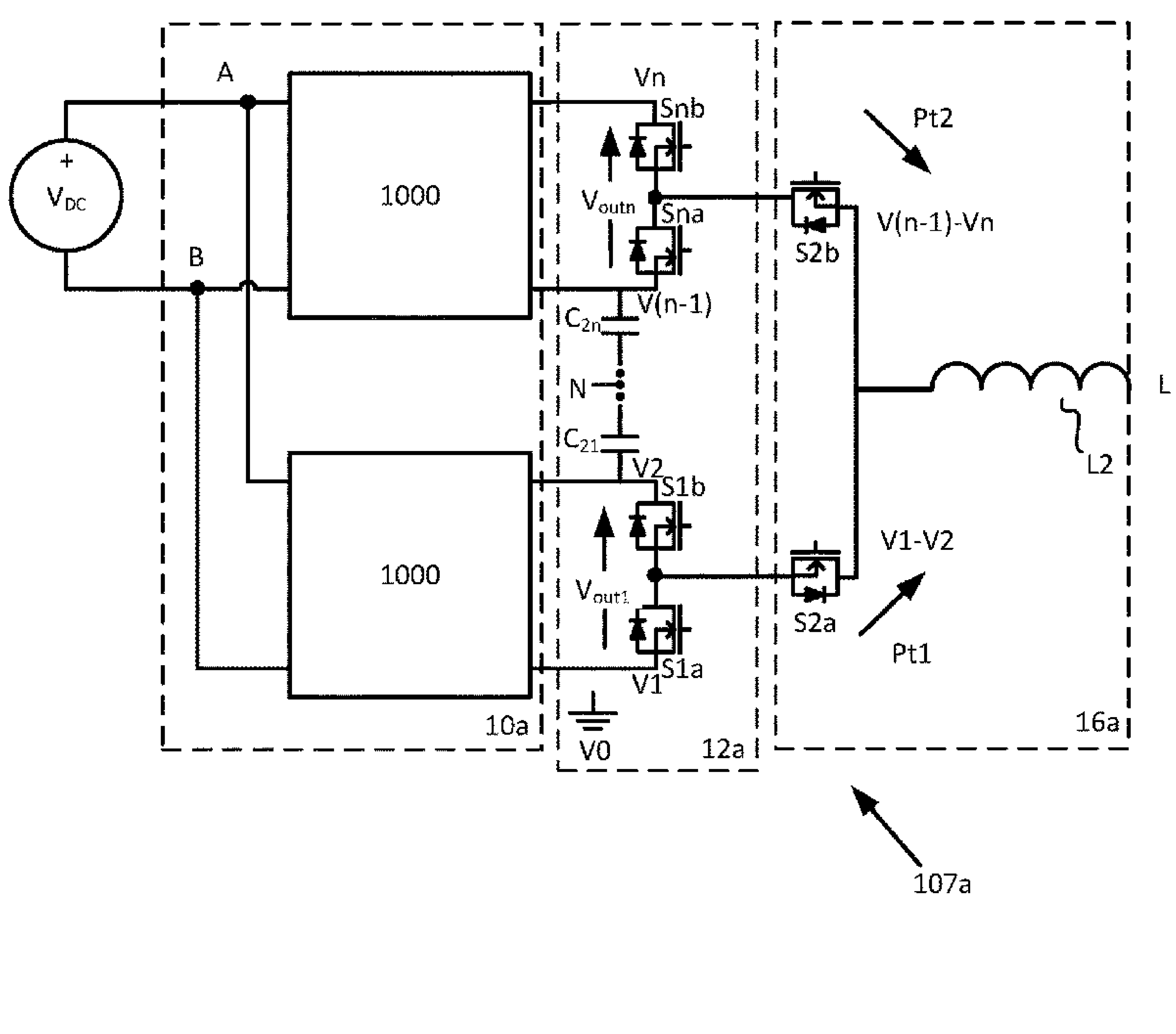
(57) **ABSTRACT**

A power conversion system including a first converter configured to convert an input voltage into a plurality of discrete voltages. A second converter configured to convert the plurality of discrete voltages into a plurality of modulated voltages. Each modulated voltage of the plurality of modulated voltages comprises two voltage levels equal, respectively, to two of the discrete voltages of the plurality of discrete voltages. A selection unit configured to alternatively output each modulated voltage of the plurality of modulated voltages across a pair of output terminals.

20 Claims, 14 Drawing Sheets



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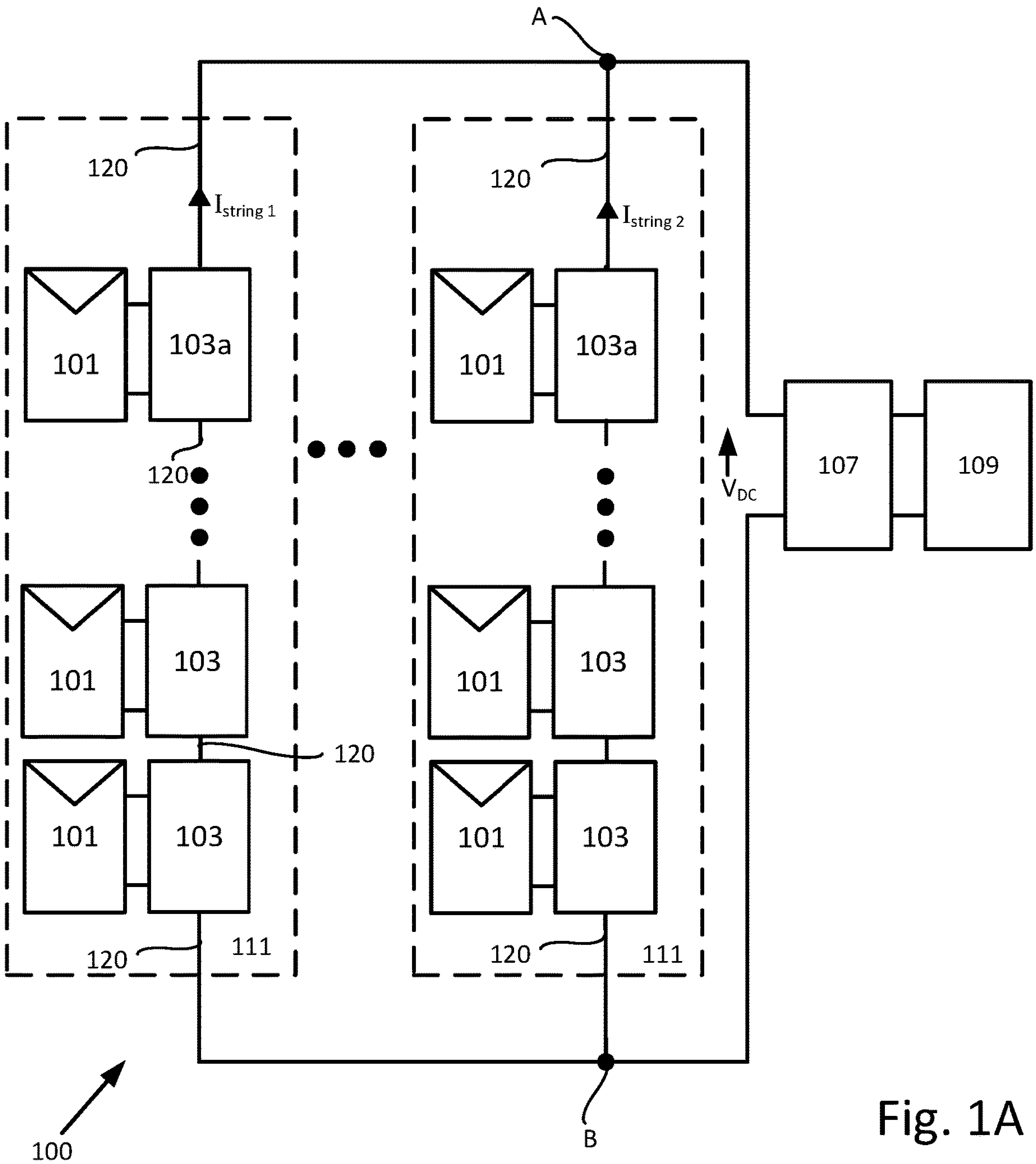
A
120
$I_{string\ 1}$
120
$I_{string\ 2}$
101
103a
101
103a
107
109
120
V_{DC}
101
103
101
103
120
101
103
101
103
120
111
120
111
100
B

Fig. 1A

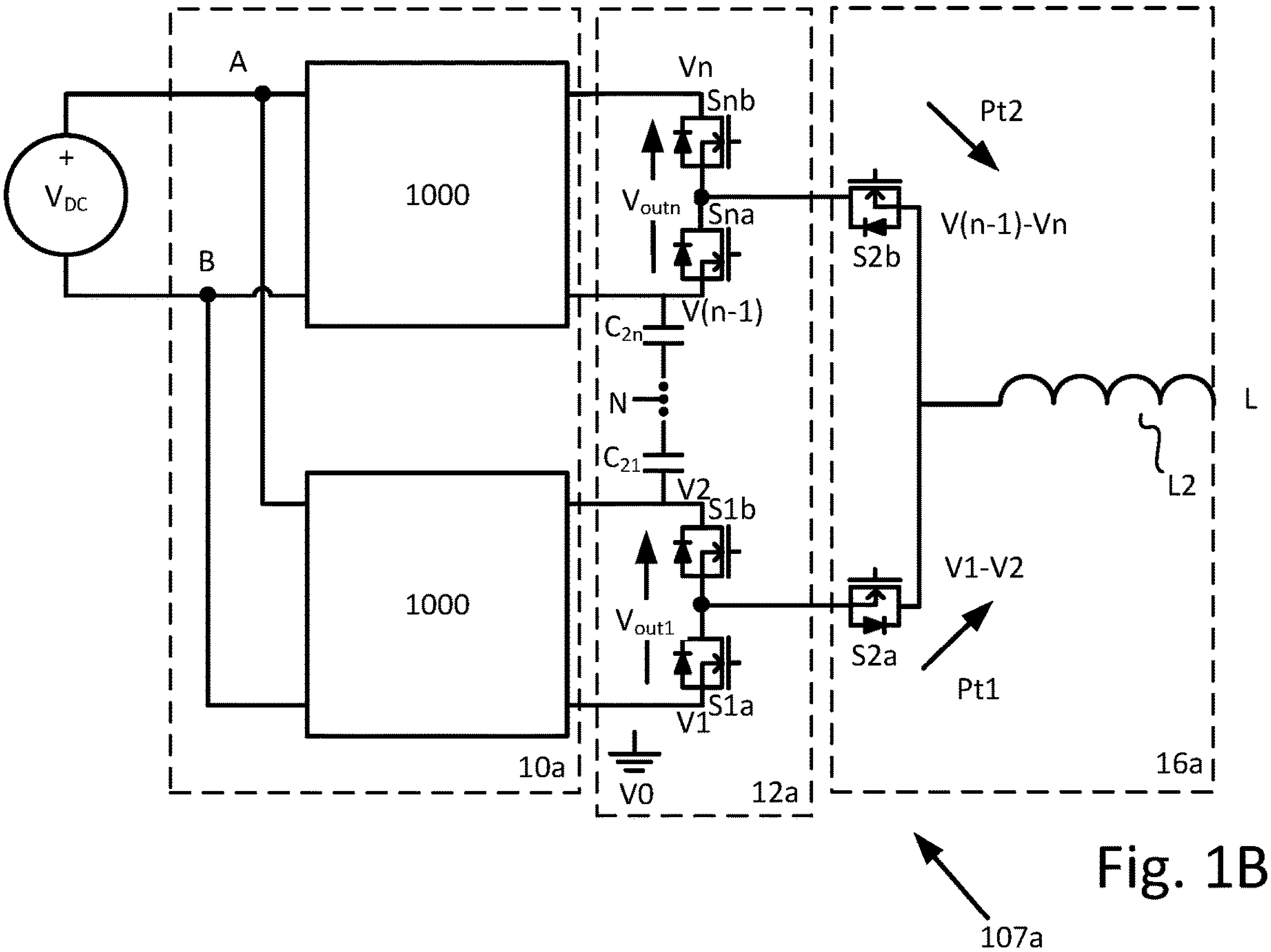
A
B
+
V_{DC}
1000
1000
10a
Vn
Snb
V_{outn}
Sna
V(n-1)
C_{2n}
N
C_{21}
V2
S1b
V_{out1}
S1a
V1
V0
12a
Pt2
V(n-1)-Vn
S2b
L
L2
V1-V2
S2a
Pt1
16a
107a

Fig. 1B

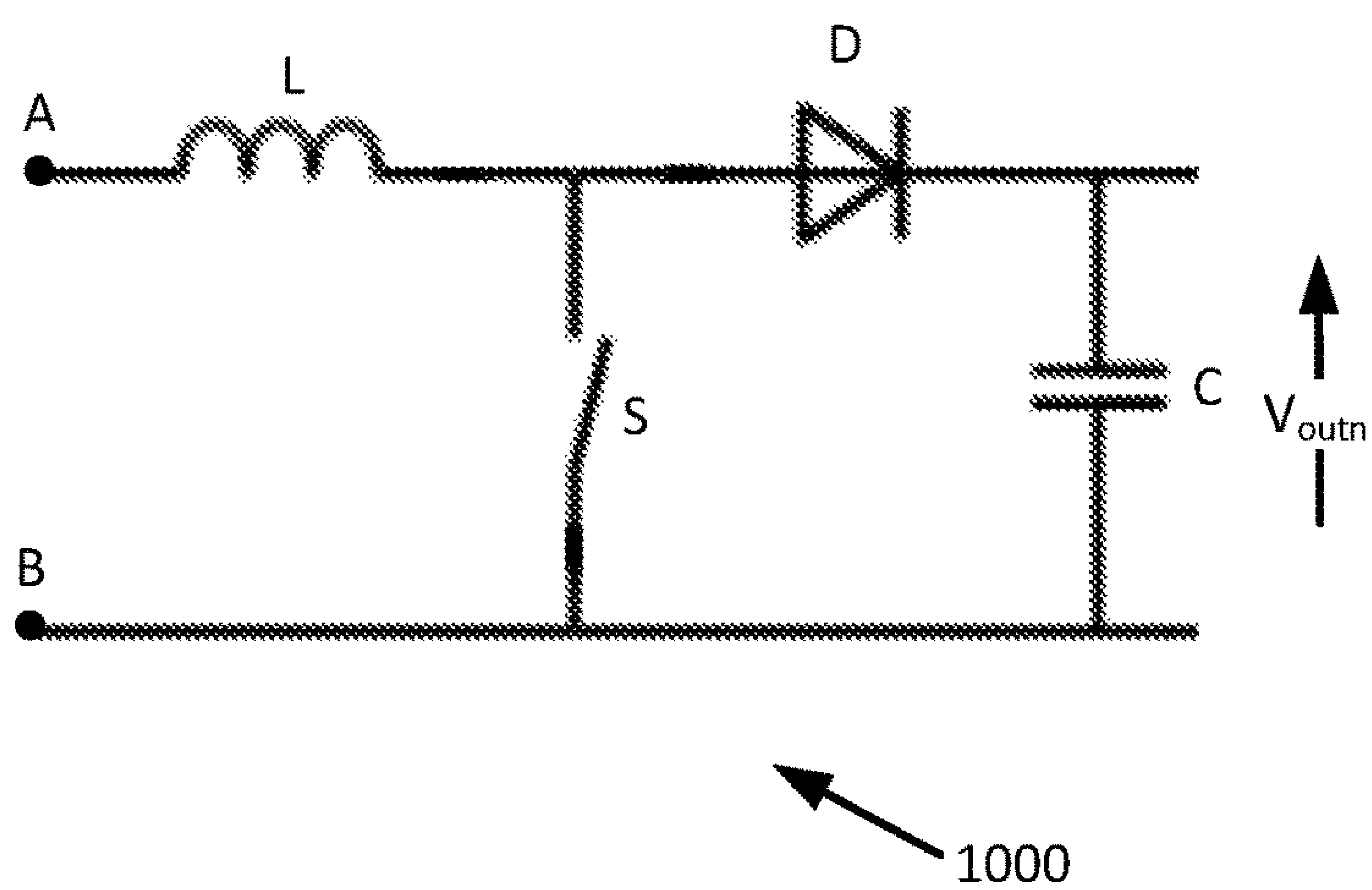
A
L
D
S
C
V_{outn}
B
1000

Fig. 1C

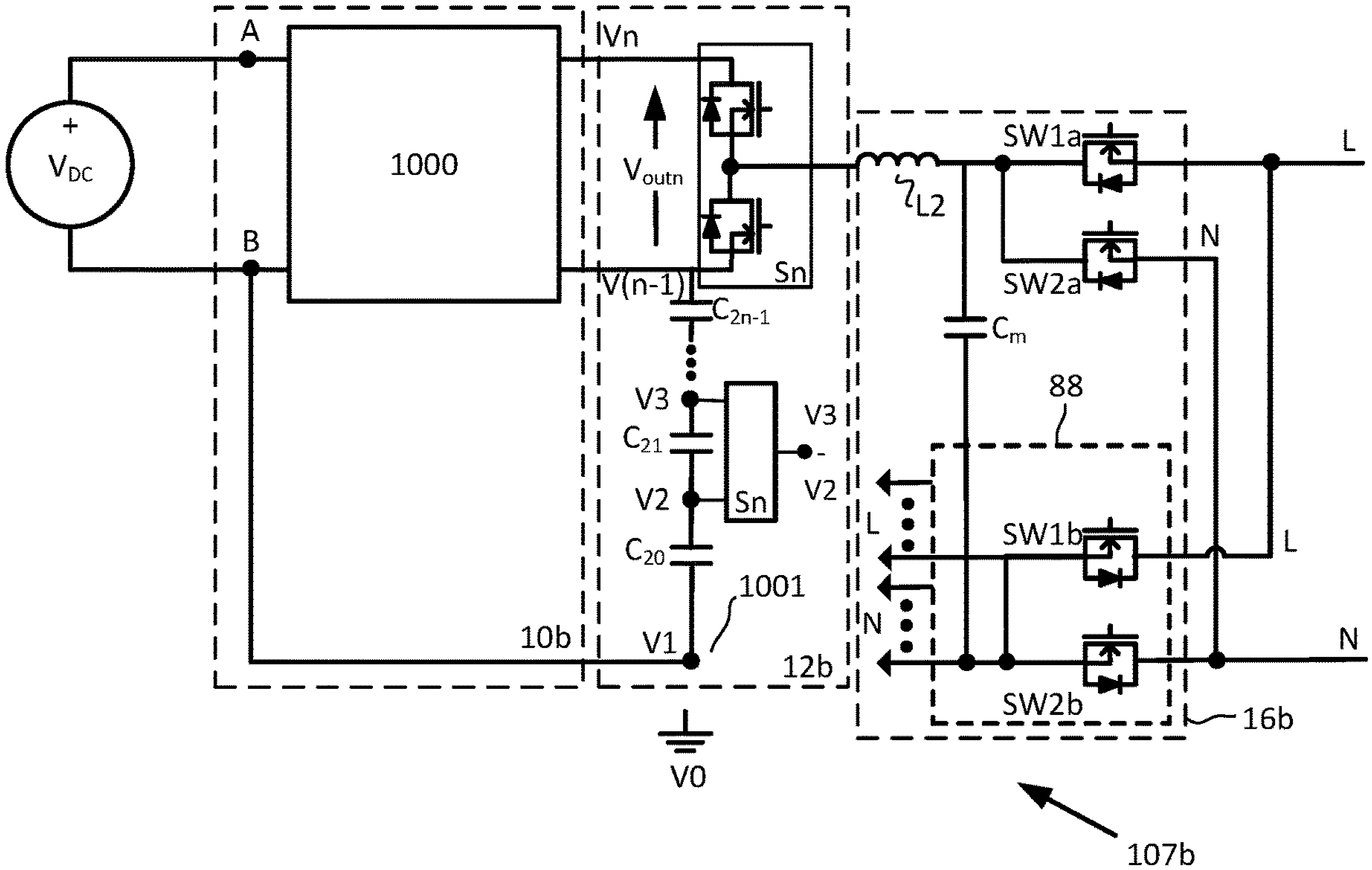
A
B
+
VDC
1000
Vn
Voutn
V(n-1)
Sn
C2n-1
V3
C21
V2
C20
V1
Sn
V3
V2
1001
10b
12b
V0
L2
SW1a
SW2a
L
N
Cm
88
L
N
SW1b
SW2b
L
N
16b
107b

Fig. 1D

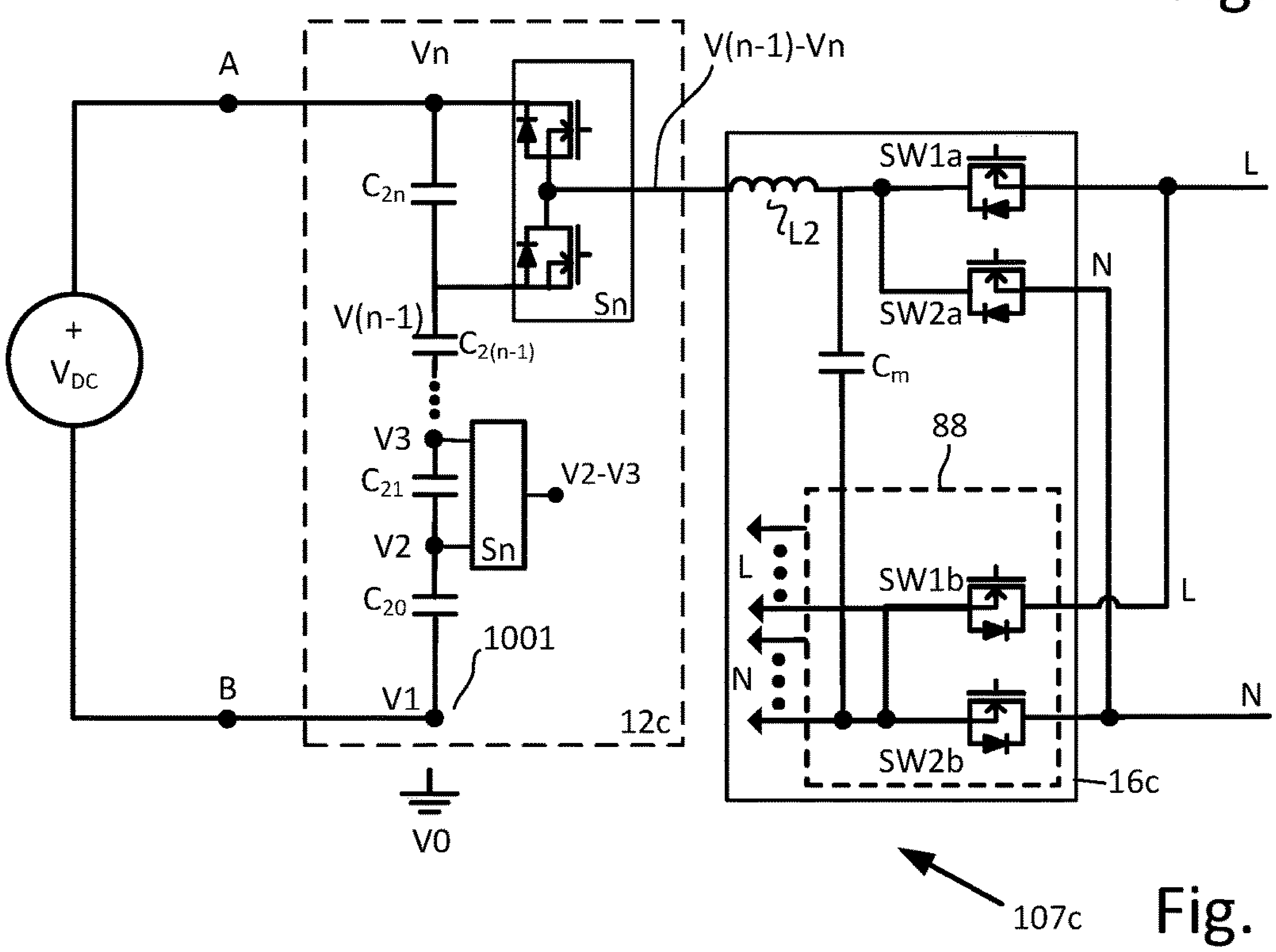
A
B
+
VDC
Vn
C2n
V(n-1)
C2(n-1)
Sn
V(n-1)-Vn
V3
C21
V2
C20
V1
Sn
V2-V3
1001
12c
V0
L2
SW1a
SW2a
L
N
Cm
88
L
N
SW1b
SW2b
L
N
16c
107c

Fig. 1E

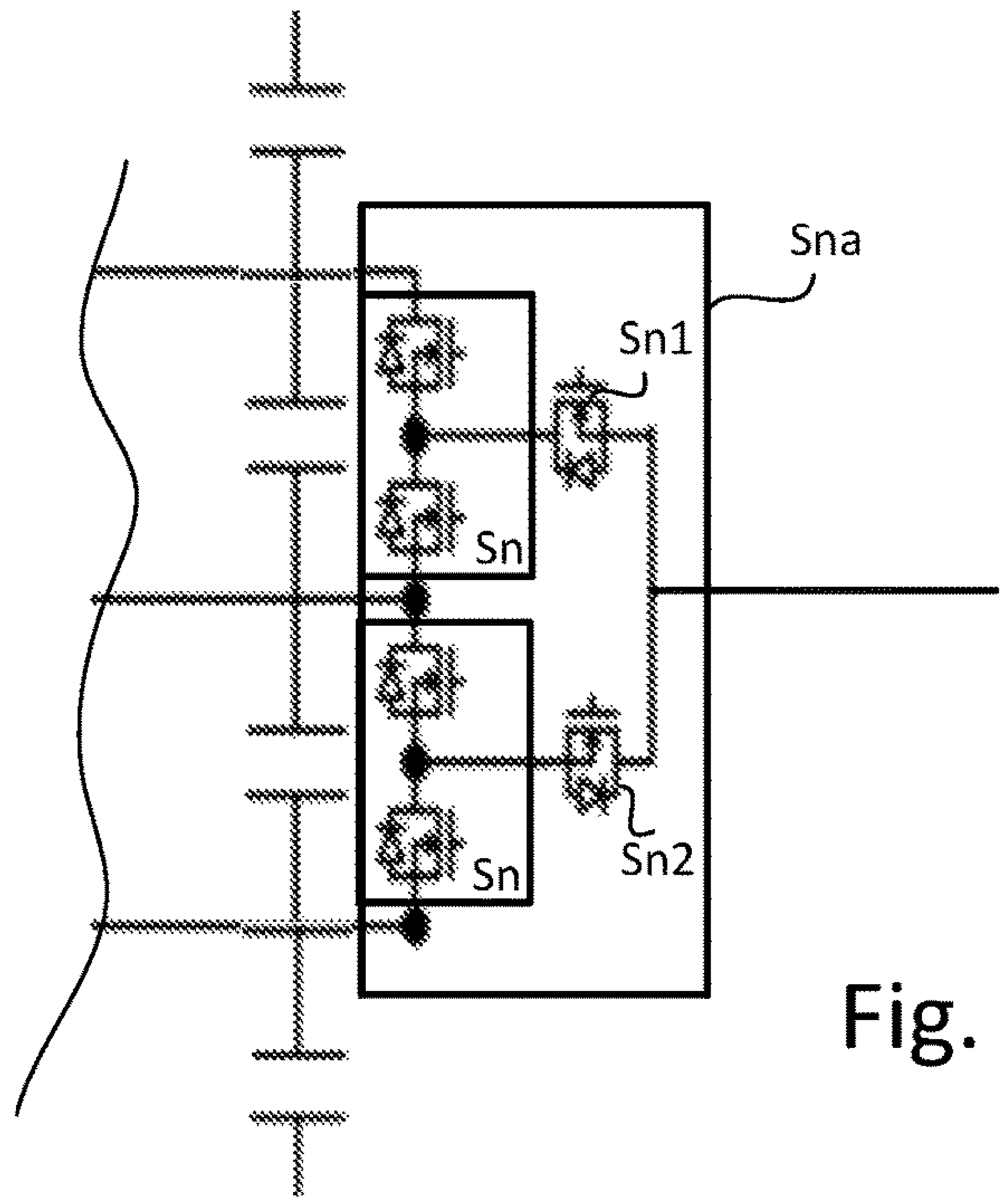
Sna
Sn1
Sn
Sn
Sn2

Fig. 1F

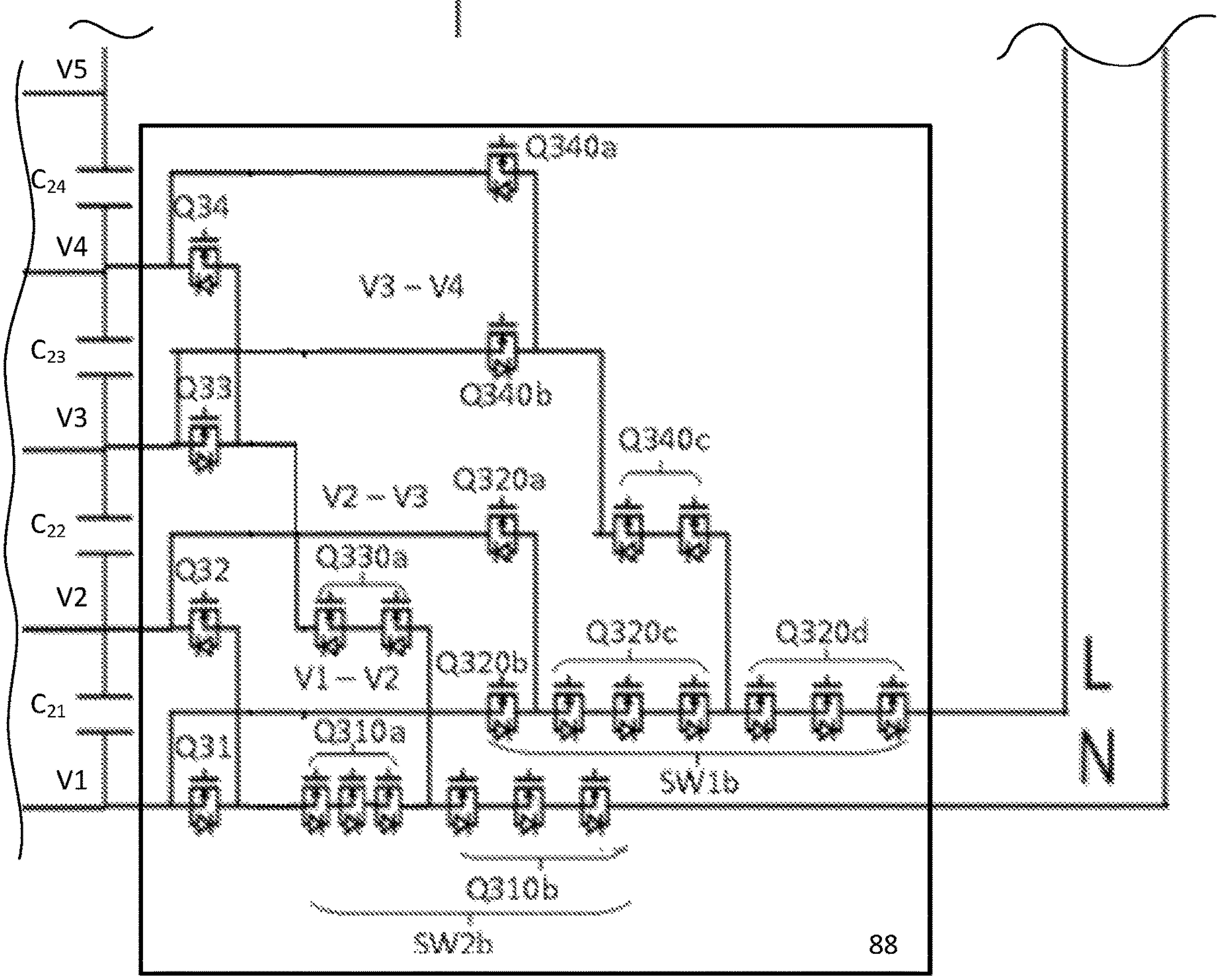
V5
C_{24}
Q340a
Q34
V4
V3 – V4
C_{23}
Q33
Q340b
V3
Q340c
V2 – V3
Q320a
C_{22}
Q32
Q330a
V2
Q320c
Q320d
Q320b
L
V1 – V2
C_{21}
Q31
Q310a
N
SW1b
V1
Q310b
SW2b
88

Fig. 1G

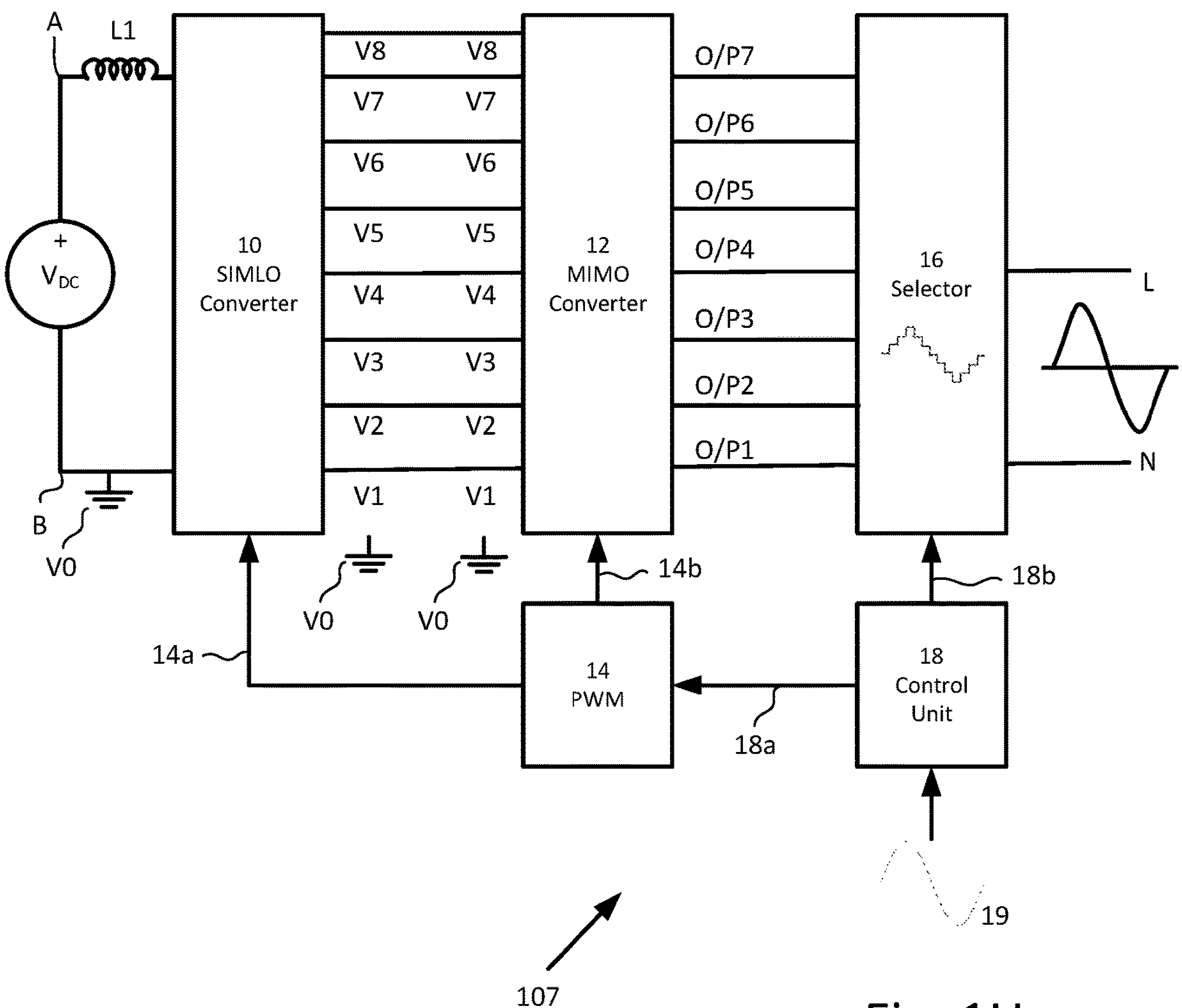
A
L1
B
V0
+
VDC
10
SIMLO
Converter
V8
V7
V6
V5
V4
V3
V2
V1
V0
V0
12
MIMO
Converter
O/P7
O/P6
O/P5
O/P4
O/P3
O/P2
O/P1
16
Selector
L
N
14a
14b
14
PWM
18a
18b
18
Control
Unit
19
107

Fig. 1H

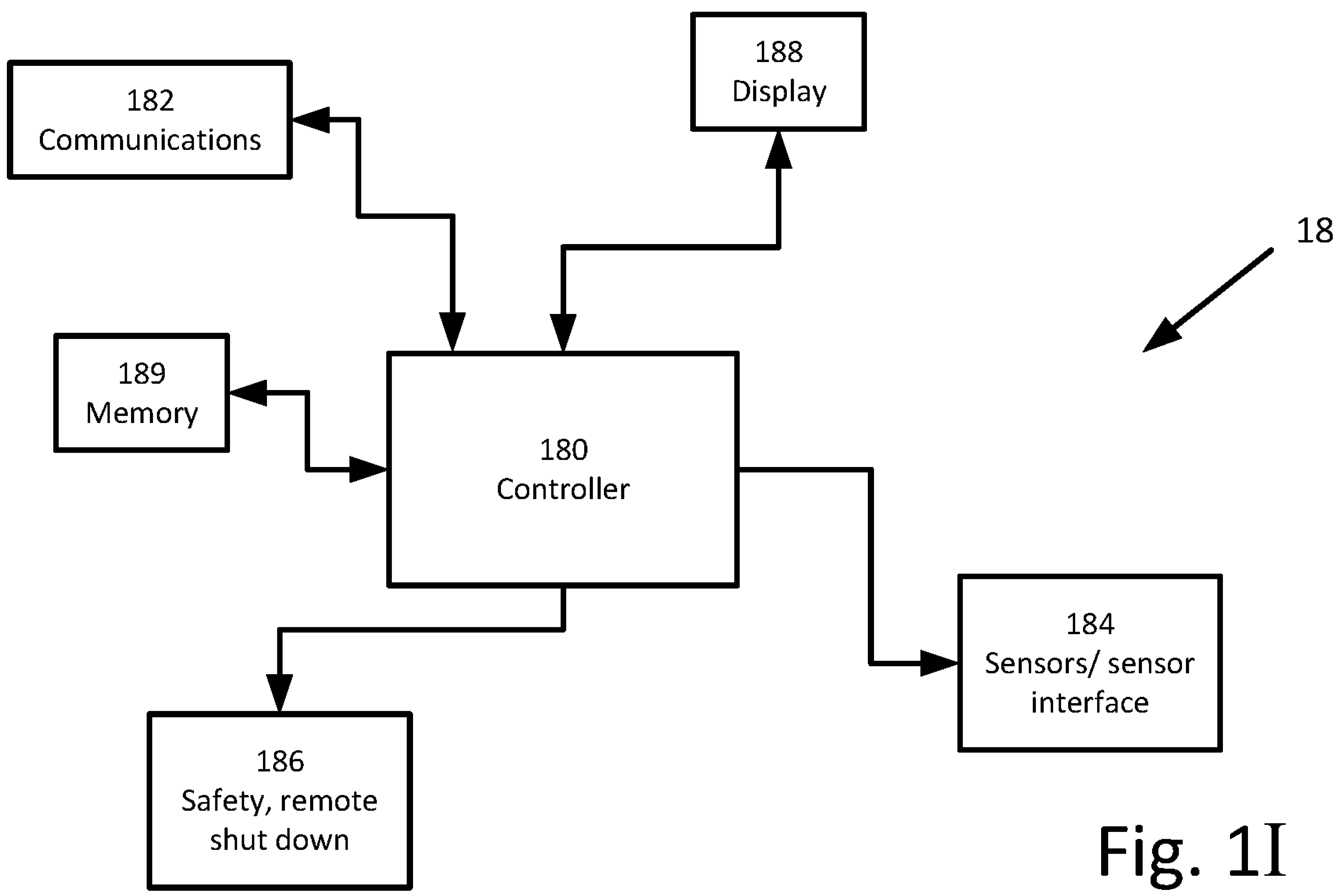
182
Communications
188
Display
18
189
Memory
180
Controller
184
Sensors/ sensor
interface
186
Safety, remote
shut down

Fig. 1I

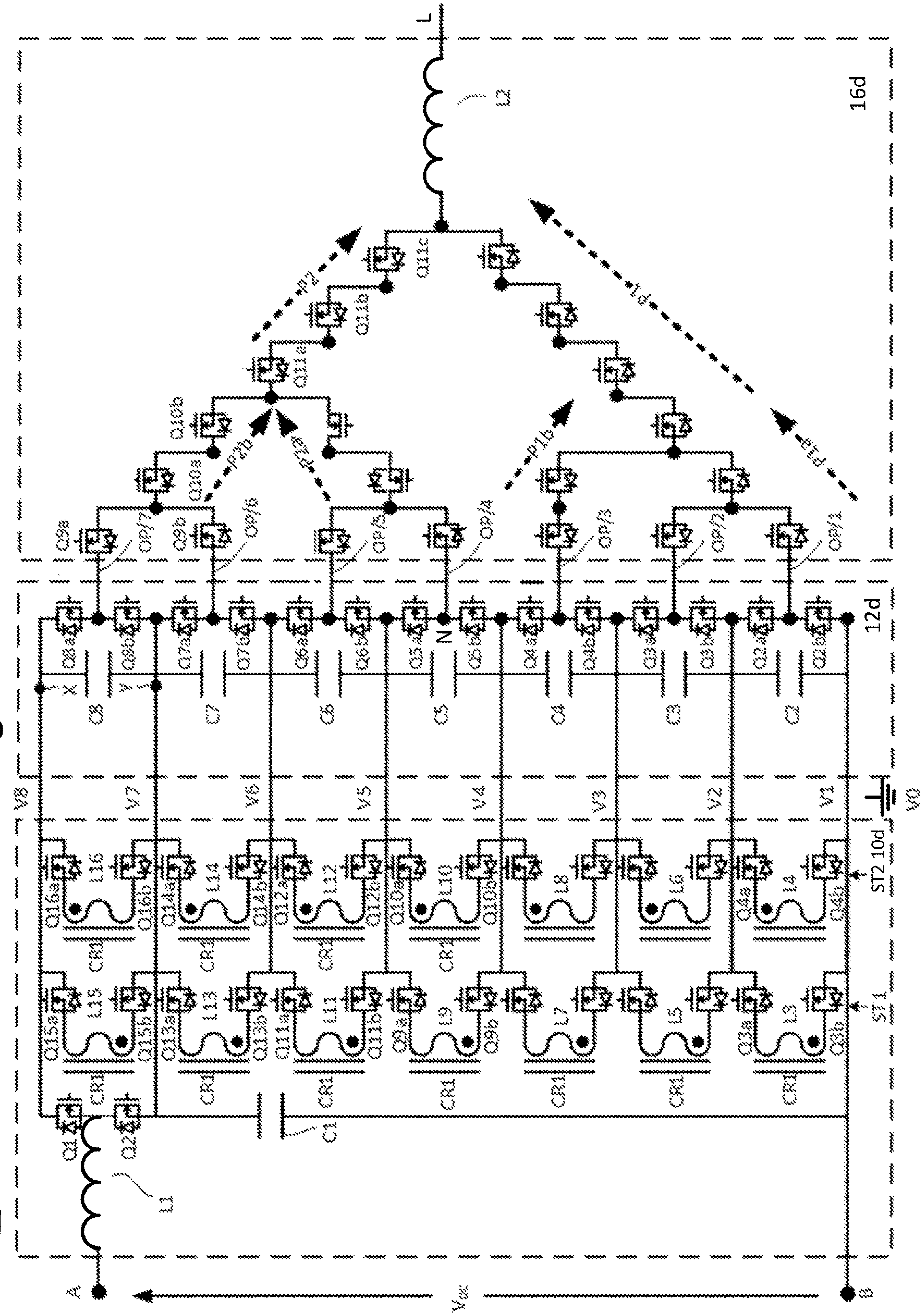
107d
A
B
V_{dc}
L
L2
16d
12d
ST2 10d
ST1
V0
V1
V2
V3
V4
V5
V6
V7
V8
L1
C1
C2
C3
C4
C5
C6
C7
C8
N
X
Y
P1a
P1b
P2a
P2b
P1d
P2

Fig. 1J

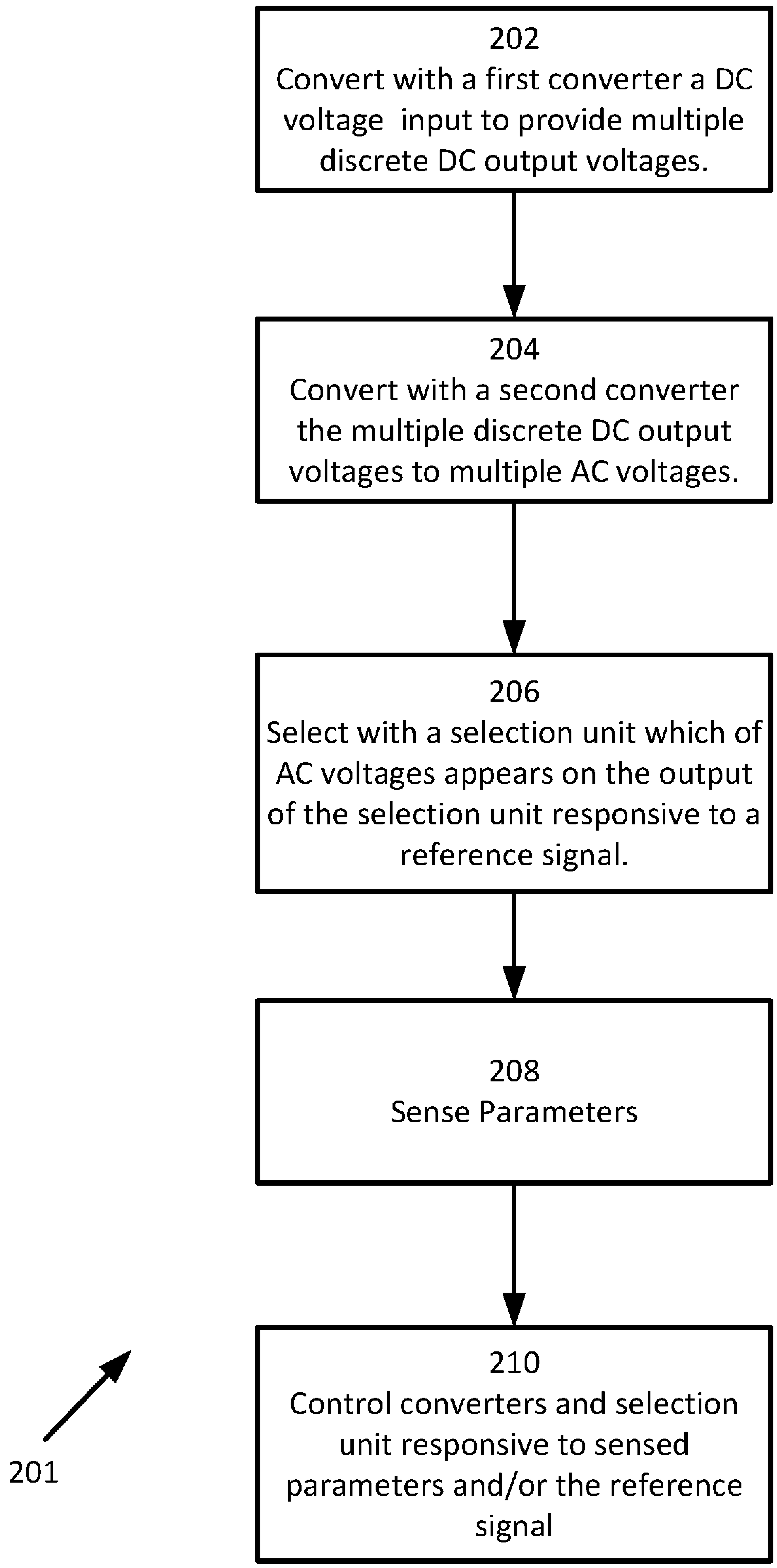
202
Convert with a first converter a DC voltage input to provide multiple discrete DC output voltages.
204
Convert with a second converter the multiple discrete DC output voltages to multiple AC voltages.
206
Select with a selection unit which of AC voltages appears on the output of the selection unit responsive to a reference signal.
208
Sense Parameters
210
Control converters and selection unit responsive to sensed parameters and/or the reference signal
201

Fig. 2A

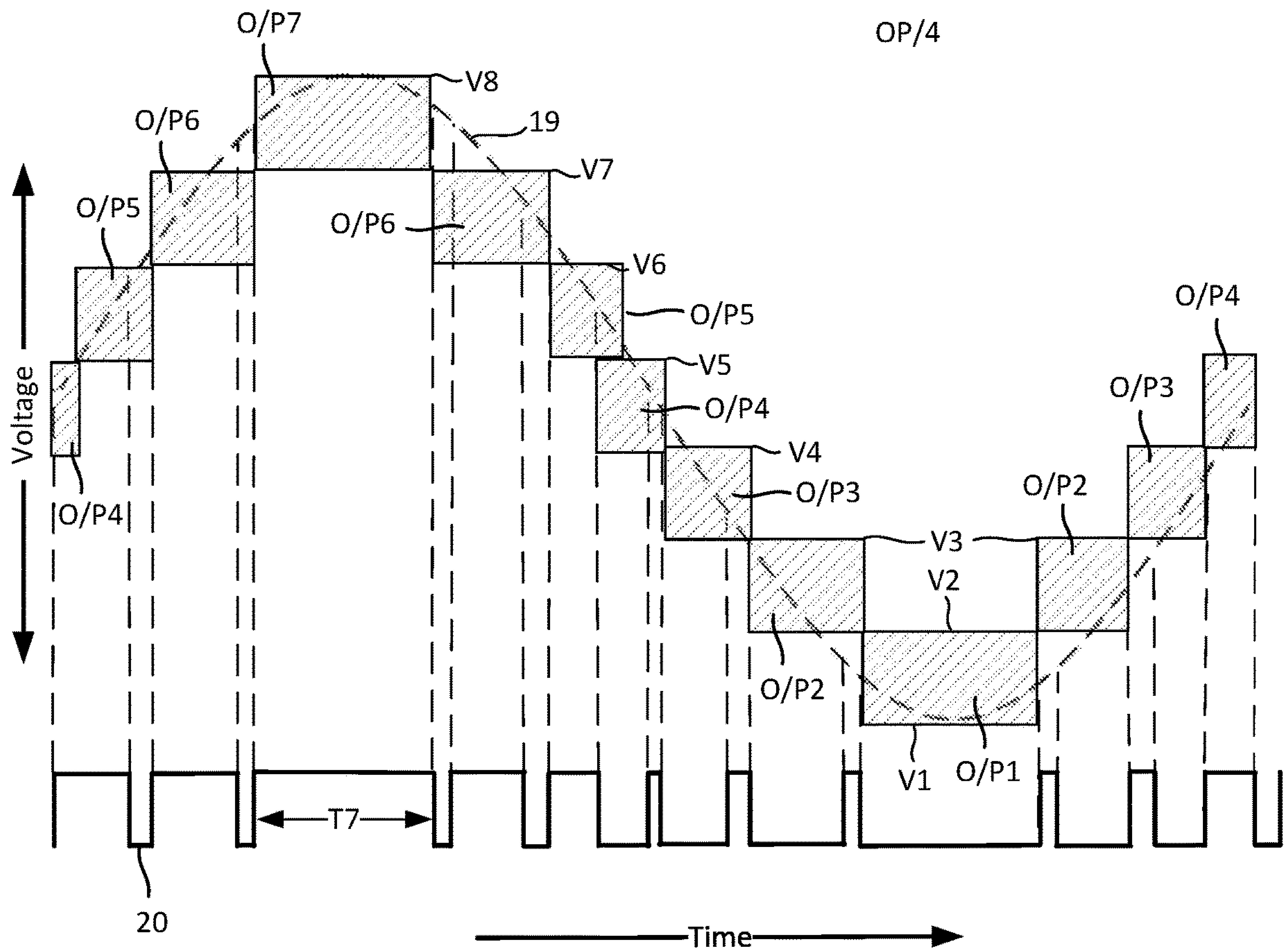
O/P7
OP/4
V8
19
O/P6
V7
O/P5
O/P6
V6
O/P5
V5
O/P4
Voltage
V4
O/P3
O/P3
O/P4
O/P2
V3
O/P4
V2
O/P2
V1
O/P1
T7
20
Time

Fig. 2B

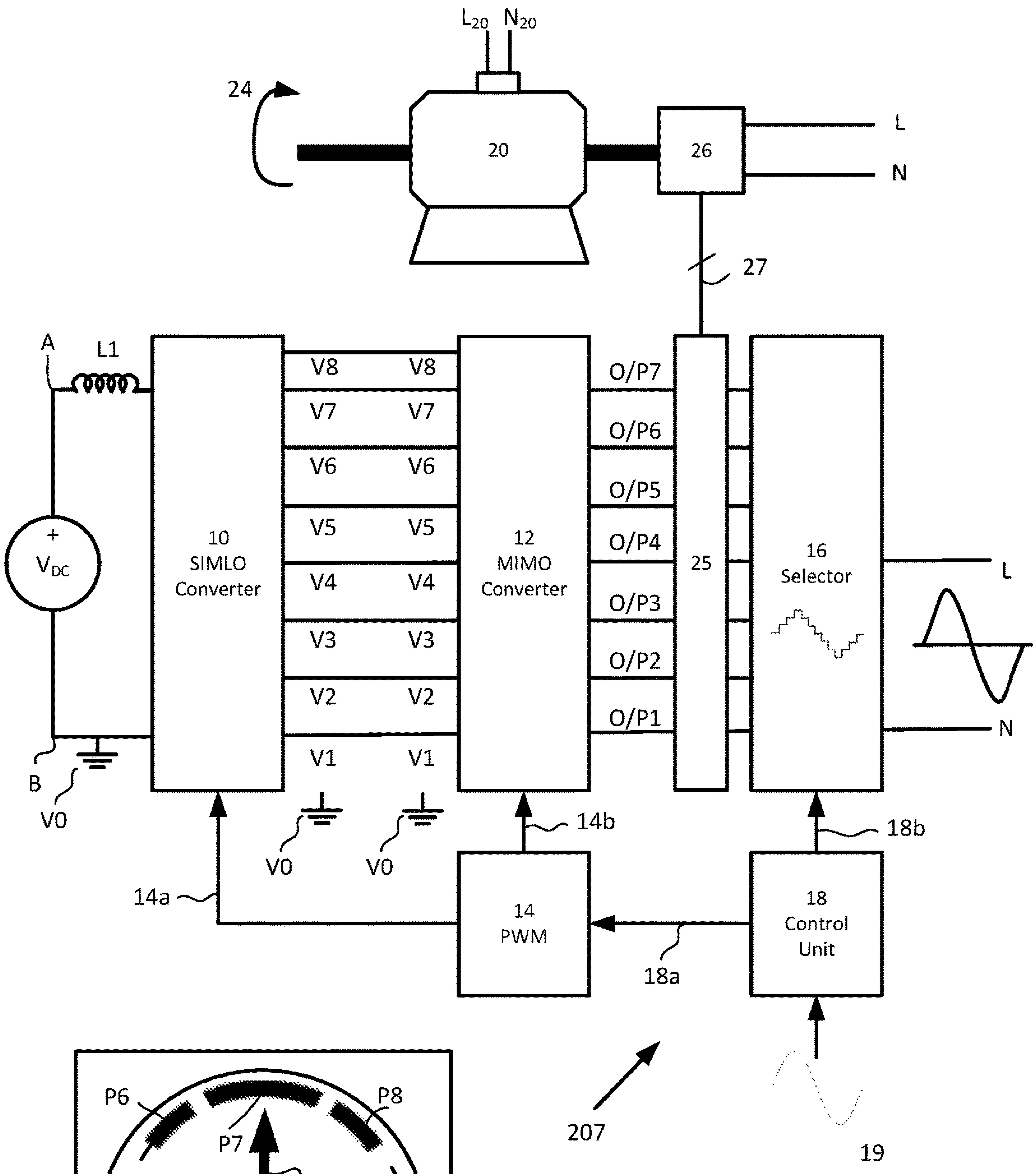
L20 N20
24
20
26
L
N
27
A
L1
+
VDC
10
SIMLO
Converter
V8 V8
V7 V7
V6 V6
V5 V5
V4 V4
V3 V3
V2 V2
V1 V1
12
MIMO
Converter
O/P7
O/P6
O/P5
O/P4
O/P3
O/P2
O/P1
25
16
Selector
L
N
B
V0
V0
V0
14b
18b
14a
14
PWM
18
Control
Unit
18a
207
19

Fig. 2C

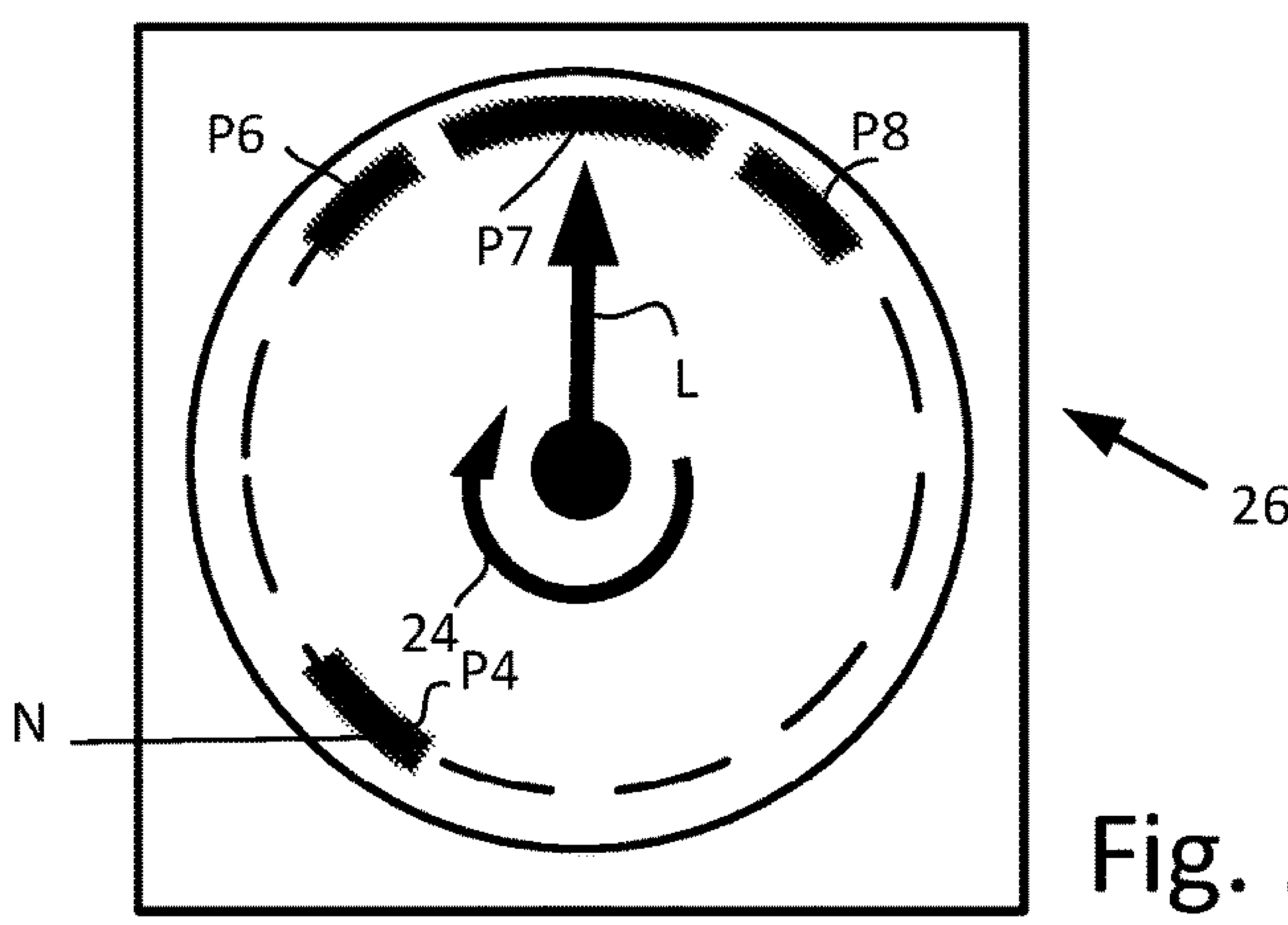
P6
P8
P7
L
24
P4
N
26

Fig. 2D

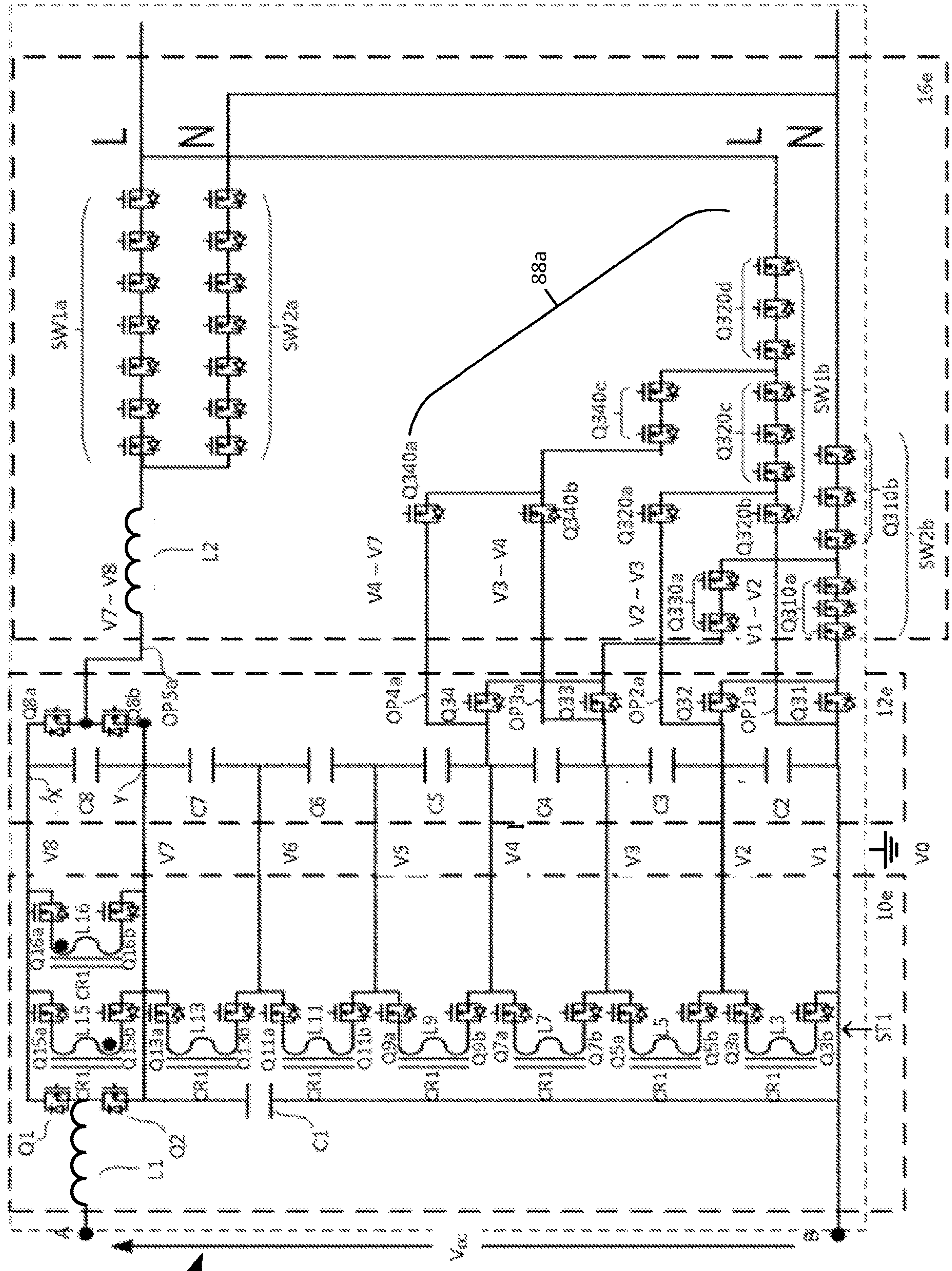
16e
L
N
L
N
SW1a
SW2a
88a
Q320d
Q340c
Q320c
SW1b
Q340a
Q340b
Q320a
Q320b
Q310b
SW2b
Q330a
Q310a
L2
V7 – V8
V4 – V7
V3 – V4
V2 – V3
V1 – V2
Q8a
Q8b
OP5a
OP4a
Q34
OP3a
Q33
OP2a
Q32
OP1a
Q31
12e
C8
C7
C6
C5
C4
C3
C2
X
Y
V8
V7
V6
V5
V4
V3
V2
V1
V0
10e
Q16a
L16
Q16b
Q15a
L15
CR1
Q15b
Q13a
L13
Q13b
Q11a
L11
Q11b
Q9a
L9
Q9b
Q7a
L7
Q7b
Q5a
L5
Q5b
Q3a
L3
Q3b
ST1
Q1
Q2
L1
C1
A
B
107e

Fig. 3A

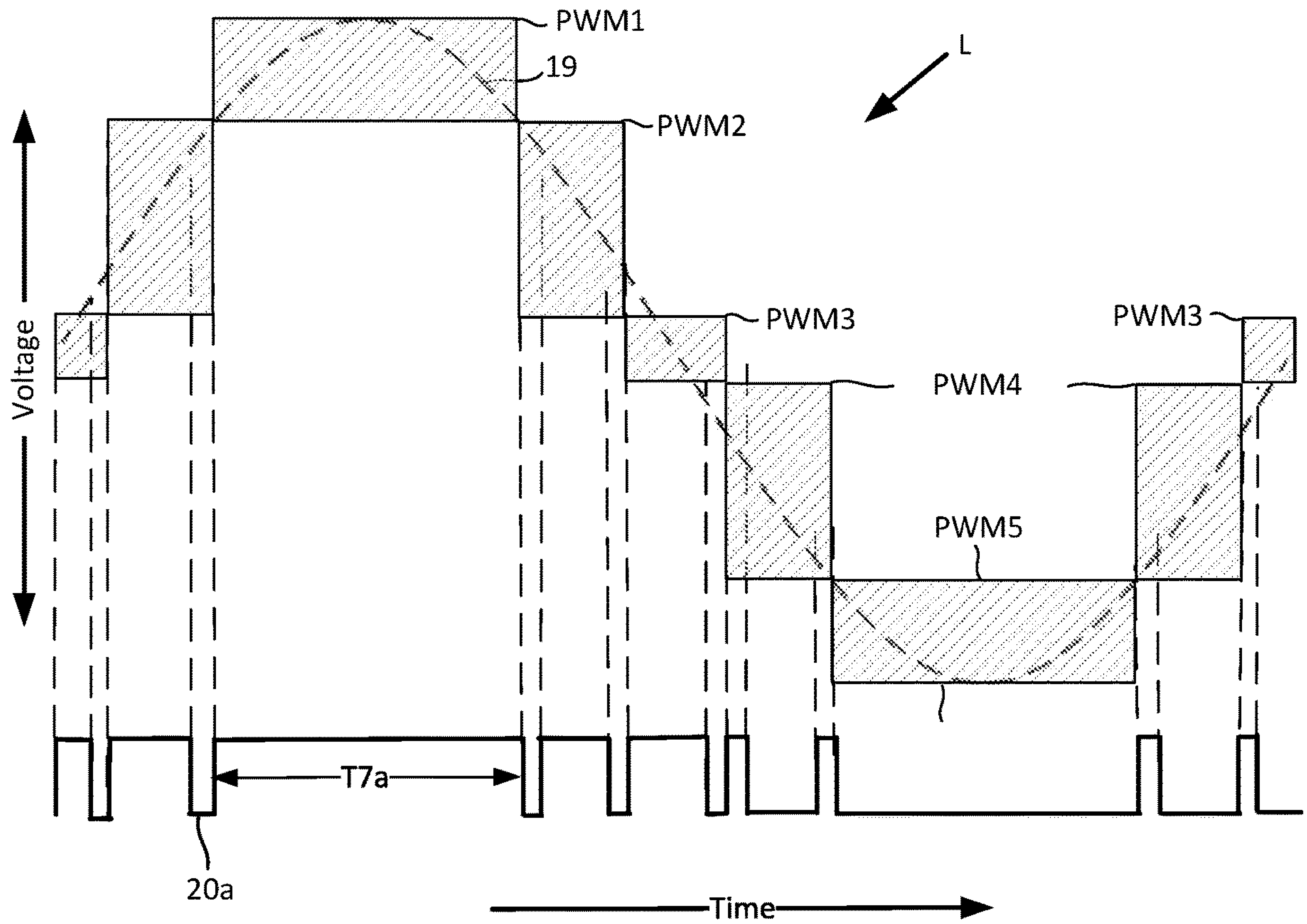

Fig. 3B

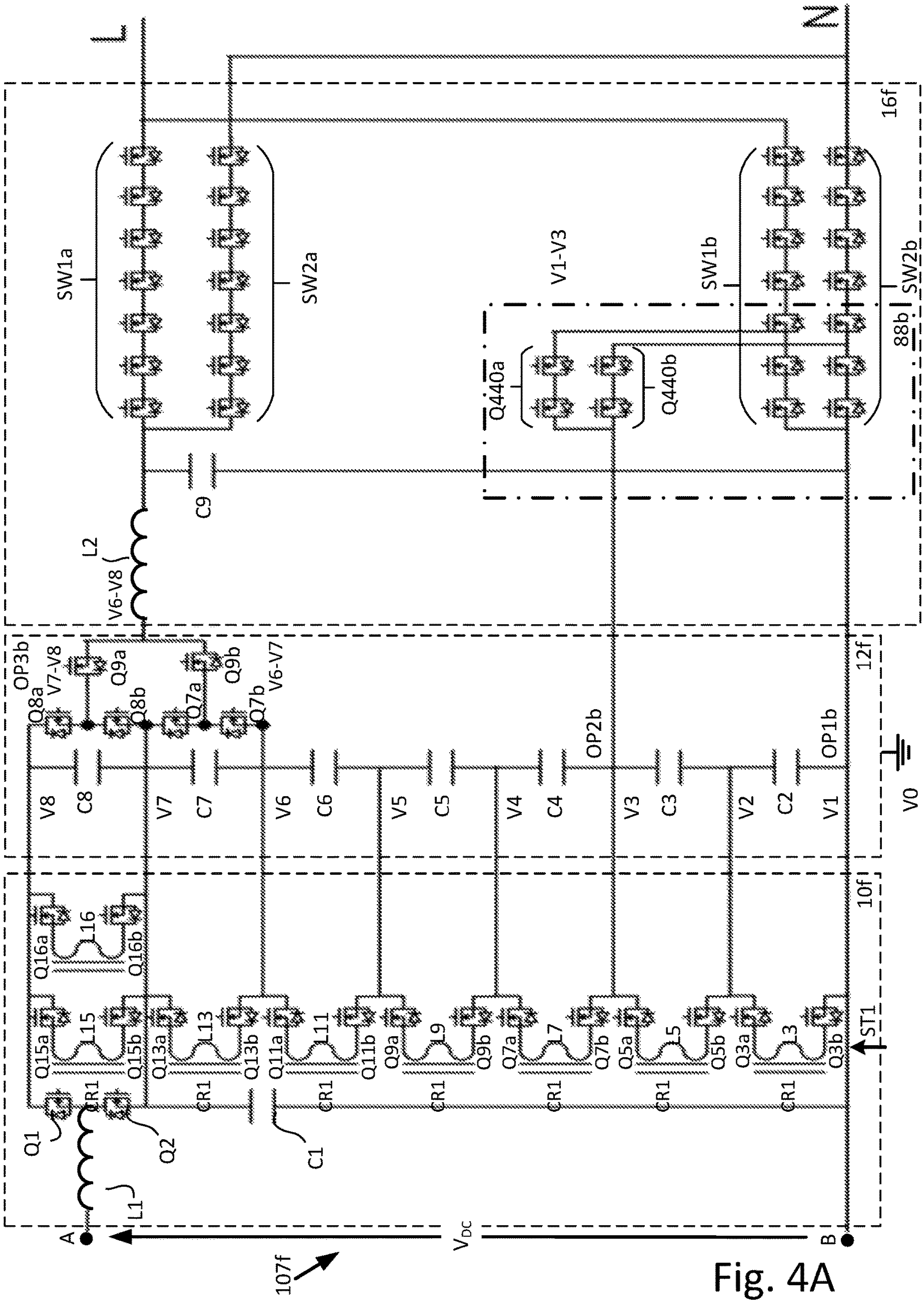
L
N
16f
SW1a
SW2a
SW1b
SW2b
V1-V3
Q440a
Q440b
88b
C9
L2
V6-V8
OP3b
V7-V8
Q9a
Q9b
Q8a
Q8b
Q7a
Q7b
V6-V7
12f
OP2b
OP1b
V8
C8
V7
C7
V6
C6
V5
C5
V4
C4
V3
C3
V2
C2
V1
V0
10f
Q16a
L16
Q16b
Q15a
L15
Q15b
Q13a
L13
Q13b
Q11a
L11
Q11b
Q9a
L9
Q9b
Q7a
L7
Q7b
Q5a
L5
Q5b
Q3a
L3
Q3b
ST1
CR1
Q1
Q2
C1
L1
A
B
V_{DC}
107f

Fig. 4A

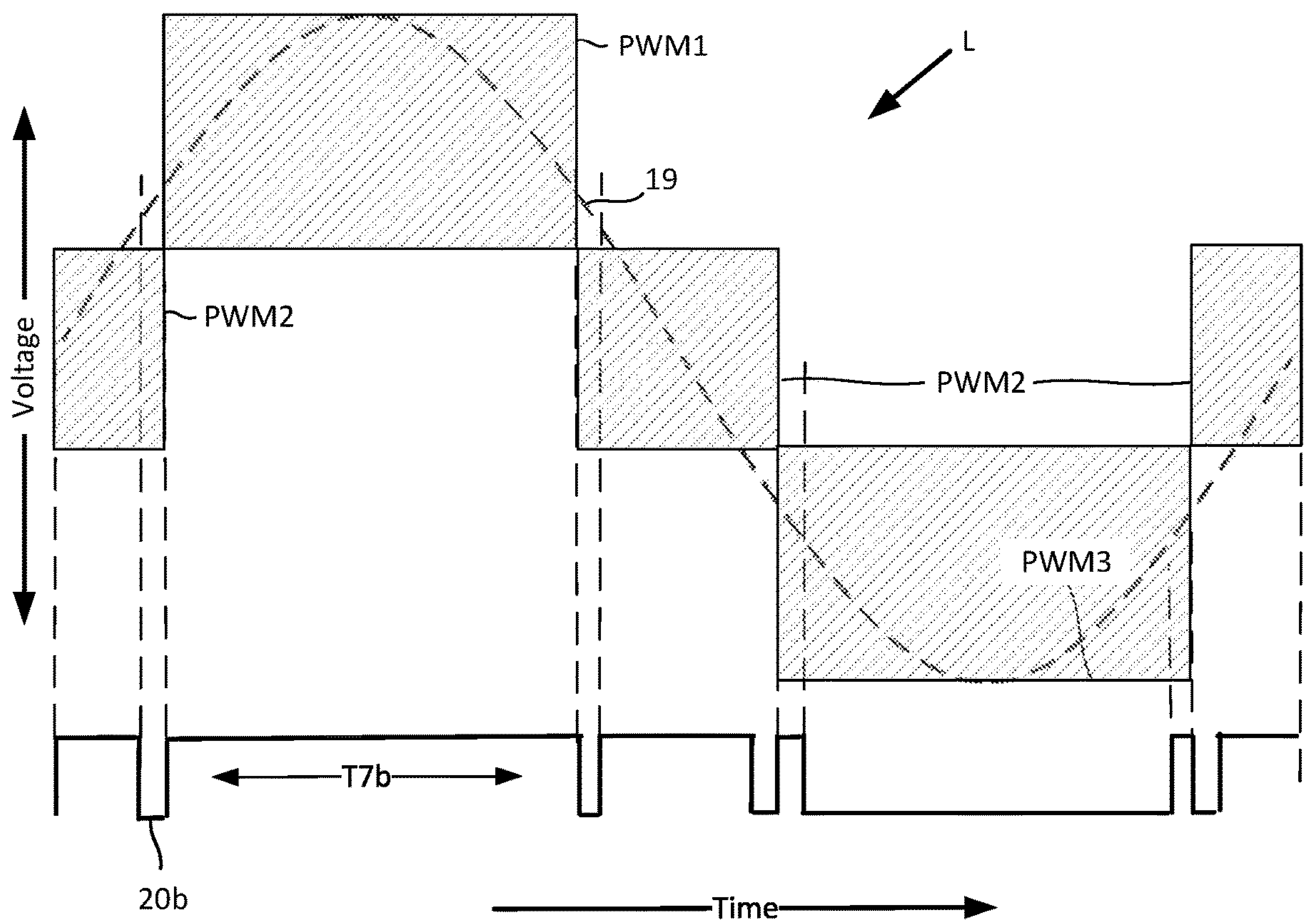

Fig. 4B

MULTILEVEL CONVERTER CIRCUIT AND METHOD

BACKGROUND

Converters may be used for converting direct current (DC) voltage into another DC voltage and/or to an alternating current (AC) voltage. Converter construction may typically make use of power transistors and diodes. The power transistors and diodes may be operated as electronic switches. Certain converter designs may use "hard" switching, which may give rise to switching losses which, for high values of the switching frequency, may cause a reduction in energy conversion efficiency. Hard switching may be characterized by a total commutation voltage drop over the current-carrying switch at a current commutation time. In case of hard switching, the voltage may increase up to the value of the commutation voltage while the current continues flowing, before it drops, which may cause high power loss peaks in the switch. It may therefore be desirable to develop converter topologies and switching methods that enable "soft" switching, which may reduce total switching losses.

In attempts to improve converter efficiency and reduce costs, high-power converters may make use of a technique referred to as multi-level inversion. Multi-level converter design may reduce the occurrence of simultaneously high values of voltage and current, and hence high-power dissipation values, during the switching process. Additionally, multi-level converter topologies may provide multiple output voltage values, which may reduce the size of associated output filters. It may be desirable to develop converter topologies and efficient switching methodologies to improve the cost and/or efficiency of converters.

SUMMARY

The following summary briefly describes certain features and is not intended to be an extensive overview and is not intended to identify key or critical elements.

Systems, apparatuses, and methods are described for a multi-level converter configurable to convert a direct current (DC) voltage its input to an alternating current (AC) at its output. A first converter may be adapted to convert an input voltage to give multiple first discrete output voltages on respective first output terminals of the first converter. A second converter may be adapted to convert at least one of the first discrete output voltages to two discrete states of voltage. The two discrete states of voltage may be provided on multiple second output terminals of the second converter for each of the first discrete output voltages. A selection unit may be adapted to provide an output voltage on output terminals selected from the second output terminals responsive to sensed electrical parameters of the multi-level converter and/or a reference signal.

These and other features and advantages are described in greater detail in the Detailed Description below.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, aspects, and advantages of the present disclosure will become better understood with regard to the following description, claims, and drawings. The present disclosure is illustrated by way of example, and not limited by, the accompanying figures.

FIG. 1A shows a block diagram of power system, according to illustrative aspects of the disclosure.

FIGS. 1B, 1C, 1D, 1E illustrate diagrams of converters, according to illustrative aspects of the disclosure.

FIG. 1F illustrates a partial view of a switch network that may be included in a converter, according to illustrative aspects of the disclosure.

FIG. 1G illustrates details of a multiplexor, according to illustrative aspects of the disclosure.

FIG. 1H illustrates a block diagram of details of a converter, according to illustrative aspects of the disclosure.

FIG. 1I shows a block diagram of details of a controller and the elements that it interfaces with, according to illustrative aspects of the disclosure.

FIG. 1J shows a block diagram of details of a single input multi-level output (SIMLO) converter, a multi input multi output (MIMO) converter and a selector unit, according to illustrative aspects of the disclosure.

FIG. 2A shows a flow chart of a method for the operation of a converter, according to illustrative aspects of the disclosure.

FIG. 2B shows graphical waveforms to illustrate the operation of a converter, according to illustrative aspects of the disclosure.

FIG. 2C illustrates a block diagram of a converter, according to illustrative aspects of the disclosure.

FIG. 2D shows further details of a rotary switch that may be included as part of the converter of FIG. 2C, according to illustrative aspects of the disclosure.

FIG. 3A shows a diagram of details of another SIMLO converter, MIMO converter and a selector unit, according to illustrative aspects of the disclosure.

FIG. 3B shows a possible waveform of the live (L) voltage output of the selection unit of FIG. 3A with respect to neutral (N), according to illustrative aspects of the disclosure.

FIG. 4A shows a diagram of details of a converter that includes a SIMLO converter, a MIMO converter and a selector unit, according to illustrative aspects of the disclosure.

FIG. 4B shows a possible waveform of the live voltage output of a selection unit of FIG. 4A with respect to neutral (N), according to illustrative aspects of the disclosure.

DETAILED DESCRIPTION

In the following description of various illustrative embodiments, reference is made to the accompanying drawings, which form a part hereof, and in which is shown, by way of illustration, various embodiments in which aspects of the disclosure may be practiced.

By way of introduction, features may be directed in general to a converter topology that converts a direct current (DC) voltage at its input to an alternating current (AC) voltage at its output. The DC voltage at the input may be a single DC voltage that, for example, may be provided from various interconnections of DC power sources. The single DC voltage in a first conversion may be separated by the first conversion to give multiple DC outputs that then in a second conversion may provide multiple AC outputs. The AC outputs may then be selected and controlled responsive to a reference signal and/or electrical parameters sensed in the converter topology. The selection control may ensure correct levels of operating voltage, current, impedance, resistance, phase angle, power factor, level of harmonic distortion, frequency and/or power for example.

The term pulse width modulation (PWM) as used herein is with respect to the operation of switches described below. Unless otherwise stated, the term "PWM" refers to an active use of a switch for a period of time. The active use of the switch during the period of time may include the switch being substantially open and closed circuit repeatedly during the time period. The term 'ON' as used herein with respect to the operation of switches described below, refers to the active use of a switch during the time period. During the time period, the switch remains substantially closed circuit for the time period. The term "'OFF'" as used herein is with respect to the operation of switches described below and refers to active use of a switch during the time period. During the time period, the switch remains substantially open circuit for the time period.

The term "multiple" as used here in the detailed description indicates the property of having or involving two or more parts, elements, or members. The claim term "a plurality of" as used herein in the claims section finds support in the description with use of the term "multiple" and/or other plural forms. Other plural forms may include for example regular nouns that form their plurals by adding either the letter 's' or 'es' so that the plural of converter is converters or the plural of switch is switches for example.

Reference is now made to FIG. **1**A, which illustrates a block diagram of a power system **100**, according to illustrative aspects of the disclosure. Power system **100** may include multiple wiring configurations **111**. Each wiring configuration **111** may include one or more power sources **101** that may be connected to a respective power device **103**. Power sources **101** may be AC power sources (e.g., wind turbines) or sources of DC power derived from wind turbines, battery banks, photovoltaic solar panels, rectified alternating current (AC) or electrical power derived from petrol generators, for example. Each wiring configuration **111** may include output terminals A and B. The outputs on terminals A and B of the wiring configurations **111** may be connected in series to form a series connection of wiring configuration **111** outputs that may be connected to input terminals of a converter **107**. Each wiring configuration **111** may include output terminals A and B. The outputs on terminals A and B of the other wiring configurations **111** may be connected in parallel to form a parallel connection of wiring configuration **111** outputs. The parallel connection may be connected to input terminals of converter **107** with a voltage V_{DC}. The output terminals converter **107** may be connected to load **109** and/or multiple loads **109**. According to illustrative aspects of the disclosure described below, converter **107** may be a DC to AC converter, and load **109** may be an AC utility grid, for example.

Reference is now made to FIG. **1**B, which illustrates a block diagram of further details of converter **107***a*, according to illustrative aspects of the disclosure. Converter **107***a* may include single input multiple level output (SIMLO) converter **10***a*, multiple input multiple output (MIMO) converter **12***a* and selector unit **16***a*. Converter **107***a* may be considered as an example of a substantially symmetric converter topology. Connected to the input of SIMLO converter **10***a* at terminals A and B is direct current (DC) voltage V_{DC}. Voltage V_{DC} may be supplied from the DC output of power system **100**. The voltage V_{DC} may be another source of DC supply such as DC from a battery, DC generator, a photovoltaic panel or any other source of DC power that may be provided on terminals A and B. Included in SIMLO converter **10***a* may be two DC to DC converters **1000** with two inputs connected in parallel to each other at terminals A and B.

Converters **1000** may have a series connection of switches S**1***a*/S**1***b* and Sna/Snb connected respectively across the two outputs of converters **1000**. Switches S**1***a*/S**1***b* and Sna/Snb may be included in MIMO converter **12***a*. A series connection of capacitors C_{21}-C_{2n} may connect between the two outputs of converters **1000**. At substantially in the middle of the series connection of capacitors C_{21}-C_{2n} may be provided the neutral (N) connection point for converter **107***a*. Two outputs of MIMO converter **12***a* may be provided at the respective points where switch S**1***a* connects to switch S**1***b* and switch Sna connects to switch Snb. The two outputs of MIMO converter **12***a* connect to the two inputs of selector unit **16***a* respectively to one side of each of switches S**2***a* and S**2***b*. The other side of switches S**2***a* and S**2***b* connect together and to one side of inductor L**2**. The other side of L**2** and the middle of the series connection of capacitors C_{21}-C_{2n} may provide respectively the live (L) and neutral (N) alternating current (AC) output of converter **107***a*. Converters **1000** located and connected on either side of the middle of the series connection of capacitors C_{21}-C_{2n}. The other side of switches S**2***a* and S**2***b* connecting together to one side of inductor L**2** provides the substantially symmetric topology of converter **107***a*.

In operation, SIMLO converter **10***a* may be configurable to convert voltage V_{DC} to two discrete voltage levels of DC output voltage respectively as V**1** or V**2** and Vn−1 or Vn. DC output voltage V**1** or V**2** and Vn−1 or Vn may be provided on each of the two output terminals of SIMLO converter **10***a* with respect to negative terminal V**0**. SIMLO converter may comprise switching circuitry as shown in FIG. **1**B and other figures. The two discrete voltage levels of DC output voltage on each the two output terminals of SIMLO converter **10***a* may provide two respective selectable current paths Pt**1** and Pt**2**. Paths Pt**1** and Pt**2** may be provided by selector unit **16***a* so as to provide the live (L) and neutral (N) alternating current (AC) output of converter **107***a*.

Reference is now made to FIG. **1**C, which illustrates a block diagram of further details of converter **1000**, according to illustrative aspects of the disclosure. Converter **1000** is shown as a DC to DC boost converter with input at terminals A and B. One side of inductor L connects to terminal A. The other side of inductor L connects to the anode of diode D and on side of switch S. The cathode of diode D connects to one side of capacitor C. The other sides of capacitor C and switch S connect to terminal B. The output of converter **1000** is provided across capacitor C as output voltage V_{outn}. In the case of converter **1000** being a DC to DC boost converter output voltage V_{outn} may be greater than the input voltage V_{DC} applied to the input of converter **1000**. Alternatively, or in addition, converter **1000** may be implemented as another DC to DC converter to give a buck, buck/boost and/or buck+boost operation on voltage V_{DC}.

Reference is now made to FIG. **1**D, which illustrates a block diagram of converter **107***b*, according to illustrative aspects of the disclosure. Converter **107***b* may include single input multiple level output (SIMLO) converter **10***b*, multiple input multiple output (MIMO) converter **12***b* and selector unit **16***b*. Converter **107***b* may be considered as an example of a substantially asymmetric converter topology. Connected to the input of SIMLO converter **10***b* at terminals A and B is direct current (DC) voltage V_{DC}. Included in SIMLO converter **10***b* may be DC to DC converter **1000** providing voltage V_{outn} at its output. Converter **1000** may have a series connection of switches in a switch network Sn connected respectively across the output of converter **1000**. Switch network Sn may be included in MIMO converter **12***b*. Further included in MIMO converter **12***b* is a series string of capacitors C_{20}-C_{2n-1} connected between the lower switch of switch network Sn and terminal B. A possibility of connecting other switch networks Sn across other capacitors is shown with respect to capacitor C_{21}.

An output of converter **12**b is provided at the point where the two series switches of switch network Sn. The output provided by switch network Sn may connect to an input of selector unit **16**b to one side of inductor L2 that may be included in selector unit **16**b. The other side of inductor L2 connects to one side of capacitor Cm and to one side of switches SW**1**a and SW**2**a, which are connected together. The other side of capacitor Cm connects to the neutral (N) connection point inside multiplexor (MUX) **88**. The other sides of switches SW**1**a and SW**2**a provide respectively the live (L) and neutral (N) outputs of converter **107**b. The live (L) and neutral (N) outputs of converter **107**b connect respectively to switches SW**1**b and SW**2**b that may be included in MUX **88**. The other side of switches SW**1**b and SW**2**b connect together and provide the multiple live (L) and neutral (N) inputs to MUX **88**. The multiple inputs may be provided by an interconnection of multiple switches (not shown). The interconnection may allow the live (L) or neutral (N) inputs of MUX **88** to be selectively connected to terminals V**1**, V**2**, V**2**-V**3**, V**3** and V(n−1) via respective switches SW**1**b and SW**2**b.

Reference is now made to FIG. **1**E, which illustrates a block diagram of converter **107**c, according to illustrative aspects of the disclosure. Converter **107**c may include multiple input multiple output (MIMO) converter **12**c and selector unit **16**c. Converter **107**c is the same as converter **107**b except that converter **107**c does not include SIMLO converter **10**b. Instead, with converter **107**c, voltage V_{DC} provided at terminals A and B may be connected across the input of MIMO converter **12**c at terminals Vn and V**1**. One converter **1000** (not shown in FIG. **1**E) may be located and connected to one side above the middle of the series connection of capacitors C_{21}-C_{2n}. The difference between connections/operating frequencies PWM of switch network Sn and multiplexor **88** may provide the substantially asymmetric topology of converters **107**d and **107**e.

Reference is now made to FIG. **1**F, which illustrates a partial view of a switch network Sna that may be included in a MIMO converter **12**, according to illustrative aspects of the disclosure. As with FIGS. **1**D and **1**E, the partial view shows two series connected switches connected across a capacitor that may be included in switch network Sn. The capacitor may be the output and/or the output capacitor C of converter **1000** or a capacitor of series string of capacitors C_{20}-C_{2n-1}. Another switch network Sn may be connected across another capacitor that may be next to the capacitor. Another switch network Sn may be separated a number of capacitors away from the capacitor in the series string of capacitors (C_{20}-C_{2n-1} for example). A further two switches Sn**1** and Sn**2** may be wired in series and wired across the two outputs of the two switch networks Sn. The point where switches Sn**1** and Sn**2** are connected together corresponds to the output of switch network Sna.

Reference is now made to FIG. **1**G, which illustrates further details of multiplexor **88**, according to illustrative aspects of the disclosure. In descriptions that follow, multiple switches wired in series such as switches Q**340**c, Q**330**a, and Q**310**a for example may be implemented with a single switch. The source of switch SW**1**a (not shown) may provide the live (L) output terminal of converters **107**b/**107**c and is further connected to the drain of switch SW**1**b/Q**320**d. The source of switch SW**2**a (not shown) may provide the neutral (N) output terminal of converters **107**b/c and is further connected to the drain of switch SW**2**b/Q**310**b. Switch SW**1**b may include switches Q**320**b, Q**320**c and Q**320**d. The source of switch Q**320**b connects to the source of switch Q**31**. In general switches Q**31**-Q**34** may be included as part of a MIMO converter **12** and/or a selector unit **16**. The drain of switch Q**320**b connects to the source of switch Q**320**c and the source of switch Q**320**a. The drain of switch Q**320**a connects to the drain of switch Q**32**. The drain of switch Q**320**c connects to the source of switch Q**320**d and to the source of switch Q**340**c. The drain of switch Q**340**c connects to the drain of switch Q**340**b and the source of switch Q**340**a. The drain of switch Q**340**a connects to the drain of switch Q**34**. The source of switch Q**340**b connects to the source of switch Q**33**. Switch SW**2**b may include switches Q**310**a where the drain of switch Q**310**a wired in series with the source switch Q**310**b. The point at which the drain of switch Q**310**a connects with the source switch Q**310**b also connects to the source of switch Q**330**a. The drain of switch Q**330**a connects to the drain of switch Q**32**. The drain of switch Q**310**b may provide the neutral (N) output terminal of converter **107**b/**107**c.

The neutral (N) point of converters **107**b/**107**c may connect to voltage terminal V**1** via switches SW**2**a (not shown) and SW**2**b and body diode of switch Q**31** and/or voltage terminal V**2** via switch SW**2**a, SW**2**b and switch Q**32**. Further, the neutral (N) point of converter **107**b/**107**c may connect to voltage terminal V**3** via the body diodes of switches Q**310**b and Q**330**a then through and Q**33** and/or voltage terminal V**4** via the body diodes of switches Q**310**b and Q**330**a and through switch Q**34**.

In a similar way, the live (L) point of converters **107**b/**107**c may connect to voltage terminal V**1** via switches SW**1**a (not shown) and SW**1**b and/or from voltage terminal V**2** via switch Q**320**a, switch Q**320**c and switch Q**320**d. Further, the live (L) point of converter **107**b/**107**c may connect to voltage terminal V**3** via switches Q**340**b, Q**340**c and Q**320**d and/or voltage terminal V**4** via switches Q**340**a, Q**340**c and Q**320**d. In sum, MUX **88** may allow the live (L) or neutral (N) inputs of MUX **88** to be selectively connected to terminals V**1**, V**2**, V**2**-V**3**, V**3** and V(n−1) via respective switches SW**1**b and SW**2**b.

Descriptions so far in general, and in greater detail in descriptions that follow, for converters may include cascade-able elements that are interchangeable in various combinations. For example, one or more outputs of one stage (e.g., a first converter) may be connected to one or more inputs of another stage (e.g., a second converter). Thus, for example, when A is cascaded with B, the outputs X and Y of A may be connected to the inputs of W and Z of B, respectively. The cascade-able elements may be configured for example to provide for the function of harmonic cancellation in a converter, reduce the occurrence of simultaneously high values of voltage and current. The reduction of simultaneously high values of voltage and current may therefore may reduce high-power dissipation values during the switching process. Additionally, the multi-level converter topologies described above and in descriptions that follow may provide multiple output voltage values. The multiple output voltage values may reduce the size of associated output filters, may minimize the number of switches utilized and enable the choice of switches that are cheaper.

Reference is now made to FIG. **1**H, which illustrates a generalized block diagram of further details of converter **107**, according to illustrative aspects of the disclosure. The generalized block diagram also includes generalized SIMLO converter **10**, MIMO converter **12** and selector unit **16**. SIMLO converter **10** may be implemented as SIMLO converters **10**a, **10**b, **10**c described above and below in the descriptions that follow. Similarly, MIMO converter **12** and selector unit **16** may be implemented respectively as MIMO converters **12***a*, **12***b*, **12***c* and selector units **16***a*, **16***b*, **16***c* described above and below in the descriptions that follow. MIMO converter **12** may comprise switching circuitry as shown in FIG. **1**H and other figures. In general, reference to SIMLO converter **10**, MIMO converter **12** and selector unit **16** is intended to include all the other embodiments of SIMLO converters, MIMO converters and selector units described above and below. Further, the embodiments described above and below for SIMLO converter **10**, MIMO converter **12** and selector unit **16** may be cascaded together in a variety of combinations. For example, a cascade of SIMLO converter **10***b*, MIMO converter **12***c* and selector unit **16***a* may be utilized in some embodiments.

As described above, voltage V_{DC} on terminals A and B may be the DC output of power system **100**. Voltage V_{DC} on terminals A and B may be another source of DC supply such as DC from a battery, DC generator, a photovoltaic panel or any other source of DC power. Voltage V_{DC} may have a negative terminal (V**0**) that may connect to neutral (N), earth or ground, or may not connect to neutral (N), earth or ground. In some aspects, negative terminal (V**0**) may be galvanically isolated from neutral (N) and/or earth. If the negative terminal of voltage V_{DC} is not connected to ground, voltage V_{DC} may be referred to as a floating voltage. V_{DC} as shown may be considered to be an example of a unipolar voltage. Voltage V_{DC} may also be a bipolar voltage so that the input to SIMLO converter **10** may have three inputs: $V_{DC}/2$, 0 and $-V_{DC}/2$ for example. Voltage V_{DC} may connect to the input of a single input multi-level output (SIMLO) converter **10**. The positive terminal of voltage V_{DC} may connect to the positive input of SIMLO converter **10** via inductor L**1**. SIMLO converter **10** may convert voltage V_{DC} to eight discrete voltage levels of DC output voltage respectively on eight output terminals V**1**-V**8** with respect to negative terminal V**0**. Eight output terminals V**1**-V**8** with respect to negative terminal V**0** of SIMLO converter **10** may connect to respective input terminals of multi input multiple output (MIMO) converter **12**.

MIMO converter **12** may convert the discrete voltage levels (V**1**-V**8**) on its input to two discrete states of voltage level on each of seven outputs O/P**1**-O/P**7**. For example, the two discrete states of voltage provided on output O/P**7** may be voltages V**7** and V**8**, the two discrete states of voltage on output O/P**6** may be voltages V**6** and V**7**. The outputs O/P**1**-O/P**7** may be summarized in Table 1 below.

TABLE 1

O/P1	O/P2	O/P3	O/P4	O/P5	O/P6	O/P7
V1 or V2	V2 or V3	V3 or V4	V4 or V5	V5 or V6	V6 or V7	V7 or V8

The two discrete values of voltage on each output (O/Pn, n=1-7) may alternate from one to each other by virtue of multiple pulse width modulation (PWM) signals from PWM unit **14**. The PWM signals may be applied to the control inputs of the switches (not shown) of MIMO converter **12**. The switches of MIMO converter **12** may provide two levels of voltage on each respective output O/P**1**-O/P**7** by virtue of the PWM applied by PWM unit **14**.

Controller **18** (e.g., control unit) may include two control line outputs and one input from reference waveform **19**. Control line output **18***a* connects to a control input of PWM unit **14** and control line output **18***b* connects to a control input of selector unit **16**. Control line output **14***a* connects to SIMLO convert **10** and control line **14***b* connects to MIMO converter **12**. Control lines **18***a* and/or **18***b* may be provided respectively to PWM unit **14** and/or selector unit **16**, responsive to parameters of reference waveform **19** and/or sensed parameters of converter **107**. Controller **18** may additionally include a PWM unit similar to that of PWM unit **14** and supply a PWM control signal to selector unit **16** via control signal **18***b*. In general, according to features described in greater detail below, the PWM supplied to SIMLO converter **10** and/or MIMO converter **12** may be at a higher frequency compared to the frequency of PWM that may be supplied to selector unit **16**.

Sensed parameters of converter **107** by sensors (not shown) may be included in control unit **18** or operatively connected to control unit **18**. Selector unit **16** may provide a single-phase output shown as terminals live (L) and neutral (N). Further details of converter **107** and its operation are shown in the descriptions that follow. In sum, converter **107** may include an input connected to DC voltage V_{DC} that may be converted by converter **107** to a single-phase AC output on terminals live (L) and neutral (N) for example. Additionally, the features described above and, in more detail, below for converter **107** may be repeatable and inter connected. Repeatable and interconnected features of converter **107** may provide, for example, a split phase and/or three phase AC output on output terminals of converter **107**.

Reference is now made to FIG. **1**I, which shows a block diagram of further details of control unit **18**, according to illustrative aspects of the disclosure. A controller **180** may include a microprocessor, microcontroller and/or digital signal processor (DSP) that may connect to a memory **189**. Controller **180** may serve as a central controller to other controllers that may be included in power devices **103** for example. Communications interface **182** connected to controller **180** may provide communications between controller **180** and other controllers/communication interfaces included in power system **100** for example. The communications to and from communications interface **182** may be as a result of a control algorithm running on controller **180**. The communications may include control signals provided on control lines **18***a* and **18***b* to control PWM unit **14** and/or selector unit **16**. Communications in communications interface **182** may also include measured or sensed parameters via sensors/sensor interface **184**. Sensors/sensor interface **184** may be included in and/or operably connected to SIMLO converter **10**, MIMO converter **12** and selector unit **16**. The communications by communications interface **182** may be conveyed by use of WiFi, power line communications (PLC), near field communications or RS232/485 communication bus, for example. Communications interface **182** may communicate with a local area network or cellular network in order to establish an internet connection that, for example, may provide a feature of remote monitoring/or reconfiguration of converter **107**.

Display **188** connected to central controller **180** may be mounted on the surface of the housing of converter **107** for example. Display **188** may display, for example, the power produced from converter **107** that may be utilized by load **109** that may be measured by sensors/sensor interface **184**.

Connected to controller **180** may be connected to safety and remote shutdown unit **186**. Sensing by sensors/sensor interface **184** as well as sensed parameters communicated between controller **180** and sensors/sensor interfaces of SIMLO converter **10**, MIMO converter **12** and selector unit **16** may be indicative of a fault condition. Upon detection of a fault, remote shutdown unit **186** may be activated in order to isolate the fault condition and/or shutdown converter **107**, for example.

Reference now made to FIG. **1**J, which shows a block diagram of further details of SIMLO converter **10***d*, MIMO converter **12***d* and selector unit **16***d*, according to illustrative aspects of the disclosure. Switches shown in SIMLO converter **10***d*, MIMO converter **12***d* and selector unit **16***d* are shown as metal oxide semiconductor field effect transistors (MOSFETs). Switches shown in SIMLO converter **10***d* may also include other solid-state semiconductor switches and/or electro-mechanical switches such as relays, for example. The cascaded series of stages in the processing chain of electrical powers and the further details SIMLO converter **10***d*, MIMO converter **12***d* and selector unit **16***d* may be utilized in converter **107** as shown in FIG. **1**A.

Voltage V_{DC} at nodes A and B connects to the input of a single input multi-level output (SIMLO) converter **10***d* via inductor L**1**. The other end of inductor L**1** connects to the point where two switches Q**1** and Q**2** are connected in series. The other ends of switches Q**1** and Q**2** connect respectively to terminal V**8** and one end of capacitor C**1**. The other end of capacitor C**1** connects to node B. Two series strings ST**1** and ST**2** of inductors connect between terminals V**8** and V**1** and/or node B. Using inductor L**11** as an example that may apply for each of the inductors in series strings ST**1** and ST**2**, inductor L**11** may include a switches Q**11***a* and Q**11***b* wired in series on either side of inductor L**11**. In a similar way, inductor L**12** may include a switches Q**12***a* and Q**12***b* wired in series on either side of inductor L**1**. Switch, Q**11***a* is wired in series with switch Q**13***b* and switch Q**12***a* is wired in series with switch Q**14***b*. The point where Q**11***a* is wired in series with switch Q**13***b* and switch Q**12***a* is wired in series with switch Q**14***b* may be further connected together to provide terminal V**6**. In a similar way, the point where Q**11***b* wired in series with switch Q**9***a* and switch Q**12***b* may be wired in series with switch Q**14***b* and these two series connections may be further connected provides terminal V**5**. The gate of switch Q**12***a* connects to terminal V**6** in a similar way that the gate of switch Q**10***a* connects to terminal V**5**. The gates of switches Q**11***a*, Q**11***b* and Q**12***b* may receive PWM from PWM unit **14** via control line output **14***a*.

Inductor L**11** and inductor L**12** as with the other inductor pairs may be both electrically connected together and also electro-magnetically connected together by virtue of the mutual inductance between inductor pairs of inductors L**11** and L**12**, L**15** and L**16** etc., being wound on the same core CR**1** that may run throughout the length of strings ST**1** and ST**2**. Inductor pairs may have the same number of winding turns, and each inductor pair may form what may be referred to as auto transformer circuits with primary windings (e.g., L**3**, L**5**, to L**15**) and secondary windings (L**4**, L**6**, to L**16**). There can be a different number of turns to each of the inductor pairs. The different number of turns may allow an adjustment of the typical relative maximum power point (MPP) voltage of each of the voltages on terminals V**1**-V**8**, for example. Additionally, with respect to inductors L**15** and L**16**, terminal V**7** also connects to capacitor C**1** where capacitor C**1** connects to switch Q**2**.

SIMLO converter **10***d* may be provided with a circuit for a separating of direct current (DC) input power (V_{DC}). The separating may provide multiple direct current (DC) voltage outputs on terminals V**1**-V**8** by use of multiple tapped inductors. Tapped inductors may include respective primary ends, secondary ends and taps connected to terminals V**1**-V**8**. The taps provided between a series connection of inductors (L**13** and L**11**, or L**14** and L**12** for example) and between two series connected switches (Q**13***b* and Q**11***a*, or Q**14***b* and Q**12***a* for example). The taps may be adapted for connecting individually to the DC voltage outputs (terminals V**1**-V**8**). Each tapped inductor may form a switched auto transformer circuit with both electrical and electro-magnetic connections. The electrical and electro-magnetic connections may be operated so that multiple direct current (DC) voltage outputs may be provided on terminals V**1**-V**8**. The multiple direct current (DC) voltage outputs may be derived from converting the input voltage (V_{DC}) by SIMLO converter **10***d*. Operation and control of the switched auto transformer circuits may include control signal **14***b* from PWM unit **14**, for example.

The single input multi-level output SIMLO converter **10***d* via inductor L**1**, where L**1** connects to the point where two switches Q**1** and Q**2** may be connected in series. The other ends of switches Q**1** and Q**2** connected to the auto transformer circuits may provide a way of operation to the input of SIMLO converter **10***d*. A central controller (not shown) such as controller **180**, for example, may sense electrical parameters in power system **100** and/or converter **107***d* to operate switches Q**1** and Q**2** and/or the auto transformer circuits. The way of operation therefore may be to provide a buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC} that may be the DC output of power system **100** for example. The electrical parameters sensed by sensors/sensor interface **184** for example may be voltage, current, impedance, resistance, phase angle, power factor, level of harmonic distortion, frequency or power. Control line output **14***a* may be used send control signals to SIMLO converter **10** to provide appropriate control of SIMLO converter **10** responsive to the sensed electrical parameters.

Two switches Q**8***a* and Q**8***b* connected in series across capacitor C**8** at nodes X and Y may present an input to a two-level inverter topology to the DC potential difference between terminals V**8** and V**7** applied to the input. The alternating current (AC) output O/P**7** of the two-level inverter topology may be derived from the mid-point connection between switches Q**8***a* and Q**8***b*. A three-level and/or multilevel inverter topology may be implemented to provide an input between nodes X and Y so that alternating current (AC) output O/P**7** may be a three-level and/or multilevel AC voltage.

Seven voltages or more may be output from SIMLO converter **10***d* to the input of MIMO converter **12***d*, i.e., the seventh voltage is the potential difference between output terminals V**7** and V**8**, the sixth voltage is the potential difference between output terminals V**7** and V**8** and so on.

Capacitor C**2** connects across terminals V**1** and V**2** and capacitors C**3**-C**8** connect across respective terminals, such that C**3** connects across terminals V**2** and V**3** and so on. By way of example using capacitor C**8** for all other capacitors C**2**-C**7**, two switches Q**8***a* and Q**8***b* connect in series across capacitor C**8**. The mid-point connection between switches Q**8***a* and Q**8***b* provides output O/P**7** of MIMO converter **12***d*. The mid-point connection between switches Q**5***a* and Q**5***b* may provide the neutral (N) connection point output of MIMO converter **12***d* and the neutral (N) output terminal of converter **107***d*/selection unit **16***d*. Selection unit **16***d* may comprise a plurality of interconnected switches (e.g., Q**9***a*, Q**9***b*, Q**10***b*, Q**11***a*, Q**11***b*, Q**11***c*, etc.) configured to output an output voltage on a selected output terminal. The mid-point connection between switches Q**5***a* and Q**5***b* may provide a symmetrical output of converter **107**/selection unit **16** that may provide for the function of harmonic cancellation in converter **107**. The other mid-point connections between the switches MIMO converter **12***d* in general also may serve to provide the neutral (N) connection point output of MIMO converter **12***d* and the neutral (N) output terminal of converter **107***d*/selection unit **16***d*. The gates of switches Q**8***a* and Q**8***b* as with the gates of the other switches of MIMO converter **12***d* may receive PWM from PWM unit **14** via control line output **14***b*.

The seven voltages output from MIMO converter **12***d* on outputs O/P**1**-O/P**7** may be input into respective inputs of selection unit **16***d* as shown. The switches of selection unit **16***d* may be connected and operated to provide two main paths P**1** and P**2** (shown by dotted line and arrow) that connect to the output of selector unit **16** via inductor L**2**. Inductor (filter) L**2** may provide a filtering of the AC voltages provided from paths P**1** and/or P**2**.

Path P**1** may be supplied from sub paths P**1***a* and/or P**1***b* and path P**2** may be supplied by sub paths P**2***a* and/or P**2***b*. Selection by selection unit **16***d* of the paths may be by the PWM supplied to selection unit **16***d*. The PWM may be at a lower frequency compared to the frequency of PWM that may be supplied to SIMLO converter **10***d* and/or MIMO converter **12***d*. As mentioned previously, MIMO converter **12***d* may convert the discrete voltage levels (V**1**-V**8**) on its input to two discrete states of voltage level on seven outputs O/P**1**-O/P**7**.

By way of non-limiting example, reference is made to path P**2**, which may be supplied from outputs O/P**7**, O/P**6**, O/P**5** or O/P**4**. If output O/P**7** is required to appear on the output of selector unit **16***d*, PWM may be applied to the gates of switches Q**9***a*, Q**10***a*, Q**10***b* to provide sub path P**2***b*. PWM applied to the gates of switches Q**11***a*, Q**11***b* and Q**11***c* to provide path P**2** while all other switches in selector unit **16***d* are OFF. Similarly, if output O/P**6** is required to appear on the output of selector unit **16***d*, PWM may be applied to the gates of switches Q**9***b*, Q**10***a*, Q**10***b* to provide sub path P**2***b*. PWM applied to switches Q**11***a*, Q**11***b* and Q**11***c* to provide path P**2** while all other switches in selector unit **16***d* are OFF. Path P**2** may be supplied by sub path P**2***a* by operation of switches connected to outputs O/P**5** and O/P**4** in a similar way as with respect to outputs O/P**6** and O/P**7** described above. Path P**1** may also supplied from outputs O/P**3**, O/P**2** and/or O/P**1** similar as that described with respect path P**2** described above.

Reference is now made to FIG. **2**A, which shows a flow chart of an example method **201** for the operation of converter **107***d*. The flow chart of method **201** may be used in general to describe the operation of interconnected and/or cascaded components of converter **107**. Steps **202**, **204**, **206**, **208**, and **210** of method **201** may be considered to be operating at substantially the same time by virtue of the cascaded stages in the processing chain of electrical powers converted by SIMLO converter **10**/MIMO converter **12** and selected by selector unit **16**.

Operation of SIMLO Converter **10***d*

At step **202**, voltage V_{DC} applied at the input of SIMLO converter **10***d* may be converted to provide multiple direct current (DC) voltage outputs on terminals V**1**-V**8**. In other words, SIMLO converter **10***d* may be a circuit for separating a direct current (DC) input power (V_{DC} for example) to provide multiple direct current (DC) voltage outputs on its output terminals V**1**-V**8**.

As part of what may be included in step **210**, controller **180** as an example of a central controller may sense electrical parameters in power system **100** and/or converter **107**/**107***d* at step **208**. Step **210** includes operation of switches Q**1** and Q**2** connected to inductor L**1** and capacitor C**1** and/or the auto transformer circuits. The auto transformer circuits may for example include inductor pairs of inductors such as L**15** and L**16** and four switches Q**15***a*, Q**15***b*, Q**16***a* and Q**16***b* to give a converter circuit function. The converter circuit provides may be a buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC}. Alternatively, converter **1000** may be utilized instead of or in addition to the auto transformer circuits to provide a buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC}. The electrical parameters sensed by sensors/sensor interface **184**, for example, may be voltage, current, impedance, resistance and/or power (P). Power P may be a calculation using sensed voltage (V) multiplied (x) by sensed current (I). The calculation performed by controller **180**, for example. Control line output **14***a* may be used to send control signals to SIMLO converter **10***d* for appropriate control of SIMLO converter **10***d* to provide a buck function on voltage V_{DC}. The buck function on voltage V_{DC} may be to step down the voltage level of voltage V_{DC} if too high whilst stepping up the input current from voltage V_{DC} responsive to the sensed electrical parameters. Whereas in contrast, a boost function on voltage V_{DC} may step up the voltage level if V_{DC} is too low whilst stepping down the input current from voltage V_{DC} responsive to the sensed electrical parameters. Responsive to the electrical parameters sensed by sensors/sensor interface **184**, configuration of inductor pairs and switches may provide where appropriate the buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC}.

Control signals provided on control line output **14***a* may also include control signals with respect to the operation of the auto transformer circuits. The operation may provide multiple direct current (DC) voltage outputs on the output terminals V**1**-V**8** of SIMO converter **10***d*. Operation of the auto transformer circuits by use of multiple tapped inductors of the auto transformer circuits may include respective primary ends, secondary ends and taps connected to terminals V**1**-V**8**. The taps provided between a series connection of inductors may be L**13** and L**11**, or L**14** and L**12** and between two series connected switches may be switches Q**13***b* and Q**11***a*, or Q**14***b* and Q**12***a*, for example. The taps may be adapted for connecting individually to the DC voltage outputs (terminals V**1**-V**8**). Each tapped inductor therefore may form a switched auto transformer circuit with both electrical and electro-magnetic connections. The switched auto transformer circuit may be operated so that multiple direct current (DC) voltage outputs may be provided on terminals V**1**-V**8**. The voltage outputs may be derived from converting the input voltage (V_{DC}) by SIMLO converter **10***d*.

Control signals on control line output **14***a* may be by a first modulation scheme responsive to the electrical parameters sensed at step **208**. The first modulation scheme may include pulse width modulation (PWM), frequency modulation (FM) or a variable frequency and variable pulse width. Control signals on control line output **14***a* may include consideration of reference waveform **19** and the effect of a load connected to the output of selector unit **16**. The control signals may be responsive to sensing step **208** so that the DC voltage outputs on terminals V**1**-V**8** may be set and maintained at the required DC levels. PWM from PWM unit **14** may be applied to the gate connections of the switches of SIMLO converter **10***d* via control line output **14***a*.

Operation of MIMO Converter **12***d*

At step **204**, MIMO converter **12***d* may convert the discrete voltage levels (V**1**-V**8**) on its input to two discrete states of alternating current (AC) voltage level on each of seven outputs O/P**1**-O/P**7**. The switches of MIMO converter **12***d* may provide two levels of voltage on each respective output O/P**1**-O/P**7**. Two levels of voltage on each respective output O/P**1**-O/P**7** may be by virtue of the PWM applied by PWM unit **14** on control line output **14***b* to the gates of the switches of MIMO converter **12***d*. The PWM on control line output **14***b* may be provided by controller **180** (as part of control step **210**) responsive to sensed electrical parameters of converter **107**/**107***d* at step **208**. The sensed electrical parameters of converter **107** may include the discrete voltage levels (V**1**-V**8**) and the effect of a load connected to the output of selector unit **16**. The sensed electrical parameters of converter **107** may further include consideration of reference waveform **19**.

For example, the two discrete states of voltage provided on output O/P**7** may be voltages V**7** and V**8**, the two discrete states of voltage on output O/P**6** may be voltages V**6** and V**7**. The outputs O/P**1**-O/P**7** may be summarized as shown in Table 1 above. By way of example, two switches Q**8***a* and Q**8***b* connected in series across capacitor C**8** at nodes X and Y may present an input to a two-level inverter topology. The DC potential difference between terminals V**8** and V**7** applied to the input of the two-level inverter topology. The alternating current (AC) output O/P**7** of the two-level inverter topology may be derived from the mid-point connection between switches Q**8***a* and Q**8***b*. A three-level and/or multilevel inverter topology may be implemented to provide an input between nodes X and Y. Therefore, alternating current (AC) output O/P**7** may be a three-level and/or multilevel AC voltage.

Operation of Selection Unit **16***d*

At step **206**, the seven voltages output from MIMO converter **12***d* on outputs O/P**1**-O/P**7** may be input into respective inputs of selection unit **16***d*. Referring again to FIG. **1**J, the switches of selection unit **16***d* may be connected and operated to provide two main paths P**1** and P**2** (shown by dotted line and arrow). Paths P**1** and P**2** connect to the output of selector unit **16***d* via inductor L**2**. Inductor (filter) L**2** may provide a filtering of the AC voltages provided from paths P**1** and/or P**2**. Path P**1** may be supplied from sub paths P**1***a* and/or P**1***b* and path P**2** may be supplied by sub paths P**2***a* and/or P**2***b*. Selection by selection unit **16** of the paths may be the PWM supplied to selection unit **16***d*. The PWM may be at a lower frequency compared to the frequency of PWM that may be supplied to SIMLO converter **10***d* and/or MIMO converter **12***d*.

By way of non-limiting example, reference is made to path P**2** that may be supplied from outputs O/P**7**, O/P**6**, O/P**5** or O/P**4**. If output O/P**7** is required to appear on the output of selector unit **16***d*, PWM may be applied to switches Q**9***a*, Q**10***a*, Q**10***b* to provide sub path P**2***b*. PWM applied to switches Q**11***a*, Q**11***b* and Q**11***c* to provide path P**2** while all other switches in selector unit **16***d* are OFF. Similarly, if O/P**6** is required to appear on the output of selector unit **16***d*, PWM may be applied to switches Q**9***b*, Q**10***a*, Q**10***b* to provide sub path P**2***b*. PWM applied to switches Q**11***a*, Q**11***b* and Q**11***c* to provide path P**2** while all other switches in selector unit **16***d* are OFF. Path P**2** may be supplied by sub path P**2***a* by operation of switches connected to outputs O/P**5** and O/P**4**. In a similar way, P**2** may be supplied by sub path P**2***b* by operation of switches connected to outputs O/P**6** and O/P**7** described above. Path P**1** may also supplied from outputs O/P**3**, O/P**2** and/or O/P**1** similar as that described with respect path P**2** described above.

Reference is now made to FIG. **2**B, which shows graphical waveforms to illustrate the operation of converter **107** *d*, according to illustrative aspects of the disclosure. Waveforms are shown with horizontal axis of time (no numerical values specified) versus voltage on the vertical axis (no units specified). Reference waveform **19** is shown as a sinewave by dotted line. Reference waveform **19** may be a sinewave, triangular wave, square wave or any periodic waveform. Reference waveform **19** may be considered to be representative of the desired output of converter **107** *d*. Control signals on control lines **18***a* and/or **18***b* may be provided respectively to PWM unit **14** and selector unit **16***d*. Control signals on control lines **14***a* and **14***b* may be provided respectively to SIMLO converter **10***d* and MIMO converter **12***d* responsive to parameters of reference waveform **19** and/or sensed parameters of converter **107** *d*.

The parameters of reference waveform **19** may include the desired voltage amplitude and frequency of the output from converter **107** *d*. For example, where load **109** may be a utility grid or single-phase AC motor, the desired voltage and frequency may be 220 Volts (V) and 50 Hertz (Hz) respectively. Electrical parameters sensed by sensors/sensor interface **184** and appropriate signals on control lines **18***a*, **18***b*, **14***a* and **14***b* may provide appropriate control of converter **107** *d*. Appropriate control of converter **107** *d* may be to ensure correct levels of operating voltage, current, impedance, resistance, phase angle, power factor, level of harmonic distortion, frequency and/or power for example.

Referring back to FIG. **2**A, at step **202**, voltage V_{DC} applied at the input of SIMLO converter **10***d* may be converted to provide multiple direct current (DC) voltage outputs on terminals V**1**-V**8**. Voltage outputs V**1**-V**8** may be shown by the horizontal lines of the shaded rectangles that represent the outputs from MIMO converter **12***d* on outputs O/P**1**-O/P**7** provided at step **204**. By way of example, referring to output O/P**7**, the two discrete states of voltage provided on output O/P**7** may be voltages V**7** and V**8**. Output O/P**7** being voltages V**7** and V**8** may be because MIMO converter **12***d*, in general, may convert the discrete voltage levels (V**1**-V**8**) on its input to two discrete states of AC voltage. The two discrete states may be provided on each of seven outputs O/P**1**-O/P**7**. The PWM used to drive both converters **10***d* and/or **12***d* in general may be much higher in frequency than PWM control signal **20** applied to selection unit **16**.

During time period T**7** of PWM control signal **20**, output O/P**7** switches between levels V**8** and V**7** many times during time period T**7**. During time period T**7**, referring again to FIG. **1**J, PWM control signals **20** may be applied to switches Q**9***a*, Q**10***a*, Q**10***b*. PWM control signals may provide sub path P**2***b*. PWM control signal **20** applied to switches Q**11***a*, Q**11***b* and Q**11***c* to provide path P**2** while all other switches in selector unit **16***d* are OFF. All other switches in selector unit **16***d* OFF means that the two discrete states of AC voltage provided on output O/P**7** appears on the output of converter **107** *d*.

In a similar way, PWM control signals **20** may be applied to switches Q**9***b*, Q**10***a*, Q**10***b* to provide sub path P**2***b*. PWM control signal **20** applied to switches Q**11***a*, Q**11***b* and Q**11***c* to provide path P**2** while all other switches in selector unit **16***d* are OFF. All other switches in selector unit **16***d* are OFF so that the two discrete states of AC voltage provided on output O/P**6** appears on the output of converter **107** *d*. PWM control signal **20** may be the PWM signal applied to selector unit **16***d* via control line **18***b*. PWM signal applied to selector unit **16***d* may be to select which outputs O/P**1**-O/P**7** appear on the output of converter **107** *d* as part of step **206**. PWM control signal **20** may be applied to selection unit **16***d* included in control step **210** responsive to reference signal **19** and/or sensed parameters of converter **107** *d* at step **208**.

Reference is now made to FIG. **2**C, which illustrates a block diagram of a converter **207**, according to illustrative aspects of the disclosure. Converter **207** is the same as converter **107** shown in FIG. **1**H but with the addition of a junction box **25**, generator **20** and rotary switch **26**. Further reference is also made to FIG. **2**D, which shows a partial plan view of rotary switch **26** that includes some of poles P**1**-P**7** (poles not shown are represented by dashed line). Generator **20** may be rotated (shown by rotation **24**) by a turbine, for example, so that generator **20** generates electricity as a single-phase supply on live L_{20} and neutral N_{20}. Generator **20** may also generate a three-phase supply of electricity. The single-phase supply on live L_{20} and neutral N_{20} may connect to the single-phase supply provided on live L and neutral N of rotary switch **26** and/or the single-phase supply provided on live L and neutral N of selector unit **16**. Specifically, converter **207** according to descriptions below may provide a combined and synchronized single phase outputs from generator **20** and rotary switch **26**, when rotary switch **26** is used instead of selector unit **16**. The combined and synchronized single phase outputs may be by virtue of rotation **24** of the rotor of generator **20** to provide a way to synchronize the AC of converter **207** (at the output of MIMO converter **12**) to the AC generated by generator **20**.

In general, converter **207** may be operated to include the single-phase output of selector unit **16** as described above, the single-phase output of generator **20** or the combined and synchronized single phase outputs from generator **20** and rotary switch **26**.

A possible electro-mechanical implementation of selector unit **16** described above may be to use rotary switch **26** with terminals/poles P**1**-P**7** connectable to the output terminals of MIMO converter **12** by way of junction box **25** and multi-core cable **27**. A pole of rotary switch **26** may provide the AC output voltage similar to that of selector unit **16** responsive to the velocity of rotation **24** of a rotor/shaft of rotary switch **26**. The rotation **24** of a rotor of rotary switch **26** may be used to implement an electro-mechanical equivalent of PWM control signal **20**, where time T**7** and corresponding arc length for the pole of output O/P**7** is greater than the corresponding arc length for the pole of output O/P**6** for example. The physical arc length of poles P**1**-P**7** of rotary switch **26** may allow for more and/or less time for an output of the output terminals of MIMO converter **12** to be ON. Poles P**1**-P**7** of rotary switch **26** are connected to outputs of MIMO converter **12** on its outputs O/P**1**-O/P**7** in junction box **25**. Therefore, converter **207** may be operated to include the single-phase output of selector unit **16** as described above, the single-phase output of generator **20** or the combined and synchronized single phase outputs from generator **20** and rotary switch **26**.

The rotor of rotary switch **26** may be rotated so that rotation **24** may be at three thousand revs per minute (RPM), for example. Three thousand revolutions per minute (RPM) may be derived from the following equation for generator **20** with n=two poles at a frequency f=50 Hz:

$$\text{speed}(RPM) = \frac{60 \times f}{n}$$

Speed of three thousand revolutions per minute (RPM) gives a frequency output of 50 Hertz (Hz) for the AC output voltage of rotary switch **26**. Rotation **24** of the rotor of generator **20** may provide a way to synchronize the AC of MIMO converter **12** to the AC generated by generator **20** on live Lao and neutral N_{20}. Therefore, a combined and synchronized single phase outputs from generator **20** and rotary switch **26** may be achieved when rotary switch **26** is used instead of selector unit **16** to provide an electro-mechanical equivalent of PWM control signal **20**.

Reference now made to FIG. **3**A, which shows a block diagram of further details of SIMLO converter **10***e*, MIMO converter **12***e* and selector unit **16***e*, according to illustrative aspects of the disclosure. Switches shown in SIMLO converter **10***e*, MIMO converter **12***e* and selector unit **16***e* may be shown as metal oxide semiconductor field effect transistors (MOSFETs). Switches may also include other solid-state semiconductor switches and/or mechanical switches. The cascaded connection of the further details SIMLO converter **10***e*, MIMO converter **12***e* and selector unit **16***e* may be one of many implementations that may be utilized to implement converter **107** shown in FIG. **1**A. The further details SIMLO converter **10***e*, MIMO converter **12***e* and selector unit **16***e* may be considered to have both some similar and dissimilar component implementations and/or functions of respective SIMLO converter **10**, MIMO converter **12** and selector unit **16** shown in FIG. **1**J. Similar components and are given the same reference number in the description below.

The positive terminal of voltage V_{DC} may connect to the positive input of SIMLO converter **10***e* via inductor L**1**. SIMLO converter **10***e* may convert voltage V_{DC} to seven discrete voltage levels of DC output voltage respectively on eight output terminals V**1**-V**8** with respect to negative terminal V**0**. The other end of inductor L**1** connects to the point where two switches Q**1** and Q**2** are connected in series. The other ends of switches Q**1** and Q**2** connect respectively to terminal V**8** and one end of capacitor C**1**. The other end of capacitor C**1** connects to node B.

Series string ST**1** may include a series string of inductors connected between terminals V**8** and V**1** and/or node B. Using inductor L**11** as an example that may apply for each of the inductors in series string ST**1**, inductor L**11** may include switches Q**11***a* and Q**11***b* wired in series on either side of inductor L**11**. In a similar way, inductor L**9** may include switches Q**9***a* and Q**9***b* wired in series on either side of inductor L**9**. The inductors in series string ST**1** may be wound around core CR**1**. The connection between switches Q**13***b* and Q**11***a* provide voltage terminal V**6** and in a similar way the connection between switches Q**11***b* and Q**9***a* provide voltage terminal V**5**. A further feature similar to that shown in FIG. **1**J, inductor L**15** is connected in parallel across inductor L**16** and via switches Q**16***a* and Q**16***b* wired in series with inductor L**16**. Inductor L**15** may also electro-magnetically coupled to inductor L**16** by virtue of inductor L**16** also wound on core CR**1**. In sum, series string ST**1** forms an auto transformer between terminals V**8** and V**1**. The auto transformer may include an inductor pair of inductors L**15** and L**16** and four switches Q**15***a*, Q**15***b*, Q**16***a* and Q**16***b*. The auto transformer may provide a buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC}. Alternatively, converter **1000** may be utilized instead or in addition to the auto transformer circuits. Converter **1000** may therefore, provide a buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC}. Gates of switches Q**15***a* and Q**16***a* may be connected terminal V**8** and the gate of switch Q**13***a* connects to terminal V**7**. All other gates of the remaining switches of SIMLO converter **10***e* may connect to control line **14***a* of PWM unit **14**.

In MIMO converter **12***e*, capacitor C**2** connects across terminals V**1** and V**2**. Capacitors C**3**-C**8** connect across respective terminals, such that C**3** connects across terminals

V2 and V3, C4 connects across terminals V3 and V4 and so on. Two switches Q8*a* and Q8*b* connect in series across capacitor C8. The mid-point connection between switches Q8*a* and Q8*b* provides output to inductor L2 of selection unit 16*e*. The switching of switches Q8*a* and Q8*b* at the point where switches connected together provides two discrete states of voltage level (V8 and V7) to inductor L2 of selection unit 16*e*. Capacitors C7, C6 and C5 do not have two series connected switches across them.

The point at which the drain of switch Q34 connects to the connection between capacitor C4 and C5 is also connected to the drain of switch Q340*a* of MIMO converter 12*e*. The point may provide (depending of the switching of the switches in MIMO converter 12*e* and selection unit 16*e*) discrete voltages V4-V7. Switches Q340*a*, Q340*c* and Q340*d* may be included in multiplexor 88*a*. The source of switch Q34 connects to the drain of switch Q33 that further connects to the drain of switch Q330*a* that is included in selection unit 16*e*. The point at which the source of switch Q33 connects to the connection between capacitor C3 and C4 is also connected to the source of switch Q340*b* of MIMO converter 12*e*. The point may provide (depending of the switching of the switches in MIMO converter 12*e* and selection unit 16*e*) discrete voltages V3-V4. The drain of switch Q33 connects to the drain of switch Q330*a* of MIMO converter 12*e*. The point at which the drain of switch Q32 connects to the connection between capacitor C2 and C3 is also connected to the drain of switch Q320*a* of MIMO converter 12*e*. The point may provide, depending of the switching of the switches in MIMO converter 12*e* and selection unit 16*e*, discrete voltages V2-V3. The source of switch Q32 connects to the drain of switch Q31. The source of switch Q31 connects to the source of switch of 320*b* of MIMO converter 12*e* to provide discrete voltages V1-V2. Provision of discrete voltages V1-V2 may be dependent on the switching of the switches in MIMO converter 12*e* and selection unit 16*e*. The drain of switch Q31 also connects to the source of switch Q310*a*.

In selection unit 16*e*, the other end of inductor L2 connects to the drains of switch SW1*a* and switch SW2*a*. Both switches SW1*a* and SW2*a* include multiple switches connected between respective sources and drains. In descriptions that follow, multiple switches wired in series such as switches Q340*c*, Q330*a*, and Q310*a* for example may be implemented with a single switch. The source of switch SW1*a* provides the live (L) output terminal of converter 107*e* and is further connected to the drain of switch SW1*b*/Q320*d*. The source of switch SW2*a* provides the neutral (N) output terminal of converter 107*e* and is further connected to the drain of switch SW2*b*/Q310*b*. Switch SW1*b* may include switches Q320*b*, Q320*c* and Q320*d*. The source of switch Q320*b* connects to the source of switch Q31 of MIMO converter 12*e*. The drain of switch Q320*b* connects to the source of switch Q320*c* and the source of switch Q320*a*. The drain of switch Q320*a* connects to the drain of switch Q32 of MIMO converter 12*e*. The drain of switch Q320*c* connects to the source of switch Q320*d* and to the source of switch Q340*c*. The drain of switch Q340*c* connects to the drain of switch Q340*b* and the source of switch Q340*a*. The drain of switch Q340*a* connects to the drain of switch Q34 of MIMO converter 12*e*. The source of switch Q340*b* connects to the source of switch Q33 of MIMO converter 12*e*. Switch SW2*b* may include switches Q310*a* where the drain of switch Q310*a* wired in series with the source switch Q310*b*. The point at which the drain of switch Q310*a* connects with the source switch Q310*b* also connects to the source of switch Q330*a*. The drain of switch Q330*a* connects to the drain of switch Q32 of MIMO converter 12*e*. The drain of switch Q310*b* may provide the neutral (N) output terminal of converter 107*e*/selection unit 16*e*.

Operation of SIMLO Converter 10*e*

Reference is now made again to method 201, at step 202 voltage V_{DC} applied at the input of SIMLO converter 10*e*. Voltage V_{DC} may be converted to provide multiple direct current (DC) voltage outputs on terminals V1-V8. In other words, SIMLO converter 10 may be a circuit for separating a direct current (DC) input power (V_{DC} for example) to provide multiple direct current (DC) voltage outputs on its output terminals V1-V8.

As part of what may be included in step 210, controller 180 as an example of a central controller may sense electrical parameters in power system 100 and/or converter/107*e* at step 208. Step 210 may operate switches Q1 and Q2 connected to inductor L1 and capacitor C1 and/or the auto transformer circuit included series string ST1. The auto transformer circuit may for example include an inductor pair of inductors such as L15 and L16 and four switches Q15*a*, Q15*b*, Q16*a* and Q16*b*. The auto transformer circuit may therefore, provide a buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC}. Alternatively, converter 1000 may be utilized instead or in addition to the auto transformer circuits to provide a buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC}. The electrical parameters sensed by sensors/sensor interface 184 for example may be voltage, current, impedance, resistance and/or power (P). The power P may be a calculation of sensed voltage (V) multiplied (x) by sensed current (I) performed by controller 180. Control line output 14*a* may be used to send control signals to SIMLO converter 10*e* for appropriate control of SIMLO converter 10*e* to provide a buck function on voltage V_{DC}. The buck function on voltage V_{DC} may be to step down the voltage level of voltage V_{DC} if too high whilst stepping up the input current from voltage V_{DC} responsive to the sensed electrical parameters. Whereas in contrast, a boost function on voltage V_{DC} may step up the voltage level if V_{DC} is too low whilst stepping down the input current from voltage V_{DC} responsive to the sensed electrical parameters.

Control signals provided on control line output 14*a* may also include control signals with respect to the operation of the auto transformer circuit. The auto transformer circuit may include inductors L3-L13 to provide multiple direct current (DC) voltage outputs on the output terminals V1-V7 of SIMO converter 10*e*. Operation of the auto transformer circuit by use of multiple tapped inductors of the auto transformer circuit that may include switches Q3*b*-Q13*a*. The taps may be adapted for connecting individually to the DC voltage input to (terminals V1-V8). Each tapped inductor therefore may form a switched auto transformer circuit with both electrical and/or electro-magnetic connections (in the case of inductors L15 and L16). The electrical and/or electro-magnetic connections may be operated so that multiple direct current (DC) voltage outputs derived from converting the input voltage (V_{DC}) by SIMLO converter 10*e* are provided on terminals V1-V8. The inductor pair of L15 and L16 may have the same number of winding turns. There may also be a different number of turns to the inductor pair of L15 and L16. The different number of turns may provide a way to adjust the typical relative maximum power point (MPP) voltage of each of the voltages on terminals V1-V8.

Control signals on control line output 14*a* may be by a first modulation scheme responsive to the electrical parameters sensed at step 208. The first modulation scheme may include pulse width modulation (PWM), frequency modulation (FM) or a variable frequency and variable pulse width. Control signals on control line output **14***a* may include consideration of reference waveform **19** and the effect of a load connected to the output of selector unit **16***e*. The control signals may be responsive to sensing step **208** so that the DC voltage outputs on terminals V**1**-V**8** may be set and maintained at the required DC levels. PWM from PWM unit **14** may be applied to the gate connections of the switches of SIMLO converter **10***e* via control line output **14***a*.

Operation of MIMO Converter **12***e* and Selection Unit **16***e*

At step **204**, MIMO converter **12***e* may convert some of the discrete voltage levels (V**1**-V**8**) on its input to two discrete states of alternating current (AC) voltage levels on the five outputs of MIMO converter **12***e* (OP**1***a*-OP**5***a*). Unlike MIMO converter **12***d*, the five outputs (OP**1***a*-OP**5***a*) of MIMO converter **12***e* may have DC sources that have different potential difference values or unequal voltage amplitude values. For example, the potential difference of two discrete voltage levels between output OP**4***a* (V**4**-V**3**) may be greater than the potential difference the two discrete voltage levels of output OP**5***a* (V**7**-V**8**). When MIMO converter **12***e* is used in conjunction with selection unit **16***e* in steps **204** and **206** to choose unequal dc sources, some switching-state redundancies may be avoided. Consequently, different output-voltage levels may be generated with substantially the same number of switches and/or less switches.

When MIMO converter **12***e* is used in conjunction with selection unit **16***e* in order to realize steps **204** and **206**, switches Q**8***a* and Q**8***b* connect in series across capacitor C**8** at nodes X and Y. Nodes X and Y present an input to a two-level inverter topology to the DC potential difference between terminals V**8** and V**7** applied to the input. The alternating current (AC) output of the two-level inverter topology (V**8**-V**7**) may be derived from the mid-point connection between switches Q**8***a* and Q**8***b*. The mid-point connection connects to inductor L**2** of selection unit **16***e*. Similar two-level inverter topologies may exist between the other switches of MIMO converter **12***e*, for example between switches Q**34** and Q**33**, Q**33** and Q**32**, Q**32** and Q**31**. The switches of selection unit **16***e* may be used to enable outputs of the two-level inverter topologies selectable by the switches of selection unit **16***e*. For example, the live (L) connection point of converter **107***e* may be provided from the mid-point connection between switches Q**8***a* and Q**8***b*. The mid-point connection connects to inductor L**2** of selection unit **16***e*, through inductor L**2** and switch SW**1***a* to the live (L) connection point of converter **107***e* as discrete voltage levels V**7** and V**8**. The operation of the other switches in selection unit **16***e* may also provide the live (L) connection point of converter **107***e*. The live (L) connection point may be provided from discrete voltage levels V**1**-V**2**, V**2**-V**3**, V**3**-V**4** and/or V**4**-V**7**.

The neutral (N) point of converter **107***e* may connect to voltage terminal V**1** via switches SW**2***a* and SW**2***b* of selection unit **16***e* and body diode of switch Q**31**. The neutral (N) point of converter **107***e* may connect to and/or voltage terminal V**2** via switch SW**2***a* and SW**2***b* of selection unit and switch Q**32**. Further, the neutral (N) point of converter **107***e* may connect to voltage terminal V**3** via the body diodes of switches Q**310***b* and Q**330***a* then through and Q**33** and/or voltage terminal V**4** via the body diodes of switches Q**310***b* and Q**330***a* and through switch Q**34**. The PWM on control line output **14***b* may be provided by controller **180** (as part of control step **210**) responsive to sensed electrical parameters of converter **107***e* at step **208**. The sensed electrical parameters of converter **107***e* may include the discrete voltage levels (V**1**-V**8**). The effect of a load connected to the output of selector unit **16***e* and may further include consideration of reference waveform **19**. In a similar way the live (L) point of converters **107***b*/**107***c* may connect to voltage terminal V**1** via switches SW**1***a* (not shown) and SW**1***b* and/or from voltage terminal V**2** via switch Q**320***a*, switch Q**320***c* and switch Q**320***d*. Further, the live (L) point of converter **107***b*/**107***c* may connect to voltage terminal V**3** via switches Q**340***b*, Q**340***c* and Q**320***d* and/or voltage terminal V**4** via switches Q**340***a*, Q**340***c* and Q**320***d*.

Reference is now made to FIG. **3**B, which shows a possible waveform of the live (L) voltage output of selection unit **16***e* with respect to neutral (N), according to illustrative aspects of the disclosure. Waveforms may be shown with horizontal axis of time (no units specified) versus voltage on the vertical axis (no numerical values specified). Reference waveform **19** is shown as a sinewave by dotted line. Reference waveform **19** may be a sinewave, triangular wave, square wave or any periodic waveform. Reference waveform **19** may be considered to be representative of the desired output of converter **107***e*/selection unit **16***e*. Control signals on control lines **18***a* and/or **18***b* may be provided respectively to PWM unit **14** and selector unit **16***e*. Control signals on control lines **14***a* and **14***b* may be provided respectively to SIMLO converter **10***e* and MIMO converter **12***e* responsive to parameters of reference waveform **19** and/or sensed parameters of converter **107***e*.

The parameters of reference waveform **19** may include the desired voltage amplitude and frequency of the output from converter **107***e*. For example, where load **109** may be a utility grid or single-phase AC motor, the desired voltage and frequency may be 220 Volts (V) and 50 Hertz (Hz) respectively. Electrical parameters sensed by sensors/sensor interface **184** and appropriate signals on control lines **18***a*, **18***b*, **14***a* and **14***b* may provide appropriate control of converter **107***e* realized by SIMLO converter **10***e*, MIMO converter **12***e* and selection unit **16***e*. Signals on control lines **18***a*, **18***b*, **14***a* and **14***b* may ensure correct levels of operating voltage, current, impedance, resistance, phase angle, power factor, level of harmonic distortion, frequency and/or power.

By way of example, in general the two discrete states of AC voltage provided on outputs OP**1***a*-OP**5***a* may be driven with PWM used to drive both converters **10***e* and/or **12***e*. the PWM may be much higher in frequency than PWM control signal **20***a* applied to selection unit **16***e* for example. The five outputs (OP**1***a*-OP**5***a*) may have different potential difference values or unequal voltage amplitude values of MIMO converter **12**. The output L of converter **107***e*/selection unit **16***e* may include PWM**1** in the positive half cycle and PWM**5** in the negative half cycle that may correspond with the selection of output OP**5***a* by selection unit **16***e*. Similarly, PWM**2**, PWM**3** and PWM**4** that may correspond with outputs OP**2***a*, OP**3***a* and OP**4***a*. For example, PWM**2** may correspond with output OP**4***a* such that the potential difference of two discrete voltage levels between output OP**4***a* (V**4**-V**3**) may be greater than the potential difference the two discrete voltage levels of output OP**5***a* (V**7**-V**8**) as shown. However, the time periods by comparison with FIG. **2**B, time T**7***a* of PWM control signal **20***a* may be greater than time period T**7** of PWM control signal **20**. In time period T**7***a* approximately fifty percent of the conversion energy provided by MIMO converter **12***e* may reduce the effect of switching-state redundancy when compared to that of MIMO converter **12***d* for example. The fifty percent of the conversion energy may be by use of the inductor pair of L**15** and L16 and four switches Q15*a*, Q15*b*, Q16*a* and Q16*b* to provide a buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC}. The buck, boost, buck/boost and/or buck+boost operation may be in in conjunction with switches Q8*a* and Q8*b* of MIMO converter 12*e*. Alternatively, converter 1000 may be utilized instead or in addition to the auto transformer circuits to provide a buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC}. SIMLO converter 10*e*, MIMO converter 12*e* and selector unit 16*e* may therefore be able to produce different output-voltage levels (V1-V8) with substantially the same amount or less switches as MIMO converter 12*d* and selector unit 16*d* described above. The different output-voltage levels (V1-V8) with substantially the same amount or less switches may reduce the size and cost of converter 107*e*. The reliability of converter 107*e* may also be improved since less semiconductors and capacitors may be employed.

Reference now made to FIG. 4A, which shows a diagram of further details converter 107*f* that includes SIMLO converter 10*f*, MIMO converter 12*f* and selector unit 16*f*, according to illustrative aspects of the disclosure. Converter 107*f* is similar to converter 107*e* in that SIMLO converter 10*e* is the same as SIMLO converter 10*f*. Common to the other MIMO converters described above, MIMO converter 12*f* includes capacitor C2 that connects across terminals V1 and V2 and capacitors C3-C8 that connect across respective terminals. Capacitor C3 connects across terminals V2 and V3, C4 connects across terminals V3 and V4 and so on. Two switches Q8*a* and Q8*b* connect in series across capacitor C8 that is the same as switching network Sn described above. A further two switches Q7*a* and Q7*b* connect in series across capacitor C7 to provide a second switch network Sn. A further two switches Q9*a* and Q9*b* may be wired in series and wired across the two outputs of the two switching networks Sn. The point where switches Q9*a* and Q9*b* are connected together gives an output of MIMO converter 12*f* that connects to one end of inductor L2 that may be included in selector unit 16*f*.

The other end of inductor L2 connects to one end of capacitor C9 and to one side of switches SW1*a* and SW2*a* that are connected together. The other side of capacitor C9 connects to both the neutral (N) and live (L) via respective switches SW2*b* and SW1*b*. The other sides of switches SW1*a* and SW2*a* provide respectively the live (L) and neutral (N) outputs of converter 107*f*. The live (L) and neutral (N) outputs of converter 107*f* connect respectively to switches SW1*b* and SW2*b* that may be included in MUX 88*b*. The other side of switches SW1*b* and SW2*b* connect together and provide the multiple live (L) and neutral (N) inputs to MUX 88*b*. Control of switches in MUX 88*b* allow connection of neutral (N) to either terminal V1 or V respectively via switch SW2*b* or a portion of switch SW2*b* and switch Q440*b*. Similarly, live (L) may be connected to terminal V1 or V3 respectively via switch SW1*b* or a portion of switch SW1*b* and switch Q440*a*. Alternatively switches Q440*a* and Q440*b* may be located in MIMO converter 12*f* so that the PWM supplied to SIMLO converter 10*f* and/or MIMO converter 12*f* may be at a higher frequency compared to the frequency of PWM that may be supplied to selector unit 16*f*.

Reference is now made to FIG. 4B, which shows a possible waveform of the live (L) voltage output of selection unit 16*f* with respect to neutral (N), according to illustrative aspects of the disclosure. Waveforms may be shown with horizontal axis of time (no units specified) versus voltage on the vertical axis (no numerical values specified). Reference waveform 19 is shown as a sinewave by dotted line. Reference waveform 19 may be a sinewave, triangular wave, square wave or any periodic waveform. Reference waveform 19 may be considered to be representative of the desired output of converter 107*f*/selection unit 16*f*. Control signals on control lines 18*a* and/or 18*b* may be provided respectively to PWM unit 14 and selector unit 16*f*. Control signals on control lines 14*a* and 14*b* may be provided respectively to SIMLO converter 10*f* and MIMO converter 12*f* responsive to parameters of reference waveform 19 and/or sensed parameters of converter 107*f*.

The parameters of reference waveform 19 may include the desired voltage amplitude and frequency of the output from converter 107*f*. For example, where load 109 may be a utility grid or single-phase AC motor, the desired voltage and frequency may be 220 Volts (V) and 50 Hertz (Hz) respectively. Electrical parameters sensed by sensors/sensor interface 184 and appropriate signals on control lines 18*a*, 18*b*, 14*a* and 14*b* may provide appropriate control of converter 107*e*. Signals on control lines 18*a*, 18*b*, 14*a* and 14*b* may ensure correct levels of operating voltage, current, impedance, resistance, phase angle, power factor, level of harmonic distortion, frequency and/or power for example.

By way of example, in general the two discrete states of AC voltage provided on outputs OP1*b*-OP3*b* may be driven with PWM used to drive both converters 10*f* and/or 12*f*. The PWM may be much higher in frequency than PWM control signal 20*b* applied to selection unit 16*f* for example. Three outputs (OP1*b*-OP3*b*) may have different potential difference values or unequal voltage amplitude values of MIMO converter 12*f*. The output L of converter 107*f* selection unit 16*f* may include PWM1 in the positive half cycle and PWM3 in the negative half cycle that may correspond with the selection of output OP3*b* by selection unit 16*f*. Similarly, PWM1 and PWM2 may correspond with outputs OP1*b* and OP2*b*. PWM2 may correspond with output OP4*a* such that the potential difference of two discrete voltage levels between output OP2*b* (V3-V1) may be greater than the potential difference the two discrete voltage levels of output OP3*b* (V8-V6) as shown. However, the time periods by comparison with FIG. 3B, time T7*b* of PWM control signal 20*b* may be greater than time period T7*a* of PWM control signal 20*a*. Time period T7*b* may be approximately more than fifty percent of the conversion energy provided by MIMO converter 12*f*. The more than fifty percent of the conversion energy may reduce the effect of switching-state redundancy when compared to that of MIMO converter 12*e*, for example.

The more than fifty percent of the conversion energy may be by use of the inductor pair of L15 and L16 and four switches Q15*a*, Q15*b*, Q16*a* and Q16*b* to provide a buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC}. The more than fifty percent of the conversion energy may be in conjunction with switches Q8*a*, Q8*b*, Q9*a* and Q9*b* of MIMO converter 12*f*. Alternatively, converter 1000 may be utilized instead or in addition to the auto transformer circuits to provide a buck, boost, buck/boost and/or buck+boost operation on voltage V_{DC}. SIMLO converter 10*f*, MIMO converter 12*f* and selector unit 16*f* may therefore be able to produce different output-voltage levels (V1-V8) with substantially the same amount or less switches as MIMO converter 12*e* and selector unit 16*e* described above. The different output-voltage levels (V1-V8) with substantially the same amount or less switches may reduce the size and cost of converter 107*f*. The reliability of converter 107*f* may also be improved since less semiconductors and capacitors may be employed. In sum, converters 107*e* and 107*f* may be considered as having asymmetric converter topologies. In general, a de-population of the number of switches used in MIMO converter **12** and selection unit **16** by use of multiplexor **88** may provide a way to reduce the size and cost of converter **107**. Whereas converter **107** *d* may have more switches compared to converters **107***e* and **107***f*. Converter **107** *d* may offer an improved reduction in total harmonic distortion (THD) by providing for the function of harmonic cancellation due to the symmetrical topology of converter **107** *d*.

Now referring to Table 2 below, Table 2 shows a comparison of the number of switches in each of MIMO converters **12***d*, **12***e*, **12***f*, selection units **16***d*, **16***e*, **16***f* shown in respective FIGS. **1**J, **3**A and **4**A. Using selection unit **16***e* as an example and applying the analysis to the other selection units **16***d* and **16***f*, multiple switches wired in series such as switches Q**340***c*, Q**330***a*, and Q**310***a* for example may be implemented using a single switch.

TABLE 2

	12d	16d	12e	16e	12f	16f
No. switches	14	12	6	12	6	6

From Table 2 it can be seen that the number of switches used is reduced when comparing converter **107***d* with converter **107***e* and converter **107***e* when compared to converter **107***f*. However, the number of levels of current/voltage outputs also decreases when comparing converter **107***d* with converter **107***e* and converter **107***e* when compared to converter **107***f*. Performance of when comparing converter **107** *d* with converter **107***e* and converter **107***e* when compared to converter **107***f* with respect to root mean square (RMS) of the filtered outputs of each selection unit **16** is summarized in Table 3 below in greater detail in descriptions that follow.

In general, the root mean square (RMS) of a function g{x} may be given by the following formula:

$$G(x)_{RMS} = \sqrt{\left[\frac{1}{T}\int_0^T (g\{x\} \times g\{x\})dx\right]}$$

Solving the above definite integral, where g(x) is an AC sine wave of frequency *f*=50 Hz, peak current Im=50 A, ω=π*f*, the RMS output current (Irms) of selection units **16** may be calculated by the following formula derived from solving the above integral:

$$I_{rms}^2 = \frac{Im^2}{4\pi}\left[\omega t2 - \frac{\sin 2\omega t2}{2}\right] - \frac{Im^2}{4\pi}\left[\omega t1 - \frac{\sin 2\omega t1}{2}\right]$$

$$Irms = \sqrt{I_{rms}^2}$$

Now referring to Table 3 below, Table 3 shows a summary of RMS current (Irms) values for the output currents of each of converters **107** *d*, **107***e* and **107***f* shown in respective figures FIGS. **1**J, **3**A and **4**A. The outputs currents of converters **107** *d*, **107***e* and **107***f* are considered sinusoidal by virtue of filtering provided by inductors L**2** in each of converters **107***d*, **107***e* and **107***f*. For each of the converters **107***d*, **107***e* and **107***f*, the above equations with respect to RMS current (Irms) are calculated for a half cycle of AC output current. Times t**1** and t**2** for each output shown in each column of Table 3 correspond to the selection times of respective selection units **16***d*, **16***e* and **16***f*. The selection times determined by respective PWM control signals **20**, **20***a* and **20***b*. The selection times in general have a lower frequency of PWM control signals compared to PWM control signals applied to respective MIMO converters **12***d*, **12***e* and **12***f*. Output waveforms for each of converters **107** *d*, **107***e* and **107***f* may be represented by graphs shown in respective FIGS. **2**B, **3**B and **4**B.

TABLE 3

	FIG. 1J, 2B 107d							
	O/P4		O/P5		O/P6		O/P7 (T7 = 2.58 ms)	
	t1	t2	t1	t2	t1	t2	t1	t2
	0 ms	0.52 ms	0.52 ms	1.81 ms	1.81 ms	2.97 ms	2.97 ms	5.55 ms
Irms	5.67 A		8.948 A		9.6695 A		15.756 A	

	FIG. 3A, 3B 107e					
	OP3a		OP4a		OP5a (T7a = 4.77 ms)	
	t1	t2	t1	t2	t1	t2
	0 ms	0.9 ms	0.9 ms	2.58 ms	2.58 ms	7.35 ms
Irms	7.462 A		10.312 A		18.853 A	

	FIG. 4A 107f			
	OP2b		OP3b (T7b = 6.58 ms)	
	t1	t2	t1	t2
	0	1.81 ms	1.81 ms	8.39 ms
Irms	10.583 A		20.709 A	

Assuming the same switching frequency and capacitor values from Table 3, it can be seen that time T**7** (2.58 ms) of MIMO converter **12*d*** may be less than time T**7*a*** (4.77 ms) of MIMO converter **12*e*** and time T**7*b*** (6.68 ms) may be greater than time period T**7*a*** of MIMO converter **12*f***. However, the differences between each RMS current (Irms) for respective time periods T**7** (15.756 A), T**7*a*** (18.853 A) and T**7*b*** (20.709 A) are not so different compared to the time differences. Therefore, a benefit of using converter **107*f*** compared to converters **107*e*** and **107 *d*** may be use of fewer switches with similar power loss in MIMO converter **12*f*** compared to MIMO converters **12*d*** and **12*e***. Whereas a benefit of MIMO converter **12*d*** compared to the asymmetric topology of MIMO converters **12*e*** and **12*f***, may offer an improved reduction in total harmonic distortion (THD). The improved reduction in THD may be provided by the symmetrical topology of converter **107*d*** that may include more switches to provide symmetrical topology. The switches of converter **107*d***, because of the lower values of rms current (Irms) compared to converters **107*e*** and **107*d***, may be realized using cheaper MOSFETs within a single converter design. The cheaper MOSFETs may be cheaper because of

RMS of a PWM current waveform (I_{RMS}) is proportional to the square root of its duty cycle D.

$$Irms = A\sqrt{D}$$

$$D = \frac{T_{ON}}{T}$$

Where A is the peak current value of the PWM current waveform in amperes, T_{ON} is the ON period of the PWM current waveform and T_{OFF} is the OFF period of the PWM current waveform. The overall time period T of the PWM current waveform is the sum of T_{ON} and T_{OFF}.

Both energy and power loss in MIMO converters **12*d***, **12*e*** and **12*f*** may therefore be inversely proportional to the capacitance values of the capacitors C**2**-C**8** in each of the MIMO converters **12*d***, **12*e*** and **12*f***, the switching frequency and duty cycle of the switches for each RMS output current (I_{rms}) may be summarized in Table 4 below. A fixed duty cycle (D) of 50% is used in calculation for each respective output of the switches of MIMO converters **12*d***, **12*e*** and **12*f***.

TABLE 4

	FIG. 1J, 2B 107d							
	O/P4		O/P5		O/P6		O/P7	
	t1	t2	t1	t2	t1	t2	t1	t2
	0 ms	0.52 ms	0.52 ms	1.81 ms	1.81 ms	2.97 ms	2.97 ms	5.55 ms
	0 A	7.1 A	7.1 A	21.3 A	21.3 A	35.51 A	35.51 A	49.97 A
Irms/ switch	6.35 A		6.35 A		6.35 A		6.35 A	

	FIG. 3A, 3B 107e					
	OP3a		OP4a		OP5a (T7a = 4.77 ms)	
	t1	t2	t1	t2	t1	t2
	0 ms	0.9 ms	0.9 ms	2.58 ms	2.58 ms	7.35 ms
	0 A	9.09 A	9.09 A	37.5 A	37.5 A	52.27 A
Irms/ switch	4.06 A		6.35 A		6.6 A	

	FIG. 4A 107f			
	OP2b		OP3b (T7b = 6.58 ms)	
	t1	t2	t1	t2
	0	1.81 ms	1.81 ms	8.39 ms
	0 A	14.77 A	14.77 A	48.8 A
Irms/ Switch	6.60 A		5.08 A	

higher drain to source (rds) resistance compared to MOSFETs of converters **107*e*** and **107*d***. Compared to converter **107*d***, the lower values of rms current (Irms) for converters **107*e*** and **107*d*** with the higher drain to source (rds) resistance may give a substantially similar power loss to more expensive lower rds resistance of MOSFETs for converter **107*d***.

More specifically, with respect to the switches in MIMO converters **12*d***, **12*e*** and **12*f***, the current in the switches may follow the substantially rectangular PWM applied to the switches of MIMO converters **12*d***, **12*e*** and **12*f***. Since the current may follow the substantially rectangular PWM, the

The substantially symmetrical topology of converter **107 *d*** is reflected in the substantially equal currents for each switch in MIMO converter **12*d*** of 6.35 amperes (A). Whereas the substantially asymmetrical topologies of converters **107*e*** and **107*f*** is reflected in different I_{RMS} current values per switch since the number of levels of current/voltage outputs also decrease when comparing converter **107*d*** with converter **107*e*** and converter **107*e*** when compared to converter **107*f***. A benefit of using converter **107*f*** compared to converters **107*e*** and **107*d*** is that it that may use fewer switches with similar power loss in MIMO converter **12*f*** compared to MIMO converters **12*d*** and **12*e***. Whereas a benefit of MIMO converter **12*d*** compared to the asymmetric topology of MIMO converters **12***e* and **12***f*, may offer an improved reduction in total harmonic distortion (THD). The improved reduction in THD may be provided by the symmetrical topology of converter **107***d* that may include more switches to provide symmetrical topology.

Descriptions above have illustrated a single-phase converter but the same use of switches may be applied to similar three phase converter circuit implementations also. The same use of switches may be applied to other converter topologies for both three-phase and single-phase converters. The same use of switches may also be similarly applied to multi-level converters of various types.

All optional and preferred features and modifications of the described aspects and dependent claims are usable in all aspects taught herein. Furthermore, the individual features of the dependent claims, as well as all optional and preferred features and modifications of the described aspects are combinable and interchangeable with one another. In addition to descriptions for FIG. **1**J, FIG. **3**A and FIG. **4**A that describe the cascaded components for converter **107**, it may be possible by way of non-limiting example to have converter **107** as SIMLO converter **10***d* cascaded with MIMO converter **12***e* and selector unit **16***f* and/or SIMLO converter **10***e*, cascaded with MIMO converter **12***f* and selector unit **16***e* and so on. A person skilled in the art would make the appropriate selection of components of converter **107** and selection of the appropriate control signals (e.g. control outputs **14***a*, **14***b*, **18***a* and **18***b*). The appropriate selection of components and selection of appropriate control signals responsive to a desired reference waveform **19** and sensed electrical parameters of converter **107**. The sensed electrical parameters may include voltage, current, impedance, resistance, phase angle, power factor, level of harmonic distortion, frequency and/or power.

What is claimed is:

1. A system comprising:

a first converter comprising first switching circuitry configured to convert an input voltage into a plurality of discrete voltages;

a second converter comprising second switching circuitry configured to convert the plurality of discrete voltages into a plurality of modulated voltages, wherein each modulated voltage of the plurality of modulated voltages comprises two voltage levels equal, respectively, to two of the discrete voltages of the plurality of discrete voltages; and

a selection circuit configured to alternatively output each modulated voltage of the plurality of modulated voltages across a pair of output terminals,

wherein the first converter is controlled according to a first modulation scheme based on an electrical parameter,

wherein the second converter is controlled according to a second modulation scheme based on the electrical parameter,

wherein the selection circuit is controlled according to a third modulation scheme based on at least one of the electrical parameter or a reference signal, and

wherein a frequency of at least one of the first modulation scheme or the second modulation scheme is lower than a frequency of the third modulation scheme.

2. The system of claim **1**, further comprising a sensor configured to sense the electrical parameter,

wherein the selection circuit is further configured to alternatively output the each modulated voltage based on the electrical parameter, and

wherein the electrical parameter is selected from at least one of: voltage, current, impedance, resistance, phase angle, power factor, harmonic distortion, frequency, or power.

3. The system of claim **1**, wherein the selection circuit comprises:

a rotary switch comprising terminals, a pole, and a shaft, wherein the terminals are connectable to one or more output terminals of the second converter, and

wherein the pole is configured to provide the each modulated voltage of the plurality of modulated voltages based on a velocity of rotation of the shaft.

4. The system of claim **1**, wherein the selection circuit comprises:

a plurality of interconnected switches configurable to output at least one of the plurality of modulated voltages that are output by the second converter.

5. The system of claim **1**, further comprising a controller configured to, based on the electrical parameter, control the second converter according to a modulation scheme.

6. The system of claim **5**, wherein the modulation scheme is at least one of: pulse width modulation (PWM), frequency modulation, or variable frequency and variable pulse width.

7. The system of claim **1**, further comprising:

a filter connected to the pair of output terminals of the selection circuit and configured to filter the each modulated voltage that is output by the selection circuit.

8. The system of claim **1**, wherein the first switching circuitry comprises at least one of: a buck circuit, a boost circuit, a buck/boost circuit, or a buck plus (+) boost circuit.

9. The system of claim **1**, wherein at least one of the first modulation scheme, the second modulation scheme, or the third modulation scheme is at least one of: pulse width modulation (PWM), frequency modulation, or variable frequency and variable pulse width modulation.

10. The system of claim **1**, wherein the second switching circuitry comprises a two-level inverter configured to output at least one modulated voltage of the plurality of modulated voltages.

11. The system of claim **1**, wherein second switching circuitry comprises a multi-level inverter configured to output at least one modulated voltage of the plurality of modulated voltages.

12. The system of claim **1**, wherein the second converter further comprises a series connection of capacitors.

13. The system of claim **12**, further comprising one or more switches connected across at least one capacitor of the series connection of capacitors.

14. The system of claim **1**, wherein the selection circuit comprises:

a plurality of interconnected switches configured to output at least one of the plurality of modulated voltages that are output by the second converter.

15. A method comprising:

converting, by a first converter, an input voltage into a plurality of discrete voltages;

converting, by a second converter, the plurality of discrete voltages into a plurality of modulated voltages, wherein each modulated voltage of the plurality of modulated voltages comprises two voltage levels equal, respectively, to two of the discrete voltages of the plurality of discrete voltages; and

alternatively outputting, by a selection circuit, each modulated voltage of the plurality of modulated voltages across a pair of output terminals, wherein the converting by the first converter is performed according to a first modulation scheme based on an electrical parameter,

wherein the converting by the second converter is performed according to a second modulation scheme based on the electrical parameter,

wherein the alternatively outputting by the selection circuit is performed according to a third modulation scheme based on at least one of the electrical parameter or a reference signal, and

wherein a frequency of at least one of the first modulation scheme or the second modulation scheme is lower than a frequency of the third modulation scheme.

16. The method of claim **15**, wherein the alternatively outputting the each modulated voltage is based on the electrical parameter sensed by a sensor, and wherein the electrical parameter is selected from at least one of: voltage, current, impedance, resistance, phase angle, power factor, harmonic distortion, frequency, or power.

17. The method of claim **15**, wherein the alternatively outputting the each modulated voltage is based on the reference signal comprising at least one of: a sine wave, a triangular wave, a square wave, or a sawtooth wave.

18. The method of claim **15**, wherein at least one of the first modulation scheme, the second modulation scheme, or the third modulation scheme is one of: pulse width modulation (PWM), frequency modulation, or variable frequency and variable pulse width modulation.

19. The method of claim **15**, wherein at least one modulated voltage of the plurality of modulated voltages is generated by the second converter via one of a two-level inverter or a multi-level inverter.

20. The method of claim **15**, wherein the first converter comprises at least one of: a buck circuit, a boost circuit, a buck/boost circuit, or a buck plus (+) boost circuit.

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