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Yamauchi et al.

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(54) **SEMICONDUCTOR DEVICE, COOLING MODULE, POWER CONVERTING DEVICE, AND ELECTRIC VEHICLE**

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(73) Assignee: **FUJI ELECTRIC CO., LTD.**, Kawasaki (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 27 days.

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**

H01L 23/473	(2006.01)
H01L 23/467	(2006.01)
H01L 23/367	(2006.01)
H01L 23/50	(2006.01)
H02M 7/00	(2006.01)
H02P 27/06	(2006.01)
H02M 7/537	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/473*** (2013.01); ***H01L 23/3675*** (2013.01); ***H01L 23/467*** (2013.01); ***H01L 23/50*** (2013.01); ***H02M 7/003*** (2013.01); *H02M 7/537* (2013.01); *H02P 27/06* (2013.01)

(58) **Field of Classification Search**

CPC H01L 23/46; H01L 23/467; H01L 23/473

USPC 257/714, E23.097, E23.098, E23.099

See application file for complete search history.

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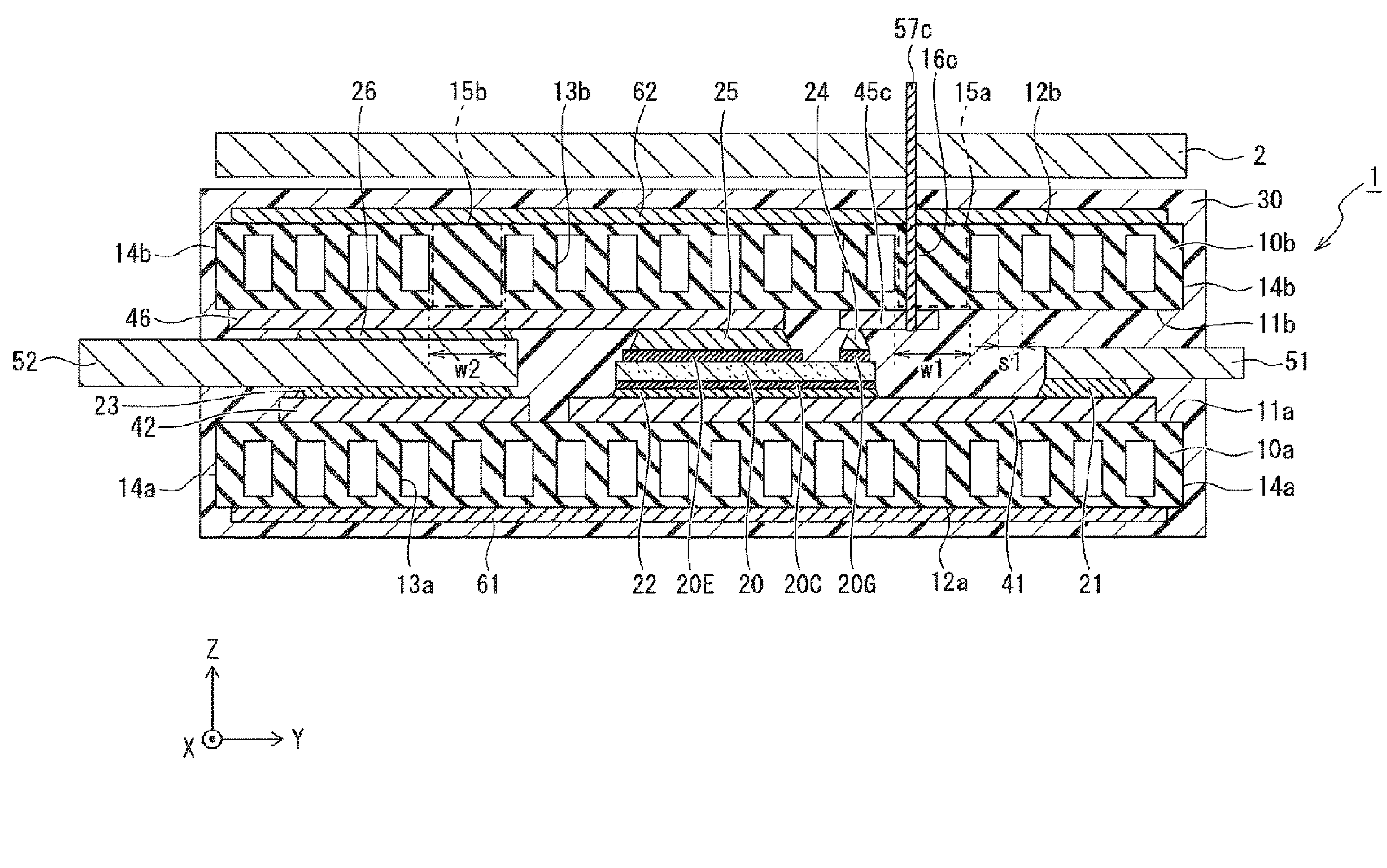
Primary Examiner — Victoria K. Hall

(57) **ABSTRACT**

A semiconductor device includes: a first cooling device including a plurality of first flow channels through which a fluid flows, between a first main surface and a second main surface opposed to each other; a second cooling device including a plurality of second flow channels through which a fluid flows, between a third main surface and a fourth main surface parallel to the first main surface; a semiconductor element interposed between the first main surface and the third main surface facing each other; and a control terminal penetrating from the third main surface to the fourth main surface in a terminal-penetrating region defined at a predetermined position between the plurality of second flow channels, and electrically connected to a control electrode of the semiconductor element.

12 Claims, 25 Drawing Sheets



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2002/0101718	A1 *	8/2002	Negishi	F28F 3/025 361/699
2002/0185260	A1 *	12/2002	Calaman	H01L 23/473 165/80.4
2002/0185718	A1 *	12/2002	Mikubo	H01L 23/433 257/678
2004/0190251	A1 *	9/2004	Prasher	H01L 23/473 361/699
2004/0196634	A1 *	10/2004	Mallik	H01L 23/36 361/704
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2005/0073042	A1 *	4/2005	Hirano	H01L 23/4338 257/717
2007/0085197	A1 *	4/2007	Arai	H01L 23/473 257/712
2007/0096278	A1 *	5/2007	Nakatsu	H01L 25/071 257/678
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2007/0227697	A1 *	10/2007	Takahashi	H01L 23/473 165/80.4
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2008/0160246	A1 *	7/2008	Buhler	H01L 23/467 428/99
2008/0224303	A1 *	9/2008	Funakoshi	H01L 23/473 257/701
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2009/0145642	A1 *	6/2009	Kuromitsu	H05K 3/38 174/258
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2010/0238627	A1 *	9/2010	Shinohara	H01L 23/3107 361/695
2010/0264520	A1 *	10/2010	Ogawa	H01L 23/3735 257/618
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2014/0138075	A1 *	5/2014	Yang	H01L 23/473 165/185
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2014/0376189	A1 *	12/2014	Sakaguchi	H01L 23/473 361/719
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2017/0314515	A1 *	11/2017	Oono	H01L 23/473
2018/0098457	A1 *	4/2018	Takeuchi	H02M 7/003
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JP	2014216589	A *	11/2014	
JP	2015008169	A *	1/2015	H01L 23/473
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WO	2013/118415	A1	8/2013	
WO	2014/132483	A1	9/2014	
WO	2015/194259	A1	12/2015	
WO	2016/009727	A1	1/2016	
WO	WO-2017179736	A1 *	10/2017	H01L 23/473

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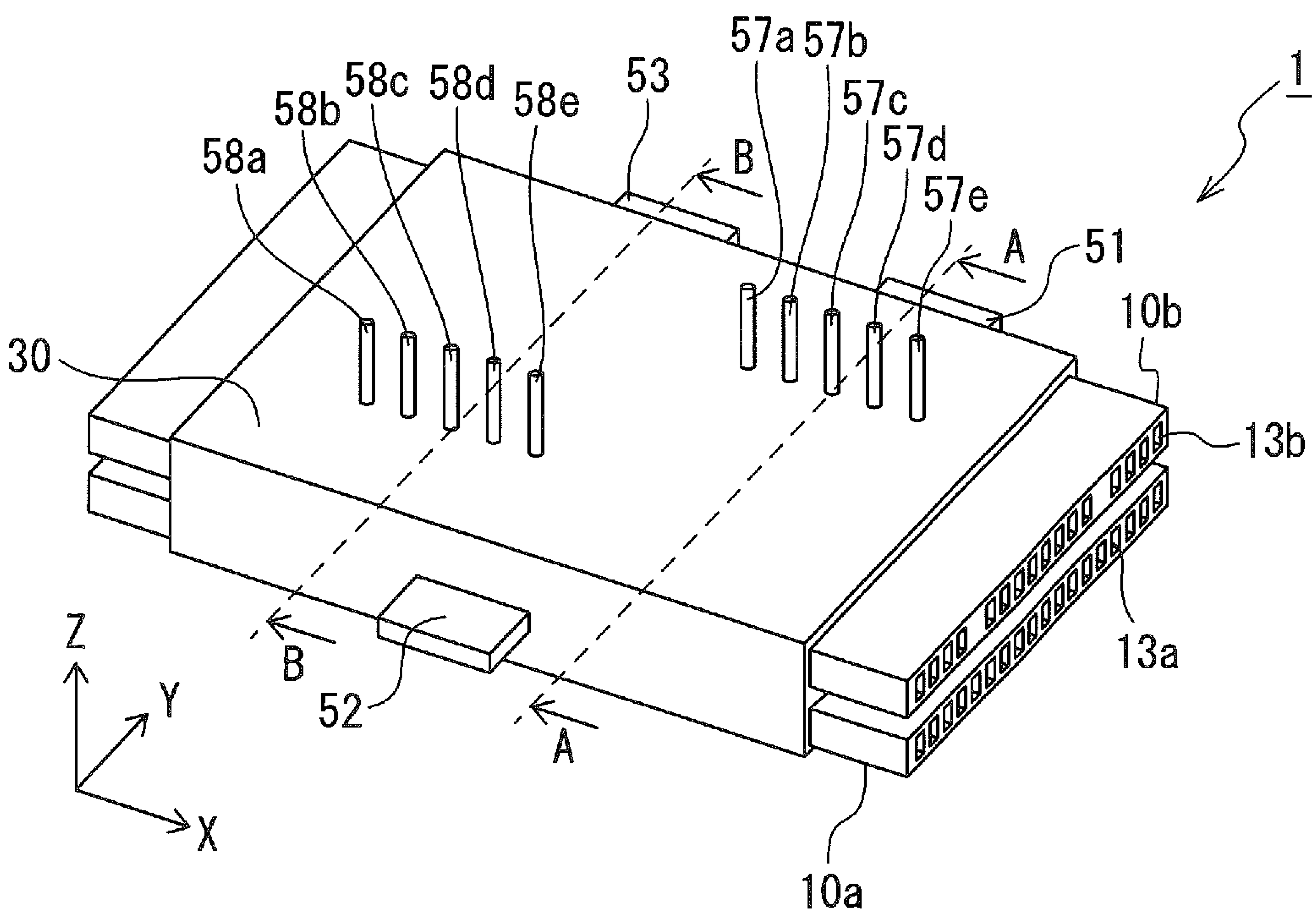
FIG. 1



58a
58b
58c
58d
58e
53
57a
57b
57c
57d
57e
B
A
51
1
10b
13b
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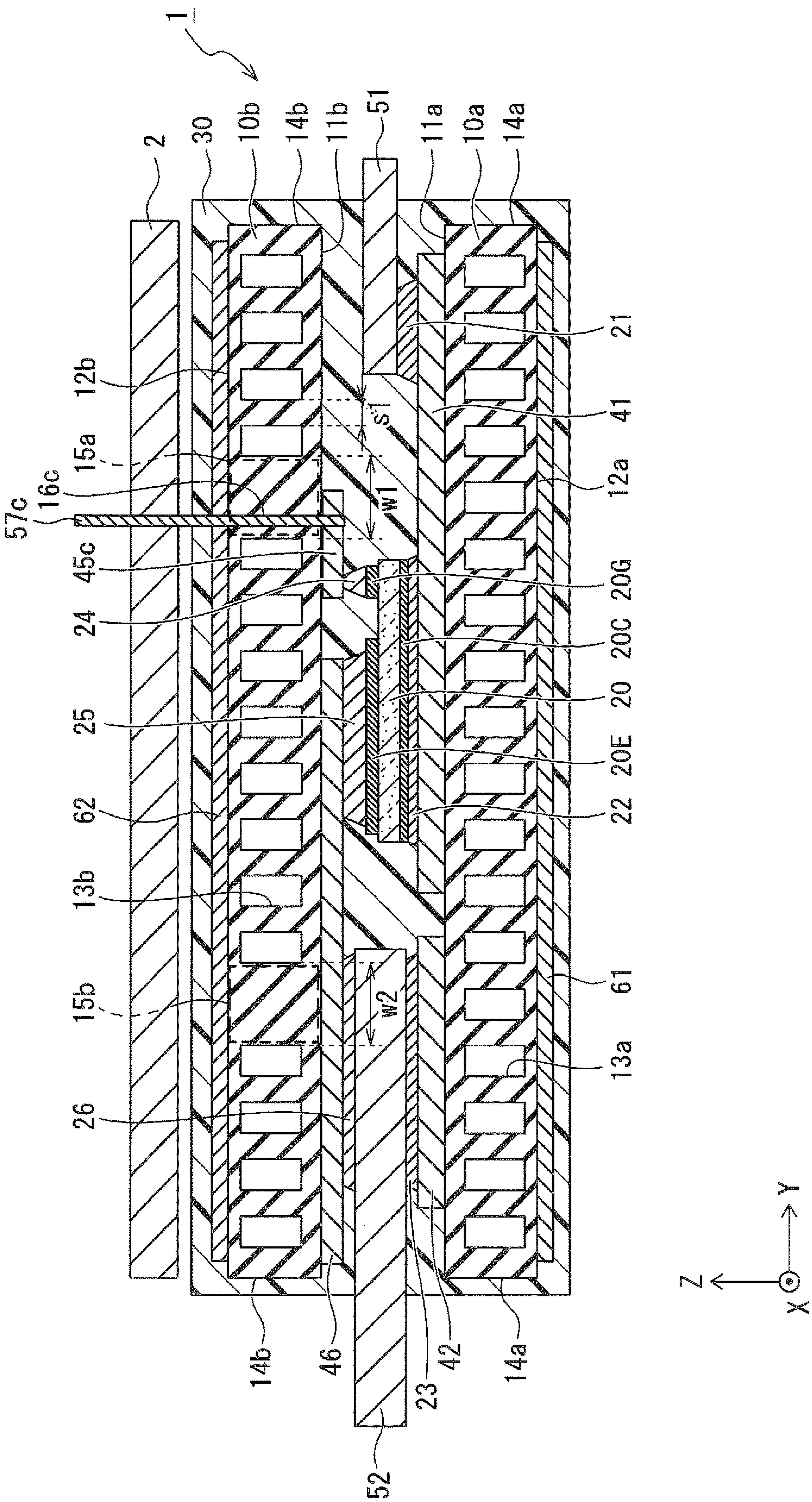
13a
Z
Y
X
B
52
A
10a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2
30
10b
14b
11b
51
11a
10a
14a
21
41
12a
20G
20C
20
20E
22
61
13a
12b
15a
16c
57c
45c
24
25
62
13b
15b
26
14b
46
52
23
42
14a
S1
W1
W2
Z
Y
X

FIG. 2

FIG. 3A

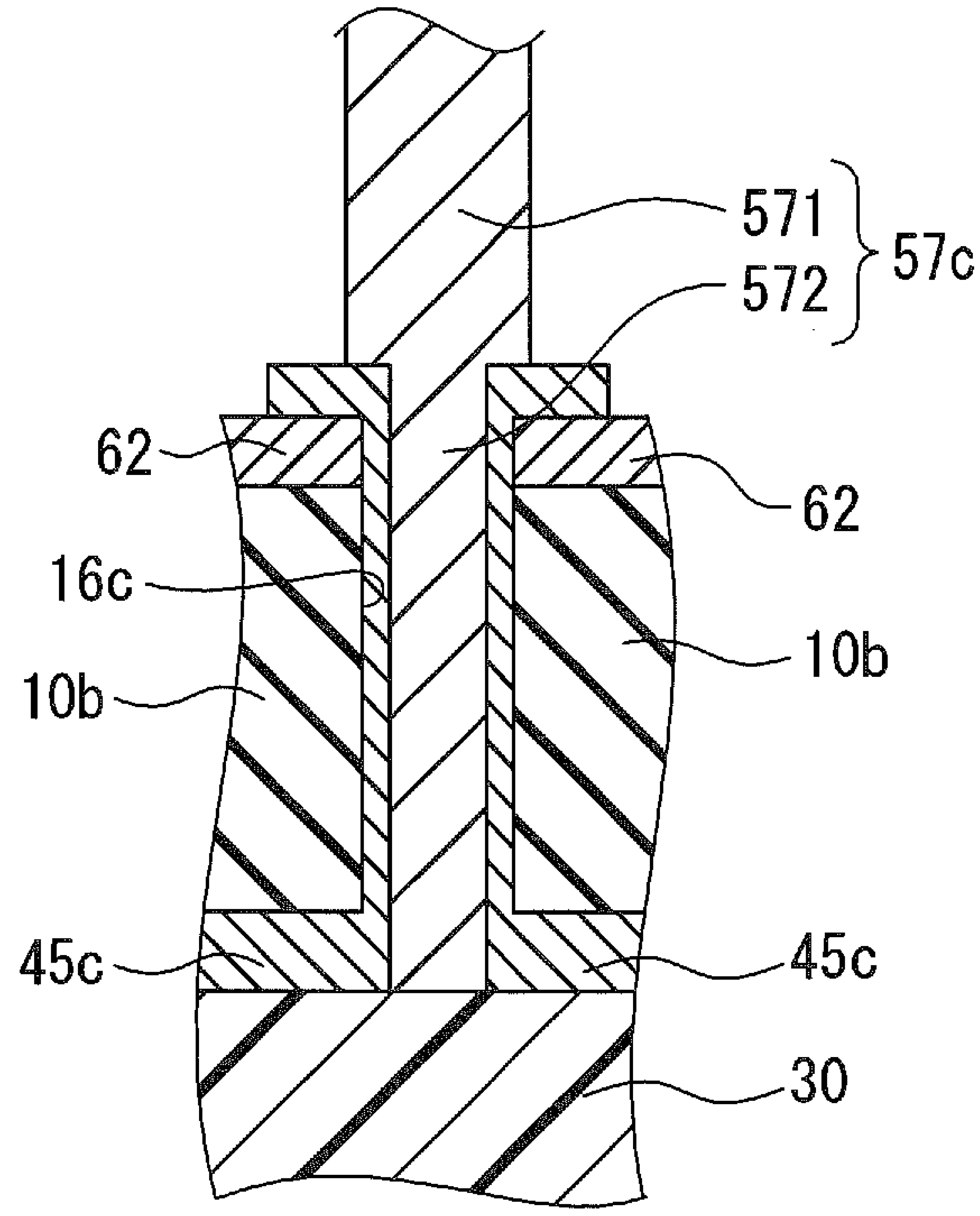
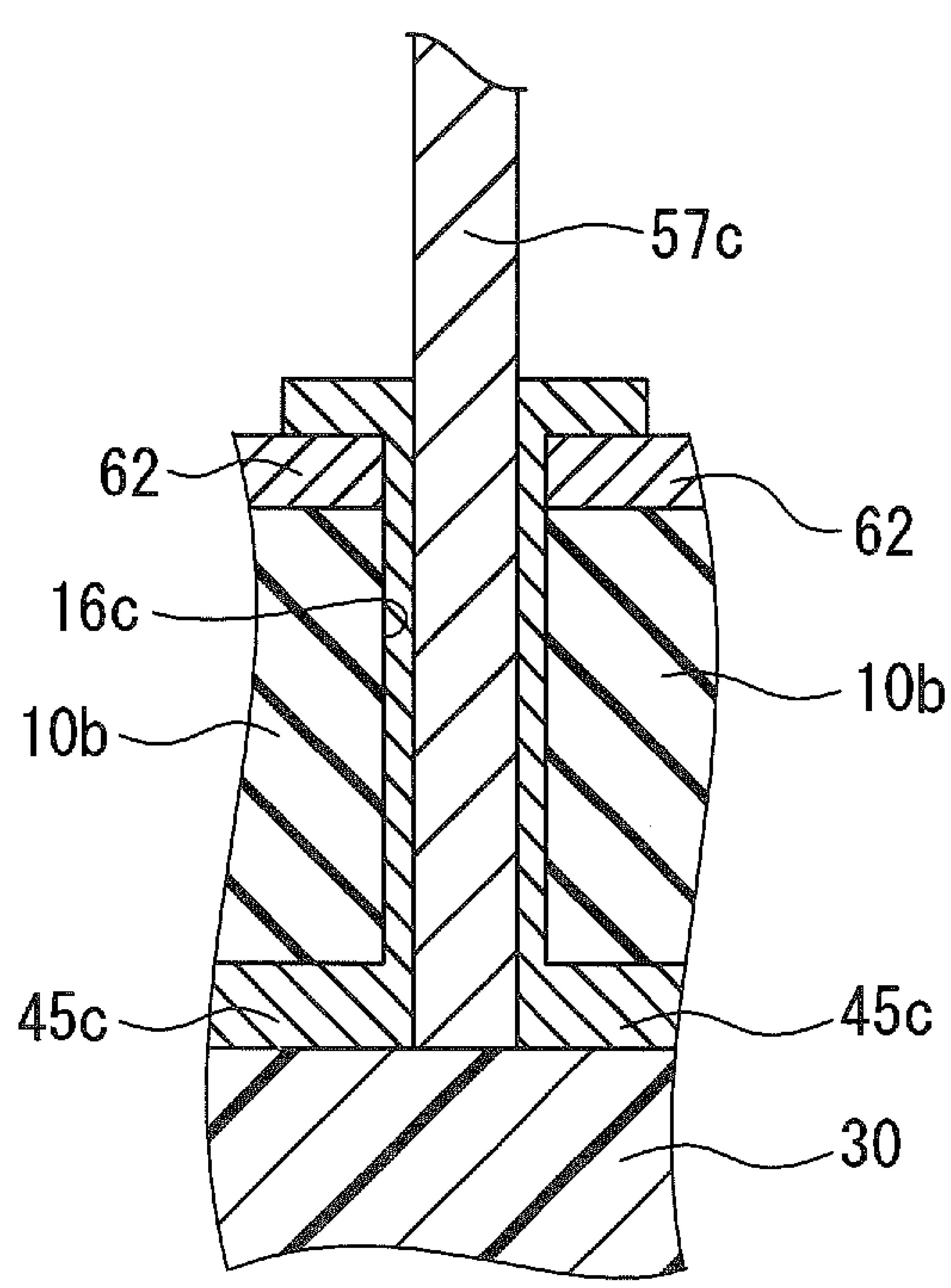

571
572
57c
62
62
16c
10b
10b
45c
45c
30

FIG. 3B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62
62
16c
10b
10b
45c
45c
30

FIG. 4

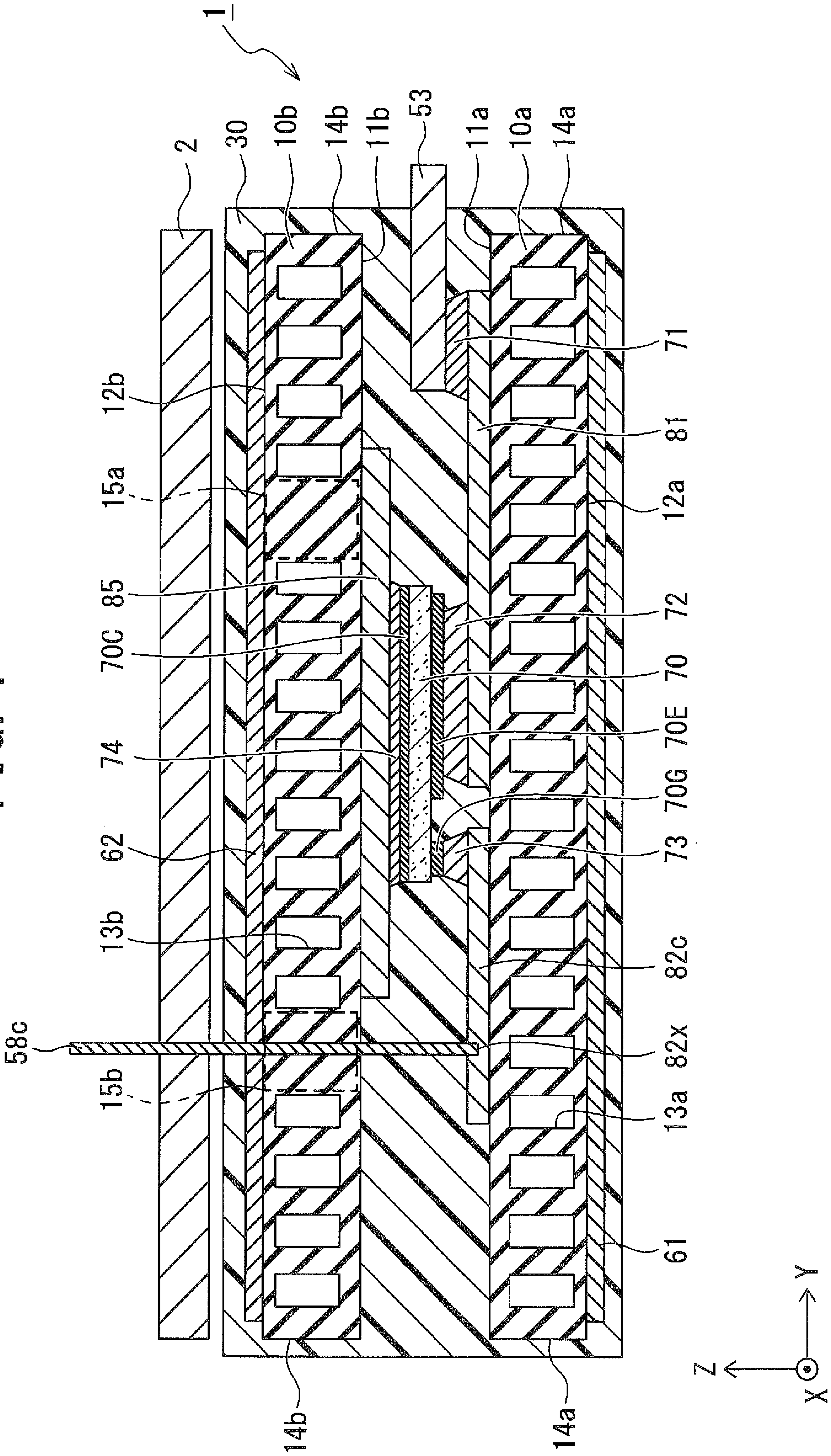

1
2
30
10b
14b
11b
53
11a
10a
14a
71
12b
81
15a
12a
85
72
70C
70
74
70E
70G
62
73
13b
82c
58c
82x
15b
13a
61
14b
14a
Y
Z
X

FIG. 5

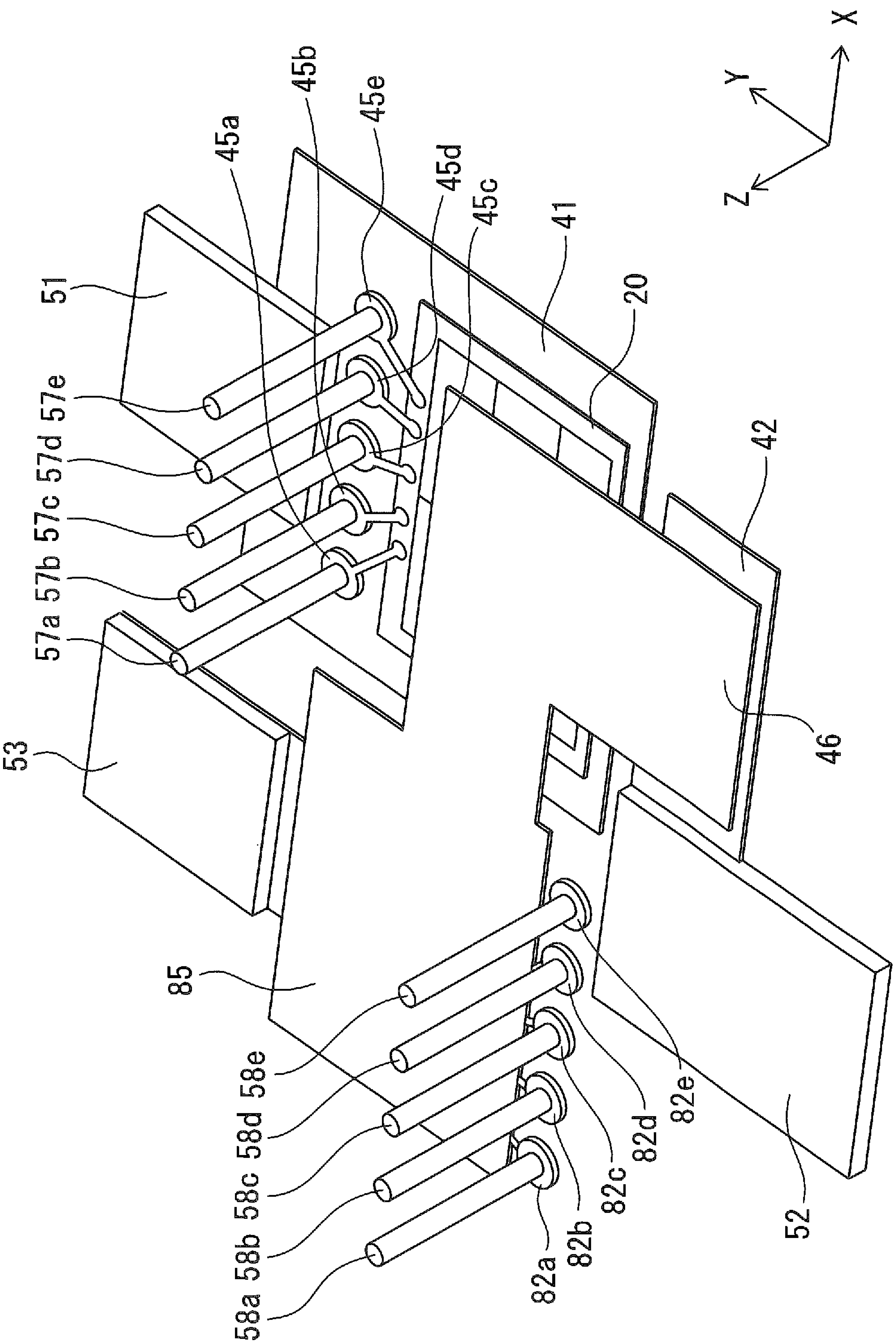

X
Y
Z
45a
45b
45c
45d
45e
41
20
42
46
51
52
53
85
57a 57b 57c 57d 57e
58a 58b 58c 58d 58e
82a
82b
82c
82d
82e

FIG. 6

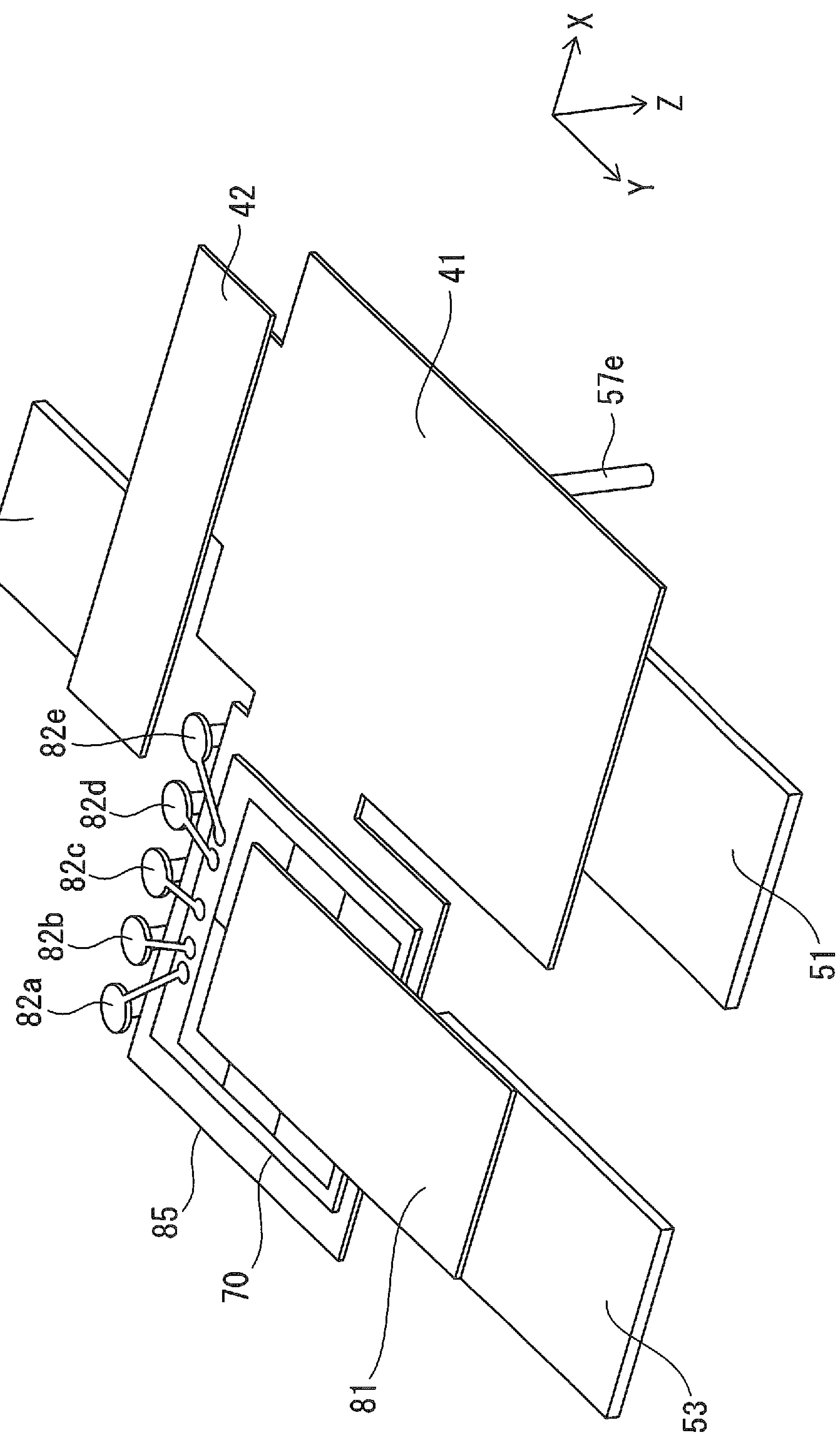


FIG. 7

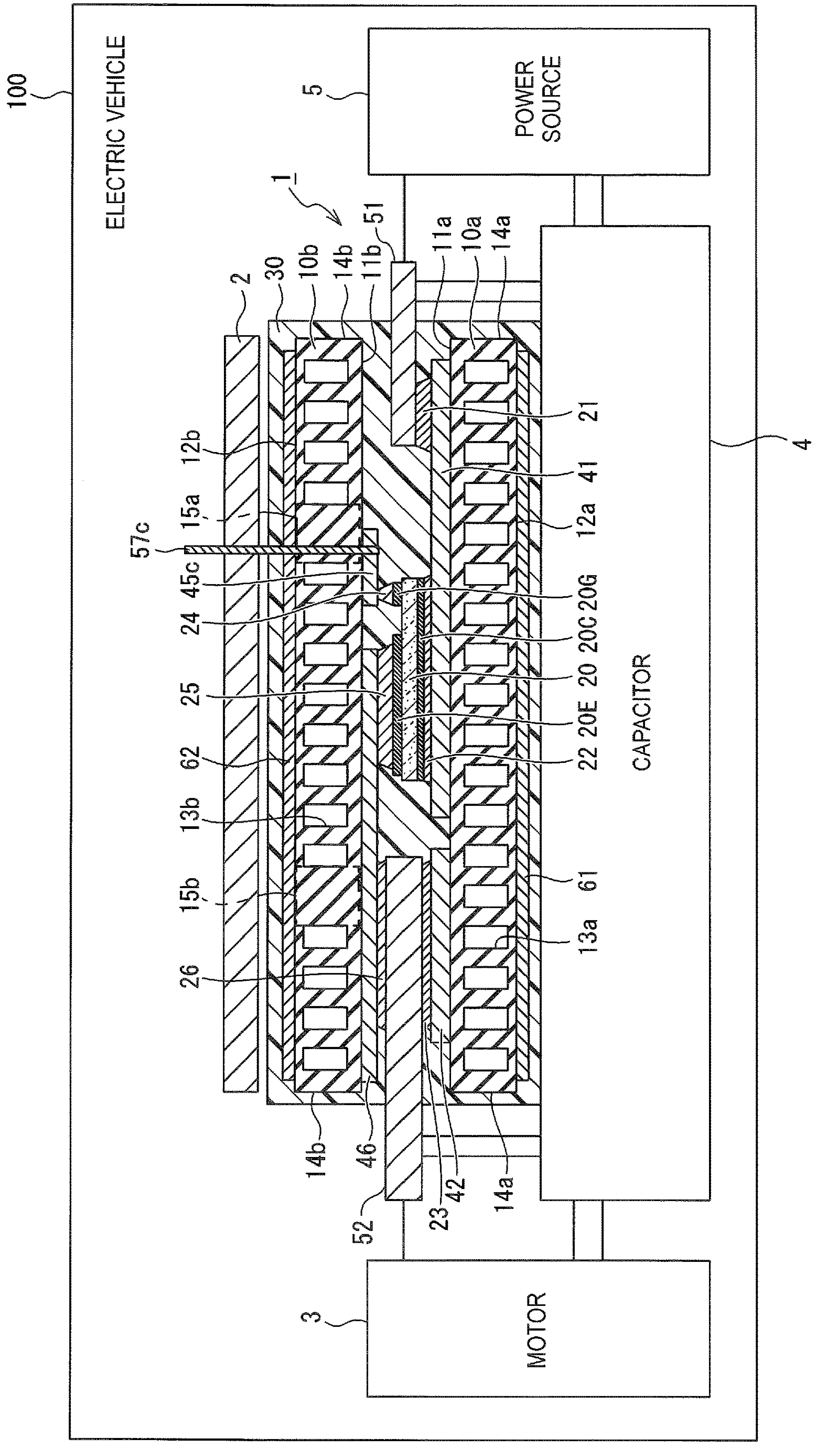

ELECTRIC VEHICLE
POWER SOURCE
CAPACITOR
MOTOR
100
5
1
2
3
4
30
10b
14b
11b
51
11a
10a
14a
21
41
12a
12b
15a
57c
45c
24
20G
20C
20
20E
22
25
62
13b
15b
26
61
13a
46
52
23
42

FIG. 8

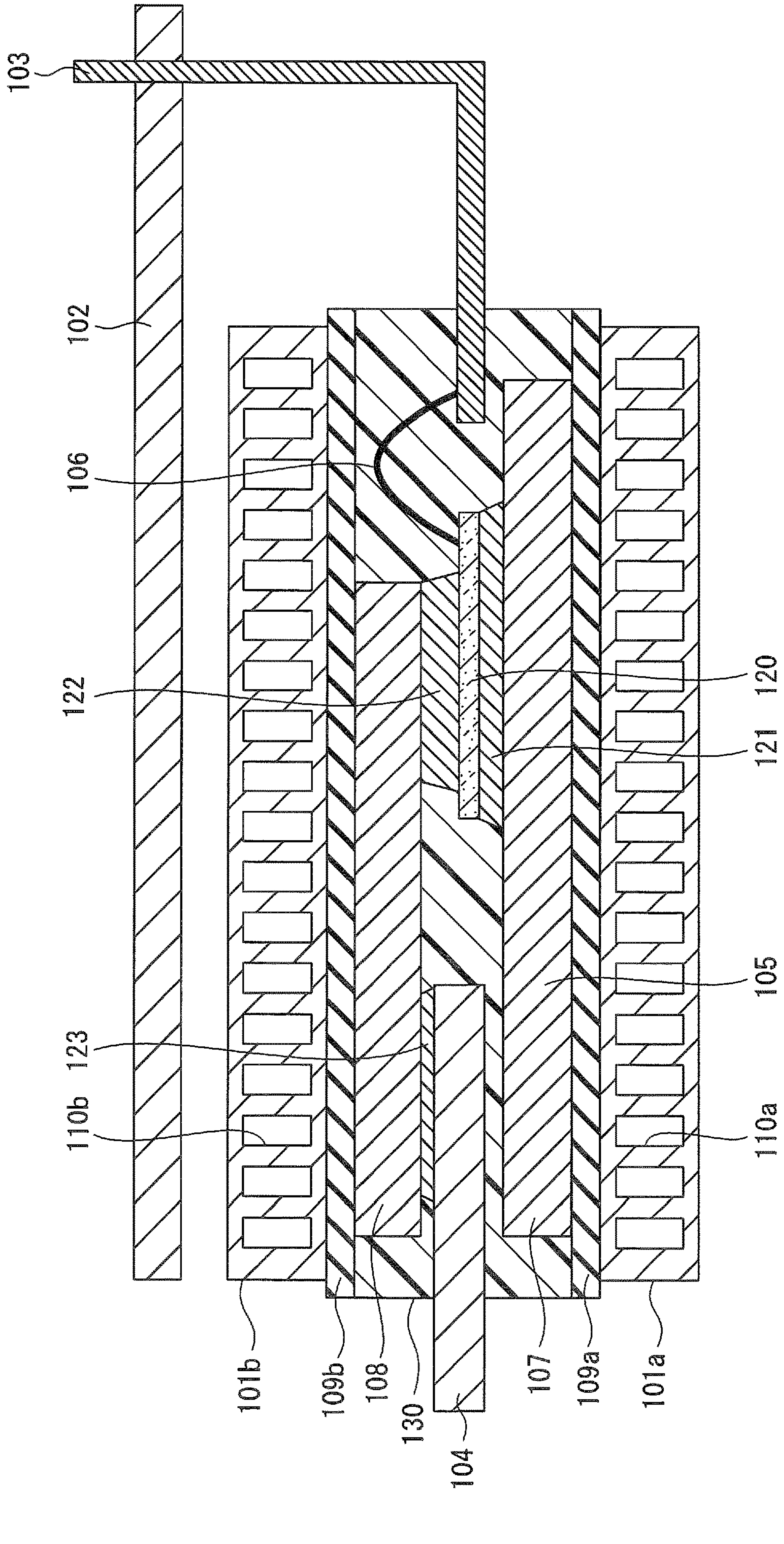

103
102
106
122
123
110b
101b
109b
108
130
104
107
109a
101a
110a
105
121
120

FIG. 9

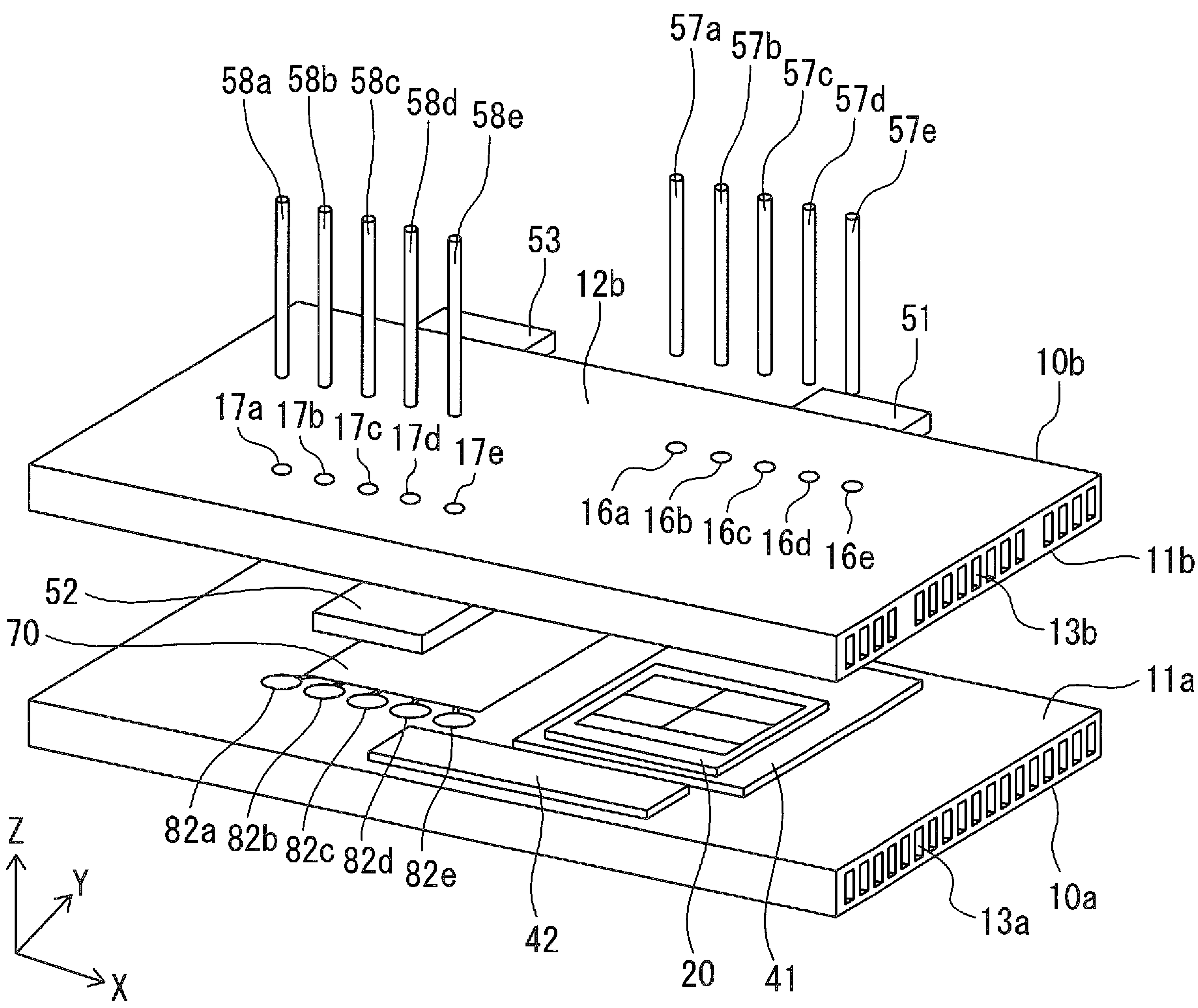
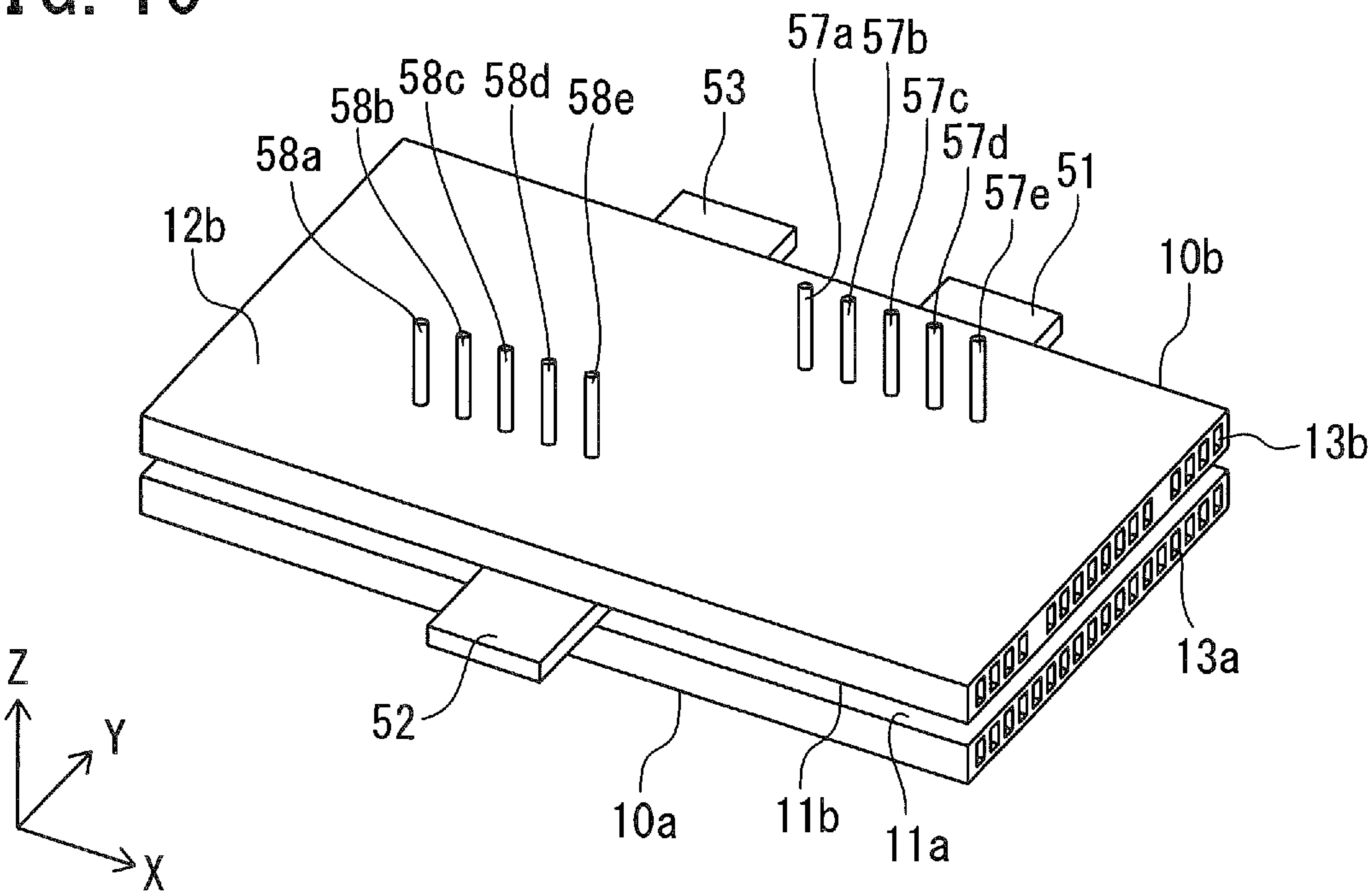
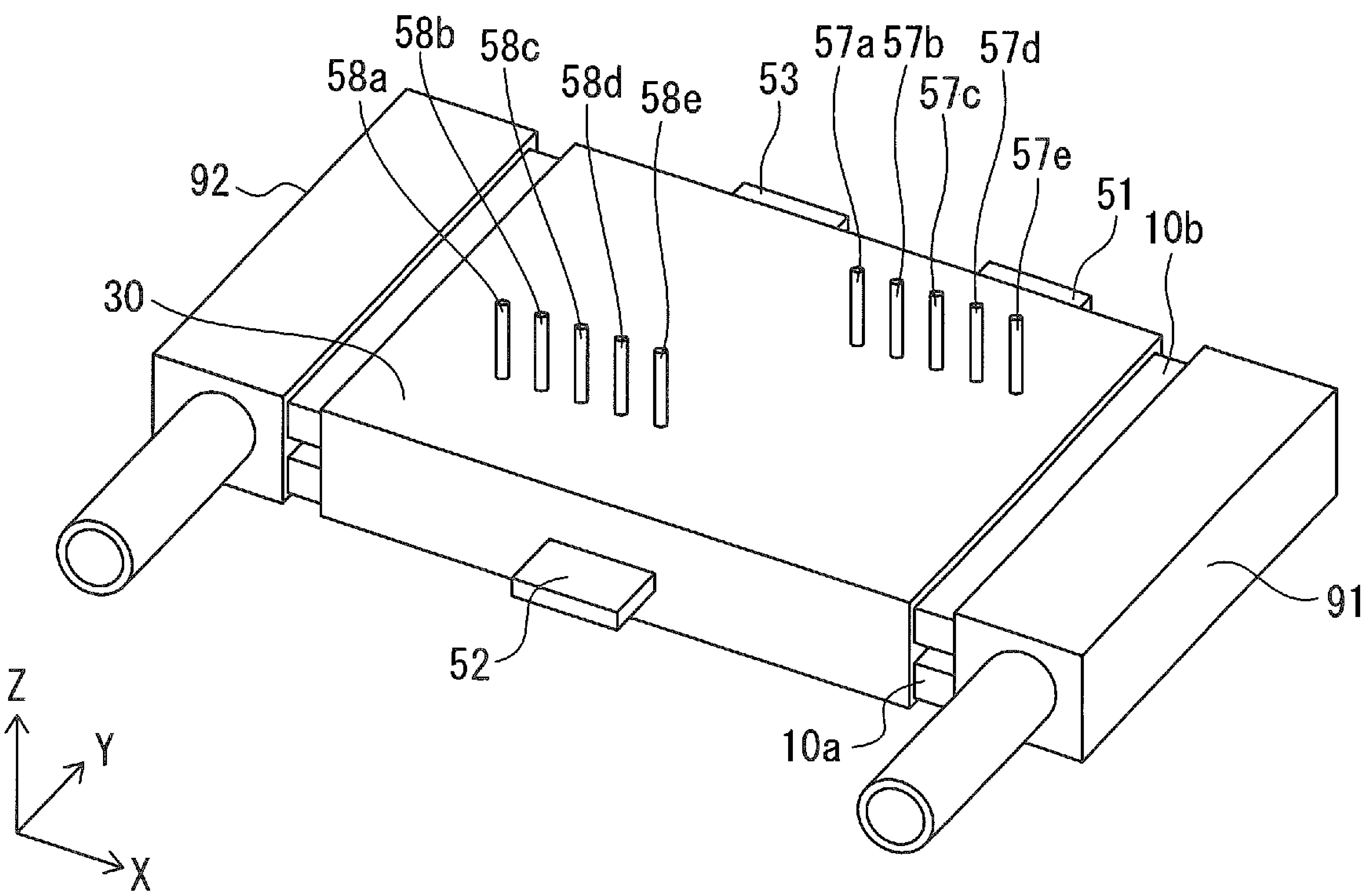

58a
58b
58c
58d
58e
57a
57b
57c
57d
57e
53
12b
51
10b
17a
17b
17c
17d
17e
16a
16b
16c
16d
16e
11b
13b
52
70
11a
82a
82b
82c
82d
82e
42
20
41
13a
10a
Z
Y
X

FIG. 10



58a
58b
58c
58d
58e
53
57a
57b
57c
57d
57e
51
12b
10b
13b
13a
52
10a
11b
11a
Z
Y
X

FIG. 11



58a
58b
58c
58d
58e
53
57a
57b
57c
57d
57e
51
10b
92
30
91
52
10a
Z
Y
X

FIG. 12

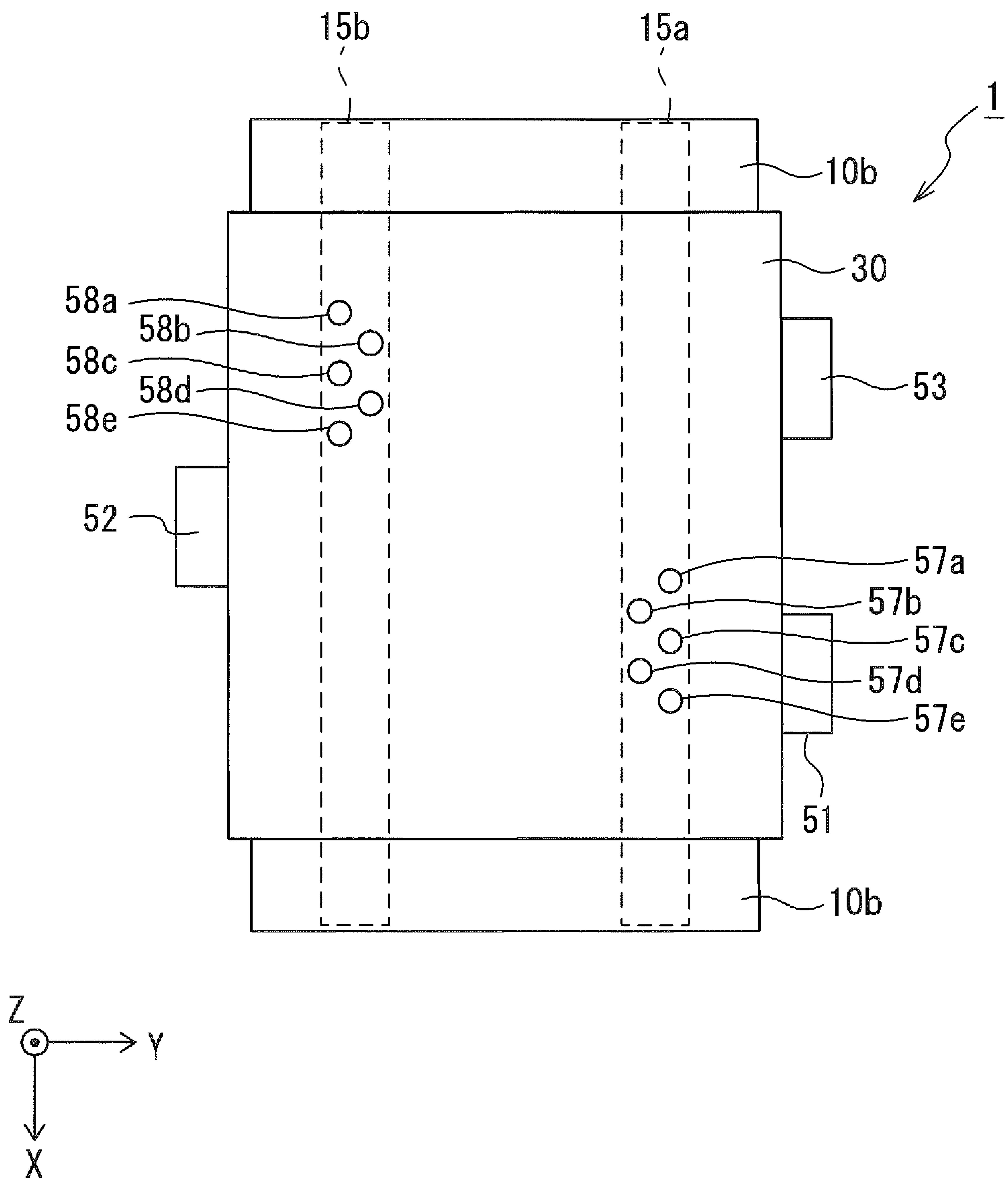

15b
15a
1
10b
30
58a
58b
58c
58d
58e
53
52
57a
57b
57c
57d
57e
51
10b
Z
Y
X

FIG. 13

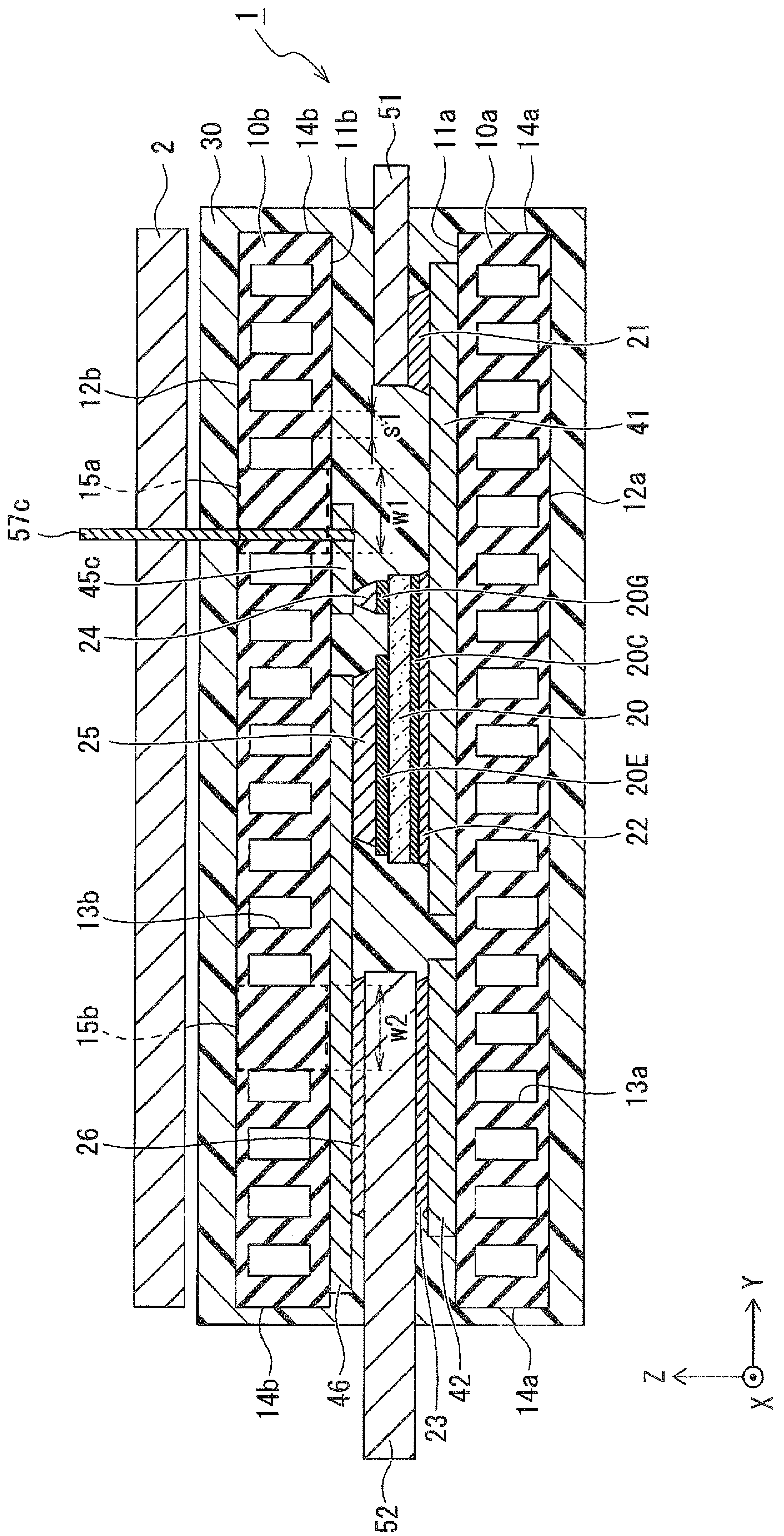

1
2
30
10b
14b
11b
51
11a
10a
14a
21
12b
S1
41
15a
W1
12a
57c
45c
20G
24
20C
20
25
20E
22
13b
15b
W2
13a
26
14b
46
23
42
14a
52
Y
Z
X

FIG. 14

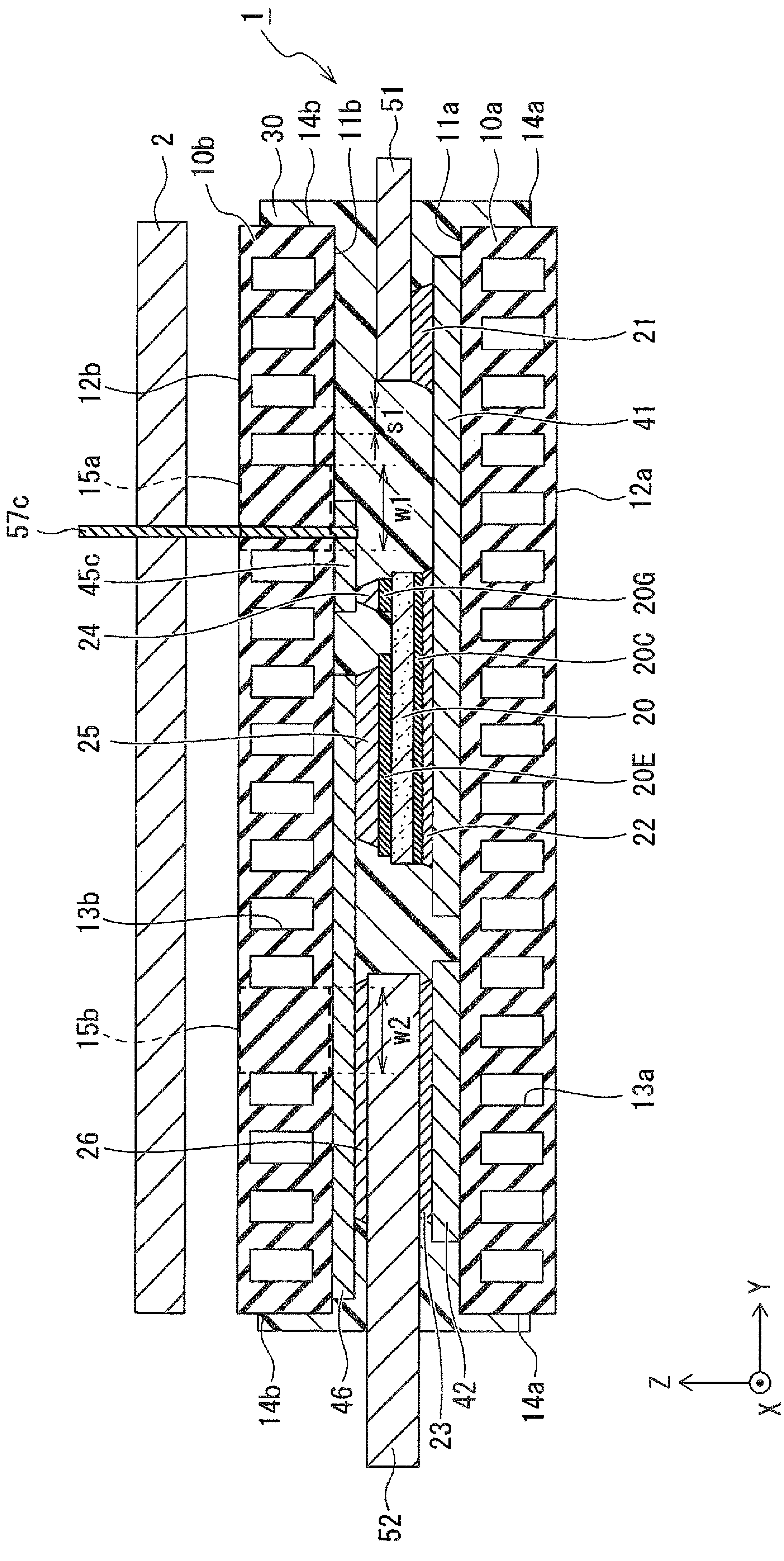
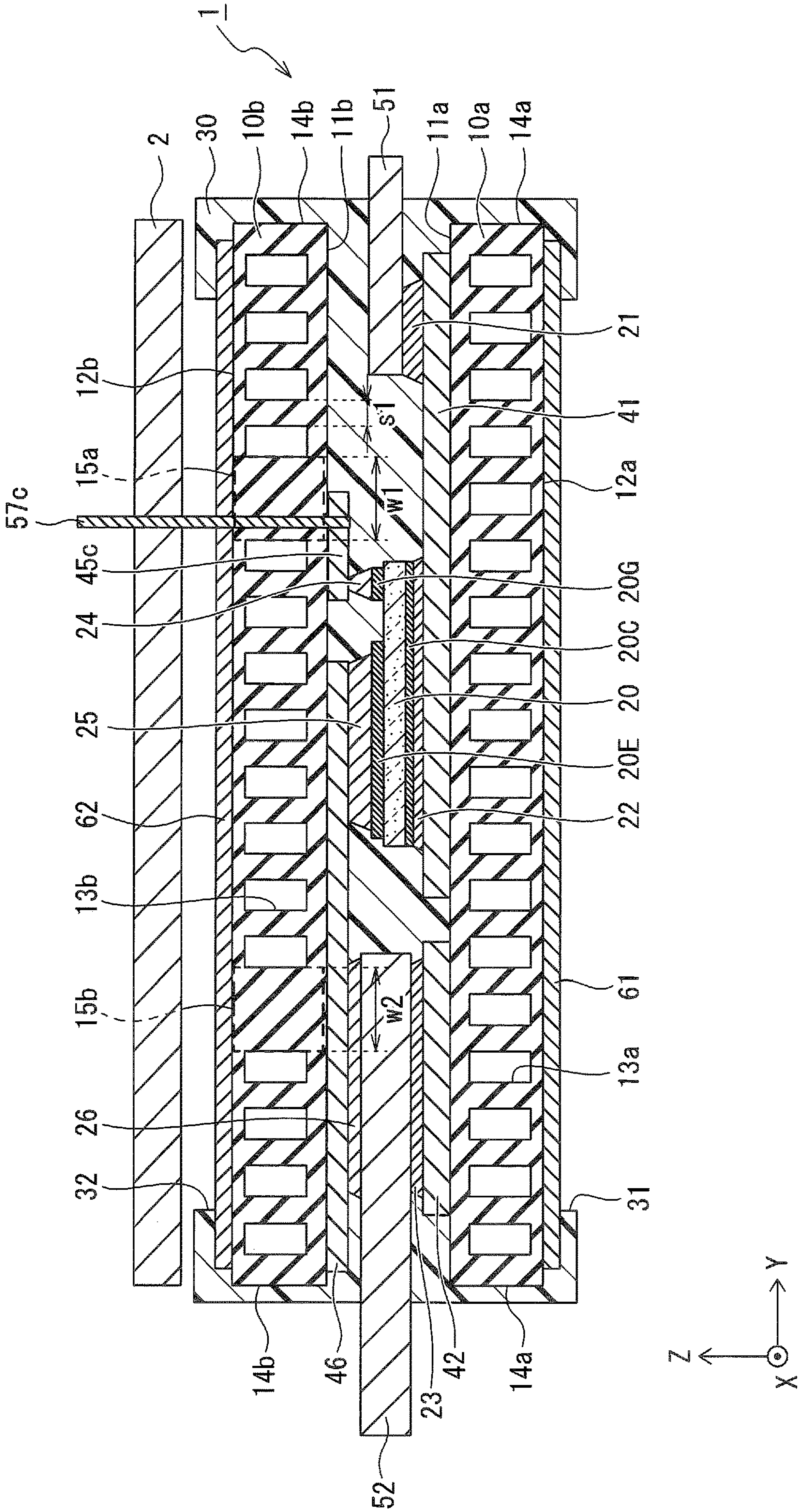

1
2
10b
30
14b
11b
51
11a
10a
14a
21
41
12b
S1
15a
W1
12a
57c
45c
20G
24
20C
20
25
20E
22
13b
15b
W2
13a
26
14b
46
52
23
42
14a
Z
Y
X

FIG. 15



1
2
30
10b
14b
11b
51
11a
10a
14a
21
12b
41
s1
15a
W1
12a
57c
45c
20G
24
20C
25
20
20E
62
22
13b
15b
W2
61
13a
26
32
31
14b
46
23
42
14a
52
Z
Y
X

FIG. 16

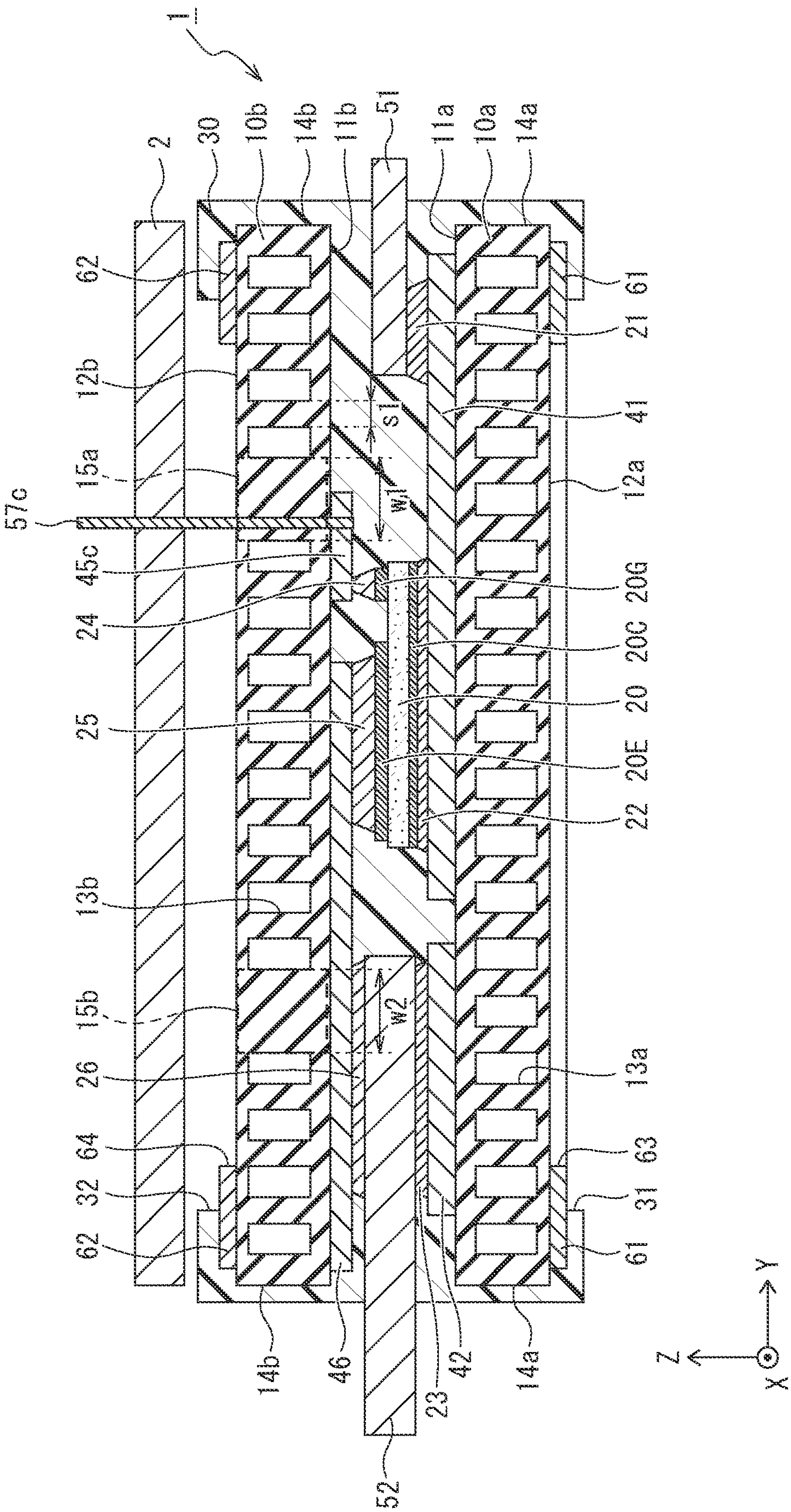

1
2
30
10b
14b
11b
51
11a
10a
14a
62
61
21
12b
s1
41
15a
12a
w1
57c
45c
20G
24
20C
20
25
20E
22
13b
15b
w2
13a
26
64
63
32
31
62
61
14b
46
23
42
14a
52
Z
Y
X

FIG. 17

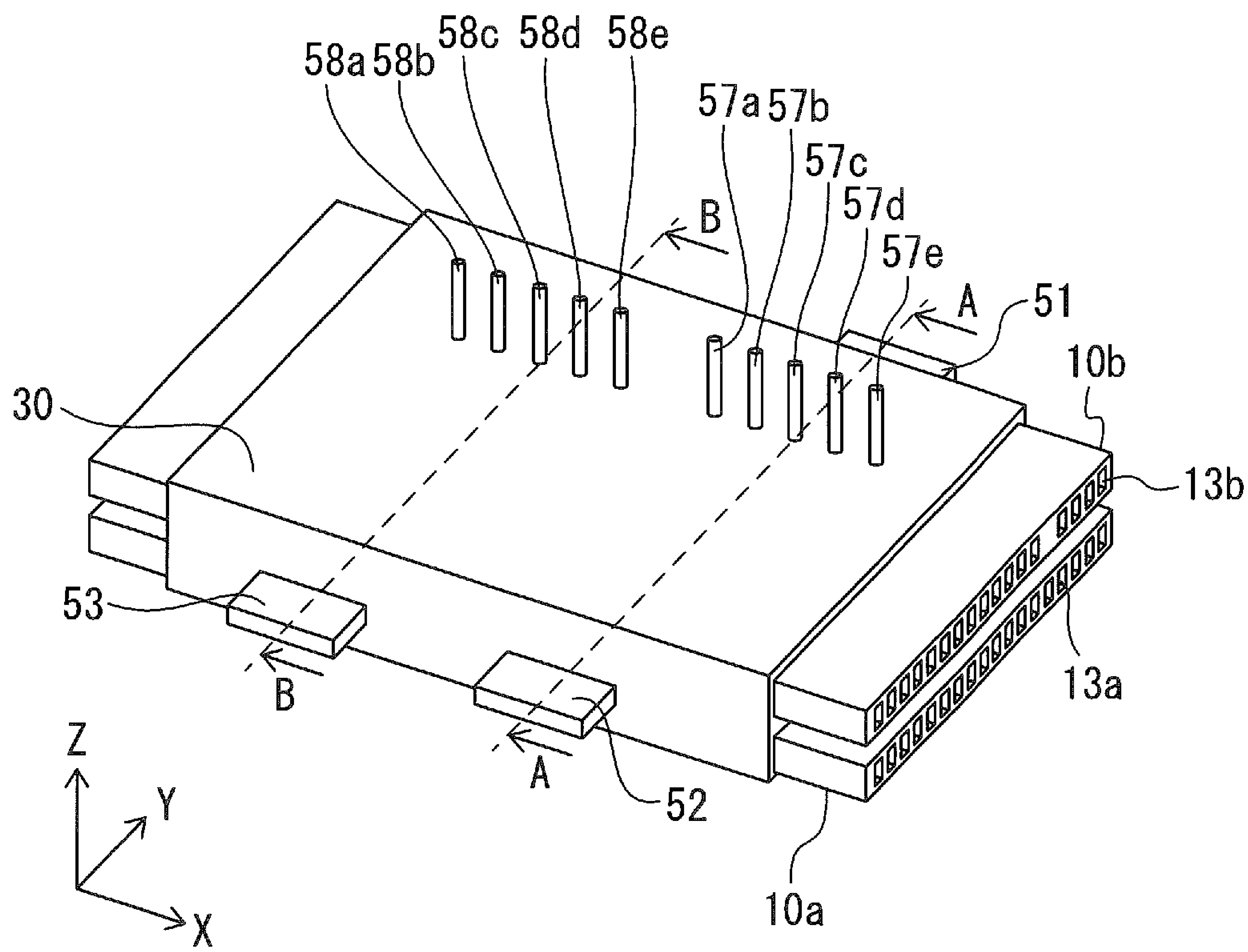

58a
58b
58c
58d
58e
57a
57b
57c
57d
57e
B
A
51
10b
13b
30
13a
53
B
A
52
10a
Z
Y
X

FIG. 18

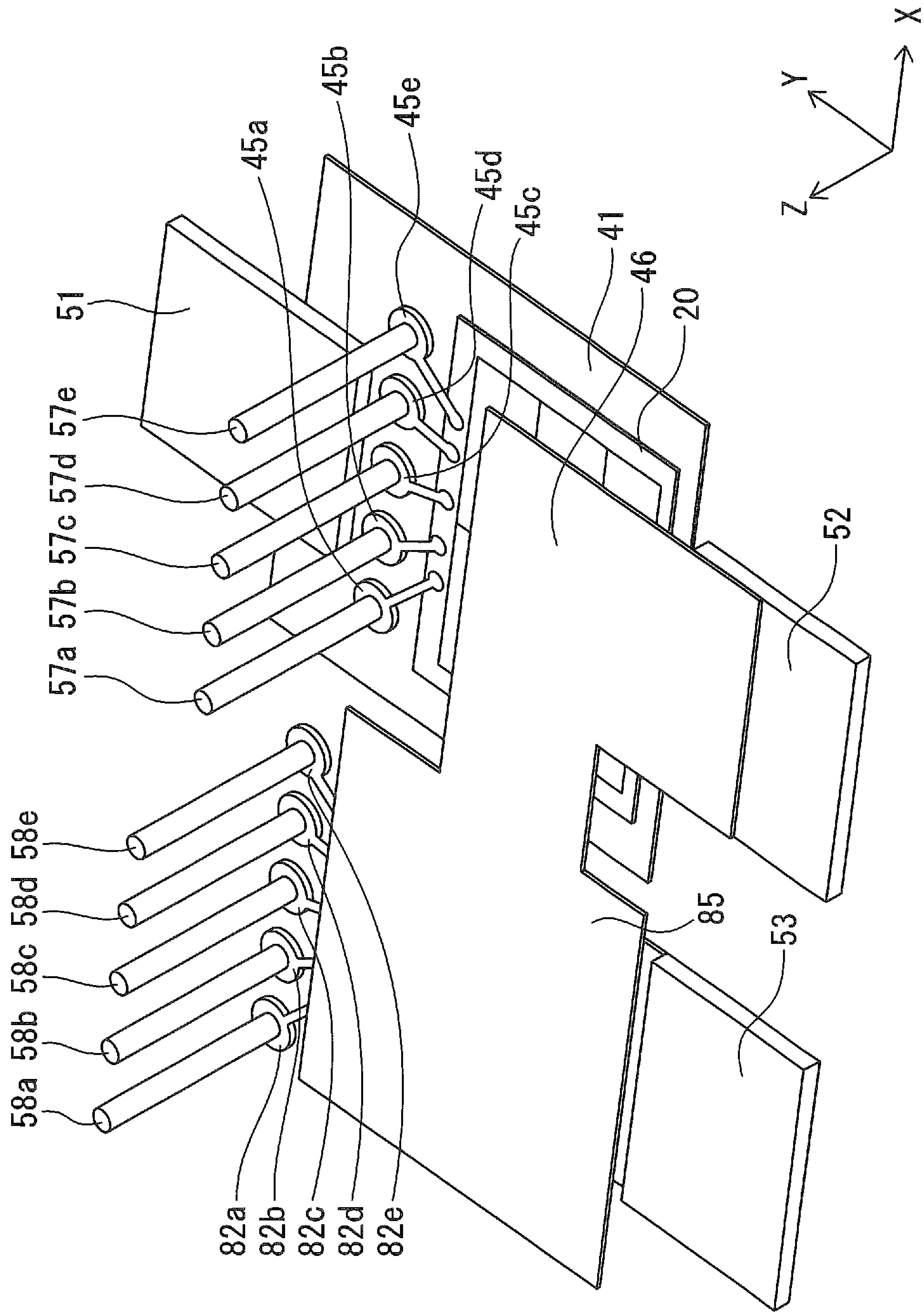
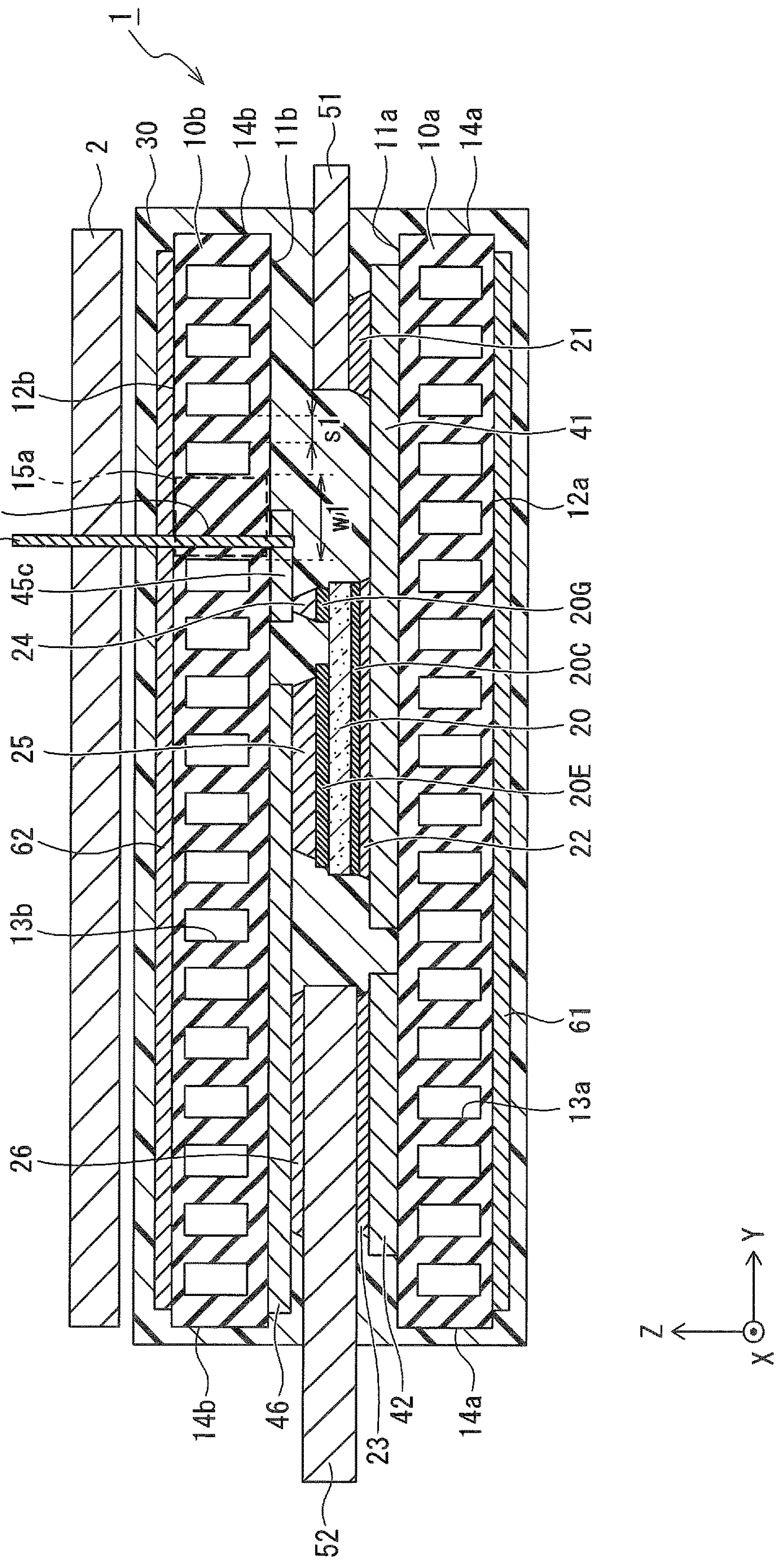

X
Y
Z
45a
45b
45c
45d
45e
41
46
20
51
52
53
57a 57b 57c 57d 57e
58a 58b 58c 58d 58e
82a
82b
82c
82d
82e
85

FIG. 19



1
2
30
10b
14b
11b
51
11a
10a
14a
21
41
12a
20G
20C
20
20E
22
61
13a
12b
15a
16c
57c
45c
24
25
62
13b
26
46
52
23
42
s1
w1
Z
Y
X

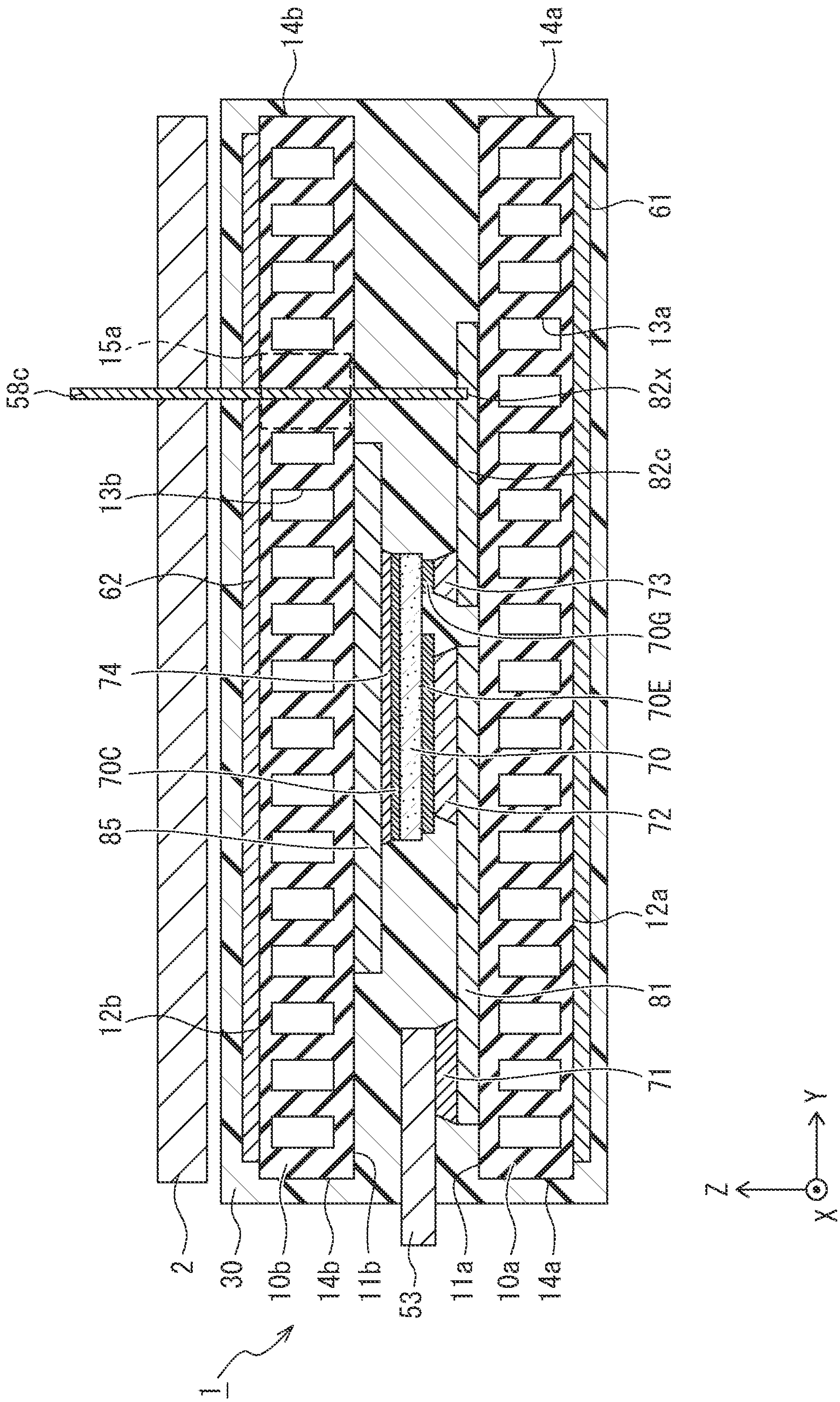

14b
14a
61
15a
13a
58c
82X
82c
13b
62
73
70G
74
70E
70
70C
72
85
12a
12b
81
71
Y
Z
X
2
30
10b
14b
11b
53
11a
10a
14a
1

FIG. 20

FIG. 21

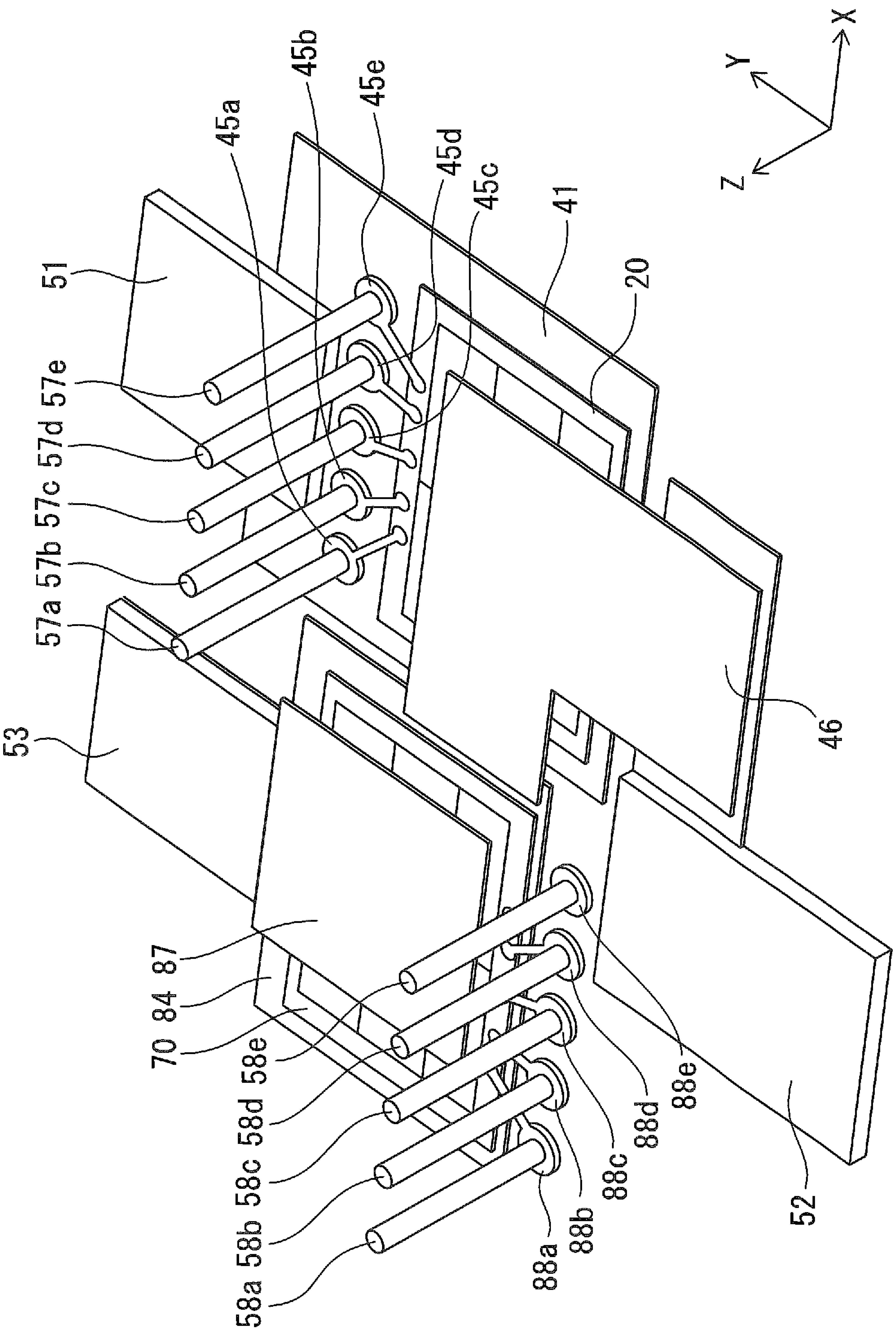

X
Y
Z
51
57a
57b
57c
57d
57e
45a
45b
45e
45d
45c
41
20
46
53
70
84
87
58a
58b
58c
58d
58e
88a
88b
88c
88d
88e
52

FIG. 22

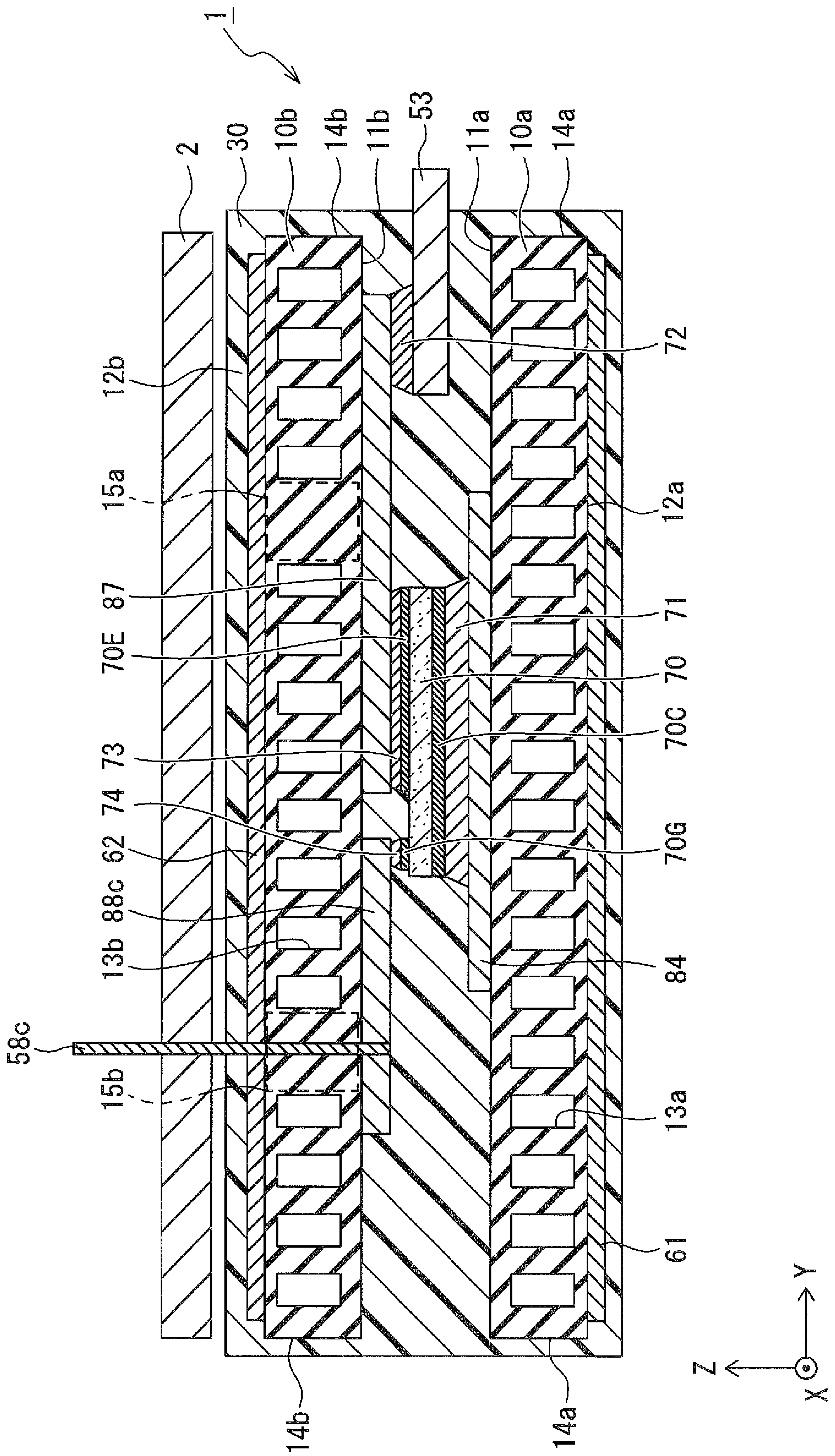
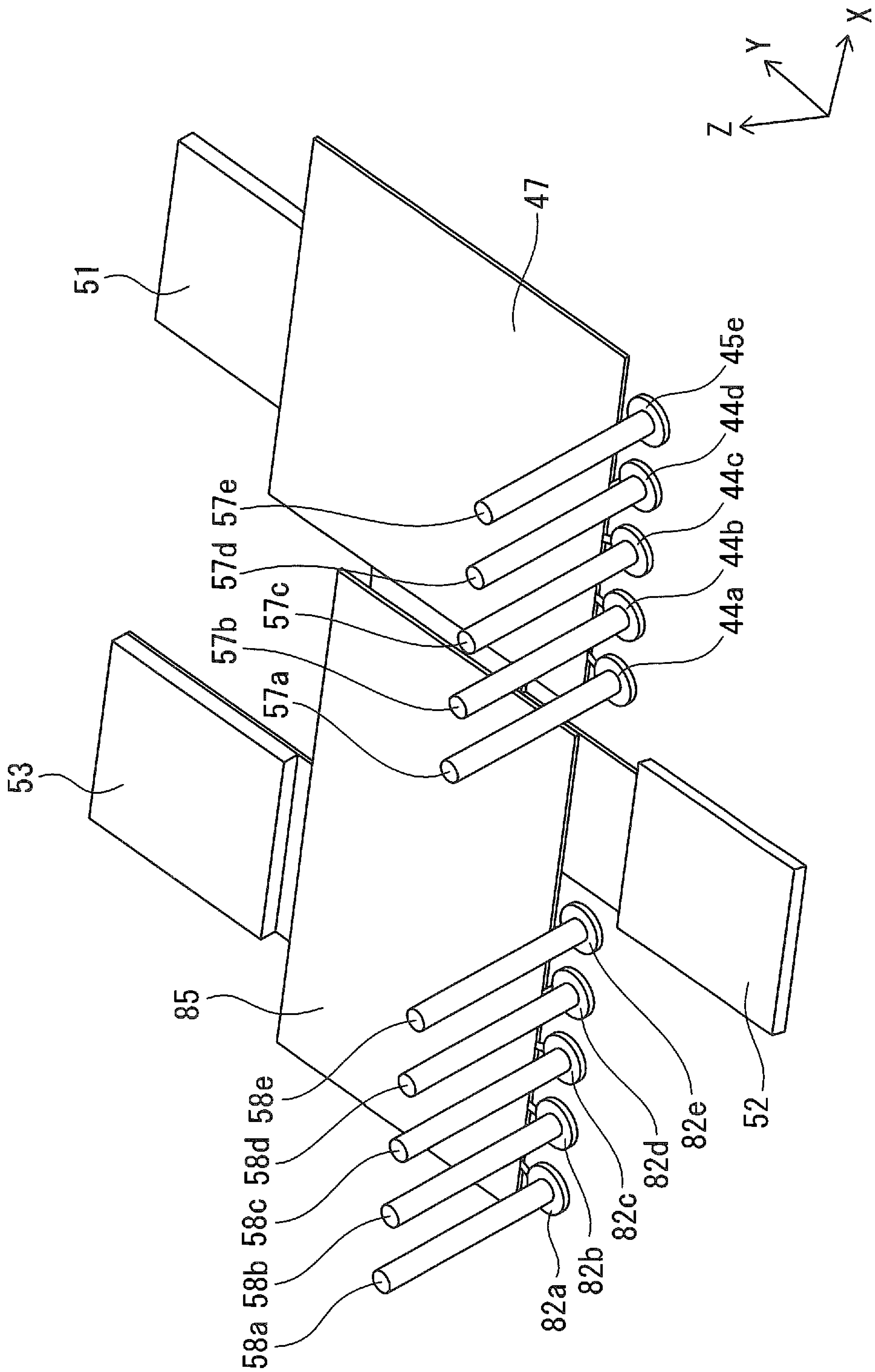

1
2
30
10b
14b
11b
53
11a
10a
14a
72
12b
12a
15a
87
71
70E
70
70C
73
74
70G
62
88c
84
13b
58c
15b
13a
61
14b
14a
Z
Y
X

FIG. 23


X
Y
Z
51
47
53
85
52
57a
57b
57c
57d
57e
44a
44b
44c
44d
45e
58a
58b
58c
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58e
82a
82b
82c
82d
82e

FIG. 24

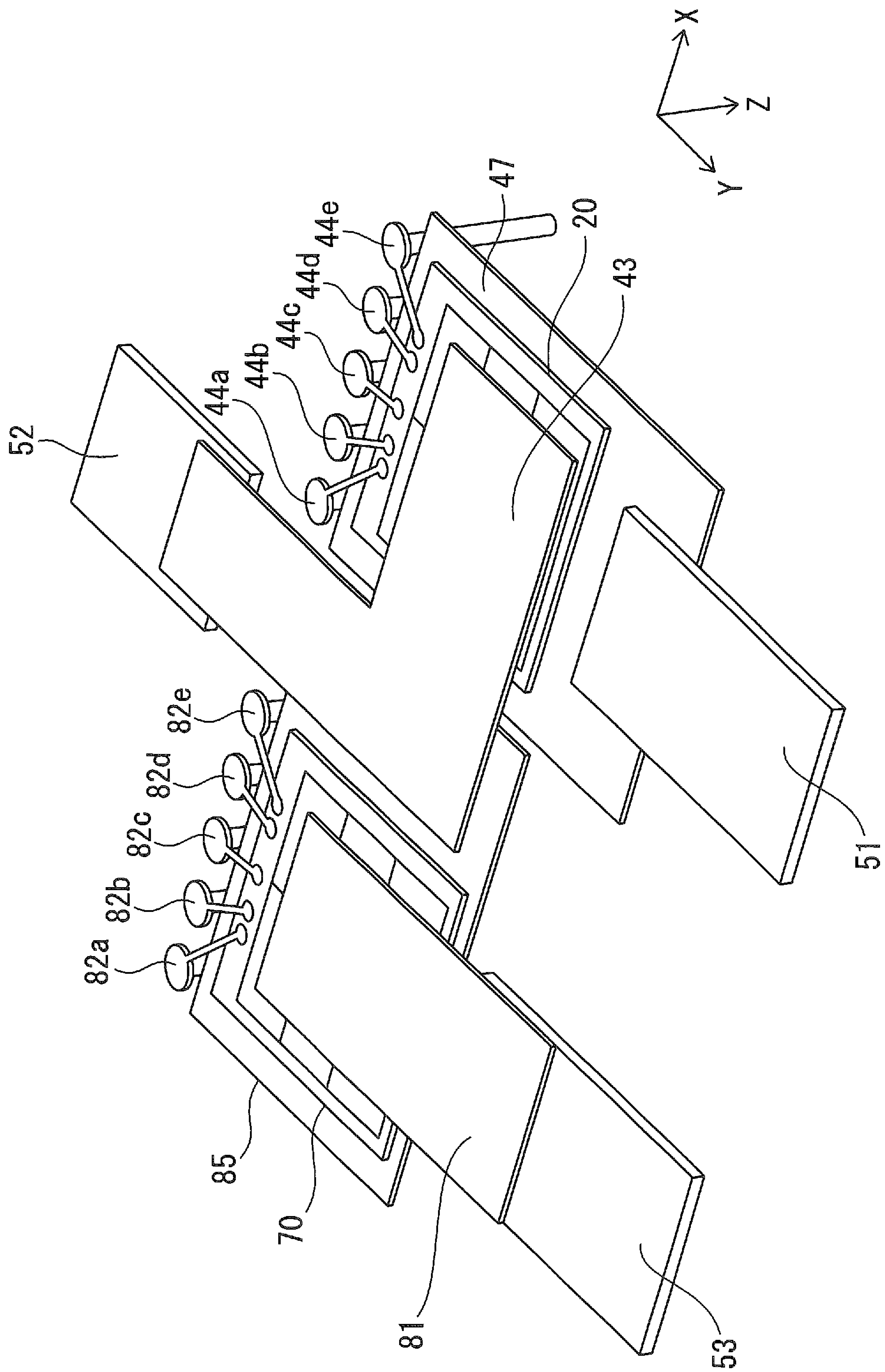

X
Z
Y
47
20
43
44e
44d
44c
44b
44a
52
82e
82d
82c
82b
82a
51
85
70
81
53

FIG. 25

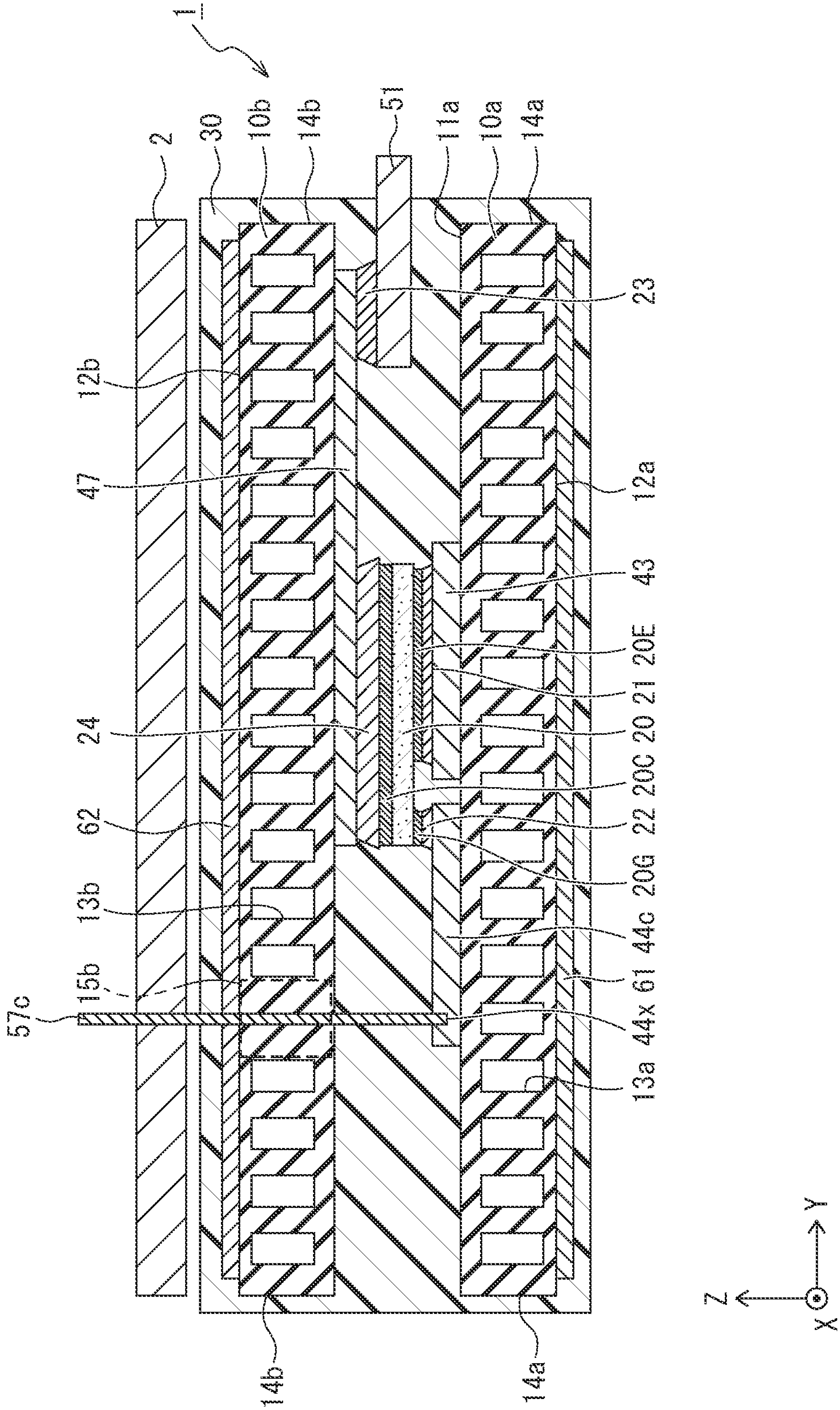
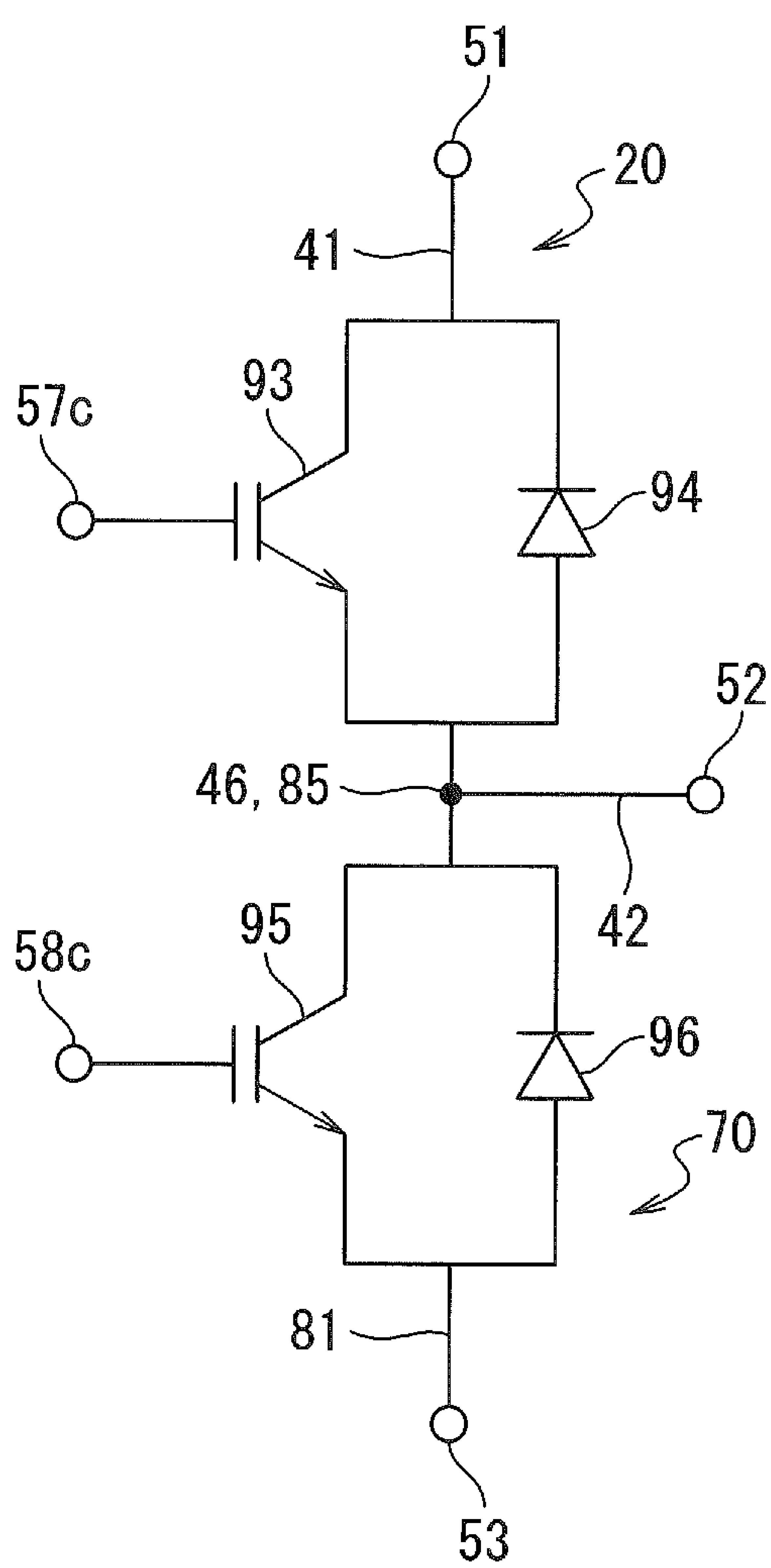

1
2
30
10b
14b
51
11a
10a
14a
23
12b
47
12a
43
20E
21
20
20C
22
20G
44c
61
44x
13a
24
62
13b
15b
57c
14b
14a
Z
Y
X

FIG. 26



SEMICONDUCTOR DEVICE, COOLING MODULE, POWER CONVERTING DEVICE, AND ELECTRIC VEHICLE

CROSS-REFERENCE TO RELATED APPLICATION

This application claims benefit of priority under 35 USC 119 based on Japanese Patent Application No. 2018-103969 filed on May 30, 2018, the entire contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, a cooling module for cooling a semiconductor element included in the semiconductor device, a power converting device including the semiconductor device, and an electric vehicle including the power converting device.

2. Description of the Related Art

Power semiconductor devices are used in motor-drive controlling inverters for elevators, for example, as industrial purposes. Power semiconductor devices have been widely used also in motor-drive controlling inverters for vehicles or DC-DC converters, for example. The power semiconductor devices are required to have a reduced size, high output power, and long-term reliability.

Such a power semiconductor device includes a power semiconductor module, and a cooling device for releasing heat from the power semiconductor module. The power semiconductor module is a semiconductor device including one or more semiconductor elements to implement partial or entire connection for conversion. The respective semiconductor elements included in the power semiconductor module are electrically connected to a control circuit outside the module via main terminals and control terminals. The power semiconductor device preferably has an electrically-insulating structure, excluding the main terminals and the control terminals, to avoid a short circuit.

The power semiconductor device is essentially required to release heat from the semiconductor elements more efficiently, as the power semiconductor device has a smaller size and higher output power. JP 2002-026469A discloses a circuit board including a ceramic substrate with which a coolant is in contact on the rear side, and a circuit pattern arranged on the front side of the ceramic substrate. JP 2008-103623A discloses a semiconductor device including a pair of lead frames interposing a semiconductor element, a resin for sealing the semiconductor element and the lead frames with the respective outer surfaces of the lead frames exposed, and ceramic tubes bonded to the respective outer surfaces of the lead frames.

JP 2002-026469A does not disclose a configuration regarding the main terminals and the control terminals connecting the semiconductor elements to the control circuit outside the module. While JP 2008-103623A discloses that signal terminals are connected to the semiconductor element via a wire bonding and are exposed to the outside between the ceramic tubes opposed to each other, such a configuration reduces the possibility of design of the wire-leading position, which prevents a reduction in size and complicates the wiring design.

SUMMARY OF THE INVENTION

In response to the above issue, the present invention provides a semiconductor device reduced in size and having a configuration capable of expanding the possibility of design of a wire-leading position and facilitating a wiring design, a cooling module for cooling semiconductor elements included in the semiconductor device, a power converting device including the semiconductor device, and an electric vehicle including the power converting device.

An aspect of the present invention discloses a semiconductor device encompassing: a first cooling device including a plurality of first flow channels through which a fluid flows, between a first main surface and a second main surface opposed to each other; a second cooling device including a plurality of second flow channels through which a fluid flows, between a third main surface and a fourth main surface parallel to the first main surface; a semiconductor element interposed between the first main surface and the third main surface facing each other; and a control terminal penetrating from the third main surface to the fourth main surface in a terminal-penetrating region defined at a predetermined position between the plurality of second flow channels, and electrically connected to a control electrode of the semiconductor element.

Another aspect of the present invention discloses a cooling module encompassing: a first cooling device including a plurality of first flow channels through which a fluid flows, between a first main surface and a second main surface opposed to each other; and a second cooling device including a plurality of second flow channels through which a fluid flows, between a third main surface and a fourth main surface parallel to the first main surface, wherein a terminal-penetrating region is defined in the second cooling device through which a control terminal, which is electrically connected to a control electrode of a semiconductor element interposed between the first main surface and the third main surface facing each other, penetrates from the third main surface to the fourth main surface at a predetermined position between the plurality of second flow channels.

Still another aspect of the present invention discloses a power converting device encompassing: a first cooling device including a plurality of first flow channels through which a fluid flows, between a first main surface and a second main surface opposed to each other; a second cooling device including a plurality of second flow channels through which a fluid flows, between a third main surface and a fourth main surface parallel to the first main surface; a semiconductor element interposed between the first main surface and the third main surface facing each other; a control terminal penetrating from the third main surface to the fourth main surface in a terminal-penetrating region defined at a predetermined position between the plurality of second flow channels, and electrically connected to a control electrode of the semiconductor element; a control substrate on which a circuit electrically connected to the control terminal is mounted; and a capacitor arranged toward the second main surface of the first cooling device.

Still another aspect of the present invention discloses an electric vehicle encompassing: a first cooling device including a plurality of first flow channels through which a fluid flows, between a first main surface and a second main surface opposed to each other; a second cooling device including a plurality of second flow channels through which a fluid flows, between a third main surface and a fourth main surface parallel to the first main surface; a semiconductor element interposed between the first main surface and the third main surface facing each other; a control terminal penetrating from the third main surface to the fourth main surface in a terminal-penetrating region defined at a predetermined position between the plurality of second flow channels, and electrically connected to a control electrode of the semiconductor element; a control substrate on which a circuit electrically connected to the control terminal is mounted; a capacitor arranged toward the second main surface of the first cooling device; a power source for supplying electricity to the semiconductor element; and a load driven by the semiconductor element.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a perspective view illustrating a fundamental configuration of a semiconductor device according to an embodiment of the present invention;

FIG. **2** is a cross-sectional view as viewed from direction A-A in FIG. **1**;

FIG. **3**A is a partly-enlarged cross-sectional view of FIG. **2** as an example;

FIG. **3**B is a partly-enlarged cross-sectional view of FIG. **2** as another example;

FIG. **4** is a cross-sectional view as viewed from direction B-B in FIG. **1**;

FIG. **5** is a perspective view omitting cooling devices and a sealing member illustrated in FIG. **1**;

FIG. **6** is a vertically-inverted perspective view corresponding to FIG. **5**;

FIG. **7** is a schematic view illustrating a configuration of an electric vehicle employing the semiconductor device according to the embodiment of the present invention;

FIG. **8** is a cross-sectional view of a semiconductor device according to a comparative example;

FIG. **9** is an explanatory view illustrating a process of fabricating the semiconductor device according to the embodiment of the present invention;

FIG. **10** is an explanatory view illustrating the process of fabricating the semiconductor device according to the embodiment of the present invention;

FIG. **11** is an explanatory view illustrating the process of fabricating the semiconductor device according to the embodiment of the present invention;

FIG. **12** is a top view illustrating a semiconductor device according to a first modified example of the embodiment of the present invention;

FIG. **13** is a cross-sectional view illustrating a semiconductor device according to a second modified example of the embodiment of the present invention;

FIG. **14** is a cross-sectional view illustrating a semiconductor device according to a third modified example of the embodiment of the present invention;

FIG. **15** is a cross-sectional view illustrating a semiconductor device according to a fourth modified example of the embodiment of the present invention;

FIG. **16** is a cross-sectional view illustrating a semiconductor device according to a fifth modified example of the embodiment of the present invention;

FIG. **17** is a perspective view illustrating a semiconductor device according to a sixth modified example of the embodiment of the present invention;

FIG. **18** is a perspective view omitting cooling devices and a sealing member illustrated in FIG. **17**;

FIG. **19** is a cross-sectional view as viewed from direction A-A in FIG. **18**;

FIG. **20** is a cross-sectional view as viewed from direction B-B in FIG. **18**;

FIG. **21** is a perspective view illustrating a semiconductor device according to a seventh modified example of the embodiment of the present invention;

FIG. **22** is a cross-sectional view of the semiconductor device according to the seventh modified example of the embodiment of the present invention;

FIG. **23** is a perspective view illustrating a semiconductor device according to an eighth modified example of the embodiment of the present invention;

FIG. **24** is a vertically-inverted perspective view corresponding to FIG. **23**;

FIG. **25** is a cross-sectional view illustrating the semiconductor device according to the eighth modified example of the embodiment of the present invention; and

FIG. **26** is a circuit diagram illustrating the semiconductor device according to the embodiment of the present invention.

DETAILED DESCRIPTION

With reference to the drawings, embodiments of the present invention will be explained in detail below. In the following description of the drawings, the same or similar reference numerals are assigned to the same or similar portions. The drawings are schematic, and it should be noted that the relationship between thickness and planar dimensions, the thickness proportion of each layer, and the like are different from real ones. Accordingly, specific thicknesses or dimensions should be determined with reference to the following description. Moreover, in some drawings, portions are illustrated with different dimensional relationships and proportions.

Further, definitions of directions such as an up-and down direction in the following description are merely definitions for convenience of understanding, and are not intended to limit the technical ideas of the present invention. For example, as a matter of course, when the subject is observed while being rotated by 90°, the subject is understood by converting the up-and-down direction into the right-and-left direction. When the subject is observed while being rotated by 180°, the subject is understood by inverting the up-and-down direction.

(Semiconductor Device)

A semiconductor device (a semiconductor module) **1** according to an embodiment of the present invention includes a first cooling device **10***a* provided with a plurality of first flow channels **13***a*, and a second cooling device **10***b* provided with a plurality of second flow channels **13***b* and arranged on the top surface side of the first cooling device **10***a*, as illustrated in FIG. **1**. FIG. **1** illustrates the respective first flow channels **13***a* and second flow channels **13***b* extending in parallel to each other and aligned in a direction perpendicular to the extending direction. Each of the first flow channels **13***a* and the second flow channels **13***b* has open ends on both sides in the extending direction.

According to the embodiment of the present invention, as illustrated in FIG. **1**, a longitudinal direction of the first flow channels **13***a* and the second flow channels **13***b* is defined as an X-axis direction (a first direction), a direction perpendicular to the X-axis direction, in which the respective first flow channels **13***a* and second flow channels **13***b* are aligned, is defined as a Y-direction (a second direction), and a direction perpendicular to the X-axis direction and the Y-axis direction is defined as a Z-axis direction. FIG. **1** and the other drawings use a right-handed XYZ coordinate system for illustration purposes. As used in the Specification, the term "planar view" refers to a case in which the top surface of the second cooling device **10***b* is viewed in the positive direction of the Z axis.

The circumference of the first cooling device **10***a* and the second cooling device **10***b* is substantially entirely covered with a sealing member **30**, excluding the regions around the open ends. FIG. **1** illustrates a case in which a plurality of (ten) control terminals **57***a*, **57***b*, **57***c*, **57***d*, **57***e*, **58***a*, **58***b*, **58***c*, **58***d*, and **58***e* project from the sealing member **30** located on the top surface side of the second cooling device **10***b*. The control terminals **57***a* to **57***e* and **58***a* to **58***e* extend in the Z-axis direction, which is a longitudinal direction. The five control terminals **57***a* to **57***e* and the five control terminals **58***a* to **58***e* are separated from each other in the Y-axis direction, and are aligned in the X-axis direction.

The control terminals **57***a* to **57***e* and **58***a* to **58***e* may be cylindrical conductive pins, for example. The control terminals **57***a* to **57***e* and **58***a* to **58***e* are not limited to the cylindrical shape, and may each be a polygonal prism. The control terminals **57***a* to **57***e* and **58***a* to **58***e* are made of metal such as copper (Cu) or a Cu alloy. The control terminals **57***a* to **57***e* and **58***a* to **58***e* may be plated with metal or an alloy of nickel (Ni), tin (Sn), or gold (Au), for example.

The first cooling device **10***a* and the second cooling device **10***b* are made of an insulating material such as ceramics. An example of ceramics used as the insulating material may be a material having high heat conductivity, such as silicon carbide (SiC), silicon nitride (Si_3N_4), aluminum nitride (AlN), alumina (Al_2O_3), titania (TiO_2), or zirconia (ZrO_2). The first cooling device **10***a* and the second cooling device **10***b* may be made of the same material or different materials.

FIG. **2** is a cross-sectional view as viewed from direction A-A in FIG. **1**. As illustrated in FIG. **2**, the first cooling device **10***a* has a first main surface (a top surface) **11***a* and a second main surface (a bottom surface) **12***a* opposed to each other. The first cooling device **10***a* may have a rectangular plate-like shape. The first cooling device **10***a* includes the plurality of first flow channels **13***a* through which a fluid serving as a coolant flows, between the first main surface **11***a* and the second main surface **12***a*. The fluid flowing through the respective first flow channels **13***a* may be liquid such as ethylene glycol aqueous solution or water, or gas such as air. Another example of the fluid flowing through the respective first flow channels **13***a* may be a phase-changeable coolant such as chlorofluorocarbon. The first cooling device **10***a* has two side surfaces **14***a* opposed to each other at both ends in the aligned direction of the first flow channels **13***a* (in the Y-axis direction). The plural first flow channels **13***a* are aligned in the direction parallel to the first main surface **11***a*. The size, the number, and the intervals of the first flow channels **13***a* may be determined as appropriate. For example, the respective first flow channels **13***a* have the common shape and are arranged at regular intervals.

The second cooling device **10***b* has a third main surface (a bottom surface) **11***b* and a fourth main surface (a top surface) **12***b* parallel to the first main surface and opposed to each other. The first main surface **11***a* of the first cooling device **10***a* and the third main surface **11***b* of the second cooling device **10***b* face each other. The second cooling device **10***b* may have a rectangular plate-like shape. The second cooling device **10***b* includes the plurality of second flow channels **13***b* through which a fluid serving as a coolant flows, between the third main surface **11***b* and the fourth main surface **12***b*. The coolant flowing through the respective second flow channels **13***b* may be the same as that flowing through the respective first flow channels **13***a*. The second cooling device **10***b* has two side surfaces **14***b* opposed to each other at both ends in the aligned direction of the second flow channels **13***b* (in the Y-axis direction). The plural second flow channels **13***b* are aligned in line in the direction parallel to the aligned direction of the first flow channels **13***a*.

The first main surface **11***a* of the first cooling device **10***a* and the third main surface **11***b* of the second cooling device **10***b* in the semiconductor device **1** may be parallel to each other. A first semiconductor element **20** and a second semiconductor element **70** (refer to FIG. **4**) are arranged to be interposed between the first main surface **11***a* of the first cooling device **10***a* and the third main surface **11***b* of the second cooling device **10***b*. The first semiconductor element **20** has two main surfaces opposed to each other. One of the main surfaces of the first semiconductor element **20** is provided with a first main electrode **20**E and a control electrode **20**G, and the other main surface is provided with a second main electrode **20**C. The second semiconductor element **70** has two main surfaces opposed to each other. One of the main surfaces of the second semiconductor element **70** is provided with a first main electrode **70**E and a control electrode **70**G, and the other main surface is provided with a second main electrode **70**C.

The size, the number, and the intervals s**1** of the respective second flow channels **13***b* may be determined as appropriate, and may be the same as or different from the size, the number, and the intervals of the respective first flow channels **13***a*. The respective second flow channels **13***b* have the common shape and are arranged substantially at regular intervals s**1**, at least at the portions in which the second flow channels **13***b* are provided.

The semiconductor device **1** according to the embodiment of the present invention includes regions in which the second flow channels **13***b* are intentionally not provided in the second cooling device **10***b*, at predetermined positions between the third main surface **11***b* and the fourth main surface **12***b*. The semiconductor device **1** according to the embodiment of the present invention employs the regions, as "terminal-penetrating regions **15***a* and **15***b*", in which the second flow channels **13***b* are not provided intentionally. The terminal-penetrating regions **15***a* and **15***b* extend in the X-axis direction parallel to the respective second flow channels **13***b*.

The terminal-penetrating region **15***a* is provided with a penetration hole **16***c* through which the control terminal **57***c* penetrates. The terminal-penetrating region **15***a* is further provided with penetration holes (not illustrated) through which the other control terminals **57***a*, **57***b*, **57***d*, and **57***e* illustrated in FIG. **1** penetrate. The terminal-penetrating region **15***b* is provided with penetration holes (not illustrated) through which the control terminals **58***a* to **58***e* illustrated in FIG. **1** penetrate. The width w**1** of the terminal-penetrating region **15***a* and the width w**2** of the terminal-penetrating region **15***b* defined in FIG. **2** are both wider than each interval s**1** of the second flow channels **13***b*. The width w**1** of the terminal-penetrating region **15***a* and the width w**2** of the terminal-penetrating region **15***b* may be the same or different from each other.

FIG. **2** illustrates a case in which first conductive pattern layers **41** and **42** composing wiring circuits are bonded to the first main surface **11***a* of the first cooling device **10***a*. The first conductive pattern layers **41** and **42** include copper (Cu), and are bonded to the first main surface **11***a* of the first cooling device **10***a* by a direct copper bonding (DCB) method due to eutectic bonding or an activated metal brazing (AMB) method, for example. The first conductive pattern layers **41** and **42** are only required to include conductive metal, and may be Cu, a Cu alloy, aluminum (Al), or an Al alloy. The first conductive pattern layers **41** and **42** may be plated with nickel (Ni) or gold (Au).

One end of a first main terminal **51** is bonded to the top surface of the first conductive pattern layer **41** via a bonding material **21**. The other end of the first main terminal **51** is exposed to the outside of the sealing member **30**, and can be connected to a power source. The second main electrode **20**C of the first semiconductor element **20** is also bonded and electrically connected to the top surface of the first conductive pattern layer **41** via a bonding material **22**. One end of a second main terminal **52** is bonded to the top surface of the first conductive pattern layer **42** via a bonding material **23**. The second main terminal **52** extends in the horizontal direction (in the Y-axis direction). The other end of the second main terminal **52** is exposed to the outside of the sealing member **30**, and can be connected to a load such as a motor.

The first main terminal **51** and the second main terminal **52** may each be a conductive plate or a conductive stick made of metal such as Cu or a Cu alloy. The first main terminal **51** and the second main terminal **52** may be plated with Ni or Au, for example. The bonding materials **21**, **22**, and **23** may each be a solder, an electrically-conductive adhesive, or a metal sintered body such as nanoparticles of silver (Ag), for example.

FIG. **2** illustrates a plurality of second conductive pattern layers **45***c* and **46** bonded to the third main surface **11***b* of the second cooling device **10***b*. The second conductive pattern layers **45***c* and **46** are bonded to the second cooling device **10***b* by a DCB method due to eutectic bonding or an AMB method, for example, as in the case of the first conductive pattern layers **41** and **42**. The second conductive pattern layers **45***c* and **46** are only required to include conductive metal, and may be Cu, a Cu alloy, Al, or an Al alloy. The second conductive pattern layers **45***c* and **46** may be plated with Ni or Au.

For example, one end of the second conductive pattern layer **46** is bonded and electrically connected to the first main electrode **20**E of the first semiconductor element **20** via a bonding material **25**. The other end of the second conductive pattern layer **46** is bonded to one end of the second main terminal **52** via a bonding material **26**. One end of the second conductive pattern layer **45***c* is bonded and electrically connected to the control electrode **20**G of the first semiconductor element **20** via a bonding material **24**. The other end of the second conductive pattern layer **45***c*, which is separated from the part bonded to the control electrode **20**G, is connected to the control terminal **57***c*. The other end of the second conductive pattern layer **45***c* connected to the control terminal **57***c* is located in the terminal-penetrating region **15***a* of the second cooling device **10***b*. The bonding materials **24**, **25**, and **26** may be a solder, an electrically-conductive adhesive, or a metal sintered body such as Ag nanoparticles, for example. The bonding material **24** may be an electrically-conductive bump or a solder ball.

The control terminal **57***c* extends in the normal direction of the first main surface **11***a* (in the Z-axis direction), and penetrates from the third main surface **11***b* to the fourth main surface **12***b* in the second cooling device **10***b* within the terminal-penetrating region **15***a* in which the second flow channels **13***b* of the second cooling device **10***b* are not provided. The control terminal **57***c* may extend above the fourth main surface **12***b* of the second cooling device **10***b* to project to the outside of the sealing member **30** so as to be connected to a control substrate **2**. The control substrate **2** may be arranged above the semiconductor device **1** using screws (not illustrated). A circuit electrically connected to the control terminal **57***c* is mounted on the control substrate **2**. The control substrate **2** supplies a control signal to the control electrode **20**G of the first semiconductor element **20** via the control terminal **57***c*. The other control terminals **57***a*, **57***b*, **57***d*, and **57***e* illustrated in FIG. **1** may also penetrate the terminal-penetrating region **15***a* illustrated in FIG. **2** so as to be connected to the control substrate **2**, in the same manner as the control terminal **57***c*.

FIG. **3**A is a partly-enlarged view around the lower end portion of the control terminal **57***c* illustrated in FIG. **2**. As illustrated in FIG. **3**A, the second conductive pattern layer **45***c* is continuously provided along the inside of the penetration hole **16***c* of the second cooling device **10***b* from the third main surface **11***b* of the second cooling device **10***b* so as to define the side wall surface of the penetration hole **16***c* through which the control terminal **57***c* penetrates. The second conductive pattern layer **45***c* further projects onto the top surface of a second buffer film **62** on the fourth main surface **12***b* side of the second cooling device **10***b* through the side wall of the penetration hole **16***c* of the second cooling device **10***b*. The second conductive pattern layer **45***c* provided along the side wall of the penetration hole **16***c* of the second cooling device **10***b* defines the penetration hole into which the control terminal **57***c* can be inserted.

The control terminal **57***c* is a stepped pin including a first part **571** on the second substrate **2** side and a second part **572** connected to the first part **571** and narrower than the first part **571**, for example. The control terminal **57***c* is not limited to this shape, and is only required to be fixed while being in contact with the second conductive pattern layer **45***c*. For example, as illustrated in FIG. **3**B, the control terminal **57***c* may be a cylindrical pin or a polygonal prism-like pin having a constant thickness with no step. The control terminal **57***c* having such a shape is also inserted in the second cooling device **10***b* in the early stage of the manufacturing process, for example, so as to be positioned appropriately in the thickness direction.

A semiconductor chip composing the first semiconductor element **20** illustrated in FIG. **2** may have a rectangular plate-like shape, for example. The first semiconductor element **20** is made of a material such as silicon (Si), SiC, or gallium nitride (GaN). The first semiconductor element **20** may be a transistor such as a bipolar junction transistor (BJT), a field-effect transistor (FET), or a static induction transistor (SIT). Alternatively, the first semiconductor element **20** may be a semiconductor switching element such as an insulated-gate bipolar transistor (IGBT), a static induction thyristor (SI thyristor), or a gate turn-off thyristor (GTO). The first semiconductor element **20** may include a plurality of semiconductor elements, or may be a monolithic power integrated circuit (IC) including a diode such as Schottky barrier diode, or an IC or a module having a hybrid structure. The first semiconductor element **20** may be a reverse conducting IGBT (RC-IGBT) in which an IGBT as a switching element and a freewheeling diode (FWD) as a protection diode for the IGBT are formed on the same semiconductor chip.

When the first semiconductor element **20** is a BJT, the first main electrode refers to either an emitter electrode or a collector electrode, the second main electrode refers to the other electrode, and the control electrode refers to a base electrode. When the first semiconductor element **20** is a FET, for example, the first main electrode refers to either a source electrode or a drain electrode, the second main electrode refers to the other electrode, and the control electrode refers to a gate electrode. When the first semiconductor element **20** is a SI thyristor, for example, the first main electrode refers to either an anode or a cathode, the second main electrode refers to the other electrode, and the control electrode refers to a gate electrode.

The first semiconductor element **20** has two main surfaces (chip surfaces) opposed to each other. The respective main surfaces (the respective chip surfaces) of the first semiconductor element **20** are opposed to the first main surface **11***a* and the third main surface **11***b* via at least a part of the respective first conductive pattern layers **41** and **42** and at least a part of the respective second conductive pattern layers **45***c* and **46**. The first semiconductor element **20** has a vertical structure in which the first main electrode (the emitter electrode) **20**E and the second main electrode (the collector electrode) **20**C are placed on the respective main surfaces (the respective chip surfaces) opposed to each other, for example. The first semiconductor element **20** may have a structure including the control electrode (the gate electrode) **20**G arranged on the same main surface (the chip surface) on which the first main electrode **20**E is placed.

The second main electrode **20**C located on the bottom surface of the first semiconductor element **20** is bonded to the first conductive pattern layer **41** via the bonding material **22**. The first main electrode **20**E located on the top surface of the first semiconductor element **20** is bonded to the second conductive pattern layer **46** via the bonding material **25**. When the first semiconductor element **20** has the structure including the control electrode **20**G arranged on the same main surface (the same chip surface) as the first main electrode **20**E, the control electrode **20**G located on the top surface of the first semiconductor element **20** is bonded to the second conductive pattern layer **45***c* via the bonding material **24**.

The second flow channels **13***b* of the second cooling device **10***b* are located at least at a position overlapping with the first main electrode **20**E of the first semiconductor element **20** arranged on the same main surface as the control electrode **20**G, in the aligned direction of the second flow channels **13***b* (in the Y-axis direction) in the planar view. The respective terminal-penetrating regions **15***a* and **15***b* are located on the outer side of the position overlapping with the first main electrode **20**E in the aligned direction of the second flow channels **13***b* (in the Y-axis direction) in the planar view.

Since heat generated from the first semiconductor element **20** is released by the coolant flowing through the first cooling device **10***a* and the second cooling device **10***b* arranged toward the respective main surfaces of the first semiconductor element **20**, the cooling performance is improved as compared with a case in which the cooling device is arranged only on one surface of the first semiconductor element **20**.

A first buffer film **61** may be bonded to the second main surface **12***a*, which is the bottom surface of the first cooling device **10***a*, located on the lower side in FIG. **2**. The first buffer film **61** bonded to the second main surface **12***a* connects the second main surface **12***a* and the sealing member **30** between one end and the other end in the aligned direction of the first flow channels **13***a*. A second buffer film **62** may be bonded to the fourth main surface **12***b*, which is the top surface of the second cooling device **10***b*, located on the upper side in FIG. **2**. The second buffer film **62** bonded to the fourth main surface **12***b* connects the fourth main surface **12***b* and the sealing member **30** between one end and the other end in the aligned direction of the second flow channels **13***b*.

The first buffer film **61** and the second buffer film **62** illustrated in FIG. **2** each may be a single film or may be divided into parts. The thickness of the first buffer film **61** and the second buffer film **62** can be preferably 0.1 millimeters or greater and 5.0 millimeters or less, more preferably 0.2 millimeters or greater and 2.5 millimeters or less.

When the material used for the first cooling device **10***a* and the second cooling device **10***b* is ceramics, for example, the material used for the first buffer film **61** and the second buffer film **62** is preferably metal having a higher thermal expansion coefficient than ceramics. The first buffer film **61** and the second buffer film **62** include Cu or a Cu alloy, for example, and are bonded to the second main surface **12***a* and the fourth main surface **12***b* by a DCB method due to eutectic bonding or an AMB method, for example. The first buffer film **61** and the second buffer film **62** may be made of the same material as the first conductive pattern layers **41** and **42** and the second conductive pattern layers **45***c* and **46**. Alternatively, the first buffer film **61** and the second buffer film **62** may include Al or an Al alloy, Ni or a Ni alloy, or stainless steel, for example, instead of Cu or the Cu alloy. The first buffer film **61** and the second buffer film **62** may also be plated with Ni or Au, for example.

The first buffer film **61** and the second buffer film **62** may have slits on the respective surfaces adhering to the sealing member **30**. The slits may be provided in parallel to the longitudinal direction of the first flow channels **13***a* and the second flow channels **13***b*, for example. The slits may be grooves carved on the surfaces of the first buffer film **61** and the second buffer film **62**, or may penetrate from the front side to the rear side of the first buffer film **61** and the second buffer film **62**. The slits having an anchoring effect improve the adhesion of the first buffer film **61** and the second buffer film **62** to the sealing member **30**.

The sealing member **30** seals the first semiconductor element **20**, the first conductive pattern layers **41** and **42**, and the second conductive pattern layers **45***c* and **46**. The sealing member **30** includes thermosetting resin and filler. The thermosetting resin is epoxy resin or resin mainly containing epoxy resin, for example. The filler is powder of insulating inorganic material such as silica, for example.

The sealing member **30** is arranged to surround the circumferential surfaces of the first cooling device **10***a* and the second cooling device **10***b* in the cross-sectional view perpendicular to the longitudinal direction of the first flow channels **13***a* and the second flow channels **13***b*. The sealing member **30** has a cuboidal shape with two surfaces opposed to the second main surface **12***a* of the first cooling device **10***a* and the fourth main surface **12***b* of the second cooling device **10***b*.

FIG. **4** is a cross-sectional view as viewed from direction B-B in FIG. **1**. As illustrated in FIG. **4**, first conductive pattern layers **81** and **82***c* are bonded to the first main surface **11***a* of the first cooling device **10***a*. One end of a third main terminal **53** is bonded to the first conductive pattern layer **81** via a bonding material **71**. The third main terminal **53** extends in the horizontal direction (in the Y-axis direction). The other end of the third main terminal **53** is exposed to the outside of the sealing member **30**, and can be connected to the power source, for example. A second conductive pattern layer **85** is connected to the third main surface **11***b* of the second cooling device **10***b*. The second conductive pattern layer **85** is connected to the second conductive pattern layer **46** illustrated in FIG. **2** at a position on the front side in the direction perpendicular to the sheet of FIG. **4** (in the X-axis direction).

The semiconductor device **1** according to the embodiment of the present invention includes the second semiconductor element (the second semiconductor chip) **70** as illustrated in FIG. **4**, in addition to the first semiconductor element **20** illustrated in FIG. **2**. The semiconductor device **1** according to the embodiment of the present invention is thus a 2-in-1 power semiconductor module. The second semiconductor element **70** may have the same structure as the first semiconductor element **20**. The second semiconductor element **70** has a vertically-inverted topology of the first semiconductor element **20**. The second semiconductor element **70** includes the first main electrode **70**E and the control electrode **70**G on the bottom surface side, and the second main electrode **70**C on the top surface side.

The second main electrode **70**C located on the top surface of the second semiconductor element **70** is bonded to the second conductive pattern layer **85** via a bonding material **74**. The second main electrode **70**C of the semiconductor element composing the second semiconductor element **70** is thus connected to the first main electrode **20**E of the semiconductor element composing the first semiconductor element **20**. The first main electrode **70**E located on the bottom surface of the second semiconductor element **70** is bonded to the first conductive pattern layer **81** via a bonding material **72**. The control electrode **70**G located on the bottom surface of the second semiconductor element **70** is bonded to one end of the first conductive pattern layer **82***c* via a bonding material **73**.

The other end of the first conductive pattern layer **82***c* is provided with a recess **82***x*. A penetration hole penetrating the first conductive pattern layer **82***c* may be provided instead of the recess **82***x*. The control terminal **58***c* is inserted and bonded to the recess **82***x* of the first conductive pattern layer **82***c*. The control terminal **58***c* is bonded to the first conductive pattern layer **82***c* by pressure welding or with a bonding material such as a solder, for example.

The control terminal **58***c* extends in the normal direction of the first main surface **11***a* (in the Z-axis direction), and penetrates from the third main surface **11***b* to the fourth main surface **12***b* in the second cooling device **10***b* within the terminal-penetrating region **15***b* in which the second flow channels **13***b* of the second cooling device **10***b* are not provided. The control terminal **58***c* projects to the outside of the sealing member **30** above the fourth main surface **12***b* of the second cooling device **10***b* so as to be connected to the control substrate **2**. The other control terminals **58***a*, **58***b*, **58***d*, and **58***e* illustrated in FIG. **1** also penetrate from the third main surface **11***b* to the fourth main surface **12***b* in the second cooling device **10***b* so as to be connected to the control substrate **2**, in the same manner as the control terminal **58***c*.

FIG. **5** is a perspective view of the semiconductor device **1**, omitting the first cooling device **10***a*, the second cooling device **10***b*, and the sealing member **30** illustrated in FIG. **1**. FIG. **6** is an inverted perspective view of FIG. **5** vertically inverted about a rotation axis in the X-axis direction. As illustrated in FIG. **5** and FIG. **6**, the control terminals **57***a*, **57***b*, **57***c*, **57***d*, and **57***e* are respectively connected to the second conductive pattern layers **45***a*, **45***b*, **45***c*, **45***d*, and **45***e*. The second conductive pattern layers **45***a* to **45***e* each include a circular land bonded to the respective control terminals **57***a* to **57***e*, and a wiring part extending from the land and connected to the first semiconductor element **20**. The lands and the wiring parts of the control terminals **57***a* to **57***e* may be provided in the terminal-penetrating region **15***a* of the second cooling device **10***b*.

The control terminals **58***a*, **58***b*, **58***c*, **58***d*, and **58***e* are respectively connected to the first conductive pattern layers **82***a*, **82***b*, **82***c*, **82***d*, and **82***e*. The first conductive pattern layers **82***a* to **82***e* each include a circular land bonded to the respective control terminals **58***a* to **58***e*, and a wiring part extending from the land and connected to the second semiconductor element **70**. The lands and the wiring parts of the control terminals **58***a* to **58***e* may be provided in a region of the first cooling device **10***a* opposed to the terminal-penetrating region **15***b* of the second cooling device **10***b*.

The semiconductor device **1** according to the embodiment of the present invention may be used for a power converting device for driving a motor **3** of an electric vehicle **100**, as illustrated in FIG. **7**. The power converting device for driving the motor **3** of the electric vehicle **100** includes the semiconductor device **1** and the control substrate **2** arranged above the semiconductor device **1**. A capacitor **4** is placed on the bottom surface of the semiconductor device **1**. The capacitor **4** may be a smoothing capacitor for stabilizing a DC voltage output from the converter, for example. The semiconductor device **1** and the capacitor **4** are connected to a power source **5**. The semiconductor device **1** and the capacitor **4** are connected to a load such as the motor **3** to fabricate the electric vehicle **100**. In a case of a three-phase inverter, the power converting device may be implemented by three 2-in-1 power semiconductor modules. The power converting device according to the embodiment of the present invention can cool the capacitor **4** arranged adjacent to the semiconductor device **1** by the first cooling device **10***a* of the semiconductor device **1**.

As illustrated in FIG. **26**, the first semiconductor element **20**, the second semiconductor element **70**, the first conductive pattern layers **41**, **42**, and **81**, the second conductive pattern layers **46** and **85**, the first main terminal **51**, the second main terminal **52**, and the third main terminal **53** included in the semiconductor device **1**, may be arranged and electrically connected to each other such that the first semiconductor element **20** and the second semiconductor element **70** are connected in series to implement a circuit (a leg). The first semiconductor element **20** and the second semiconductor element **70** of this example may each be a RC-IGBT.

The first semiconductor element **20** may include an IGBT **93** and a FWD **94**. A gate of the IGBT **93** may be connected to the control terminal **57***c*. The second semiconductor element **70** may include an IGBT **95** and a FWD **96**. A gate of the IGBT **95** may be connected to the control terminal **58***c*.

A semiconductor device according to a comparative example is illustrated below with reference to FIG. **8**. The semiconductor device according to the comparative example includes a first cooling device **101***a* provided with a plurality of first flow channels **110***a*, and a second cooling device **101***b* provided with a plurality of second flow channels **110***b*. The bottom surface of the second cooling device **101***b* is opposed to the top surface of the first cooling device **101***a*. A conductive pattern layer **107** is placed on the top surface of the first cooling device **101***a* via an insulating substrate **109***a*. The conductive pattern layer **107** is bonded to the bottom surface of a semiconductor element **120** via a bonding material **121**. A conductive pattern layer **108** is placed on the bottom surface of the second cooling device **101***b* via an insulating substrate **109***b*. A main terminal **104** is bonded to one end of the conductive pattern layer **108** via a bonding material **123**. The other end of the conductive pattern layer **108** is bonded to the top surface of the semiconductor element **120** via a bonding material **122**. The semiconductor element **120** and the respective conductive pattern layers **107** and **108** are covered with a sealing resin **130**.

The semiconductor element **120** is connected to a control terminal **103** via a bonding wire **106**. The control terminal **103** extends parallel to the top surface of the first cooling device **101***a*, and projects to the outside of the sealing resin **130** between the first cooling device **101***a* and the second cooling device **101***b*. The control terminal **103** is bent into an L-shape outside the sealing resin **130**, and extends in the normal direction of the top surface of the first cooling device **101***a* so as to be connected to a control substrate **102** arranged above the second cooling device **101***b*. Since the semiconductor device according to the comparative example includes the control terminal **103** extending in parallel to the top surface of the first cooling device **101***a* and projecting to the outside between the first cooling device **101***a* and the second cooling device **101***b*, the possibility of design of the wire-leading position is reduced. This prevents a reduction in size and complicates the wiring design.

In contrast, the semiconductor device **1** according to the embodiment of the present invention includes the control terminals **57***a* to **57***e* and **58***a* to **58***e* which extend in the normal direction of the first main surface **11***a* of the first cooling device **10***a* (in the Z-axis direction), and penetrate from the third main surface **11***b* to the fourth main surface **12***b* in the terminal-penetrating regions **15***a* and **15***b* defined at the predetermined positions between the plurality of second flow channels **13***b*. The control terminals **57***a* to **57***e* and **58***a* to **58***e* are led out from the fourth main surface **12***b* of the second cooling device **10***b*. The possibility of design of the wire-leading position of the respective control terminals **57***a* to **57***e* and **58***a* to **58***e* thus can be expanded. Accordingly, a reduction in size of the semiconductor device **1** according to the embodiment of the present invention can be achieved to facilitate the wiring design of the semiconductor device **1** and the power converting device including the semiconductor device **1**.

(Method of Fabricating Semiconductor Device)

A method of fabricating the semiconductor device (the semiconductor module) **1** according to the embodiment of the present invention is illustrated below with reference to FIG. **1** and FIG. **9** to FIG. **11**.

First, first conductive pattern layers composing circuit patterns such as the first conductive pattern layers **41** and **42**, are formed on the first main surface **11***a* of the first cooling device **10***a* (refer to FIG. **2**, for example). Also, second conductive pattern layers composing circuit patterns such as the second conductive pattern layers **45***c* and **46**, are formed on the third main surface **11***b* of the second cooling device **10***b* (refer to FIG. **4**, for example).

Next, the first semiconductor element **20** and the second semiconductor element **70** are mounted on the first conductive pattern layers of the first cooling device **10***a* so that the bottom surfaces of the first semiconductor element **20** and the second semiconductor element **70** are bonded via bonding materials (refer to FIG. **2** and FIG. **4**, for example). Further, the first main terminal **51**, the second main terminal **52**, and the third main terminal **53** are bonded to the top surfaces of the first conductive pattern layers (refer to FIG. **2** and FIG. **4**, for example). The conductive pattern layers composing the respective circuit patterns may be designed as appropriate depending on the type of the elements or circuits.

Next, as illustrated in FIG. **9**, the first cooling device **10***a* and the second cooling device **10***b* are opposed and stacked to each other so that the first conductive pattern layers on the first main surface **11***a* of the first cooling device **10***a* and the second conductive pattern layers on the third main surface **11***b* of the second cooling device **10***b* correspond to each other. The second cooling device **10***b* is provided with penetration holes **16***a*, **16***b*, **16***c*, **16***d*, and **16***e* to which the control terminals **57***a* to **57***e* are inserted, and penetration holes **17***a*, **17***b* **17***c*, **17***d*, and **17***e* to which the control terminals **58***a* to **58***e* are inserted. The both main surfaces (the chip surfaces) of the respective first semiconductor element **20** and second semiconductor element **70** are interposed between the first main surface **11***a* of the first cooling device **10***a* and the third main surface **11***b* of the second cooling device **10***b*.

Next, as illustrated in FIG. **10**, the first semiconductor element **20** and the second semiconductor element **70** are bonded to the first conductive pattern layers on the first main surface **11***a* of the first cooling device **10***a* and the second conductive pattern layers on the third main surface **11***b* of the second cooling device **10***b*. The first main terminal **51**, the second main terminal **52**, and the third main terminal **53** are arranged to project to the outside from both ends of the first cooling device **10***a* and the second cooling device **10***b* in the aligned direction of the first flow channels **13***a* and the second flow channels **13***b* (in the Y-axis direction). The control terminals **57***a* to **57***e* are inserted to the penetration holes **16***a* to **16***e* to be bonded to the second conductive pattern layers on the third main surface **11***b* of the second cooling device **10***b*, and the control terminals **58***a* to **58***e* are inserted to the penetration holes **17***a* to **17***e* to be bonded to the first conductive pattern layers on the first main surface **11***a* of the first cooling device **10***a*.

Thereafter, the first cooling device **10***a*, the second cooling device **10***b*, the first semiconductor element **20**, and the second semiconductor element **70** are bonded together and placed inside a metal mold. The sealing member **30** before being solidified is injected to the metal mold and then solidified. Accordingly, the sealing member **30** covering the first cooling device **10***a* and the second cooling device **10***b*, excluding both ends of the respective first flow channels **13***a* and second flow channels **13***b*, is provided, as illustrated in FIG. **1**. The respective end portions of the first flow channels **13***a*, the second flow channels **13***b*, the first main terminal **51**, the second main terminal **52**, and the third main terminal **53** project to be exposed to the outside from the surface of the sealing member **30**.

The semiconductor device **1** thus fabricated is connected with manifolds **91** and **92** at both ends of the first flow channels **13***a* and the second flow channels **13***b* of the first cooling device **10***a* and the second cooling device **10***b* (refer to FIG. **1**) during the use, as illustrated in FIG. **11**. The openings at both ends of the respective first flow channels **13***a* and second flow channels **13***b* (refer to FIG. **1**) are connected to an external circulation system via the respective manifolds **91** and **92**, so that a fluid serving as a coolant flows in the respective first flow channels **13***a* and second flow channels **13***b* in the same direction.

First Modified Example

As illustrated in FIG. **12**, a semiconductor device **1** according to a first modified example of the embodiment of the present invention differs from the semiconductor device **1** according to the embodiment of the present invention, in that the control terminals **57***a* to **57***e* are arranged in two lines in the first semiconductor element **20** illustrated in FIG.

2, and the control terminals **58***a* to **58***e* are arranged in two lines in the second semiconductor element **70** illustrated in FIG. **4**.

The control terminals **57***a* to **57***e* are arranged to penetrate the terminal-penetrating region **15***a* of the second cooling device **10***b*. The respective sets of the control terminals **57***a*, **57***c*, and **57***e* and the control terminals **57***b* and **57***d* aligned in the X-axis direction, are shifted from each other in the Y-axis direction. The control terminals **58***a* to **58***e* are arranged to penetrate the terminal-penetrating region **15***b* of the second cooling device **10***b*. The respective sets of the control terminals **58***a*, **58***c*, and **58***e* and the control terminals **58***b* and **58***d* aligned in the X-axis direction, are shifted from each other in the Y-axis direction. The semiconductor device **1** according to this example thus includes the four sets of the control terminals **57***a*, **57***c*, and **57***e*, the control terminals **57***b* and **57***d*, the control terminals **58***a*, **58***c*, and **58***e*, and the control terminals **58***b* and **58***d*, which are arranged in four lines in the X-axis direction.

The semiconductor device **1** according to the first modified example of the embodiment of the present invention includes the control terminals **57***a* to **57***e* and **58***a* to **58***e* of which the positions can be adjusted, so that the size and the positions of the terminal-penetrating regions **15***a* and **15***b* can also be adjusted depending on the positions of the control terminals **57***a* to **57***e* and **58***a* to **58***e*.

Second Modified Example

As illustrated in FIG. **13**, a semiconductor device **1** according to a second modified example of the embodiment of the present invention differs from the semiconductor device **1** according to the embodiment of the present invention illustrated in FIG. **2**, in that the first buffer film **61** and the second buffer film **62** illustrated in FIG. **2** are excluded. The semiconductor device **1** may include only one of the first buffer film **61** and the second buffer film **62** illustrated in FIG. **2**. The semiconductor device **1** according to the second modified example of the embodiment of the present invention thus has a reduced thickness due to the exclusion of the first buffer film **61** and the second buffer film **62**.

Third Modified Example

As illustrated in FIG. **14**, a semiconductor device **1** according to a third modified example of the embodiment of the embodiment of the present invention differs from the semiconductor device **1** according to the second modified example of the embodiment of the present invention illustrated in FIG. **13**, in that the second main surface **12***a* of the first cooling device **10***a* and the fourth main surface **12***b* of the second cooling device **10***b* are not covered with the sealing member **30**. The sealing member **30** covers the continuous region on the surface of the first cooling device **10***a* including the first main surface **11***a* and at least a part of the respective side surfaces **14***a*, in the cross-sectional view perpendicular to the longitudinal direction of the first flow channels **13***a* and the second flow channels **13***b*. The sealing member **30** also covers the continuous region on the surface of the second cooling device **10***b* including the third main surface **11***b* and at least a part of the respective side surfaces **14***b*, in the cross-sectional view perpendicular to the longitudinal direction of the first flow channels **13***a* and the second flow channels **13***b*.

Fourth Modified Example

As illustrated in FIG. **15**, a semiconductor device **1** according to a fourth modified example of the embodiment of the present invention differs from the semiconductor device **1** according to the embodiment of the present invention illustrated in FIG. **2**, in that the sealing member **30** has a first opening **31** at which the first buffer film **61** is exposed and a second opening **32** at which the second buffer film **62** is exposed. The exposed surfaces of the first buffer film **61** and the second buffer film **62** can be bonded to other circuit components or elements required to be cooled. Since the other components radiating heat are bonded to the first buffer film **61** and the second buffer film **62**, which are bonded directly to the first cooling device **10***a* and the second cooling device **10***b* through which the fluid serving as a coolant flows, the cooling performance of the entire system can be enhanced.

Fifth Modified Example

As illustrated in FIG. **16**, a semiconductor device **1** according to a fifth modified example of the embodiment of the present invention differs from the semiconductor device **1** according to the fourth modified example of the embodiment of the present invention illustrated in FIG. **15**, in that the first buffer film **61** has a first opening **63** at which a part of the second main surface **12***a* of the first cooling device **10***a* is exposed, and in that the second buffer film **62** has a second opening **64** at which a part of the fourth main surface **12***b* of the second cooling device **10***b* is exposed. The exposed second main surface **12***a* at the first opening **63** and the exposed fourth main surface **12***b* at the second opening **64** can be bonded directly to other circuit components or elements required to be cooled. Accordingly, the cooling performance of the entire system can be enhanced.

Sixth Modified Example

As illustrated in FIG. **17**, a semiconductor device **1** according to a sixth modified example of the embodiment of the present invention differs from the semiconductor device **1** according to the embodiment of the present invention illustrated in FIG. **1**, in that the respective sets of the control terminal **57***a* to **57***e* and the control terminals **58***a* to **58***e* are located at the same position in the Y-axis direction and aligned in line in the X-axis direction. Further, the semiconductor device **1** of this example differs from the semiconductor device **1** illustrated in FIG. **1** in that the third main terminal **53** projects from the sealing member **30** on the same side as the second main terminal **52**.

FIG. **18** is a perspective view of the semiconductor device **1**, omitting the first cooling device **10***a*, the second cooling device **10***b*, and the sealing member **30** illustrated in FIG. **17**. As illustrated in FIG. **18**, the control terminals **57***a* to **57***e* are bonded to the second conductive pattern layers **45***a* to **45***e*, and the control terminals **58***a* to **58***e* are bonded to the first conductive pattern layers **82***a* to **82***e*.

FIG. **19** is a cross-sectional view as viewed from direction A-A in FIG. **17**. The second cooling device **10***b* illustrated in FIG. **19** differs from the second cooling device **10***b* illustrated in FIG. **2** in including a single terminal-penetrating region **15***a*. The other structure of the second cooling device **10***b* of this example is the same as the second cooling device **10***b* illustrated in FIG. **2**. The control terminals **57***a* to **57***e* and **58***a* to **58***e* illustrated in FIG. **17** and FIG. **18** penetrate the terminal-penetrating region **15***a* illustrated in FIG. **19**.

FIG. **20** is a cross-sectional view as viewed from direction B-B in FIG. **17**. The second semiconductor element **70** illustrated in FIG. **20** differs from the second semiconductor element **70** illustrated in FIG. **4** in having a topology inverted in the right-left direction. The other structure of the second semiconductor element **70** of this example is the same as the second semiconductor element **70** illustrated in FIG. **4**.

The semiconductor device **1** according to the sixth modified example of the embodiment of the present invention includes the control terminals **57***a* to **57***e* and **58***a* to **58***e* arranged to be aligned in line in the X-axis direction. The arrangement of the control terminals **57***a* to **57***e* and **58***a* to **58***e* aligned in line in the X-axis direction can decrease the region occupied by the terminal-penetrating region **15***a*, as compared with the case in which the control terminals **57***a* to **57***e* and **58***a* to **58***e* are arranged in two lines, so as to increase the number of the second flow channels **13***b* of the second cooling device **10***b*.

Seventh Modified Example

A semiconductor device **1** according to a seventh modified example of the embodiment of the present invention, as illustrated in the cross-sectional view of FIG. **21** omitting the first cooling device **10***a*, the second cooling device **10***b*, and the sealing member **30**, includes the first semiconductor element **20** which has substantially the same structure as that in the semiconductor device **1** according to the embodiment of the present invention illustrated in FIG. **5**, for example. The second semiconductor element **70** of this example differs from that in the semiconductor device **1** according to the embodiment of the present invention illustrated in FIG. **5** in having a topology inverted in the vertical direction. The control terminals **58***a* to **58***e* are bonded to second conductive pattern layers **88***a*, **88***b*, **88***c*, **88***d*, and **88***e*.

FIG. **22** is a cross-sectional view of the semiconductor device **1** according to the seventh modified example of the embodiment of the present invention, corresponding to the cross-sectional view as viewed from direction B-B in FIG. **1**. A semiconductor element composing the second semiconductor element **70** includes the second main electrode **70**C on the bottom surface side, and the first main electrode **70**E and the control electrode **70**G on the top surface side. The second main electrode **70**C located on the bottom surface of the second semiconductor element **70** is bonded to a first conductive pattern layer **84** via the bonding material **71**. The first conductive pattern layer **84** is connected to the second conductive pattern layer **46** illustrated in FIG. **21**. The first main electrode **70**E located on the top surface of the second semiconductor element **70** illustrated in FIG. **22** is bonded to one end of a second conductive pattern layer **87** via the bonding material **73**. The other end of the second conductive pattern layer **87** is bonded to the third main terminal **53** via the bonding material **72**.

The control electrode **20**G located on the top surface of the first semiconductor element **20** is bonded to one end of the second conductive pattern layer **88***c* via the bonding material **74**. The other end of the second conductive pattern layer **88***c* is bonded to the control terminal **58***c*. The control terminal **58***c* extends in the normal direction of the first main surface **11***a* (in the Z-axis direction), and penetrates from the third main surface **11***b* to the fourth main surface **12***b* in the second cooling device **10***b* within the terminal-penetrating region **15***b* in which the second flow channels **13***b* of the second cooling device **10***b* are not provided. The control terminal **58***c* projects to the outside of the sealing member **30** above the fourth main surface **12***b* of the second cooling device **10***b* so as to be connected to the control substrate **2**.

The semiconductor device **1** according to the seventh modified example of the embodiment of the present invention including the second semiconductor element **70** having the vertically-inverted topology, can also allow the control terminals **58***a* to **58***e* to penetrate the second cooling device **10***b* so as to be led out from the fourth main surface **12***b*.

Eighth Modified Example

A semiconductor device **1** according to an eighth modified example of the embodiment of the present invention, as illustrated in the cross-sectional view of FIG. **23** and FIG. **24** omitting the first cooling device **10***a*, the second cooling device **10***b*, and the sealing member **30**, includes the second semiconductor element **70** which has substantially the same structure as that in the semiconductor device **1** according to the embodiment of the present invention illustrated in FIG. **5**, for example. The first semiconductor element **20** of this example differs from that in the semiconductor device **1** according to the embodiment of the present invention in having a topology inverted in the vertical direction. FIG. **24** is an inverted perspective view of FIG. **23** vertically inverted about a rotation axis in the X-axis direction.

The control terminals **57***a* to **57***e* and **58***a* to **58***e* are located at the same position in the Y-axis direction and aligned in line in the X-axis direction. The control terminals **57***a* to **57***e* are bonded to first conductive pattern layers **44***a*, **44***b*, **44***c*, **44***d*, and **44***e*, and the control terminals **58***a* to **58***e* are bonded to the first conductive pattern layers **82***a* to **82***e*.

FIG. **25** is a cross-sectional view of the semiconductor device **1** according to the eighth modified example of the embodiment of the present invention, corresponding to the cross-sectional view as viewed from direction A-A in FIG. **1**. A semiconductor element composing the first semiconductor element **20** includes the first main electrode **20**E and the control electrode **20**G on the bottom surface side, and the second main electrode **20**C on the top surface side. The second main electrode **20**C located on the top surface of the first semiconductor element **20** is bonded to one end of a second conductive pattern layer **47** via the bonding material **24**. The other end of the second conductive pattern layer **47** is bonded to the first main terminal **51** via the bonding material **23**. The first main electrode **20**E located on the bottom surface of the first semiconductor element **20** is bonded to a first conductive pattern layer **43** via the bonding material **21**. The first conductive pattern layer **43** is connected to the second conductive pattern layer **85** and the second main terminal **52** illustrated in FIG. **23** and FIG. **24**. The control electrode **20**G located on the bottom surface of the first semiconductor element **20** is bonded to one end of the first conductive pattern layer **44***c* via the bonding material **22**.

The other end of the first conductive pattern layer **44***c* is provided with a recess **44***x*. A penetration hole penetrating the first conductive pattern layer **44***c* may be provided instead of the recess **44***x*. The control terminal **57***c* is inserted to the recess **44***x* of the first conductive pattern layer **44***c*. The control terminal **57***c* is bonded to the first conductive pattern layer **44***c* by pressure welding or with a bonding material, for example.

The control terminal **57***c* extends in the normal direction of the first main surface **11***a* (in the Z-axis direction), and penetrates from the third main surface **11***b* to the fourth main surface **12***b* in the second cooling device **10***b* within the terminal-penetrating region **15***b* in which the second flow channels **13***b* of the second cooling device **10***b* are not provided. The control terminal **57***c* projects to the outside of the sealing member **30** above the fourth main surface **12***b* of the second cooling device **10***b* so as to be connected to the control substrate **2**.

The semiconductor device **1** according to the eighth modified example of the embodiment of the present invention including the first semiconductor element **20** having the vertically-inverted topology, can also allow the control terminals **57***a* to **57***e* to penetrate the second cooling device **10***b* so as to be led out from the fourth main surface **12***b*.

Other Embodiments

As described above, the invention has been described according to the embodiments, but it should not be understood that the description and drawings implementing a portion of this disclosure limit the invention. Various alternative embodiments of the present invention, examples, and operational techniques will be apparent to those skilled in the art from this disclosure.

The embodiment of the present invention has been illustrated above with the 2-in-1 power semiconductor module in which the two semiconductor chips of the first semiconductor element **20** and the second semiconductor element **70** are mounted, but is not limited to this illustration. For example, a single semiconductor chip may be mounted in the semiconductor module, or three or more semiconductor chips may be mounted in the semiconductor module. While the embodiment of the present invention has been illustrated above with the case of including the ten control terminals **57***a* to **57***e* and **58***a* to **58***e*, the number of the control terminals may be determined as appropriate. The number of the control terminals used in each of the first semiconductor element **20** and the second semiconductor element **70** may differ from each other.

As described above, the invention includes various embodiments of the present invention and the like not described herein. Therefore, the scope of the present invention is defined only by the technical features specifying the present invention, which are prescribed by claims, the words and terms in the claims shall be reasonably construed from the subject matters recited in the present Specification.

What is claimed is:

1. A semiconductor device comprising:

a first cooling device including a plurality of first flow channels through which a fluid is to flow, between a first main surface and a second main surface opposed to each other;

a second cooling device including a plurality of second flow channels through which a fluid is to flow, between a third main surface and a fourth main surface parallel to the first main surface;

a semiconductor element interposed between the first main surface and the third main surface facing each other; and

a control terminal penetrating from the third main surface to the fourth main surface in a terminal-penetrating region provided at a position between adjacent second flow channels among the plurality of second flow channels, and electrically connected to a control electrode of the semiconductor element.

2. The semiconductor device of claim **1**, further comprising:

a plurality of first conductive patterned layers bonded to the first main surface; and

a plurality of second conductive patterned layers bonded to the third main surface,

wherein

the semiconductor element has a first main surface and a second main surface,

the first main surface of the semiconductor element is opposed to the first main surface of the first cooling device via at least a part of the first conductive pattern layers, and

the second main surface of the semiconductor element is opposed to the third main surface of the second cooling device via at least a part of the second conductive pattern layers.

3. The semiconductor device of claim **1**, wherein:

the plurality of second flow channels extend in a first direction parallel to the first main surface, and are aligned in a second direction perpendicular to the first direction; and

the terminal-penetrating region extends in the first direction.

4. The semiconductor device of claim **3**, wherein:

the semiconductor element includes a first main electrode on the main surface on which the control electrode is located;

the second flow channels are located at least at a position overlapping with the first main electrode in the second direction; and

the terminal-penetrating region is located on an outer side of the position overlapping with the first main electrode in the second direction.

5. The semiconductor device of claim **4**, further comprising a first main terminal connected to the first main electrode and extending in parallel to the first main surface.

6. The semiconductor device of claim **1**, wherein the control terminal comprises a plurality of control terminals, arranged in a line or two lines, in a first direction parallel to the first main surface.

7. The semiconductor device of claim **1**, wherein the control terminal comprises a plurality of control terminals, connected to the semiconductor element and arranged in a line or two lines, in a first direction parallel to the first main surface.

8. The semiconductor device of claim **2**, wherein the control terminal is electrically connected to the control electrode via at least a part of the first conductive pattern layers.

9. The semiconductor device of claim **2**, wherein the control terminal is electrically connected to the control electrode via at least a part of the second conductive pattern layers.

10. A cooling module comprising:

a first cooling device including a plurality of first flow channels through which a fluid is to flow, between a first main surface and a second main surface opposed to each other; and

a second cooling device including a plurality of second flow channels through which a fluid is to flow, between a third main surface and a fourth main surface parallel to the first main surface,

wherein a terminal-penetrating region is defined in the second cooling device through which a control terminal, which is electrically connected to a control electrode of a semiconductor element interposed between the first main surface and the third main surface facing each other, penetrates from the third main surface to the fourth main surface at a position between adjacent second flow channels among the plurality of second flow channels.

11. A power converting device comprising:

a first cooling device including a plurality of first flow channels through which a fluid is to flow, between a first main surface and a second main surface opposed to each other;

a second cooling device including a plurality of second flow channels through which a fluid is to flow, between a third main surface and a fourth main surface parallel to the first main surface;

a semiconductor element interposed between the first main surface and the third main surface facing each other;

a control terminal penetrating from the third main surface to the fourth main surface in a terminal-penetrating region provided at a position between adjacent second flow channels among the plurality of second flow channels, and electrically connected to a control electrode of the semiconductor element;

a control substrate on which a circuit electrically connected to the control terminal is mounted; and

a capacitor arranged toward the second main surface of the first cooling device.

12. An electric vehicle comprising:

a first cooling device including a plurality of first flow channels through which a fluid is to flow, between a first main surface and a second main surface opposed to each other;

a second cooling device including a plurality of second flow channels through which a fluid is to flow, between a third main surface and a fourth main surface parallel to the first main surface;

a semiconductor element interposed between the first main surface and the third main surface facing each other;

a control terminal penetrating from the third main surface to the fourth main surface in a terminal-penetrating region provided at a position between adjacent second flow channels among the plurality of second flow channels, and electrically connected to a control electrode of the semiconductor element;

a control substrate on which a circuit electrically connected to the control terminal is mounted;

a capacitor arranged toward the second main surface of the first cooling device;

a power source for supplying electricity to the semiconductor element; and

a load driven by the semiconductor element.

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