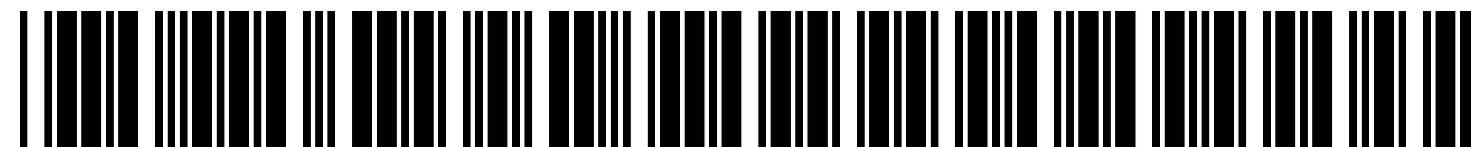

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Doyle et al.

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(45) **Date of Patent: Oct. 6, 2020**

(54) **IMPLEMENTING BACKDRILLING ELIMINATION UTILIZING ANTI-ELECTROPLATE COATING**

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H05K 1/11	(2006.01)

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CPC ***H05K 3/425*** (2013.01); ***H05K 1/034*** (2013.01); ***H05K 1/115*** (2013.01); ***H05K 3/423*** (2013.01);

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(Continued)

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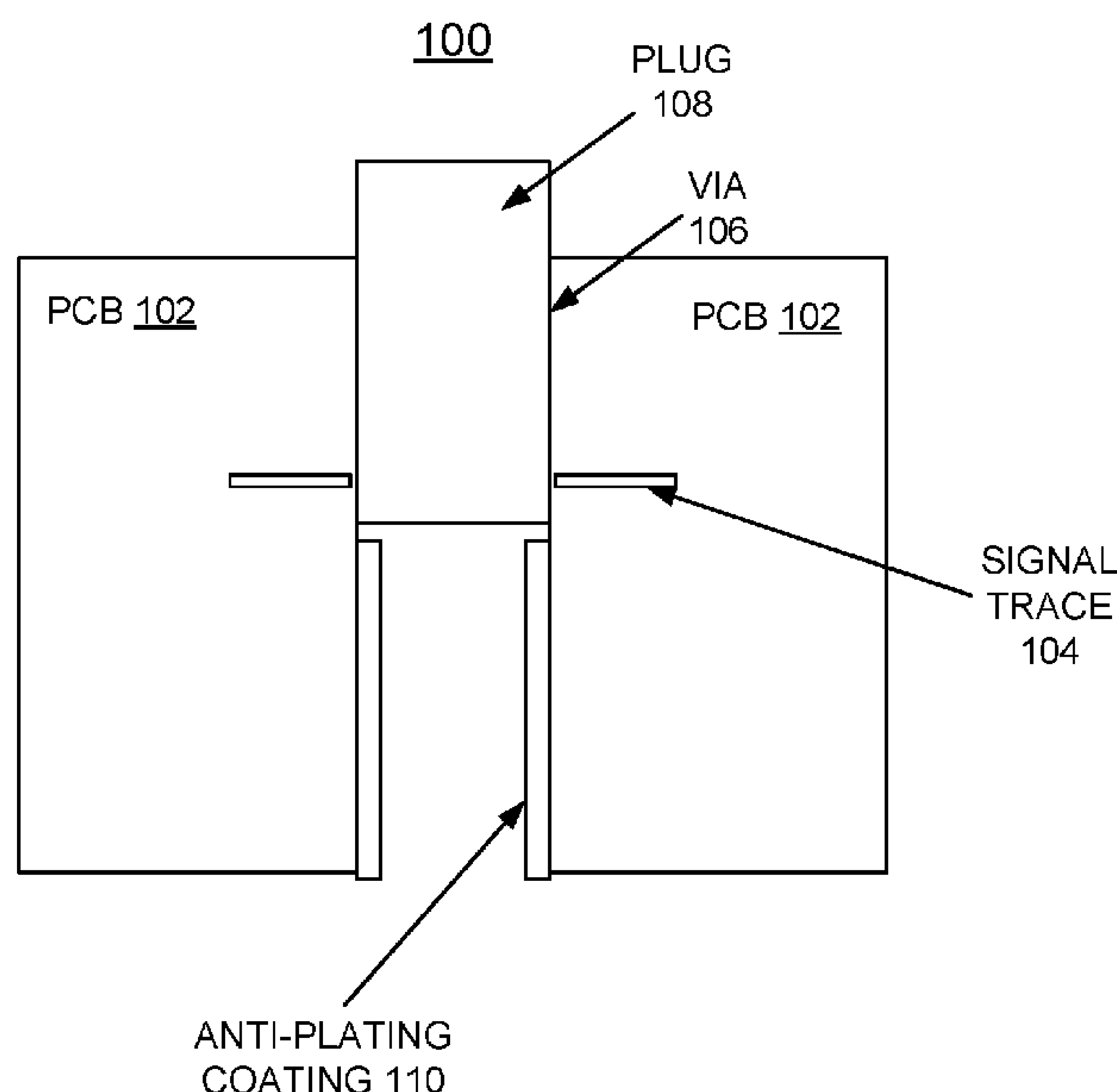
(57) **ABSTRACT**

A method and structure are provided for implementing enhanced via creation without creating a via barrel stub. The need to backdrill vias during printed circuit board (PCB) manufacturing is eliminated. After the vias have been drilled, but before plating, a plug is inserted into each via and the plug is lowered to a depth just below a desired signal trace layer. A thin anti-electroplate coating is applied onto the walls of the via below the signal trace. Then the plugs are removed and a standard board plating process for the PCB is performed.

5 Claims, 3 Drawing Sheets



(51) **Int. Cl.**
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H05K 3/40 (2006.01)
H05K 3/42 (2006.01)
H01L 21/311 (2006.01)
H01L 23/48 (2006.01)
H05K 1/03 (2006.01)

(52) **U.S. Cl.**
CPC . *H05K 2201/015* (2013.01); *H05K 2203/143* (2013.01)

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CPC .. H05K 3/42; H05K 3/46; H05K 1/34; H05K 1/36; H05K 1/115; H05K 1/257; H05K 3/40; H05K 3/308; H05K 3/423; H05K 3/425; H05K 3/429; H01L 21/311; H01L 23/48
USPC 174/258, 255, 260, 264, 266, 257, 262; 29/745, 852, 846; 438/700; 428/137, 428/209
See application file for complete search history.

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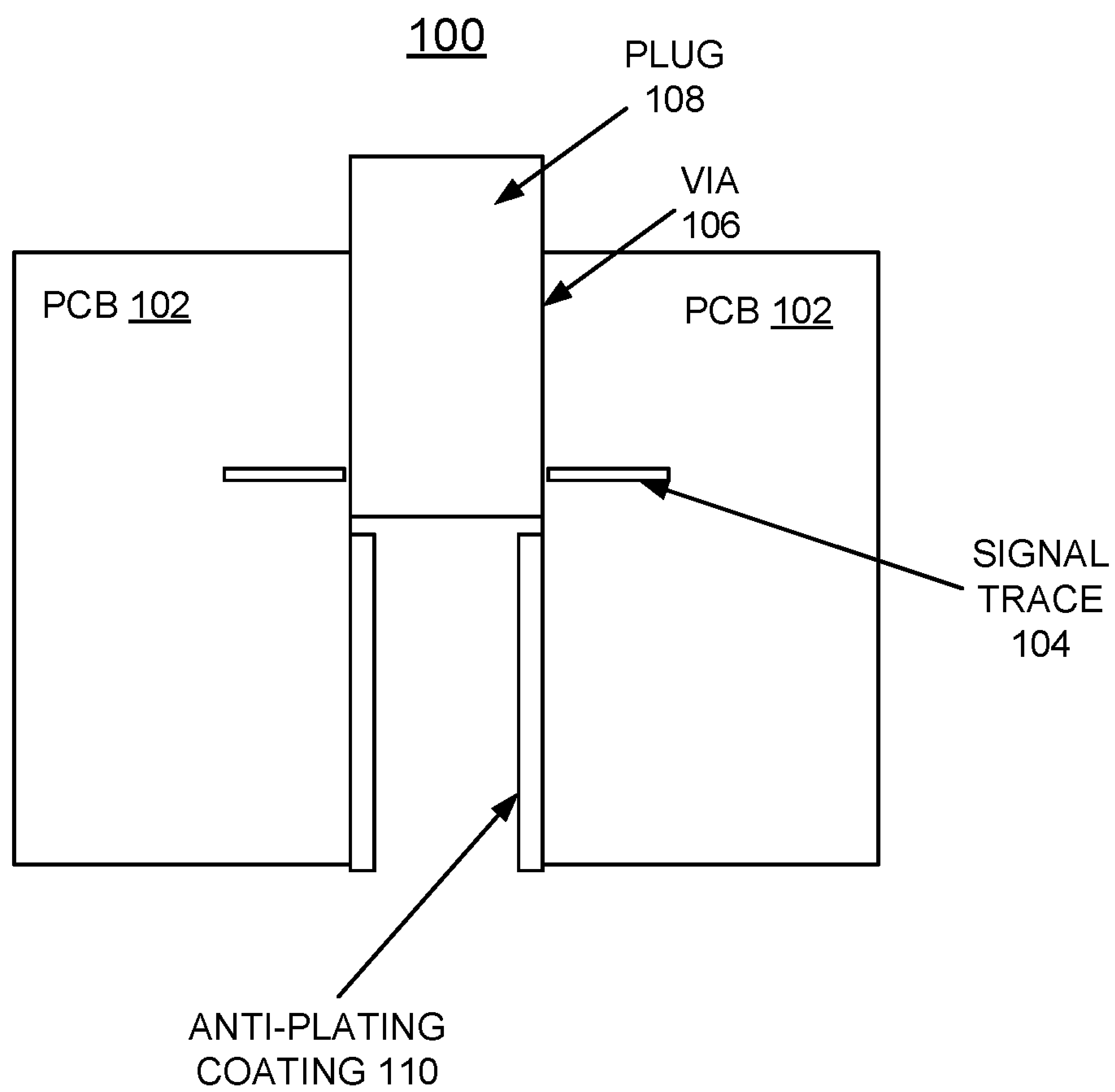

FIG. 1

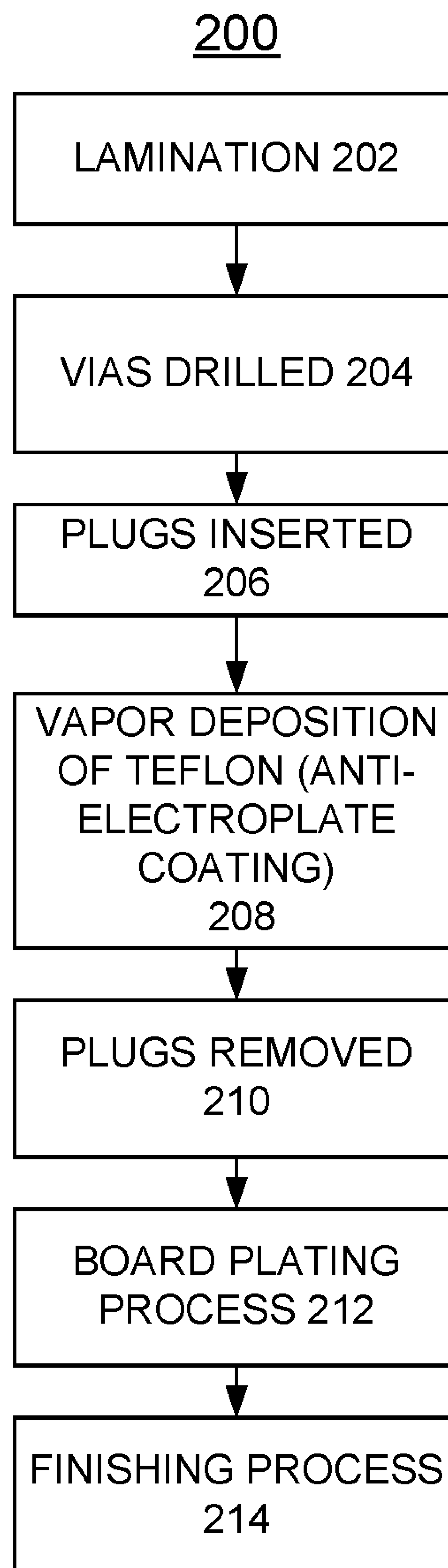

FIG. 2

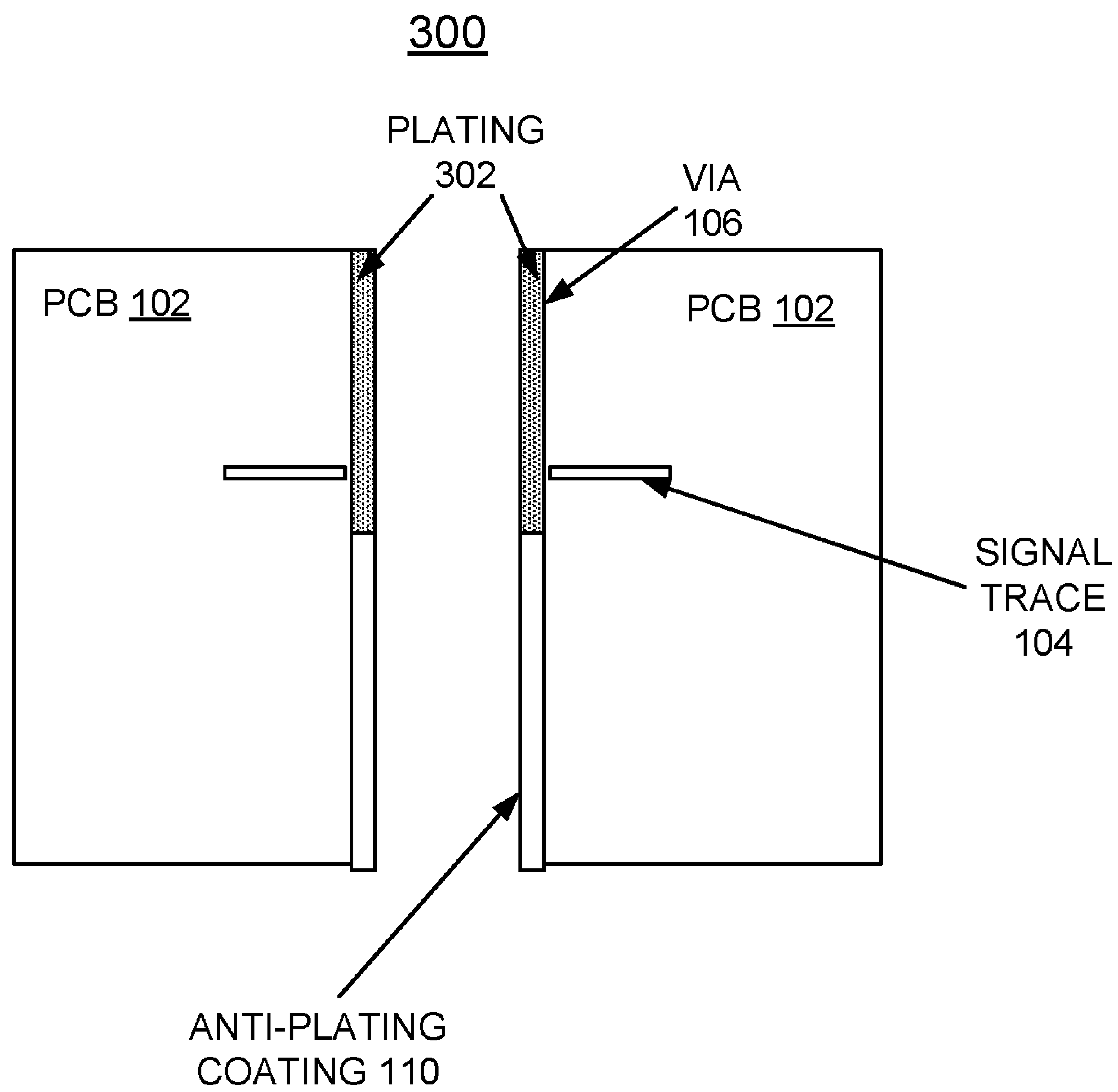

FIG. 3

IMPLEMENTING BACKDRILLING ELIMINATION UTILIZING ANTI-ELECTROPLATE COATING

This application is a continuation application of Ser. No. 15/217,019 filed Jul. 22, 2016.

FIELD OF THE INVENTION

The present invention relates generally to the data processing field, and more particularly, relates to a method and structure for implementing manufacture of a printed circuit board (PCB) with enhanced via creation without creating a via barrel stub, eliminating the need to back-drill.

DESCRIPTION OF THE RELATED ART

The computer hardware development industry has reached a point wherein many computer interfaces are of sufficient switching speed as to require signal routing layer change vias to be back-drilled to remove via barrel stubs. Backdrilling is a conventional technique used to remove the via barrel stub. Without removal of the unnecessary section or length of a via barrel, some amount of the propagating signal is reflected away from the intended receiver, thereby significantly reducing the amount of total energy effectively transferred from driver to receiver.

While there are known processes to mechanically remove these stubs, once back-drilled, it is no longer possible to probe those locations on the printed circuit board (PCB), cost of the PCB increases substantially, and success of the process is statistically less than ideal. These facts significantly complicate our ability to manufacture cost-effective PCBs, measure high-speed interfaces in the lab during system bring-up and model-to-hardware correlation activities, and maximize the electrical performance of our computer interfaces. When system errors occur in the field, the field engineer cannot measure and confirm function at these PCB via locations while at the customer's site.

A need exists for a method and structure for implementing via creation that eliminates creation of a via barrel stub, eliminating the need to back-drill, reducing PCB cost, and maximizing interface margin.

As used in the following description and claims, the term printed circuit board (PCB) should be understood to broadly include a printed wiring board or other substrate, an interconnect substrate, and various substrates including a plurality of insulator layers, and internal conductive traces.

SUMMARY OF THE INVENTION

Principal aspects of the present invention are to provide a method and structure for implementing manufacture of a printed circuit board (PCB) with enhanced via creation without creating a via barrel stub, eliminating the need to back-drill. Other important aspects of the present invention are to provide such method and structure substantially without negative effects and that overcome many of the disadvantages of prior art arrangements.

In brief, a method and structure are provided for implementing enhanced via creation without creating a via barrel stub. The need to backdrill during printed circuit board (PCB) manufacturing is eliminated. After the vias have been drilled, but before plating, a plug is inserted into each via and the plug is lowered to a depth just below a desired signal trace layer. A thin anti-electroplate coating is applied onto the walls of the via below the signal trace. Then the plugs are removed and a board plating process for the PCB is performed.

In accordance with features of the invention, the anti-electroplate coating includes, for example, a Teflon coating or a polytetrafluoroethylene (PTFE) coating, Teflon is a trade name for PTFE.

In accordance with features of the invention, the Teflon coating is applied, for example, using vapor deposition onto the walls of the via below the signal trace.

In accordance with features of the invention, the coating prevents the plating from creating via barrel stubs, thus eliminating the need to backdrill each via after the plating process.

In accordance with features of the invention, eliminating back-drilling improves yield and late fail discoveries, both of which can improve cost and reliability of boards.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention together with the above and other objects and advantages may best be understood from the following detailed description of the preferred embodiments of the invention illustrated in the drawings, wherein:

FIG. **1** illustrates an example structure for manufacturing a printed circuit board (PCB) with enhanced via creation without creating a via barrel stub, eliminating the need to back-drill in accordance with the preferred embodiment;

FIG. **2** is a flow chart illustrating example steps for implementing a structure embodying the enhanced via creation without creating a via barrel stub in accordance with the preferred embodiment; and

FIG. **3** illustrates an example structure for manufacturing a printed circuit board (PCB) with enhanced via creation without creating a via barrel stub, eliminating the need to back-drill in accordance with the preferred embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following detailed description of embodiments of the invention, reference is made to the accompanying drawings, which illustrate example embodiments by which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the invention.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

In accordance with features of the invention, a method and structure are provided for implementing enhanced via creation without creating a via barrel stub. The need to backdrill vias during printed circuit board (PCB) manufacturing is eliminated. After the vias have been drilled, but before plating, a plug is inserted into each via and the plug is lowered to a depth just below a desired signal trace layer. A thin anti-electroplate coating is applied onto the walls of

the via below the plug and the signal trace. Then the plugs are removed and a board plating process for the PCB is performed.

Having reference now to the drawings, in FIG. **1**, there is shown an example structure generally designated by reference character **100** for manufacturing a printed circuit board (PCB) with enhanced via creation without creating a via barrel stub, eliminating the need to back-drill in accordance with the preferred embodiment.

Structure **100** includes a printed circuit board (PCB) **102** having an internal conductive or signal trace **104**. PCB **102** includes an insulator substrate or insulator layers, with one or more internal conductive traces **104**. Structure **100** includes a via **106** extending through the printed circuit board (PCB) **102** and the internal conductive trace **104**. Structure **100** includes an anti-electroplate coating **110** covering the walls of the via **106** below the signal trace **104**. The anti-electroplate coating **110** eliminates via barrel stub creation during a PCB plating process during PCB manufacturing. The anti-electroplate coating **110** is a chemically resistant polymer and is hydrophobic. The anti-electroplate coating **110** has a selected thickness, for example, in a range between 0.2 μm and 0.5 μm.

The anti-electroplate coating **110** includes, for example, a polytetrafluoroethylene (PTFE) coating (e.g., trade name Teflon), that is applied for example, using vapor deposition onto the walls of the via **106** below the signal trace **104**.

"PTFE Deposition: View" by MNX MEMS & Nanotechnology Exchange, detailing example vapor deposition of Teflon, is provided at: https://www.mems-exchange.org/catalog/P3372/

The PTFE coating **110** prevents the PCB plating process from creating via barrel stubs, thus eliminating the need to backdrill each via after the plating process. Eliminating back-drilling improves yield and late fail discoveries, both of which can improve cost and reliability of boards.

In accordance with features of the invention, the printed circuit board (PCB) **102** and via **106** are formed generally including standard PCB manufacturing processes, including via drilling and plating. However, the step of back-drilling at the end is removed and the PCB process of the invention provides that after the vias **106** have been drilled, but before plating, a small plug **108** is inserted into each via **106** extending to a defined depth just below the desired signal trace layer **104**. A thin coating **110** of Teflon is then applied using vapor deposition onto the walls of the via **106** below the signal trace **104**, and then the plugs **108** are removed. The PCB **102** is then sent through the normal plating process. The coating **110** prevents the plating from taking hold, thus eliminating the need to backdrill each via after the plating process.

Referring now to FIG. **2**, there is shown a flow chart illustrating example steps generally designated by reference character **200** for implementing a structure embodying the enhanced via creation without creating a via barrel stub in accordance with the preferred embodiment starting at a block **202**.

As indicated at a block **202**, a lamination is formed defining the PCB **102** and at least one internal conductive traces **104**.

As indicated at a block **204**, vias **106** are drilled. Conventional via drilling is performed.

As indicated at a block **206**, the plugs **108** are inserted into the via **106**, with the plugs extending from a top or first surface to a depth below the signal trace **104**. The plugs **108** optionally are configured as sprayers (like fuel injectors) to apply the Teflon coating applied to the walls of the via **106** below plugs **108**. Optionally, individual plugs **108** having a specified length are pushed flush with one side of the PCB **102**, then moved or poked out from the other PCB side. Optionally, individual plugs **108** are mechanically inserted to a specific depth, the retracted. Optionally, an array of plugs **108**, typically of differing lengths extending from a plate are all inserted at once, the removed.

As indicated at a block **208**, the anti-electroplate coating **110** is applied to the walls of the via **106** below plugs **108** and the signal trace **104**, for example, by vapor deposition of Teflon.

As indicated at a block **210**, the plugs **108** are removed from the vias **106** after the anti-electroplate coating **110** is applied.

As indicated at a block **212**, the PCB plating process is performed, using a conventional plating process.

As indicated at a block **214**, conventional PCB finishing processes are performed, advantageously eliminating the need to backdrill each via after the plating process.

Referring now to FIG. **3**, there is shown an example resulting structure generally designated by reference character **300** resulting from manufacturing a printed circuit board (PCB) with enhanced via creation without creating a via barrel stub, eliminating the need to back-drill in accordance with the preferred embodiment. Structure **300** shows the plugs **108** removed from the vias **106** after the anti-electroplate coating **110** is applied.

Structure **300** includes the printed circuit board (PCB) **102** having the internal conductive or signal trace **104**. Structure **100** includes the via **106** extending through the printed circuit board (PCB) **102** and the internal conductive trace **104**. Structure **300** includes the anti-electroplate coating **110** covering the walls of the via **106** below the signal trace **104**. Structure **300** includes a plating **302** applied during the PCB plating process that is performed using a conventional plating process.

In accordance with features of the invention, the alternative method for via creation eliminates creation of the via barrel stub. Since the via barrel stub is not created, the need to back-drill is eliminated, reducing PCB cost and maximizing interface margin.

While the present invention has been described with reference to the details of the embodiments of the invention shown in the drawing, these details are not intended to limit the scope of the invention as claimed in the appended claims.

What is claimed is:

1. A structure for implementing enhanced via creation during printed circuit board (PCB) manufacturing comprising:

a printed circuit board (PCB);

said printed circuit board (PCB) having an internal conductive signal trace;

a single through hole defining a via formed by via drilling, said via having a single uniform diameter extending through the printed circuit board (PCB) and said via extending through the internal conductive signal trace;

an anti-electroplate coating covering the walls of said via spaced below the internal conductive signal trace; said anti-electroplate coating formed of a chemically resistant polymer;

said anti-electroplate coating chemically resistant polymer having a selected thickness of approximately 0.2 μm;

a via plating formed on walls of said via, said via plating extending above said anti-electroplate coating on walls of said via and extending on walls of said via through

and below the internal conductive signal trace; said via plating electrically connected to the internal conductive signal trace; and

said anti-electroplate coating preventing via plating from taking hold in the structure on the walls of said via spaced below the internal conductive signal trace, eliminating via barrel stub creation during PCB manufacturing;

wherein said anti-electroplate coating is applied below a plug in said via, said plug used during printed circuit board (PCB) manufacturing.

2. The structure as recited in claim **1**, wherein said anti-electroplate coating includes a hydrophobic polymer applied by vapor deposition.

3. The structure as recited in claim **1**, wherein said PCB manufacturing PCB includes forming said via coating applied by conventional plating processes being performed after forming said anti-electroplate coating.

4. The structure as recited in claim **1**, wherein said anti-electroplate coating includes a hydrophobic polymer applied by vapor deposition.

5. The structure of claim **1**, wherein said anti-electroplate coating includes a polytetrafluoroethylene (PTFE) coating applied by vapor deposition.

* * * * *