US010673338B2

(12) **United States Patent**
Lee et al.

(10) **Patent No.: US 10,673,338 B2**
(45) **Date of Patent: Jun. 2, 2020**

(54) **VOLTAGE CONVERTER AND OPERATING METHOD OF VOLTAGE CONVERTER**

(71) Applicant: **Samsung Electronics Co., Ltd.**, Suwon-si, Gyeonggi-do (KR)

(72) Inventors: **Kwang Chan Lee**, Hwaseong-si (KR); **Sungwoo Lee**, Suwon-si (KR); **Jungwook Heo**, Yongin-si (KR); **Hyoungseok Oh**, Seoul (KR); **Jiheon Kang**, Hwaseong-si (KR); **Hocheol Chung**, Suwon-si (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.**, Gyeonggi-do (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/519,398**

(22) Filed: **Jul. 23, 2019**

(65) **Prior Publication Data**

US 2019/0348917 A1 Nov. 14, 2019

Related U.S. Application Data

(63) Continuation-in-part of application No. 15/967,687, filed on May 1, 2018, now Pat. No. 10,361,620.

(30) **Foreign Application Priority Data**

Sep. 8, 2017 (KR) 10-2017-0115348

(51) **Int. Cl.**
H02M 3/158 (2006.01)
H02M 3/07 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H02M 3/1582*** (2013.01); ***G05F 1/56*** (2013.01); ***H02M 3/073*** (2013.01); *H02M 2001/0006* (2013.01)

(58) **Field of Classification Search**
CPC H02M 3/1582; H02M 3/073; H02M 3/155; H02M 1/088; H02M 2001/0006; G05F 1/56
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,392,364 B1 5/2002 Yamamoto et al.
6,812,782 B2 11/2004 Grant
(Continued)

FOREIGN PATENT DOCUMENTS

CN 1783679 A 6/2006
CN 202150796 U 2/2012
(Continued)

OTHER PUBLICATIONS

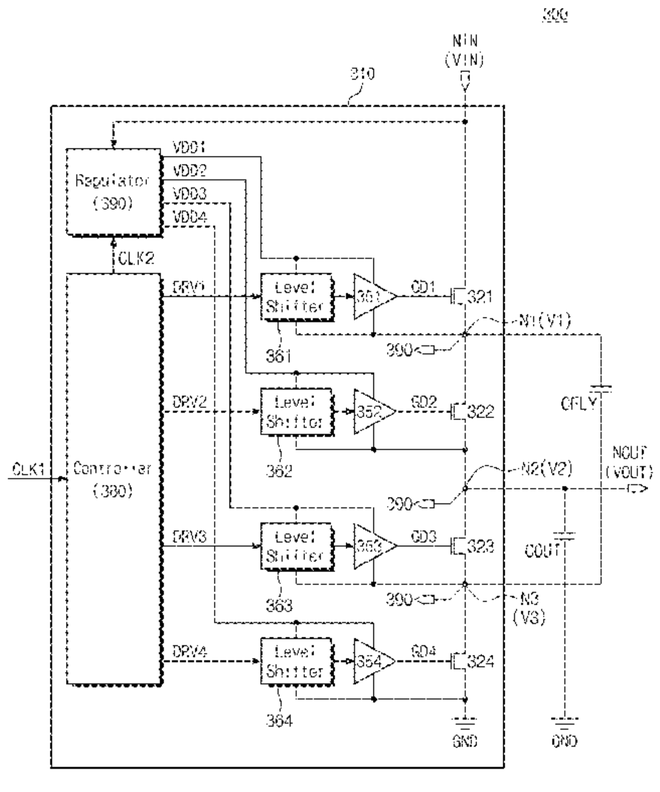
Chinese Office Action dated Apr. 2, 2020 issued in corresponding Chinese Patent Application No. 201810940847.6.

Primary Examiner — Jue Zhang
Assistant Examiner — Afework S Demisse
(74) *Attorney, Agent, or Firm* — Harness, Dickey & Pierce, P.L.C.

(57) **ABSTRACT**

A voltage converter includes a first transistor, a second transistor, a third transistor, a fourth transistor connected, an output capacitor, a flying capacitor, a first gate driver configured to output a first power supply voltage as a first high level and a first voltage as a first low level, a second gate driver configured to output a second power supply voltage as a second high level and a second voltage as a second low level, a third gate driver configured to output a third power supply voltage as a third high level and a third voltage as a third low level, a fourth gate driver configured to output a fourth power supply voltage as a fourth high level and a ground voltage as a fourth low level.

20 Claims, 22 Drawing Sheets



(51) **Int. Cl.**
G05F 1/56 (2006.01)
H02M 1/00 (2006.01)

(56) **References Cited**

U.S. PATENT DOCUMENTS

7,265,601	B2	9/2007	Ahmad	
7,518,352	B2	4/2009	De Lima Filho et al.	
7,656,690	B2	2/2010	Yamada et al.	
8,502,511	B1	8/2013	Kung	
8,779,733	B2	7/2014	Chen	
8,970,185	B1	3/2015	Sutardja et al.	
9,312,773	B2 *	4/2016	Li	H02M 3/1588
9,484,758	B2	11/2016	Chen et al.	
9,577,520	B2	2/2017	Xiu et al.	
9,590,608	B2	3/2017	Xu	
9,625,932	B2	4/2017	Qu et al.	
2013/0099846	A1	4/2013	Sohma	
2015/0042298	A1	2/2015	Kung et al.	
2015/0061611	A1	3/2015	Li	
2017/0117803	A1	4/2017	Matsuki et al.	
2017/0133929	A1	5/2017	Matsuki et al.	

FOREIGN PATENT DOCUMENTS

CN	102832810	A	12/2012
EP	1748683	A2	1/2007

* cited by examiner

FIG. 1

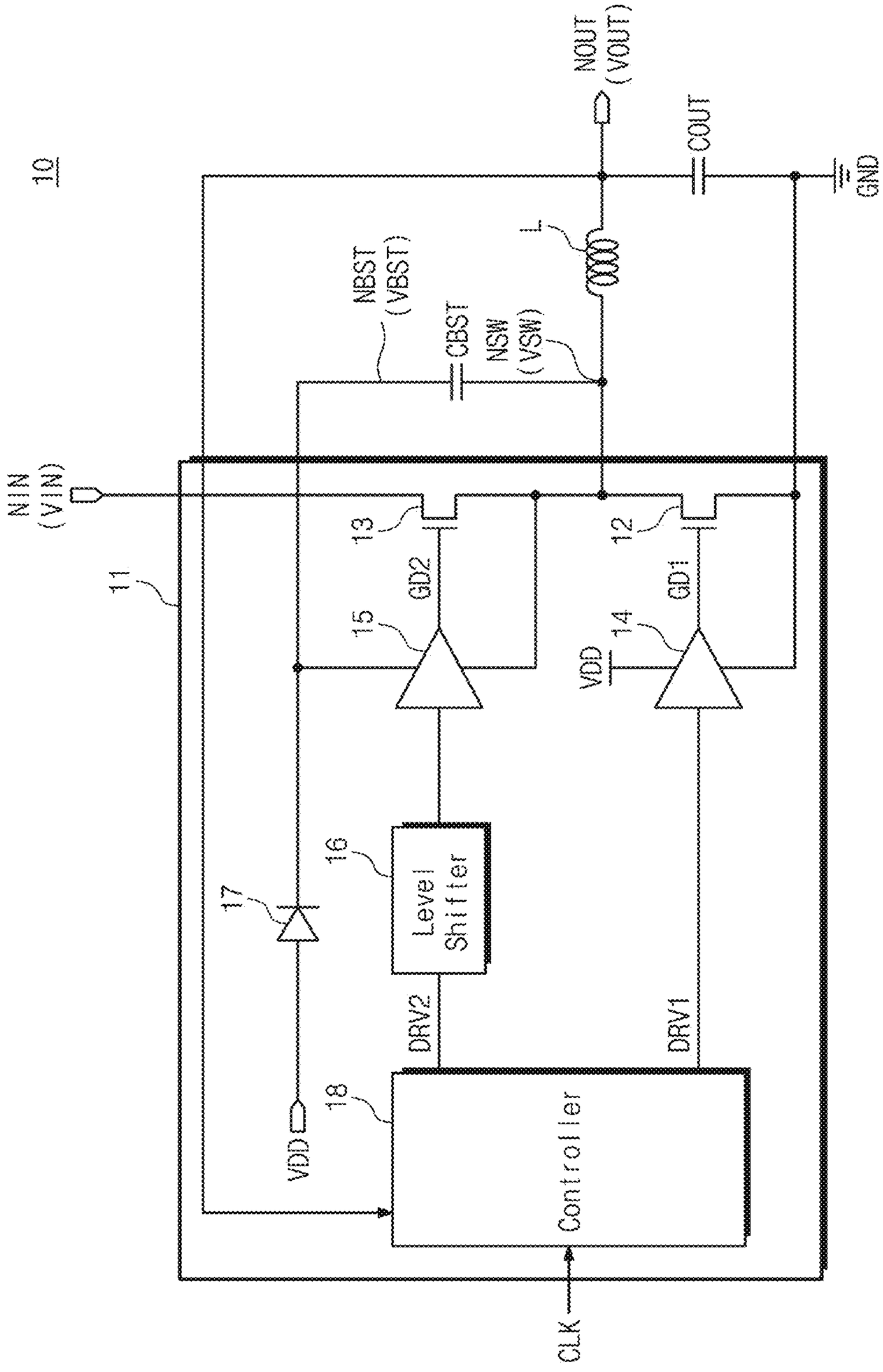

10
NOUT
(VOUT)
COUT
GND
L
NBST
(VBST)
CBST
NSW
(VSW)
NIN
(VIN)
11
13
GD2
15
12
GD1
14
VDD
16
Level
Shifter
17
DRV2
DRV1
18
VDD
Controller
CLK

FIG. 2

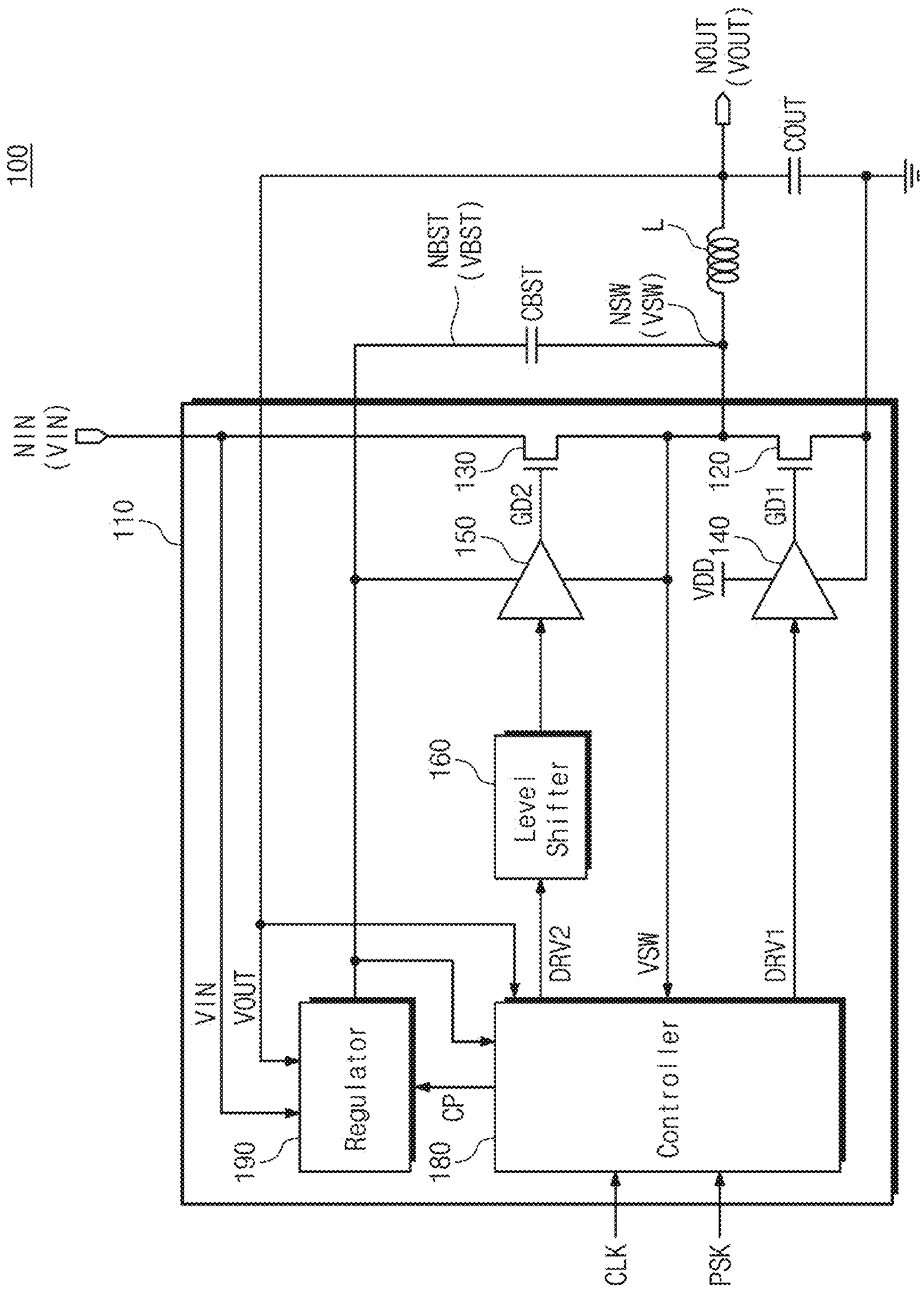

100
NOUT (VOUT)
COUT
NBST (VBST)
CBST
NSW (VSW)
L
NIN (VIN)
110
130
GD2
150
120
GD1
VDD
140
160
Level Shifter
DRV2
VSW
DRV1
VIN
VOUT
190
Regulator
180
CP
Controller
CLK
PSK

FIG. 3

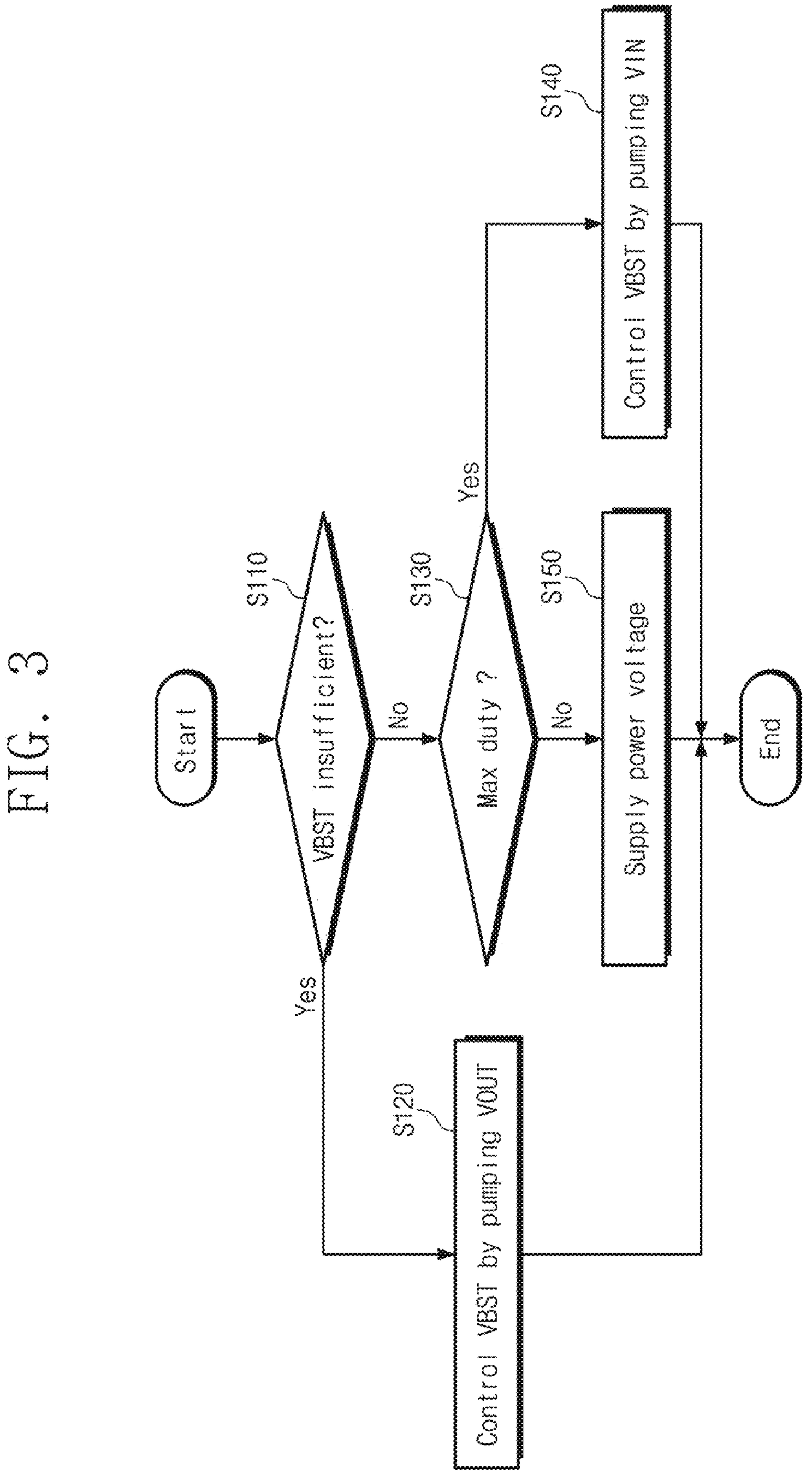

Start
S110
VBST insufficient?
Yes
S120
Control VBST by pumping VOUT
No
S130
Max duty ?
Yes
S140
Control VBST by pumping VIN
No
S150
Supply power voltage
End

FIG. 4

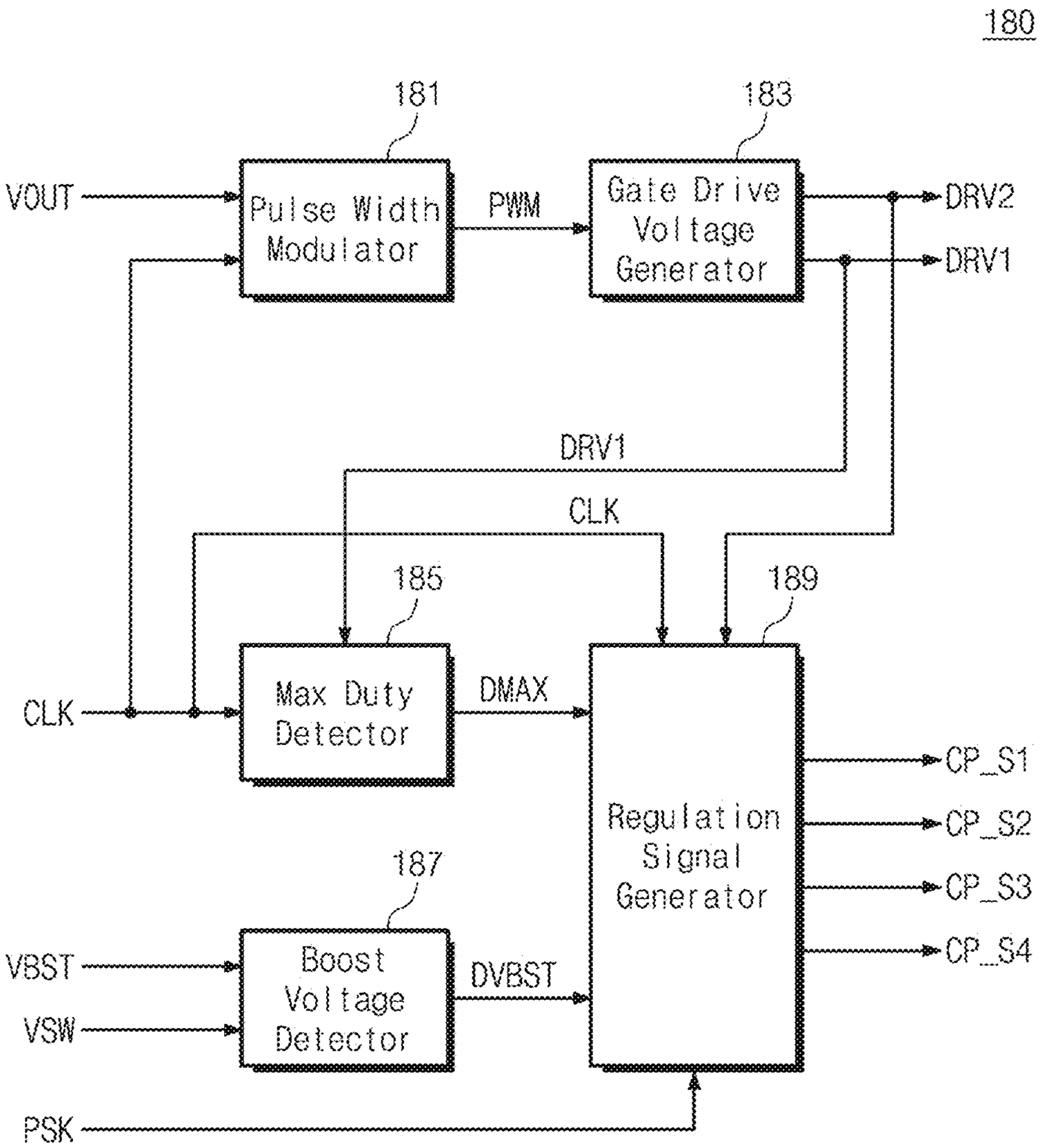

180
181
183
VOUT
Pulse Width Modulator
PWM
Gate Drive Voltage Generator
DRV2
DRV1
DRV1
CLK
185
189
CLK
Max Duty Detector
DMAX
Regulation Signal Generator
CP_S1
CP_S2
CP_S3
CP_S4
187
VBST
VSW
Boost Voltage Detector
DVBST
PSK

FIG. 5

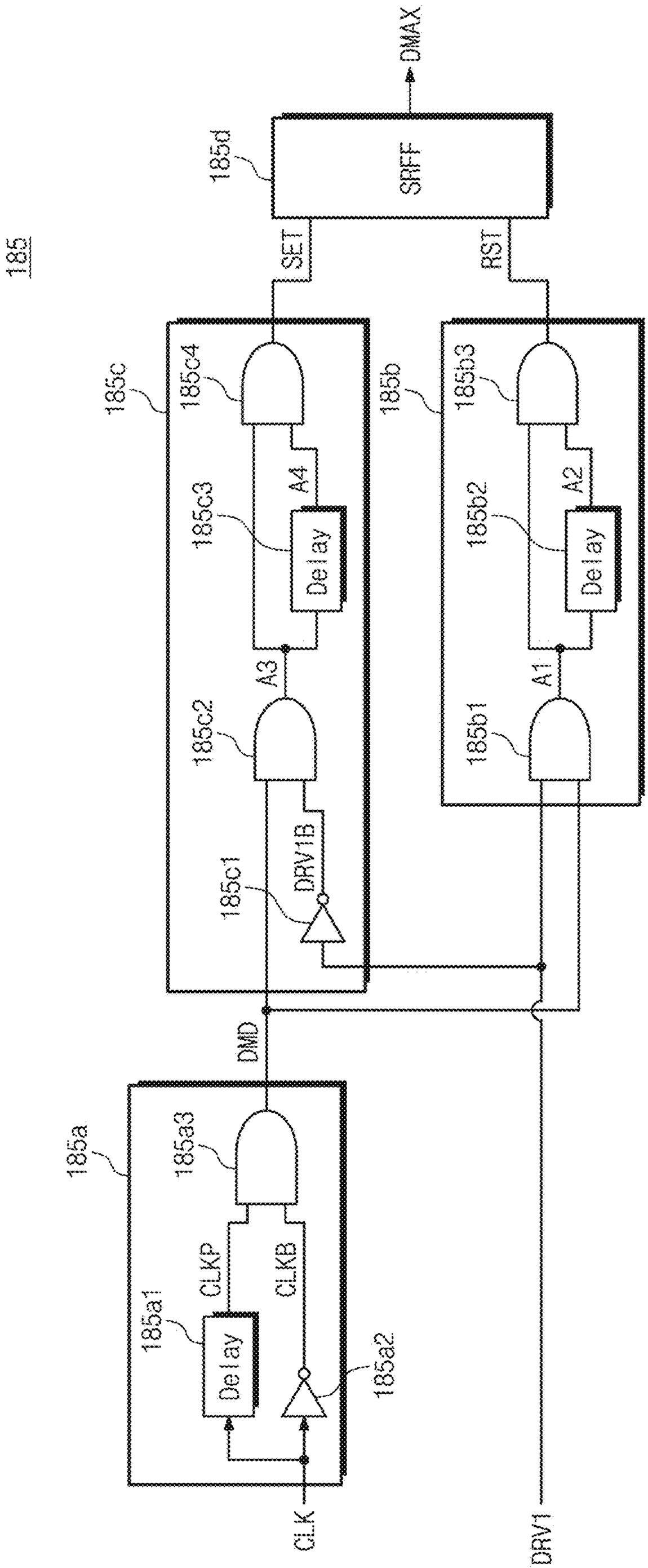

185
DMAX
185d
SRFF
SET
RST
185c
185c4
A4
185c3
Delay
A3
185c2
DRV1B
185c1
185b
185b3
A2
185b2
Delay
A1
185b1
DMD
185a
185a3
CLKP
CLKB
185a1
Delay
185a2
CLK
DRV1

FIG. 6

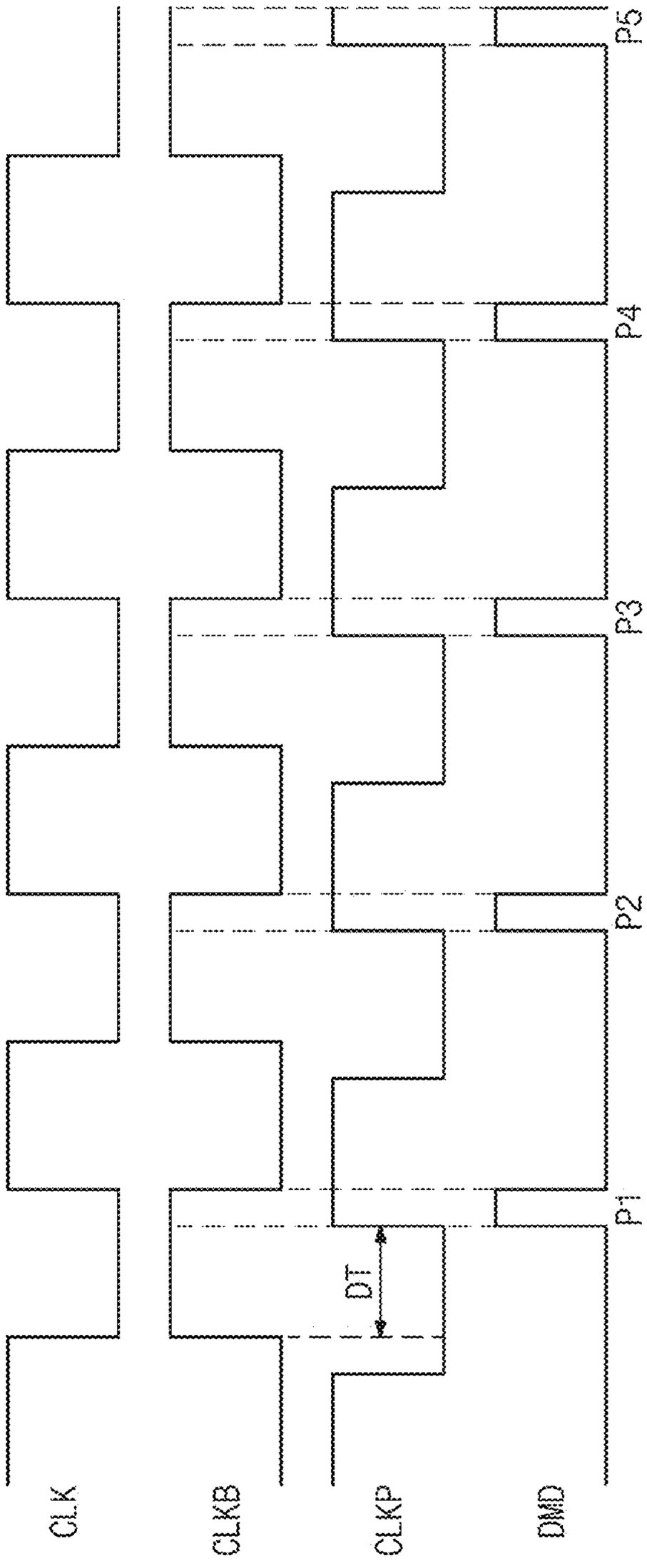


FIG. 7

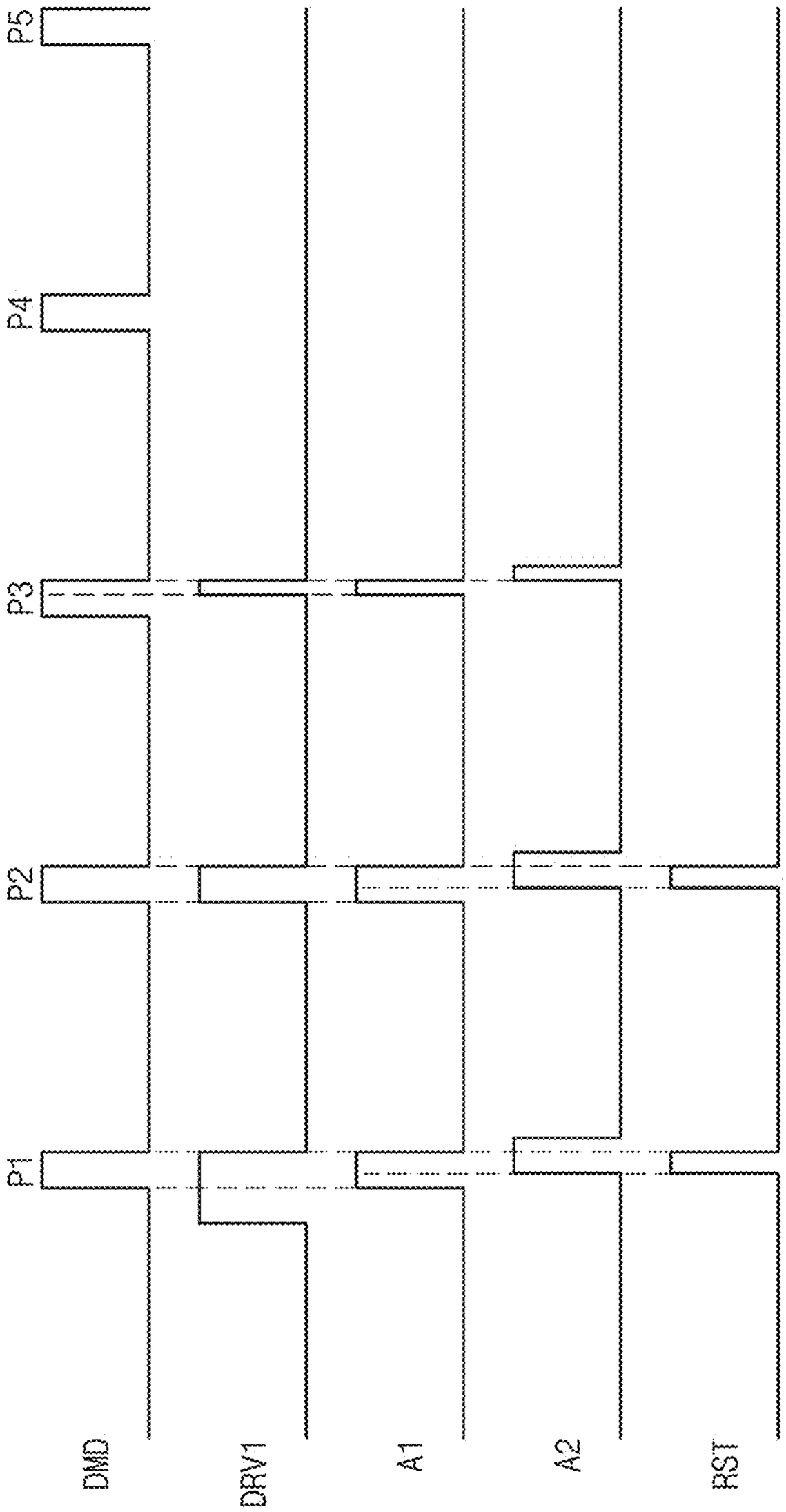


FIG. 8

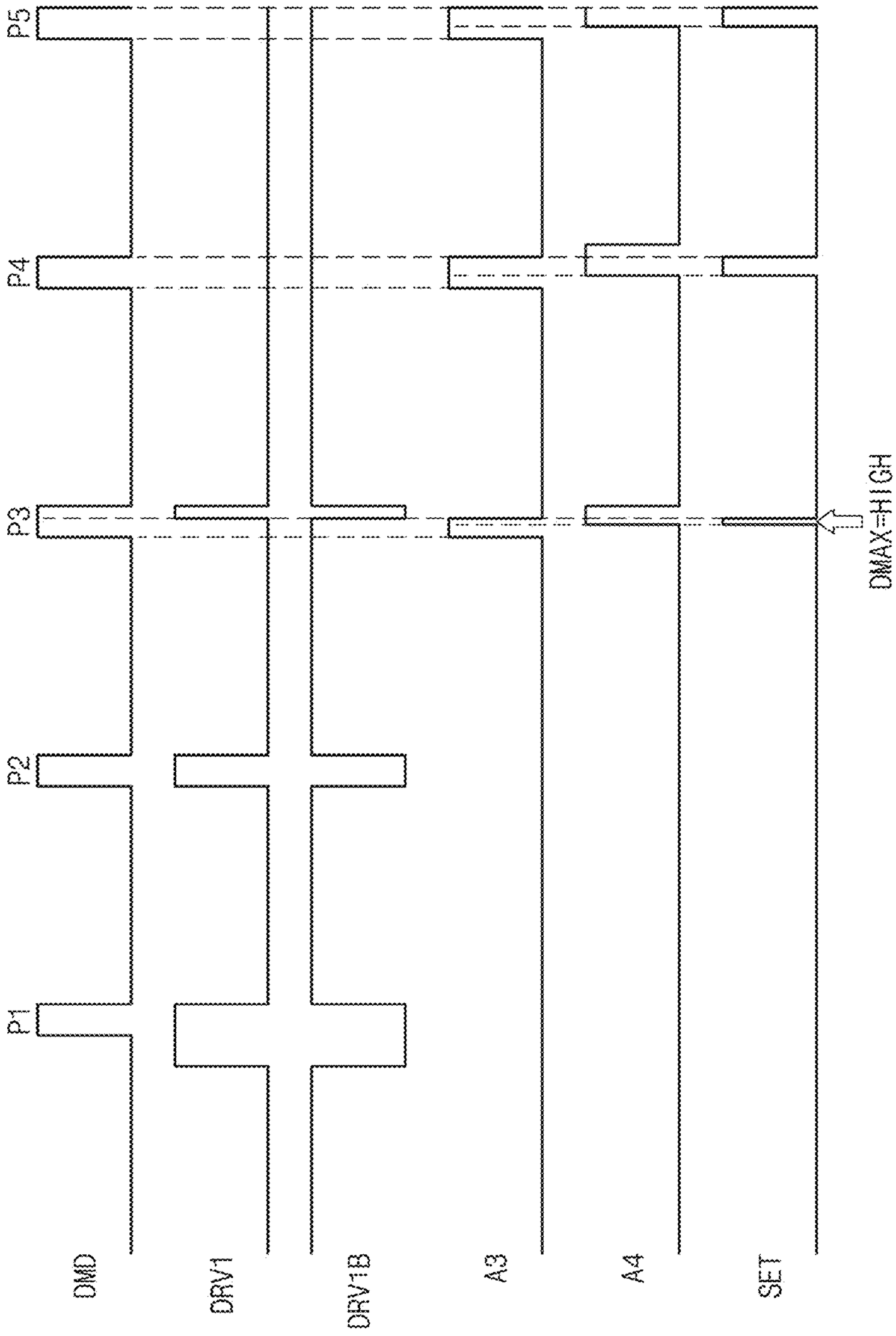


FIG. 9

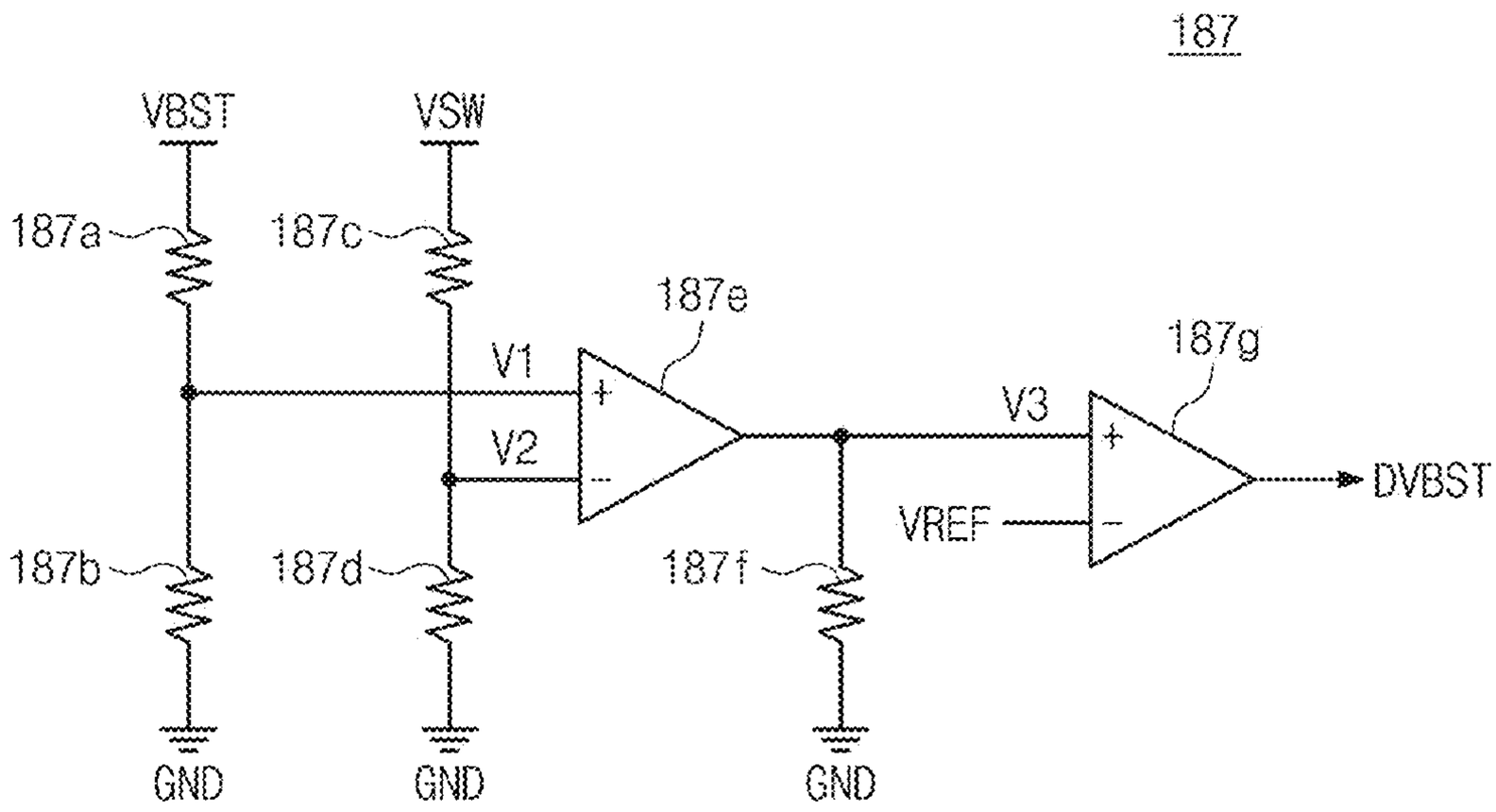

187
VBST
VSW
187a
187c
187e
V1
V2
187g
V3
DVBST
VREF
187b
187d
187f
GND
GND
GND

FIG. 10

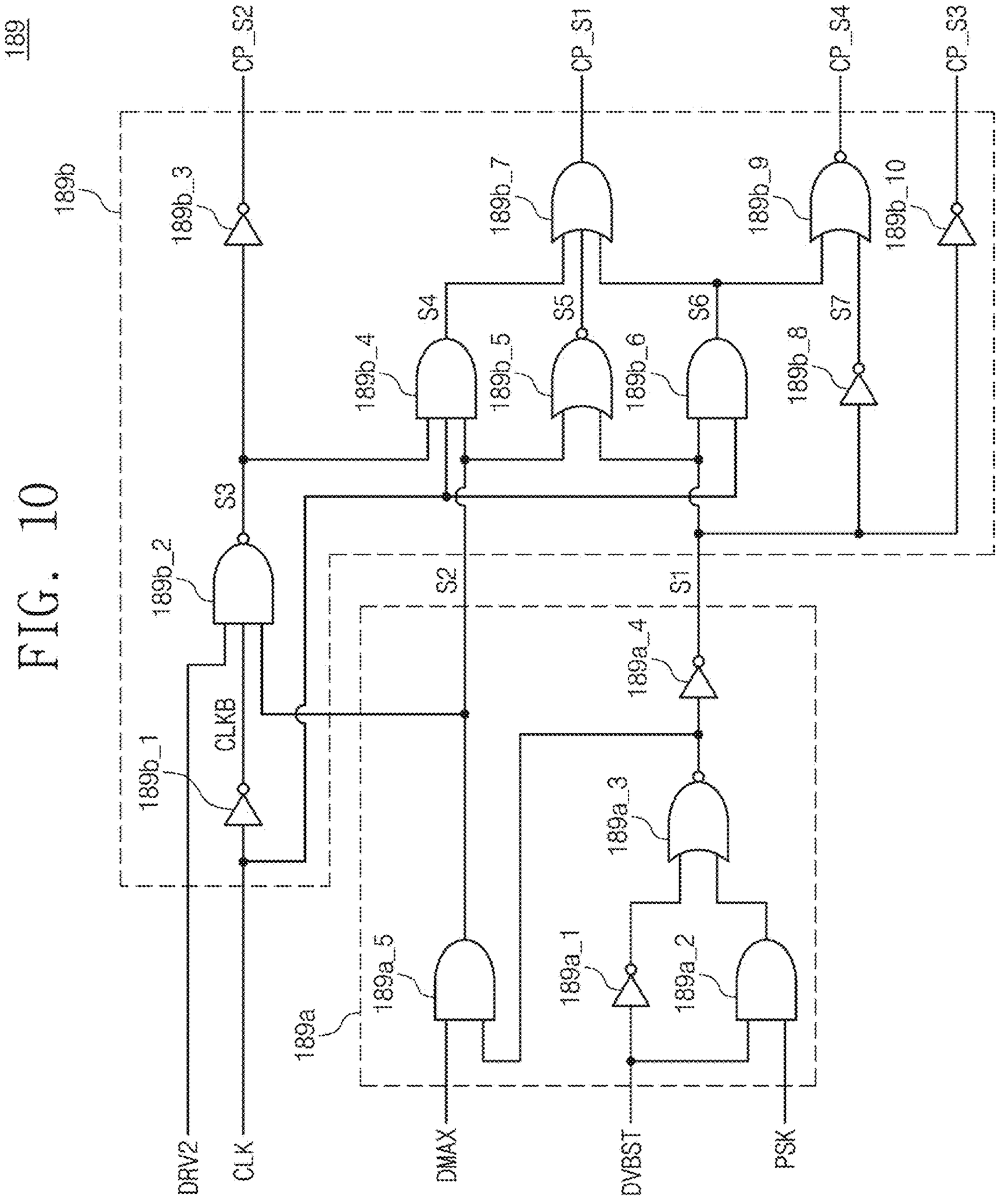

189
CP_S2
CP_S1
CP_S4
CP_S3
189b
189b_3
189b_7
189b_9
189b_10
S4
S5
S6
S7
189b_4
189b_5
189b_6
189b_8
S3
189b_2
S2
S1
189a_4
CLKB
189b_1
189a_3
189a
189a_5
189a_1
189a_2
DRV2
CLK
DMAX
DVBST
PSK

FIG. 11

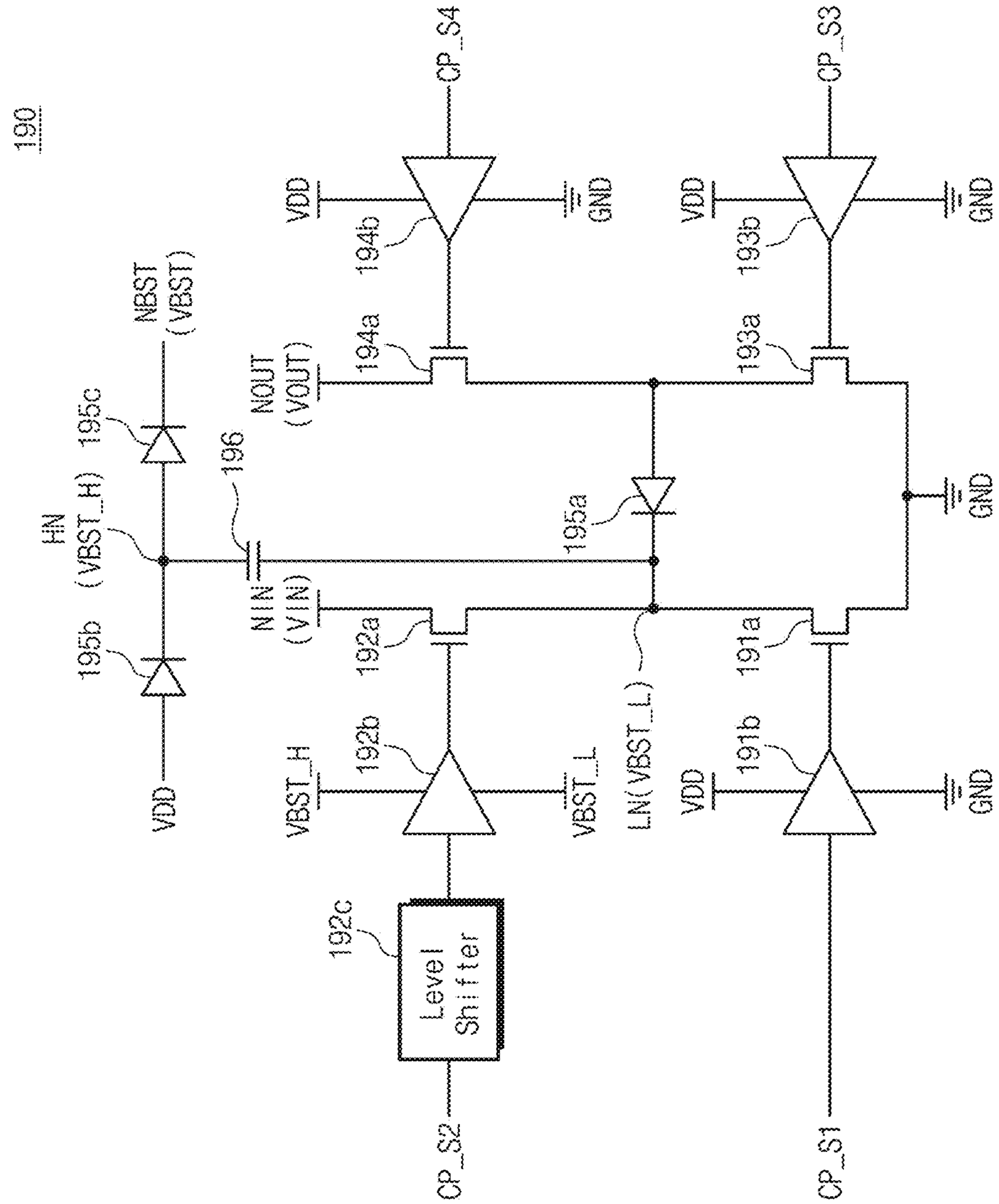

190
NBST (VBST)
HN (VBST_H)
195c
195b
VDD
196
NOUT (VOUT)
NIN (VIN)
194a
194b
193a
193b
195a
192a
192b
192c
Level Shifter
VBST_H
VBST_L
LN(VBST_L)
VDD
191a
191b
GND
CP_S4
CP_S3
CP_S2
CP_S1

FIG. 12

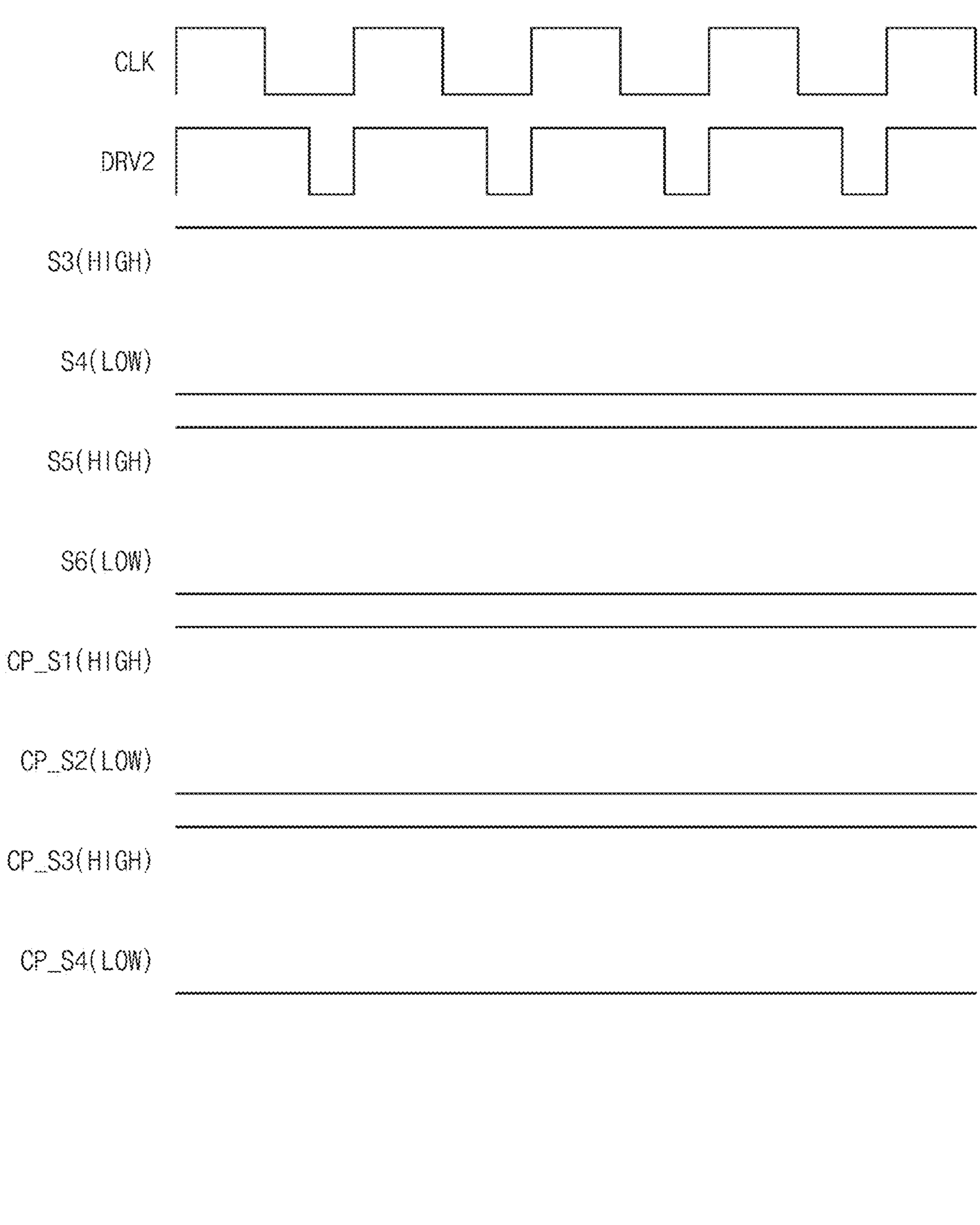

CLK
DRV2
S3(HIGH)
S4(LOW)
S5(HIGH)
S6(LOW)
CP_S1(HIGH)
CP_S2(LOW)
CP_S3(HIGH)
CP_S4(LOW)

FIG. 13

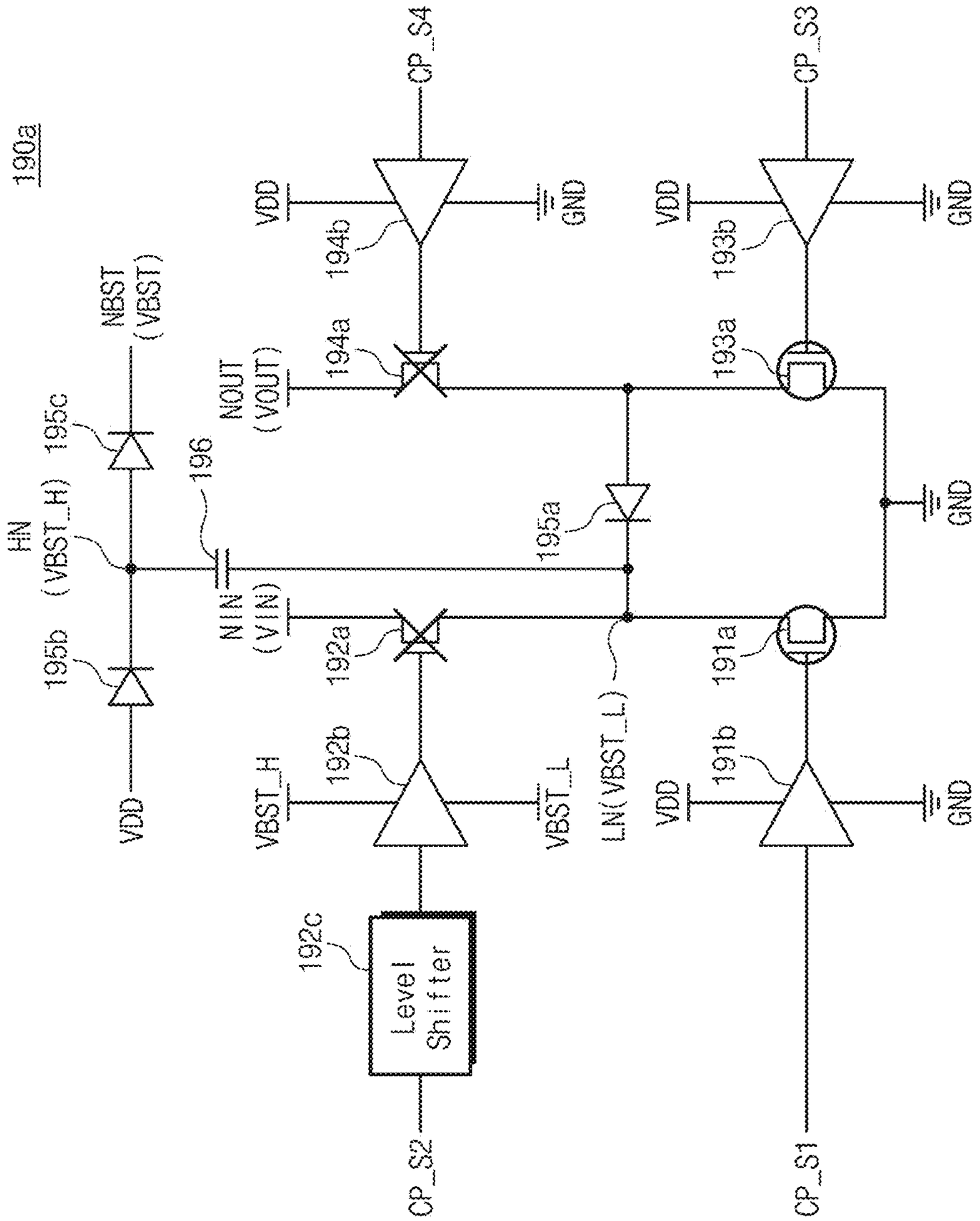

190a
HN
(VBST_H)
NBST
(VBST)
NOUT
(VOUT)
NIN
(VIN)
LN(VBST_L)
VBST_H
VBST_L
VDD
GND
CP_S4
CP_S3
CP_S2
CP_S1
195b
195c
196
194b
194a
193b
193a
195a
192a
192b
192c
191a
191b
Level Shifter

FIG. 14

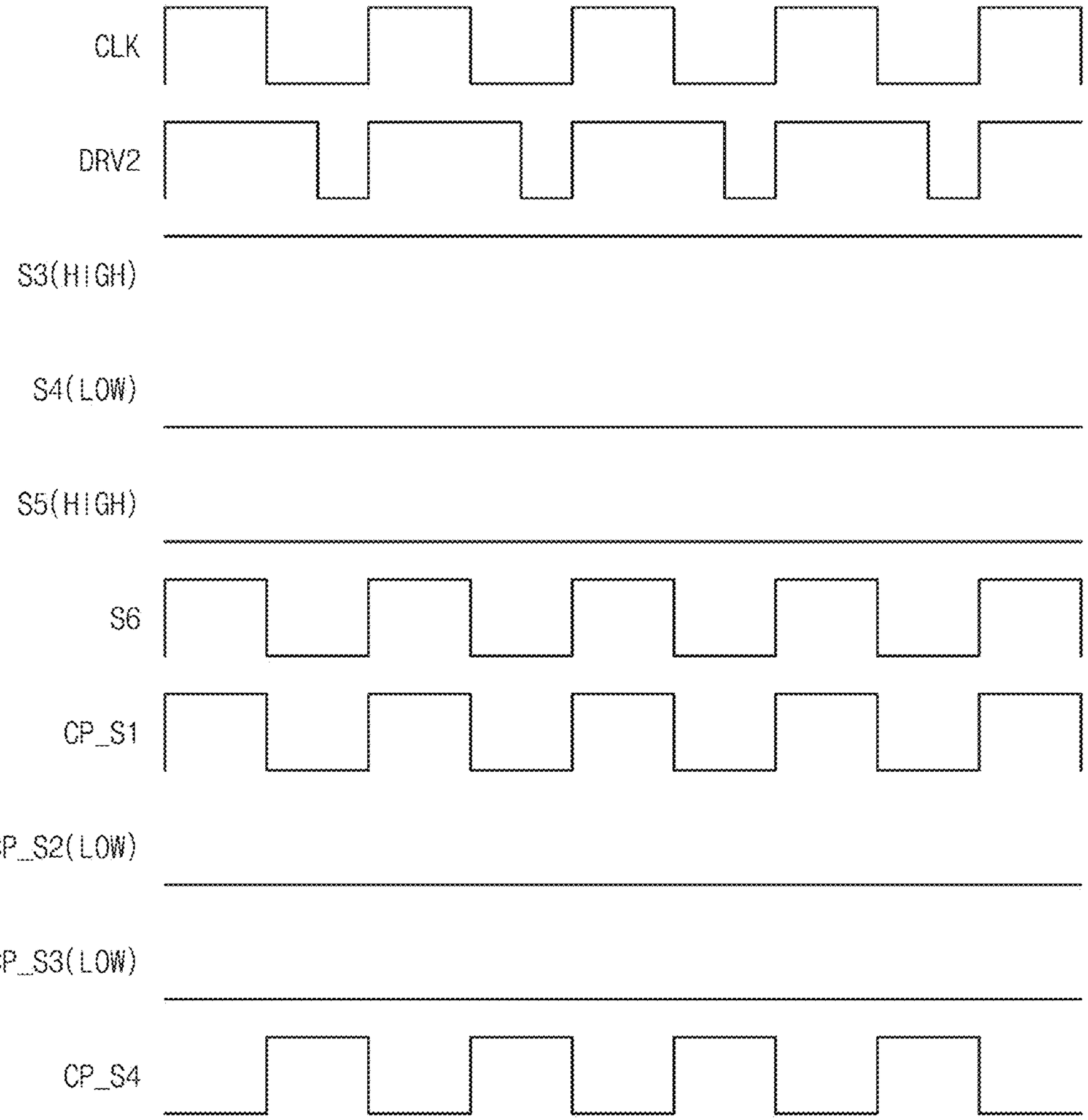


FIG. 15

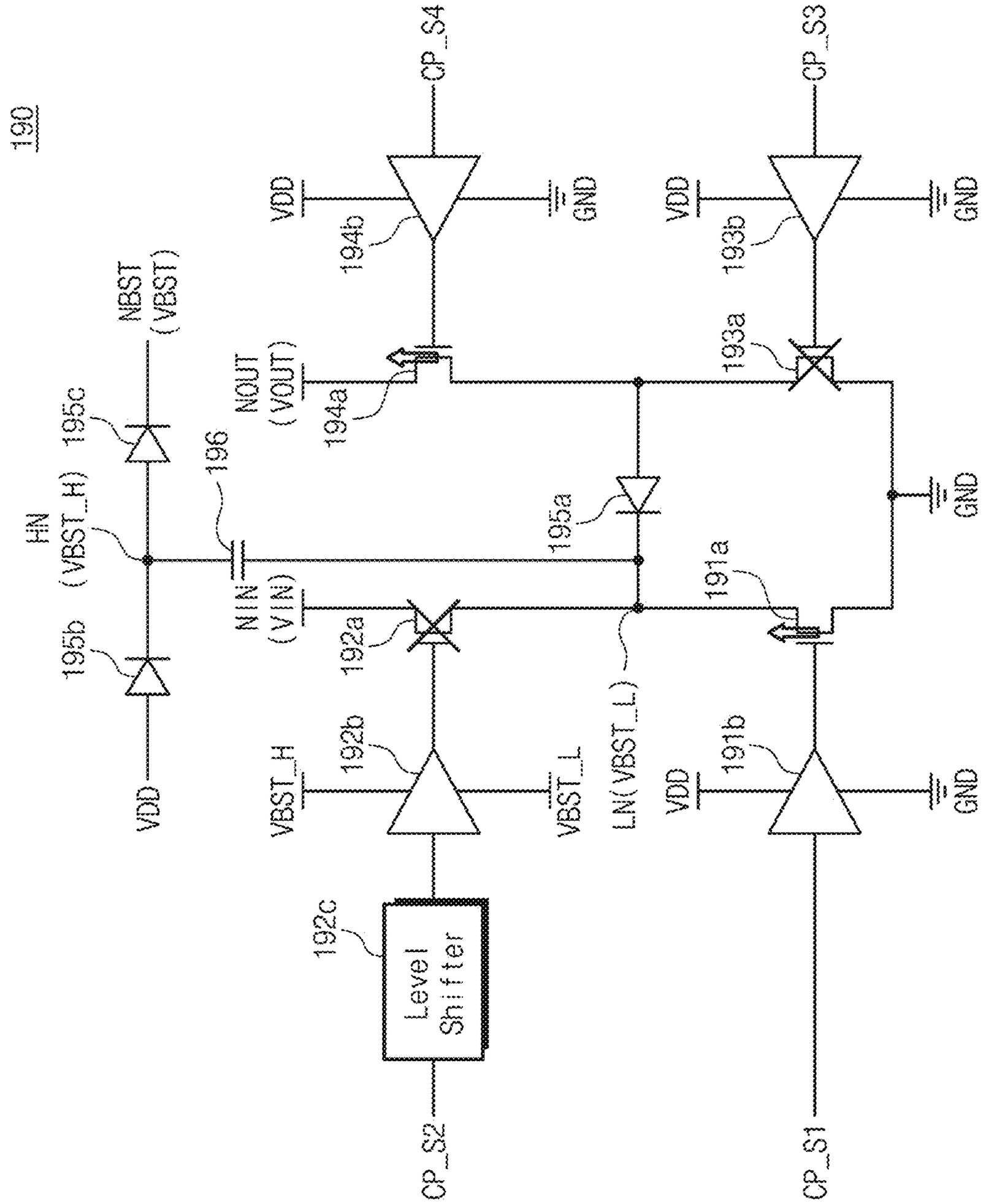

190
CP_S4
VDD
GND
194b
CP_S3
VDD
GND
193b
NBST (VBST)
HN (VBST_H)
195c
196
NOUT (VOUT)
194a
193a
195a
GND
195b
NIN (VIN)
192a
191a
VBST_H
192b
VBST_L
LN(VBST_L)
VDD
191b
GND
192c
Level Shifter
CP_S2
CP_S1

FIG. 16

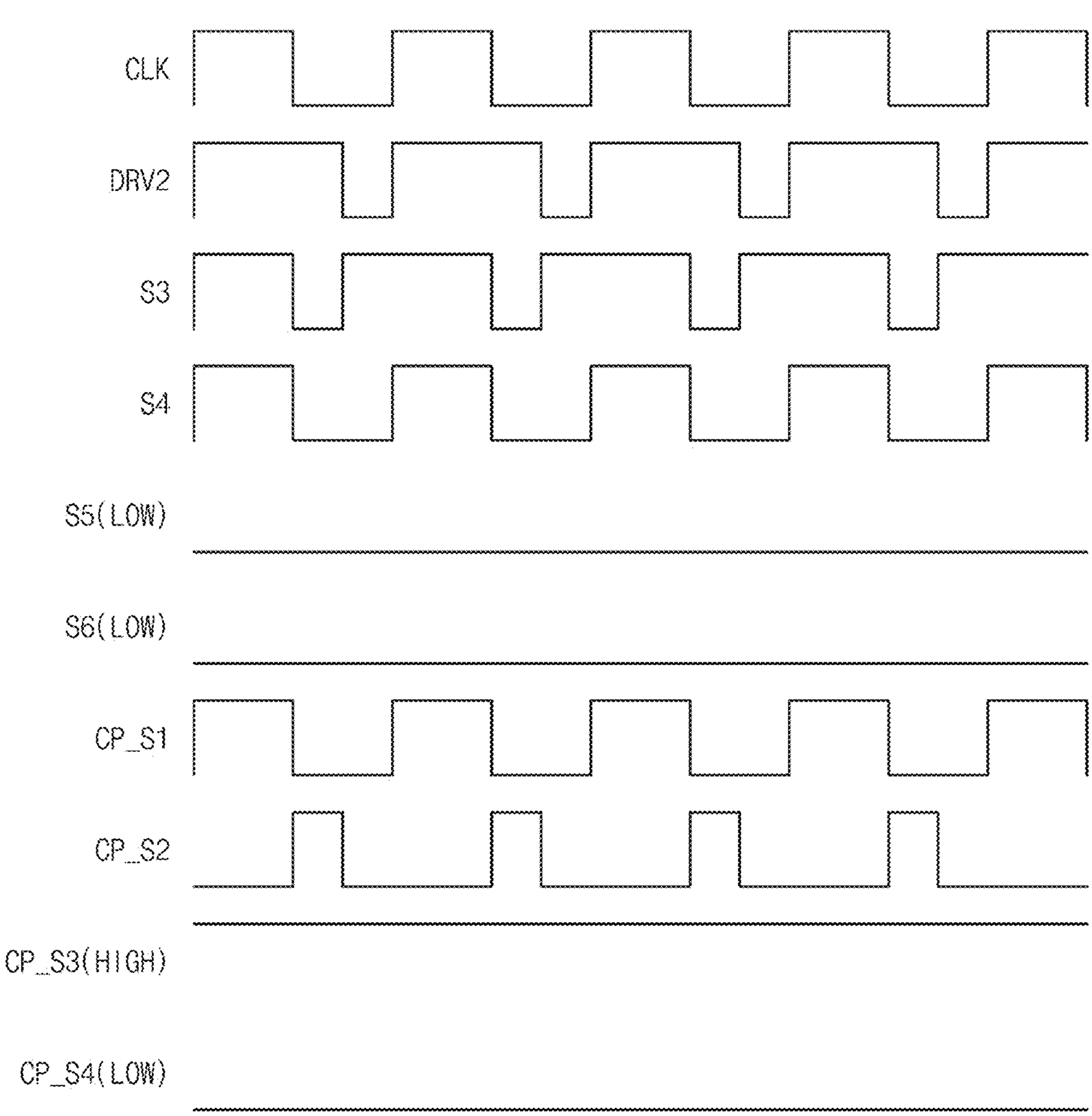


FIG. 17

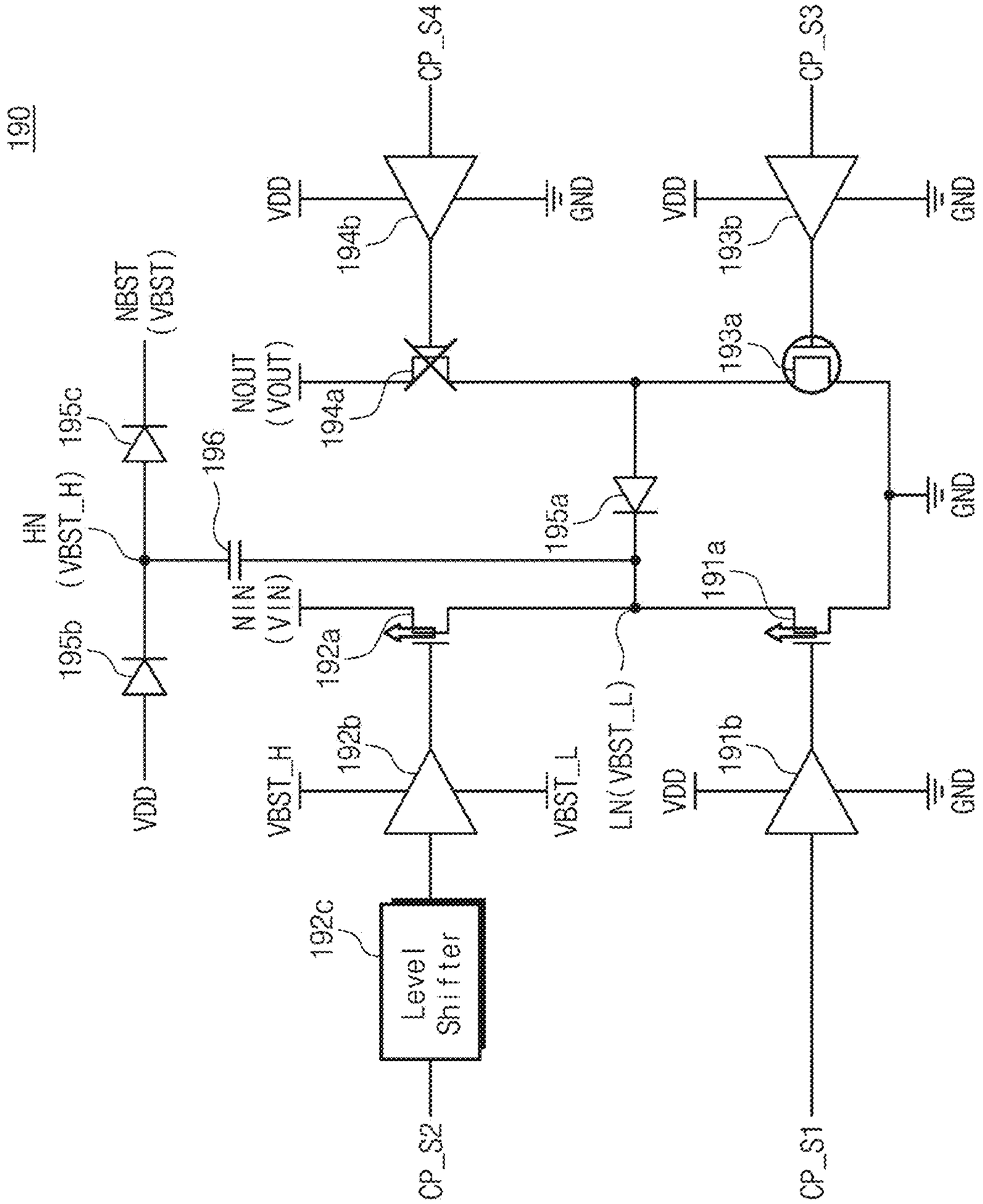

190
NBST (VBST)
HN (VBST_H)
195c
195b
196
NOUT (VOUT)
NIN (VIN)
194a
194b
193a
193b
195a
192a
192b
192c
191a
191b
VDD
VBST_H
VBST_L
LN(VBST_L)
GND
Level Shifter
CP_S1
CP_S2
CP_S3
CP_S4

FIG. 18

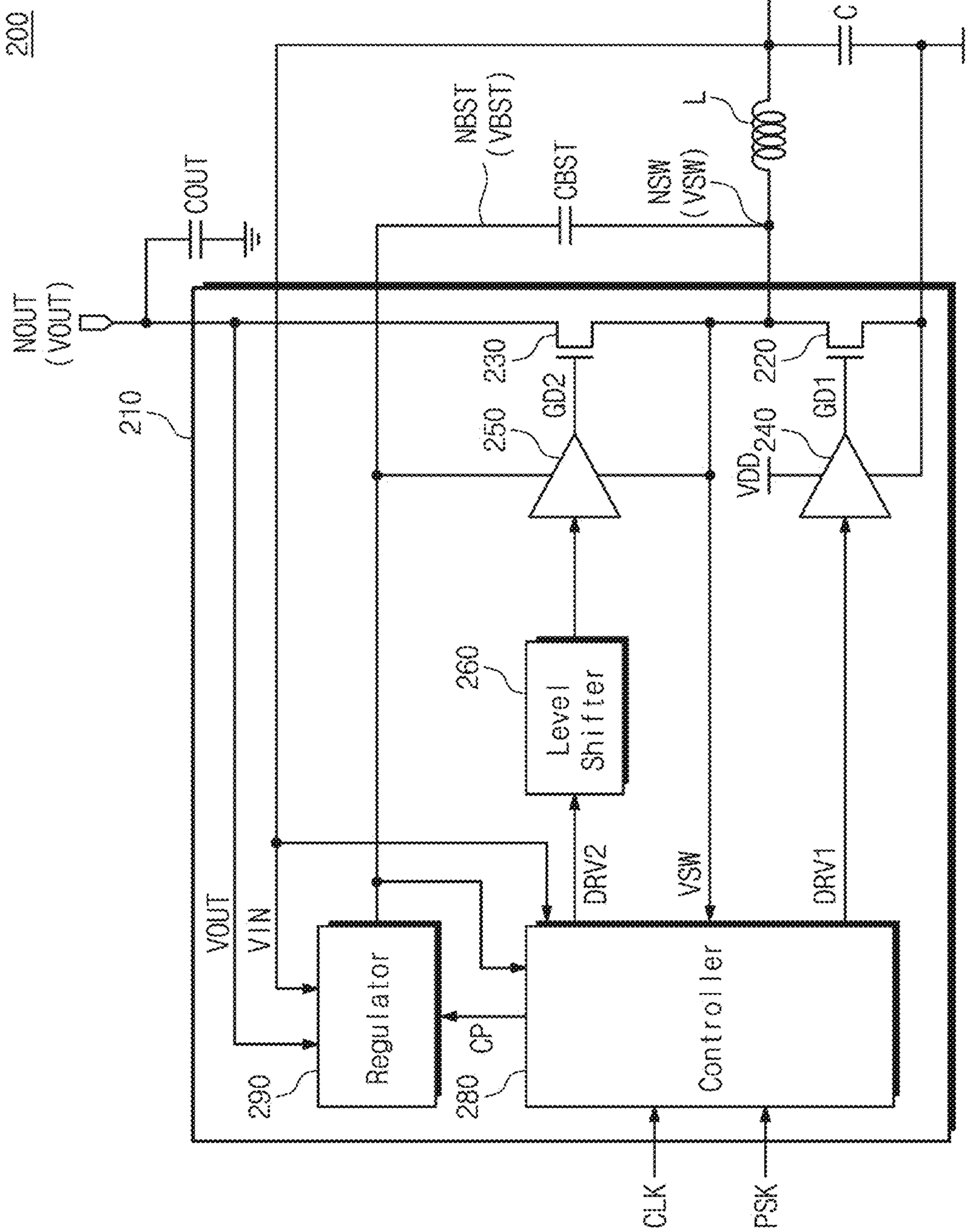

200
NIN (VIN)
CIN
NBST (VBST)
CBST
NSW (VSW)
L
COUT
NOUT (VOUT)
210
230
GD2
250
220
GD1
VDD
240
260
Level Shifter
DRV2
VSW
DRV1
VOUT
VIN
290
Regulator
280
CP
Controller
CLK
PSK

FIG. 19

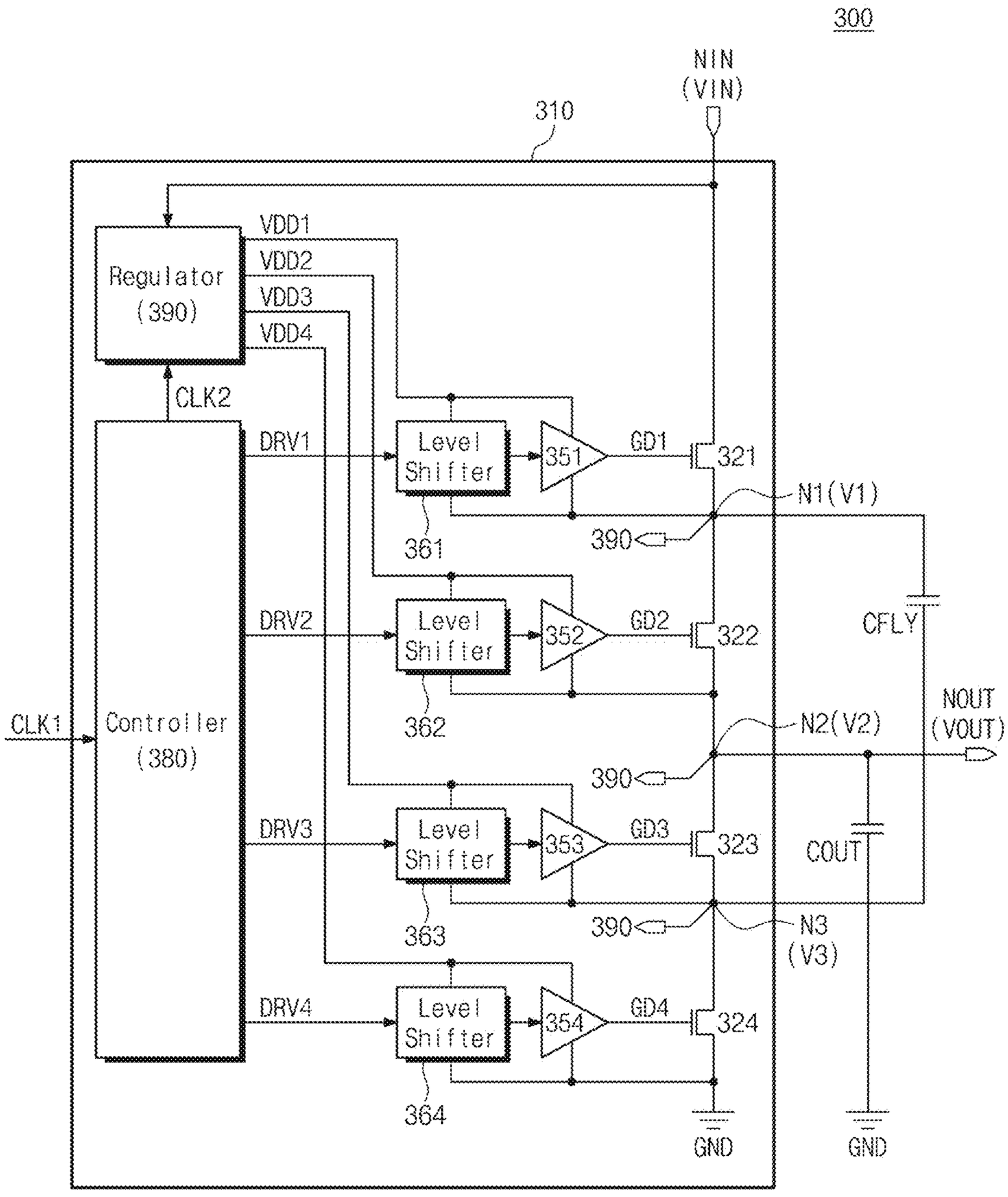

300
NIN
(VIN)
310
Regulator
(390)
VDD1
VDD2
VDD3
VDD4
CLK2
DRV1
Level
Shifter
351
GD1
321
N1(V1)
361
390
DRV2
Level
Shifter
352
GD2
322
CFLY
CLK1
Controller
(380)
362
N2(V2)
NOUT
(VOUT)
390
DRV3
Level
Shifter
353
GD3
323
COUT
363
390
N3
(V3)
DRV4
Level
Shifter
354
GD4
324
364
GND
GND

FIG. 20

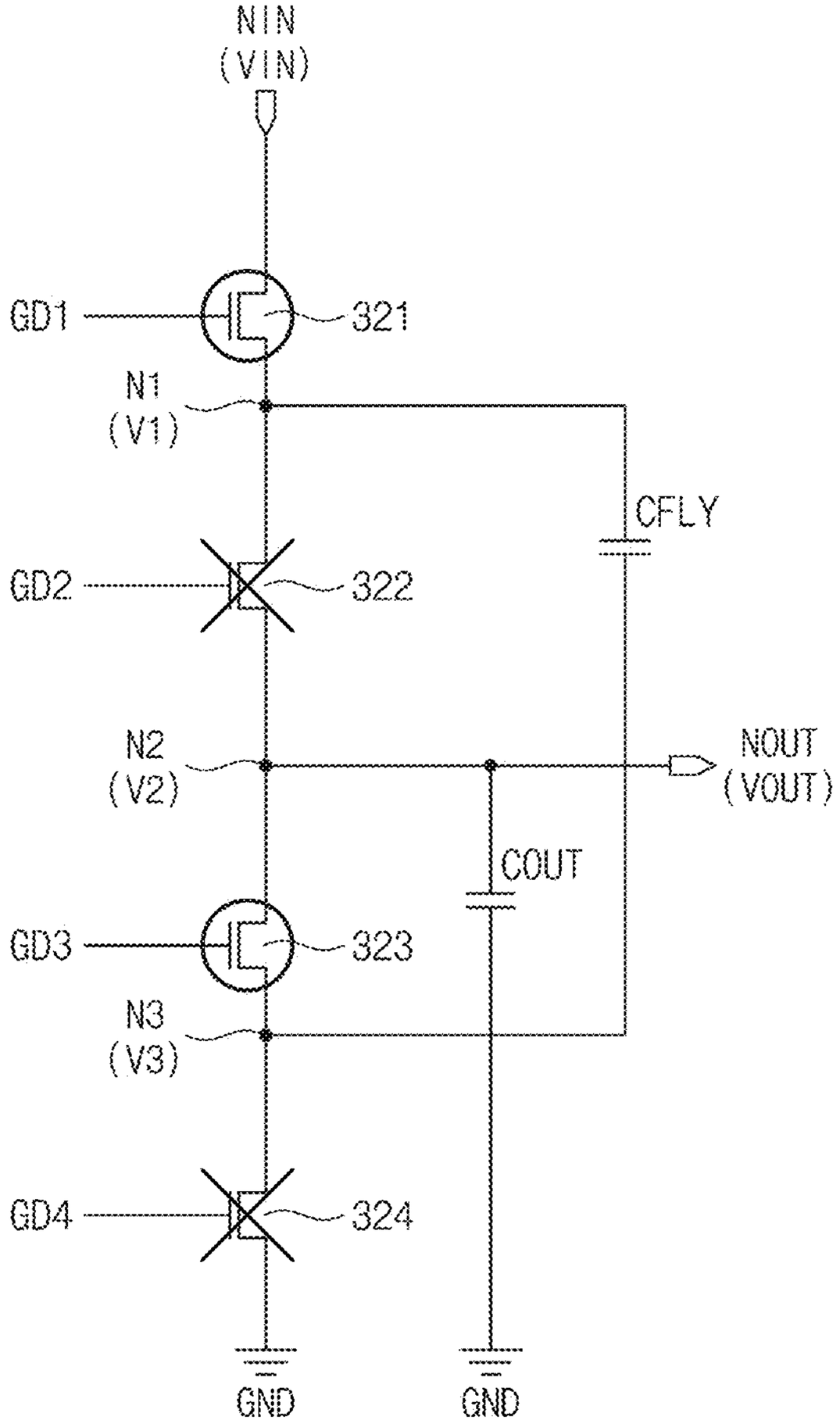

NIN
(VIN)
GD1
321
N1
(V1)
CFLY
GD2
322
N2
(V2)
NOUT
(VOUT)
COUT
GD3
323
N3
(V3)
GD4
324
GND
GND

FIG. 21

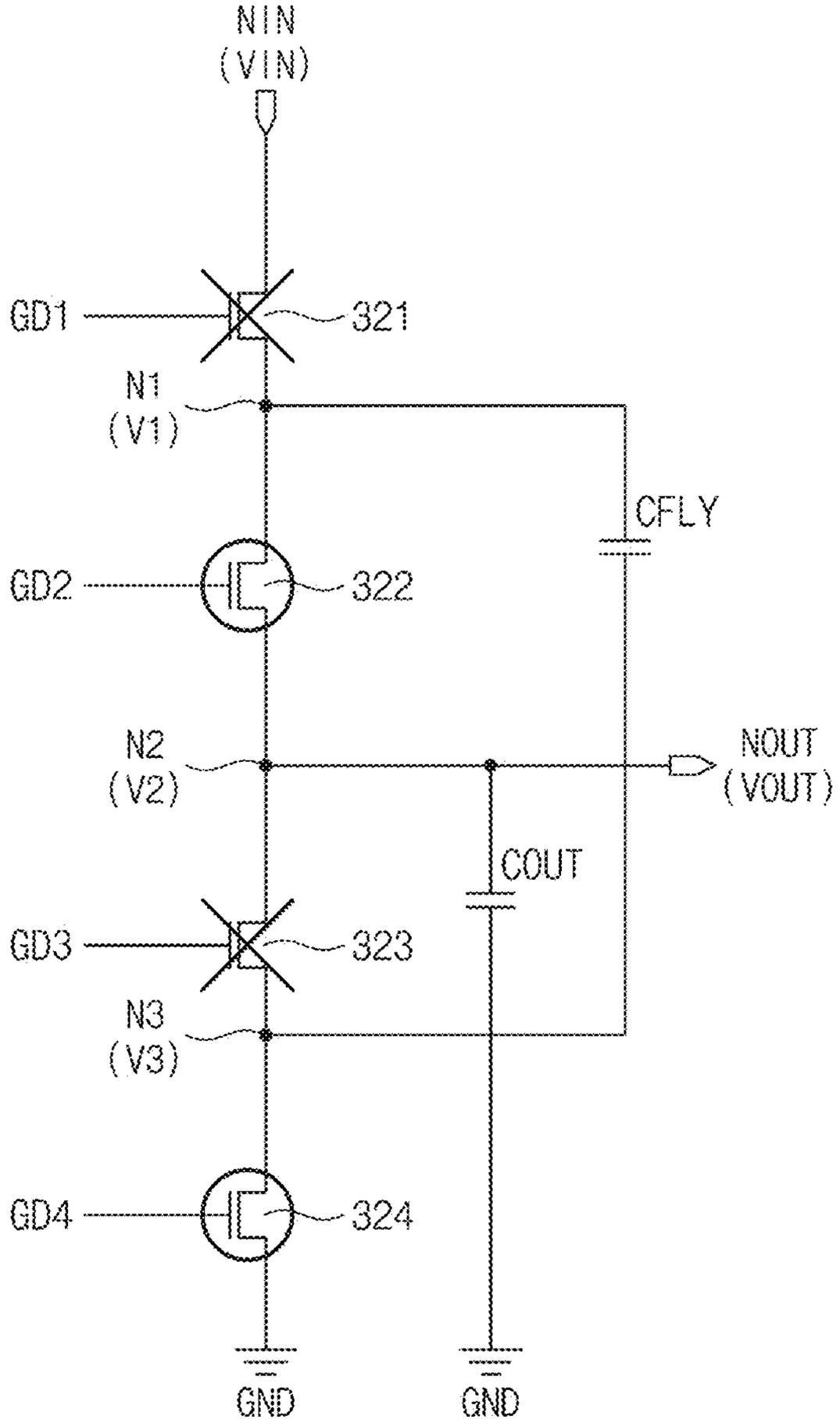
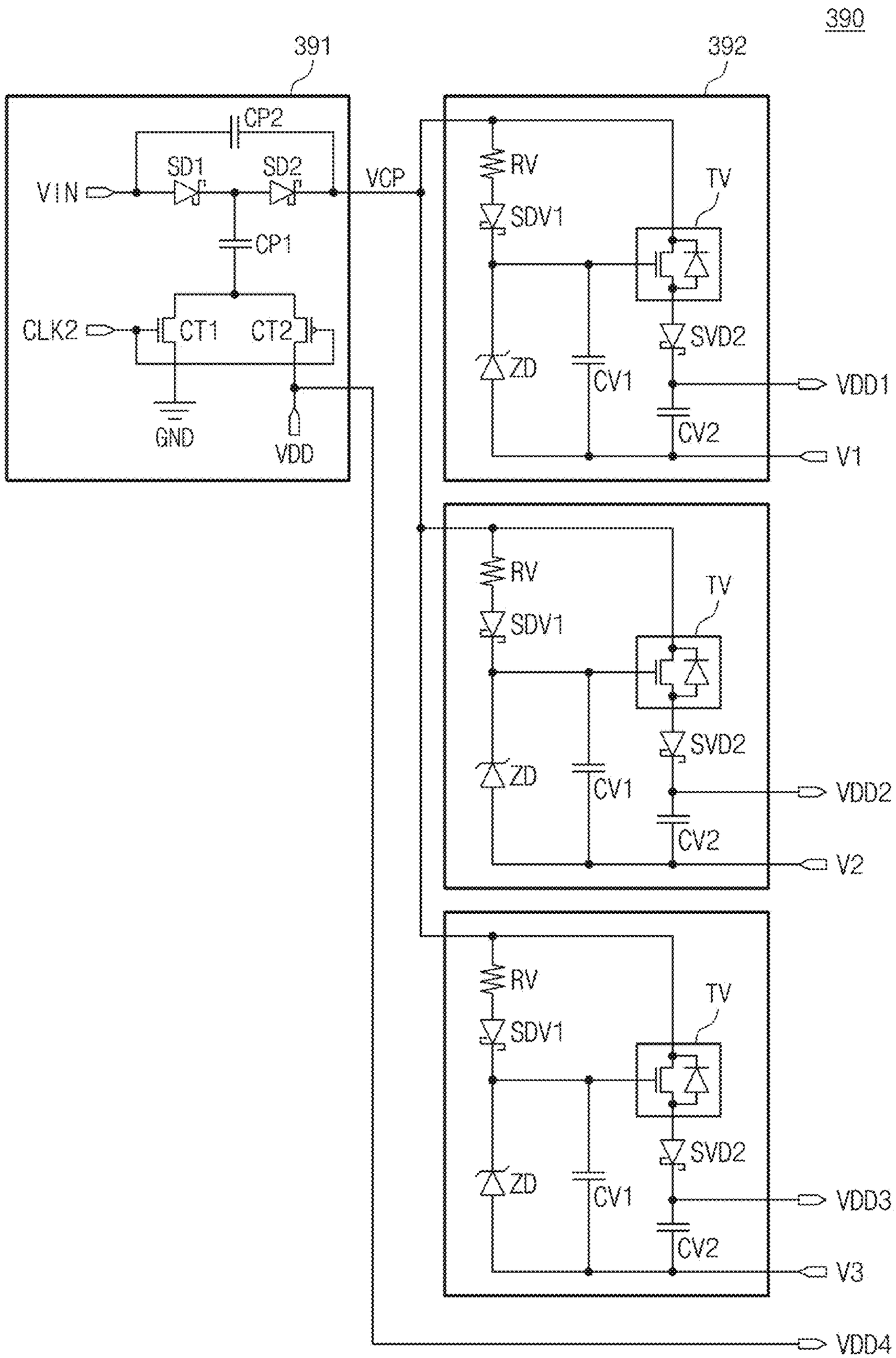

NIN
(VIN)
GD1
321
N1
(V1)
CFLY
GD2
322
N2
(V2)
NOUT
(VOUT)
COUT
GD3
323
N3
(V3)
GD4
324
GND
GND

FIG. 22


390
391
392
CP2
SD1
SD2
VIN
VCP
CP1
CLK2
CT1
CT2
GND
VDD
RV
SDV1
TV
SVD2
ZD
CV1
VDD1
CV2
V1
RV
SDV1
TV
SVD2
ZD
CV1
VDD2
CV2
V2
RV
SDV1
TV
SVD2
ZD
CV1
VDD3
CV2
V3
VDD4

VOLTAGE CONVERTER AND OPERATING METHOD OF VOLTAGE CONVERTER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation-In-Part of U.S. application Ser. No. 15/967,687, filed on May 1, 2018, now U.S. Pat. No. 10,361,620 issued Jul. 23, 2019, which claims priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2017-0115348, filed on Sep. 8, 2017, in the Korean Intellectual Property Office, the entire contents of each of which are hereby incorporated by reference.

BACKGROUND

Example embodiments of the inventive concepts disclosed herein relate to semiconductor circuits, and more particularly, to voltage converters and/or operating methods thereof.

A voltage converter is configured to convert a level of an input voltage and output the converted input voltage as an output voltage. The voltage converter is used in various electronic devices. Generally, a supply voltage provided in a home, a company, or a public facility has a level of 110 V or 220 V.

However, electronic devices usually use internal voltages having a level lower than 110 V or 220 V. To convert the supply voltage to internal voltages, various voltage converters are used in an electronic device. Accordingly, there is an increasing demand for highly reliable voltage converters to be used in various electronic devices.

SUMMARY

Some example embodiments of the inventive concepts provide voltage converters with improved reliability and/or an method of operating the same.

According to an example embodiment, a voltage converter includes a first transistor connected between an input node and a first node, a second transistor connected between the first node and the output node, a third transistor connected between a second node and a third node, a fourth transistor connected between the third node and a ground node, an output capacitor connected between the third node and the ground node, a flying capacitor connected between the first node and the fourth node, a first gate driver connected to a first gate of the first transistor and configured to output a first power supply voltage as a first high level and a first voltage of the first node as a first low level, a second gate driver connected to a second gate of the second transistor and configured to output a second power supply voltage as a second high level and a second voltage of the second node as a second low level, a third gate driver connected to a third gate of the third transistor and configured to output a third power supply voltage as a third high level and a third voltage of the third node as a third low level, a fourth gate driver connected to a fourth gate of the fourth transistor and configured to output a fourth power supply voltage as a fourth high level and a ground voltage of the ground node as a fourth low level, and a regulator configured to receive an input voltage from the input node, the first voltage from the first node, the second voltage from the second node and the third voltage from the third node, and generate the first power supply voltage being higher than the first voltage, the second power supply voltage being higher than the second voltage, the third power supply voltage being higher than the third voltage and the fourth power supply voltage being higher than a ground voltage of the ground node.

According to an example embodiment, a method of operating a voltage converter includes obtaining a first voltage between a first transistor and a second transistor, a second voltage between the second transistor and a third transistor, and a third voltage between the third transistor and a fourth transistor, the first through fourth transistors being connected in series between an input node and a ground node, generating a first power supply voltage higher than the first voltage based on the first voltage, generating a second power supply voltage higher than the second voltage based on the second voltage, generating a third power supply voltage higher than the third voltage based on the third voltage, generating a fourth power supply voltage higher than a ground voltage of the ground node, applying the first power supply voltage to a gate of the first transistor in a first phase and the first voltage to the gate of the first transistor in a second phase, applying the second voltage to a gate of the second transistor in the first phase and the second power supply voltage to the gate of the second transistor in the second phase, applying the third power supply voltage to a gate of the third transistor in the first phase and the third voltage to the gate of the third transistor in the second phase, and applying the ground voltage to a gate of the fourth transistor in the first phase and the fourth power supply voltage to the gate of the fourth transistor in the second phase. An output capacitor is connected between the ground node and a first node between the second and third transistors. A flying capacitor is connected between a second node and a third node, the second node being between the first transistor and the second transistor, the third node being between the third transistors and the fourth transistors.

According to an example embodiment, a voltage converter comprises a first transistor connected between an input node and a first node, a second transistor connected between the first node and the output node, a third transistor connected between a second node and a third node, a fourth transistor connected between the third node and a ground node, an output capacitor connected between the third node and the ground node, a flying capacitor connected between the first node and the fourth node, a first gate driver connected to a first gate of the first transistor and configured to output a first power supply voltage as a first high level and a first voltage of the first node as a first low level, a second gate driver connected to a second gate of the second transistor and configured to output a second power supply voltage as a second high level and a second voltage of the second node as a second low level, a third gate driver connected to a third gate of the third transistor and configured to output a third power supply voltage as a third high level and a third voltage of the third node as a third low level, a fourth gate driver connected to a fourth gate of the fourth transistor and configured to output a fourth power supply voltage as a fourth high level and a fourth voltage of the fourth node as a fourth low level, a regulator configured to receive an input voltage from the input node, the first voltage from the first node, the second voltage from the second node and the third voltage from the third node, and generate the first power supply voltage being higher than the first voltage, the second power supply voltage being higher than the second voltage, the third power supply voltage being higher than the third voltage and the fourth power supply voltage being higher than a ground voltage of the ground node, a controller configured to output a first driving signal, a second driving signal, a third driving signal and a fourth

driving signal, the first through fourth driving signals belong to a voltage domain between a common power supply voltage and the ground voltage, a first level shifter configured to convert the first driving signal to a first voltage domain to output the converted first driving signal to the first gate driver, the first voltage domain being between the first power supply voltage and the first voltage, a second level shifter configured to convert the second driving signal to a second voltage domain to output the converted second driving signal to the second gate driver, the second voltage domain being between the second power supply voltage and the second voltage, and a third level shifter configured to convert the third driving signal to a third voltage domain to output the converted third driving signal to the third gate driver, the third voltage domain being between the third power supply voltage and the third voltage. The fourth driving signal is transferred to the fourth gate driver. The regulator includes a charge pump configured to receive a common power supply voltage, the input voltage and a clock signal, and output a pump voltage which is the common power supply voltage plus the input voltage in response to the clock signal, a first generator configured to receive the pump voltage and the first voltage, and output the first power supply voltage, a second generator configured to receive the pump voltage and the second voltage, and output the second power supply voltage, and a third generator configured to receive the pump voltage and the third voltage, and output the third power supply voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and features will become apparent from the following description with reference to the following figures, wherein like reference numerals refer to like parts throughout the various figures unless otherwise specified, and wherein:

FIG. **1** illustrates a voltage converter according to an example embodiment of the inventive concepts;

FIG. **2** illustrates a voltage converter according to an example embodiment of the inventive concepts, for solving the above-described issues;

FIG. **3** is a flowchart illustrating an operating method of the voltage converter according to an example embodiment of the inventive concepts;

FIG. **4** is a block diagram illustrating a controller according to an example embodiment of the inventive concepts;

FIG. **5** illustrates an example of a max duty detector according to an example embodiment of the inventive concepts;

FIG. **6** illustrates an example in which a max duty detection signal is generated from a clock signal, an inverted clock signal, and a delayed clock signal;

FIG. **7** illustrates an example in which a second block generates a reset signal as a pulse width of a first driving signal changes;

FIG. **8** illustrates an example in which a third block generates a set signal as a pulse width of a first driving signal changes;

FIG. **9** illustrates an example of a boost voltage detector according to an example embodiment of the inventive concepts;

FIG. **10** illustrates an example of a regulation signal generator according to an example embodiment of the inventive concepts;

FIG. **11** illustrates an example of a regulator according to an example embodiment of the inventive concepts;

FIG. **12** illustrates an example of signals associated with a regulation signal generation block when a first signal and a second signal are deactivated;

FIG. **13** illustrates how the regulator is controlled by signals of FIG. **12**;

FIG. **14** illustrates an example of signals associated with the regulation signal generation block when a first signal is activated and a second signal are deactivated;

FIG. **15** illustrates how the regulator is controlled by signals of FIG. **14**;

FIG. **16** illustrates an example of signals associated with the regulation signal generation block when a first signal is deactivated and a second signal are activated;

FIG. **17** illustrates how the regulator is controlled by signals of FIG. **16**; and

FIG. **18** illustrates a voltage converter according to an example embodiment of the inventive concepts.

FIG. **19** illustrates a voltage converter according to another example embodiment of the inventive concepts.

FIG. **20** illustrates a first phase of the voltage converter according to an example embodiment of the inventive concepts.

FIG. **21** illustrates a second phase of the voltage converter subsequent to the first phase of FIG. **20**.

FIG. **22** illustrates an example of a regulator according to an example embodiment of the inventive concepts.

DETAILED DESCRIPTION

Below, some example embodiments of the inventive concepts may be described in detail and clearly to such an extent that an ordinary one in the art easily implements the inventive concepts.

FIG. **1** illustrates a voltage converter **10** according to an example embodiment of the inventive concepts. Referring to FIG. **1**, the voltage converter **10** includes first and second transistors **12** and **13**, first and second gate drivers **14** and **15**, a level shifter **16**, a diode **17**, a controller **18**, an output capacitor COUT, an inductor "L", and a boost capacitor CBST.

The voltage converter **10** may convert an input voltage VIN of an input node NIN to an output voltage VOUT of an output node NOUT. For example, the voltage converter **10** may be a buck converter that steps down a level of the input voltage VIN to output the output voltage VOUT.

The first and second transistors **12** and **13** may be connected in series between a ground node GND supplied with a ground voltage and the input node NIN. A node between the first and second transistors **12** and **13** may be a switch node NSW. The inductor "L" is connected between the switch node NSW and the output node NOUT. The output capacitor COUT is connected between the output node NOUT and the ground node GND.

The first gate driver **14** is biased by a power supply voltage VDD and the ground voltage. The first gate driver **14** may output a first gate driving signal GD**1** to control a gate of the first transistor **12**. The second gate driver **15** is biased by a boost voltage VBST of a boost node NBST and a switch voltage VSW of the switch node NSW. The second gate driver **15** may output a second gate driving signal GD**2** to control a gate of the second transistor **13**.

The controller **18** may receive a clock signal CLK and the output voltage VOUT. The controller **18** may control the first and second gate drivers **14** and **15** in response to the clock signal CLK and the output voltage VOUT. A first driving signal DRV**1** of the controller **18** is transmitted to the first gate driver **14**.

A second driving signal DRV2 of the controller **18** is transmitted to the second gate driver **15** through the level shifter **16**. The level shifter **16** may convert (e.g., increase) a level of the second driving signal DRV2 to a level defined by the boost voltage VBST and the switch voltage VSW.

The boost capacitor CBST is connected between the boost node NBST and the switch node NSW. The power supply voltage VDD is transmitted to the boost capacitor CBST through the diode **17**. When the first transistor **12** is turned on, the boost capacitor CBST may be charged by the power supply voltage VDD. The first and second transistors **12** and **13**, the first and second gate drivers **14** and **15**, the level shifter **16**, the diode **17**, and the controller **18** may be implemented with a single chip **11**.

When the first transistor **12** is turned off, the boost capacitor CBST may maintain the boost voltage VBST to be higher, by an amount of the charged voltage, than the switch voltage VSW. That is, the boost capacitor CBST may control the boost voltage VBST for biasing the second gate driver **15** to be greater than the switch voltage VSW, so as to output a level that allows the second gate driver **15** to turn on the second transistor **13**.

However, some issues may occur in the voltage converter **10** illustrated in FIG. **1**. For example, when the voltage converter **10** is powered on, the boost capacitor CBST may not be charged. That is, the boost voltage VBST may be the same as the switch voltage VSW, and the second gate driving signal GD2 of the second gate driver **15** may fail to turn on the second transistor **13**. Accordingly, the voltage converter **10** may cause an abnormal operation.

The voltage converter **10** may enter a power saving mode or a sleep mode or may stop voltage conversion under control of an external device. For example, stopping of the voltage conversion is called a "pulse skip". During the pulse skip, a voltage charged in the boost capacitor CBST may be leaked out. Accordingly, the second gate driving signal GD2 may fail to turn on the second transistor **13**, thereby causing an abnormal operation of the voltage converter **10**.

The first gate driving signal GD1 and the second gate driving signal GD2 of the voltage converter **10** are complementary. When a duty ratio of the second gate driving signal GD2 is close to 100%, the second gate driving signal GD2 has a max duty. If the second gate driving signal GD2 has the max duty, a duty ratio of the first gate driving signal GD1 is close to 0%. That is, when the max duty occurs in the second gate driving signal GD2, the first transistor **12** may not be turned on, and the boost capacitor CBST may not be charged. Accordingly, an abnormal operation that the second gate driving signal GD2 fails to turn on the second transistor **13** may occur in the voltage converter **10**.

FIG. **2** illustrates a voltage converter **100** according to an example embodiment of the inventive concepts, for solving the above-described issues. Referring to FIG. **2**, the voltage converter **100** includes first and second transistors **120** and **130**, first and second gate drivers **140** and **150**, a level shifter **160**, a controller **180**, a regulator **190**, an inductor "L", an output capacitor COUT, and a boost capacitor CBST.

The voltage converter **100** may convert an input voltage VIN of an input node NIN to an output voltage VOUT of an output node NOUT. For example, the voltage converter **100** may be a buck converter that steps down a level of the input voltage VIN to output an output voltage VOUT.

The first and second transistors **120** and **130** may be connected in series between a ground node GND supplied with a ground voltage and the input node NIN. A node between the first and second transistors **120** and **130** may be a switch node NSW. The inductor "L" is connected between the switch node NSW and the output node NOUT. The output capacitor COUT is connected between the output node NOUT and the ground node GND.

The first and second gate drivers **140** and **150** may control the first and second transistors **120** and **130**, respectively, under control of the controller **180**. The first gate driver **140** is biased by a power supply voltage VDD and the ground voltage. The first gate driver **140** may output a first gate driving signal GD1 to control a gate (or a gate voltage) of the first transistor **120**.

The second gate driver **150** is biased by a boost voltage VBST of a boost node NBST and a switch voltage VSW of the switch node NSW. The second gate driver **150** may output a second gate driving signal GD2 to control a gate (or a gate voltage) of the second transistor **130**.

The controller **180** may receive a clock signal CLK, the output voltage VOUT, and the switch voltage VSW. The controller **180** may control the first and second driving signals DRV1 and DRV2 in response to the clock signal CLK, the output voltage VOUT, and/or the switch voltage VSW. For example, the controller **180** may control the first and second driving signals DRV1 and DRV2 such that the output voltage VOUT or the switch voltage VSW is maintained at a target level.

The first driving signal DRV1 of the controller **180** is transmitted to the first gate driver **140**. The second driving signal DRV2 of the controller **180** is transmitted to the second gate driver **150** through the level shifter **160**. The level shifter **160** may translate (e.g., increase) a level of the second driving signal DRV2 to a level defined by the boost voltage VBST and the switch voltage VSW.

The controller **180** may further receive the boost voltage VBST and a pulse skip signal PSK. The controller **180** may generate control signals CP in response to the clock signal CLK, the boost voltage VBST, the switch voltage VSW, and the pulse skip signal PSK. The control signals CP may be transmitted to the regulator **190** to control an operation of the regulator **190**.

The pulse skip signal PSK may be received from an external device (e.g., logic) that controls a pulse skip. If the voltage converter **100** is controlled to operate in a pulse skip mode, the pulse skip signal PSK may be activated (e.g., to a high level). If the voltage converter **100** exits from the pulse skip mode and a given time elapses, the pulse skip signal PSK may be deactivated (for example, a low level).

The regulator **190** may receive the control signals CP from the controller **180**. The regulator **190** may further receive the input voltage VIN and the output voltage VOUT. The regulator **190** may control a voltage of the boost node NBST in response to the control signals CP, the input voltage VIN, and the output voltage VOUT. The boost capacitor CBST is connected between the boost node NBST and the switch node NSW.

The regulator **190** may operate in at least three modes under control of the control signals CP. The at least three modes may include a normal mode, an input voltage pumping mode, and an output voltage pumping mode. In the normal mode, the regulator **190** may output the power supply voltage VDD to the boost node NBST.

In the input voltage pumping mode, the regulator **190** may output a voltage pumped from the input voltage VIN to the boost node NBST. In the output voltage pumping mode, the regulator **190** may output a voltage pumped from the output voltage VOUT to the boost node NBST. An operation of the regulator **190** will be described in detail later.

The first and second transistors **120** and **130**, the first and second gate drivers **140** and **150**, the level shifter **160**, the

controller **180**, and the regulator **190** may be implemented with a single chip **110**. However, components included in the single chip **110** are not limited to the first and second transistors **120** and **130**, the first and second gate drivers **140** and **150**, the level shifter **160**, the controller **180**, and the regulator **190**.

FIG. **3** is a flowchart illustrating an operating method of the voltage converter **100** according to an example embodiment of the inventive concepts. Referring to FIGS. **2** and **3**, in operation S**110**, the voltage converter **100** determines whether the boost voltage VBST is insufficient. For example, when a difference between the boost voltage VBST and the switch voltage VSW is lower than a reference voltage, the voltage converter **100** may determine that the boost voltage VBST is insufficient. As another example, when the voltage converter **100** exits from the pulse skip mode, the voltage converter **100** may determine that the boost voltage VBST is insufficient.

If the boost voltage VBST is insufficient, the voltage converter **100** enters the output voltage pumping mode. In operation S**120**, the voltage converter **100** may control the boost voltage VBST by pumping the output voltage VOUT. For example, the regulator **190** may control the boost voltage VBST to be higher in level, by an amount of the power supply voltage VDD, than the output voltage VOUT.

The boost voltage VBST may be insufficient in two cases. For example, when the voltage converter **100** start to be powered, the boost voltage VBST may be insufficient. When the voltage converter **100** exits from the pulse skip mode, the boost voltage VBST may be insufficient.

In the case where the voltage converter **100** is used in a mobile device including a battery, the output voltage VOUT may be a voltage of the battery. When power is not supplied to the voltage converter **100** or when the voltage converter **100** is in the pulse skip mode, the switch voltage VSW may gradually increase to the output voltage VOUT.

If the boost voltage VBST is pumped from the output voltage VOUT when power starts to be supplied to the voltage converter **100** or when the voltage converter **100** exits from the pulse skip mode, then the boost voltage VBST to be greater than the switch voltage VSW may be secured. Accordingly, an abnormal operation in which the second transistor **130** is not turned on may be prevented or mitigated.

For example, if the boost voltage VBST is sufficient, the voltage converter **100** may enter the normal mode. For example, in the normal mode, the voltage converter **100** may control the boost voltage VBST depending on operation S**150**, which will be described below.

If the boost voltage VBST is sufficient, operation S**130** is performed. In operation S**130**, the voltage converter **100** may determine whether a max duty occurs. For example, when a duty ratio of the second driving signal DRV**2** is greater than a threshold value, the max duty may be determined. If the max duty is determined, the voltage converter **100** may enter an input voltage pumping mode. In the input voltage pumping mode, operation S**140** is performed.

In operation S**140**, the voltage converter **100** may control the boost voltage VBST through pumping from the input voltage VIN. If the max duty occurs, in an operation period of the first and second transistors **120** and **130**, a time when the second transistor **130** is turned on is longer than a time when the first transistor **120** is turned on.

When the second transistor **130** is turned on, the switch voltage VSW is the same as the input voltage VIN. If the boost voltage VBST is pumped from the input voltage VIN when the second transistor **130** is turned on, then the boost voltage VBST to be greater than the switch voltage VSW may be secured. Accordingly, an abnormal operation in which the second transistor **130** is not turned on may be prevented or mitigated.

For example, if the voltage converter **100** does not have the max duty any longer, the voltage converter **100** may enter the normal mode. For example, in the normal mode, the voltage converter **100** may control the boost voltage VBST depending on operation S**150**, which will be described below.

If the boost voltage VBST is sufficient and the max duty is not determined, the voltage converter **100** may operate in the normal mode. In the normal mode, operation S**150** is performed. In operation S**150**, the regulator **190** may output the power supply voltage VDD to the boost node NBST. When the first transistor **120** is turned on, the boost capacitor CBST may be charged to the power supply voltage VDD.

When the second transistor **130** is turned on, the boost voltage VBST may be a voltage that corresponds to a sum of the switch voltage VSW (e.g., the input voltage VIN) and a charging voltage of the boost capacitor CBST. Thus, the boost voltage VBST to be greater than the switch voltage VSW may be secured. Accordingly, an abnormal operation in which the second transistor **130** is not turned on may be prevented or mitigated.

FIG. **4** is a block diagram illustrating the controller **180** according to an example embodiment of the inventive concepts. Referring to FIG. **4**, the controller **180** includes a pulse width modulator **181**, a gate drive voltage generator **183**, a max duty detector **185**, a boost voltage detector **187**, and a regulation signal generator **189**.

The pulse width modulator **181** may receive the clock signal CLK and the output voltage VOUT. The pulse width modulator **181** may output a pulse width modulation signal PWM having a pulse width that varies depending on a level of the output voltage VOUT. The pulse width modulation signal PWM is transmitted to the gate drive voltage generator **183**.

The gate drive voltage generator **183** may output the first and second driving signals DRV**1** and DRV**2** in response to the pulse width modulation signal PWM. For example, the gate drive voltage generator **183** may increase (or decrease) a high level interval or a low level interval of the first driving signal DRV**1** or the second driving signal DRV**2** as a pulse width of the pulse width modulation signal PWM increases.

The first and second driving signals DRV**1** and DRV**2** may be complementary. If the high level interval of the first driving signal DRV**1** increases (or the low level interval thereof decreases), the high level interval of the second driving signal DRV**2** may decrease (or the low level interval thereof may increase). Likewise, if the high level interval of the first driving signal DRV**1** decreases (or the low level interval thereof increases), the high level interval of the second driving signal DRV**2** may increase (or the low level interval thereof may decrease).

The pulse width modulator **181** and the gate drive voltage generator **183** may adjust lengths of high level intervals or low level intervals of the first and second driving signals DRV**1** and DRV**2** depending on a level of the output voltage VOUT. The output voltage VOUT may be controlled to a target level by adjusting the first and second driving signals DRV**1** and DRV**2**.

The max duty detector **185** receives the clock signal CLK and the first driving signal DRV**1**. The max duty detector **185** may determine whether the second driving signal DRV**2** has the max duty in response to the clock signal CLK and the

first driving signal DRV**1**. The max duty detector **185** may output the determination result as a max duty signal DMAX.

If the second driving signal DRV**2** has the max duty, the max duty detector **185** may activate the max duty signal DMAX (or may make the max duty signal DMAX high). If the second driving signal DRV**2** does not have the max duty, the max duty detector **185** may deactivate the max duty signal DMAX (or may make the max duty signal DMAX low).

The boost voltage detector **187** may receive the boost voltage VBST and the switch voltage VSW. The boost voltage detector **187** may determine whether a difference between the boost voltage VBST and the switch voltage VSW is less than a reference voltage. If the difference is less than the reference voltage, the boost voltage detector **187** may activate a boost voltage signal DVBST (or may make the boost voltage signal DVBST low). If the difference is not less than the reference voltage, the boost voltage detector **187** may deactivate the boost voltage signal DVBST (or may make the boost voltage signal DVBST high).

The regulation signal generator **189** may receive the clock signal CLK, the max duty signal DMAX, the boost voltage signal DVBST, the pulse skip signal PSK, and the second driving signal DRV**2**. The regulation signal generator **189** may control first to fourth control signals CP_S**1** to CP_S**4** in response to the clock signal CLK, the max duty signal DMAX, the boost voltage signal DVBST, the pulse skip signal PSK, and the second driving signal DRV**2**.

The first to fourth control signals CP_S**1** to CP_S**4** may be transmitted to the regulator **190**. The regulation signal generator **189** may allow the regulator **190** to operate in one of at least three modes including the input voltage pumping mode, the output voltage pumping mode, and the normal mode, by using the first to fourth control signals CP_S**1** to CP_S**4**.

FIG. **5** illustrates an example of the max duty detector **185** according to an example embodiment of the inventive concepts. The max duty detector **185** may determine the max duty of the second driving signal DRV**2** in response to the clock signal CLK and the first driving signal DRV**1**. Referring to FIGS. **4** and **5**, the max duty detector **185** includes first to third blocks **185***a*, **185***b*, and **185***c* and a flip-flop **185***d*.

In an example embodiment, the max duty detector **185** may detect the max duty of the second driving signal DRV**2** from the first driving signal DRV**1** based on a complementary characteristic of the first and second driving signals DRV**1** and DRV**2**. However, the scope and spirit of the inventive concepts are not limited thereto. In some example embodiments, the max duty detector **185** may detect the max duty directly from the second driving signal DRV**2**.

The first block **185***a* may periodically output a max duty detection pulse DMD for detecting the max duty of the second driving signal DRV**2**. The first block **185***a* may include a first delay **185***a***1**, a first inverter **185***a***2**, and a first AND element **185***a***3**.

The first delay **185***a***1** may delay the clock signal CLK to output a delayed clock signal CLKP. The first inverter **185***a***2** may invert the clock signal CLK to output an inverted clock signal CLKB. The first AND element **185***a***3** may perform an AND operation on the delayed clock signal CLKP and the inverted clock signal CLKB to output the max duty detection pulse DMD.

The second block **185***b* may output a reset signal RST representing that the second driving signal DRV**2** does not have the max duty. The second block **185***b* may include a second AND element **185***b***1**, a second delay **185***b***2**, and a third AND element **185***b***3**. The second AND element **185***b***1** may output the result of performing an AND operation on the max duty detection pulse DMD and the first driving signal DRV**1** as a first internal signal A**1**.

The second delay **185***b***2** may delay the first internal signal A**1** to output a second internal signal A**2**. The third AND element **185***b***3** may output the result of performing an AND operation on the first and second internal signals A**1** and A**2** as the reset signal RST. The reset signal RST may be transmitted to a reset input of the flip-flop **185***d*.

In an example embodiment, the second delay **185***b***2** and the third AND element **185***b***3** may prevent or mitigate the reset signal RST from fluctuating when a level of the max duty detection pulse DMD or the first driving signal DRV**1** is converted. In an anti-fluctuation system, the output of the second AND element **185***b***1** may be used as the reset signal RST.

The third block **185***c* may output a set signal SET representing that the second driving signal DRV**2** has the max duty. The set signal SET may be transmitted to a set input of the flip-flop **185***d*. The third block **185***c* may include a second inverter **185***c***1**, a fourth AND element **185***c***2**, a third delay **185***c***3**, and a fifth AND element **185***c***4**.

The second inverter **185***c***1** may invert the first driving signal DRV**1** to output an inverted first driving signal DRV**1**B. The fourth AND element **185***c***2** may output the result of performing an AND operation on the max duty detection pulse DMD and the inverted first driving signal DRV**1**B as a third internal signal A**3**.

The third delay **185***c***3** may delay the third internal signal A**3** to output a fourth internal signal A**4**. The fifth AND element **185***c***4** may output the result of performing an AND operation on the third and fourth internal signals A**3** and A**4** as the set signal SET. The output of the flip-flop **185***d* may be set in response to the set signal SET and may be reset in response to the reset signal RST. The output of the flip-flop **185***d* may be the max duty signal DMAX. The flip-flop **185***d* may include a set-reset flip-flop (SRFF).

In an example embodiment, the third delay **185***c***3** and the fifth AND element **185***c***4** may prevent or mitigate the set signal SET from fluctuating when a level of the max duty detection pulse DMD or the first driving signal DRV**1** is converted. In an anti-fluctuation system, the output of the fourth AND element **185***c***2** may be used as the set signal SET.

FIG. **6** illustrates an example in which the max duty detection signal DMD is generated from the clock signal CLK, the inverted clock signal CLKB, and the delayed clock signal CLKP. Referring to FIGS. **2**, **5**, and **6**, the inverted clock signal CLKB may have an inverted waveform of the clock signal CLK. The delayed clock signal CLKP may have a waveform of the inverted clock signal CLKB delayed as much as a delay time DT.

The max duty detection pulse DMD may be generated through a logical AND of the inverted clock signal CLKB and the delayed clock signal CLKP. Accordingly, the max duty detection pulse DMD has high levels in intervals in which the inverted clock signal CLKB and the delayed clock signal CLKP all have a high level.

The max duty detection pulse DMD has low levels in intervals in which at least one of the inverted clock signal CLKB and the delayed clock signal CLKP has a low level. The max duty detection pulse DMD is illustrated in FIG. **6** as first to fifth pulses P**1** to P**5** having a high level periodically. In an example embodiment, a delay amount of the first delay **185***a***1** may be adjusted to set a pulse width of the max duty detection pulse DMD to a desired value.

FIG. **7** illustrates an example in which the second block **185***b* generates the reset signal RST as a pulse width of the first driving signal DRV**1** changes. Referring to FIGS. **2**, **5**, and **7**, the first to fifth pulses P**1** to P**5** are illustrated as the max duty detection pulse DMD. The pulse width of the first driving signal DRV**1** may gradually decrease. That is, the pulse width of the second driving signal DRV**2** may gradually increase.

For example, the pulse width of the first driving signal DRV**1** may gradually decrease with regard to the first to third pulses P**1** to P**3**. A pulse of the first driving signal DRV**1** may not be generated with regard to the fourth and fifth pulses P**4** and P**5**. The second driving signal DRV**2** may have the max duty with regard to the fourth and fifth pulses P**4** and P**5**.

The internal signal A**1** may be generated by performing an AND operation on the max duty detection pulse DMD and the first driving signal DRV**1**. Accordingly, when the max duty detection pulse DMD and the first driving signal DRV**1** all have a high level, the first internal signal A**1** has a high level. When at least one of the max duty detection pulse DMD and the first driving signal DRV**1** has a low level, the first internal signal A**1** has a low level.

The second internal signal A**2** may be a signal generated by delaying the first internal signal A**1**. The reset signal RST is generated by performing an AND operation on the first and second internal signals A**1** and A**2**. Accordingly, when the first and second internal signals A**1** and A**2** all have a high level, the reset signal RST may have a high level.

With regard to the first and second pulses P**1** and P**2**, the first and second internal signals A**1** and A**2** have an interval in which high levels thereof overlap with each other. Accordingly, the second block **185***b* may output (or activate) the reset signal RST with regard to the first and second pulses P**1** and P**2**. That is, with regard to the first and second pulses P**1** and P**2**, the second block **185***b* may determine that the second driving signal DRV**2** does not have the max duty.

The max duty signal DMAX, which is the output of the flip-flop **185***d*, may be periodically reset in response to the activated reset signal RST. For example, with regard to the first and second pulses P**1** and P**2**, the flip-flop **185***d* may reset the max duty signal DMAX to a low level.

With regard to the third to fifth pulses P**3** to A**5**, the first and second internal signals A**1** and A**2** do not have an interval in which high levels thereof overlap with each other. Accordingly, with regard to the third to fifth pulses P**3** to P**5**, the second block **185***b* may not output (or activate) the reset signal RST. For example, the second block **185***b* may not determine that the second driving signal DRV**2** does not have the max duty.

FIG. **8** illustrates an example in which the third block **185***c* generates the set signal SET as a pulse width of the first driving signal DRV**1** changes. Referring to FIGS. **2**, **5**, and **8**, the first to fifth pulses P**1** to P**5** are illustrated as the max duty detection pulse DMD. The pulse width of the first driving signal DRV**1** may gradually decrease. That is, the pulse width of the second driving signal DRV**2** may gradually increase.

The inverted first driving signal DRV may be an inverted waveform of the first driving signal DRV**1**. The third internal signal A**3** may be generated by performing an AND operation on the max duty detection pulse DMD and the inverted first driving signal DRV**1**B. Accordingly, the third internal signal A**3** has high levels in intervals where the max duty detection pulse DMD and the inverted first driving signal DRV**1**B all have high levels.

The fourth internal signal A**4** may be a signal generated by delaying the third internal signal A**3**. The set signal SET is generated by performing an AND operation on the third and fourth internal signals A**3** and A**4**. Accordingly, the set signal SET may have high levels in intervals where the third and fourth internal signals A**3** and A**4** all have high levels.

With regard to the first and second pulses P**1** and P**2**, the third internal signal A**3** does not have a high level. Accordingly, with regard to the first and second pulses P**1** and P**2**, the third block **185***c* may not output (or activate) the set signal SET. With regard to the third to fifth pulses P**3** to P**5**, the third internal signal A**3** has high levels.

With regard to the third to fifth pulses P**3** to P**5**, the third and fourth internal signals A**3** and A**4** have intervals in which high levels thereof overlap with each other. Accordingly, with regard to the third to fifth pulses P**3** to P**5**, the third block **185***c* may output (or activate) the set signal SET representing that the second driving signal DRV**2** has the max duty.

As the third block **185***c* activates the set signal SET, the flip-flop **185***d* may activate the max duty signal DMAX to a high level. For example, with regard to the third to fifth pulses P**3** to P**5**, the third block **185***c* may periodically set the max duty signal DMAX of the flip-flop **185***d* to a high level.

The inventive concepts are not limited to the case that the max duty detector **185** activates the max duty signal DMAX only when the second driving signal DRV**2** completely has the max duty. In some example embodiments, the max duty detector **185** may activate the max duty signal DMAX when the duty ratio of the second driving signal DRV**2** is greater than a threshold value. The threshold value may be determined by parameters of the voltage converter **100** that have high levels in intervals where the third and fourth internal signals A**3** and A**4** overlap with each other.

As described above, if the duty ratio of the second driving signal DRV**2** (or a duty ratio of a low level of the first driving signal DRV**1**) is greater than the threshold value, the max duty detector **185** may activate the max duty signal DMAX to a high level. If the duty ratio of the second driving signal DRV**2** is not greater than the threshold value, the max duty detector **185** may deactivate the max duty signal DMAX to a low level. Accordingly, the max duty detector **185** may detect the max duty of the second driving signal DRV**2**.

FIG. **9** illustrates an example of the boost voltage detector **187** according to an example embodiment of the inventive concepts. Referring to FIGS. **5** and **9**, the boost voltage detector **187** includes first to fourth resistors **187***a* to **187***d*, a first comparator **187***e*, a fifth resistor **187***f*, and a second comparator **187***g*.

The first and second resistors **187***a* and **187***b* may divide the boost voltage VBST. A first voltage V**1**, which is the result obtained by dividing the boost voltage VBST by the first and second resistors **187***a* and **187***b*, may be transmitted to a positive input of the first comparator **187***e*. The third and fourth resistors **187***c* and **187***d* may divide the switch voltage VSW. A second voltage V**2**, which is the result obtained by dividing the switch voltage VSW by the third and fourth resistors **187***c* and **187***d*, may be transmitted to a negative input of the first comparator **187***e*.

In an example embodiment, a division ratio of the first and second resistors **187***a* and **187***b* and a division ratio of the third and fourth resistors **187***c* and **187***d* may be the same. That is, a difference between the first and second voltages V**1** and V**2** may be proportional to a difference between the boost voltage VBST and the switch voltage VSW.

The first comparator **187***e* may compare the first voltage V**1** and the second voltage V**2**. The first comparator **187***e*

may output a third voltage V3 that is proportional to a difference between the first voltage V1 and the second voltage V2. The third voltage V3 may be proportional to a difference between the boost voltage VBST and the switch voltage VSW. The third voltage V3 may be transmitted to a positive input of the second comparator **187***g*.

The fifth resistor **187***f* may allow the third voltage V3 to be generated at an output of the first comparator **187***e*. The second comparator **187***g* may compare the third voltage V3 and a reference voltage VREF. If the third voltage V3 is greater than the reference voltage VREF, that is, if a difference between the boost voltage VBST and the switch voltage VSW (or a voltage proportional to the difference) is greater than the reference voltage VREF, the second comparator **187***g* may deactivate the boost voltage signal DVBST (or may make the boost voltage signal DVBST high).

If the third voltage V3 is not greater than the reference voltage VREF, that is, if the difference between the boost voltage VBST and the switch voltage VSW (or the voltage proportional to the difference) is not greater than the reference voltage VREF, the second comparator **187***g* may activate the boost voltage signal DVBST (or may make the boost voltage signal DVBST low).

If the boost voltage signal DVBST is deactivated (e.g., to a high level), the boost voltage VBST is determined as being sufficiently greater than the switch voltage VSW. For example, the boost voltage VBST is determined to be sufficient if the second gate driver **150** drives the second transistor **130** to be turned on.

If the boost voltage signal DVBST is activated (e.g., to a low level), the boost voltage VBST is determined as being not sufficiently greater than the switch voltage VSW. For example, the boost voltage VBST is determined to be insufficient if the second gate driver **150** fails to drive the second transistor **130** to be turned on.

FIG. **10** illustrates an example of the regulation signal generator **189** according to an example embodiment of the inventive concepts. Referring to FIGS. **2**, **5**, and **10**, the regulation signal generator **189** includes a status determination block **189***a* and a regulation signal generation block **189***b*. The status determination block **189***a* may determine the status of the voltage converter **100** in response to the max duty signal DMAX, the boost voltage signal DVBST, and the pulse skip signal PSK.

The status determination block **189***a* may control first and second signals S1 and S2 based on the determined status. For example, if a difference between the boost voltage VBST and the switch voltage VSW is less than a reference voltage or if it is determined that the voltage converter **100** exist from the pulse skip mode, and thus, the boost voltage VBST is insufficient, the status determination block **189***a* may activate the first signal S1 to a high level.

In the case where the boost voltage VBST is sufficient, the status determination block **189***a* may deactivate the first signal S1 to a low level. If the boost voltage VBST is sufficient, but that the second driving signal DRV2 is determined to have the max duty (refer to operation S130 of FIG. **3**), the status determination block **189***a* may activate the second signal S2 to a high level.

The status determination block **189***a* includes a first status determination inverter **189***a*_1, a first status determination AND element **189***a*_2, a status determination NOR element **189***a*_3, a second status determination inverter **189***a*_4, and a second status determination AND element **189***a*_5. The first status determination inverter **189***a*_1 may invert and output the boost voltage signal DVBST.

The first status determination AND element **189***a*_2 may output a logical product of the boost voltage signal DVBST and the pulse skip signal PSK. The status determination NOR element **189***a*_3 may output logical NOR of an output of the first status determination inverter **189***a*_1 and an output of the first status determination AND element **189***a*_2.

The second status determination inverter **189***a*_4 may invert the output of the status determination NOR element **189***a*_3 to output the first signal S1. The second status determination AND element **189***a*_5 may output a logical product of the max duty signal DMAX and the output of the status determination NOR element **189***a*_3 to output the second signal S2.

If the boost voltage signal DVBST has a low level (e.g., the boost voltage VBST is not sufficiently high) or the pulse skip signal PSK has a high level (e.g., if the voltage converter **100** exits from the pulse skip mode), the status determination block **189***a* may determine that the boost voltage VBST is insufficient (refer to operation S110 of FIG. **3**). The first signal S1 may have values of Table 1 depending on the boost voltage signal DVBST and the pulse skip signal PSK.

TABLE 1

Boost voltage signal (DVBST)	Pulse skip signal (PSK)	First signal (S1)
1 (sufficient)	1 (pulse skip mode)	1 (activation)
1 (sufficient)	0	0 (deactivation)
0 (insufficient)	1 (pulse skip mode)	1 (activation)
0 (insufficient)	0	1 (activation)

If the boost voltage VBST is sufficient, but the second driving signal DRV2 has the max duty, the status determination block **189***a* may activate the second signal S2. The second signal S2 may have values of Table 2 depending on the first signal S1 and the max duty signal DMAX.

TABLE 2

First signal (S1)	Max duty signal (DMAX)	Second signal (S2)
0 (deactivation)	1 (max duty)	1
0 (deactivation)	0	0
1 (activation)	1 (max duty)	0
1 (activation)	0	0

The regulation signal generation block **189***b* may control the first to fourth control signals CP_S1 to CP_S4 in response to the first and second signals S1 and S2, the clock signal CLK, and the second driving signal DRV2. The regulation signal generation block **189***b* includes a first regulation inverter **189***b*_1, a regulation NAND element **189***b*_2, a second regulation inverter **189***b*_3, a first regulation AND element **189***b*_4, a regulation NOR element **189***b*_5, a second regulation AND element **189***b*_6, a regulation OR element **189***b*_7, a third regulation inverter **189***b*_8, a regulation NOR element **189***b*_9, and a fourth regulation inverter **189***b*_10.

The first regulation inverter **189***b*_1 may invert the clock signal CLK to output the inverted clock signal CLKB. The regulation NAND element **189***b*_2 may output the result of performing a NAND operation on the second driving signal DRV2, the inverted clock signal CLKB, and the second signal S2 as a third signal S3.

The second regulation inverter **189***b*_**3** may invert the third signal S**3** to output the second control signal CP_S**2**. The first regulation AND element **189***b*_**4** may output the result of performing an AND operation on the third signal S**3**, the clock signal CLK, and the second signal S**2** as a fourth signal S**4**. The regulation NOR element **189***b*_**5** may output the result of performing a NOR operation on the second signal S**2** and the first signal S**1** as a fifth signal S**5**.

The second regulation AND element **189***b*_**6** may output the result of performing an AND operation on the first signal S**1** and the clock signal CLK as a sixth signal S**6**. The regulation OR element **189***b*_**7** may output the result of performing an OR operation on the fourth signal S**4**, the fifth signal S**5**, and the sixth signal S**6** as the first control signal CP_S**1**.

The third regulation inverter **189***b*_**8** may invert the first signal S**1** to output a seventh signal S**7**. The regulation NOR element **189***b*_**9** may output the result of performing a NOR operation on the seventh signal S**7** and the sixth signal S**6** as the fourth control signal CP_S**4**. The fourth regulation inverter **189***b*_**10** may invert the first signal S**1** to output the third control signal CP_S**3**. The first to fourth control signals CP_S**1** to CP_S**4** may be transmitted to the regulator **190**.

FIG. **11** illustrates an example of the regulator **190** according to an example embodiment of the inventive concepts. Referring to FIGS. **2** and **11**, the regulator **190** includes first to fourth transistors **191***a* to **194***a*, first to fourth drivers **191***b* to **194***b*, a level shifter **192***c*, first to third diodes **195***a* to **195***c*, and a capacitor **196**.

The first and second transistors **191***a* and **192***a* are connected in series between the ground node GND and the input node NIN. A node between the first and second transistors **191***a* and **192***a* may be a low node LN. A gate voltage of the first transistor **191***a* is controlled by the first driver **191***b*. A gate voltage of the second transistor **192***a* is controlled by the second driver **192***b*.

The third and fourth transistors **193***a* and **194***a* are connected in series between the ground node GND and the output node NOUT. A gate voltage of the third transistor **193***a* is controlled by the third driver **193***b*. A gate voltage of the fourth transistor **194***a* is controlled by the fourth driver **194***b*.

A cathode of the first diode **195***a* is connected to the low node LN. An anode of the first diode **195***a* is connected to a node between the third and fourth transistors **193***a* and **194***a*. The second and third diodes **195***b* and **195***c* are connected in series between a power node, to which the power supply voltage VDD is supplied, and the boost node NBST. A node between the second and third diodes **195***b* and **195***c* may be a high node HN.

The first driver **191***b* is biased by the power supply voltage VDD and the ground voltage of the ground node GND. The first driver **191***b* may operate in response to the first control signal CP_S**1**. The second driver **192***b* is biased by a high boost voltage VBST_H of the high node HN and a low boost voltage VBST_L of the low node LN.

The second driver **192***b* may be controlled according to a signal that is generated by translating a level of the second control signal CP_S**2** at the level shifter **192***c*. For example, the level shifter **192***c* may translate (e.g., increase) a level of the second control signal CP_S**2** to a level defined by the high boost voltage VBST_H and the low boost voltage VBST_L.

The third driver **193***b* is biased by the power supply voltage VDD and the ground voltage. The third driver **193***b* may be controlled by the third control signal CP_S**3**. The fourth driver **194***b* is biased by the power supply voltage VDD and the ground voltage. The fourth driver **194***b* is controlled by the fourth control signal CP_S**4**. The capacitor **196** is connected between the high node HN and the low node LN.

FIG. **12** illustrates an example of signals associated with the regulation signal generation block **189***b* when the first signal S**1** and the second signal S**2** are deactivated. That is, FIG. **12** illustrates signals when the voltage converter **100** is at a normal state. In other words, FIG. **12** illustrates signals when a difference between the boost voltage and the switch voltage is not less than a reference voltage, when the voltage converter does not exit from a pulse skip mode, and when a duty ratio of the gate voltage of the second transistor is not greater than a threshold value. Referring to FIGS. **2**, **10**, and **12**, the clock signal CLK and the second driving signal DRV**2** are illustrated.

The third signal S**3** has a low level when the second signal S**2** is at a high level (e.g., is activated), the clock signal CLK is at a low level, and the second driving signal DRV**2** is at a high level. Because FIG. **12** assumes that the second signal S**2** is at a low level (e.g., is deactivated), the third signal S**3** is fixed to a high level.

The fourth signal S**4** has a high level when the third signal S**3**, the clock signal CLK, and the second signal S**2** all are at a high level. Because FIG. **12** assumes that the second signal S**2** is at a low level (e.g., is deactivated), the fourth signal S**4** is fixed to a low level. The fifth signal S**5** has a high level when both the first and second signals S**1** and S**2** are at a low level. Because FIG. **12** assumes that both the first signal S**1** and the second signal S**2** are at a low level, the fifth signal S**5** is fixed to a high level.

The sixth signal S**6** has a high level when both the first signal S**1** and the clock signal CLK are at a high level. Because FIG. **12** assumes that the first signal S**1** is at a low level, the sixth signal S**6** is fixed to a low level. The first control signal CP_S**1** has a low level only when all the fourth to sixth signals S**4** to S**6** are at a low level. Because FIG. **12** assumes that the fifth signal S**5** is at a high level, the first control signal CP_S**1** is fixed to a high level.

The second control signal CP_S**2** may be an inverted version of the third signal S**3**. Because the third signal S**3** is at a high level, the second control signal CP_S**2** is fixed to a low level. The third control signal CP_S**3** may be an inverted version of the first signal S**1**. Because FIG. **12** assumes that the first signal S**1** is at a low level, the third control signal CP_S**3** is fixed to a high level.

The fourth control signal CP_S**4** has a high level only when both the sixth and seventh signals S**6** and S**7** are at a low level. The sixth signal S**6** may be an inverted version of the first signal S**1**. Accordingly, the fourth control signal CP_S**4** has a high level only when the first signal S**1** is at a high level and the sixth signal S**6** is at a low level. Because the first signal S**1** has a low level, the fourth control signal CP_S**4** is fixed to a low level.

FIG. **13** illustrates how the regulator **190** is controlled by signals of FIG. **12**. Referring to FIGS. **2**, **12**, and **13**, because the second and fourth control signals CP_S**2** and CP_S**4** are fixed to a low level, the second and fourth transistors **192***a* and **194***a* maintain a turn-off state. Because the first and third control signals CP_S**1** and CPS_**3** are fixed to a high level, the first and third transistors **191***a* and **193***a* maintain a turn-on state.

A voltage of the low node LN is a ground voltage. The power supply voltage VDD is supplied to the boost node NBST through the second and third diodes **195***b* and **195***c*.

While the first transistor **120** is turned on, the boost capacitor CBST is charged by the power supply voltage VDD output from the regulator **190**.

At timing when the first transistor **120** is turned off and the second transistor **130** is turned on, the boost voltage VBST may be greater than the switch voltage VSW by a voltage (e.g., the power supply voltage VDD) charged in the boost capacitor CBST. Accordingly, the second gate driver **150** may turn on the second transistor **130** based on the boost voltage VBST.

FIG. **14** illustrates an example of signals associated with the regulation signal generation block **189***b* when the first signal S**1** is activated and the second signal S**2** are deactivated. That is, FIG. **14** illustrates signals that are controlled to the output voltage pumping mode due to the insufficiency of the boost voltage VBST in the voltage converter **100**. Referring to FIGS. **2**, **10**, and **14**, the clock signal CLK and the second driving signal DRV**2** are illustrated.

The third signal S**3** has a low level when the second signal S**2** is at a high level (e.g., is activated), the clock signal CLK is at a low level, and the second driving signal DRV**2** is at a high level. Because FIG. **14** assumes that the second signal S**2** is at a low level (e.g., is deactivated), the third signal S**3** is fixed to a high level.

The fourth signal S**4** has a high level when the third signal S**3**, the clock signal CLK, and the second signal S**2** all are at a high level. Because FIG. **14** assumes that the second signal S**2** is at a low level (e.g., is deactivated), the fourth signal S**4** is fixed to a low level. The fifth signal S**5** has a high level when both the first signal S**1** and the second signal S**2** are at a low level. Because FIG. **14** assumes that the first signal S**1** is at a high level, the fifth signal S**5** is fixed to a low level.

The sixth signal S**6** has a high level when both the first signal S**1** and the clock signal CLK are at a high level. Because FIG. **14** assumes that the first signal S**1** is at a high level, the sixth signal S**6** may have the same waveform as the clock signal CLK. The first control signal CP_S**1** has a low level only when all the fourth to sixth signals S**4** to S**6** are at a low level. In FIG. **14**, because the fourth and fifth signals S**4** and S**5** are fixed to a low level, the first control signal CP_S**1** has the same waveform as the sixth signal S**6**.

The second control signal CP_S**2** may be an inverted version of the third signal S**3**. In FIG. **14**, because the third signal S**3** is at a high level, the second control signal CP_S**2** is fixed to a low level. The third control signal CP_S**3** may be an inverted version of the first signal S**1**. Because FIG. **14** assumes that the first signal S**1** is at a high level, the third control signal CP_S**3** is fixed to a low level.

The fourth control signal CP_S**4** has a high level only when the first signal S**1** is at a high level and the sixth signal S**6** is at a low level. Because FIG. **14** assumes that the first signal S**1** is at a high level and the sixth signal S**6** switches between a high level and a low level, the fourth control signal CP_S**4** has an inverted waveform of the sixth signal S**6**. The fourth control signal CP_S**4** may be complementary to the first control signal CP_S**1**.

FIG. **15** illustrates how the regulator **190** is controlled by signals of FIG. **14**. Referring to FIGS. **2**, **14**, and **15**, because the second and third control signals CP_S**2** and CP_S**3** are fixed to a low level, the second and third transistors **192***a* and **193***a* maintain a turn-off state. As illustrated by an arrow, each of the first and fourth control signals CP_S**1** and CP_S**4** may switch between a high level and a low level and may transmit a voltage pumped from the output voltage VOUT to the boost node NBST.

When the first transistor **191***a* is turned on and the fourth transistor **194***a* is turned off, the capacitor **196** is charged with the power supply voltage VDD transmitted through the second diode **195***b*. When the first transistor **191***a* is turned off and the fourth transistor **194***a* is turned on, a voltage of the high node HN increases to a voltage corresponding to a sum of the output voltage VOUT and a voltage (e.g., the power supply voltage VDD) charged in the capacitor **196**. That is, a voltage pumped from the output voltage VOUT by an amount as much as the power supply voltage VDD is transmitted to the boost node NBST.

FIG. **16** illustrates an example of signals associated with the regulation signal generation block **189***b* when the first signal S**1** is deactivated and the second signal S**2** are activated. That is, FIG. **16** illustrates signals that are controlled to the input voltage pumping mode when the max duty occurs in the voltage converter **100**. Referring to FIGS. **2**, **10**, and **16**, the clock signal CLK and the second driving signal DRV**2** are illustrated.

The third signal S**3** has a low level when the second signal S**2** is at a high level (e.g., is activated), the clock signal CLK is at a low level, and the second driving signal DRV**2** is at a high level. Because FIG. **16** assumes that the second signal S**2** is at a high level (e.g., is activated), the third signal S**3** has low levels in intervals where the clock signal CLK is at a low level and the second driving signal DRV**2** is at a high level. In the remaining intervals, the third signal S**3** has a high level.

The fourth signal S**4** has a high level when the third signal S**3**, the clock signal CLK, and the second signal S**2** all are at a high level. Because FIG. **16** assumes that the second signal S**2** is at a high level (e.g., is activated), the fourth signal S**4** has high levels in intervals where the third signal S**3** and the clock signal CLK are at a high level. In the remaining intervals, the fourth signal S**4** has low levels.

The fifth signal S**5** has a high level when the first and second signals S**1** and S**2** all are at a low level. Because FIG. **16** assumes that the second signal S**2** is at a high level, the fifth signal S**5** is fixed to a low level. The sixth signal S**6** has a high level when the first signal S**1** and the clock signal CLK all are at a high level. Because FIG. **16** assumes that the first signal S**1** is at a low level, the sixth signal S**6** is fixed to a low level.

The first control signal CP_S**1** has a low level only when the fourth to sixth signals S**4** to S**6** all are at a low level. Because FIG. **16** assumes that the fifth and sixth signals S**5** and S**6** are fixed to a low level, the first control signal CP_S**1** has the same waveform as the fourth signal S**4**. The second control signal CP_S**2** may be an inverted version of the third signal S**3**.

The third control signal CP_S**3** may be an inverted version of the first signal S**1**. Because FIG. **16** assumes that the first signal S**1** is at a low level, the third control signal CP_S**3** is fixed to a high level. The fourth control signal CP_S**4** has a high level only when the first signal S**1** is at a high level and the sixth signal S**6** is at a low level. Because FIG. **16** assumes that the first signal S**1** is at a low level, the fourth control signal CP_S**4** is fixed to a low level.

The first and second control signals CP_S**1** and CP_S**2** may be complementary in intervals where the second driving signal DRV**2** is at a high level. For example, in intervals where the second driving signal DRV**2** is at a high level, if the first control signal CP_S**1** is at a high level, the second control signal CP_S**2** may be at a low level.

In intervals where the second driving signal DRV**2** is at a high level, if the first control signal CP_S**1** is at a low level, the second control signal CP_S**2** may be at a high level. The

first and second control signals CP_S1 and CP_S2 may have low levels in intervals where the second driving signal DRV2 is at a low level.

FIG. **17** illustrates how the regulator **190** is controlled by signals of FIG. **16**. Referring to FIGS. **2**, **16**, and **17**, since the fourth control signal CP_S4 is fixed to a low level, the fourth transistor **194***a* maintains a turn-off state. Because the third control signal CP_S3 is fixed to a high level, the third transistor **193***a* maintains a turn-on state.

As illustrated by an arrow, each of the first and second control signals CP_S1 and CP_S2 may switch between a high level and a low level in intervals where the second driving signal DRV2 is at a high level and may transmit a voltage pumped from the input voltage VIN to the boost node NBST. When the first transistor **191***a* is turned on and the second transistor **192***a* is turned off, the capacitor **196** is charged with the power supply voltage VDD transmitted through the second diode **195***b*.

When the first transistor **191***a* is turned off and the second transistor **192***a* is turned on, a voltage of the high node HN increases to a voltage corresponding to a sum of a voltage of the high node HN and a voltage (e.g., the power supply voltage VDD) charged in the capacitor **196**. That is, a voltage pumped from the input voltage VIN by an amount as much as the power supply voltage VDD is transmitted to the boost node NBST.

FIG. **18** illustrates a voltage converter **200** according to an example embodiment of the inventive concepts. Referring to FIG. **18**, the voltage converter **200** includes first and second transistors **220** and **230**, first and second gate drivers **240** and f, a level shifter **260**, a controller **280**, a regulator **290**, an inductor "L", an input capacitor CIN, an output capacitor COUT, and a boost capacitor CBST.

The voltage converter **200** may convert an input voltage VIN of an input node NIN to an output voltage VOUT of an output node NOUT. For example, the voltage converter **200** may be a boost converter that steps up a level of the input voltage VIN to output the output voltage VOUT.

The first and second transistors **220** and **230** may be connected in series between a ground node GND supplied with a ground voltage and the output node NOUT. A node between the first and second input transistors **120** and **130** may be a switch node NSW. The inductor "L" is connected between the switch node NSW and the input node NIN. The input capacitor CIN is connected between the input node NIN and the ground node GND.

The boost capacitor CBST is connected between the switch node NSW and the boost node NBST. The output capacitor COUT is connected between the output node NOUT and the ground node GND. The first and second transistors **220** and **230**, the first and second gate drivers **240** and **250**, the level shifter **260**, the controller **280**, and the regulator **290** are the same as described with reference to FIG. **2**, and thus, a description thereof will not be repeated here.

The voltage converter **200** may enter the input voltage pumping mode when the boost voltage VBST is insufficient. The voltage converter **200** may enter the output voltage pumping mode when the second driving signal DRV2 has the max duty. The regulator **290** may have the same structure of FIG. **11** except that the input node NIN and the output node NOUT are exchanged. The controller **280** may have the same structure as described with reference to FIGS. **4** to **10**.

According to an example embodiment of the inventive concepts, the voltage converter **100** or **200** in which switching transistors may be implemented with NMOS transistors. Because PMOS transistors are not used, the size of the voltage converter **100** or **200** may be reduced. By configuring the regulator **190** or **290** to operate in at least three modes including the normal mode, the output voltage pumping mode, and the input voltage pumping mode, the second transistor **130** or **230** can be securely turned on at all times. Accordingly, the voltage converter **100** or **200** with improved reliability can be implemented.

FIG. **19** illustrates a voltage converter **300** according to another example embodiment of the inventive concepts. Referring to FIG. **19**, the voltage converter **300** includes a first transistor **321**, a second transistor **322**, a third transistor **323** and a fourth transistor connected in series between an input node NIN to which an input voltage VIN is applied.

The voltage converter **300** further includes a first gate driver **351**, a second gate driver **352**, a third gate driver **353** and a fourth gate driver **354**. The first gate driver **351** may output a first gate driving signal GD1 to turn on or turn off the first transistor **351**. The first gate driver **351** is biased with a first power supply voltage VDD1 and a first voltage V1 of a first node N1 between the first transistor **321** and the second transistor **322**. The first gate driver **351** may output the first power supply voltage VDD1 as a high level and output the first voltage V1 as a low level.

The second gate driver **352** may output a second gate driving signal GD2 to turn on or turn off the second transistor **322**. The second gate driver **352** is biased with a second power supply voltage VDD2 and a second voltage V2 of a second node N2 between the second transistor **322** and the third transistor **323**. The second gate driver **352** may output the second power supply voltage VDD2 as a high level and output the second voltage V2 as a low level.

The third gate driver **353** may output a third gate driving signal GD3 to turn on or turn off the third transistor **323**. The third gate driver **353** is biased with a third power supply voltage VDD3 and a third voltage V3 of a third node N3 between the third transistor **323** and the fourth transistor **324**. The third gate driver **353** may output the third power supply voltage VDD3 as a high level and output the third voltage V3 as a low level.

The fourth gate driver **354** may output a fourth gate driving signal GD4 to turn on or turn off the fourth transistor **324**. The fourth gate driver **354** is biased with a fourth power supply voltage VDD4 and a ground voltage GND of a ground node. The fourth gate driver **354** may output the fourth power supply voltage VDD4 as a high level and output the ground voltage GND as a low level.

The voltage converter **300** further includes a first level shifter **361**, a second level shifter **362**, a third level shifter **363** and a fourth level shifter **364**. The first level shifter **361** may receive a first driving signal DRV1 belong to a first voltage domain between a common power supply voltage (VDD) and the ground voltage GND, shift the first voltage domain to a second voltage domain between the first power supply voltage VDD1 and the first voltage V1, and output the shifted signal to the first gate driver **351**.

The first voltage domain may have the common power supply voltage (VDD) as a high level and the ground voltage GND as a low level. The second voltage domain may have the first power supply voltage VDD1 as a high level and the first voltage V1 as a low level.

The second level shifter **362** may receive a second driving signal DRV2 belong to a second voltage domain between the common power supply voltage (VDD) and the ground voltage GND, shift the second voltage domain to a fourth voltage domain between the second power supply voltage VDD2 and the second voltage V2, and output the shifted signal to the second gate driver **352**. The fourth voltage

domain may have the second power supply voltage VDD2 as a high level and the second voltage V2 as a low level.

The third level shifter **363** may receive a third driving signal DRV3 belong to a fifth voltage domain between the common power supply voltage (VDD) and the ground voltage GND, shift the fifth voltage domain to a sixth voltage domain between the third power supply voltage VDD3 and the third voltage V3, and output the shifted signal to the third gate driver **353**. The sixth voltage domain may have the third power supply voltage VDD3 as a high level and the third voltage V3 as a low level.

The fourth level shifter **364** may receive a fourth driving signal DRV4 belong to a seventh voltage domain between the common power supply voltage (VDD) and the ground voltage GND, shift the seventh voltage domain to a eighth voltage domain between the fourth power supply voltage VDD4 and the ground voltage GND, and output the shifted signal to the fourth gate driver **354**. The eighth voltage domain may have the fourth power supply voltage VDD4 as a high level and the ground voltage GND as a low level.

The voltage converter **300** further includes a controller **380**. The controller **380** may receive a first clock signal CLK1. The controller **380** may control the first driving signal DRV1, the second driving signal DRV2, the third driving signal DRV3 and the fourth driving signal DRV4 for turning on or turning off the first transistor **321**, the second transistor **322**, the third transistor **323** and the fourth transistor **324** respectively based on the first clock signal CLK1.

The controller **380** may control the first driving signal DRV1 and the third driving signal DRV3 identically. The controller **380** may turn on or turn off the first transistor **321** and the third transistor **323** simultaneously. The controller **380** may control the second driving signal DRV2 and the fourth driving signal DRV4 identically. The controller **380** may turn on or turn off the second transistor **322** and the fourth transistor **324** simultaneously.

The controller **380** may control the first driving signal DRV1 (or the third driving signal DRV3) and the second driving signal DRV2 (or the fourth driving signal DRV4) complementally. When the controller **380** turns on the first transistor **321** and the third transistor **323**, the controller **380** turns off the second transistor **322** and the fourth transistor **324**. When the controller **380** turns off the first transistor **321** and the third transistor **323**, the controller **380** turns on the second transistor **322** and the fourth transistor **324**.

The controller **380** may generate a second clock signal CLK2 based on the first clock signal CLK1. The controller may output the second clock signal CLK2 to a regulator **390**.

The voltage converter **300** may further include the regulator **390**. The regulator **390** receives the input voltage VIN, the first voltage V1, the second voltage V2, the third voltage V3 and the second clock signal CLK2. The paths delivering the first voltage V1, the second voltage V2 and the third voltage V3 are omitted to avoid unnecessary complexity of the drawing.

The regulator **390** may generate the first power supply voltage VDD1, the second power supply voltage VDD2, the third power supply voltage VDD3 and the fourth power supply voltage VDD4 based on the input voltage VIN, the first voltage V1, the second voltage V2, the third voltage V3 and the second clock signal CLK2.

The regulator **390** may control the first power supply voltage VDD1 being higher than the first voltage V1 such that the first gate driving signal GD1 is able to turn on the first transistor **321** when the first gate driving signal GD1 has a high level which is the first power supply voltage VDD1.

The regulator **390** may control the second power supply voltage VDD2 being higher than the second voltage V2 such that the second gate driving signal GD2 is able to turn on the second transistor **322** when the second gate driving signal GD2 has a high level which is the second power supply voltage VDD2.

The regulator **390** may control the third power supply voltage VDD3 being higher than the third voltage V3 such that the third gate driving signal GD3 is able to turn on the third transistor **323** when the third gate driving signal GD3 has a high level which is the third power supply voltage VDD3.

The regulator **390** may control the fourth power supply voltage VDD4 being higher than the ground voltage GND such that the fourth gate driving signal GD4 is able to turn on the fourth transistor **324** when the fourth gate driving signal GD4 has a high level which is the fourth power supply voltage VDD4.

The voltage converter **300** may further include a output capacitor COUT and a flying capacitor CFLY. The output capacitor COUT is connected between the second node N2 and the ground node. The flying capacitor CFLY is connected between the first node N1 and the third node N3. The second node N2 may be an output node NOUT from which the second voltage V2 is output as a output voltage VOUT.

The first transistor **321**, the second transistor **322**, the third transistor **323**, the fourth transistor **324**, the first gate driver **351**, the second gate driver **352**, the third gate driver **353**, the fourth gate driver **354**, the first level shifter **361**, the second level shifter **362**, the third level shifter **363**, the fourth level shifter **364**, the controller **380** and the regulator **390** may be included in a single chip **310**. The output capacitor COUT and the flying capacitor CFLY may be connected to the single chip **310**.

In at least one example embodiment, the fourth power supply voltage VDD4 may be the common power supply voltage (VDD). In this case, the eighth voltage domain of the fourth level shifter **364** may be identical with the seventh voltage domain. Thus, the fourth level shifter **364** is able to be omitted. The common power supply voltage (VDD) may be supplied from any component (not excluding the regulator **390**) to the fourth gate driver **354**. In at least one example embodiment, the first transistor **321**, the second transistor **322**, the third transistor **323** and the fourth transistor **324** may be high voltage transistors having endurances for high voltages.

FIG. **20** illustrates a first phase of the voltage converter **300**. Only some elements of the voltage converter **300** which are necessary for describing the first phase are illustrated in FIG. **20**. Referring to FIGS. **19** and **20**, in the first phase, the controller **380** may turn on the first transistor **321** and the third transistor using the first gate driving signal GD1 and the third gate driving signal. The controller **380** may turn off the second transistor **322** and the fourth transistor **324** using the second gate driving signal GD2 and the fourth gate driving signal GD4.

The output capacitor COUT and the flying capacitor CFLY are connected in series between the input node NIN and the ground node through the first transistor **321** and the third transistor **323**. The output capacitor COUT and the flying capacitor CFLY are charged with the input voltage VIN.

FIG. **21** illustrates a second phase of the voltage converter **300** subsequent to the first phase of FIG. **20**. Referring to FIGS. **19** and **21**, in the second phase, the controller **380** may turn off the first transistor **321** and the third transistor using the first gate driving signal GD1 and the third gate driving

signal. The controller **380** may turn on the second transistor **322** and the fourth transistor **324** using the second gate driving signal GD**2** and the fourth gate driving signal GD**4**.

The output capacitor COUT and the flying capacitor CFLY are connected in parallel between the output node NOUT and the ground node through the second transistor **322** and the fourth transistor **324**. Thus, the output voltage VOUT may become a half of the input voltage VIN.

By repeating the first phase and the second phase in response to the first clock signal, the output voltage VOUT may converge on the half of the input voltage. The voltage converter **300** may perform 2:1 capacitor voltage division.

In at least one example embodiment, the first voltage V**1** may swing between the half of the input voltage VIN and the input voltage VIN. The third voltage may swing between the ground voltage and the half of the input voltage VIN. The flying capacitor CFLY may be charged with the half of the input voltage VIN.

When outputting the half of the input voltage VIN as the output voltage VOUT, the first voltage V**1** and the third voltage V**3** swing. When the first transistor **321** and the third transistor **323** are turned on, the first voltage V**1** and the third voltage V**3** increase. When the second transistor **322** and the fourth transistor **324** are turned on, the first voltage V**1** and the third voltage V**3** decrease. Thus, maintaining the first power supply voltage VDD**1**, the second power supply voltage VDD**2** and the third power supply voltage VDD**3** respectively being higher than the first voltage V**1**, the second voltage V**2** and the third voltage V**3** is very important for successfully turning on or off the first transistor **321**, the second transistor **322**, the third transistor **323** and the fourth transistor **324**.

The regulator **390** according to at least one example embodiment of the inventive concepts control the first power supply voltage VDD**1**, the second power supply voltage VDD**2** and the third power supply voltage VDD**3** respectively being higher than the first voltage V**1**, the second voltage V**2** and the third voltage V**3**.

FIG. **22** illustrates at least one example embodiment of the regulator **390**. Referring to FIGS. **19** and **22**, the regulator **390** may include a charge pump **391**, a first generator **392**, a second generator **393** and a third generator **394**.

The charge pump **391** may include a first Schottky diode SD**1** and a second Schottky diode SD**2** connected in series. The charge pump **391** may further include a first pump capacitor CP**1** having a first terminal connected to a node between the first Schottky diode SD**1** and the second Schottky diode SD**2**, a first pump transistor CT**1** connected between a second terminal of the first pump capacitor CP**1** and the ground node, and a second pump transistor CT**2** connected between the second terminal of the first pump capacitor CP**1** and a common power supply node through which the common power supply voltage VDD is supplied.

The first pump transistor CT**1** may be a NMOS transistor and have a gate controlled by the second clock signal CLK**2**. The second pump transistor CT**2** may be a PMOS transistor and have a gate controlled by the second clock signal. The first pump transistor CT**1** and the second pump transistor CT**2** may have complementary types. The regulator **390** may further include a second pump capacitor CP**2** connected in parallel with the first Schottky diode SD**1** and the second Schottky diode SD**2**.

When the second clock signal CLK**2** has a high level, the first pump transistor CT**1** may be turned on, and the second pump transistor CT**2** may be turned off. The first pump capacitor CP**1** may be charged with the input voltage VIN. When the second clock signal CLK**2** has a low level, the first pump transistor CT**1** may be turned off, and the second pump transistor CT**2** may be turned on. The second terminal of the first pump capacitor CP**1** is supplied with the common power supply voltage CDD. Thus, the first pump capacitor CP**1** may charge the second pump transistor with the common power supply voltage VDD.

The pump voltage VCP, which is an output voltage of the charge pump **391**, may be the input voltage VIN plus the common power supply voltage VDD. The pump voltage VCP is applied to the first generator **392**, the second generator **393** and the third generator **394**. The first Schottky diode SD**1** and the second Schottky diode SD**2** may prevent a reversal of current. In at least one example embodiment, the first pump transistor CT**1** and the second pump transistor CT**2** may be high voltage transistors.

The first generator may receive the pump voltage VCP and the first voltage V**1**. The first generator may include a voltage resistor RV, a first voltage Schottky diode SDV**1**, and a Zener diode ZD connected in series between a node through which the pump voltage VCP is supplied and another node through which the first voltage V**1** is supplied.

The first generator **392** may further include a first voltage capacitor CV**1** connected between the node through which the first voltage V**1** is supplied and another node between the first voltage Schottky diode SDV**1** and the Zener diode ZD. The regulator **390** may further include a voltage transistor TV, a second voltage Schottky diode SDV**2** and a second voltage capacitor CV**2** connected in series between the node through which the pump voltage VCP is supplied and the node through the first voltage V**1** is supplied.

The voltage transistor TV may be shown as a model having a body diode to help thorough understanding of the inventive concepts. Because of the body diode, there may be a reversal of current. The first voltage Schottky diode SDV**1** and the second voltage Schottky diode SDV**2** may prevent the reversal of the current.

A voltage of the node between the Zener diode ZD and the first voltage Schottky diode SDV**1** (hereinafter, a voltage of the Zener diode ZD) is determined by characteristics or features of the Zener diode ZD. The voltage transistor TV may flow current in response to the voltage of the Zener diode ZD. The current may cause a voltage at a node between the second voltage Schottky diode SDV**2** and the second voltage capacitor CV**2**.

The voltage of the node between the second voltage Schottky diode SDV**2** and the second voltage capacitor CV**2** may be output as the first power supply voltage VDD**1**. Because the voltage of the Zener diode ZD is higher than the first voltage V**1**, the first power supply voltage V**1** may be higher than the first power supply voltage.

The second generator **393** has the same structure with the first generator **392**. Instead of receiving the first voltage V**1** and outputting the first power supply voltage VDD**1**, the second generator **393** may receive the second voltage V**2** and output the second power supply voltage VDD**2** higher than the second voltage V**2**.

The third generator **394** has the same structure with the first generator **392**. Instead of receiving the first voltage V**1** and outputting the first power supply voltage VDD**1**, the third generator **394** may receive the third voltage V**3** and output the third power supply voltage VDD**3** higher than the third voltage V**3**. The regulator **390** may output the common power supply voltage VDD as the fourth power supply voltage VDD.

In FIG. **22**, the first voltage Schottky diode SDV**1**, the second voltage Schottky diode SDV**2**, the first voltage capacitor CV**1**, the second voltage capacitor CV**2** and the

voltage transistor TV are named using a term 'voltage'. The term 'voltage' merely means that these elements are related with generating a voltage, and does not limit the scope and sprit of the inventive concepts.

In at least one example embodiment, the charge pump **391** may be implemented with the regulator **190** which operates as shown in FIG. **17**. In at least one example embodiment, when the voltage converter **300** employs additional transistors between the input node NIN and the ground node, additional power supply voltages for the additional transistors may be obtained by adding generators as shown in FIG. **22**. Thus, the voltage converter **300** provides enhanced flexibility.

In the above-described example embodiments, components according to example embodiments of the inventive concepts are referred to by using the term "block". The "block" may be implemented with various hardware devices, such as an integrated circuit, an application specific IC (ASCI), a field programmable gate array (FPGA), and a complex programmable logic device (CPLD), software, such as firmware and applications driven in hardware devices, or a combination of a hardware device and software. Also, "block" may include circuits or intellectual property (IP) implemented with semiconductor devices.

According to at least one example embodiment of the inventive concepts, a voltage converter adjusts a gate voltage of a switching transistor such that the switching transistor is turned on according to a change in environment. Accordingly, the voltage converter with improved reliability and/or an operating method thereof may be provided.

While various example embodiments of the inventive concepts have been described with reference to example embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the spirit and scope of the inventive concepts. Therefore, it should be understood that the above example embodiments are not limiting, but illustrative.

What is claimed is:

1. A voltage converter comprising:

a first transistor connected between an input node and a first node;

a second transistor connected between the first node and an output node;

a third transistor connected between a second node and a third node;

a fourth transistor connected between the third node and a ground node;

an output capacitor connected between the third node and the ground node;

a flying capacitor connected between the first node and a fourth node;

a first gate driver connected to a first gate of the first transistor and configured to output a first power supply voltage as a first high level and a first voltage of the first node as a first low level;

a second gate driver connected to a second gate of the second transistor and configured to output a second power supply voltage as a second high level and a second voltage of the second node as a second low level;

a third gate driver connected to a third gate of the third transistor and configured to output a third power supply voltage as a third high level and a third voltage of the third node as a third low level;

a fourth gate driver connected to a fourth gate of the fourth transistor and configured to output a fourth power supply voltage as a fourth high level and a ground voltage of the ground node as a fourth low level; and

a regulator configured to receive an input voltage from the input node, the first voltage from the first node, the second voltage from the second node and the third voltage from the third node, and generate the first power supply voltage being higher than the first voltage, the second power supply voltage being higher than the second voltage, the third power supply voltage being higher than the third voltage and the fourth power supply voltage being higher than the ground voltage.

2. The voltage converter of claim **1**, further comprising:

a controller configured to turn on or turn off the first transistor and the third transistor simultaneously and turn on or turn off the second transistor and the fourth transistor simultaneously,

wherein the controller is further configured to turn on or turn off the first transistor and the second transistor alternately.

3. The voltage converter of claim **2**, wherein the controller is further configured to:

receive a first clock signal;

turn on or turn off the first through fourth transistors in response to the first clock signal;

generate a second clock signal based on the first clock signal; and

transmit the first clock signal to the regulator.

4. The voltage converter of claim **3**, wherein the second voltage is output as an output voltage of the voltage converter.

5. The voltage converter of claim **4**, wherein the output voltage is a half of the input voltage.

6. The voltage converter of claim **1**, wherein the regulator includes:

a charge pump configured to

receive a common power supply voltage, the input voltage and a clock signal; and

output a pump voltage which is the common power supply voltage plus the input voltage in response to the clock signal.

7. The voltage converter of claim **6**, wherein the charge pump includes:

a first diode connected between the input node and a fifth node;

a second diode connected between the fifth node and a sixth node through which the pump voltage is output;

a first capacitor having a first terminal connected to the fifth node;

a fifth transistor connected between a second terminal of the first capacitor and the ground node and having a gate controlled by the clock signal;

a sixth transistor connected between the second terminal of the first capacitor and a seventh node through which the common power supply voltage is input; and

a second capacitor connected between the input node and the sixth node,

wherein the fifth transistor and the sixth transistor have complementary types.

8. The voltage converter of claim **7**, wherein the first diode and the second diode are Schottky diodes.

9. The voltage converter of claim **6**, wherein the regulator further includes:

a first generator configured to receive the pump voltage and the first voltage, and output the first power supply voltage;

a second generator configured to receive the pump voltage and the second voltage, and output the second power supply voltage; and

a third generator configured to receive the pump voltage and the third voltage, and output the third power supply voltage.

10. The voltage converter of claim **9**, wherein the first generator includes:

a resistor having a first terminal connected to a fifth node through which the pump voltage is input;

a first diode having a first terminal connected to a second terminal of the resistor;

a second diode connected between a second terminal of the first diode and a sixth node through which the first voltage is input;

a first capacitor connected between the sixth node and a seventh node between the first diode and the second diode;

a transistor having a first terminal connected to the fifth node and a gate connected to the seventh node;

a third diode connected to a second terminal of the transistor and a eighth node through which the first power supply voltage is output; and

a second capacitor connected between the eighth node and the sixth node.

11. The voltage converter of claim **10**, wherein

the first and third diodes are Schottky diodes; and

the second diode is a Zener diode.

12. The voltage converter of claim **10**, wherein the second diode is configured to control the first power supply voltage to be higher than the first voltage.

13. The voltage converter of claim **10**, wherein the second generator and the third generator have the same structure with the first generator.

14. The voltage converter of claim **6**, wherein the regulator is configured to output the common power supply voltage as the fourth power supply voltage.

15. The voltage converter of claim **1**, further comprising:

a controller configured to output a first driving signal, a second driving signal, a third driving signal and a fourth driving signal, the first through fourth driving signals belong to a voltage domain between a common power supply voltage and the ground voltage;

a first level shifter configured to convert the first driving signal to a first voltage domain to output the converted first driving signal to the first gate driver, the first voltage domain being between the first power supply voltage and the first voltage;

a second level shifter configured to convert the second driving signal to a second voltage domain to output the converted second driving signal to the second gate driver, the second voltage domain being between the second power supply voltage and the second voltage;

a third level shifter configured to convert the third driving signal to a third voltage domain to output the converted third driving signal to the third gate driver, the third voltage domain being between the third power supply voltage and the third voltage; and

a fourth level shifter configured to convert the fourth driving signal to a fourth voltage domain to output the converted fourth driving signal to the fourth gate driver, the fourth voltage domain being between the fourth power supply voltage and the ground voltage.

16. The voltage converter of claim **1**, wherein the first through fourth transistors, the first through fourth gate drivers and the regulator are included in a single chip.

17. A method of operating a voltage converter, comprising:

obtaining a first voltage between a first transistor and a second transistor, a second voltage between the second transistor and a third transistor, and a third voltage between the third transistor and a fourth transistor, the first through fourth transistors being connected in series between an input node and a ground node;

generating a first power supply voltage higher than the first voltage based on the first voltage;

generating a second power supply voltage higher than the second voltage based on the second voltage;

generating a third power supply voltage higher than the third voltage based on the third voltage;

generating a fourth power supply voltage higher than a ground voltage of the ground node;

applying the first power supply voltage to a gate of the first transistor in a first phase and the first voltage to the gate of the first transistor in a second phase;

applying the second voltage to a gate of the second transistor in the first phase and the second power supply voltage to the gate of the second transistor in the second phase;

applying the third power supply voltage to a gate of the third transistor in the first phase and the third voltage to the gate of the third transistor in the second phase; and

applying the ground voltage to a gate of the fourth transistor in the first phase and the fourth power supply voltage to the gate of the fourth transistor in the second phase,

wherein an output capacitor is connected between the ground node and a first node between the second and third transistors, and

wherein a flying capacitor is connected between a second node and a third node, the second node being between the first transistor and the second transistor, the third node being between the third transistors and the fourth transistors.

18. The method of claim **17**, further comprising:

outputting the second voltage which is a half of an input voltage from the input node.

19. The method of claim **17**, wherein generating the first power supply voltage includes:

generating a pump voltage which is a sum of a common power supply voltage and an input voltage from the input node; and

generating the first power supply voltage using the pump voltage, the first voltage and a Zener diode.

20. A voltage converter comprising:

a first transistor connected between an input node and a first node;

a second transistor connected between the first node and an output node;

a third transistor connected between a second node and a third node;

a fourth transistor connected between the third node and a ground node;

an output capacitor connected between the third node and the ground node;

a flying capacitor connected between the first node and a fourth node;

a first gate driver connected to a first gate of the first transistor and configured to output a first power supply voltage as a first high level and a first voltage of the first node as a first low level;

a second gate driver connected to a second gate of the second transistor and configured to output a second

power supply voltage as a second high level and a second voltage of the second node as a second low level;

a third gate driver connected to a third gate of the third transistor and configured to output a third power supply voltage as a third high level and a third voltage of the third node as a third low level;

a fourth gate driver connected to a fourth gate of the fourth transistor and configured to output a fourth power supply voltage as a fourth high level and a fourth voltage of the fourth node as a fourth low level;

a regulator configured to receive an input voltage from the input node, the first voltage from the first node, the second voltage from the second node and the third voltage from the third node, and generate the first power supply voltage being higher than the first voltage, the second power supply voltage being higher than the second voltage, the third power supply voltage being higher than the third voltage and the fourth power supply voltage being higher than a ground voltage of the ground node;

a controller configured to output a first driving signal, a second driving signal, a third driving signal and a fourth driving signal, the first through fourth driving signals belong to a voltage domain between a common power supply voltage and the ground voltage;

a first level shifter configured to convert the first driving signal to a first voltage domain to output the converted first driving signal to the first gate driver, the first voltage domain being between the first power supply voltage and the first voltage;

a second level shifter configured to convert the second driving signal to a second voltage domain to output the converted second driving signal to the second gate driver, the second voltage domain being between the second power supply voltage and the second voltage; and

a third level shifter configured to convert the third driving signal to a third voltage domain to output the converted third driving signal to the third gate driver, the third voltage domain being between the third power supply voltage and the third voltage,

wherein the fourth driving signal is transferred to the fourth gate driver, and

wherein the regulator includes,

a charge pump configured to receive a common power supply voltage, the input voltage and a clock signal, and output a pump voltage which is the common power supply voltage plus the input voltage in response to the clock signal,

a first generator configured to receive the pump voltage and the first voltage, and output the first power supply voltage,

a second generator configured to receive the pump voltage and the second voltage, and output the second power supply voltage, and

a third generator configured to receive the pump voltage and the third voltage, and output the third power supply voltage.

* * * * *