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Chung et al.

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(54) **EFFICIENT METAL-INSULATOR-METAL CAPACITOR**

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*H01L 49/02* (2006.01)

(52) **U.S. Cl.**
CPC .................................... ***H01L 28/60*** (2013.01)

(58) **Field of Classification Search**
CPC ................................................. H01L 27/10829
See application file for complete search history.

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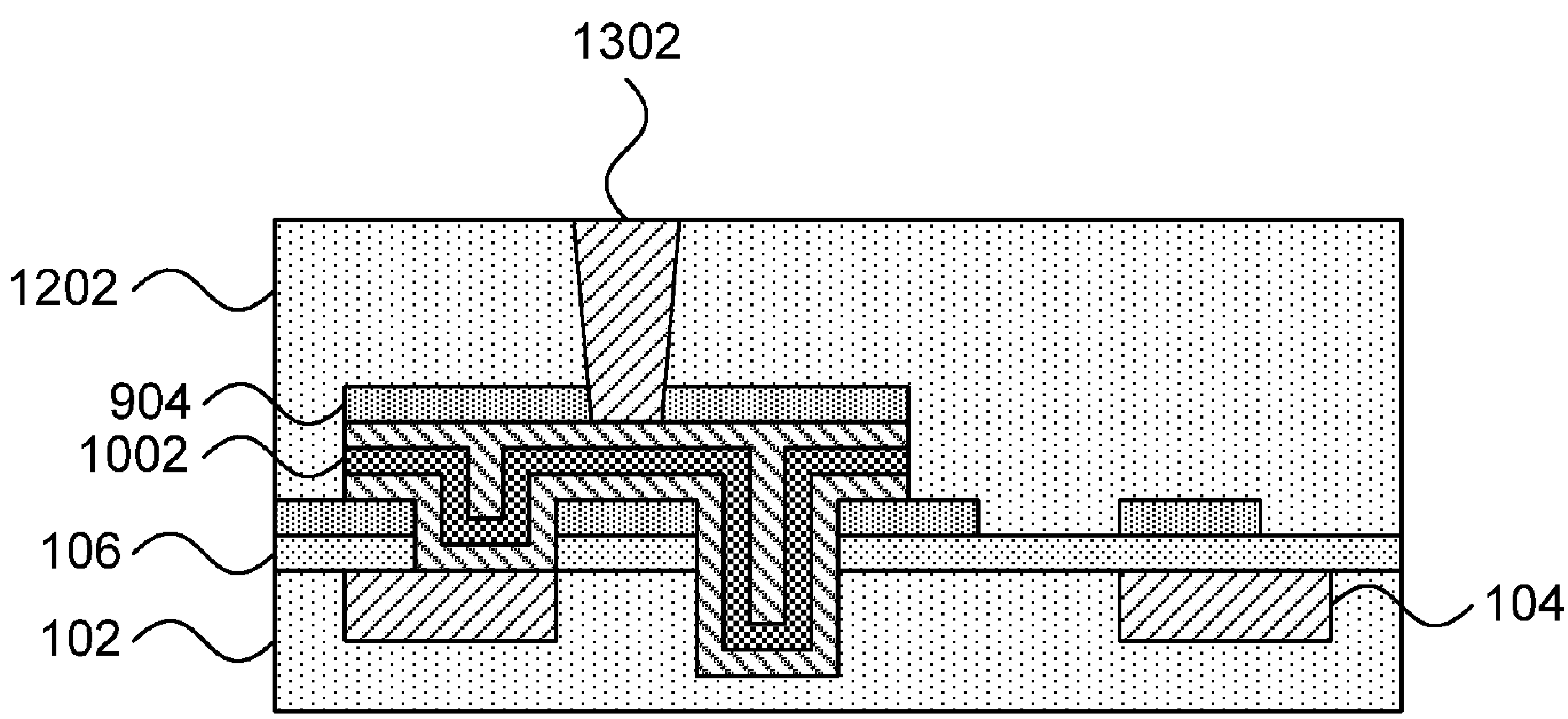
(57) **ABSTRACT**

Capacitors include a stack that has a first metallic layer formed over a substrate with at least one high domain and at least one low domain, an insulator formed over the first metallic layer, and a second metallic layer formed over the insulator. A bottom contact is formed in the substrate having a top surface that is even with a top surface of the substrate in the at least one high domain. A cap layer is formed directly on the substrate in the high domains, under the stack.

**17 Claims, 5 Drawing Sheets**



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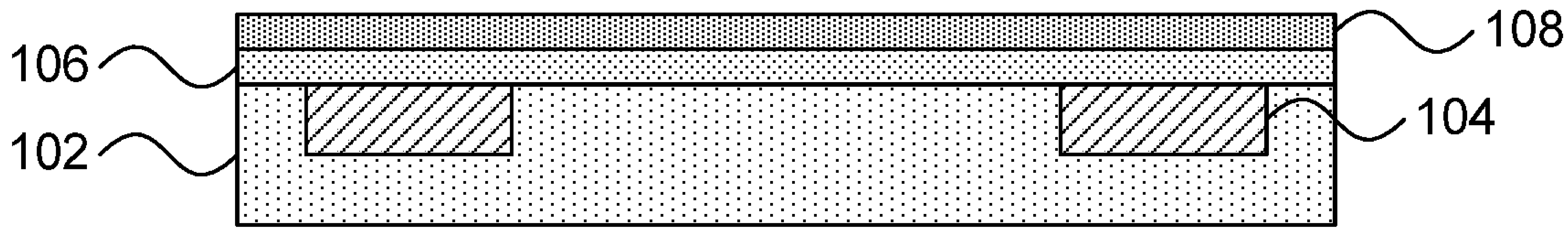


FIG. 1

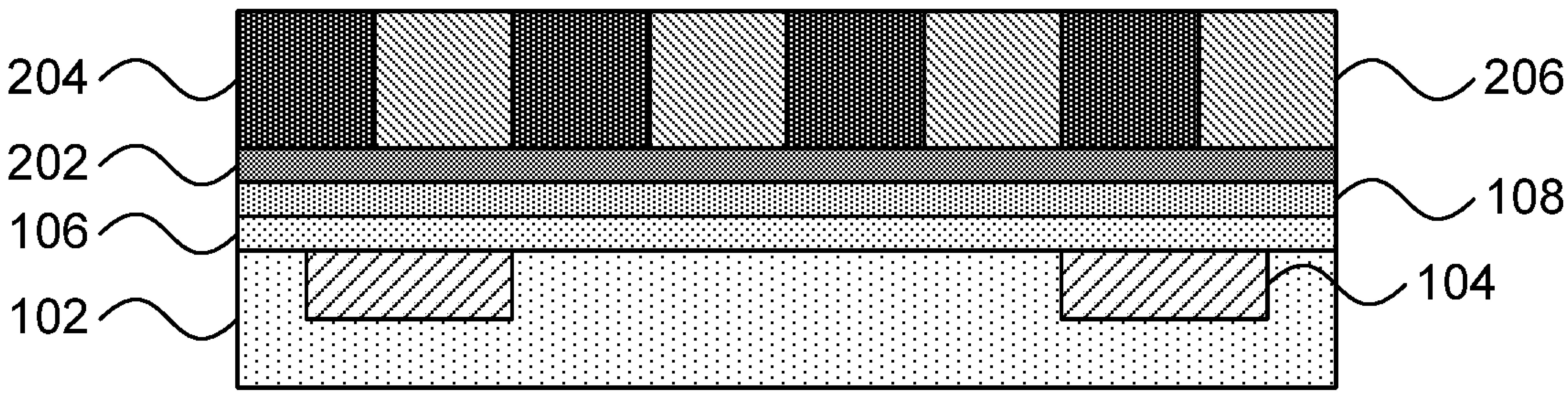


FIG. 2

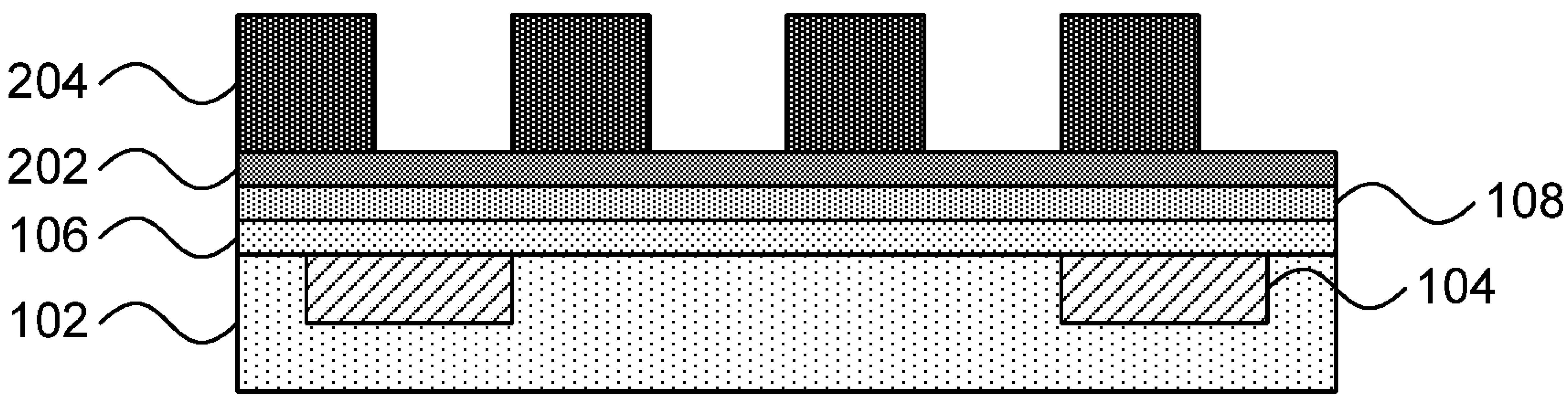


FIG. 3

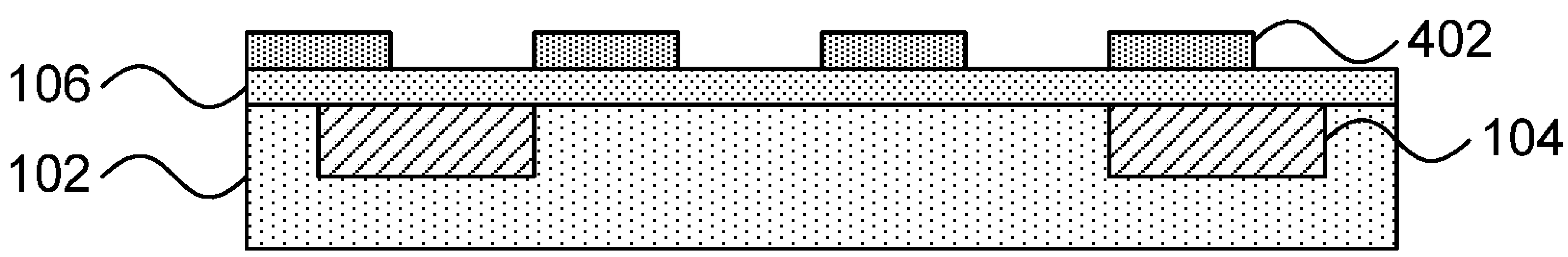


FIG. 4

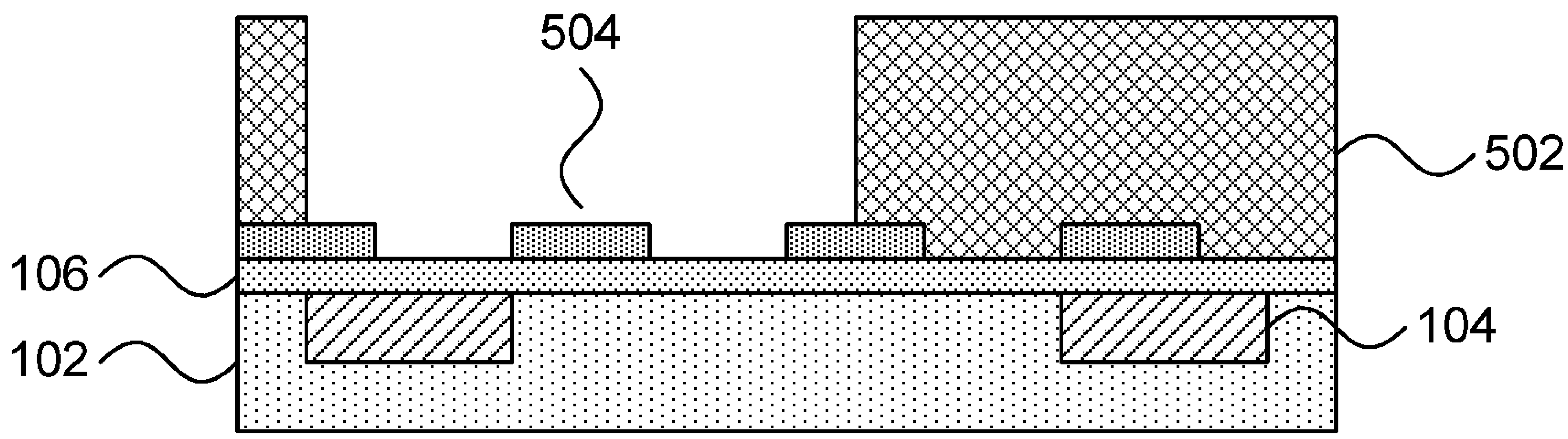


FIG. 5

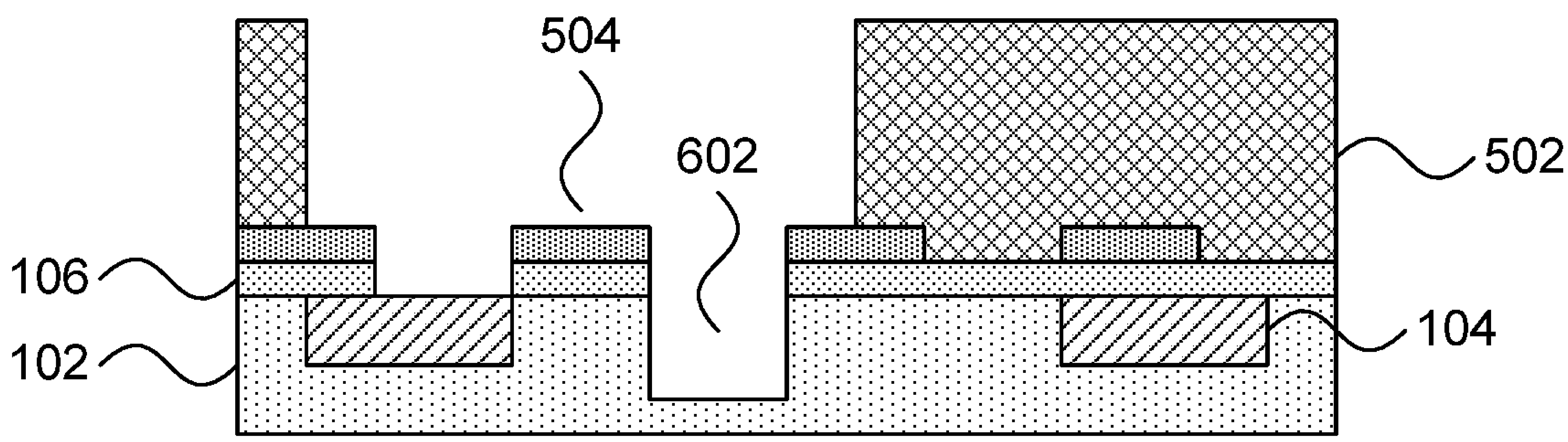


FIG. 6

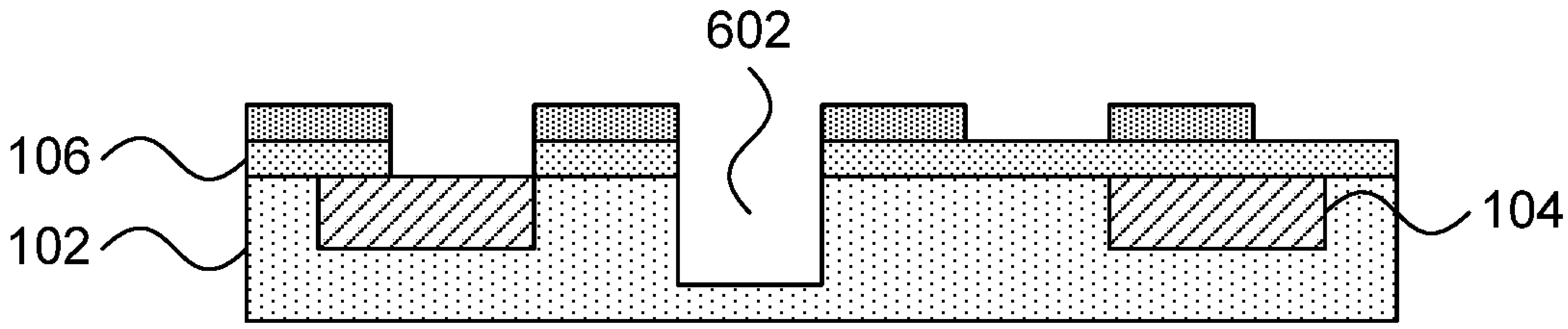


FIG. 7

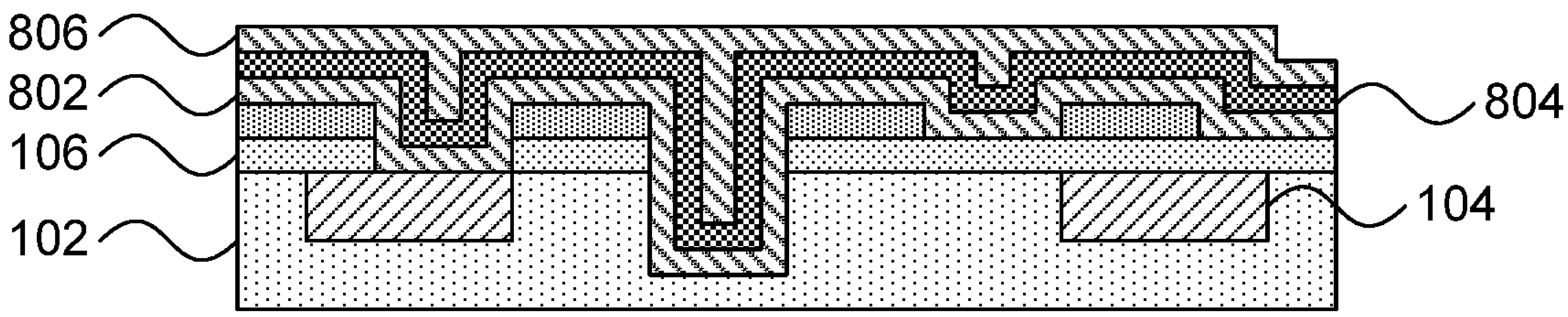


FIG. 8

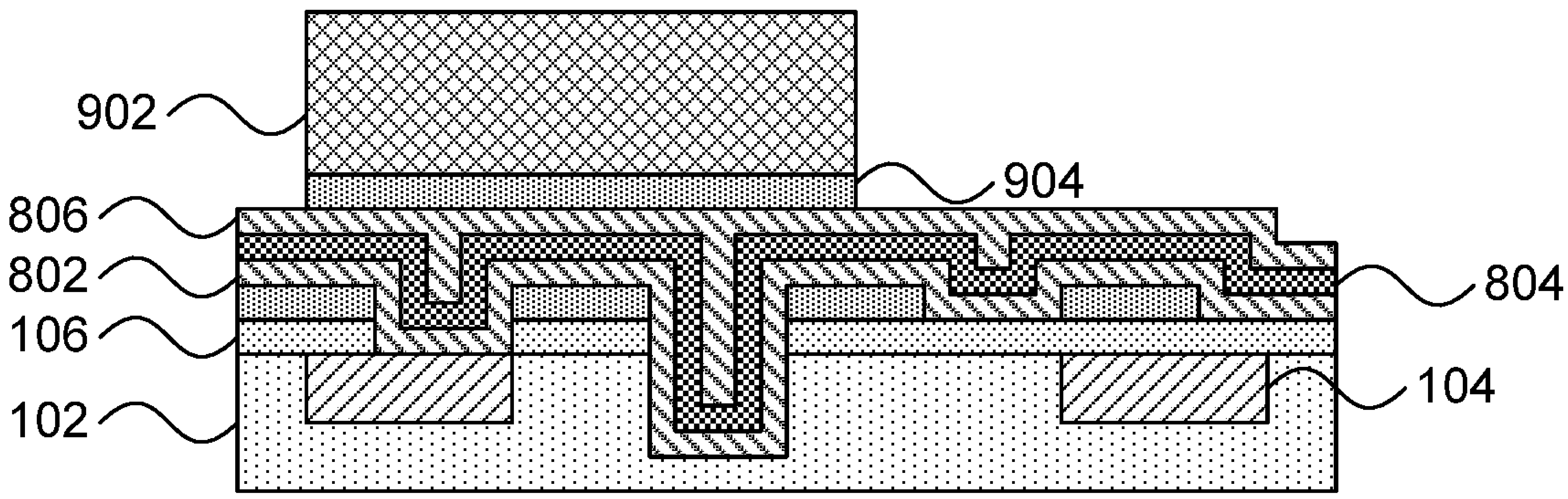


FIG. 9

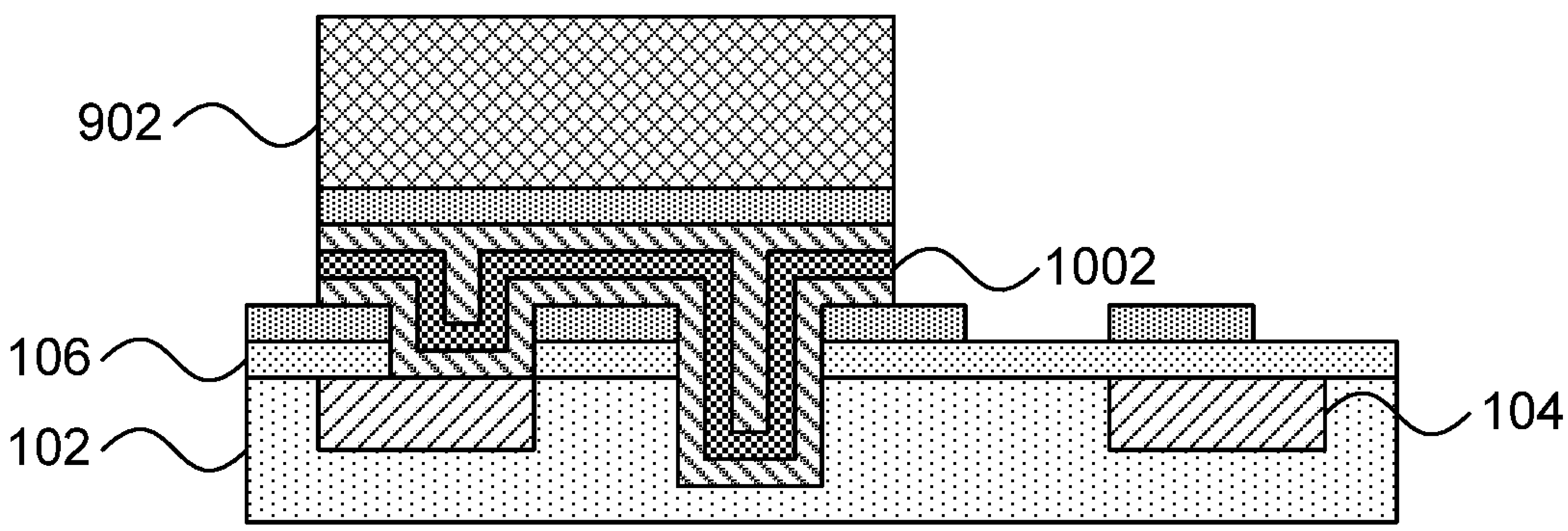


FIG. 10

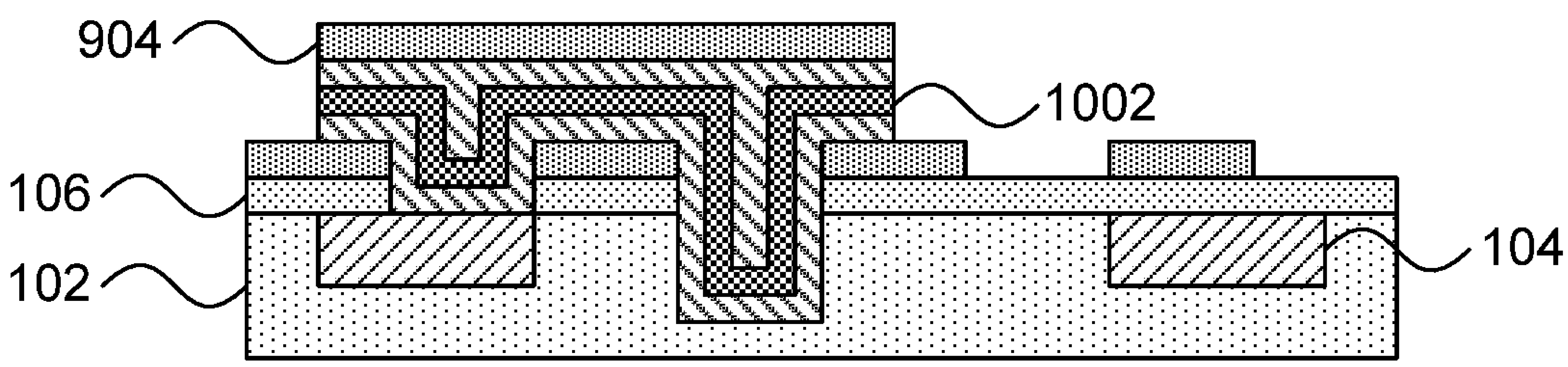


FIG. 11

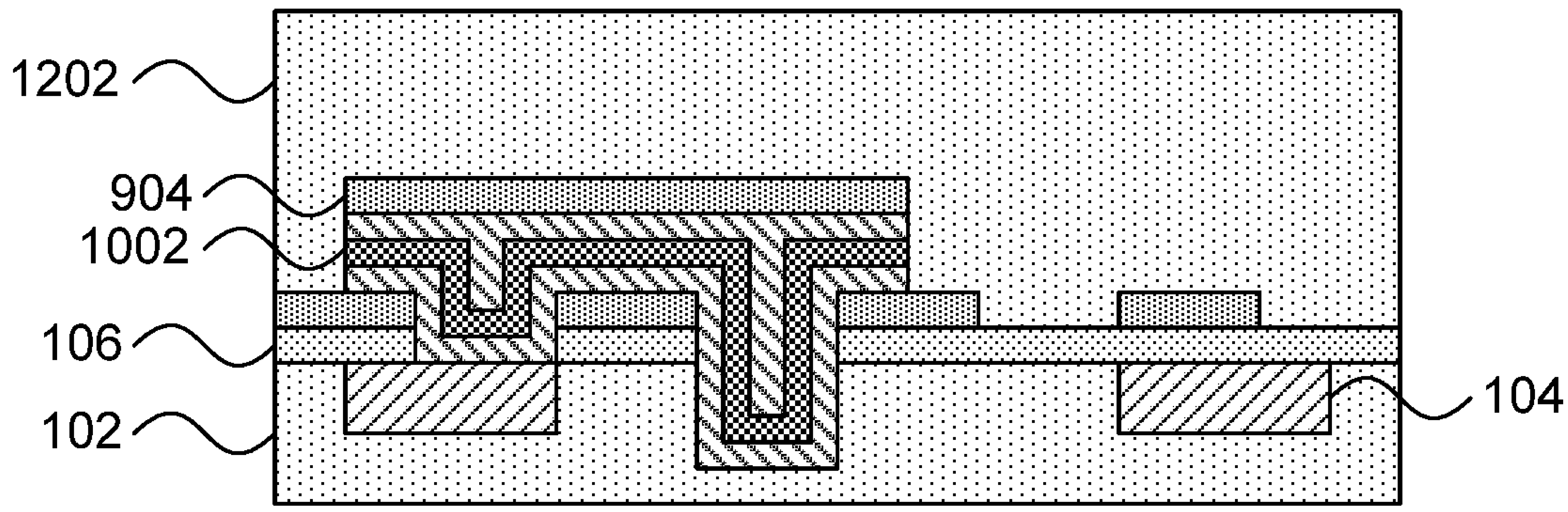


FIG. 12

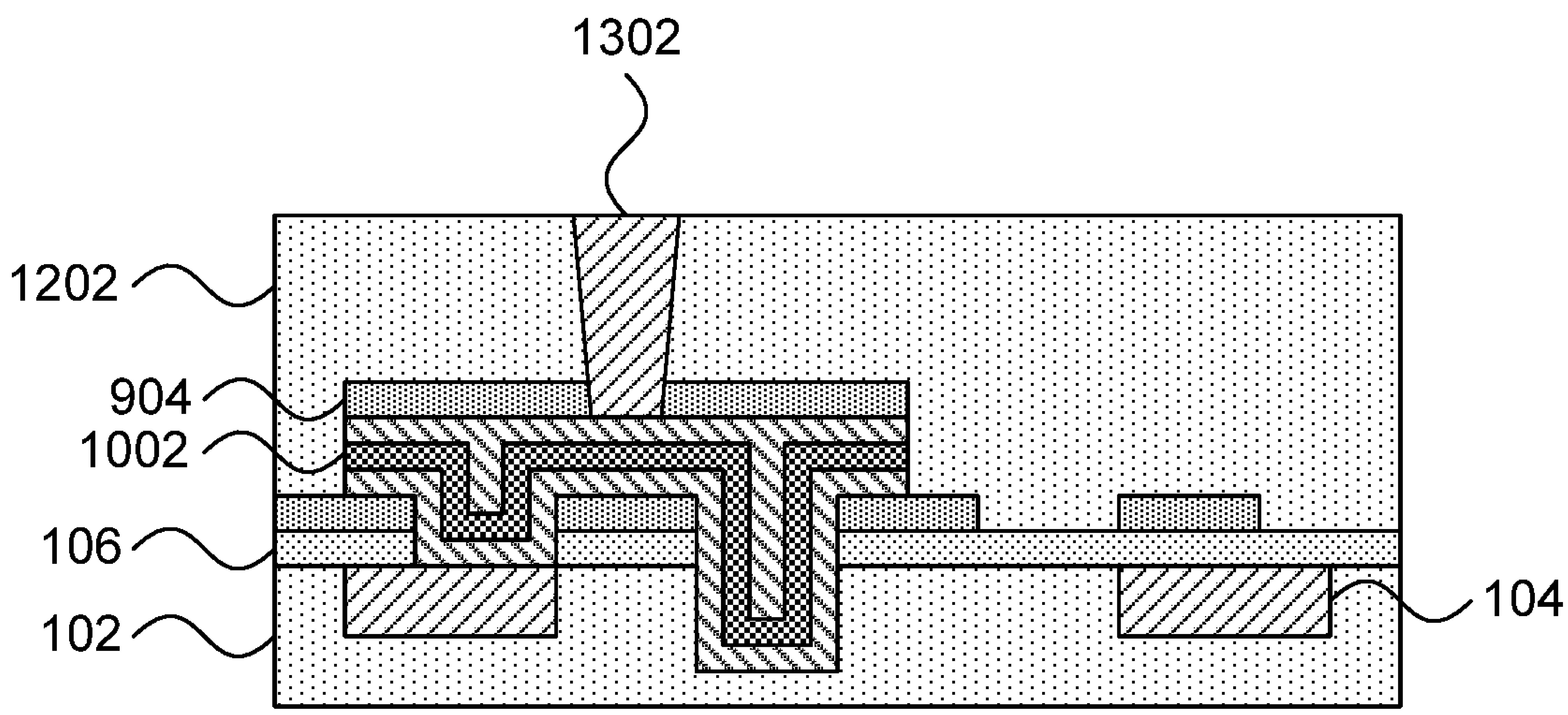


FIG. 13

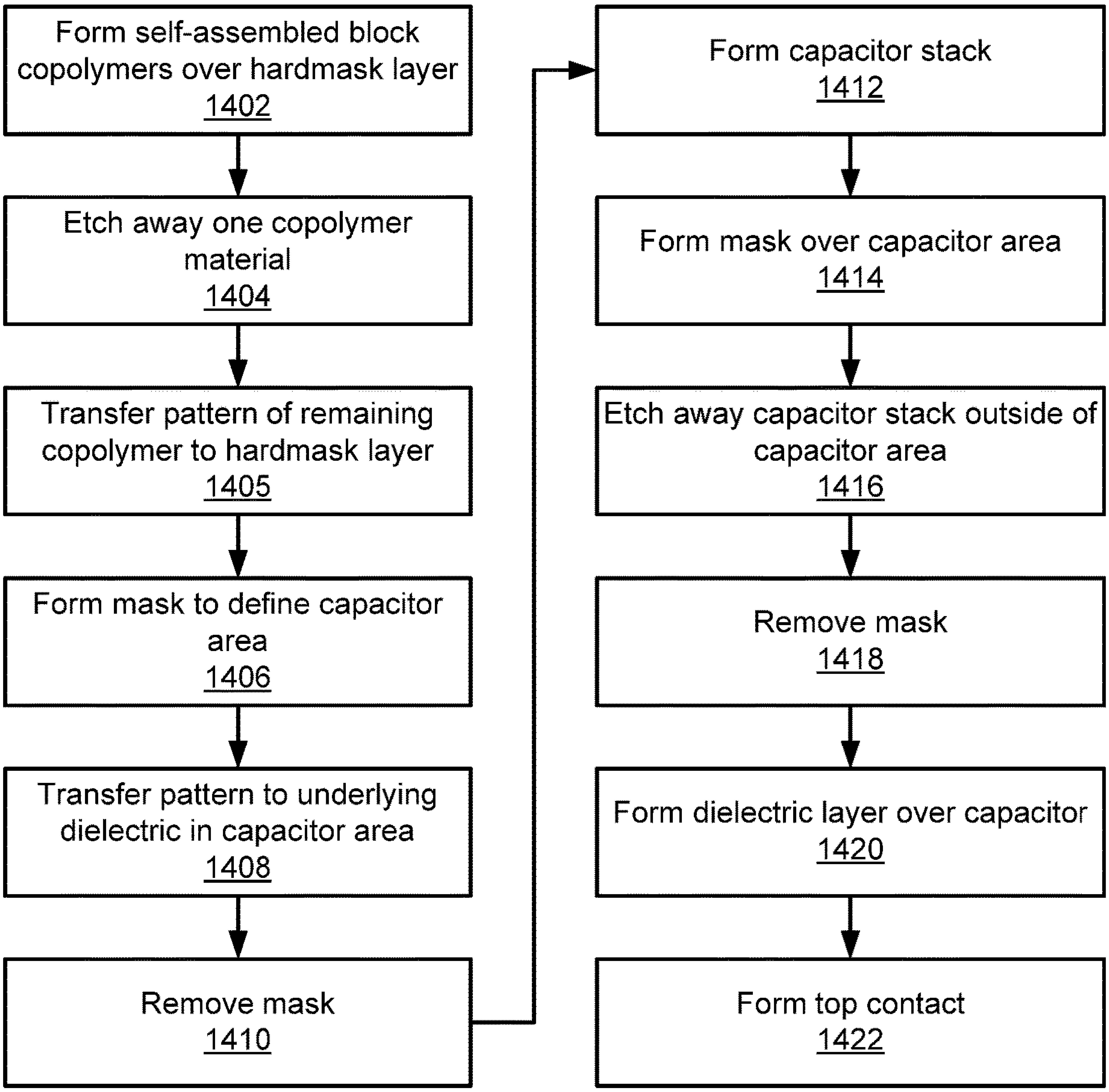
Form self-assembled block copolymers over hardmask layer
1402
Etch away one copolymer material
1404
Transfer pattern of remaining copolymer to hardmask layer
1405
Form mask to define capacitor area
1406
Transfer pattern to underlying dielectric in capacitor area
1408
Remove mask
1410
Form capacitor stack
1412
Form mask over capacitor area
1414
Etch away capacitor stack outside of capacitor area
1416
Remove mask
1418
Form dielectric layer over capacitor
1420
Form top contact
1422

FIG. 14

# EFFICIENT METAL-INSULATOR-METAL CAPACITOR

## BACKGROUND

### Technical Field

The present invention generally relates to capacitor fabrication and, more particularly, to improved processes for fabricating metal-insulator-metal capacitors that use self-assembling block copolymers to increase capacitance per unit area without increasing the number of photomasks needed.

### Description of the Related Art

Metal-insulator-metal capacitors are used throughout circuit designs to provide integrated capacitors that can be formed during semiconductor fabrication processes instead of using discrete capacitors on circuit board. However, to increase the capacitance per unit area, additional steps are needed to change the topography of the device. In particular, additional mask steps are often used to provide patterning. These additional mask steps increase process complexity, and hence fabrication costs, as well as potential plasma damage at the interface between metal and dielectric layers.

## SUMMARY

A capacitor includes a stack that has a first metallic layer formed over a substrate with at least one high domain and at least one low domain, an insulator formed over the first metallic layer, and a second metallic layer formed over the insulator. A bottom contact is formed in the substrate having a top surface that is even with a top surface of the substrate in the at least one high domain. A cap layer is formed directly on the substrate in the high domains, under the stack.

A capacitor includes a stack having a first metallic layer formed over a substrate with at least one high domain and a plurality of low domains, an insulator formed over the first metallic layer, and a second metallic layer formed over the insulator. A bottom contact is formed in the substrate under a first low domain of the first metallic layer, having a top surface that is even with a top surface of the substrate in the at least one high domain. A cap layer is formed directly on the substrate in the high domains, under the stack.

A capacitor includes a stack having a first metallic layer formed over a substrate that comprises at least one high domain and at least one low domain, an insulator formed over the first metallic layer, and a second metallic layer formed over the insulator. A bottom contact is formed in the substrate in electrical contact with the first metallic layer, having a top surface that is even with a top surface of the substrate in the at least one high domain. A cap layer is formed directly on the substrate in the high domains, under the stack. A protective layer is formed over the stack. A dielectric layer is formed over and around the protective layer and the stack. A top contact penetrates the dielectric layer and the protective layer to form an electrical contact with the top metallic layer.

These and other features and advantages will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.



## BRIEF DESCRIPTION OF THE DRAWINGS

The following description will provide details of preferred embodiments with reference to the following figures wherein:

FIG. **1** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **2** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **3** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **4** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **5** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **6** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **7** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **8** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **9** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **10** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **11** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **12** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **13** is a cross-sectional diagram of a step in the formation of a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention;

FIG. **14** is a block/flow diagram of a method of forming a metal-insulator-metal capacitor using block copolymers in accordance with an embodiment of the present invention.

## DETAILED DESCRIPTION

Embodiments of the present invention use self-assembling block copolymers to define patterning regions before the deposition of metal-insulator-metal capacitor (MIMCAP) structures that make use of two metal layers with an insulator layer between them. Patterning creates a more complicated topography and increases the surface area of the MIMCAP structures and, hence, the capacitance per unit area. The use of the self-assembling block copolymers removes the need for an extra masking/patterning step to define the patterning regions, thereby decreasing the process complexity.

Referring now to FIG. **1**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. Conductive contacts **104** are formed in an inter-layer dielectric **102**. It should be understood that, while dielectric materials are particularly contemplated for the interlayer dielectric **102**, other substrate materials such as, e.g., polymers, glass, resins, etc. may be used instead. It is specifically contemplated that the interlayer dielectric **102** can be, e.g., silicon dioxide, silicon nitride, or a low-k dielectric such as SiCOH. The conductive contacts may be formed from any appropriate conductive material such as, e.g., tungsten, titanium, tantalum, ruthenium, zirconium, cobalt, copper, aluminum, lead, platinum, tin, silver, or gold.

A hardmask cap is formed from layers **106** and **108** over the interlayer dielectric **102** and the contacts **104**. The layer **106** may be formed from an appropriate conductor cap to prevent oxidation of the contacts **104** and may be formed from, e.g., tantalum nitride. The layer **106** may also function as an etch stop layer in some cases. The layer **108** is a hardmask material such as, e.g., silicon nitride, tetraethylorthosilicate oxide, or any other appropriate hardmask material for later topography etching of the interlayer dielectric **102**.

Referring now to FIG. **2**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. A neutral layer **202** is formed over the hardmask layer **108**. A layer of self-assembling block copolymer (BCP) is formed over the neutral layer **202** by, e.g., a spin-coating process. An exemplary BCP material is made of two linear and chemically distinct polymer chains covalently bonded together. BCPs can self-assemble into nanoscale structures having dimensions, pitch, and morphology that are determined by the molecular weight of each block, the molecular weight of the BCP molecules, and the ratio of the two blocks, respectively. In the present embodiments, a cylinder forming BCP system may be used, where the first block of the BCP forms matrix domain **204** and the second block of BCP self-assemble in to the minority domain (cylinders) **206**. At molecular level, the BCP chains, once annealed, organize themselves in contact with like materials, arranging themselves abutting end-to-end. Thus, each microdomain is about the size of two blocks. In one specific example, the self-assembling material may have one block that is polystyrene, e.g., forming fins **204**, and one block that is poly(methyl methacrylate) (PMMA), e.g., forming fins **206**.

The neutral layer **202** modifies the surface energy and facilitates the self-assembled structures into vertical cylinders instead of in-plane parallel cylinders, which would have occurred if the substrate had a strong preference to one of the blocks of the BCP. The lengths of the polymer chains can be selected to produce cylinders of diameter between about 10 nm and about 100 nm. In this case, it is specifically contemplated that the self-assembled cylinders may have a center-to-center distance of about 20 nm to about 25 nm. An exemplary annealing condition for self-assembly is a temperature between about 200° C. to about 280° C. for a duration between about 2 minutes and about 300 minutes under ambient atmosphere or a nitrogen atmosphere. The arrangement of the resulting cylinders will be close to a hexagonal array with local grain size ranging from tens to hundreds of nanometers depending on the annealing conditions.

Referring now to FIG. **3**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. One of the self-assembling materials is removed. For example, if polystyrene-PMMA BCPs are used, the PMMA block may be selectively etched with minimum damage to the polystyrene. As used herein, the term "selective" in reference to a material removal process denotes that the rate of material removal for a first material is greater than the rate of removal for at least another material of the structure to which the material removal process is being applied.

Referring now to FIG. **4**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. The pattern from the remaining polymer structure is transferred to the neutral layer **202** and hardmask layer **108**, forming hardmask regions **402**. The pattern can be transferred using, e.g., a directional etch such as reactive ion etching (RIE). The remaining polymer material from the first block of self-assembling material **204** and the neutral layer **202** is etched away.

RIE is a form of plasma etching in which during etching the surface to be etched is placed on the RF powered electrode. Moreover, during RIE the surface to be etched takes on a potential that accelerates the etching species extracted from plasma toward the surface, in which the chemical etching reaction is taking place in the direction normal to the surface. Other examples of anisotropic etching that can be used at this point of the present invention include ion beam etching, plasma etching or laser ablation.

Referring now to FIG. **5**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. A first mask **502** is deposited to define a MIMCAP area **504**. In one example, a layer of photoresist material is deposited and is exposed over the MIMCAP area **504**. The exposed photoresist material can then be selectively removed. In an alternative embodiment, regions outside the MIMCAP area **504** may be exposed, with the unexposed region being selectively removed.

Referring now to FIG. **6**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. The exposed regions of the cap layer **106** are anisotropically etched, exposing one of the conductive contacts **104** and other regions of the interlayer dielectric **102**. Exposed regions of the interlayer dielectric **102** are then anisotropically etched to form cavities **602**. The cavities **602** are used to provide topographies that will increase the capacitance of MIMCAPs.

It should be understood that an arbitrary number of cavities **602** may be formed to any appropriate depth. The cavities **602** are formed according to the exposed capacitor area **504**, so a larger capacitor area **504** (as defined by the mask **502**) will result in more cavities. The horizontal area of the cavities, meanwhile, is determined by the length of the block copolymer chains, with longer chains producing larger block structures and, hence, larger cavities **602**. The depth of the cavities may be determined according to a timed etch, with a longer etch resulting in deeper cavities **602**. It should be understood that the more cavities **602** are included, and the deeper those cavities **602** are, the more vertical surface is provided to increase the capacitance per unit area of the ultimate MIMCAP.

Referring now to FIG. **7**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. The mask **502** is removed, followed by a wet clean to remove any residues or oxides that may remain on the exposed conductive material surfaces.

Referring now to FIG. **8**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. A first metal layer **802** is formed on the surface. The first metal layer **802** may be formed from any appropriate conductive metallic material. It is specifically contemplated that the first metal layer **802** may be formed from, e.g., titanium nitride, although other materials may be used if they will react with oxygen to form an insulating barrier layer. The first metal layer **802** may be formed by any appropriate process including, e.g., chemical vapor deposition (CVD), physical vapor deposition (PVD), or atomic layer deposition (ALD).

CVD is a deposition process in which a deposited species is formed as a result of chemical reaction between gaseous reactants at greater than room temperature (e.g., from about 25° C. about 900° C.). The solid product of the reaction is deposited on the surface on which a film, coating, or layer of the solid product is to be formed. Variations of CVD processes include, but are not limited to, Atmospheric Pressure CVD (APCVD), Low Pressure CVD (LPCVD), Plasma Enhanced CVD (PECVD), and Metal-Organic CVD (MOCVD) and combinations thereof may also be employed. In alternative embodiments that use PVD, a sputtering apparatus may include direct-current diode systems, radio frequency sputtering, magnetron sputtering, or ionized metal plasma sputtering. In alternative embodiments that use ALD, chemical precursors react with the surface of a material one at a time to deposit a thin film on the surface.

A dielectric layer **804** is deposited on the first metal layer **802** using any appropriate process including, e.g., CVD, PVD, or ALD. The dielectric layer **804** may be formed from any appropriate dielectric material, but is specifically contemplated as being a high-k dielectric material such as, e.g., hafnium dioxide, zirconium dioxide, aluminum oxide, tantalum oxide, and multilayers thereof. As used herein, the term “high-k” refers to a dielectric material having a dielectric constant k that is higher than that of silicon dioxide.

A second metal layer **806** is deposited on top of the dielectric layer **804**. It is specifically contemplated that the second metal layer **806** may be formed from, e.g., titanium nitride, although any other material may be used instead. It is furthermore contemplated that the second metal layer **806** will be formed from the same material as the first metal layer **802**, although in some embodiments these two materials may differ. The second metal layer **806** may be formed by any appropriate deposition process including, e.g., CVD, PVD, or ALD.

The first metal layer **802**, dielectric layer **804**, and second metal layer **806** are formed conformally over the topography of the surface. This vertical extension effectively increases the capacitance of the resulting capacitor without increasing the horizontal surface area consumed by the device. Because capacitance for a capacitor generally increases with increased surface area between two conductive plates, the topographical convolutions created by the cavities provide vertical surfaces for capacitance in addition to the horizontal surfaces.

Referring now to FIG. **9**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. A protective layer **904** is formed on the capacitor area and a mask **902** is formed over the protective **904**. In this case the same mask and material may be used as was used for the first mask **502**, but a developer of the opposite tone may be used (e.g., removing the unexposed region where the exposed region was removed in FIG. **5**, or removing the exposed region if the unexposed region was removed in FIG. **5**). The result is that the mask **902** is in the same location as the open capacitor area **504** formed by the first mask **502**.

The protective layer **904** protects the underlying portions of the MIM stack from damage during the definition of the mask **902** and the subsequent etching of the MIM stack outside of the area protected by the mask **902**. Thus the protective layer **904** may be any appropriate material that has etch selectivity with respect to the mask **902** and the second metal layer **806**.

Referring now to FIG. **10**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. The first metal layer **802**, dielectric layer **804**, and second metal layer **806** are etched away in the areas around the second mask **902**, leaving behind MIMCAP **1002**. Any appropriate anisotropic etch or combination of etches may be used to remove this material, said etches selectively removing the metal and dielectric layers without affecting the hardmask regions **402** or the underlying cap layer **106**.

Referring now to FIG. **11**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. The mask **902** is removed, leaving the hardmask **904** over the MIMCAP **1002**.

Referring now to FIG. **12**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. After the exposed surfaces are cleaned using, e.g., a wet clean, a layer of dielectric material **1202** is deposited over the MIMCAP **1002** and surrounding structures. The layer of dielectric material **1202** may be, e.g., a low-k dielectric material and may be the same material as the interlayer dielectric **102**. Any appropriate deposition process may be used to form the layer of dielectric material **1202** including, e.g., CVD, ALD, or PVD.

Once the layer of dielectric material **1202** is deposited, the top surface may be planarized using, e.g., chemical mechanical planarization (CMP). CMP is performed using, e.g., a chemical or granular slurry and mechanical force to gradually remove upper layers of the device. The slurry may be formulated to be unable to dissolve, for example, the work function metal layer material, resulting in the CMP process’s inability to proceed any farther than that layer.

Referring now to FIG. **13**, a cross-sectional diagram of a step in the fabrication of MIMCAP structures is shown. A new mask is used to pattern an opening in the layer of dielectric material **1202** and a contact **1302** is formed therein. The contact **1302** may be formed from any appropriate conductive material and may, in particular, be formed from the same material as the conductive contacts **104**. It should be understood that two masks are therefore used—a first mask that is used twice two define the capacitor area and a second mask that is used to define the top contact **1302**. No additional material is needed to change the topography that is provided by the cavities **602**.

It is to be understood that aspects of the present invention will be described in terms of a given illustrative architecture; however, other architectures, structures, substrate materials and process features and steps can be varied within the scope of aspects of the present invention.

It will also be understood that when an element such as a layer, region or substrate is referred to as being “on” or “over” another element, it can be directly on the other element or intervening elements can also be present. In contrast, when an element is referred to as being “directly on” or “directly over” another element, there are no intervening elements present. It will also be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements can be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

The present embodiments can include a design for an integrated circuit chip, which can be created in a graphical computer programming language, and stored in a computer storage medium (such as a disk, tape, physical hard drive, or virtual hard drive such as in a storage access network). If the designer does not fabricate chips or the photolithographic masks used to fabricate chips, the designer can transmit the resulting design by physical means (e.g., by providing a copy of the storage medium storing the design) or electronically (e.g., through the Internet) to such entities, directly or indirectly. The stored design is then converted into the appropriate format (e.g., GDSII) for the fabrication of photolithographic masks, which typically include multiple copies of the chip design in question that are to be formed on a wafer. The photolithographic masks are utilized to define areas of the wafer (and/or the layers thereon) to be etched or otherwise processed.

Methods as described herein can be used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case, the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case, the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

It should also be understood that material compounds will be described in terms of listed elements, e.g., SiGe. These compounds include different proportions of the elements within the compound, e.g., SiGe includes $Si_xGe_{1-x}$ where x is less than or equal to 1, etc. In addition, other elements can be included in the compound and still function in accordance with the present principles. The compounds with additional elements will be referred to herein as alloys.

Reference in the specification to "one embodiment" or "an embodiment", as well as other variations thereof, means that a particular feature, structure, characteristic, and so forth described in connection with the embodiment is included in at least one embodiment. Thus, the appearances of the phrase "in one embodiment" or "in an embodiment", as well any other variations, appearing in various places throughout the specification are not necessarily all referring to the same embodiment.

It is to be appreciated that the use of any of the following "/", "and/or", and "at least one of", for example, in the cases of "A/B", "A and/or B" and "at least one of A and B", is intended to encompass the selection of the first listed option (A) only, or the selection of the second listed option (B) only, or the selection of both options (A and B). As a further example, in the cases of "A, B, and/or C" and "at least one of A, B, and C", such phrasing is intended to encompass the selection of the first listed option (A) only, or the selection of the second listed option (B) only, or the selection of the third listed option (C) only, or the selection of the first and the second listed options (A and B) only, or the selection of the first and third listed options (A and C) only, or the selection of the second and third listed options (B and C) only, or the selection of all three options (A and B and C). This can be extended, as readily apparent by one of ordinary skill in this and related arts, for as many items listed.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of example embodiments. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes" and/or "including," when used herein, specify the presence of stated features, integers, steps, operations, elements and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components and/or groups thereof.

Spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, can be used herein for ease of description to describe one element's or feature's relationship to another element(s) or feature(s) as illustrated in the FIGS. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the FIGS. For example, if the device in the FIGS. is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the term "below" can encompass both an orientation of above and below. The device can be otherwise oriented (rotated 90 degrees or at other orientations), and the spatially relative descriptors used herein can be interpreted accordingly. In addition, it will also be understood that when a layer is referred to as being "between" two layers, it can be the only layer between the two layers, or one or more intervening layers can also be present.

It will be understood that, although the terms first, second, etc. can be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, a first element discussed below could be termed a second element without departing from the scope of the present concept.

Referring now to FIG. **14**, a method of forming a MIMCAP is shown. Block **1402** forms self-assembled nanoscale domains **204** and **206** over a hardmask layer **108** which, in turn, lies over a dielectric layer **102** with conductive contacts **104** embedded therein. The self-assembled domains **204** and **206** are formed by block copolymer chains having two blocks on each chain that comprise distinct chemical compositions. Upon annealing, the BCP molecules rearrange where like ends of different molecules form in groups, resulting in periodic structures.

Block **1404** etches away one of the copolymer materials. In particular, minority domain **206** is etched away, leaving the other material in place. Block **1405** transfers the resulting pattern to hardmask layer **108** to form hardmask regions **402**. The transfer of the pattern may be performed using an anisotropic etch that selectively removes material from the hardmask layer **108**.

Block **1406** forms mask **502** that defines capacitor area **504**. Block **1408** transfers the pattern in the exposed capacitor area **504** down into the dielectric layer **102**, exposing at least one conductive contact **104** and creating cavities **602**. Block **1410** removes the mask **502**.

Block **1412** forms the MIMCAP capacitor stack, including a first metal layer **802**, a dielectric layer **804**, and a second metal layer **806**. The capacitor stack is formed without patterning steps between layers, thereby minimizing plasma damage on the interfaces and improving device yield.

Block **1414** forms mask **902** over the capacitor area **504**, for example using the same lithographic mask as was used in block **1406** but with a developer of an opposite polarity. Block **1416** anisotropically etches away the layers of the capacitor stack outside of the capacitor area **504**. Block **1418** removes the mask **902**. After the capacitor **1002** is formed, block **1420** deposits a layer of dielectric material **1202**. The layer of dielectric material **1202** may be deposited by any appropriate process such as, e.g., CVD, ALD, or PVD, and then planarized using, e.g., CMP. Block **1422** forms an opening in the layer of dielectric material **1202** and hardmask **904** using, e.g., an appropriate mask and an anisotropic etch. Block **1422** then forms top contact **1302** in the opening to complete the capacitor.

Having described preferred embodiments of a system and method (which are intended to be illustrative and not limiting), it is noted that modifications and variations can be made by persons skilled in the art in light of the above teachings. It is therefore to be understood that changes may be made in the particular embodiments disclosed which are within the scope of the invention as outlined by the appended claims. Having thus described aspects of the invention, with the details and particularity required by the patent laws, what is claimed and desired protected by Letters Patent is set forth in the appended claims.

What is claimed is:

**1**. A capacitor, comprising:

a stack, comprising:

a first metallic layer formed over a substrate that comprises at least one high domain and at least one low domain, where a surface of the substrate in the at least one low domain has a height that is lower than a surface of the substrate in the at least one high domain;

an insulator formed over the first metallic layer; and

a second metallic layer formed over the insulator;

a bottom contact formed in the substrate having a top surface that is even with a top surface of the substrate in the at least one high domain; and

a cap layer formed directly on the substrate in the high domains, under the stack.

**2**. The capacitor of claim **1**, wherein the cap layer is absent over the low domains.

**3**. The capacitor of claim **1**, further comprising:

a protective layer formed over the stack; and

a dielectric layer formed over and around the protective layer and the stack.

**4**. The capacitor of claim **3**, further comprising a top contact that penetrates the dielectric layer and the protective layer to form an electrical contact with the top metallic layer.

**5**. The capacitor of claim **1**, wherein the first metallic layer has low domain with a bottom surface that is lower than a bottom surface of the bottom contact.

**6**. The capacitor of claim **1**, wherein the second metallic layer comprises a single-walled downward extension above a low domain.

**7**. The capacitor of claim **1**, wherein the first metallic region comprises a plurality of low regions, including a low region over the bottom contact and at least one additional low region.

**8**. A capacitor, comprising:

a stack, comprising:

a first metallic layer formed over a substrate that comprises at least one high domain and a plurality of low domains, where a surface of the substrate in the at least one low domain has a height that is lower than a surface of the substrate in the at least one high domain;

an insulator formed over the first metallic layer; and

a second metallic layer formed over the insulator;

a bottom contact formed in the substrate under a first low domain of the first metallic layer, having a top surface that is even with a top surface of the substrate in the at least one high domain; and

a cap layer formed directly on the substrate in the high domains, under the stack.

**9**. The capacitor of claim **8**, wherein the cap layer is absent over the low domains.

**10**. The capacitor of claim **8**, further comprising:

a protective layer formed over the stack; and

a dielectric layer formed over and around the protective layer and the stack.

**11**. The capacitor of claim **10**, further comprising a top contact that penetrates the dielectric layer and the protective layer to form an electrical contact with the top metallic layer.

**12**. The capacitor of claim **8**, wherein the first metallic layer has low domain with a bottom surface that is lower than a bottom surface of the bottom contact.

**13**. The capacitor of claim **8**, wherein the second metallic layer comprises a single-walled downward extension above a low domain.

**14**. A capacitor, comprising:

a stack, comprising:

a first metallic layer formed over a substrate that comprises at least one high domain and at least one low domain, where a surface of the substrate in the at least one low domain has a height that is lower than a surface of the substrate in the at least one high domain;

an insulator formed over the first metallic layer; and

a second metallic layer formed over the insulator;

a bottom contact formed in the substrate in electrical contact with the first metallic layer, having a top surface that is even with a top surface of the substrate in the at least one high domain;

a cap layer formed directly on the substrate in the high domains, under the stack;

a protective layer formed over the stack;

a dielectric layer formed over and around the protective layer and the stack; and

a top contact that penetrates the dielectric layer and the protective layer to form an electrical contact with the top metallic layer.

**15**. The capacitor of claim **14**, wherein the cap layer is absent over the low domains.

**16**. The capacitor of claim **14**, wherein the first metallic layer has low domain with a bottom surface that is lower than a bottom surface of the bottom contact.

**17**. The capacitor of claim **14**, wherein the second metallic layer comprises a single-walled downward extension above a low domain.

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