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(54) **HIERARCHICALLY ELABORATED PHASED-ARRAY ANTENNA MODULES AND METHOD OF OPERATION**

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H01Q 3/34	(2006.01)
H01Q 3/26	(2006.01)

(52) **U.S. Cl.**

CPC ***H01Q 3/34*** (2013.01); ***H01Q 3/2605*** (2013.01); ***H01Q 3/2629*** (2013.01); ***H01Q 21/0025*** (2013.01)

(58) **Field of Classification Search**

CPC H01Q 21/0006; H01Q 21/0025; H01Q 3/2605; H01Q 3/2629; H01Q 3/34

USPC 342/361, 368, 372, 373; 375/316, 319

See application file for complete search history.

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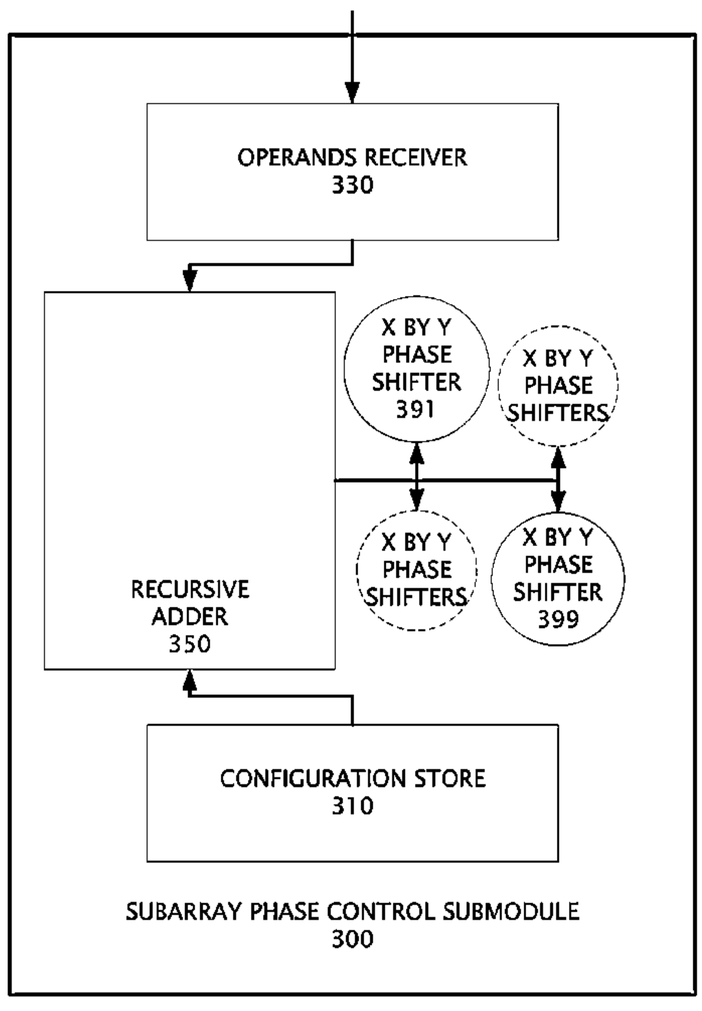
(57) **ABSTRACT**

A phased-array antenna panel has front end modules mounted on a Printed Circuit Board (PCB). Several phased-array processing die, transform phase and gain according to a register array in an RFIC on the PCB. The register array are grouped into a local register group and a global register group. Each set of local registers control an individual antenna element and a global register group controls overall RFIC function. The apparatus elaborates phase shift weights into a submodule of a phased-array antenna system. Each submodule determines its own base phase shift weight per its unique location and configuration to accelerate antenna beam direction changes.

7 Claims, 7 Drawing Sheets



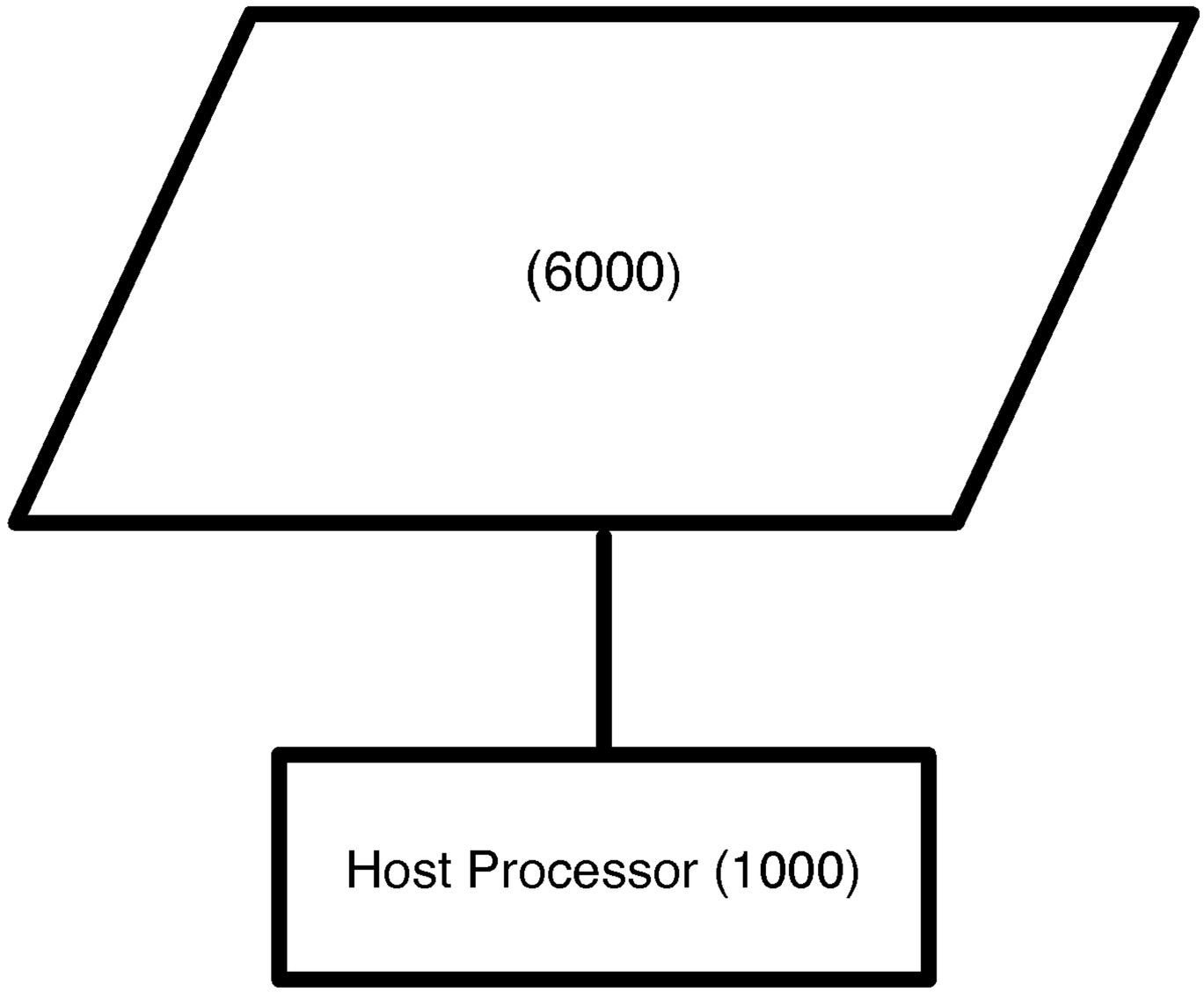


FIG.1

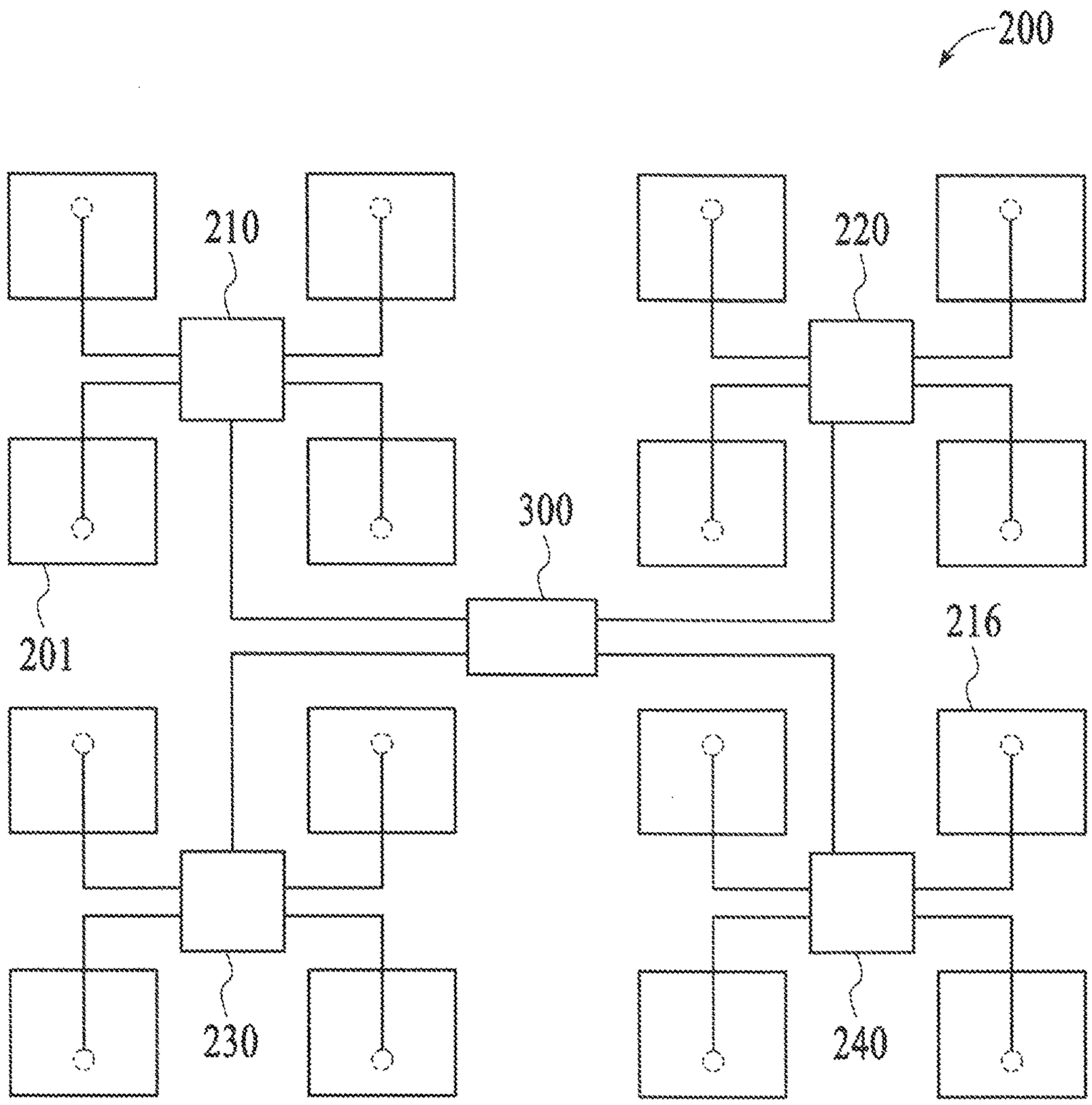


FIG. 2

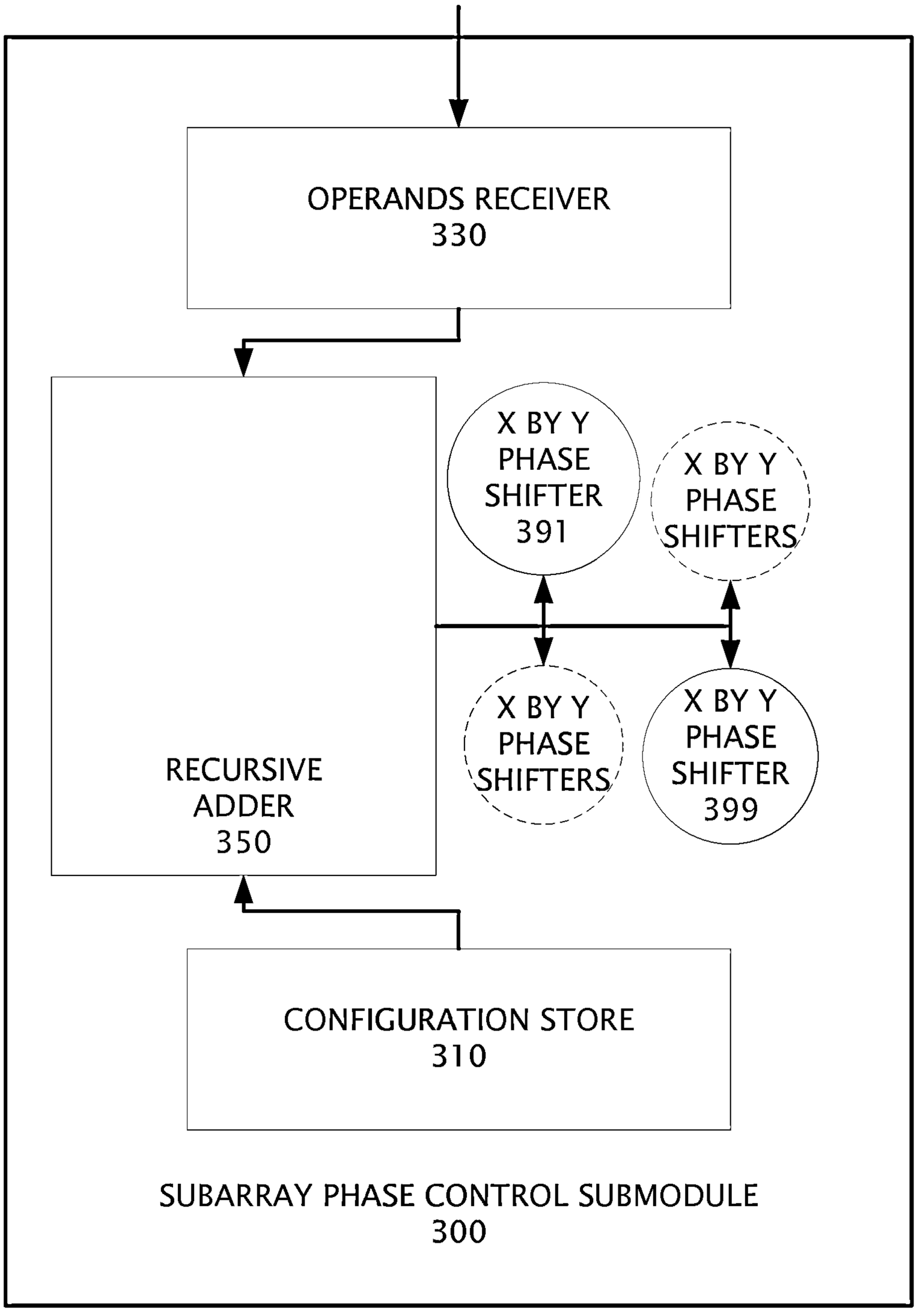

OPERANDS RECEIVER
330
RECURSIVE
ADDER
350
X BY Y
PHASE
SHIFTER
391
X BY Y
PHASE
SHIFTERS
X BY Y
PHASE
SHIFTERS
X BY Y
PHASE
SHIFTER
399
CONFIGURATION STORE
310
SUBARRAY PHASE CONTROL SUBMODULE
300

FIG 3

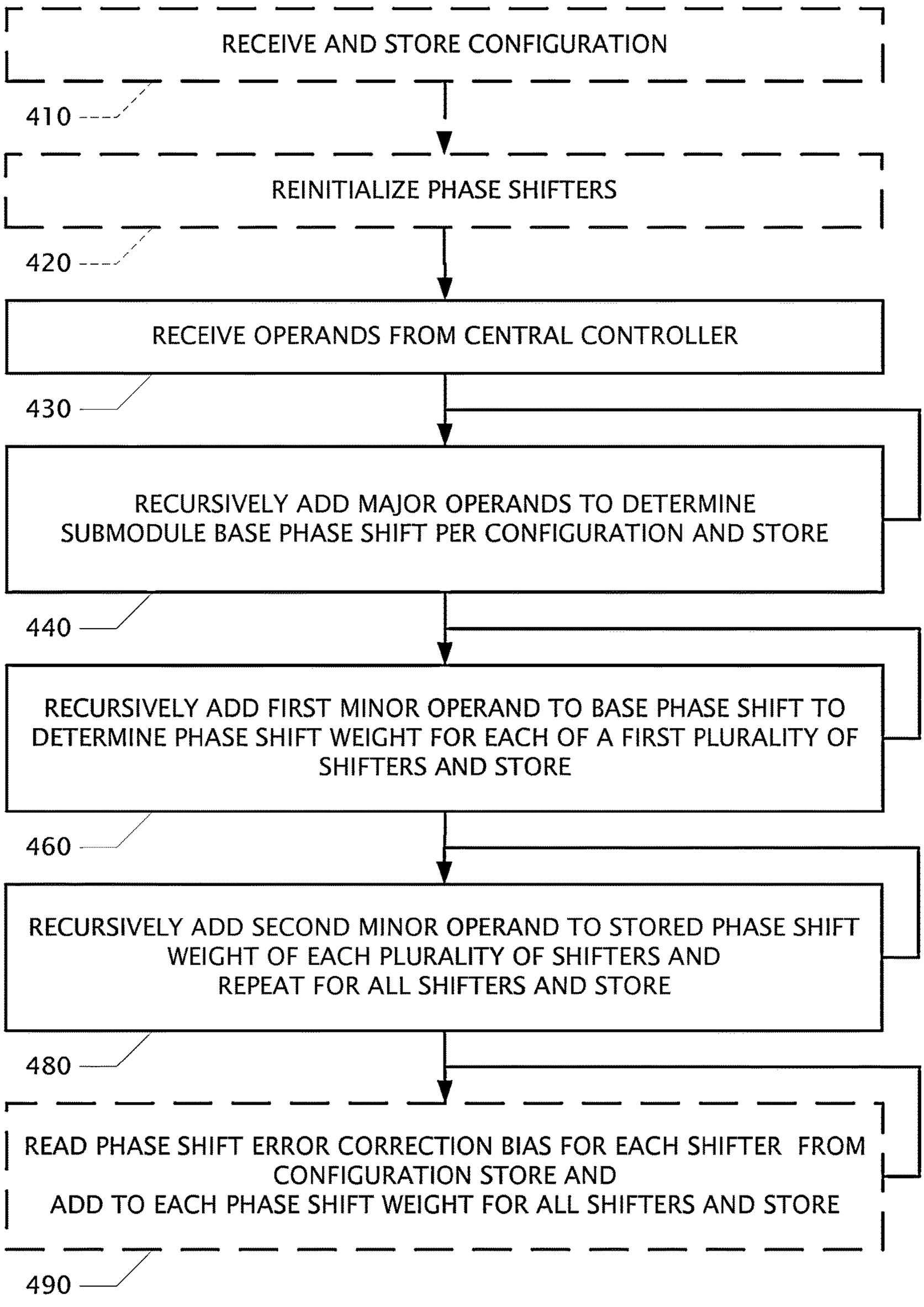

RECEIVE AND STORE CONFIGURATION
410
REINITIALIZE PHASE SHIFTERS
420
RECEIVE OPERANDS FROM CENTRAL CONTROLLER
430
RECURSIVELY ADD MAJOR OPERANDS TO DETERMINE SUBMODULE BASE PHASE SHIFT PER CONFIGURATION AND STORE
440
RECURSIVELY ADD FIRST MINOR OPERAND TO BASE PHASE SHIFT TO DETERMINE PHASE SHIFT WEIGHT FOR EACH OF A FIRST PLURALITY OF SHIFTERS AND STORE
460
RECURSIVELY ADD SECOND MINOR OPERAND TO STORED PHASE SHIFT WEIGHT OF EACH PLURALITY OF SHIFTERS AND REPEAT FOR ALL SHIFTERS AND STORE
480
READ PHASE SHIFT ERROR CORRECTION BIAS FOR EACH SHIFTER FROM CONFIGURATION STORE AND ADD TO EACH PHASE SHIFT WEIGHT FOR ALL SHIFTERS AND STORE
490

FIG 4

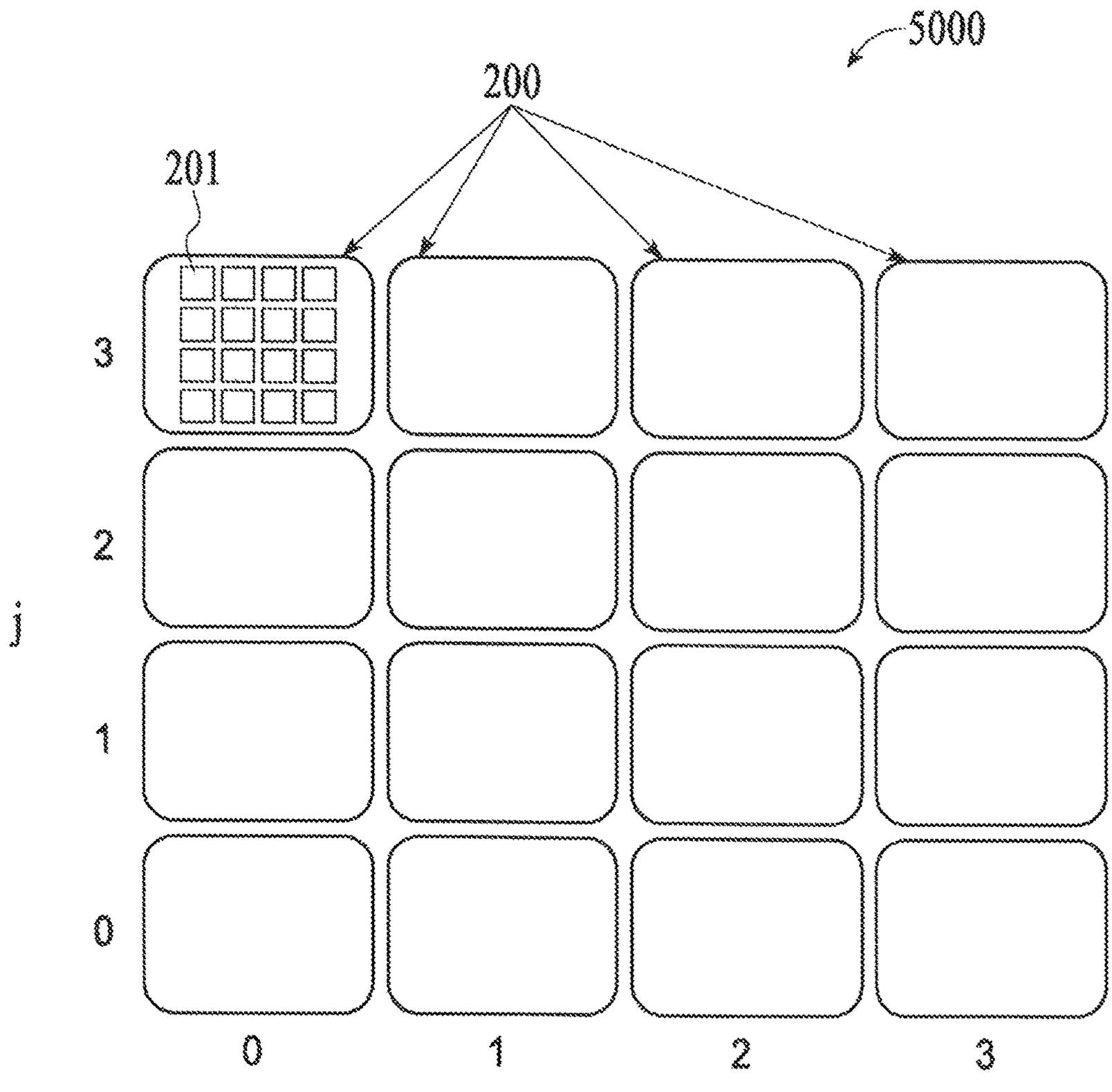


FIG. 5A

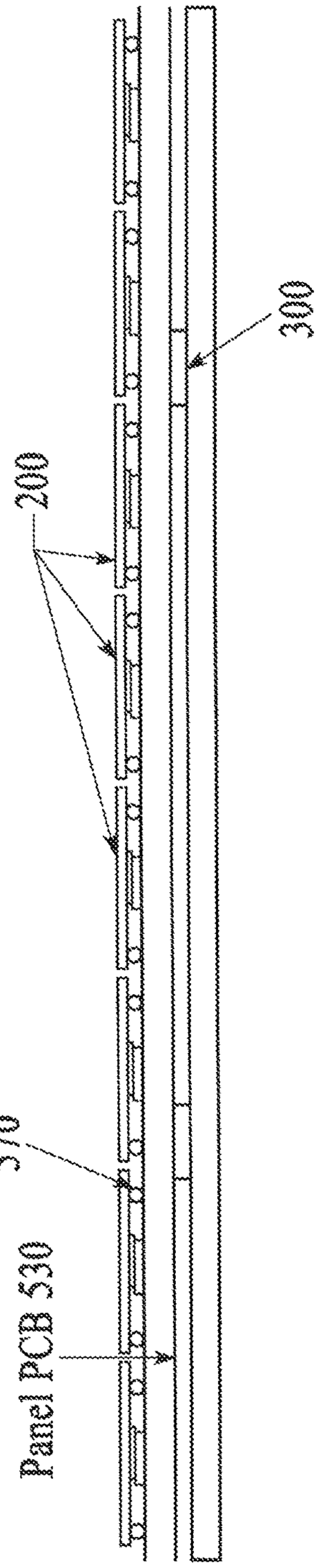


FIG. 5B

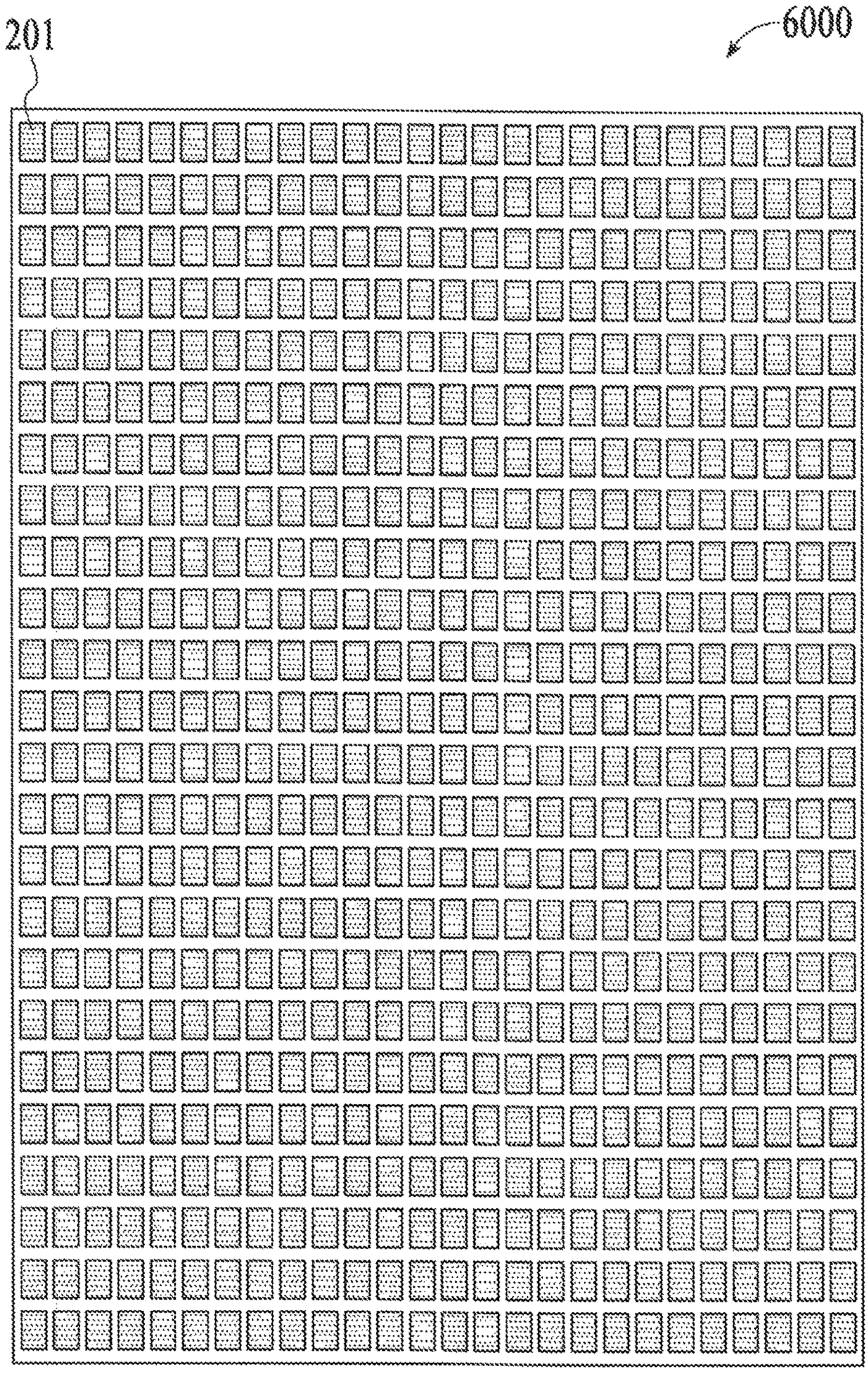


FIG. 6

HIERARCHICALLY ELABORATED PHASED-ARRAY ANTENNA MODULES AND METHOD OF OPERATION

RELATED APPLICATIONS

Applicants claim priority from provisional application 61/757,688 Efficient Phase Shift Control Apparatus and Method for Hierarchically Distributed Elaboration Within a Phased Array Antenna filed 28 Jan. 2013 which is incorporated by reference in its entirety.

BACKGROUND

A conventional phased-array antenna enables a highly directive antenna beam to be steered toward a single certain direction. The direction of an antenna beam may be controlled by setting the phase shifts of each of the antenna elements in the array. However, to enable higher mobility, the phase shifts must be updated more quickly than conventionally practiced. In addition, cost and space considerations eliminate the obvious deployment of parallel data buses. Thus it can be appreciated that what is needed is a more efficient way of dissemination of the phase shift control information to a substantial number of phase shifters for an antenna array with a high number of antenna elements and possibly more than one simultaneous target.

SUMMARY OF THE INVENTION

An efficient phase control scheme for a phased-array antenna consisting of a number of small submodules (subarrays) is disclosed. Each submodule (subarray) has a digital interface and contains a number of antenna elements and the associated phase shifters. The disclosed phase control scheme requires dissemination of minimum amount of phase control information to the submodules.

A serial bus is used to disseminate the phase shift control information. The serial bus has the advantages of simplicity and reduced volume, routing, and cost over a conventional parallel bus. This is especially true for a phased-array antenna with high number of antenna elements. Minimizing the distribution of information enables a substantially lower bus speed and cost.

An array of registers local to each antenna element of a phased-array antenna contains phase shifter and gain equalizer values. Receiving an address, position, or location within the register array from a directional beam controller determines a beam direction. These values can be preloaded and a specific set of phase shifter and gain equalizer values corresponding to a beam direction indicated by disseminating a pointer. Alternatively, a digital functional logic circuit for each antenna element can determine the required phase shift on the fly by receiving a phase increment broadcast to every antenna element.

An apparatus is configured to efficiently elaborate phase shift weights into a submodule of a phased-array antenna system. Each subarray phase control submodule is uniquely configured to receive and elaborate weights for a submodule of elements to control phase shifters. Major operators and minor operators are received and transformed by an apparatus coupled to a phased-array antenna suitable for a high mobility device. Each submodule determines its own base phase shift weight per its unique configuration. A recursive adder or multiplier applies phase increments to direct an antenna beam by controlling elements within an array subset.

A phased-array antenna panel is constructed from building blocks. These are a plurality of front end modules, mounted to a Printed Circuit Board (PCB).

Each front end module has a plurality of antenna elements coupled to a frontend die. The frontend die is coupled to a phased-array processing die. The antenna elements are embedded in the top of a substrate and the frontend dies and the phased-array processing die are flip-chip mounted onto the bottom layer of substrate. Input or output signals are conducted through the substrate to the PCB.

A customized and customizable Radio Frequency Integrated Circuit (RFIC) device includes: phased-array processing blocks; phase-shifters, combiners, splitters, gain equalizers, buffer amplifiers, and a digital signal control and interface circuit.

Each digital signal control and interface circuit has at least one global/individual indicator pad and a plurality of individual die address setting pads enabling a first die address to be configured at a first location on the PCB which connects a plurality of die address pads to a first combination of logic high or logic low and a second die address to be configured at a second location on the PCB which connects a plurality of die address pads to a second combination of logic high or logic low whereby registers within the RFIC are assigned unique addresses.

Tying the front end modules together is a PCB comprising a data and address bus; a plurality of die address pads; and a global die selection pad and a transfer format mode pad.

A register array in each RFIC is grouped into a local register group and a global register group, the local registers physically places close in proximity to RF chains which each correspond to an element of array antenna, whereby each set of local registers control an individual antenna element and a global register controlling overall RFIC function.

The system provides several choices for configuring the antenna array. A lookup method determines antenna element phase and gain settings from storage and a computation method determines antenna element phase and gain settings. They may be used separately or combined for corner cases.

The method of operation for the apparatus includes several alternatives explicated below for controlling slave RFIC devices in an antenna array.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the detailed disclosure below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

BRIEF DESCRIPTION OF FIGURES

The purpose of the accompanying figures is to aid in the appreciation of the subject matter without clutter or limitation. While the illustrations of 2 by 2, 4 by 4, or 16 element modules are intended to support the understanding of the reader, it can be appreciated that the disclosed economies are even greater for a much larger array of modules and submodules. Thus the discussion and claims are not limited to the values or numbers of elements shown wherein:

FIG. **1** is a system diagram of an antenna element array controlled by a host processor.

FIG. **2** is an electrical schematic of antenna elements, amplifiers, and a phase control circuit communicatively coupled.

FIG. **3** is a block diagram of a subarray phase control submodule.

FIG. **4** is a flow chart of method steps to operate a phase control circuit device.

FIG. **5**A is a radiating surface view of an array of front end modules mounted on a phased-array antenna panel.

FIG. **5**B is an edge or side view of an array of front and modules mounted on a phased array antenna panel.

FIG. **6** is a radiating surface view of the antenna elements of a plurality of front end modules mounted on a phased-array antenna panel.

DETAILED DISCLOSURE OF EMBODIMENTS

A phased-array antenna panel shown in FIG. **5**B is constructed from building blocks. These are a plurality of front end modules **200**, Ball Grid Array(BGA)-mounted to a main PANEL Printed Circuit Board (PCB) **530**. A phased-array antenna allows a highly directive antenna beam to be steered toward a variable target direction in any mobile situation. The direction of the antenna beam is adjusted by resetting the phase shifts of the antenna elements. To enable high mobility, the phase shifts need to be updated quickly. Thus, Applicants' efficient way of dissemination of the phase shift control information to the phase shifters of the antenna elements addresses a long sought need.

Each front end module **200** of FIG. **2** has a plurality of antenna elements **201-216** coupled to a frontend die **210-240** in best mode using GaAs. The frontend die is coupled to a phased-array processing die **300** economically manufactured in CMOS. The antenna elements are embedded in the top of a substrate and the frontend dies and the phased-array processing die are flip-chip mounted onto the bottom layer of substrate of each front end module. Input or output signals are conducted through the substrate to the phased-array processing die and to passive combiners and splitters embedded in the PCB; and a transceiver die **300** flip-chip mounted on the PANEL PCB whereby the antenna transmitted and received signals are frequency translated.

An apparatus/article of manufacture aspect of the invention is a customized and customizable Radio Frequency Integrated Circuit (RFIC) device comprising: phased-array processing blocks; phase-shifters, combiners, splitters, gain equalizers, buffer amplifiers, and a digital signal control and interface circuit.

The digital signal control and interface circuit has at least one global/individual indicator pad and a plurality of individual die address setting pads enabling a first die address to be configured at a first location on the PCB which connects a plurality of die address pads **570** to a first combination of logic high or logic low and a second die address to be configured at a second location on the PCB which connects a plurality of die address pads to a second combination of logic high or logic low whereby registers within the RFIC are assigned unique addresses.

Tying the front end modules together is a PCB comprising a data and address bus; a plurality of die address pads; and a global die selection pad and a transfer format mode pad. In order to scale, a driver is disclosed in an embodiment, which buffers the bus output; the bus coupling a microcontroller master device and coupling a plurality of slave devices on each RFIC.

A register array in each RFIC is grouped into a local register group and a global register group, the local registers physically placed close in proximity to RF chains which each correspond to an element of array antenna, whereby each set of local registers control an individual antenna element and a global register controls overall RFIC function.

The system provides several choices for configuring an antenna array. A lookup method determines antenna element phase and gain settings from storage and a computation method determines antenna element phase and gain settings. They may be used separately, simultaneously in parallel, or combined for corner cases.

The method of operation for the apparatus includes several alternatives for controlling slave RFIC devices in an antenna array. These include initializing common registers with calibrated gain values; storing phase shifter values in local registers; computing phase shifter values; and looking up gain settings.

To illustrate the scheme, consider an exemplary submodule **5000** of 4×4 elements **200** using 4 bit phase shifters for a planar array in two dimensions. The extension to three dimensional array is conceptually straightforward for those well versed in the art of phased array design. The extension from Cartesian to Spherical Coordinate for the element layout is also routine. For the purpose of simplicity we use the planar example. The elements are indexed as shown in FIG. **5**A.

The phase increments required for pointing are Δx and Δy. Let the phase of element (0,0) be ϕ_{00}. Then

a. $\phi_{xy}=\phi_{00}+x\cdot\Delta x+y\cdot\Delta y$.

Multiplying a phase increment by an integer may be expensive in one technology and less significant in another implementation. The method of the invention is the multiplication of phase increments which have been distributed to the submodules. In one preferred embodiment which avoids literal multiplication by integer, it can be computed recursively:

Compute first row: $\phi_{x+1,0}=\phi_{x0}+\Delta x$ (3 adds)

Compute the next rows: $\phi_{x,y+1}=\phi_{x,y}+\Delta y$ (12 adds)

To avoid quantization errors in the computation, the phases used in computation are represented in finer increments, e.g. 6 bits. The exact number of bits enable embodiments to accommodate different quality requirements. After computation, the phases can be rounded off to lesser resolution.

Advantageously, the non-conventional central controller (digital signal processor) of the phased-array antenna only needs to send the ϕ_{00}, Δx, Δy to the submodule for each steering direction. In an illustrative embodiment, the number of bits required per submodule is 3×6 bits. The number of additions is 15.

In one embodiment, wherein the number of submodule is large, a large volume of phase control information would need to be disseminated to all the submodules. A non-conventional second level of hierarchy illustrated in FIG. **5**A is introduced by this invention to enable massive scaling.

If the submodules are arranged in the planar rectangular grid, each with i, j indices (e.g. 0, 1, 2, 3 . . .) corresponding to the position in the two orthogonal axes, for the phased-array antenna, the initial phase $\phi_{00}[i,j]$ of the $[i,j]^{th}$ submodule **201**, is computed as follows.

a. $\phi_{xy}[i,j]=\phi_{00}[i,j]+x\cdot\Delta x+y\cdot\Delta y$.

b. $\phi_{xy}[i,j]=\phi_{00}[0,0]+i\cdot\Delta x'+j\cdot\Delta y'+x\cdot\Delta x+y\cdot\Delta y$.

c. In an embodiment, a set of fixed offsets ($\phi_{fixed\ x,y}[i,j]$) are added to the equation to account for any fixed phase offset (delay) offset for each antenna element in the implementation. And such fixed offsets do not need to be updated everytime and the $\phi_{00}[0,0]$ value can be absorbed into $\phi_{fixed\ x,y}[i,j]$.

d. $\phi_{xy}[i,j]=\phi_{fixed\ x,y}[i,j]+i\cdot\Delta x'+j\cdot\Delta y'+x\cdot\Delta x+y\cdot\Delta y$.

The principle of operation of the invention is to multiply a phase increment by an integer. Embodiments of the invention may be more expensive in some technologies than

in other embodiments of the invention. In one preferred embodiment which avoids use of a multiplier circuit, phase increment is computed recursively:

Computing first row: $\phi_{00}[i+1,0]=\phi_{00}[i,0]+\Delta x'$

Computing the next rows: $\phi_{0,0}[i,j+1]=\phi_{0,0}[i,j]+\Delta y'$

Because the antenna steering remains unchanged if the phase shifts of all antenna elements are added the same amount of phase shift, the initial phase $\phi_{00}[0,0]$ can be set to zero. Therefore, the phase control information, Δx, Δy, $\Delta x'$, $\Delta y'$, to be disseminated to all the submodules is independent of the number of submodules. This bears emphasis and elaboration. Even if the number of submodules is 1024 or 512 instead of 16, there are only four operands which need to be disseminated to all of the submodules. The present invention is easily distinguished from conventional phased antenna array control by the substantially lower bandwidth requirement to distribute phase information into the shift circuits. Both lower data rates and higher phase data uploads are accomplished with less cost. The invention reduces bus speed or increases beam direction change rapidity or both.

One preferred embodiment for realizing the indexing of submodules is to provide address pins for the two orthogonal axes. Each address pin would be tied to logic high or logic low based on the indices: i and j.

Referring to FIG. **3**, a non-limiting illustration of an apparatus embodiment of the subject matter is provided to facilitate appreciation of the invention. Each one of a plurality of subarray phase control submodules **300** comprises a configuration store **310** communicatively coupled to a recursive adder **350**. At minimum the configuration store is no more than the value of i and the value of j representing the position of the subarray phase control submodule within a flat rectangular grid. This may be accomplished by a memory, fuses, or pins tied to logic one or zero. In an embodiment, the configuration store further has a set of correction phase errors for each antenna element or phase shifter.

The recursive adder **350** is further coupled to each of a plurality of x by y phase shifter circuits **391-399** which control an antenna beam direction by each shifting the phase of an antenna element (not shown) by a multiple of phase increments. An operands receiver **330** is communicatively coupled to an external central controller and to the recursive adder **350**. In an embodiment, a single major operand is the base phase shift for a submodule. In an embodiment, a pair of major operands is received and used in combination with the configuration stored data to determine a base phase shift for the entire submodule. In an embodiment, a pair of minor operands is received and used as phase increments in determining each individual array element's phase shift weight.

Referring to FIG. **4**, a method for operating an exemplary system such as illustrated in FIG. **3** is disclosed. Each submodule receives a plurality of operands from a central controller **430**. Advantageously, the disclosed subject matter enables a low cost serial bus to disseminate the phase shift control information. In an embodiment, only four operands are required and may be shared among many submodules. Each submodule has either stored or hardwired a configuration which reflects its unique position within an array. In an embodiment this is a value for i and a value for j within a planar rectangular grid. An alternative embodiment could use a polar coordinate system. Two of the operands distributed to many or all of the submodules are major operands. One or both are recursively added to determine and store a base phase shift for the submodule **440**. In an embodiment the number of additions is related to the values of i and j. Thus the determination of the base phase shift for each submodule is done in parallel at the submodule itself and central controller performs a broadcast transmission to many if not all submodules.

Each subarray phase control submodule **300** having determined its own base phase shift, the recursive adder then recursively adds a first minor operand to the base phase shift to determine a phase shift weight for each of a first plurality of shifters and stores the result **460**. This can be thought of as determining a phase weight vector for a row (or a column) by adding a phase increment once, twice, or thrice and so forth for index 1, 2, 3, etc.

Each subarray phase control submodule **300** having determined a phase weight vector, the recursive adder then recursively adds a second minor operand to the stored phase shift weight of each plurality of shifters **480**. In other words the second phase increment is added once, twice, or thrice to the vector to determine phase shift weights for the full array.

Again, each submodule is operating in parallel with each other submodule and only performing additions. In an embodiment, a multiplexor can perform shifting if area and speed are improved but this is an implementation optimization. In an embodiment the major and minor operands may be transmitted separately by the central controller or all in one transmission. In embodiments self-clocking may control computation and storage and in another a clock.

Referring again to FIG. **4**, in an embodiment, it may be advantageous to reinitialize the weights of the phase shifters prior to the previously disclosed steps **420**. Or it may be sufficient to overwrite selected phase shift weights as each one is determined. In an embodiment, the manufacture and assembly of the antenna array may determine the i and j indexing of each submodule of the array or they may be stored into programmable memory **410**. One embodiment for realizing the indexing of submodules is to provide address pins for the two orthogonal axes. Each address pin may be tied to a logic high or logic low based on the indices: i and J. Sockets for the submodules may be soldered into the substrate according to the indices. Even floating gates, wirebonding, switches or jumpers may be a cost effective embodiments. Resistive fuses may be blown to tie address pads for each die to a unique address value at each location on the PCB.

In an embodiment, a phase shift error correction bias is stored into the configuration for each shifter **410**. To mitigate phase errors in the implementation, a set of phase shift error correction bias values can be added into a configuration store within each submodule, in an embodiment, during configuration **410**. Optionally, in that embodiment, a further process is to read phase shift error correction base for each shifter from configuration store and to add to each phase shift weight for all shifters and to store **490**.

In other words, to compensate the phase errors in the implementation, a set of correction phase errors $\Delta\phi_{xy}$ can be pre-stored inside the registers within the submodules. The correction phase errors $\Delta\phi_{xy}$ can be obtained via calibration procedure in the lab or production process. The phase shift to be applied to each antenna element would be $\Delta\phi_{xy}+\phi_{xy}$. Note that $\Delta\phi_{xy}$ does not change with different steering angles, but could be a function of temperature and other factors.

In an embodiment the apparatus and method is extended into a 3 dimensional phased-array which comprises operands Δx, Δy, Δz, $\Delta x'$, $\Delta y'$, $\Delta z'$.

For clarity of exposition, an illustrative non-limiting embodiment of the subject invention is first provided:

Each antenna element of a phased-array antenna has a local antenna weight vector table which contains phase shifter and gain equalizer values. An beam controller transmits a location, position, or address of a register in which the antenna weight vector table is stored to control each antenna element. The antenna element further has a digital functional logic circuit configured to generate required phase shifts into the registers of each element.

Two possible approaches for setting the phase shifter and gain equalizer values in the RF chain are described first. In approach 1, the phased-array beam is formed by loading each antenna element with specific phase shifter setting value (and gain equalizer setting value) from an antenna weight vector table. The antenna weight vector table contains a set of antenna weight vectors, in an embodiment, sixty-four (64). Each weight vector contains a set of phase shifter settings for all antenna elements. A table of phase shifter settings, (again e.g. 64) is stored in the local registers for each RF circuit chain corresponding to an antenna element. The antenna weight vector table consists of these local phase shifter registers. The values of phase shifter setting are pre-stored in the antenna weight vector table of each die and be used for pointing various beam directions, in this embodiment up to 64, typically, covering the vicinity of a particular beam direction in discretely chosen settings. The resolution of these discretely settings are chosen from system level study. Once the weight table is loaded, the host processor only needs to select which position in the antenna weight vector table to be used for the phase shifters. A specific position within the antenna weight vector table stores the antenna weight corresponding to a beam direction. The preferred embodiment uses a common register to store the address pointer of the position in the antenna weight vector table. The distribution of register addresses (via address pointer) rather than conventional antenna weights improves the antenna beam transition movement speed within the beam directional range covered by the antenna weight vector table. Note that only a single address pointer is disseminated for all the RFIC dies within the phased-array antenna for a beam direction.

However, when the beam direction is outside of the directional range covered by the stored antenna weight vector table, a new antenna weight vector table would need to be loaded. There might be some delay in loading the new table. This is especially true for a phased-array antenna with high number of antenna elements. To enable improved higher mobility, the phase shifts need to be updated quickly. Thus, it can be appreciated that a more efficient dissemination of the phase shift control information to the phase shifters of the antenna elements is needed.

Note that the antenna weight table values can be obtained through calibration of antenna beam in the laboratory. This allows correction of any anomaly in the phase shifter and equalizer values.

We further disclose a second approach for fast loading of the phase shifter setting by employing a plurality of digital functional logic circuits to generate in parallel each required phase shift on-the-fly. In an embodiment wherein the antenna elements are placed linearly in a x and y directional rectangular grid on a plane, the phase shift of the corner element (0,0) is represented as ϕ_{00} and the phase increment in the required for x direction and y direction are Δx and Δy, respectively. The phase shift for the (n_x, n_y) element on the rectangular grid can be represented as

$$\phi_{xy}=\phi_{00}+n_x\cdot\Delta x+n_y\cdot\Delta y.$$

When the index (n_x, n_y) for the antenna element maps to the address of the registers, the invention provides that only the Δx and Δy needs to be passed to each digital functional logic circuit to determine the phase shift. Note that the phase shifter setting has limited quantization. So, the actual phase shifter value for each (n_x, n_y) element is

$$\text{Quan}[\phi_{xy}]=\text{Quan}[\phi_{00}+n_x\cdot\Delta x+n_y\cdot\Delta y.]$$

Given that in actual silicon implementation, the phase shifter value will need to be corrected by some fixed offset Δ n_x, n_y, the phase shifter value to be used should be

$$\text{Quan}[\phi_{xy}]=\text{Quan}[\phi_{00}+n_x\cdot\Delta x+n_y.\Delta y.+\Delta n_x,n_y]$$

To generalize the subject matter of the invention, the application discloses two approaches for setting the phase shifter and gain equalizer values in the RF chain. In applicant's approach 1, the phased-array beam is formed by loading each antenna element with specific phase shifter setting value (and gain equalizer setting value) from an antenna weight vector table. The antenna weight vector table contains a set of V antenna weight vectors. In an embodiment, the integer value of V is within the range 16-512. However, as storage densities continue to improve geometrically, the number of antenna weight vectors may be multiplied. Each weight vector contains a set of phase shifter settings for all antenna elements. A table of V phase shifter settings is stored in the local registers for each RF circuit chain corresponding to an antenna element. The antenna weight vector table consists of these local phase shifter registers. The values of phase shifter setting are pre-stored in the antenna weight vector table of each die and be used for pointing up to V beam directions, typically, covering the vicinity of a particular beam direction in discretely chosen settings. The resolution of these discretely settings are chosen from system level study. Once the weight table is loaded, the host processor only needs to select which position in the antenna weight vector table to be used for the phase shifters. The address pointer is used for the selection of position in the antenna weight vector table. Since all the RFIC dies are loaded with the antenna weight vector table corresponding to V beam directions, dissemination of a single address pointer would update the beam direction. This speeds up the antenna beam transition movement within the beam directional range covered by the antenna weight vector table.

However, when a desired beam direction is outside of the directional range covered by the stored antenna weight vector table, new antenna weight vector table values need to be loaded. Any delay in loading the new table, especially for a phased-array antenna with high number of antenna elements will degrade the useful mobility of the antenna. Thus, it can be appreciated that what is needed is a more efficient dissemination of the phase shift control information to the phase shifters of the antenna elements. As mentioned above, the antenna weight table values can be obtained through calibration of antenna beam in the laboratory which allows correction of any anomaly in the phase shifter and equalizer values.

A second general approach for fast loading of the phase shifter setting is to employ a plurality of digital functional logic circuits to generate the required phase shift values in parallel on-the-fly. In an embodiment wherein the antenna elements are placed linearly in an x, y and z orthogonal array the phase shift of the corner element (0,0,0) is represented as ϕ_{000} and the phase increment in the required are Δx, Δy, and Δz, respectively. The phase shift for the (n_x, n_y) element on the rectangular grid can be represented as

$$\phi_{xyz}=\phi_{000}+n_x\cdot\Delta x+n_y\cdot\Delta y+n_z\cdot\Delta z.$$

The index (n_x, n_y, n_z) for the antenna element reflects the address of the registers. Note that the only the phase increments need be broadcast to every digital functional logic circuit to generate the phase shift. As before, the phase shifter setting has limited quantization and will need to be corrected by some fixed offset in each dimension.

The invention further comprises combining approaches 1 & 2. In a condition when the beam direction is outside of the directional range covered by the antenna weight vector table per approach 1, the new antenna table can be computed via approach 2 to minimize the data transfer requirement between the central controller and the local modules.

A method for operating a phased-array antenna has the steps: receiving from a host processor a position in an antenna weight vector table; reading phase shifter and gain equalizer values from said position in the antenna weight vector table; and pointing a beam by controlling a phase shifter and gain equalizer according to said read values.

An other method for operating a phased-array antenna has the steps: at an antenna element of a phased-array antenna, receiving a phase increment for each orthogonal direction; determining a phase shift for the antenna element according to its index and the phase shift of its corner element; adding a fixed offset to correct the phase shifter value for an anomaly; and storing the phase shift into a position of an antenna weight vector table.

An apparatus embodiment of the invention shown in FIG. **1** is a plurality of antenna elements **6000** communicatively coupled to a host processor **1000** whereby phase increments or addresses, positions, or locations within an antenna weight vector table may be distributed to every antenna element, wherein each antenna element comprises a phase shifter and gain equalizer coupled to a plurality of local registers which contain an antenna weight vector table.

In an embodiment, the method includes having previously stored the condition that the antenna is currently operating in a given region R, the host processor determines the region that the antenna will be pointing next R+1; the host processor determines that the region is adequately covered by one of the set of d phase weights previously associated with d directions for each element according to a content addressable memory store device wherein the phase weights are computed using the element index and the Submodule index:

For each submodule of 4×4 elements using 4 bit phase shifters, the elements indexed as follows: the phase increments required for pointing are Δx and Δy; set the phase of element (0,0) to be $\phi 00$ and $\phi xy=\phi 00+x\cdot\Delta x+y\cdot\Delta y$; as the submodules are arranged in the planar rectangular grid, each with i, j indices corresponding to the position in the two orthogonal axes, for the phased-array antenna, the initial phase $\phi 00[i,j]$ of the [i,j]th submodule, is computed as $\phi xy[i,j]=\phi 00[i,j]+x\cdot\Delta x+y\cdot\Delta y$ and $\phi xy[i,j]=\phi 00[0,0]+i\cdot\Delta x'+j\cdot\Delta y'+x\cdot\Delta x+y\cdot\Delta y$; the host processor transmits to the Submodules an instruction to load phase weight set d=5 (for example) to the phase shifters on the condition that the phase weight set for direction d has not been overwritten at each submodule.

An apparatus embodiment of the invention further includes a functional digital logic circuit coupled to the phase shifter, the gain equalizer, and the plurality of local registers configured to receive one or more phase increment, determine a phase shift for the antenna element, correct the phase shift by a fixed offset, and store into a location of an antenna weight vector table or load the antenna element with the resulting phase shifter setting value and gain equalizer setting value.

One aspect of the invention is a phased-array antenna panel comprising: a plurality of front end modules, Ball Grid Array(BGA)-mounted to a main PANEL Printed Circuit Board (PCB); the main PANEL PCB; each front end module including a plurality of antenna elements; the antenna element coupled to a frontend die; the frontend die coupled to a phased-array processing die; wherein the antenna elements are embedded in the top of a substrate and the frontend dies and the phased-array processing die are flip-chip mounted onto the bottom layer of substrate of each front end module whereby input or output signals are conducted through the substrate to the phased-array processing die and to passive combiners and splitters embedded in the PANEL PCB; and a transceiver die flip-chip mounted on the PANEL PCB whereby the antenna transmitted and received signals are frequency translated.

Another aspect of the invention is a Radio Frequency Integrated Circuit (RFIC) device which includes: phased-array processing blocks; phase-shifters, combiners, splitters, gain equalizers, buffer amplifiers, and a digital signal control and interface circuit; which interface circuit has at least one global/individual indicator pad and a plurality of individual die address setting pads enabling a first die address to be configured at a first location on the PCB which connects a plurality of die address pads to a first combination of logic high or logic low and a second die address to be configured at a second location on the PCB which connects a plurality of die address pads to a second combination of logic high or logic low whereby registers within the RFIC are assigned unique addresses.

The invention is has a PCB with a data and address bus, a plurality of die address pads, a global die selection pad, and a transfer format mode pad.

In an embodiment for improved scaling the apparatus has a driver to buffer the bus output; the bus coupling a microcontroller master device and coupling a plurality of slave devices on each RFIC.

Another aspect of the invention is a register array in each RFIC grouped into a local register group and a global register group, the local registers physically places close in proximity to RF chains which each correspond to an element of array antenna, whereby each set of local registers control an individual antenna element and a global register controlling overall RFIC function;

Another aspect of the invention is a method for operation of the invention which offers a plurality of methods including a lookup method for determining antenna element phase and gain settings; a computation method for determining antenna element phase and gain settings.

The method of operation for controlling slave RFIC devices in an antenna array includes: initializing common registers with calibrated gain values; storing phase shifter values in local registers; computing phase shifter values; and looking up gain settings.

One non-limiting exemplary embodiment illustrates advantageously the principle subject matter. A Ka-band SatCom frontend module consists of a phased-array antenna panel **6000** and its housing. The phased-array panel currently has a number of antenna elements **201** arranged as shown FIG. **6**. In an embodiment, the footprint of the array is approximately 19×25 cm.

Referring now to FIG. **6**, a phased-array panel contains a number of frontend modules, BGA-mounted onto the main PCB (i.e. the PANEL PCB) of the panel. Each frontend module contains a certain number of embedded antenna elements, GaAs frontend dies, and CMOS phased-array processing die(s). The antenna elements are embedded in the

top few layers of the substrate and both the GaAs dies and the CMOS die are flip-chip mounted onto the bottom layer of substrate in the frontend module. The input or output signals of the frontend modules can be either actively processed (combining, splitting, and buffering of the received and transmitted signals) with the CMOS phased-array processing dies or passively processed (combining, splitting) with passive combiners and splitters embedded in the PANEL PCB.

Finally, a transceiver die, flip-chip mounted on the PANEL PCB, performs the frequency translation from Ka-band to L-band for the receive signal and from L-band to Ka-band for the transmitted signal. Note that all active phased-array processing shall use the same CMOS die configured with different gain settings.

The PANEL PCB with the attached frontend modules and flip-chip(s) constitute the phased-array antenna panel.

The CMOS die (RFIC) consists of phased-array processing blocks which includes phase-shifters, combiners, splitters, gain equalizers, buffer amplifiers, digital signal control and interface (digital module).

Each CMOS supports 16 antenna elements as shown in FIG. **7**. A total of 48 CMOS phased-array processing dies on the 48 frontend modules are grouped into 4 groups, each with 3×4 dies. Each 3×4 dies interfaces with a microcontroller on the PCB via one SPI bus interface as 12 slaves (might be expanded into 16 slaves) at a data rate of 25 MHz. A driving requirement of the SPI bus design is to achieve the 25 MHz data rate in the configuration of the 12 (or 16) slaves.

Note that in each CMOS phased-array processing die, there are 16 RF chains to process the signals for 16 antenna elements on the frontend module. To minimize the digital traces on the CMOS die, the on-chip registers are partitioned into 16 local register groups and one central register group. Each of the 16 register groups is located in the corresponding RF chains.

In an embodiment, the digital module includes

1. Digital control interface and registers,
2. Digital functional logic circuit, and
3. Data and Address Bus.

The digital control interface provides the digital interface and the registers. To distinguish among many RFIC dies on the Panel, the RFIC die has in an embodiment, one global/individual indicator pad and 5 individual die address setting pads for accommodating global or individual die write operation and up to 32 unique die addresses.

While conventional configuration and control of antenna element is through registers connected to analog circuits, this introduces noise, power consumption, and wastes area. In order to scale and to reduce cost and size, each RFIC die obtains its address as follows. The address for each die is accomplished by using 5 external I/O address pins (pads) in the CMOS die which are connected to logic high (VCC) or logic Low (GND) in a unique way in the Panel PCB to set the die address.

(Note that the die pads are connected to BGA balls on the frontend modules and then connectors to the resistors on PCB.) Depending on how many registers within each die, the registers are assigned unique addresses within the chip. The host processor can access the registers in each CMOS die by writing to or reading from the corresponding unique CMOS die address/register address.

The PCB onto which the modules are mounted provides additional distinguishing characteristics.

Data and Address Bus provides the interface between all RFICs and the main processor/microcontroller. Since there are a large number of RFICs in the system, the main processor needs to drive a large number of RFICs.

There are three formats of SSI bus available on the host processor. For the Freescale SSI formats, the clock polarity bit (SPO) is set to low for the steady (idle) state of logical low on clock line and the phase control bit (SPH) is set to low for the data latching on the first clock edge. As is known to those skilled in the art, the start of transmission is signified by the SSIFss master signal being driven Low, causing slave data to be enabled onto the SSIRx input line of the master. The master SSITx output pad is enabled.

One half SSICIk period later, valid master data is transferred to the SSITx pin. Once both the master and slave data have been set, the SSICIk master clock pin goes High after one additional half SSICIk period. The data is now captured on the rising and propagated on the falling edges of the SSICIk signal.

In the case of a single word transmission, after all bits of the data word have been transferred, the SSIFss line is returned to its idle High state one SSICIk period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the SSIFss signal must be pulsed High between each data word transfer because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the SPH bit is clear. Therefore, the master device must raise the SSIFss pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the SSIFss pin is returned to its idle state one SSICIk period after the last bit has been captured.

In embodiments, the SSICIk clock phase from the host process is slightly different in the single transfer mode versus continuous transfer mode. In the continuous transfer mode, the SSICIk clock phase is delayed by half a clock cycle at the beginning of each transfer cycle. So, the SSICIk clock phase is not continuous across the transfer cycles. This format is different from TI synchronous serial format which has continuous SSICIk clock phase and is slightly faster. By this disclosure, Applicant intends illustration of constructive reduction to practice of the invention in either embodiment.

As is known to those skilled in the art, both Freescale and TI formats are designed for full duplex data transfer using FIFO. Unanticipated in conventional practice, Applicants adopt a half-duplex byte read/write format as follows. In the write operation, the first 7 bits are the register address, the 8th bit is the write or read (Write=1, read=0), the last 8 bits are the data byte. The following timing diagram shows the Freescale format. For TI format, the data is latched at the falling edge.

In the read operation, the first 7 bits are the register address, the 8th bit is the read (read=0), the last 8 bits are the data byte. The following timing diagram shows the Freescale format. For TI format, the data is latched at the falling edge.

In an embodiment, a 7 bit address accommodates up to 128 registers. In an embodiment, the on-chip registers are organized in multiple banks of 128 registers. The selection of the register bank is done through setting the RB_CONFIG register. Detailed description will be provided in the later section.

In an embodiment, there are 5-31 external input pads (DIE_ADD) to accept the die address from host processor. If the 5 input matches the die address, the die is selected for read/write operation. An additional input pad (GI_SEL) is used for global or individual die selection. If the global/individual die selection input is high, it is a global setting

and all dies shall accept the SSI signal. If the global/individual die selection input is low, only the individual die with die address match shall accept the SSI signal. As shown on the right side of die, the 5 pads are connected to Logic high or Logic low to set the die address. The Freescale/TI pad selects which format to be used. Note that the digital design shall support Freescale frame formats (SPO=0, SPH=0) for both the single or continuous transfer mode and the TI synchronous serial mode.

In a currently believed preferred embodiment, the apparatus connects serial SSI bus to up to 32 dies in parallel. The parasitics of large number of fan-outs might affect the bus speed. In an embodiment, external line drivers such as 74HTC244 buffer the SPI bus to drive large fan out. Multiple layers of buffering using line drivers might be required. It is advisable to include bus driver and bypass jumper using chip resistor in the final PCB design to enhance the reliability of the design. The decision to include bus driver or not are embodiments.

SPI bus supports the master or slave device. The SPI Master will provide the SPI clock and the control of the bus direction. The host processor shall be configured as the SPI master and all CMOS dies shall be SPI slaves. All CMOS dies will have unique SPI address which is configured through resistors on PCB connected to the I/O pads of the frontend modules. The address of the frontend module will be set according to pre-determined order which allows fast antenna weight vector update. The target SPI bus write speed is 25 MHz when 16 slave dies are connected to a master. The SPI bus speed will be decided after the initial testing. The maximum read speed of SPI bus is 12.5 MHz (TBD0).

In an embodiment, the candidate microcontroller is TI's ARM Cortex-M4 core based Stellaris processor with maximum speed up to 80 MHz. The LM4F230H5QR contains 4 SPI ports on-chip, each allows up to 8 16 bit values to be stored independently in both transmit and receive modes in the 8-locations deep FIFO. Other microcontrollers are substantially equivalent.

For 48 dies on the Panel PCB, each SPI port can communicate with 12~16 dies. Note that the SPI bus can operate at a maximum of 25 MHz write speed. With 16 bit data registers, the read/write is about 1 MHz.

Write Operation

When host processor writes to the SPI bus, all the dies connected to the same bus simultaneously receive the data. For individual die write (GI_SEL=0), the die with an address match (Die_ADD) shall accept the data into the register. To be precise, when the Die_ADD bits matches the die address (determined by the pad connections), an internal chip select is generated to allow further address decoding and the local register matching the address accepts the data into register.

Read Operation

The host processor reads from the SPI bus. All the data_out pad of the die shall be initially in the high impedance tri-state. Once the first 5 address bit matches the die address, the data_out pad would become active. Once the read operation is complete, the data_out pad would return to high impedance tri-state.

Since the CMOS dies contain lots of RF circuits, it is extremely important to reduce the digital traces going through the die. This creates parasitic coupling with the RF traces and would affect the performance of the RF circuit. We want to keep the global digital traces within each CMOS die to be a limited number only which go through some pre-planned area only, such as underneath the passive RF combiners (RF combiner only uses the top 2 layers of the metal) of each RF chain.

In an exemplary embodiment, registers in each RFIC are grouped into local registers and global registers, based on where they reside within the die as shown in the diagram where (n=16). The global registers control the overall RFIC functions and the local registers, which are physically placed in close proximity to the local circuit (RF chains) blocks they control. In the CMOS array processing RFIC, there are multiple RF chains corresponding to the elements of array antenna, each set of the local registers controls the RF circuit chain corresponding to individual antenna element and the set of global registers controls the overall RFIC function.

Common Registers

In an embodiment, a small subset of local registers, i.e. the common registers, contains identical values for all RF chains. The values of the sets of common registers are duplicated in all RF chains and also in the global area as well. The corresponding common registers are arranged in the same order in all RF chains and the global area. The corresponding common registers in all sets are assigned the same address.

Writing to Common Registers

The corresponding common registers in all sets is written with a single write operation to the die when only one beam is desired. This reduces the time required to configure all corresponding registers to enable high speed system operation. The sole purpose of the common registers is to speed up the write operation. Instead of writing to 16 local non-common registers, a single write would set the 16 corresponding common registers.

Reading from Common Registers

In an embodiment, when the host processor reads a common register address, only one set of physical common register (i.e., global common register set) within the die shall respond to the read operation and output the register value. All the other sets shall be read-disabled. This avoids the bus contention during read operation of the common registers.

Non-Common Global Register and Non-Common Local Register

In contrast, the set of non-common global registers controlling the centralized circuits are not duplicated in the RF chains. The set of non-common local registers controlling the local circuits and are not duplicated in other RF chains and the global area.

SPI Bus within the Die

By partitioning registers into global and local registers, only a single global data and address bus within a die is required. The address decoders are duplicated in each RF chain. No other traces except for SPI bus shall connect the global registers to a local circuits or local register to a global circuit. This reduces the number of global interconnection traces. Local registers should be placed carefully by the local circuits to minimize crossing of digital traces through RF circuits. As a guideline, the set of local registers and address decoder should be placed on the same relative location of all the local RF circuits so that interconnections can be routed properly. The local and global registers are defined in this specification.

In an embodiment, only 7 address bits are available for accessing registers within the die, accordingly, the registers are grouped to different banks of registers, each bank contains a maximum of 128 registers. At any time, only one bank of register is active. This is configured via the TBD1 bits within a configuration register (RB_CONFIG) within the set of the common registers. At the power up, the RB_CONFIG shall be defaulted to zero and a default set of bank 0 registers is active. When the TBD1 bits in the RB_CONFIG is set to a value other than zero, a different

bank of registers becomes active. This allows the maximum number of addressable registers to be TBD2×128 (where TBD2 is the number of register banks, note that 2^(TBD1−1)≤TBD2<2^TBD1). The address of the RB_CONFIG register shall not be re-used at different banks. Physically, there shall be only one RB-CONFIG register in each set of common registers.

Most of the RFIC functions are controlled by the Digital Control Interface Circuit. Digital Function Logic Circuit will be needed to provide the control of the phase shifter/gain equalizer. Two approaches (Approach 1 and Approach 2) for setting the phase shifter and gain equalizer values in the RF chain are to be implemented. The implementation shall allow independent operation of each approach configured by setting a global register. Each approach should be functional when the digital logics implementing the other approach is removed from the production chip.

In an embodiment, the digital function logic circuit is duplicated in each RF chain.

Approach I (Table Lookup)

In approach 1, the phased-array beam is formed by loading each antenna element with specific phase shifter setting value and gain equalizer setting value from an antenna weight vector table. The antenna weight vector table contains a set of TBD3 antenna weight vectors. Each weight vector contains a set of phase shifter/gain equalizer settings for all antenna elements. A table of TBD3 phase shifter/gain equalizer settings is stored in the local registers for each RF circuit chain corresponding to an antenna element. The antenna weight vector table consists of these local phase shifter/gain equalizer registers. The values of phase shifter setting are pre-stored in the antenna weight vector table of each die and be used for pointing up to TBD3 beam directions. Once the weight table is loaded, the host processor only needs to select which position in the antenna weight vector table to be used for the phase shifters. This should be accomplished by a single write to the die. This speeds up the antenna beam transition movement within the beam directional range covered by the antenna weight vector table. However, when the beam direction is outside of the directional range covered by the antenna weight vector table, new antenna weight vector table need to be loaded. There might be some delay in loading the new table. This is especially true for a phased-array antenna with high number of antenna elements. To enable high mobility, the phase shifts need to be updated quickly. Thus, an efficient way of dissemination of the phase shift control information to the phase shifters of the antenna elements are important. In an embodiment we disclose 2 AWV tables—one table will be used for immediate phase shifter/gain equalizer settings for each RF circuit chain based on the AWV pointer and another AWV table will be used for future phase shifter/gain equalizer settings. The future table can be updated independently of the immediate table. The two tables can then be ping-ponged by an appropriate index.

Note that the antenna weight vector (AWV) table shall be in the local registers. Each AWV contains 16 registers for the 16 RF chains with the same local address (LSB). Note that phase-equalizer values stored inside the registers in RF chain need not be the same. Different values can be loaded into different RF chains to account for any discrepancies of the phase shifter/gain equalizer at different RF chains. The different values are obtained through lab calibration of the phased-array antenna.

Loading up and Phase Shifter/Gain Equalizer Value

To load up the proper antenna weight within the antenna weight vector, a pointer shall be provided for pointing to which one of the TBD3 registers within the local registers. Note that the pointer resides in a register AWV_POINTER within the common registers. Each time a value is written into the common register, it points to a specific AWV register within the AWV table. Depending on the implementation, the specific register being pointed either directly control the phase and gain equalizer (via a multiplexer controlled by the AWV_POINTER) in one implementation or in an alternate implementation, the value of the specific register is copied onto (read out to) a latch located at the phase shifter/gain equalizer upon each write operation into the AWV_POINTER.

Approach II (Computation)

A second approach for fast loading of the phase shifter setting is to employ digital functional logic circuit to generate the required phase shift on-the-fly. Assuming the antenna elements are placed linearly in a x and y directional rectangular grid on a receiving device. Let the phase shift of the corner element (0,0) be ϕ00 and the phase increment for x direction and y direction are ΔX and ΔY, respectively, for each frontend module, and phase increment for x direction and y direction are Δx and Δy, respectively, for each element within the frontend module. The phase shift for the (nx, ny) antenna element in the (mx, my) frontend module on the rectangular grid can be represented as

$$\phi xy=\phi 00+mx\cdot\Delta X+my\cdot\Delta Y+nx\cdot\Delta x+ny\cdot\Delta y \quad \text{(Equation 1)}$$

This allows different frontend module-to-frontend module spacing from the element-to-element spacing within the frontend module. Note that mx, my, ΔX, ΔY, nx, ny, Δx, and Δy are needed in the digital functional logic circuit to generate the phase shift. The nx and ny corresponds to the RF chain index within each CMOS die. For a CMOS die controlling 4×4 antenna element, nx and ny takes on the value from the set of [0, 1, 2, 3].

In an embodiment, the phase shifter setting has limited resolution (4 bits). So, the actual phase shifter value for the (mx, my, nx, ny) element is

$$\text{Quan}[\phi xy]=\text{Quan}[\phi 00+mx\cdot\Delta X+my\cdot\Delta Y+nx\cdot\Delta x+ny\cdot\Delta y\urcorner] \quad \text{(Equation 2)}$$

In an embodiment, the on-the-fly phase shifter value computation is accomplished by digital functional logic circuit. In an embodiment, 8 bits (resolution=360/256 degree) is used to represent the values ϕ00, ΔX, ΔY, Δx, Δy to yield high precision computation. The computation of Equation 1 is with modulo 8 bit arithmetic in that embodiment.

In an embodiment, the phase shifter value is represented in the fractional value of 360 degree.

Phase shifter	Fraction	Integer Representation
0 degree	0/360 = 0/16	0000
22.5 degree	22.5/360 = 1/16	0001
45 degree	45/360 = 2/16	0010
. . .		
337.5 degree	337.5/360 = 15/16	1111

In an embodiment, all values are modulo 360 degree, i.e., all integer portion of the fractional representation shall be set to zero after each operation.

The Quan[.] function is used to round-up the resulting arithmetic into the length of phase shifter bits as well as the modulo operation. Mathematically, the following operation is performed

1. Compute ϕ00+mx·ΔX+my·ΔY+nx·Δx+ny·Δy¬ using modulo 8 bit integer arithmetic (dropping carry bits)

2. Select 4 MSBs as the phase shifter value

Here mx, my, ΔX, ΔY, Δx, and Δy are stored in the common registers. The values of nx and ny are stored in local registers. For each AWV update of the whole phased-array, only ΔX, ΔY, Δx, and Δy are changed. mx, my, nx and ny are written once only during configuration stage.

AWV Setting

In approach 1, to write AWV_POINTER (common register) to multiple dies simultaneously, global write operation (GI_SEL=1) is used. Similarly, in approach 2, when global write operation is used to write ΔX, ΔY, Δx, Δy.

Note that approach 1 or approach 2 is selected via B1 in RB_CONFIG.

Gain Equalization Setting

In an embodiment, the antenna weight table values are obtained through calibration of antenna beam in the laboratory. This allows correction of an anomaly in the phase shifter and equalizer values. Since the gain setting for each phase shifter setting for a given element is based on calibration and do not change (except may be for large temperature swing), it can be pre-loaded into the RF module during initialization, thereby reducing real time data transfer throughput. For approach 2, there are 16 gain register settings for the 4 bit phase shifter settings. For approach 2, the gain equalizer values shall be stored in a 16 element lookup table (each Gain Equalizer is TBD4 bits), in which the input address is the phase shifter value and output corresponds calibrated gain setting for each phase shift. The 16 registers in the lookup table are local registers.

Quan[ϕ*xy*]- -/- ->16×1 Lookup Table->Gain equalizer value

AWV from Approach 2 (Computational Mode)

Method Embodiments

The RFIC digital module shall interface with the PCB microcontroller SPI master via one of the SPI frame format as slave. Each SSI master will control **12** (TBR) slave RFIC digital circuits.

There are 4 modes of system operation:

- Mode 1 (Initialization). In this mode the digital module is initialized and the data received by the die will be destined for the Global and Local Registers.
- Mode 2 (Read Back). In this mode, the data from the Global and Local Registers in the die with the die address match is read by the SPI master.
- Mode 3 (Table Execute). In this mode, the phase shifter/gain equalizer index is received by the AWV_POINTER register.
- Mode 4 (Compute). In this mode, ΔX, ΔY, Δx, and Δy needed for Approach 2 are received by the Digital Module.

a. Initialization

The digital module shall accept the data from the microcontroller and load into the local common registers of appropriate antenna elements the calibrated gain values.

Read Back Mode

Upon command by the SPI master, the Digital Module shall send the contents of all registers to the SPI master.

Tabulation Mode

The tabulation mode is set by the B1 bit of RB_CONFIG register. The Digital Module shall accept the data from the SPI master and load into the common local registers the phase vector table. Upon command form the SPI master, the Digital Module shall load the phase shifter values into the appropriate local registers. The Digital Module shall look up the gain settings for the associated phase shifter value into the local registers.

Computation Mode

The computation mode is set by the B1 bit of RB_CONFIG register. The Digital Module shall accept the data from the SPI master and load into the Global and common local registers the constants. the Digital Module shall compute the phase shifter values per (Equation 2) and load the result into the appropriate local registers. The Digital Module shall look up the gain settings for the associated phase shifter value into the local registers.

Conclusion

Phased-array antenna elements are placed linearly in a x and y directional rectangular grid on a receiving device. Let the phase shift of the corner element (0,0) be ϕ00 and the phase increment for x direction and y direction are ΔX and ΔY, respectively, for each frontend module, and phase increment for x direction and y direction are Δx and Δy, respectively, for each element within the frontend module. This allows different frontend module-to-frontend module spacing from the element-to-element spacing within the frontend module. Note that mx, my, ΔX, ΔY, nx, ny, Δx, and Δy are needed in the digital functional logic circuit to generate the phase shift. The nx and ny are position of antenna element x, y and, in a currently preferred embodiment, has a correspondence to the RF chain index from 0 to 15 within each CMOS die which controls 4×4 antenna elements within a frontend module. For a CMOS die controlling 4×4 antenna element, nx and ny takes on the value from the set of [0, 1, 2, 3].

In some embodiments, the RF traces between antenna elements to CMOS die within a frontend module have equal length. In other embodiments, the RF traces between antenna elements to CMOS die within a frontend module have un-equal lengths, Some fixed phase correction factors ϕx,y are needed to compensate for the time delays Tx,y introduced by the un-equal trace lengths. However, these phase correction factors do not change when beam direction changes. The phase correction factors are proportional to the center frequency of the signal.

In some implementations, the RF traces for different frontend modules have equal length. In other implementations, the RF traces for different frontend modules have un-equal lengths, Some fixed phase correction factors ϕX,Y are needed in the above equation to compensate for the time delays τX,Y introduced by the un-equal trace lengths. Note that these phase correction factors do not change with beam directions. The phase correction factors, however, are proportional to the center frequency of the signal ϕX,Y=fc*τX,Y.

Note that the two phase correction factors due to un-equal trace lengths can be absorbed into a single correction factor ϕX,Y+ϕx,y=ΔϕX,Y,x,y.

A Quan[.] function is used to round-up the resulting arithmetic into the length of phase shifter bits as well as the modulo operation. In an embodiment, the following operation is performed in parallel at a location advantageously near to each antenna element:

1. Compute ΔϕX,Y,x,y+mx·ΔX+my·ΔY+nx·Δx+ny·Δy¬ using modulo 8 bit integer arithmetic (dropping carry bits)

2. Select 4 MSBs as the phase shifter value

A conventional method of implementing the phased array beamsteering is to compute the antenna phase shifts for every individual antenna element in a single processor and distribute the antenna weight vectors (phases and amplitudes) to each frontend module one by one. This would require dissemination of Nx*Ny weight vectors to (Nx*Ny)/16 frontend modules where each frontend module receives 16 antenna weight vectors. Conventional dissemination of weight vectors adds noise to the signal channel and consumes area for routing of parallel buses which are problems rather than solutions.

Note that with the proposed computational mode where the computation of the antenna weight is done locally at each antenna element, the values for mx, my, ΔX, ΔY, Δx, and Δy are stored in the common registers and the ΔϕX,Y,x,y, nx and ny are stored in local registers. For each beam direction, only ΔX, ΔY, Δx, and Δy need to be updated. The values for ΔϕX,Y,x,y, mx, my, nx and ny are written only once during the initial configuration phase. This is significant reduction from the prior art method of updating which requires Nx*Ny antenna weight vectors to be updated. Note also that there is no need to write ΔX, ΔY, Δx, and Δy 16 times for each antenna element within a frontend module.

A single chip antenna array control submodule is disclosed in the present patent application. The identical chip may be deployed over an antenna array with many elements. Only four operands need to be distributed by the central control no matter how many antenna elements or submodules are configured.

The present invention is easily distinguished from conventional phased antenna array control by the substantially lower bandwidth requirement to distribute phase information into the shift circuits. Both lower data rates and higher phase data uploads are accomplished with less cost. The invention reduces bus speed or increases beam direction change rapidity or both.

The present invention is easily distinguished from conventional systems by the characteristic of the RFIC to have global registers, local registers, and common registers. Global registers are registers which are located in global area controlling function at the global area. For example, the voltage reference source is in the global area which provides voltage reference or current bias to all local area. The voltage reference would be controlled the global area. Local registers are distributed to be physically close to their respective antenna element. When the common registers on each device receives content, it is duplicated to the local registers on the device. In the compute mode of operation, phase is determined based on delta X and delta Y locally using multiplier or recursive adder circuits. We designate two common registers per device for delta X and delta Y which are written to once for each device. The content is then duplicated locally on the same device, in an embodiment, 16 times when there are 16 antenna elements. Advantageously, only a single bus needs to be routed within each semiconductor device which lowers area and routing resource consumption. This is hierarchical structure is substantially advantageous over conventional many write operations to local registers. Advantageously, each device has a pin to control global vs individual operations with the effect that 4 write operations can distribute delta X, delta Y, delta'X and delta'Y to all the devices in the array. In the compute mode, the address setting of each die position on the PCB enables indexing. In a tabulate mode of operation, a pointer is distributed across the array by a global write of a pointer to a common register which updates a weight vector in a single write operation.

The present invention is easily distinguished from conventional phased-array antennas by its method for transforming electrical signals by determining antenna weight vectors for a series of beam directions at digital functional logic circuits distributed among RFIC devices adjacent to their associated phased-array antenna element: initializing local registers and common registers with integer-pair values for location of each antenna element in an phased-array antenna and a phase correction factor. For each desired beam direction in the series of beam directions subsequent to initializing local registers and common registers, the method provides reading four binary coded phase shift values from a serial bus; storing the four binary coded phase shift values into common registers on each RFIC device accessible to each digital functional logic circuit associated with one of the phased-array antenna elements. At each digital functional logic circuit associated with one of the phased-array antenna elements, the method distributes computation by reading from common registers a pair of binary coded phase shift increment values for each increment in module location on the printed circuit board and a pair of binary coded phase shift increment values for each increment in antenna element location on the module; reading from common registers integer-pair values corresponding to the location of the module on a printed circuit board; reading from common registers a phase correction factor; reading from local registers associated with each digital functional logic circuit integer-pair values corresponding to the coordinate location of its associated phased-array antenna element in the phased-array antenna on a radiating surface of the module; summing the phase correction factor and the multiplication products of the four binary coded phase shift values with their corresponding location specific integer value; setting an antenna phase shift and amplitude weight value for its phased-array antenna element according to a resolution, in an embodiment, 4 bits; and transforming the electrical signal according to the computed weight values. Advantageously, speed is improved, area and cost is reduced, and bandwidth is conserved over conventional systems by initializing local registers and common registers by the following steps: writing integer-pair values for m into common registers where m corresponds to a coordinate location of each module on a printed circuit board, in an embodiment, reading the integer-pair values from tie-up and tie-down circuits at each mounting location on the printed circuit board; writing integer-pair values for n into local registers where n corresponds to a coordinate location of an phased-array antenna element in the phased-array antenna on a radiating surface of the module, in an embodiment, reading the integer-pair values from a location on a mounting surface of the module; and writing a binary coded value, within the range of 4 to 64 bits, in an embodiment 8 bits, for phase correction factor due to unequal trace lengths into local registers, in an embodiment, reading the binary coded value from a non-transitory storage device.

The techniques described herein can be implemented in digital electronic circuitry, or in computer hardware, firmware, software, or in combinations of them. The techniques can be implemented as a computer program product, i.e., a computer program tangibly embodied in an information carrier, e.g., in a machine-readable storage device or in a propagated signal, for execution by, or to control the operation of, data processing apparatus, e.g., a programmable processor, a computer, or multiple computers. A computer program can be written in any form of programming language, including compiled or interpreted languages, and it can be deployed in any form, including as a stand-alone

program or as a module, component, subroutine, or other unit suitable for use in a computing environment. A computer program can be deployed to be executed on one computer or on multiple computers at one site or distributed across multiple sites and interconnected by a communication network.

Method steps of the techniques described herein can be performed by one or more programmable processors executing a computer program to perform functions of the invention by operating on input data and generating output. Method steps can also be performed by, and apparatus of the invention can be implemented as, special purpose logic circuitry, e.g., an FPGA (field programmable gate array) or an ASIC (application-specific integrated circuit). Modules can refer to portions of the computer program and/or the processor/special circuitry that implements that functionality.

Processors suitable for the execution of a computer program include, by way of example, both general and special purpose microprocessors, and any one or more processors of any kind of digital computer. Generally, a processor will receive instructions and data from a read-only memory or a random access memory or both. The essential elements of a computer are a processor for executing instructions and one or more memory devices for storing instructions and data. Generally, a computer will also include, or be operatively coupled to receive data from or transfer data to, or both, one or more mass storage devices for storing data, e.g., magnetic, magneto-optical disks, or optical disks. Information carriers suitable for embodying computer program instructions and data include all forms of non-volatile memory, including by way of example semiconductor memory devices, e.g., EPROM, EEPROM, and flash memory devices; magnetic disks, e.g., internal hard disks or removable disks; magneto-optical disks; and CD-ROM and DVD-ROM disks. The processor and the memory can be supplemented by, or incorporated in special purpose logic circuitry. The special purpose logic circuit can incorporate a state machine implementation which provides the required control flow for the operation.

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, other network topologies may be used. Accordingly, other embodiments are within the scope of the following claims.

We claim:

1. A submodule apparatus of an antenna array comprising:

a configuration store readable by a digital phase shift weight multiplier (multiplier);

said multiplier coupled to the configuration store;

a plurality of phase shifter circuits coupled to said multiplier and further each coupled to an external antenna array element; and

an operand receiver coupled to said multiplier and further communicatively coupled to a central control;

wherein the configuration store comprises phase shift error correction bias for each element of the antenna array, whereby phase shift weights for the phase shifter circuits determined by the multiplier operating on received operands are corrected by phase shift error bias stored in the configuration store.

2. A phased-array antenna panel comprising:

a plurality of front end modules, Ball Grid Array(BGA)-mounted to a main PANEL Printed Circuit Board (PCB);

the main PANEL PCB;

each front end module comprising:

a plurality of antenna elements;

the antenna element coupled to a frontend die;

the frontend die (submodule) coupled to a phased-array processing die;

wherein the antenna elements are embedded in the top of a substrate and the frontend dies and the phased-array processing die are flip-chip mounted onto the bottom layer of substrate of each front end module whereby input or output signals are conducted through the substrate to the phased-array processing die and to passive combiners and splitters embedded in the PANEL PCB; and

a transceiver die flip-chip mounted on the PANEL PCB whereby the antenna transmitted and received signals are frequency translated; wherein, each submodule comprises:

a configuration store readable by a digital phase shift weight multiplier (multiplier);

said multiplier coupled to the configuration store;

a plurality of phase shifter circuits coupled to said multiplier and further coupled to an external antenna array element; and

an operand receiver coupled to said multiplier and further communicatively coupled to a central control;

wherein the configuration store comprises phase shift error correction bias for each element of the antenna array, whereby phase shift weights for the phase shifter circuits determined by the multiplier operating on received operands are corrected by phase shift error bias stored in the configuration store.

3. The phased-array antenna panel of claim **2** wherein said phased-array processing die comprising:

a single bus coupling

phased-array processing blocks (blocks);

said block comprising phase-shifters, combiners, splitters, gain equalizers, buffer amplifiers, and a digital signal control and interface circuit;

at least one global/individual indicator pad; and

a plurality of individual die address setting pads, said pads in combination enabling a first die address to be configured at a first location on a main PANEL Printed Circuit Board (PCB) which connects a plurality of die address pads to a first combination of logic high or logic low and a second die address to be configured at a second location on the PCB which connects a plurality of die address pads to a second combination of logic high or logic low whereby registers within each instantiated phased-array processing die are assigned unique addresses and whereby indexing is provided for use in a computational mode.

4. The PANEL printed circuit board (PCB) of claim **2** further comprising:

a data and address bus;

a plurality of die address pads and a global die selection pat and a transfer format mode pad, whereby a plurality of die address pads at a first location coupled to a first combination of logic high and logic low and a plurality of die address pads at a second location coupled to a second combination of logic high and logic low assigns unique addresses to registers within each instantiated phased-array processing die when coupled to pads at said locations.

5. The PANEL PCB of claim 4 further comprising:
at least one driver to buffer bus outputs;
the driver coupling a microcontroller master device and coupling a plurality of slave devices on each phased-array processing die.

6. The phased-array processing die of claim 3 further comprising:
a plurality of Radio Frequency circuits (RF chains);
a register array in each phased-array processing die grouped into a local register group and a global register group, the local registers physically placed close in proximity to said RF chains which each correspond to an element of array antenna,
whereby each set of local registers control an individual antenna element and said global register controls overall phased-array processing die function; wherein at least one local register is a common register coupled to input output circuits of the phased-array processing die and further coupled to other local registers to distribute data values for each of the antenna elements.

7. A phased-array processing die comprising:
a single serial bus, said serial bus communicatively coupling a common register to a plurality of local registers, said serial bus further coupled to die address settings of the device whereby a single pointer is disseminated to all antenna elements or whereby an indexing can be determined in a computation mode of operation;
a plurality of Radio Frequency circuits (RF chains);
a register array in each phased-array processing die grouped into a local register group and a global register group, the local registers physically placed close in proximity to said RF chains which each correspond to an element of array antenna,
whereby each set of local registers control an individual antenna element and said global register controls overall phased-array processing die function; wherein at least one local register is a common register coupled to input output circuits of the phased-array processing die and further coupled to other local registers to distribute data values for each of the antenna elements;
a single bus coupling
phased-array processing blocks (blocks);
said block comprising phase-shifters, combiners, splitters, gain equalizers, buffer amplifiers, and a digital signal control and interface circuit;
at least one global/individual indicator pad; and
a plurality of individual die address setting pads, said pads in combination enabling a first die address to be configured at a first location on a main PANEL Printed Circuit Board (PCB) which connects a plurality of die address pads to a first combination of logic high or logic low and a second die address to be configured at a second location on the PCB which connects a plurality of die address pads to a second combination of logic high or logic low whereby registers within each instantiated phased-array processing die are assigned unique addresses and whereby indexing is provided for use in a computational mode.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 10,439,284 B2
APPLICATION NO. : 13/959542
DATED : October 8, 2019
INVENTOR(S) : Wang et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page

At the second line of the "Inventors" field associated with item (72), delete "Chak Chie" and insert -- Chak-Ming Chie --, therefor.

Signed and Sealed this
Ninth Day of June, 2020

Andrei Iancu
Director of the United States Patent and Trademark Office