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(54) **DEMUX CIRCUIT**

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***G09G 3/36*** (2006.01)

(52) **U.S. Cl.**
CPC ... ***G09G 3/3685*** (2013.01); *G09G 2300/0417* (2013.01); *G09G 2310/0251* (2013.01); *G09G 2310/0297* (2013.01); *G09G 2330/04* (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

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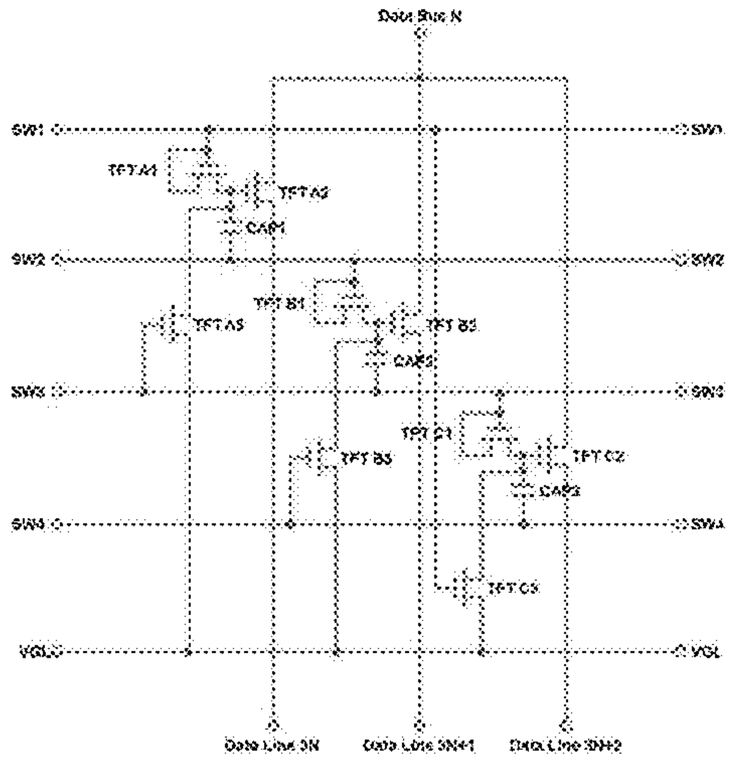
(57) **ABSTRACT**

The invention provides a DEMUX circuit, comprising: data bus, a first, second and third data lines, connected respectively to data bus and a first unit, a second unit and a third unit respectively; each unit respectively comprising: a TFT, a second TFT, a third TFT, and a capacitor, and inputting corresponding a first, a second, and a third switch signals; for each unit, during operation, when the first switch signal being turned on, the first TFT and the second TFT being turned on, and the corresponding data line is pre-charged; when the first switch signal being turned off, the second switch signal being turned on and the corresponding data line being charged to a preset voltage. The DEMUX circuit of the invention can increase the TFT gate driving voltage, leading to improving TFT electron mobility from IGZO and a-Si process, and improving the data line charging rate.

**11 Claims, 5 Drawing Sheets**



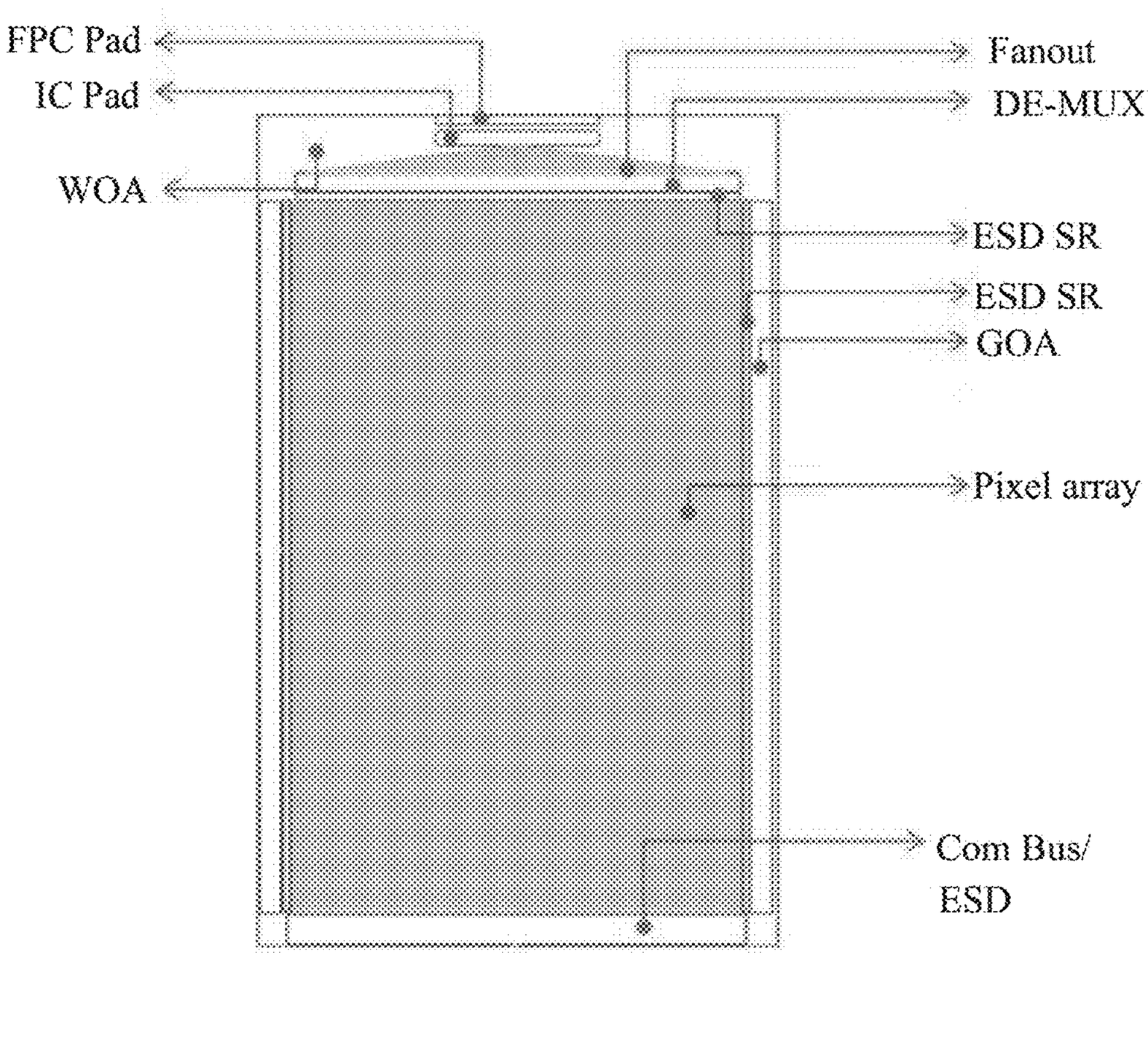



Fig. 1

Prior Art

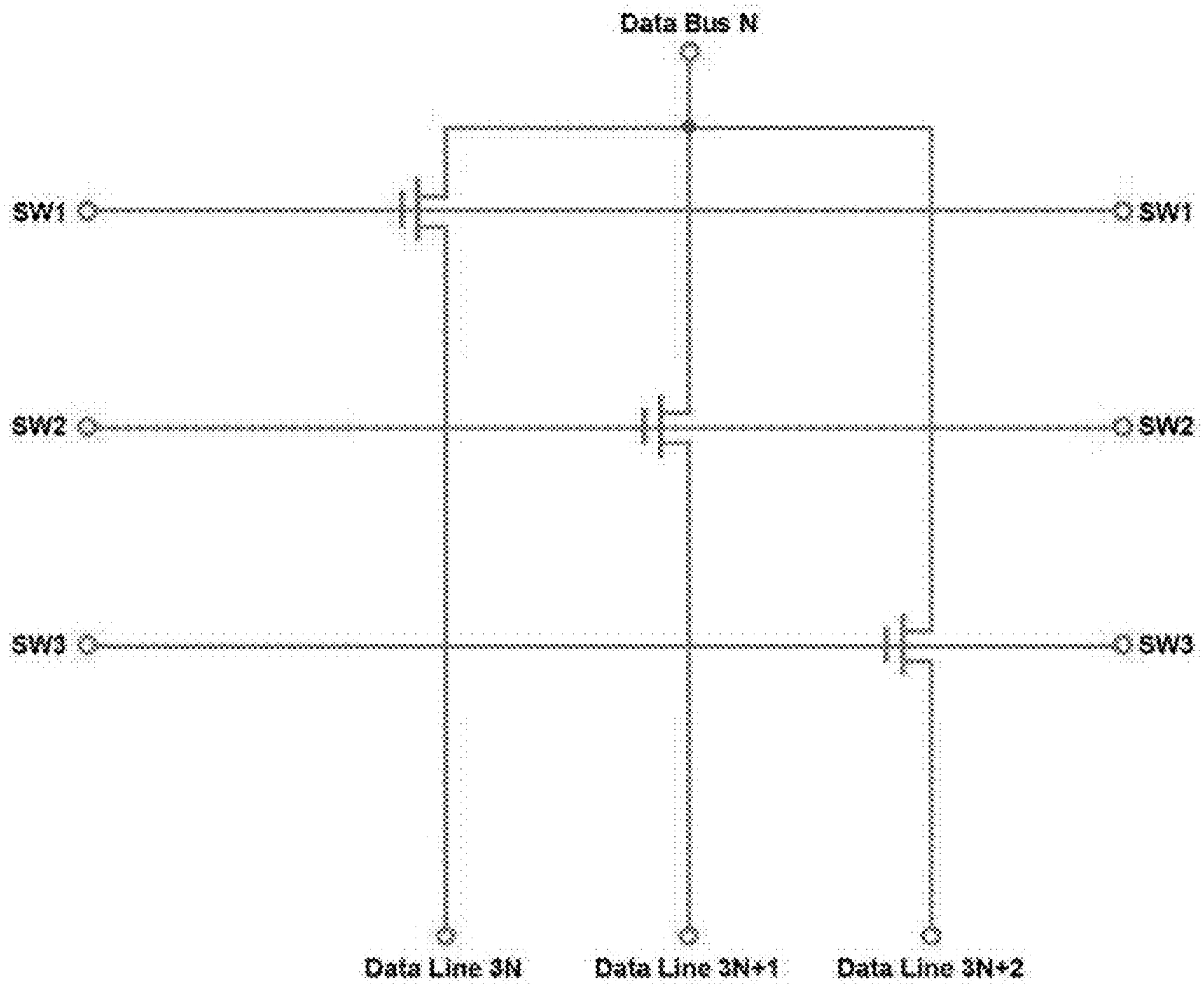



Fig. 2

Prior Art

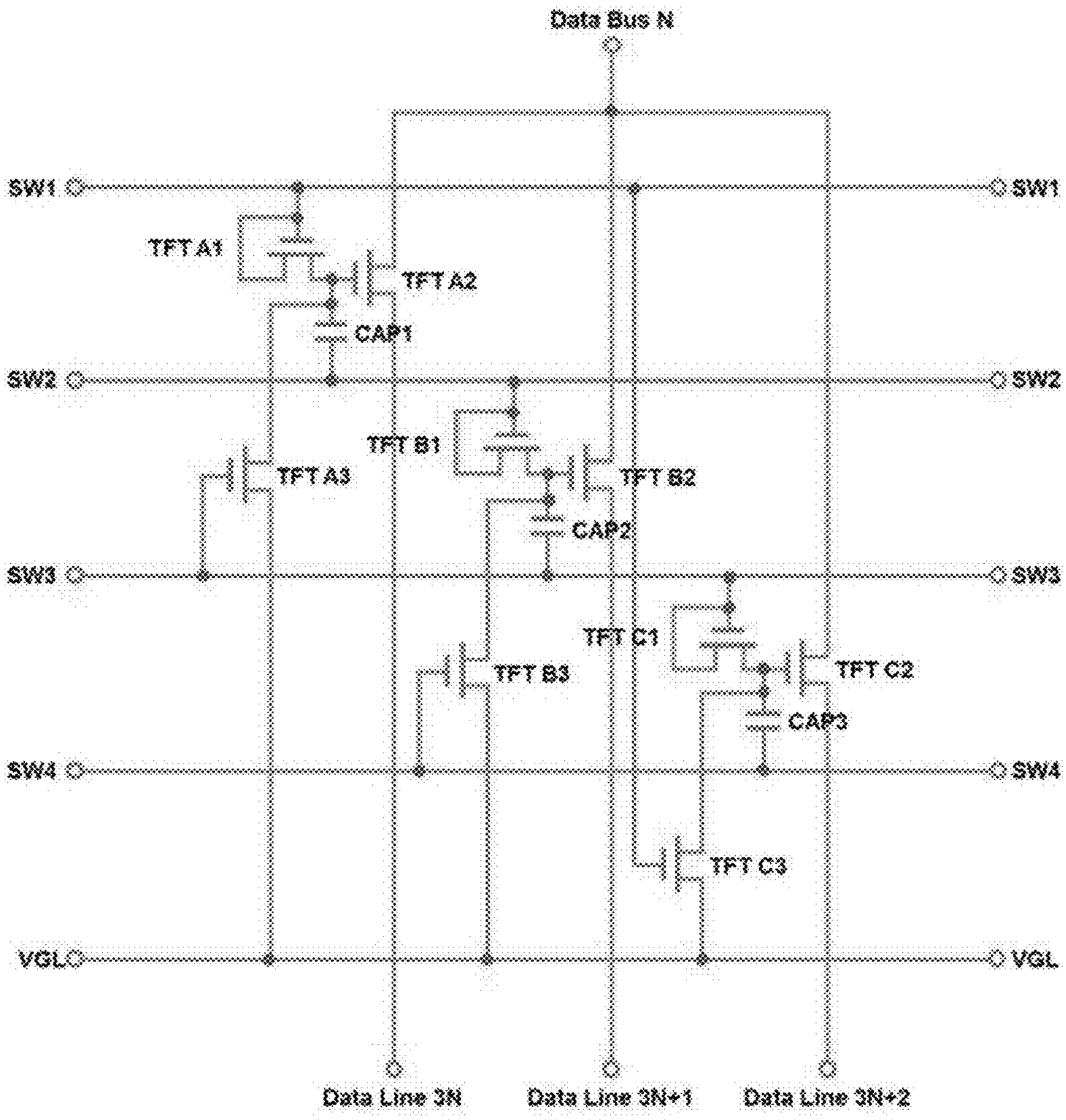

Data Bus N
SW1
SW1
TFT A1
TFT A2
CAP1
SW2
SW2
TFT B1
TFT A3
TFT B2
CAP2
SW3
SW3
TFT C1
TFT B3
TFT C2
CAP3
SW4
SW4
TFT C3
VGL
VGL
Data Line 3N
Data Line 3N+1
Data Line 3N+2

Fig. 3

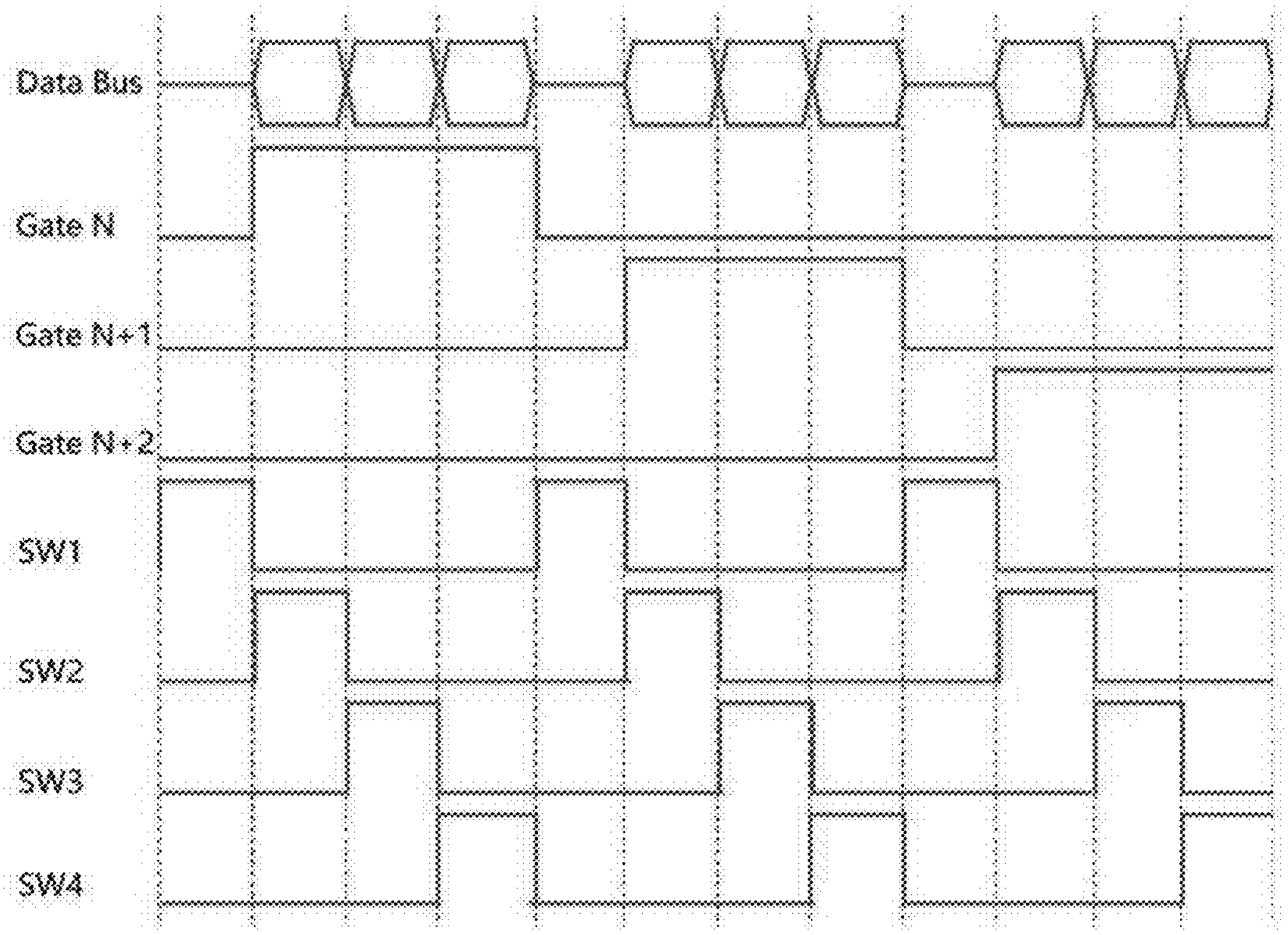



Fig. 4

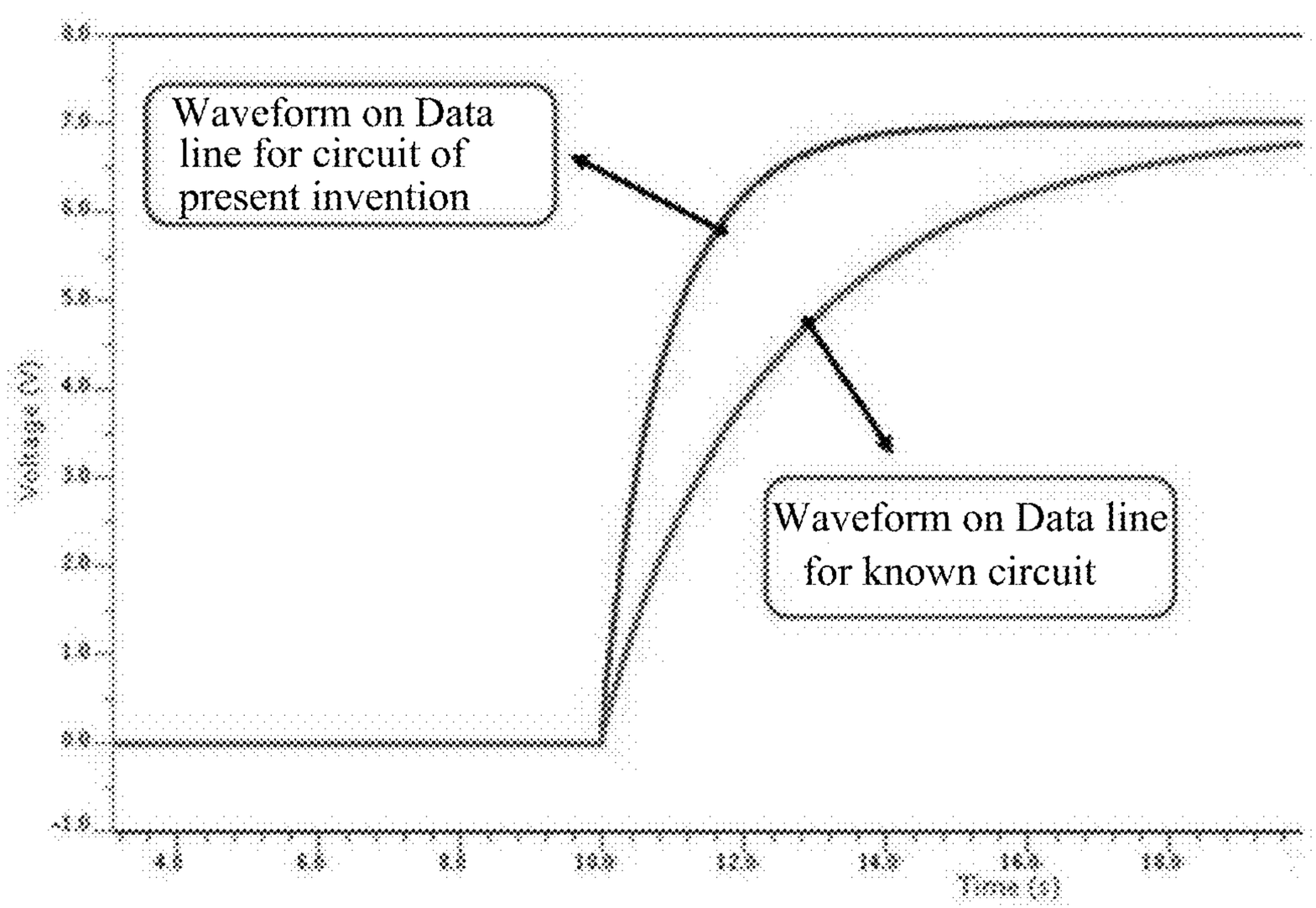

Waveform on Data line for circuit of present invention
Waveform on Data line for known circuit
Time (s)

Fig. 5

# DEMUX CIRCUIT

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to the field of display, and in particular to a DEMUX circuit.

### 2. The Related Arts

The liquid crystal display (LCD) is the most widely used panel display, and has become the choice of high resolution color screen display for various electronic products, such as, mobile phones, Personal digital assistant (PDAs), digital cameras, computer monitor or notebook computer screen. As the LCD technology progresses, the demands on the display quality and external appearances of the LCD also get higher, and the objectives is to further lower cost and narrow border designs.

The demultiplexer (DEMUX) is used for de-composing a signal channel into a plurality of signal channels, and is widely used in small-to medium size LCD. In LCD, DEMUX is usually with low temperature polysilicon (LTPS) process, the thin film transistor (TFT) manufactured by LTPS process usually has high electron mobility satisfying the needs of DEMUX.

As the LCD technology moves towards low cost, IGZO process and amorphous silicon (a-Si) process also have a demand for DEMUX. However, because the elements manufactured by the IGZO process and a-Si process has electron mobility much lower than the LTPS process, the charging rate of the panel is affected after using DEMUX.

FIG. **1** shows a known LCD driving structure. The pixel array is surrounded with various wires and circuits, including: flexible printed circuit pad (FPC pad), IC pad, wire on array (WOA), fan-out, DEMUX, electrostatic discharge (ESD) SR (trigger), gate driver on array (GOA), common bus/ESD (Com Bus/ESD). The present invention is related to the DEMUX shown in FIG. **1**.

FIG. **2** shows the known DEMUX circuit used in LCD. The DEMUX circuit comprises three thin film transistors (TFT), and the gates of the three TFTs are respectively inputted with signals SW**1**, SW**2** and SW**3**, the sources/drains are respectively connected to Data Bus N, and the drains/sources are connected respectively to Data line **3**N, **3**N+1 and **3**N+2. The signals SW**1**, SW**2** and SW**3** control the ON and OFF of the individual TFT according to the preset timing. When the TFT is turned on, the Data Bus N can be connected with the corresponding Data Line to charge the Data Line. This kind of DEMUX circuit is usually with LTPS process, because the LTPS process has higher electron mobility, the use of the DEMUX circuit can still maintain a relatively high Data Line charging rate. As the LCD technology moves towards low cost, IGZO process and amorphous silicon (a-Si) process also have a demand for DEMUX. However, because the elements manufactured by the IGZO process and a-Si process has electron mobility much lower than the LTPS process, the charging rate of the panel is affected after using DEMUX.

## SUMMARY OF THE INVENTION

The object of the present invention is to provide a DEMUX circuit, improving the DEMUX charging rate for a-Si process.



To achieve the above object, the present invention provides a DEMUX circuit, comprising:

a data bus, a first data line, a second data line and a third data line, connected respectively to the data bus and a first unit, a second unit and a third unit respectively corresponding to the first, second and third data lines;

each unit respectively comprising: a first thin film transistor (TFT), a second TFT, a third TFT, and a capacitor, and inputting corresponding a first, a second, and a third switch signals; the first TFT having a gate inputting the first switch signal, and a source and a drain irrespectively inputting to the first switch signal and connected to a gate of the second TFT; the second TFT having a source and a drain respectively connected to the data bus and the corresponding data line; the capacitor having one end connected to the gate of the second TFT and the other connected to the second switch signal; the third TFT having a gate inputting the third switch signal, a source and a drain respectively connected to the gate of the second TFT and a constant low voltage;

for each unit, during operation, when the first switch signal being turned on, the first TFT and the second TFT being turned on, and the corresponding data line is pre-charged; when the first switch signal being turned off, the second switch signal being turned on and the corresponding data line being charged to a preset voltage.

According to a preferred embodiment of the present invention, four switch signals are used for inputting to the first, second and third units, each unit selects three switch signals out of the four to use as the first, second and third switch signals corresponding to the unit.

According to a preferred embodiment of the present invention, the four switch signals are square waveform having a duty cycle of 0.25, with a phase difference of ¼ cycle among one another.

According to a preferred embodiment of the present invention, during operation, by controlling timing of the switch signals corresponding to each unit, when the first unit charges the first data line to a preset voltage, the second unit simultaneously pre-charges the second data line; when the second unit charges the second data line to a preset voltage, the third unit simultaneously pre-charges the third data line; when the third unit charges the third data line to a preset voltage, the first unit simultaneously pre-charges the first data line.

According to a preferred embodiment of the present invention, the DEMUX circuit is for indium gallium zinc oxide (IGZO) process.

According to a preferred embodiment of the present invention, the DEMUX circuit is for amorphous silicon (a-Si) process.

According to a preferred embodiment of the present invention, the DEMUX circuit is connected to an RGB display panel for outputting RGB data signals.

According to a preferred embodiment of the present invention, the data bus uses every four periods as a cycle, and stays vacant for a period after continuously outputs RGB data signals.

The present invention also provides a DEMUX circuit, comprising:

a data bus, a first data line, a second data line and a third data line, connected respectively to the data bus and a first unit, a second unit and a third unit respectively corresponding to the first, second and third data lines;

each unit respectively comprising: a first thin film transistor (TFT), a second TFT, a third TFT, and a capacitor, and inputting corresponding a first, a second, and a third switch signals; the first TFT having a gate inputting the first switch

signal, and a source and a drain irrespectively inputting to the first switch signal and connected to a gate of the second TFT; the second TFT having a source and a drain respectively connected to the data bus and the corresponding data line; the capacitor having one end connected to the gate of the second TFT and the other connected to the second switch signal; the third TFT having a gate inputting the third switch signal, a source and a drain respectively connected to the gate of the second TFT and a constant low voltage;

for each unit, during operation, when the first switch signal being turned on, the first TFT and the second TFT being turned on, and the corresponding data line is pre-charged; when the first switch signal being turned off, the second switch signal being turned on and the corresponding data line being charged to a preset voltage;

wherein four switch signals being used for inputting to the first, second and third units, each unit selecting three switch signals out of the four to use as the first, second and third switch signals corresponding to the unit;

wherein the DEMUX circuit being connected to an RGB display panel for outputting RGB data signals.

In summary, the DEMUX circuit of the present invention can increase the driving voltage of the TFT gate, leading to improving the TFT electron mobility from IGZO process and a-Si process, and improving the data line charging rate.

## BRIEF DESCRIPTION OF THE DRAWINGS

To make the technical solution of the embodiments according to the present invention, a brief description of the drawings that are necessary for the illustration of the embodiments will be given as follows. Apparently, the drawings described below show only example embodiments of the present invention and for those having ordinary skills in the art, other drawings may be easily obtained from these drawings without paying any creative effort. In the drawings:

FIG. **1** is a schematic view showing a driving structure in known LCD;

FIG. **2** is a schematic view showing the DEMUX circuit in known LCD;

FIG. **3** is a schematic view showing the DEMUX circuit according to the present invention;

FIG. **4** is a schematic view showing the timing of the DEMUX circuit according to the present invention;

FIG. **5** is a schematic view showing the comparison of the charging waveform of the known DEMUX circuit and the DEMUX circuit according to the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

To further explain the technical means and effect of the present invention, the following refers to embodiments and drawings for detailed description.

FIG. **3** is a schematic view showing the DEMUX circuit according to the present invention. The DEMUX circuit comprises: a data bus N, a first data line **3**N, a second data line **3**N+1, and a third data line **3**N+2, connected respectively to the data bus N and a first unit, a second unit and a third unit respectively corresponding to the first, second and third data lines.

The first unit comprises: a first thin film transistor (TFT) A**1**, a second TFT A**2**, a third TFT A**3**, and a capacitor CAP**1**; the second unit comprises: a first TFT B**1**, a second TFT B**2**, a third TFT B**3**, and a capacitor CAP**2**; the third unit comprises: a first TFT C**1**, a second TFT C**2**, a third TFT C**3**, and a capacitor CAP**3**.

The following uses the first unit as an example to describe the structure and function of each unit. In the first unit:

the first TFT A**1** having a gate inputting the first switch signal SW**1**, and a source and a drain irrespectively inputting to the first switch signal SW**1** and connected to a gate of the second TFT A**2**;

the second TFT A**2** having a source and a drain respectively connected to the data bus N and the corresponding data line **3**N;

the capacitor CAP**1** having one end connected to the gate of the second TFT A**2** and the other connected to the second switch signal SW**2**;

the third TFT A**3** having a gate inputting the third switch signal SW**3**, a source and a drain respectively connected to the gate of the second TFT A**2** and a constant low voltage VGL;

for the first unit, during operation, when the first switch signal SW**1** being turned on, the first TFT A**1** and the second TFT A**2** being turned on, and the corresponding data line **3**N is pre-charged; when the first switch signal SW**1** being turned off, the second switch signal SW**2** being turned on and the corresponding data line **3**N being charged to a preset voltage.

For other units, during operation, when the first switch signal is turned on, the first TFT and the second TFT are turned on, and the corresponding data line is pre-charged; then, when the first switch signal is turned off, the second switch signal is turned on and the corresponding data line is charged to a preset voltage. The switch signals of the other units are different from the switch signals of the first unit.

Moreover, the constant low voltage VGL can be used for discharge recovery for each capacitor. For example, for the first unit, when the switch signal SW**2** is turned off, the switch signal SW**3** is turned on, the capacitor CAP**1** can achieve discharge recovery through the constant low voltage.

Furthermore, the present invention can control the operation of the first, second and third units by providing switch signals SW**1**, SW**2**, SW**3**, and SW**4** and disposing appropriate timing. Each unit selects three appropriate switch signals out of the four switch signals to use as the first, second, and third switch signals corresponding to the unit. The four switch signals are square waveform having a duty cycle of 0.25, with a phase difference of ¼ cycle among one another (see FIG. **4**).

FIG. **4** shows the timing of the DEMUX circuit of the present invention. Refer to FIG. **3** and FIG. **4** for the operation principle of the DEMUX circuit of the present invention. When SW**1** is turned on, TFT A**1** and TFT A**2** are turned on, and Data line **3**N is pre-charged; then SW**1** is off and SW**2** is on, through the coupling effect of the capacitor CAP**1**, the gate voltage of TFT A**2** is further raised and data line **3**N is charged to a preset voltage, and the data line **3**N+1 is pre-charged simultaneously; then, n, TFT A**1** and TFT A**2** are turned on, and Data line **3**N is pre-charged; then SW**2** is off and SW**3** is on, through the coupling effect of the capacitor CAP**2**, the gate voltage of TFT B**2** is further raised and data line **3**N+1 is charged to a preset voltage, and the data line **3**N+2 is pre-charged simultaneously. At this point, TFT A**3** is turned on and TFT A**2** is turned off. As such, the cycle is complete.

Refer to the timing sequence of DEMUX circuit. The DEMUX circuit of the present invention can be used to connect to the RGB display panel to output RGB data

signals. The data bus uses every four periods as a cycle, and stays vacant for a period after continuously outputs RGB data signals. At this point, the four periods form a cycle for the corresponding gate line of the display panel, wherein the gate line stays in an on state during three periods and off state in one period. For the switch signals SW**1**-SW**4**, four periods form a cycle, wherein each switch signal stays on during one period, and stays off during the other three periods.

FIG. **5** shows the comparison of the charging waveform of the known DEMUX circuit and the DEMUX circuit according to the present invention, with x-axis as time (unit: sec) and y-axis as voltage (unit: volt). As shown in FIG. **5**, the charging rate is greatly improved with the DEMUX circuit of the present invention.

In summary, the DEMUX circuit of the present invention can increase the driving voltage of the TFT gate, leading to improving the TFT electron mobility from IGZO process and a-Si process, and improving the data line charging rate.

Embodiments of the present invention have been described, but not intending to impose any unduly constraint to the appended claims. Any modification of equivalent structure or equivalent process made according to the disclosure and drawings of the present invention, or any application thereof, directly or indirectly, to other related fields of technique, is considered encompassed in the scope of protection defined by the claims of the present invention.

What is claimed is:

**1**. A demultiplexer (DEMUX) circuit, comprising:

a data bus, a first data line, a second data line and a third data line, connected respectively to the data bus and a first unit, a second unit and a third unit respectively corresponding to the first, second and third data lines;

each unit respectively comprising: a first thin film transistor (TFT), a second TFT, a third TFT, and a capacitor, and inputting corresponding a first, a second, and a third switch signals; the first TFT having a gate inputting the first switch signal, and a source and a drain irrespectively inputting to the first switch signal and connected to a gate of the second TFT; the second TFT having a source and a drain respectively connected to the data bus and the corresponding data line; the capacitor having one end connected to the gate of the second TFT and the other connected to the second switch signal; the third TFT having a gate inputting the third switch signal, a source and a drain respectively connected to the gate of the second TFT and a constant low voltage;

for each unit, during operation, when the first switch signal being turned on, the first TFT and the second TFT being turned on, and the corresponding data line is pre-charged; when the first switch signal being turned off, the second switch signal being turned on and the corresponding data line being charged to a preset voltage;

wherein four switch signals are used for inputting to the first, second and third units, each unit selects three switch signals out of the four to use as the first, second and third switch signals corresponding to the unit, and the four switch signals are square waveform having a duty cycle of 0.25, with a phase difference of ¼ cycle among one another.

**2**. The DEMUX circuit as claimed in claim **1**, wherein during operation, by controlling timing of the switch signals corresponding to each unit, when the first unit charges the first data line to a preset voltage, the second unit simultaneously pre-charges the second data line; when the second unit charges the second data line to a preset voltage, the third unit simultaneously pre-charges the third data line; when the third unit charges the third data line to a preset voltage, the first unit simultaneously pre-charges the first data line.

**3**. The DEMUX circuit as claimed in claim **1**, wherein the DEMUX circuit is for indium gallium zinc oxide (IGZO) process.

**4**. The DEMUX circuit as claimed in claim **1**, wherein the DEMUX circuit is for amorphous silicon (a-Si) process.

**5**. The DEMUX circuit as claimed in claim **1**, wherein the DEMUX circuit is connected to an RGB display panel for outputting RGB data signals.

**6**. The DEMUX circuit as claimed in claim **5**, wherein the data bus uses every four periods as a cycle, and after continuously outputs RGB data signals, the data bus stays vacant for a period.

**7**. A demultiplexer (DEMUX) circuit, comprising:

a data bus, a first data line, a second data line and a third data line, connected respectively to the data bus and a first unit, a second unit and a third unit respectively corresponding to the first, second and third data lines;

each unit respectively comprising: a first thin film transistor (TFT), a second TFT, a third TFT, and a capacitor, and inputting corresponding a first, a second, and a third switch signals; the first TFT having a gate inputting the first switch signal, and a source and a drain irrespectively inputting to the first switch signal and connected to a gate of the second TFT; the second TFT having a source and a drain respectively connected to the data bus and the corresponding data line; the capacitor having one end connected to the gate of the second TFT and the other connected to the second switch signal; the third TFT having a gate inputting the third switch signal, a source and a drain respectively connected to the gate of the second TFT and a constant low voltage;

for each unit, during operation, when the first switch signal being turned on, the first TFT and the second TFT being turned on, and the corresponding data line is pre-charged; when the first switch signal being turned off, the second switch signal being turned on and the corresponding data line being charged to a preset voltage;

wherein four switch signals being used for inputting to the first, second and third units, each unit selecting three switch signals out of the four to use as the first, second and third switch signals corresponding to the unit;

wherein the DEMUX circuit being connected to an RGB display panel for outputting RGB data signals, the four switch signals are square waveform having a duty cycle of 0.25, with a phase difference of ¼ cycle among one another.

**8**. The DEMUX circuit as claimed in claim **7**, wherein during operation, by controlling timing of the switch signals corresponding to each unit, when the first unit charges the first data line to a preset voltage, the second unit simultaneously pre-charges the second data line; when the second unit charges the second data line to a preset voltage, the third unit simultaneously pre-charges the third data line; when the third unit charges the third data line to a preset voltage, the first unit simultaneously pre-charges the first data line.

**9**. The DEMUX circuit as claimed in claim **7**, wherein the DEMUX circuit is for indium gallium zinc oxide (IGZO) process.

**10**. The DEMUX circuit as claimed in claim **7**, wherein the DEMUX circuit is for amorphous silicon (a-Si) process.

11. The DEMUX circuit as claimed in claim 7, wherein the data bus uses every four periods as a cycle, and after continuously outputs RGB data signals, the data bus stays vacant for a period.

* * * * *