US010374184B2

(12) United States Patent
Eguchi et al.

(10) Patent No.: US 10,374,184 B2
(45) Date of Patent: Aug. 6, 2019

(54) **LIGHT-EMITTING DEVICE AND MANUFACTURING METHOD THEREOF**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **15/332,195**

(22) Filed: **Oct. 24, 2016**

(65) **Prior Publication Data**

US 2017/0040400 A1 Feb. 9, 2017

Related U.S. Application Data

(60) Continuation of application No. 13/767,250, filed on Feb. 14, 2013, now Pat. No. 9,666,820, which is a (Continued)

(30) **Foreign Application Priority Data**

Sep. 16, 2009 (JP) 2009-215053

(51) **Int. Cl.**
H01L 29/10 (2006.01)
H01L 51/50 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 51/5012*** (2013.01); ***H01L 27/12*** (2013.01); ***H01L 27/1225*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC .. H01L 27/12; H01L 27/1225; H01L 51/5012
(Continued)

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(57) **ABSTRACT**

An object of the invention is to improve the reliability of a light-emitting device. Another object of the invention is to provide flexibility to a light-emitting device having a thin film transistor using an oxide semiconductor film. A light-emitting device has, over one flexible substrate, a driving circuit portion including a thin film transistor for a driving circuit and a pixel portion including a thin film transistor for a pixel. The thin film transistor for a driving circuit and the thin film transistor for a pixel are inverted staggered thin film transistors including an oxide semiconductor layer which is in contact with a part of an oxide insulating layer.

21 Claims, 30 Drawing Sheets

Related U.S. Application Data

division of application No. 12/880,269, filed on Sep. 13, 2010, now Pat. No. 8,377,762.

(51) **Int. Cl.**
H01L 27/12 (2006.01)
H01L 27/32 (2006.01)
H01L 51/00 (2006.01)
H01L 29/786 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 27/3262*** (2013.01); ***H01L 27/3272*** (2013.01); ***H01L 27/3276*** (2013.01); ***H01L 51/0097*** (2013.01); *H01L 27/124* (2013.01); *H01L 29/7869* (2013.01); *H01L 29/78678* (2013.01)

(58) **Field of Classification Search**
USPC 257/43, 98, E27.1, E27.113
See application file for complete search history.

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FIG. 1

100
122
129
191
192
110
106
170
109
107
108
147
102
162
165b
180
128
120
121
111
195
194
193

FIG. 2A

FIG. 2B

FIG. 2C

FIG. 3A

FIG. 3B

FIG. 3C

FIG. 4A

FIG. 4B

FIG. 5A

FIG. 5B

FIG. 6A
FIG. 6B
FIG. 6C
FIG. 6D
100
102
101
134
108
162
123
133
161
121
119
122
136f
136e
105b
140
136d
105a
136g
149
136c
165b
165a
136b
120
136a
139
104b
104a
185
164b
164a
138
192
191
127
125
117b
103
171
116
117a
107
106
146
109
181
167b
163
166
167a
126

FIG. 7A

FIG. 7B

FIG. 8A
FIG. 8B
FIG. 8C
FIG. 8D
100
102
101
143
134
108
162
123
133
142
161
121
119
136f
122
136e
105b
105a
136d
136g
149
136c
165b
165a
136b
136a
120
104b
104a
164b
164a
192
191
127
125
117b
103
172
116
117a
107
106
147
109
182
167b
163
166
167a
126

FIG. 9A

FIG. 9B

100
122
129
191
192
110
106
173
118
109
107
108
147
102
162
165b
168
183
128
121
195
194
193
145
111

FIG. 10

FIG. 11A1

FIG. 11A2

FIG. 11B1

FIG. 11B2

FIG. 12A

FIG. 12B

FIG. 13A

FIG. 13B

FIG. 14A

FIG. 14B

FIG. 14C

FIG. 14D

FIG. 15A

FIG. 15B

100
122
114
191
192
196
110
105b
106
170
109
107
108
147
102
162
115b
180
113
120
121
112
195
194
193

FIG. 16

FIG. 17A

FIG. 17B

FIG. 17C

FIG. 17D

FIG. 18A

FIG. 18B

FIG. 19

FIG. 20A

FIG. 20B

FIG. 20C

FIG. 21A

FIG. 21B

FIG. 22A

FIG. 22B

FIG. 23A

1413
1421
1423
1425
1411a
1411b
FIG. 23B
1411b
1427
1411a
FIG. 23D
FIG. 23C
1414
1413
1411a
1404
1411b

FIG. 24

FIG. 25A

FIG. 25B

FIG. 26

8104
8141
8100
8255
195
8142
194
191
192
110
106
170
8250
8144
109
193
107
147
8400
8252
180
8254

FIG. 27

304
8104
302
300
191
192
110
106
170
109
107
147
180
306
305
FIG. 28A
FIG. 28B

FIG. 29A

FIG. 29B

FIG. 30

LIGHT-EMITTING DEVICE AND MANUFACTURING METHOD THEREOF

TECHNICAL FIELD

The present invention relates to a light-emitting device including a layer containing an organic compound as a light-emitting layer, and a manufacturing method for the light-emitting device. For example, the present invention relates to an electronic device in which a light-emitting display device having an organic light-emitting element is mounted as a component.

Note that in this specification, a semiconductor device refers to all devices that can function by utilizing semiconductor characteristics, and electro-optic devices such as light-emitting devices, semiconductor circuits, and electronic devices are all semiconductor devices.

BACKGROUND ART

A light-emitting element using an organic compound as a light-emitting body, which has features such as thinness, lightness, high-speed response, and DC drive at a low voltage, has been examined to be applied to a next-generation flat panel display or next-generation lighting. In particular, a display device in which light-emitting elements are arranged in matrix is considered to have advantages in a wide viewing angle and excellent visibility over a conventional liquid crystal display device.

A light-emitting mechanism of a light-emitting element is thought as follows: when voltage is applied between a pair of electrodes with an EL layer interposed therebetween, electrons injected from a cathode and holes injected from an anode are recombined at emission centers in the EL layer to form molecular excitons, and the molecular excitons release energy and emit light when relax to the ground state. Singlet excitation and triplet excitation are known as excited states, and it is considered that light emission can probably be achieved through either of the excited states.

An EL layer included in a light-emitting element has at least a light-emitting layer. In addition, the EL layer can have a stacked-layer structure including a hole-injection layer, a hole-transport layer, an electron-transport layer, an electron-injection layer, or the like, in addition to the light-emitting layer.

Further, as a material having semiconductor characteristics, metal oxides attracts attention. Examples of such metal oxides having semiconductor characteristics include tungsten oxide, tin oxide, indium oxide, zinc oxide, and the like. Thin film transistors in which a channel formation region is formed of such metal oxides having semiconductor characteristics are already known (Patent Documents 1 and 2).

Furthermore, a TFT including an oxide semiconductor has high field-effect mobility. Thus, the TFT can be used to form a driving circuit of a display device or the like.

REFERENCE

Patent Document

[Patent Document 1] Japanese Published Patent Application No. 2007-123861

[Patent Document 2] Japanese Published Patent Application No. 2007-096055

DISCLOSURE OF INVENTION

For a thin film transistor using an oxide semiconductor film, high speed operation, a comparatively easy manufacturing process, and sufficient reliability are required.

One object of the present invention is to improve operation characteristics and reliability of a thin film transistor using an oxide semiconductor film.

In particular, a thin film transistor used for a driving circuit portion preferably operates at high speed.

For example, the operation speed becomes higher when the channel length (L) of a thin film transistor is shortened or when the channel width (W) is increased. However, in the case where the channel length (L) is shortened, there is a problem of switching characteristics, for example, an on/off ratio becomes small. In addition, when the channel width (W) is increased, there is a problem in that the capacity load of a thin film transistor itself is increased.

Therefore, an object of the present invention is also to provide a light-emitting device including a thin film transistor having stable electric characteristics even when the channel length is short.

In addition, when a plurality of circuits which are different from each other is formed over an insulating surface, for example, when a pixel portion and a driving circuit portion are formed over one substrate, excellent switching characteristics such as a high on/off ratio are needed for a thin film transistor used for the pixel portion, while high operation speed is needed for a thin film transistor used for the driving circuit portion. In particular, a thin film transistor used for a driving circuit portion preferably operates at high speed, since writing time of a display image is reduced as a resolution of a display device is increased.

Another object of the present invention is to reduce variations in electric characteristics of a thin film transistor using an oxide semiconductor film.

Still another object of the present invention is to give flexibility to a light-emitting device having a thin film transistor using an oxide semiconductor film.

A thin film transistor including a light-emitting element and an oxide semiconductor layer is formed over a flexible substrate, and a flexible light-emitting device is manufactured.

A thin film transistor including a light-emitting element and an oxide semiconductor layer may be directly formed over a flexible substrate. Alternatively, a thin film transistor including a light-emitting element and an oxide semiconductor layer may be formed over a manufacturing substrate, and after that, the thin film transistor may be separated and transferred to a flexible substrate. Note that in order to separate and transfer a thin film transistor from a manufacturing substrate to a flexible substrate, a separation layer is provided between the manufacturing substrate and the thin film transistor including a light-emitting element and an oxide semiconductor layer.

For a flexible substrate, for example, a polyester resin such as polyethylene terephthalate (PET) or polyethylene naphthalate (PEN), a polyacrylonitrile resin, a polyimide resin, a polymethyl methacrylate resin, a polycarbonate (PC) resin, a polyethersulfone (PES) resin, a polyamide resin, a cycloolefin resin, a polystyrene resin, a polyamide imide resin, or a polyvinylchloride resin can be preferably used. A structure body in which a fibrous body is impregnated with an organic resin (so-called prepreg) may also be used as a flexible substrate.

In addition, a metal substrate which is made thin enough to have flexibility may be used. The metal substrate is provided on the side through which light is not extracted. A material for forming the metal substrate is not limited to a particular material, but aluminum, copper, nickel, an alloy of metal such as an aluminum alloy or stainless steel, or the like can be preferably used.

One embodiment of the present invention is a light-emitting device including: a driving circuit portion having a thin film transistor for a driving circuit; and a pixel portion having a thin film transistor for a pixel, which are formed over one flexible substrate. The thin film transistor for a driving circuit and the thin film transistor for a pixel each include: a gate electrode layer, a gate insulating layer over the gate electrode layer, an oxide semiconductor layer over the gate insulating layer, a source electrode layer and a drain electrode layer over the oxide semiconductor layer, and an oxide insulating layer over the oxide semiconductor layer, the source electrode layer, and the drain electrode layer, which is in contact with a part of the oxide semiconductor layer. In the pixel portion, a color filter layer is provided over the oxide insulating layer, and a stack of a first electrode layer, an EL layer, and a second electrode layer, which is electrically connected to the thin film transistor for a pixel, is provided over the color filter layer. In the thin film transistor for a driving circuit, a conductive layer overlapping with the gate electrode layer and the oxide semiconductor layer is provided over the oxide insulating layer. The gate electrode layer, the source electrode layer, and the drain electrode layer are each a metal conductive film.

Another embodiment of the present invention is a light-emitting device including: a driving circuit portion having a thin film transistor for a driving circuit; and a pixel portion having a thin film transistor for a pixel, which are formed over one flexible substrate. The thin film transistor for a driving circuit and the thin film transistor for a pixel each include: a gate electrode layer, a gate insulating layer over the gate electrode layer, an oxide semiconductor layer over the gate insulating layer, a source electrode layer and a drain electrode layer over the oxide semiconductor layer, and an oxide insulating layer over the oxide semiconductor layer, the source electrode layer, and the drain electrode layer, which is in contact with a part of the oxide semiconductor layer. In the pixel portion, a color filter layer is provided over the oxide insulating layer, and a stack of a first electrode layer, an EL layer, and a second electrode layer, which is electrically connected to the thin film transistor for a pixel through a connection electrode layer, is provided over the color filter layer. In the thin film transistor for a driving circuit, a conductive layer overlapping with the gate electrode layer and the oxide semiconductor layer is provided over the oxide insulating layer. The gate electrode layer, the source electrode layer, and the drain electrode layer are each a metal conductive film.

As the thin film transistor for a pixel and the thin film transistor for a driving circuit, an inverted staggered thin film transistor with a bottom-gate structure is used. The thin film transistor for a pixel and the thin film transistor for a driving circuit are each a channel-etched thin film transistor in which the oxide insulating film is provided in contact with the oxide semiconductor layer exposed between the source electrode layer and the drain electrode layer.

The thin film transistor for a driving circuit has a structure in which the oxide semiconductor layer is sandwiched between the gate electrode and the conductive layer. With this structure, variation in threshold voltage of the thin film transistor can be reduced; accordingly, a light-emitting device including the thin film transistor with stable electric characteristics can be provided. The conductive layer may have the same potential as the gate electrode layer or may have a floating potential or a fixed potential such as GND potential or 0 V. By setting the potential of the conductive layer to an appropriate value, the threshold voltage of the thin film transistor can be controlled.

The thin film transistor for a pixel and a pixel electrode may be formed in direct contact with each other or may be electrically connected through the connection electrode layer. As the connection electrode layer, a film including an element selected from Al, Cr, Cu, Ta, Ti, Mo, and W as its main component or a stacked-layer film including the film and an alloy film of any of the elements can be used.

The conductive layer formed over the oxide semiconductor layer of the thin film transistor for a driving circuit, a first wiring (also referred to as a terminal or a connecting electrode), and a second wiring (also referred to as a terminal or a connecting electrode) may be formed in the same process as the pixel electrode using indium oxide, an indium oxide-tin oxide alloy, an indium oxide-zinc oxide alloy, or oxide conductive materials such as zinc oxide, or in the same process as the connecting electrode layer using a method material such as a film including an element selected from Al, Cr, Cu, Ta, Ti, Mo, and W as its main component or an alloy film of any of the elements.

In addition, light-emitting elements emitting light of a plurality of emission colors, and thin film transistors for pixels which are electrically connected to the light-emitting elements, may be formed over one substrate, so that a light-emitting device such as a display device can be manufactured.

Further, a plurality of light-emitting elements emitting white light may be provided and an optical film, specifically color filters may be provided so as to overlap with light-emitting regions of the light-emitting elements, whereby a light-emitting display device capable of full-color display can be manufactured. Note that in this specification, the color filter refers not to a whole film including color filter layers with three colors (e.g., a red color filter, a blue color filter, and a green color filter) in addition to a black matrix or an overcoat, but to a color filter with one color.

One embodiment of the present invention to realize the above structure is a method for manufacturing a light-emitting device including the steps of: forming a gate electrode layer using a metal conductive film over a flexible substrate having an insulating surface and including a driving circuit portion and a pixel portion; forming a gate insulating layer over the gate electrode; forming an oxide semiconductor layer over the gate insulating layer; forming a source electrode layer and a drain electrode layer using a metal conductive film, over the oxide semiconductor layer which is dehydrated or dehydrogenated and is not exposed to air so as to prevent water or hydrogen from entering again; forming an oxide insulating layer over the oxide semiconductor layer, the source electrode layer, and the drain electrode layer, which is in contact with a part of the oxide semiconductor layer, thereby forming a thin film transistor for a driving circuit over the driving circuit portion, and forming a thin film transistor for a pixel over the pixel portion; in the pixel portion, forming a color filter layer over the oxide insulating layer, forming a first electrode layer over the color filter layer, which is electrically connected to the thin film transistor for a pixel, forming an EL layer over the first electrode layer, and forming a second electrode layer over the EL layer; and in the driving circuit portion, forming a conductive layer, in the same process as the first electrode layer, over the oxide insulating layer overlapping with the gate electrode layer and the oxide semiconductor layer of the thin film transistor for a driving circuit.

Another embodiment of the present invention to realize the above structure is a method for manufacturing a light-emitting device including the steps of: forming a gate

electrode layer over a flexible substrate having an insulating surface and including a driving circuit portion and a pixel portion; forming a gate insulating layer over the gate electrode using a metal conductive film; forming an oxide semiconductor layer over the gate insulating layer; forming a source electrode layer and a drain electrode layer using a metal conductive film, over the oxide semiconductor layer which is dehydrated or dehydrogenated and is not exposed to air so as to prevent water or hydrogen from entering again; forming an oxide insulating layer over the oxide semiconductor layer, the source electrode layer and the drain electrode layer, which is in contact with a part of the oxide semiconductor layer, thereby forming a thin film transistor for a driving circuit over the driving circuit portion, and forming a thin film transistor for a pixel over the pixel portion; in the pixel portion, forming a color filter layer over the oxide insulating layer, forming a first electrode layer over the color filter layer, which is electrically connected to the thin film transistor for a pixel through a connection electrode layer; forming an EL layer over the first electrode layer, and forming a second electrode layer over the EL layer in the driving circuit portion, and forming a conductive layer in the same process as the connection electrode layer, over the oxide insulating layer overlapping with the gate electrode layer and the oxide semiconductor layer of the thin film transistor for a driving circuit.

Another embodiment of the present invention to realize the above structure is a method for manufacturing a light-emitting device including the steps of: forming a separation layer over a manufacturing substrate having an insulating surface and including a driving circuit portion and a pixel portion; in the driving circuit portion, forming a thin film transistor for a driving circuit having an oxide semiconductor layer over the separation layer; in the pixel portion, forming a thin film transistor for a pixel having an oxide semiconductor layer over the separation layer and forming a first electrode layer electrically connecting to the thin film transistor for a pixel; transferring the thin film transistor for a driving circuit, the thin film transistor for a pixel, and the first electrode layer from the manufacturing substrate to a supporting substrate using the separation layer; transferring to a flexible substrate the thin film transistor for a driving circuit, the thin film transistor for a pixel, and the first electrode layer which have been transferred to the supporting substrate forming an EL layer over the first electrode layer which has been transferred to the flexible substrate; and forming a second electrode layer over the EL layer.

Another embodiment of the present invention to realize the above structure is a method for manufacturing a light-emitting device including the steps of; forming a separation layer over a manufacturing substrate having an insulating surface and including a driving circuit portion and a pixel portion; in the driving circuit portion, forming a thin film transistor for a driving circuit having an oxide semiconductor layer over the separation layer; in the pixel portion, forming a thin film transistor for a pixel having an oxide semiconductor layer over the separation layer; forming a first electrode layer electrically connected to the thin film transistor for a pixel; transferring the thin film transistor for a driving circuit, the thin film transistor for a pixel, and the first electrode layer from the manufacturing substrate to a supporting substrate using the separation layer; transferring to a flexible substrate the thin film transistor for a driving circuit, the thin film transistor for a pixel, and the first electrode layer which have been transferred to the supporting substrate; forming an EL layer over the first electrode layer which has been transferred to the flexible substrate; forming a second electrode layer over the EL layer; and forming a flexible metal substrate over the second electrode layer so that the driving circuit portion and the pixel portion are sealed with the flexible metal substrate.

Note that in a photolithography steps in the above-described manufacturing process of a light-emitting device, an etching step may be performed with the use of a mask layer formed using a multi-tone mask which is a light-exposure mask through which light is transmitted so as to have a plurality of intensities.

Since a mask layer formed with the use of a multi-tone mask has a plurality of film thicknesses and further can be changed in shape by performing etching on the mask layer, the mask layer can be used in a plurality of etching steps for processing a film into different patterns. Therefore, a mask layer corresponding to at least two kinds or more of different patterns can be formed by one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography steps can be also reduced, whereby simplification of the process can be realized.

With the above structure, at least one of the above problems can be resolved.

For example, the oxide semiconductor used in this specification is formed into a thin film represented by $InMO_3(ZnO)_m$ (m>0), and the thin film is used to manufacture a thin film transistor. Note that M denotes one metal element or a plurality of metal elements selected from Ga, Fe, Ni, Mn, and Co. As an example, M may be Ga or may include the above metal element in addition to Ga, such as M may be Ga and Ni or Ga and Fe. Further, in the above oxide semiconductor, in some cases, a transition metal element such as Fe or Ni or an oxide of the transition metal is contained as an impurity element in addition to a metal element contained as M. In this specification, an oxide semiconductor layer whose composition formula is represented as $InMO_3(ZnO)_m$ (m>0) where an oxide semiconductor at least Ga is included as M is referred to as an In—Ga—Zn—O-based oxide semiconductor, and a thin film thereof is also referred to as an In—Ga—Zn—O-based non-single-crystal film.

As a metal oxide used for the oxide semiconductor layer, any of the following metal oxides can be used in addition to the above: an In—Sn—Zn—O-based metal oxide; an In—Al—Zn—O-based metal oxide; a Sn—Ga—Zn—O-based metal oxide; an Al—Ga—Zn—O-based metal oxide; a Sn—Al—Zn—O-based metal oxide; an In—Zn—O-based metal oxide; a Sn—Zn—O-based metal oxide; an Al—Zn—O-based metal oxide; an In—O-based metal oxide; a Sn—O-based metal oxide; and a Zn—O-based metal oxide. Silicon oxide may be contained in the oxide semiconductor layer formed using any of the above metal oxides.

The oxide semiconductor preferably includes In, and more preferably, In and Ga. In order to obtain an i-type (intrinsic) oxide semiconductor layer, it is effective to perform a dehydration or dehydrogenation process.

In the case where heat treatment is performed in an atmosphere of an inert gas such as nitrogen or a rare gas (for example, argon or helium), the oxide semiconductor layer is changed into an oxygen-deficient oxide semiconductor layer by the heat treatment. Thus, a low-resistant oxide semiconductor layer, that is, an n-type (such as n^--type) oxide semiconductor layer is formed. Then, the oxide semiconductor layer is brought into an oxygen-excess state by formation of an oxide insulating film which is in contact with the oxide semiconductor layer and heat treatment after the formation of the oxide insulating film, so that a high-

resistance oxide semiconductor layer, that is, an i-type oxide semiconductor layer is formed. This process can also be referred to as solid phase oxidation by which the oxide semiconductor layer is placed in an oxygen-excess state. In this manner, a light-emitting device including a thin film transistor having high electric characteristics and high reliability can be manufactured and provided.

For dehydration or dehydrogenation, heat treatment is performed in an inert gas atmosphere of nitrogen or a rare gas (such as argon or helium) at a temperature of 400° C. to 750° C., preferably 420° C. to 570° C., so that impurities such as moisture included in the oxide semiconductor layer are reduced. Further, water (H_2O) can be prevented from entering again in the oxide semiconductor layer later.

The heat treatment for dehydration or dehydrogenation is preferably performed in a nitrogen atmosphere with an H_2O concentration of 20 ppm or lower. Alternatively, the heat treatment may be performed in ultra-dry air with an H_2O concentration of 20 ppm or lower.

The oxide semiconductor layer is subjected to heat treatment for dehydration or dehydrogenation under a condition that two peaks of water or at least one peak of water at around 300° C. is not detected even if TDS is performed at up to 450° C. on the oxide semiconductor layer after being subjected to dehydration or dehydrogenation. Therefore, even if TDS is performed at up to 450° C. on a thin film transistor including an oxide semiconductor layer subjected to dehydration or dehydrogenation, at least the peak of water at around 300° C. is not detected.

In addition, when the temperature is lowered from a heating temperature T at which dehydration or dehydrogenation is performed, it is important to prevent the dehydrated or dehydrogenated oxide semiconductor layers from being exposed to air by continuously using a furnace in which dehydration or dehydrogenation is performed, so that water or hydrogen is prevented from entering the oxide semiconductor layers. A thin film transistor is formed using an oxide semiconductor layer obtained by changing an oxide semiconductor layer into a low-resistant oxide semiconductor layer, that is, an n-type (such as n^--type) oxide semiconductor layer by dehydration or dehydrogenation, and then by changing the low-resistant oxide semiconductor layer into a high-resistant oxide semiconductor layer so as to be an i-type semiconductor layer. In that case, the threshold voltage (Vth) of the thin film transistor can be positive value, so that a so-called normally-off switching element can be realized. It is desirable for a semiconductor device (a light-emitting device) that a channel be formed with a threshold voltage that is a positive value and as close to 0 V as possible. If the threshold voltage of the thin film transistor is negative, the thin film transistor tends to be a so-called normally on, in other words, a current flows between the source electrode and the drain electrode even when the gate voltage is 0 V. In an active matrix display device, the electric characteristics of a thin film transistor included in a circuit are important and significantly affect the performance of the display device. A threshold voltage value is specifically important in the electric characteristics of a thin film transistor. In the case where a positive value of the threshold voltage is high or the threshold voltage is a negative value even when the field-effect mobility is high, it is difficult to control the circuit. Further, in the case of a thin film transistor having a large absolute value of the threshold voltage, the thin film transistor cannot perform switching function at low driving voltage and may be a load. In the case of an n-channel thin film transistor, it is desirable that a channel be formed and a drain current begins to flow only when the positive voltage is applied to a gate. It is unsuitable for a thin film transistor used in a circuit that a channel is not formed unless driving voltage is raised and a channel is formed and a drain current begins to flow even in a negative voltage state.

Furthermore, the gas atmosphere in which the temperature is lowered from the heat temperature T may be switched to a gas atmosphere which is different from the gas atmosphere in which the temperature is raised to the heat temperature T. For example, cooling is performed while the furnace used for dehydration or dehydrogenation is filled with a high-purity oxygen gas, a high-purity N_2O gas, or an ultra-dry air (with a dew point of −40° C. or lower, preferably −60° C. or lower) without exposure to the air.

By using an oxide semiconductor film cooled slowly (or cooled) in an atmosphere that does not contain moisture (with a dew point of −40° C. or lower, preferably −60° C. or lower) after moisture contained in the film is reduced by heat treatment for dehydration or dehydrogenation, the electric characteristics of a thin film transistor are improved and high-performance thin film transistors that can be mass-produced are realized.

In this specification, heat treatment in an inert gas atmosphere of nitrogen or a rare gas (such as argon or helium) is referred to as heat treatment for dehydration or dehydrogenation. In this specification, "dehydrogenation" does not indicate elimination of only H_2 by heat treatment. For convenience, elimination of H, OH, and the like is referred to as "dehydration or dehydrogenation".

In the case where heat treatment is performed in an atmosphere of an inert gas such as nitrogen or a rare gas (such as argon or helium), the oxide semiconductor layer is changed into an oxygen-deficient oxide semiconductor layer by the heat treatment to be a low-resistance oxide semiconductor layer, that is, an n-type (such as n^--type) oxide semiconductor layer.

Moreover, a region overlapping with the drain electrode layer is formed as a high-resistance drain region (also referred to as an HRD region) which is an oxygen-deficient region. In addition, a region overlapping with the source electrode layer is formed as a high-resistance source region (also referred to as an HRS region) which is an oxygen-deficient region.

Specifically, the carrier concentration of the high-resistance drain region is $1\times10^{18}/cm^3$ or higher and is at least higher than the carrier concentration of the channel formation region (less than $1\times10^{18}/cm^3$). Note that the carrier concentration in this specification refers to a value of carrier concentration obtained by Hall effect measurement at room temperature.

The channel formation region is formed by placing at least a part of the dehydrated or dehydrogenated oxide semiconductor layer in an oxygen-excess state to have higher resistance, that is, to become an i-type region. Note that as the treatment for placing the dehydrated or dehydrogenated oxide semiconductor layer in an oxygen-excess state, the following treatment is given: formation of an oxide insulating film which is in contact with the dehydrated or dehydrogenated oxide semiconductor layer by a sputtering method; heat treatment or heat treatment in an atmosphere including oxygen, or cooling treatment in an oxygen atmosphere or ultra-dry air (having a dew point of −40° C. or lower, preferably −60° C. or lower) after heat treatment in an inert gas atmosphere, after the deposition of the oxide insulating film; or the like.

Further, in order to use at least a part (a portion overlapping with a gate electrode layer) of the dehydrated or

dehydrogenated oxide semiconductor layer as the channel formation region, the oxide semiconductor layer may be selectively made to be in an oxygen-excess state so as to be a high-resistance oxide semiconductor layer, that is, an i-type oxide semiconductor layer. The channel formation region can be formed in the following manner: a source electrode layer and a drain electrode layer formed using metal electrodes of Ti or the like are formed on and in contact with the dehydrated or dehydrogenated oxide semiconductor layer and exposure regions that do not overlap with the source electrode layer and the drain electrode layer are selectively made to be in an oxygen-excess state. When the exposure regions are selectively made to be in an oxygen-excess state, a first high-resistance source region overlapping with the source electrode layer and a second high-resistance drain region overlapping with the drain electrode layer are formed, and a region between the first high-resistance source region and the second high-resistance drain region serves as the channel formation region. That is, a channel length of the channel formation region is formed between the source electrode layer and the drain electrode layer in a self-aligned manner.

In this manner, a light-emitting device including a thin film transistor having high electric characteristics and high reliability can be manufactured and provided.

Note that by forming the high-resistance drain region in the oxide semiconductor layer overlapping with the drain electrode layer, the reliability can be improved when a driving circuit is formed. Specifically, by forming the high-resistance drain region, the conductivity can vary stepwise from the drain electrode layer to the high-resistance drain region and the channel formation region. Therefore, in the case where the thin film transistor operates with the drain electrode layer connected to a wiring for supplying a high power supply potential VDD, the high-resistance drain region serves as a buffer and a high electric field is not applied locally even if a high electric field is applied between the gate electrode layer and the drain electrode layer, so that the withstand voltage of the thin film transistor can be improved.

In addition, the high-resistance drain region and the high-resistance source region are formed in the oxide semiconductor layer overlapping with the drain electrode layer and the source electrode layer, respectively, whereby reduction in leakage current can be achieved in the channel formation region when forming the driving circuit. In particular, by forming the high-resistance drain region, leakage current flowing between the drain electrode layer and the source electrode layer of the transistor flows through the drain electrode layer, the high-resistance drain region on the drain electrode layer side, the channel formation region, the high-resistance source region on the source electrode layer side, and the source electrode layer in this order. At this time, in the channel formation region, leakage current flowing from the high-resistance drain region on the drain electrode layer side to the channel formation region can be concentrated on the vicinity of an interface between the channel formation region and a gate insulating layer which has high resistance when the transistor is off. Thus, the amount of leakage current in a back channel portion (a part of a surface of the channel formation region, which is apart from the gate electrode layer) can be reduced.

Further, the high-resistance source region overlapping with the source electrode layer and the high-resistance drain region overlapping with the drain electrode layer, although depending on the width of the gate electrode layer, overlap with each other with a part of the gate electrode layer and the gate insulating layer interposed therebetween, and the intensity of an electric field in the vicinity of an end portion of the drain electrode layer can be reduced more effectively.

Furthermore, an oxide conductive layer may be formed between the oxide semiconductor layer and the source and drain electrodes. The oxide conductive layer preferably contains zinc oxide as a component and preferably does not contain indium oxide. For example, zinc oxide, zinc aluminum oxide, zinc aluminum oxynitride, or gallium zinc oxide can be used. The oxide conductive layer also functions as a low-resistance drain region (LRD, also referred to as an LRN (low-resistance n-type conductivity) region). Specifically, the carrier concentration of the low-resistance drain region is higher than that of the high-resistance drain region (the HRD region) and preferably in a range of $1\times10^{20}/cm^3$ to $1\times10^{21}/cm^3$. Provision of the oxide conductive layer between the oxide semiconductor layer and the source and drain electrodes can reduce contact resistance and realizes higher speed operation of the transistor. Accordingly, frequency characteristics of a peripheral circuit (a driving circuit) can be improved.

The oxide conductive layer and a metal layer for forming the source and drain electrodes can be formed in succession.

Moreover, the above-described first wiring and second wiring may be formed using a wiring which is formed by stacking a metal material and the same material as that of the oxide conductive layer functioning as an LRN or an LRD. By stacking the metal and the oxide conductive layer, coverage at the step such as an overlapping portion of wirings or an opening can be improved; thus, wiring resistance can be lowered. Further, effects of preventing local increase in resistance of a wiring due to migration or the like and preventing disconnection of a wiring can be expected; accordingly, a highly reliable light-emitting device can be provided.

Regarding the above-described connection between the first wiring and the second wiring, when the oxide conductive layer is sandwiched therebetween, it is expected to prevent increase in contact resistance which is caused by formation of an insulating oxide on a metal surface in the connection portion (contact portion); thus, a highly reliable light-emitting device can be provided.

Since a thin film transistor is easily broken due to static electricity or the like, a protective circuit for protecting the thin film transistor for a pixel portion is preferably provided over the same substrate as a gate line or a source line. The protective circuit is preferably formed with a non-linear element including an oxide semiconductor layer.

Note that the ordinal numbers such as "first" and "second" in this specification are used for convenience and do not denote the order of steps and the stacking order of layers. In addition, the ordinal numbers in this specification do not denote particular names which specify the present invention.

By using an oxide semiconductor layer, a light-emitting device including a thin film transistor having excellent electric characteristics and high reliability can be realized.

BRIEF DESCRIPTION OF DRAWINGS

In the accompanying drawings:

FIG. **1** is a view showing a light-emitting device;

FIGS. **2**A to **2**C are views showing a method for manufacturing a light-emitting device;

FIGS. **3**A to **3**C are views showing a method for manufacturing a light-emitting device;

FIGS. **4**A and **4**B are views showing a method for manufacturing a light-emitting device;

FIGS. **5**A and **5**B are views showing a method for manufacturing a light-emitting device;

FIGS. **6**A to **6**D are views showing a method for manufacturing a light-emitting device;

FIGS. **7**A and **7**B are views showing a method for manufacturing a light-emitting device;

FIGS. **8**A to **8**D are views showing a method for manufacturing a light-emitting device;

FIGS. **9**A and **9**B are views showing a method for manufacturing a light-emitting device;

FIG. **10** is a view showing a light-emitting device;

FIGS. **11**A**1**, **11**A**2**, **11**B**1**, and **11**B**2** are views showing a light-emitting device;

FIGS. **12**A and **12**B are block diagrams of a light-emitting device;

FIGS. **13**A and **13**B are views illustrating a configuration of a signal line driving circuit;

FIGS. **14**A to **14**D are circuit diagrams showing a configuration of a shift register;

FIG. **15**A is showing an equivalent circuit of a shift register and **15**B is timing charts showing an operation thereof;

FIG. **16** is a view showing a light-emitting device;

FIGS. **17**A to **17**D are views showing a method for manufacturing a light-emitting device;

FIGS. **18**A and **18**B are views showing a method for manufacturing a light-emitting device;

FIG. **19** is a view showing a pixel equivalent circuit of a light-emitting device;

FIGS. **20**A to **20**C are views showing a light-emitting device;

FIGS. **21**A and **21**B are views showing a light-emitting element;

FIGS. **22**A and **22**B are views showing a light-emitting device;

FIGS. **23**A to **23**D are views showing an electronic device;

FIG. **24** is a view showing an electronic device;

FIGS. **25**A and **25**B are views showing an electronic device;

FIG. **26** is a view showing electronic devices;

FIG. **27** is a view showing a light-emitting device;

FIGS. **28**A and **28**B are views showing a method for manufacturing a light-emitting device;

FIGS. **29**A and **29**B are views showing a method for manufacturing a light-emitting device; and

FIG. **30** is a view showing a method for manufacturing a light-emitting device.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiments of the present invention will be described with reference to the accompanying drawings. Note that the present invention is not limited to the following description, and various changes for the modes and details thereof will be apparent to those skilled in the art unless such changes depart from the spirit and the scope of the invention. Therefore, the present invention should not be interpreted as being limited to the following description of the embodiments. In the structures to be given below, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and explanation thereof will not be repeated.

Embodiment 1

A light-emitting device including a thin film transistor and a manufacturing process thereof will be described with reference to FIG. **1**, FIGS. **2**A to **2**C, FIGS. **3**A to **3**C, FIGS. **4**A and **4**B, FIGS. **5**A and **5**B, and FIGS. **11**A**1**, **11**A**2**, **11**B**1**, and **11**B**2**.

FIG. **1** shows a light-emitting device which is one mode of the present invention. The light-emitting device in FIG. **1** includes, over a flexible substrate **100**, a pixel portion including a light-emitting element, a thin film transistor **170**, and a capacitor **147**, and a driving circuit portion including a thin film transistor **180**. Further, a first terminal **121**, a connection electrode **120**, and a terminal electrode **128** for connection are provided in a terminal portion for a gate wiring and a second terminal **122** and a terminal electrode **129** for connection are provided in a terminal portion of a source wiring. In addition, an oxide insulating film **107** and a protective insulating layer **106** are formed over the thin film transistor **180** and the thin film transistor **170**.

The light-emitting element is formed using a stack of a first electrode layer **110**, an EL layer **194**, and a second electrode layer **195**. A drain electrode layer of the thin film transistor **170** and the first electrode layer **110** are formed so as to be in contact with each other, so that the light-emitting element and the thin film transistor **170** are electrically connected to each other. In the pixel portion, a color filter layer **191** is formed over the protective insulating layer **106**. The color filter layer **191** is covered with an overcoat layer **192**, and the protective insulating layer **109** is further formed thereover. The first electrode layer **110** is formed over the protective insulating layer **109**. Further, a partition **193** separating between light-emitting elements is formed over the thin film transistor **170**.

In the thin film transistor **180** of the driving circuit portion, a conductive layer **111** is provided over a gate electrode layer and a semiconductor layer, and a drain electrode layer **165***b* is electrically connected to a conductive layer **162** which is formed in the same step as the gate electrode layer.

For the flexible substrate **100**, for example, a polyester resin such as polyethylene terephthalate (PET) or polyethylene naphthalate (PEN), a polyacrylonitrile resin, a polyimide resin, a polymethyl methacrylate resin, a polycarbonate (PC) resin, a polyethersulfone (PES) resin, a polyamide resin, a cycloolefin resin, a polystyrene resin, a polyamide imide resin, a polyvinylchloride resin, or the like is preferably used. Note that a structure body in which a fibrous body is impregnated with an organic resin (so-called prepreg) may be used as the flexible substrate.

The light-emitting device shown in this embodiment is a bottom emission type in which light is emitted through the flexible substrate **100** side, so that a substrate having a light-transmitting property is used as the flexible substrate **100**. On the other hand, in the case where the light-emitting device shown in this embodiment is a top emission type in which light emitted through the opposite surface of the flexible substrate **100**, a metal substrate which is made thin enough to have flexibility and does not have light-transmitting properties may be used as the flexible substrate **100**. The metal substrate is formed over a side through which light is not emitted. A material for forming the metal substrate is not limited to a particular material, but it is preferable to use aluminum, copper, nickel, an alloy of metal such as an aluminum alloy or stainless steel, or the like.

Hereinafter, a manufacturing method will be described in detail with reference to FIGS. **2**A to **2**C, FIGS. **3**A to **3**C, FIGS. **4**A and **4**B, FIGS. **5**A and **5**B, and FIGS. **11**A**1**, **11**A**2**, **11**B**1**, and **11**B**2**. FIGS. **2**A to **2**C, FIGS. **3**A to **3**C, FIGS. **4**A and **4**B, and FIGS. **5**A and **5**B each correspond to a cross-sectional view of the light-emitting device.

A conductive layer is formed over the entire surface of the flexible substrate **100** having an insulating surface, and then a first photolithography step is performed to form a resist mask. Unnecessary portions of the conductive layer are removed by etching to form wirings and electrodes (a gate electrode layer **101**, a gate electrode layer **161**, the conductive layer **162**, a capacitor wiring layer **108**, and the first terminal **121**). Etching is preferably performed so that end portions of the wirings and electrodes have tapered shapes as shown in FIG. **2**A, because coverage with a film stacked thereover can be improved. Note that the gate electrode layer **101** and the gate electrode layer **161** are each included in the gate wiring.

Although there is no particular limitation on a flexible substrate which can be used as the flexible substrate **100** having an insulating surface, the flexible substrate needs to have heat resistance enough to withstand at least heat treatment to be performed later.

An insulating film serving as a base film may be provided between the flexible substrate **100**, and the gate electrode layer **101**, the gate electrode layer **161**, the conductive layer **162**, the capacitor wiring layer **108**, and the first terminal **121**. The base film has a function of preventing diffusion of an impurity element from the flexible substrate **100**, and can be formed with a single-layer or a stacked-layer using one or more of a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

The gate electrode layer **101**, the gate electrode layer **161**, the conductive layer **162**, the capacitor wiring layer **108**, and the first terminal **121** can be formed with a single-layer or a stacked-layer using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium; or an alloy material which contains any of these materials as a main component.

For example, as a two-layer structure of each of the gate electrode layer **101**, the gate electrode layer **161**, the conductive layer **162**, the capacitor wiring layer **108**, and the first terminal **121**, the following structures are preferable: a two-layer structure of an aluminum layer and a molybdenum layer stacked thereover, a two-layer structure of a copper layer and a molybdenum layer stacked thereover, a two-layer structure of a copper layer and a titanium nitride layer or a tantalum nitride layer stacked thereover, and a two-layer structure of a titanium nitride layer and a molybdenum layer stacked thereover. As a stacked structure of layers, a stacked-layer of a tungsten layer or a tungsten nitride layer, an alloy of aluminum and silicon or an alloy of aluminum and titanium, and a titanium nitride layer or a titanium layer is preferable.

Next, a gate insulating layer **102** is formed over the gate electrode layer **101**, the gate electrode layer **161**, the conductive layer **162**, the capacitor wiring layer **108**, and the first terminal **121** (see FIG. **2**A).

The gate insulating layer **102** can be formed to have a single-layer of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, or an aluminum oxide layer or a stacked-layer thereof by a plasma CVD method, a sputtering method, or the like. For example, a silicon oxynitride layer may be formed using SiH_4, oxygen, and nitrogen as a film formation gas by a plasma CVD method. The thickness of the gate insulating layer **102** is set to 100 nm to 500 nm. In the case of a stacked structure, for example, a first gate insulating layer having a thickness from 50 nm to 200 nm and a second gate insulating layer having a thickness from 5 nm to 300 nm are stacked in this order.

In this embodiment, a silicon oxide layer having a thickness of 200 nm or less is formed by a plasma CVD method as the gate insulating layer **102**.

Then, an oxide semiconductor film **130** with a thickness of 2 nm to 200 nm is formed over the gate insulating layer **102** (see FIG. **2**B).

Note that before the oxide semiconductor film is formed by a sputtering method, dust on a surface of the gate insulating layer **102** is preferably removed by reverse sputtering in which an argon gas is introduced and plasma is generated. The reverse sputtering is a method in which voltage is applied to a substrate side with the use of an RF power supply in an argon atmosphere without applying voltage to a target side and plasma is generated in the vicinity of the substrate so that a substrate surface is modified. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, or the like may be used. Alternatively, an argon atmosphere to which oxygen, N_2O, or the like is added may be used. Further alternatively, an argon atmosphere to which Cl_2, CF_4, or the like is added may be used.

The oxide semiconductor film **130** is formed using any of the following films: an In—Ga—Zn—O-based non-single-crystal film, an In—Sn—Zn—O-based oxide semiconductor film, an In—Al—Zn—O-based oxide semiconductor film, a Sn—Ga—Zn—O-based oxide semiconductor film, an Al—Ga—Zn—O-based oxide semiconductor film, a Sn—Al—Zn—O-based oxide semiconductor film, an In—Zn—O-based oxide semiconductor film, a Sn—Zn—O-based oxide semiconductor film, an Al—Zn—O-based oxide semiconductor film, an In—O-based oxide semiconductor film, a Sn—O-based oxide semiconductor film, or a Zn—O-based oxide semiconductor film. In this embodiment, the oxide semiconductor film **130** is formed by a sputtering method with the use of an In—Ga—Zn—O-based oxide semiconductor target. Alternatively, the oxide semiconductor film **130** can be formed by a sputtering method under a rare gas (typically argon) atmosphere, an oxygen atmosphere, or an atmosphere of a rare gas (typically argon) and oxygen. When a sputtering method is employed, it is preferable that film formation be performed using a target containing SiO_2 of 2 wt % to 10 wt % and SiOx (x>0) which inhibits crystallization be contained in the oxide semiconductor film **130** so as to prevent crystallization at the time of the heat treatment for dehydration or dehydrogenation in a later step.

Here, the oxide semiconductor film is formed using an oxide semiconductor target containing In, Ga, and Zn (In_2O_3:Ga_2O_3:ZnO=1:1:1 [mol %], In:Ga:Zn=1:1:0.5 [atom %]) under conditions where the distance between the substrate and the target is 100 mm, the pressure is 0.2 Pa, and the direct current (DC) power supply is 0.5 kW in an atmosphere containing argon and oxygen (argon:oxygen=30 sccm:20 sccm, the proportion of the oxygen flow is 40%). Note that a pulse direct current (DC) power supply is preferable because dust can be reduced and the film thickness can be uniform. The In—Ga—Zn—O-based non-single-crystal film is formed to have a thickness of 5 nm to 200 nm. In this embodiment, as the oxide semiconductor film, an In—Ga—Zn—O-based non-single-crystal film having a thickness of 30 nm is formed using the In—Ga—Zn—O-based oxide semiconductor target by a sputtering method. In addition, as the oxide semiconductor target containing In, Ga, and Zn, a target having a composition ratio of In:Ga:Zn=1:1:1 [atom %] or In:Ga:Zn=1:1:2 [atom %] can be used.

Examples of a sputtering method include an RF sputtering method in which a high-frequency power source is used as

a sputtering power source, a DC sputtering method in which a DC power source is used as a sputtering power source, and a pulsed DC sputtering method in which a bias is applied in a pulsed manner. An RF sputtering method is mainly used in the case of forming an insulating film, and a DC sputtering method is mainly used in the case of forming a metal film.

Further, there is a multi-source sputtering apparatus in which a plurality of targets of different materials can be set. With the multi-source sputtering apparatus, films of different materials can be formed to be stacked in the same chamber, and a film of plural kinds of materials can be formed by electric discharge at the same time in the same chamber.

Furthermore, there are a sputtering apparatus provided with a magnet system inside the chamber and used for a magnetron sputtering, and a sputtering apparatus used for an ECR sputtering in which plasma generated with the use of microwaves is used without using glow discharge.

Moreover, as a film formation method by sputtering, there are also a reactive sputtering method in which a target substance and a sputtering gas component are chemically reacted with each other during film formation to form a thin compound film, and a bias sputtering method in which a voltage is also applied to a substrate during film formation.

Next, a second photolithography step is performed. A resist mask **137** is formed over the oxide semiconductor film **130**, and unnecessary portions of the oxide semiconductor film **130** and the gate insulating layer **102** are removed by etching to form a contact hole **119** reaching the first terminal **121** and a contact hole **123** reaching the conductive layer **162** in the gate insulating layer **102** (see FIG. **2**C).

Thus, when the contact holes are formed in the gate insulating layer **102** while the oxide semiconductor film **130** is formed over the entire surface of the gate insulating layer **102**, the resist mask is not in direct contact with the surface of the gate insulating layer **102**; accordingly, contamination of the surface of the gate insulating layer **102** (e.g., attachment of impurities or the like to the gate insulating layer **102**) can be prevented. Thus, a favorable state of the interface between the gate insulating layer **102** and the oxide semiconductor film **130** can be obtained, leading to improvement in reliability.

Alternatively, a resist pattern may be formed directly on the gate insulating layer, and then contact holes may be formed. In such a case, heat treatment is preferably performed to dehydrate or dehydrogenate the surface of the gate insulating film after removal of the resist. For example, impurities such as hydrogen and water included in the gate insulating layer may be removed by heat treatment (at 400° C. to 750° C.) under an inert gas (e.g., nitrogen, helium, neon, or argon) atmosphere or an oxygen atmosphere.

Next, the resist mask **137** is removed. The oxide semiconductor film **130** is etched with the use of resist masks **135***a* and **135***b* formed in a third photolithography step, so that island-shaped oxide semiconductor layers **131** and **132** are formed (see FIG. **3**A). Alternatively, the resist masks **135***a* and **135***b* used for forming the island-shaped oxide semiconductor layers may be formed by an ink-jet method. When the resist masks are formed by an ink-jet method, a photomask is not used, leading to reduction in manufacturing cost.

Next, the oxide semiconductor layers **131** and **132** are subjected to dehydration or dehydrogenation, so that dehydrated or dehydrogenated oxide semiconductor layers **133** and **134** are formed (see FIG. **3**B). The temperature of first heat treatment at which dehydration or dehydrogenation is performed is 400° C. to 750° C., preferably 425° C. or higher. Note that in the case where the temperature of the first heat treatment is 425° C. or higher, the heat treatment time may be one hour or less, while in the case where the temperature of the first heat treatment is lower than 425° C., the heat treatment time is set to more than one hour. Here, the substrate is introduced into an electric furnace which is one example of heat treatment apparatuses, and the oxide semiconductor layers are subjected to heat treatment in a nitrogen atmosphere. Then, the oxide semiconductor layers are not exposed to air so as to prevent water and hydrogen from entering the oxide semiconductor layers again. In this manner, the oxide semiconductor layers **133** and **134** are formed. In this embodiment, slow cooling is performed from the heating temperature T at which the oxide semiconductor layers are dehydrated or dehydrogenated to a temperature low enough to prevent water from entering again. Specifically, slow cooling is performed to a temperature that is lower than the heating temperature T by 100° C. or more, in a nitrogen atmosphere in one furnace. Without limitation to a nitrogen atmosphere, dehydration or dehydrogenation may be performed in a rare gas atmosphere such as helium, neon, or argon.

When the oxide semiconductor layers are subjected to heat treatment at 400° C. to 700° C., the dehydration or dehydrogenation of the oxide semiconductor layers can be achieved; thus, water (H_2O) can be prevented from being contained again in the oxide semiconductor layers in later steps.

Note that the heat treatment apparatus is not limited to the electric furnace, and for example, an RTA (rapid thermal annealing) apparatus such as a GRTA (gas rapid thermal annealing) apparatus or an LRTA (lamp rapid thermal annealing) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp. In addition, the LRTA apparatus may be provided with not only a lamp but also a device which heats an object to be processed by heat conduction or heat radiation from a heater such as a resistance heater. GRTA is a method of heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with an object to be processed by heat treatment, for example, nitrogen or a rare gas such as argon, is used. The heat treatment may be performed by an RTA method at 600° C. to 750° C. for several minutes.

Note that in the first heat treatment, it is preferable that water, hydrogen and the like be not contained in nitrogen, or the rare gas such as helium, neon, or argon. In particular, the heat treatment which is performed on the oxide semiconductor layers for dehydration or dehydrogenation at 400° C. to 750° C. is preferably performed in a nitrogen atmosphere in which the concentration of H_2O is 20 ppm or lower. Alternatively, it is preferable that nitrogen or a rare gas such as helium, neon, or argon introduced into an apparatus for heat treatment have purity of 6N (99.9999%) or higher, preferably, 7N (99.99999%) or higher; that is, an impurity concentration is set to 1 ppm or lower, preferably, 0.1 ppm or lower.

In some cases, the oxide semiconductor layers are crystallized to be microcrystalline films or polycrystalline films depending on the conditions of the first heat treatment or the material of the oxide semiconductor layers. For example, the oxide semiconductor layers may crystallize to become microcrystalline semiconductor layers having a degree of crystallization of 90% or more, or 80% or more. Further, depending on the conditions of the first heat treatment and

the material of the oxide semiconductor layers, the oxide semiconductor layers may become amorphous oxide semiconductor layers containing no crystalline component. Furthermore, in some cases, the oxide semiconductor film became an amorphous oxide film in which a microcrystal portion (the grain size of the microcrystal portion is 1 nm to 20 nm (typically, 2 nm to 4 nm)) is mixed. When high temperature heat treatment is performed using RTA (GRTA, LRTA), needle-like crystals might be generated longitudinally (in the film thickness direction) on the surface side of the oxide semiconductor film.

The first heat treatment of the oxide semiconductor layer can also be performed on the oxide semiconductor film **130** which has not been processed into the island-shaped oxide semiconductor layers **131** and **132**. In that case, after the first heat treatment, the substrate is taken out of the heating device and a photolithography step is performed.

The heat treatment for dehydration or dehydrogenation of the oxide semiconductor layers may be performed at any of the following timings after the oxide semiconductor layers are formed; after a source electrode and a drain electrode are formed over the oxide semiconductor layer; and after a passivation film is formed over the source electrode and the drain electrode.

Further, the step of forming the contact holes **123** and **119** in the gate insulating layer **102** as shown in FIG. **2**C may be performed after the oxide semiconductor film **130** is subjected to dehydration or dehydrogenation treatment.

Note that this etching step of the oxide semiconductor film is not limited to wet etching and dry etching may also be performed.

As the etching gas for dry etching, a gas containing chlorine (chlorine-based gas such as chlorine (Cl_2), boron chloride (BCl_3), silicon chloride ($SiCl_4$), or carbon tetrachloride (CCl_4)) is preferably used.

Alternatively, a gas containing fluorine (fluorine-based gas such as carbon tetrafluoride (CF_4), sulfur fluoride (SF_6), nitrogen fluoride (NF_3), or trifluoromethane (CHF_3)); hydrogen bromide (HBr); oxygen (O_2); any of these gases to which a rare gas such as helium (He) or argon (Ar) is added; or the like can be used.

As the dry etching method, a parallel plate RIE (reactive ion etching) method or an ICP (inductively coupled plasma) etching method can be used. In order to etch the films into desired shapes, the etching condition (the amount of electric power applied to a coil-shaped electrode, the amount of electric power applied to an electrode on a substrate side, the temperature of the electrode on the substrate side, or the like) is adjusted as appropriate.

As an etchant used for wet etching, a solution obtained by mixing phosphoric acid, acetic acid, nitric acid, or the like can be used. In addition, ITO-07N (produced by KANTO CHEMICAL CO., INC.) may also be used.

The etchant used in the wet etching is removed by cleaning together with the material which is etched off. The waste liquid including the etchant and the material etched off may be purified and the material may be reused. When a material such as indium included in the oxide semiconductor layer is collected from the waste liquid after the etching and reused, the resources can be efficiently used and the cost can be reduced.

The etching conditions (such as an etchant, etching time, and temperature) are adjusted as appropriate depending on the material so that the material can be etched into a desired shape.

Next, a metal conductive film is formed using a metal material over the oxide semiconductor layers **133** and **134** by a sputtering method or a vacuum evaporation method.

As a material of the metal conductive film, there are an element selected from Al, Cr, Cu, Ta, Ti, Mo, or W, an alloy including the above element, an alloy film in which some of the above elements are combined, and the like. Further, the metal conductive film may have a single-layer structure or a stacked-layer structure of two or more layers. For example, a single-layer structure of an aluminum film including silicon, a two-layer structure of an aluminum film and a titanium film stacked thereover, a three-layer structure in which a Ti film, an aluminum film, and a Ti film are stacked in this order, and the like can be given. Alternatively, a film, an alloy film, or a nitride film which contains aluminum (Al) and one or a plurality of elements selected from titanium (Ti), tantalum (Ta), tungsten (W), molybdenum (Mo), chromium (Cr), neodymium (Nd), and scandium (Sc) may be used.

In the case where heat treatment is performed after formation of the metal conductive film, the metal conductive film preferably has heat resistance enough to withstand the heat treatment.

Next, a fourth photolithography step is performed. Resist masks **136***a*, **136***b*, **136***c*, **136***d*, **136***e*, **136***f*, and **136***g* are formed, and unnecessary portions of the metal conductive film are removed by etching, so that a source electrode layer **105***a*, a drain electrode layer **105***b*, a source electrode layer **165***a*, the drain electrode layer **165***b*, a capacitor electrode layer **149**, the connection electrode **120**, and the second terminal **122** are formed (see FIG. **3**C).

Note that each material and etching conditions are adjusted as appropriate so that the oxide semiconductor layers **133** and **134** are not removed when the metal conductive film is etched.

In this embodiment, a Ti film is used as the metal conductive film, an In—Ga—Zn—O-based is used as the oxide semiconductor layers **133** and **134**, and an ammonia hydrogen peroxide solution (a mixture of ammonia, water, and a hydrogen peroxide solution) is used as an etchant.

In the fourth photolithography step, the connection electrode **120** and the second terminal **122**, which are formed using the same material as that of the source electrode layers **105***a* and **165***a* and the drain electrode layers **105***b* and **165***b*, are formed in the respective terminal portions. Note that the second terminal **122** is electrically connected to a source wiring (a source wiring including the source electrode layers **105***a* and **165***a*). The connection electrode **120** is formed in contact with the first terminal **121** in the contact hole **119** and electrically connected to the first terminal **121**.

Note that the resist masks **136***a*, **136***b*, **136***c*, **136***d*, **136***e*, **136***f*, and **136***g* used for forming the source electrode layers and the drain electrode layers may be formed by an ink-jet method. When the resist masks are formed by an ink-jet method, a photomask is not used, leading to reduction in manufacturing cost.

Next, the resist masks **136***a*, **136***b*, **136***c*, **136***d*, **136***e*, **136***f*, and **136***g* are removed, and an oxide insulating film **107** serving as a protective insulating film in contact with the oxide semiconductor layers **133** and **134** is formed.

At this stage, in the oxide semiconductor layers **133** and **134**, there are regions in contact with the oxide insulating film. Among these regions, the regions in which the gate electrode layers overlap with the oxide insulating film **107** with the gate insulating layer interposed therebetween are channel formation regions.

The oxide insulating film **107** can be formed to have a thickness of at least 1 nm or more by a sputtering method or the like, as appropriate, which is a method with which impurities such as water and hydrogen, are not mixed into the oxide insulating film **107**. In this embodiment, a silicon oxide film with a thickness of 300 nm is formed as the oxide insulating film **107** by a sputtering method. The substrate temperature in film formation may be room temperature to 300° C. In this embodiment, the substrate temperature is at room temperature. The silicon oxide film can be formed by a sputtering method in a rare gas (typically argon) atmosphere, an oxygen atmosphere, or an atmosphere including a rare gas (typically argon) and oxygen. Further, a silicon oxide target or a silicon target can be used as a target. For example, a silicon oxide can be formed by a sputtering method using a silicon target in an atmosphere of oxygen and nitrogen. As the oxide insulating film which is formed in contact with the oxide semiconductor layer whose resistance is reduced, an inorganic insulating film which does not include impurities such as moisture, a hydrogen ion, and OH^- and blocks entry of these from the outside is used. Typically, a silicon oxide film, a silicon nitride oxide film, an aluminum oxide film, or an aluminum oxynitride film is used.

Next, second heat treatment is performed in an inert gas atmosphere or a nitrogen atmosphere (at a preferable temperature from 200° C. to 400° C., e.g., from 250° C. to 350° C.). For example, the second heat treatment is performed in a nitrogen atmosphere at 250° C. for one hour. By the second heat treatment, part of the oxide semiconductor layers **133** and **134** which overlaps with the oxide insulating film **107** is heated in the state of being in contact with the oxide insulating film **107**.

Through the above-described steps, heat treatment for dehydration or dehydrogenation is performed on the oxide semiconductor layer after film formation to reduce the resistance, and then, part of the oxide semiconductor layer is selectively made to be in an oxygen-excess state.

As a result, in the oxide semiconductor layer **133**, a channel formation region **166** overlapping with the gate electrode layer **161** becomes an i-type channel formation region, and a high-resistance source region **167***a* overlapping with the source electrode layer **165***a* and a high-resistance drain region **167***b* overlapping with the drain electrode layer **165***b* are formed in a self-aligned manner; thus, an oxide semiconductor layer **163** is formed. Similarly, in the oxide semiconductor layer **134**, a channel formation region **116** overlapping with the gate electrode layer **101** becomes an i-type channel formation region, and a high-resistance source region **117***a* overlapping with the source electrode layer **105***a* and a high-resistance drain region **117***b* overlapping with the drain electrode layer **105***b* are formed in a self-aligned manner; thus, an oxide semiconductor layer **103** is formed.

By formation of the high-resistance drain regions **117***b* and **167***b* (or the high-resistance source regions **117***a* and **167***a*) in the oxide semiconductor layers **103** and **163** which overlap with the drain electrode layers **105***b* and **165***b* (and the source electrode layers **105***a* and **165***a*), respectively, reliability in a formed circuit can be improved. Specifically, by forming the high-resistance drain region **117***b*, the conductivity can vary stepwise from the drain electrode layer **105***b* to the high-resistance drain region **117***b* and the channel formation region **116**; similarly, by formation of the high-resistance drain region **167***b*, the conductivity can vary stepwise from the drain electrode layer **165***b* to the high-resistance drain region **167***b* and the channel formation region **166**. Therefore, when the transistors operate in the state of being connected to a wiring which supplies the drain electrode layers **105***b* and **165***b* with a high power source potential VDD, the high-resistance drain regions serve as buffers and a high electric field is not applied locally even if a high electric field is applied between the gate electrode layers **101** and **161** and the drain electrode layers **105***b* and **165***b*, so that the withstand voltage of the transistor can be improved.

In addition, by formation of the high-resistance drain regions **117***b* and **167***b* (or the high-resistance source regions **117***a* and **167***a*) in the oxide semiconductor layers **103** and **163** which overlap with the drain electrode layers **105***b* and **165***b* (and the source electrode layers **105***a* and **165***a*), respectively, leakage current in the channel formation regions **116** and **166** which may flow in a formed circuit can be reduced.

In this embodiment, after a silicon oxide film is formed by a sputtering method as the oxide insulating film **107**, heat treatment is performed at 250° C. to 350° C., whereby oxygen enters each of the oxide semiconductor layers from the exposed portion (the channel formation region) of the oxide semiconductor layer between the source region and the drain region, and is diffused thereinto. By formation of the silicon oxide film by a sputtering method, an excessive amount of oxygen can be contained in the silicon oxide film, and oxygen can enter the oxide semiconductor layers and can be diffused thereinto through the heat treatment. Oxygen enters the oxide semiconductor layers and is diffused thereinto, whereby the channel region can have higher resistance (such as i-type conductivity). Thus, normally-off thin film transistors can be obtained.

Further, the high-resistance source region or the high-resistance drain region in the oxide semiconductor layer is formed in the entire thickness direction in the case where the thickness of the oxide semiconductor layer is 15 nm or smaller. In the case where the thickness of the oxide semiconductor layer is 30 nm to 50 nm, in part of the oxide semiconductor layer, that is, in a region in the oxide semiconductor layer which is in contact with the source electrode layer or the drain electrode layer and the vicinity thereof, resistance is reduced. Then, a high-resistance source region or a high-resistance drain region is formed, while a region in the oxide semiconductor layer, which is close to the gate insulating film, can be made to be an i-type region.

Furthermore, the heat treatment may be performed at 100° C. to 200° C. for one hour to 30 hours in an air atmosphere. In this embodiment, the heat treatment is performed at 150° C. for 10 hours. This heat treatment may be performed at a fixed heating temperature. Alternatively, the following change in the heating temperature may be conducted plural times repeatedly: the heating temperature is increased from a room temperature to a temperature of 100° C. to 200° C. and then decreased to a room temperature. In addition, this heat treatment may be performed before formation of the oxide insulating film under a reduced pressure. Under the reduced pressure, the heat treatment time can be shortened. With such heat treatment, hydrogen is introduced from the oxide semiconductor layers to the oxide insulating layer; thus, normally-off thin film transistors can be obtained. Therefore, reliability of the semiconductor device can be improved.

A protective insulating layer may be additionally formed over the oxide insulating film **107**. For example, a silicon nitride film is formed by an RF sputtering method. Since an RF sputtering method has high productivity, it is preferably used as a film formation method of the protective insulating

layer. As the protective insulating layer, an inorganic insulating film which does not include impurities such as moisture, a hydrogen ion, and OH^- and blocks entry of these from the outside is used. Specifically, a silicon nitride film, an aluminum nitride film, a silicon nitride oxide film, an aluminum oxynitride film, or the like is used. In this embodiment, a silicon nitride film is formed as the protective insulating layer **106** (see FIG. **4**A).

Through the above steps, the transistor **180** in the driving circuit portion, the thin film transistor **170** in the pixel portion, and the capacitor **147** can be manufactured over one substrate. Each of the thin film transistors **170** and **180** is a bottom-gate thin film transistor including an oxide semiconductor layer in which a high-resistance source region, a high-resistance drain region, and a channel formation region are formed. Therefore, in each of the thin film transistors **170** and **180**, the high-resistance drain region or the high-resistance source region serves as a buffer and a high electric field is not applied locally even if a high electric field is applied, so that the withstand voltage of the transistor can be improved.

The capacitor **147** is formed using the gate insulating layer **102**, the capacitor wiring layer **108**, and the capacitor electrode layer **149**, in which the gate insulating layer **102** in the capacitor portion is used as a dielectric.

By providing the driving circuit and the pixel portion over the same substrate, connection wirings between the driving circuit and an external signal can be shortened; thus, reduction in size and cost of the light-emitting device can be achieved.

Then, the color filter layer **191** is formed over the protective insulating layer **106**. As the color filter layer, a green color filter layer, a blue color filter layer, a red color filter layer, or the like can be used, and a green color filter layer, a blue color filter, and a red color filter layer are sequentially formed. Each color filter layer is formed by a printing method, an ink-jet method, an etching method with the use of a photolithography technique, or the like. By providing the color filter layers, alignment of the color filter layers and light-emitting regions of light-emitting elements can be performed without depending on the attachment accuracy of the sealing substrate. In this embodiment, fifth, sixth, and seventh photolithography steps are performed to form a green color filter layer, a blue color filter layer, and a red color filter layer.

Next, an overcoat layer **192** which covers the color filter layers (the green color filter layer, the blue color filter layer, and the red color filter layer) is formed. The overcoat layer **192** is formed using a light-transmitting resin. In this embodiment, the overcoat layer **192** is formed in an eighth photolithography step.

Here, an example in which full color display is performed using three colors of RGB is shown; however, the invention is not particularly limited thereto, and full color display may be performed using four colors of RGBW.

Next, a protective insulating layer **109** which covers the overcoat layer **192** and the protective insulating layer **106** is formed (see FIG. **4**B). For the protective insulating layer **109**, an inorganic insulating film such as a silicon nitride film, an aluminum nitride film, a silicon nitride oxide film, or an aluminum oxynitride film is used. It is preferable that the protective insulating layer **109** be an insulating film having the same component as that of the protective insulating layer **106** because they can be etched in one step when contact holes are formed.

Next, a ninth photolithography step is performed. A resist mask is formed, and a contact hole **125** which reaches the drain electrode layer **105***b* is formed by etching the oxide insulating film **107**, the protective insulating layer **106**, and the protective insulating layer **109**. Then, the resist mask is removed (see FIG. **5**A). In addition, a contact hole **127** which reaches the second terminal **122** and a contact hole **126** which reaches the connection electrode **120** are also formed by this etching. Alternatively, a resist mask for forming the contact holes may be formed by an ink-jet method. A photomask is not used when the resist mask is formed by an ink-jet method, leading to reduction in manufacturing cost.

Next, a light-transmitting conductive film is formed. The light-transmitting conductive film is formed using a material such as indium oxide (In_2O_3) or an alloy of indium oxide and tin oxide (In_2O_3—SnO_2, abbreviated to ITO) by a sputtering method, a vacuum evaporation method, or the like. Alternatively, an Al—Zn—O-based non-single-crystal film containing nitrogen (i.e., an Al—Zn—O—N-based non-single-crystal film), a Zn—O-based non-single-crystal film containing nitrogen, or a Sn—Zn—O-based non-single-crystal film containing nitrogen may be used as the material of the light-transmitting conductive film. Note that the composition ratio (atomic %) of zinc in the Al—Zn—O—N-based non-single-crystal film is 47 atomic % or lower and is higher than that of aluminum in the non-single-crystal film; the composition ratio (atomic %) of aluminum in the Al—Zn—O—N-based non-single-crystal film is higher than that of nitrogen in the non-single-crystal film. Such a material is etched with a hydrochloric acid-based solution. However, since a residue is easily left on the substrate particularly in etching ITO, an alloy of indium oxide and zinc oxide (In_2O_3—ZnO) may be used in order to improve etching processability.

Note that the unit of the composition ratio in the light-transmitting conductive film is atomic percent (atomic %), and the composition ratio is evaluated by analysis using an electron probe X-ray microanalyzer (EPMA).

Next, a tenth photolithography step is performed. A resist mask is formed, and unnecessary portions of the light-transmitting conductive film are removed by etching, so that the first electrode layer **110**, the conductive layer **111**, and the terminal electrodes **128** and **129** are formed. Then, the resist mask is removed.

The capacitor **147**, which includes the gate insulating layer **102** as a dielectric, the capacitor wiring layer **108**, and the capacitor electrode layer **149**, can also be formed over the same substrate as the driving circuit portion and the pixel portion. In a light-emitting device, the capacitor electrode layer **149** is part of a power supply line, and the capacitor wiring layer **108** is part of a gate electrode layer of a driving TFT.

The terminal electrodes **128** and **129** which are formed in the terminal portion function as electrodes or wirings connected to an FPC. The terminal electrode **128** formed over the first terminal **121** with the connection electrode **120** interposed therebetween is a connection terminal electrode serving as an input terminal for the gate wiring. The terminal electrode **129** formed over the second terminal **122** is a connection terminal electrode serving as an input terminal for the source wiring.

Further, FIGS. **11**A**1** and **11**A**2** are a cross-sectional view of a gate wiring terminal portion at this stage and a top view thereof, respectively. FIG. **11**A**1** is a cross-sectional view taken along line C**1**-C**2** in FIG. **11**A**2**. In FIG. **11**A**1**, a conductive film **155** formed over the oxide insulating film **107** is a connection terminal electrode serving as an input terminal. Furthermore, in FIG. **11**A**1**, in the terminal portion,

a first terminal **151** formed using the same material as that of the gate wiring and a connection electrode **153** formed using the same material as that of the source wiring overlap with each other with the gate insulating layer **102** interposed therebetween, and are electrically connected to each other. In addition, the connection electrode **153** and the conductive film **155** are in direct contact with each other through a contact hole provided in the oxide insulating film **107** to form conduction therebetween.

Further, FIGS. **11**B**1** and **11**B**2** are a cross-sectional view of a source wiring terminal portion at this stage and a top view thereof, respectively. FIG. **11**B**1** corresponds to a cross-sectional view taken along line D**1**-D**2** in FIG. **11**B**2**. In FIG. **11**B**1**, the conductive film **155** formed over the oxide insulating film **107** is a connection terminal electrode serving as an input terminal. Furthermore, in FIG. **11**B**1**, in the terminal portion, an electrode **156** formed using the same material as that of the gate wiring is located below and overlapped with the second terminal **150**, which is electrically connected to the source wiring, with the gate insulating layer **102** interposed therebetween. The electrode **156** is not electrically connected to the second terminal **150**, and a capacitor for preventing noise or static electricity can be formed when the potential of the electrode **156** is set to a potential different from that of the second terminal **150**, such as floating, GND, or 0 V. The second terminal **150** is electrically connected to the conductive film **155** with the oxide insulating film **107** interposed therebetween.

A plurality of gate wirings, source wirings, and capacitor wirings are provided depending on the pixel density. In the terminal portion, the first terminal at the same potential as the gate wiring, the second terminal at the same potential as the source wiring, the third terminal at the same potential as the capacitor wiring, and the like are each arranged in plurality. The number of each of the terminals may be any number, and the number of the terminals may be determined by a practitioner as appropriate.

The thin film transistors and the storage capacitor are arranged in matrix in respective pixels so that a pixel portion is formed, which can be used as one of substrates for manufacturing an active matrix display device. In this specification, such a substrate is referred to as an active matrix substrate for convenience.

The conductive layer **111** is provided so as to overlap with the channel formation region **166** in the oxide semiconductor layer, whereby in a bias-temperature stress test (hereinafter, referred to as a BT test) for examining the reliability of a thin film transistor, the amount of change in threshold voltage of the thin film transistor **180** before and after the BT test can be reduced. A potential of the conductive layer **111** may be the same as or different from that of the gate electrode layer **161**. The conductive layer **111** can also serve as a second gate electrode layer. Alternatively, the potential of the conductive layer **111** may be GND or 0 V, or the conductive layer **111** may be in a floating state.

Next, a partition **193** is formed so as to cover the periphery portion of the first electrode layer **110**. The partition **193** is formed using a film of an organic resin such as polyimide, acrylic, polyamide, or epoxy, an inorganic insulating film, or a siloxane-based resin.

Note that the siloxane-based resin corresponds to a resin including a Si—O—Si bond formed using a siloxane-based material as a starting material. The siloxane-based resin may include, as a substituent, an organic group (e.g., an alkyl group or an aryl group) or a fluoro group. In addition, the organic group may include a fluoro group.

The partition **193** can be formed using phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), or the like. Note that the partition **193** may be formed by stacking a plurality of insulating films formed using any of these materials.

There is no particular limitation on the method for forming the partition **193**. The partition **193** can be formed, depending on the material, with a method such as a sputtering method, an SOG method, a spin coating method, a dipping method, a spray coating method, or a droplet discharge method (e.g., an ink-jet method, screen printing, or offset printing), or with a means such as a doctor knife, a roll coater, a curtain coater, or a knife coater. Further, other insulating layers used in the light-emitting device may be formed using the materials and the methods which are shown as examples of the materials and the methods of the partition **193**.

It is particularly preferable that the partition **193** be formed using a photosensitive resin material to have an opening portion over the first electrode layer **110** so that a sidewall of the opening portion is formed as a tilted surface with continuous curvature. When the partition **193** is formed using a photosensitive resin material, a step for forming a resist mask can be omitted. In this embodiment, an eleventh photolithography steps is performed, so that the partition **193** is formed.

The EL layer **194** is formed over the first electrode layer **110** and the second electrode layer **195** is formed over the EL layer **194**, whereby a light-emitting element is formed. Note that the second electrode layer **195** is electrically connected to a common potential line. Any of a variety of materials can be used for the second electrode layer **195**. Specifically, the second electrode layer **195** is preferably formed using a material having a low work function, for example, an alkali metal such as Li or Cs; an alkaline earth metal such as Mg, Ca, or Sr; an alloy containing any of these metals (e.g., Mg:Ag or Al:Li); or a rare earth metal such as Yb or Er. In this embodiment, an aluminum film is used as the second electrode layer **195**.

Through these eleven photolithography steps with the use of the eleven photomasks, the light-emitting device of this embodiment shown in FIG. **1** can be manufactured, which includes the driving circuit portion having the thin film transistor **180**, the pixel portion having the thin film transistor **170** and the light-emitting element, the capacitor **147** having the storage capacitor, and an external extraction terminal portion.

Further, in this embodiment, an example where the contact holes in the oxide insulating film **107**, the protective insulating layer **106**, and the protective insulating layer **109** are formed in one photolithography step is described; however, contact holes may be formed in a plurality of photolithography steps with different photomasks. For example, the fifth photolithography step may be performed to form contact holes in the oxide insulating film **107** and the protective insulating layer **106** serving as interlayer insulating layers, the sixth to ninth photolithography steps may be performed to form the RGB color filter layers and the overcoat layer, and then contact holes may be formed in the protective insulating layer **109** in the tenth photolithography step. In this case, the number of photolithography steps and photomasks increases by one; accordingly, the light-emitting device is formed through the twelve photolithography steps with twelve photomasks.

Note that in the above-described photolithography steps, an etching step may be performed with the use of a mask layer formed using a multi-tone mask which is a light-

exposure mask through which light is transmitted so as to have a plurality of intensities.

Since a mask layer formed with the use of a multi-tone mask has a plurality of film thicknesses and can be changed shapes thereof by performing etching on the mask layer, the mask layer can be used in a plurality of etching steps for processing into different patterns. Therefore, a mask layer corresponding at least two kinds or more of different patterns can be formed by one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography steps can also be reduced, whereby simplification of a process can be realized.

Further, when a light-emitting device is manufactured, a power supply line electrically connected to the source electrode layer of the driving TFT is provided. The power supply line intersects with a gate wiring and a source wiring and is formed using the same material and in the same step as the gate electrode layer.

Furthermore, in the case where a light-emitting device is manufactured, one electrode of the light-emitting element is electrically connected to the drain electrode layer of the driving TFT, and a common potential line which is electrically connected to the other electrode of the light-emitting element is provided. Note that the common potential line can be formed using the same material and in the same step as the gate electrode layer.

Moreover, in the case where a light-emitting device is manufactured, a plurality of thin film transistors are provided in one pixel, and a connection portion which connects the gate electrode layer of one thin film transistor to the drain electrode layer of the other thin film transistor is provided.

The use of an oxide semiconductor for a thin film transistor leads to reduction in manufacturing cost. In particular, an oxide insulating film is formed in contact with an oxide semiconductor layer by the above method, whereby a thin film transistor having stable electric characteristics can be manufactured and provided. Therefore, a light-emitting device which includes highly reliable thin film transistors having favorable electric characteristics can be provided.

The channel formation region in the semiconductor layer is a high-resistance region; thus, electric characteristics of the thin film transistor are stabilized and increase in off current or the like can be prevented. Therefore, a light-emitting device including a highly reliable thin film transistor having favorable electric characteristics can be provided.

Since a thin film transistor is easily broken due to static electricity or the like, a protective circuit is preferably provided over the same substrate as the pixel portion or the driving circuit. The protective circuit is preferably formed with a non-linear element including an oxide semiconductor layer. For example, protective circuits are provided between the pixel portion and a scan line input terminal and between the pixel portion and a signal line input terminal. In this embodiment, a plurality of protective circuits are provided so that the pixel transistor and the like are not broken when surge voltage due to static electricity or the like is applied to a scan line, a signal line, and a capacitor bus line. Therefore, the protective circuit is formed so as to release charge to a common wiring when surge voltage is applied to the protective circuit. Further, the protective circuit includes non-linear elements arranged in parallel to the scan line. The non-linear element includes a two-terminal element such as a diode or a three-terminal element such as a transistor. For example, the non-linear element can also be formed through the same step as the thin film transistor **170** in the pixel portion, and can be made to have the same properties as a diode by connecting a gate terminal to a drain terminal of the non-linear element.

This embodiment can be implemented in appropriate combination with the structures described in the other embodiments.

Embodiment 2

In this embodiment, an example in which oxide conductive layers are provided as a source region and a drain region between the oxide semiconductor layer and the source and drain electrode layers in Embodiment 1 will be described with reference to FIGS. **6**A to **6**D and FIGS. **7**A and **7**B. Therefore, part of this embodiment can be performed in a manner similar to that of Embodiment 1; thus, repetitive description of the same portions as or portions having functions similar to those in Embodiment 1 and steps for forming such portions will be omitted. Since FIGS. **6**A to **6**D and FIGS. **7**A and **7**B are the same as FIG. **1**, FIGS. **2**A to **2**C, FIGS. **3**A to **3**C, FIGS. **4**A and **4**B, and FIGS. **5**A and **5**B except for part of steps, the same portions are denoted by the same reference numerals and detailed description of the same portions is omitted.

First, the steps up to and including the step in FIG. **3**B in Embodiment 1 are performed in accordance with Embodiment 1. FIG. **6**A shows the same step as FIG. **3**B.

An oxide conductive film **140** is formed over the dehydrated or dehydrogenated oxide semiconductor layers **133** and **134**, and a metal conductive film formed using a metal conductive material is stacked over the oxide conductive film **140**.

As a film formation method of the oxide conductive film **140**, a sputtering method, a vacuum evaporation method (e.g., an electron beam evaporation method), an arc discharge ion plating method, or a spray method is used. A material of the oxide conductive film **140** preferably contains zinc oxide as a component and preferably does not contain indium oxide. For such an oxide conductive film **140**, zinc oxide, aluminum zinc oxide, aluminum zinc oxynitride, gallium zinc oxide, or the like can be used. The thickness of the oxide conductive film is selected as appropriate in the range of 50 nm to 300 nm. In addition, in the case where a sputtering method is used, it is preferable that film formation be performed using a target containing SiO_2 at 2 wt % or more to 10 wt % or less, and SiO_x (x>0), which inhibits crystallization, be contained in the oxide conductive film so that crystallization is suppressed when the heat treatment for dehydration or dehydrogenation is performed in a later step.

Next, a fourth photolithography step is performed. The resist masks **136***a*, **136***b*, **136***c*, **136***d*, **136***e*, **136***f*, and **136***g* are formed. Then, unnecessary portions of the metal conductive film are removed by etching, whereby the source electrode layer **105***a*, the drain electrode layer **105***b*, the source electrode layer **165***a*, the drain electrode layer **165***b*, the capacitor electrode layer **149**, the connection electrode **120**, and the second terminal **122** are formed (see FIG. **6**B).

Note that each material and etching conditions are adjusted as appropriate so that the oxide conductive film **140** and the oxide semiconductor layers **133** and **134** are not removed in etching of the metal conductive film.

Next, the resist masks **136***a*, **136***b*, **136***c*, **136***d*, **136***e*, **136***f*, and **136***g* are removed. The oxide conductive film **140** is etched using the source electrode layer **105***a*, the drain electrode layer **105***b*, the source electrode layer **165***a*, and the drain electrode layer **165***b* as masks, so that oxide

conductive layers **164***a* and **164***b*, oxide conductive layers **104***a* and **104***b*, and a capacitor electrode layer **185** are formed (see FIG. **6**C). The oxide conductive film **140** containing zinc oxide as a component can be easily etched with an alkaline solution such as a resist stripping solution, for example. In addition, oxide conductive layers **138** and **139** are also formed in respective terminal portions in this step.

Etching treatment for dividing the oxide conductive layer to form channel formation regions is performed by utilizing the difference in etching rates between the oxide semiconductor layers and the oxide conductive layer. The oxide conductive layer over the oxide semiconductor layers is selectively etched utilizing a higher etching rate of the oxide conductive film as compared to that of the oxide semiconductor layers.

Therefore, removal of the resist masks **136***a*, **136***b*, **136***c*, **136***d*, **136***e*, **136***f*, and **136***g* is preferably performed by an ashing process. In the case of etching with a stripping solution, etching conditions (the kind of the etchant, the concentration, and the etching time) are adjusted as appropriate so that the oxide conductive film **140** and the oxide semiconductor layers **133** and **134** are not etched excessively.

As described in this embodiment, after forming the island-shaped oxide semiconductor layers by etching, the oxide conductive film and the metal conductive film are stacked thereover, and etching is performed using the same masks to form a wiring pattern including source electrode layers and drain electrode layers, oxide conductive films can be left under the wiring pattern of the metal conductive film.

At the contact portion between the gate wiring (the conductive layer **162**) and the source wiring (the drain electrode layer **165***b*), the oxide conductive layer **164***b* is formed below the source wiring. The oxide conductive layer **164***b* serves as a buffer, the resistance is only the series resistance depending on the thickness of the oxide conductive layer, and further the oxide conductive layer **164***b* does not form an insulating oxide with metal, which is preferable.

Next, the oxide insulating film **107** serving as a protective insulating film is formed in contact with the oxide semiconductor layer **133** and **134**. In this embodiment, a silicon oxide film with a thickness of 300 nm is formed as the oxide insulating film **107** by a sputtering method.

Next, second heat treatment is performed in an inert gas atmosphere or a nitrogen atmosphere at a preferable temperature from 200° C. to 400° C., e.g., from 250° C. to 350° C. For example, the second heat treatment is performed in a nitrogen atmosphere at 250° C. for one hour. By the second heat treatment, part of the oxide semiconductor layers **133** and **134** which overlaps with the oxide insulating film **107** is heated in the state of being in contact with the oxide insulating film **107**.

Through the above steps, heat treatment for dehydration or dehydrogenation is performed on the oxide semiconductor layer after film formation to reduce the resistance, and then, part of the oxide semiconductor layer is selectively made to be in an oxygen-excess state.

As a result, in the oxide semiconductor layer **133**, a channel formation region **166** overlapping with the gate electrode layer **161** becomes an i-type channel formation region, and a high-resistance source region **167***a* overlapping with the source electrode layer **165***a* and the oxide conductive layer **164***a*, and a high-resistance drain region **167***b* overlapping with the drain electrode layer **165***b* and the oxide conductive layer **164***b* are formed in a self-aligned manner; thus, an oxide semiconductor layer **163** is formed. Similarly, in the oxide semiconductor layer **134**, a channel formation region **116** overlapping with the gate electrode layer **101** becomes an i-type channel formation region, and a high-resistance source region **117***a* overlapping with the source electrode layer **105***a* and the oxide conductive layer **104***a*, and a high-resistance drain region **117***b* overlapping with the drain electrode layer **105***b* and the oxide conductive layer **164***b* are formed in a self-aligned manner; thus, an oxide semiconductor layer **103** is formed.

The oxide conductive layers **104***b* and **164***b* which are provided between the oxide semiconductor layers **103** and **163** and the drain electrode layers **105***b* and **165***b* formed using a metal material, each also function as a low-resistance drain (LRD, also referred to as an LRN (low-resistance n-type conductivity)) region. Similarly, the oxide conductive layers **104***a* and **164***a* which are provided between the oxide semiconductor layers **103** and **163** and the source electrode layers **105***a* and **165***a* formed using a metal material, each also function as a low-resistance source (LRS, also referred to as an LRN (low-resistance n-type conductivity)) region. With the structure including the oxide semiconductor layer, the low-resistance drain region, and the drain electrode layer formed using a metal material, withstand voltage of the transistor can be further increased. Specifically, the carrier concentration of the low-resistance drain region is higher than that of the high-resistance drain region (the HRD region) and preferably in a range of $1\times10^{20}/cm^3$ or higher and $1\times10^{21}/cm^3$ or lower.

Through the above steps, a thin film transistor **171** in the pixel portion and a transistor **181** in the driving circuit portion can be manufactured over the same substrate. Each of the thin film transistors **171** and **181** is a bottom-gate thin film transistor including an oxide semiconductor layer in which a high-resistance source region, a high-resistance drain region, and a channel formation region are formed. Therefore, in each of the thin film transistors **172** and **181**, the high-resistance drain region or the high-resistance source region serves as a buffer and a high electric field is not applied locally even if a high electric field is applied, so that the withstand voltage of the transistor can be improved.

In the capacitor portion, a capacitor **146** is formed from a stack of the capacitor wiring layer **108**, the gate insulating layer **102**, the capacitor electrode layer **185** formed in the same step as the oxide conductive layer **104***b*, and the capacitor electrode layer **149** formed in the same step as the drain electrode layer **105***b*.

Next, the protective insulating layer **106** is formed over the oxide insulating film **107** and the color filter layer **191** is formed over the protective insulating layer **106** in the pixel portion. The overcoat layer **192** is formed so as to cover the color filter layer **191** and the protective insulating layer **109** is formed so as to cover the protective insulating layer **106** and the overcoat layer **192**.

Next, a ninth photolithography step is performed in a manner similar to that performed in Embodiment 1. A resist mask is formed, and the contact hole **125** which reaches the drain electrode layer **105***b* is formed by etching the oxide insulating film **107**, the protective insulating layer **106**, and the protective insulating layer **109**. Then, the resist mask is removed (see FIG. **6**D). In addition, the contact hole **127** which reaches the second terminal **122** and the contact hole **126** which reaches the connection electrode **120** are also formed by this etching.

Next, a light-transmitting conductive film is formed, and a tenth photolithography step is performed. A resist mask is formed and unnecessary portions of the light-transmitting conductive film are removed by etching to form the first

electrode layer **110**, the conductive layer **111**, and the terminal electrodes **128** and **129**. Then, the resist masks are removed (see FIG. **7**A).

As in Embodiment 1, the partition **193** is formed in an eleventh photolithography step. The EL layer **194** and the second electrode layer **195** are stacked over the first electrode layer **110**, so that the light-emitting device of this embodiment which includes a light-emitting element is manufactured (see FIG. **7**B).

When the oxide conductive layers are provided between the oxide semiconductor layer and the source and drain electrode layers as the source region and the drain region, the source region and the drain region can have lower resistance and the transistor can operate at high speed. It is effective to use the oxide conductive layers for a source region and a drain region in order to improve frequency characteristics of a peripheral circuit (a driving circuit). This is because the contact between a metal electrode (e.g., Ti) and an oxide conductive layer can reduce the contact resistance as compared to the contact between a metal electrode (e.g., Ti) and an oxide semiconductor layer.

There has been a problem in that molybdenum (Mo) which is used as a part of a wiring material (e.g., Mo/Al/Mo) in a light-emitting device has high contact resistance with an oxide semiconductor layer. This is because Mo is less likely to be oxidized and has a weaker effect of extracting oxygen from the oxide semiconductor layer as compared to titanium (Ti), and a contact interface between Mo and the oxide semiconductor layer is not changed to have n-type conductivity. However, even in such a case, the contact resistance can be reduced by interposing an oxide conductive layer between the oxide semiconductor layer and source and drain electrode layers; accordingly, frequency characteristics of a peripheral circuit (a driving circuit) can be improved.

The channel length of the thin film transistor is determined at the time of etching the oxide conductive layer; accordingly, the channel length can be further shortened. For example, the channel length L can be set as small as 0.1 μm to 2 μm; in this way, operation speed can be increased.

Embodiment 3

In this embodiment, another example in which oxide conductive layers are provided as a source region and a drain region between the oxide semiconductor layer and the source and drain electrode layers in Embodiment 1 or 2 will be described with reference to FIGS. **8**A to **8**D and FIGS. **9**A and **9**B. Therefore, part of this embodiment can be performed in a manner similar to that of Embodiment 1 or 2; thus, repetitive description of the same portions as or portions having functions similar to those in Embodiment 1 or 2 and steps for forming such portions will be omitted. Since FIGS. **8**A to **8**D and FIGS. **9**A and **9**B are the same as FIG. **1**, FIGS. **2**A to **2**C, FIGS. **3**A to **3**C, FIGS. **4**A and **4**B, FIGS. **5**A and **5**B, FIGS. **6**A to **6**D, and FIGS. **7**A and **7**B except for part of steps, the same portions are denoted by the same reference numerals and detailed description of the same portions is omitted.

First, in accordance with Embodiment 1, a metal conductive film is formed over the substrate **100**, and the metal conductive film is etched using a resist mask formed in a first photolithography step, so that the first terminal **121**, the gate electrode layer **161**, the conductive layer **162**, the gate electrode layer **101**, and the capacitor wiring layer **108** are formed.

Next, the gate insulating layer **102** is formed over the first terminal **121**, the gate electrode layer **161**, the conductive layer **162**, the gate electrode layer **101**, and the capacitor wiring layer **108**, and then an oxide semiconductor film and an oxide conductive film are stacked. The gate insulating layer, the oxide semiconductor film, and the oxide conductive film can be formed in succession without being exposed to air.

Resist masks are formed over the oxide conductive film in a second photolithography step. The gate insulating layer, the oxide semiconductor film, and the oxide conductive film are etched using the resist masks to form the contact hole **119** which reaches the first terminal **121** and the contact hole **123** which reaches the conductive layer **162**.

The resist masks formed in the second photolithography step are removed, and resist masks are newly formed over the oxide conductive film in a third photolithography step. With the use of the resist masks in the third photolithography step, island-shaped oxide semiconductor layers and island-shaped oxide conductive layers are formed.

When the contact holes are formed in the gate insulating layer in the state where the oxide semiconductor film and the oxide conductive film are stacked over the entire surface of the gate insulating layer in such a manner, the resist masks are not directly in contact with the surface of the gate insulating layer; accordingly, contamination of the surface of the gate insulating layer (e.g., attachment of impurities or the like to the gate insulating layer) can be prevented. Thus, a favorable state of the interfaces between the gate insulating layer and the oxide semiconductor film and between the gate insulating layer and the oxide conductive film can be obtained, whereby reliability can be improved.

Next, heat treatment for dehydration or dehydrogenation is performed in the state where the oxide semiconductor layers and the oxide conductive layers are stacked. By the heat treatment at 400° C. to 700° C., the dehydration or dehydrogenation of the oxide semiconductor layers can be achieved; thus, water (H_2O) can be prevented from being contained again in the oxide semiconductor layers in later steps.

As long as a substance which inhibits crystallization such as silicon oxide is not contained in the oxide conductive layers, the oxide conductive layers are crystallized through this heat treatment. Crystal of the oxide conductive layers grows in a columnar shape with respect to a base surface. Accordingly, when the metal conductive film formed over the oxide conductive layers is etched in order to form a source electrode layer and a drain electrode layer, formation of an undercut can be prevented.

Further, by the heat treatment for dehydration or dehydrogenation of the oxide semiconductor layers, conductivity of the oxide conductive layers can be improved. Note that only the oxide conductive layers may be subjected to heat treatment at a temperature lower than that for the oxide semiconductor layers.

In addition, in the case where the separation layer is formed and then the thin film transistor and the light-emitting element are formed over the manufacturing substrate, the heat treatment for dehydration or dehydrogenation allows separation at an interface of the separation layer to be easily performed from the manufacturing substrate to a supporting substrate in a later process.

The first heat treatment of the oxide semiconductor layers and the oxide conductive layers can also be performed on the oxide semiconductor film and the oxide conductive film which have not been processed into island-shaped oxide semiconductor layers and the island-shaped oxide conductive layers. In that case, after the first heat treatment, the

substrate is taken out of the heating device, and then a photolithography step is performed.

Through the above steps, the oxide semiconductor layers **133** and **134** and oxide conductive layers **142** and **143** can be obtained (see FIG. **8**A). The oxide semiconductor layer **133** and the oxide conductive layer **142** are island-shaped stacked-layers formed using the same mask, and the oxide semiconductor layer **134** and the oxide conductive layer **143** are island-shaped stacked-layers formed using the same mask.

Next, a fourth photolithography step is performed. The resist masks **136***a*, **136***b*, **136***c*, **136***d*, **136***e*, **136***f*, and **136***g* are formed, and unnecessary portions of the metal conductive film are removed by etching, so that the source electrode layer **105***a*, the drain electrode layer **105***b*, the source electrode layer **165***a*, the drain electrode layer **165***b*, the capacitor electrode layer **149**, the connection electrode **120**, and the second terminal **122** are formed (see FIG. **8**B).

Note that each material and etching conditions are adjusted as appropriate so that the oxide conductive layers **142** and **143** and the oxide semiconductor layers **133** and **134** are not removed in etching of the metal conductive film.

Next, the resist masks **136***a*, **136***b*, **136***c*, **136***d*, **136***e*, **136***f*, and **136***g* are removed. Then the oxide conductive layers **142** and **143** are etched using the source electrode layer **105***a*, the drain electrode layer **105***b*, the source electrode layer **165***a*, and the drain electrode layer **165***b* as masks, so that the oxide conductive layers **164***a* and **164***b* and the oxide conductive layers **104***a* and **104***b* are formed (see FIG. **8**C). The oxide conductive layers **142** and **143** containing zinc oxide as a component can be easily etched with an alkaline solution such as a resist stripping solution, for example.

Therefore, removal of the resist masks **136***a*, **136***b*, **136***c*, **136***d*, **136***e*, **136***f*, and **136***g* is preferably performed by an ashing process. In the case of etching with a stripping solution, etching conditions (the kind of the etchant, the concentration, and the etching time) are adjusted as appropriate so that the oxide conductive layers **142** and **143** and the oxide semiconductor layers **133** and **134** are not etched excessively.

Next, the oxide insulating film **107** serving as a protective insulating film is formed in contact with the oxide semiconductor layer **133** and **134**. In this embodiment, a silicon oxide film with a thickness of 300 nm is formed as the oxide insulating film **107** by a sputtering method.

Next, second heat treatment is performed in an inert gas atmosphere or a nitrogen atmosphere at a preferable temperature from 200° C. to 400° C., e.g., from 250° C. to 350° C. For example, the second heat treatment is performed in a nitrogen atmosphere at 250° C. for one hour. By the second heat treatment, part of the oxide semiconductor layers **133** and **134** which overlaps with the oxide insulating film **107** is heated in the state of being in contact with the oxide insulating film **107**.

Through the above steps, heat treatment for dehydration or dehydrogenation is performed on the oxide semiconductor layer after film formation to reduce the resistance. Then, part of the oxide semiconductor layer is selectively made to be in an oxygen-excess state.

As a result, in the oxide semiconductor layer **133**, a channel formation region **166** overlapping with the gate electrode layer **161** becomes an i-type channel formation region, and a high-resistance source region **167***a* overlapping with the source electrode layer **165***a* and the oxide conductive layer **164***a*, and a high-resistance drain region **167***b* overlapping with the drain electrode layer **165***b* and the oxide conductive layer **164***b* are formed in a self-aligned manner; thus, an oxide semiconductor layer **163** is formed. Similarly, in the oxide semiconductor layer **134**, a channel formation region **116** overlapping with the gate electrode layer **101** becomes an i-type channel formation region, and a high-resistance source region **117***a* overlapping with the source electrode layer **105***a* and the oxide conductive layer **104***a*, and a high-resistance drain region **117***b* overlapping with the drain electrode layer **105***b* and the oxide conductive layer **164***b* are formed in a self-aligned manner; thus, an oxide semiconductor layer **103** is formed.

The oxide conductive layers **104***b* and **164***b* which are provided between the oxide semiconductor layers **103** and **163** and the drain electrode layers **105***b* and **165***b* formed using a metal material, each also function as a low-resistance drain (LRD, also referred to as an LRN) region. Similarly, the oxide conductive layers **104***a* and **164***a* which are provided between the oxide semiconductor layers **103** and **163** and the source electrode layers **105***a* and **165***a* formed using a metal material, each also function as a low-resistance source (LRS, also referred to as an LRN) region. With the structure including the oxide semiconductor layer, the low-resistance drain region, and the drain electrode layer formed using a metal material, withstand voltage of the transistor can be further increased. Specifically, the carrier concentration of the low-resistance drain region is higher than that of the high-resistance drain region (the HRD region) and preferably in a range of $1\times10^{20}/cm^3$ to $1\times10^{21}/cm^3$.

Through the above steps, a thin film transistor **172** in the pixel portion and a transistor **182** in the driving circuit portion can be manufactured over the same substrate. Each of the thin film transistors **172** and **181** is a bottom-gate thin film transistor including an oxide semiconductor layer in which a high-resistance source region, a high-resistance drain region, and a channel formation region are formed. Therefore, in each of the thin film transistors **172** and **181**, the high-resistance drain region or the high-resistance source region serves as a buffer and a high electric field is not applied locally even if a high electric field is applied, so that the withstand voltage of the transistor can be improved.

Further, in the capacitor portion, the capacitor **147** is formed from a stack of the capacitor wiring layer **108**, the gate insulating layer **102**, and the capacitor electrode layer **149** formed in the same step as the drain electrode layer **105***b*.

Next, the protective insulating layer **106** is formed over the oxide insulating film **107**. In the pixel portion, the color filter layer **191** is formed over the protective insulating layer **106**. The overcoat layer **192** is formed so as to cover the color filter layer **191**. Then, the protective insulating layer **109** is formed so as to cover the protective insulating layer **106** and the overcoat layer **192**.

Next, a ninth photolithography step is performed in a manner similar to that performed in Embodiment 1. A resist mask is formed, and the contact hole **125** which reaches the drain electrode layer **105***b* is formed by etching the oxide insulating film **107**, the protective insulating layer **106**, and the protective insulating layer **109**. Then, the resist mask is removed (see FIG. **8**D). In addition, the contact hole **127** which reaches the second terminal **122** and the contact hole **126** which reaches the connection electrode **120** are also formed by this etching.

Next, a light-transmitting conductive film is formed, and a tenth photolithography step is performed. A resist mask is formed and unnecessary portions of the light-transmitting conductive film are removed by etching to form the first

electrode layer **110**, the conductive layer **111**, and the terminal electrodes **128** and **129**. Then, the resist masks are removed (see FIG. **9**A).

As in Embodiment 1, the partition **193** is formed in an eleventh photolithography step. The EL layer **194** and the second electrode layer **195** are stacked over the first electrode layer **110**, so that the light-emitting device of this embodiment which includes a light-emitting element is manufactured (see FIG. **9**B).

When the oxide conductive layers are provided between the oxide semiconductor layer and the source and drain electrode layers as the source region and the drain region, the source region and the drain region can have lower resistance and the transistor can operate at high speed. It is effective to use the oxide conductive layers for a source region and a drain region in order to improve frequency characteristics of a peripheral circuit (a driving circuit). This is because the contact resistance between a metal electrode (e.g., Ti) and an oxide conductive layer is lower than the contact resistance between a metal electrode (e.g., Ti) and an oxide semiconductor layer.

The contact resistance can be reduced by interposing the oxide conductive layers between the oxide semiconductor layer and the source and drain electrode layers; accordingly, frequency characteristics of a peripheral circuit (a driving circuit) can be improved.

The channel length of the thin film transistor is determined at the time of etching the oxide conductive layer; accordingly, the channel length can be further shortened. For example, the channel length L can be set as small as 0.1 μm to 2 μm; in this way, operation speed can be increased.

Embodiment 4

In this embodiment, an example of a light-emitting device in Embodiment 1, in which a thin film transistor in a pixel portion and a first electrode layer of a light-emitting element are electrically connected to each other through a connection electrode layer will be described with reference to FIG. **16**, FIGS. **17**A to **17**D, and FIGS. **18**A and **18**B. Therefore, part of this embodiment can be performed in a manner similar to that of Embodiment 1; thus, repetitive description of the same portions as or portions having functions similar to those in Embodiment 1 and steps for forming such portions will be omitted. Since FIG. **16**, FIGS. **17**A to **17**D, and FIGS. **18**A and **18**B are the same as FIG. **1**, FIGS. **2**A to **2**C, FIGS. **3**A to **3**C, FIGS. **4**A and **4**B, and FIGS. **5**A and **5**B except for part of steps, the same portions are denoted by the same reference numerals and detailed description of the same portions is omitted

FIG. **16** shows a light-emitting device of this embodiment. The drain electrode layer **105***b* of the thin film transistor **170** in the pixel portion is electrically connected to the first electrode layer **110** through a connection electrode layer **196**. A method for manufacturing the light-emitting device illustrated in FIG. **16** will be described with reference to FIGS. **17**A to **17**D and FIGS. **18**A and **18**B.

First, according to Embodiment 1, the steps up to and including the step in FIG. **4**A in Embodiment 1 are performed. FIG. **17**A illustrates the same step as FIG. **4**A.

Next, a fifth photolithography step is performed. A resist mask is formed, and the contact hole **125** which reaches the drain electrode layer **105***b*, the contact hole **127** which reaches the second terminal **122**, and the contact hole **126** which reaches the connection electrode **120** are formed by etching the oxide insulating film **107** and the protective insulating layer **106**. Then, the resist mask is removed (see FIG. **17**B).

Next, a conductive film is formed, and a sixth photolithography step is performed. A resist mask is formed and unnecessary portions of the conductive film are removed by etching to form the connection electrode layer **196**, a conductive layer **112**, and terminal electrodes **113** and **114**. Then, the resist masks are removed (see FIG. **17**C). As the conductive film, a metal conductive film can be used; therefore, the connection electrode layer **196**, the conductive layer **112**, and the terminal electrodes **113** and **114** can be formed of a metal conductive layer.

As the connection electrode layer **196**, a film including an element selected from Al, Cr, Cu, Ta, Ti, Mo, and W as its main component or a stacked film including a film of any of the elements and an alloy film thereof can be used. Accordingly, in the case where the conductive layer **112** and the terminal electrodes **113** and **114** are formed in the same step as the connection electrode layer **196** as in this embodiment, the conductive layer **112** and the terminal electrodes **113** and **114** can also be formed using a film including an element selected from Al, Cr, Cu, Ta, Ti, Mo, and W as its main component or a stacked film including a film of any of the elements and an alloy film thereof. The conductive film is not limited to a single-layer including the above element and can be formed in a stacked-layer of two or more layers. As a film formation method of the conductive film, a sputtering method, a vacuum evaporation method (e.g., an electron beam evaporation method), an arc discharge ion plating method, or a spray method can be used.

Next, the color filter layer **191** is formed over the protective insulating layer **106** in the pixel portion in seventh to ninth photolithography steps and the overcoat layer **192** is formed so as to cover the color filter layer **191** in a tenth photolithography step. The protective insulating layer **109** is formed so as to cover the connection electrode layer **196**, the conductive layer **112**, the terminal electrodes **113** and **114**, the protective insulating layer **106**, and the overcoat layer **192** (see FIG. **17**D).

Next, an eleventh photolithography step is performed. A resist mask is formed, and the contact hole **125** which reaches the connection electrode layer **196** is formed by etching the protective insulating layer **109**. Then, the resist mask is removed. In addition, the protective insulating layer **109** over the terminal electrodes **113** and **114** is also removed by this etching, so that the terminal electrodes **113** and **114** are exposed (see FIG. **18**A).

Then, a light-transmitting conductive film is formed. A twelfth photolithography step is performed. A resist mask is formed and unnecessary portions of the light-transmitting conductive film are etched to form the first electrode layer **110**. Then, the resist mask is removed.

As in Embodiment 1, the partition **193** is formed in a thirteenth photolithography step. The EL layer **194** and the second electrode layer **195** are stacked over the first electrode layer **110**; thus, the light-emitting device of this embodiment, which includes a light-emitting element, is manufactured (see FIG. **18**B).

In the case where the connection electrode layer **196** is formed, a power supply line can be formed using the same material as and in the same step as the connection electrode layer **196**. Further, a common potential line can also be formed using the same material as and in the same step as the connection electrode layer **196**.

This embodiment can be implemented in appropriate combination with any of the structures described in Embodiments 1 to 3.

Embodiment 5

In this embodiment, FIG. **10** shows an example of a thin film transistor whose manufacturing process is partly different from that of Embodiment 1. FIG. **10** is the same as FIG. **1**, FIGS. **2**A to **2**C, FIGS. **3**A to **3**C, FIGS. **4**A and **4**B, and FIGS. **5**A and **5**B except for part of the steps. Thus, the same parts as in FIG. **1**, FIGS. **2**A to **2**C, FIGS. **3**A to **3**C, FIGS. **4**A and **4**B, and FIGS. **5**A and **5**B are denoted by the same reference numerals and detailed description on the parts is omitted.

First, according to Embodiment 1, the gate electrode layer and the gate insulating layer are formed over a substrate. Then, in the pixel portion, a contact hole which reaches the gate electrode layer is formed in a second photolithography step (not shown).

Next, the oxide semiconductor film **130** is formed and then processed into the island-shaped oxide semiconductor layers **131** and **132** in a third photolithography step.

Next, the oxide semiconductor layers **131** and **132** are dehydrated or dehydrogenated. The temperature of first heat treatment at which dehydration or dehydrogenation is performed is 400° C. to 750° C., preferably 425° C. or higher. Note that in the case where the temperature of the first heat treatment is 425° C. or higher, the heat treatment time may be one hour or less, while in the case where the temperature of the first heat treatment is lower than 425° C., the heat treatment time is set to more than one hour. Here, the substrate is introduced into an electric furnace which is one example of heat treatment apparatuses, and the oxide semiconductor layers are subjected to heat treatment in a nitrogen atmosphere. Then, the oxide semiconductor layers are not exposed to air so as to prevent water and hydrogen from entering the oxide semiconductor layers again. In this manner, oxide semiconductor layers are obtained. Then, a high-purity oxygen gas, a high-purity N_2O gas, or ultra-dry air (having a dew point of −40° C. or lower, preferably −60° C. or lower) is introduced to the same furnace and cooling is performed. It is preferable that water, hydrogen, or the like be not contained in the oxygen gas or the N_2O gas. Alternatively, it is preferable that the oxygen gas or the N_2O gas, which is introduced into an apparatus for heat treatment, have purity of 6N (99.9999%) or more, preferably 7N (99.99999%) or more; that is, an impurity concentration in the oxygen gas or the N_2O gas is preferably 1 ppm or lower, further preferably 0.1 ppm or lower.

Note that the heat treatment apparatus is not limited to the electric furnace, and, for example, an RTA (rapid thermal annealing) apparatus such as a GRTA (gas rapid thermal annealing) apparatus or an LRTA (lamp rapid thermal annealing) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp. In addition, the LRTA apparatus may be provided with not only a lamp but also a device which heats an object to be processed by heat conduction or heat radiation from a heater such as a resistance heater. GRTA is a method of heat treatment using a high-temperature gas. As the gas, an inert gas which does not react with an object to be processed by heat treatment, for example, nitrogen or a rare gas such as argon, is used. The heat treatment may be performed by an RTA method at 600° C. to 750° C. for several minutes.

Further, after the first heat treatment for dehydration or dehydrogenation, heat treatment may be performed at 200° C. to 400° C., preferably 200° C. to 300° C., in an oxygen gas atmosphere or an N_2O gas atmosphere.

Furthermore, the first heat treatment of the oxide semiconductor layers **131** and **132** can also be performed on the oxide semiconductor film **130** which has not been processed into the island-shaped oxide semiconductor layers. In that case, after the first heat treatment, the substrate is taken out of the heating device and a photolithography step is performed.

Through the above process, the entire region of the oxide semiconductor film is made in an oxygen-excess state, thereby having higher resistance; accordingly, oxide semiconductor layers **168** and **118** which are entirely intrinsic are obtained.

Next, a fourth photolithography step is performed. Resist masks are formed over the oxide semiconductor layers **168** and **118** and a source electrode layer and a drain electrode layer are formed by a selective etching. An oxide insulating film **107** is formed by a sputtering method.

Next, in order to reduce variation in electric characteristics of the thin film transistors, heat treatment (preferably 150° C. to lower than 350° C.) may be performed in an inert gas atmosphere or a nitrogen gas atmosphere. For example, heat treatment may be performed under a nitrogen atmosphere at 250° C. for an hour.

Next, the protective insulating layer **106** is formed over the oxide insulating film **107**. In the pixel portion, the color filter layer **191** is formed over the protective insulating layer **106**. The overcoat layer **192** is formed so as to cover the color filter layer **191** and the protective insulating layer **109** is formed so as to cover the protective insulating layer **106** and the overcoat layer **192**.

Next, a ninth photolithography step is performed. A resist mask is formed and contact holes which reach the first terminal **121**, the conductive layer **162**, the drain electrode layer **105***b*, and the second terminal **122** are formed by etching the gate insulating layer **102**, the oxide insulating film **107**, the protective insulating layer **106**, and the protective insulating layer **109**. After a light-transmitting conductive film is formed, a tenth photolithography step is performed. Resist masks are formed and selective etching is performed to form the first electrode layer **110**, the terminal electrode **128**, the terminal electrode **129**, and a wiring layer **145**.

This embodiment is an example where the first terminal **121** and the terminal electrode **128** are directly connected to each other without the connection electrode **120**. Further, the drain electrode layer **165***b* and the conductive layer **162** are connected to each other through the wiring layer **145**.

In the capacitor portion, the capacitor **147** is formed from a stack of the capacitor wiring layer **108**, the gate insulating layer **102**, and the capacitor electrode layer **149** formed in the same step as the source electrode layer and the drain electrode layer.

Through the above steps, a thin film transistor **183** in the driving circuit portion and a thin film transistor **173** in a pixel portion can be formed over one substrate.

As an Embodiment 1, the partition **193** is formed and the EL layer **194** and the second electrode layer **195** are stacked over the first electrode layer **110**, whereby the light-emitting device of this embodiment, which includes a light-emitting element, is manufactured (see FIG. **10**).

This embodiment can be implemented in appropriate combination with any of the structures described in Embodiments 1 to 4.

Embodiment 6

This embodiment shows an example of a manufacturing method for a light-emitting device by separating a thin film transistor from a manufacturing substrate and transferring the thin film transistor to a flexible substrate. A light-emitting device, one embodiment of the present invention, is described using FIG. **27**, FIGS. **28**A and **28**B, FIGS. **29**A and **29**B, and FIG. **30**. FIG. **27** shows an example of the light-emitting device described in this embodiment. Note that this embodiment is the same as Embodiment 1 except part of the process; thus, the same portions are denoted by the same reference numerals, and detailed description of the same portions is omitted.

A light-emitting device **8400** has a pixel portion **8250**, a driving circuit portion **8252**, and terminal portions **8254** and **8255**. The pixel portion **8250** and the driving circuit portion **8252** are formed between a first substrate **8100** which is thin, lightweight and has a light-transmitting property, and a second substrate **8144** which is thin and has low water permeability. In addition, the pixel portion **8250** and the driving circuit portion **8252** are held between a resin layer **8141** touching the first substrate **8100** and a resin layer **8142** touching the second substrate **8144**.

The pixel portion **8250** has the thin film transistor **170**, and a light-emitting element including the first electrode layer **110**, the EL layer **194**, and the second electrode layer **195**. Further, one of a source electrode and a drain electrode of the thin film transistor **170** is connected to the first electrode layer **110** of the light-emitting element. Note that the partition **193** is provided to cover a part of the first electrode layer **110**. The pixel portion **8250** has the capacitor **147**.

The driving circuit portion **8252** has the thin film transistor **180**.

A summary of the manufacturing method for the light-emitting device **8400** shown as an example in this embodiment is as follows. First, as a layer to be separated, the terminal portions of the light-emitting device **8400**, the thin film transistor **170**, the thin film transistor **180**, the capacitor **147**, the color filter layer **191**, the overcoat layer **192**, the oxide insulating film **107**, the protective insulating layer **106**, the protective insulating layer **109**, and the first electrode layer **110** of the light-emitting element are formed over a separation layer of a first manufacturing substrate. Next, after the layer to be separated is temporarily bonded to a second manufacturing substrate (also referred to as a support substrate), the layer to be separated is separated from the first manufacturing substrate. Then, the layer to be separated is bonded and transferred to the first substrate **8100** which is thin, lightweight and has a light-transmitting property, and the second manufacturing substrate which is temporarily bonded is removed from the layer to be separated. Then, after forming a light-emitting element over the first electrode layer **110** exposed on the surface of the layer to be separated, the second substrate **8144** which is thin and has low water permeability is bonded to a surface of the layer to be separated on which the light-emitting element is formed, so that the light-emitting device **8400** is manufactured.

An example of the manufacturing method for the light-emitting device **8400** is described in detail with reference to FIGS. **28**A and **28**B, FIGS. **29**A and **29**B, and FIG. **30**.

A separation layer **302** is formed over a first manufacturing substrate **300** and a first insulating layer **8104** is formed over the separation layer **302**. Preferably, the first insulating layer **8104** is successively formed without exposing the formed separation layer **302** to air. This successive formation prevents dust or impurities from entering between the separation layer **302** and the insulating layer **8104**.

As the first manufacturing substrate **300**, a glass substrate, a quartz substrate, a sapphire substrate, a ceramic substrate, a metal substrate, or the like can be used. Alternatively, a plastic substrate having heat resistance to the processing temperature of this embodiment may be used. In the manufacturing process of a semiconductor device, a manufacturing substrate can be selected as appropriate in accordance with the process.

Further, when the temperature of heat treatment performed later is high, a substrate having a strain point of 730° C. or higher is preferably used as the glass substrate. For a glass substrate, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used, for example. By containing more barium oxide (BaO) than boric acid, a more practical heat-resistant glass substrate can be obtained. Therefore, a glass substrate containing BaO more than B_2O_3 is preferably used. Furthermore, crystallized glass or the like can be used.

Note that in this process, the separation layer **302** is formed on an entire surface of the first manufacturing substrate **300**; however, after forming the separation layer **302** on the entire surface of the first manufacturing substrate **300**, the separation layer **302** may be selectively removing so that the separation layer can be formed only on a desired region, if needed. Further, the separation layer **302** is formed in contact with the first manufacturing substrate **300** in FIGS. **28**A and **28**B, though an insulating layer can be formed between the first manufacturing substrate **300** and the separation layer **302** using a silicon oxide film, a silicon oxynitride film, a silicon nitride film, a silicon nitride oxide film, or the like, if needed.

The separation layer **302** has a single-layer structure or a stacked-layer structure containing an element selected from tungsten (W), molybdenum (Mo), titanium (Ti), tantalum (Ta), niobium (Nb), nickel (Ni), cobalt (Co), zirconium (Zr), ruthenium (Ru), rhodium (Rh), palladium (Pd), osmium (Os), iridium (Ir), or silicon (Si); or an alloy material containing any of the elements as its main component; a compound material containing any of the elements as its main component. A crystalline structure of a layer containing silicon may be any of an amorphous structure, a microcrystalline structure, and a polycrystalline structure.

The separation layer **302** can be formed by a sputtering method, a plasma CVD method, a coating method, a printing method, or the like. Note that the coating method includes a spin coating method, a droplet discharge method, and a dispensing method.

In the case where the separation layer **302** has a single-layer structure, a tungsten layer, a molybdenum layer, or a layer containing a mixture of tungsten and molybdenum is preferably formed. Alternatively, a layer containing an oxide or an oxynitride of tungsten, a layer containing an oxide or an oxynitride of molybdenum, or a layer containing an oxide or an oxynitride of a mixture of tungsten and molybdenum is formed. Note that the mixture of tungsten and molybdenum corresponds to an alloy of tungsten and molybdenum, for example.

In the case where the separation layer **302** has a stacked-layer structure, as a first layer, a tungsten layer, a molybdenum layer, or a layer containing a mixture of tungsten and

molybdenum is preferably formed. As a second layer, an oxide of tungsten, molybdenum, or a mixture of tungsten and molybdenum; a nitride of tungsten, molybdenum, or a mixture of tungsten and molybdenum; an oxynitride of tungsten, molybdenum, or a mixture of tungsten and molybdenum; or a nitride oxide of tungsten, molybdenum, or a mixture of tungsten and molybdenum is preferably formed.

In the case where the stacked-layer structure of a layer containing tungsten and a layer containing an oxide of tungsten is formed as the separation layer **302**, the following manner may be utilized: the layer containing tungsten is formed, and an insulating layer formed using an oxide is formed over the layer containing tungsten, whereby the layer containing an oxide of tungsten is formed in the interface between the tungsten layer and the insulating layer.

In addition, in the case where the separation layer is formed and then the thin film transistor and the light-emitting element are formed over the manufacturing substrate, the separation layer is heated by heat treatment for dehydration or dehydrogenation of an oxide semiconductor layer. Thus, when separation is performed from the manufacturing substrate to a supporting substrate in a later process, separation at an interface of the separation layer can be easily performed.

Further, the layer containing an oxide of tungsten may be formed by performing thermal oxidation treatment, oxygen plasma treatment, treatment with a highly oxidizing solution such as ozone water, or the like on the surface of the layer containing tungsten. The plasma treatment and the heat treatment may be performed in an atmosphere of oxygen, nitrogen, or dinitrogen monoxide alone, or a mixed gas of any of these gases and another gas. The same applies to the case of forming a layer containing a nitride, an oxynitride, or a nitride oxide of tungsten. After a layer containing tungsten is formed, a silicon nitride layer, a silicon oxynitride layer, or a silicon nitride oxide layer may be formed thereover.

A layer **304** to be separated is formed over the separation layer **302**. The layer **304** to be separated has the first insulating layer **8104** over which the thin film transistor **170**, the thin film transistor **180**, the capacitor **147**, the color filter layer **191**, the overcoat layer **192**, the oxide insulating film **107**, the protective insulating layer **106**, the protective insulating layer **109**, and the first electrode layer **110** of the light-emitting element are formed.

First, the first insulating layer **8104** is formed over the separation layer **302**. The first insulating layer **8104** is preferably formed as a single-layer or a multilayer of an insulating film containing nitrogen and silicon, such as a silicon nitride film, a silicon oxynitride film, or a silicon nitride oxide film.

The first insulating layer **8104** can be formed using a sputtering method, a plasma CVD method, a coating method, a printing method, or the like. For example, the first insulating layer **8104** is formed at a film formation temperature of 250° C. to 400° C. by a plasma CVD method, whereby a dense film having very low water permeability can be obtained. Note that the first insulating layer **8104** is preferably formed to a thickness of 10 nm to 1000 nm, more preferably a thickness of 100 nm to 700 nm.

By forming the first insulating layer **8104**, separation can be easily performed at an interface between the first insulating layer **8104** and the separation layer **302** in a later separation process. Further, the semiconductor element or the wiring can be prevented from being cracked or damaged in the later separation process. Furthermore, the first insulating layer **8104** serves as a protective layer of the light-emitting device **8400**.

The layer **304** to be separated is formed over the first insulating layer **8104**. The layer **304** to be separated can be formed using the method described in Embodiment 1; accordingly a detailed description thereof is omitted here.

Next, a second manufacturing substrate **306** is temporarily bonded to the layer **304** to be separated using an adhesive layer **305** which can be removed. By bonding the second manufacturing substrate **306** to the layer **304** to be separated, the layer **304** to be separated can be easily separated from the separation layer **302**. In addition, it is possible to lower stress added to the layer **304** to be separated through the separation process, and the thin film transistors can be protected. Further, since the adhesive layer **305** which can be removed is used, the second manufacturing substrate **306** can be easily removed after use.

As the adhesive layer **305** which can be removed, for example, a water-soluble resin can be used. Unevenness of the layer **304** to be separated is reduced by applying the water soluble-resin, so that the layer **304** to be separated can be easily bonded to the second manufacturing substrate **306**. In addition, as the adhesive layer **305** which can be removed, a stack of water-soluble resin and an adhesive capable of being separated by light or heat may be used.

Next, the layer **304** to be separated is separated from the first manufacturing substrate **300** (see FIG. **28**B). As a separation method, any of various methods can be used.

For example, when a metal oxide film is formed as the separation layer **302** on the side that is in contact with the first insulating layer **8104**, the metal oxide film is weakened by crystallization, so that the layer **304** to be separated can be separated from the first manufacturing substrate **300**. In addition, after the metal oxide film is weakened by crystallization, a part of the separation layer **302** may be removed by etching using a solution or a fluoride halogen gas such as NF_3, BrF_3, or ClF_3 and separation may be performed along the weakened metal oxide film.

When a film containing nitrogen, oxygen, hydrogen, or the like (e.g., an amorphous silicon film containing hydrogen, an alloy film containing hydrogen, or an alloy film containing oxygen) is used as the separation layer **302** and a substrate having a light-transmitting property is used as the first manufacturing substrate **300**, the following manner can be used: the separation layer **302** is irradiated with laser light through the first manufacturing substrate **300**, and nitrogen, oxygen, or hydrogen contained in the separation layer is evaporated, so that separation can occur between the first manufacturing substrate **300** and the separation layer **302**.

Further, by removing the separation layer **302** by etching, the layer **304** to be separated may be separated from the first manufacturing substrate **300**.

It is also possible to use a method for removing the first manufacturing substrate **300** by mechanical polishing, a method for removing the first manufacturing substrate **300** by etching using a halogen fluoride gas such as NF_3, BrF_3 or ClF_3, or HF, or the like. In this case, the separation layer **302** is not necessarily used.

Moreover, the layer **304** to be separated can be separated from the first manufacturing substrate **300** in the following manner: a groove to expose the separation layer **302** is formed by laser irradiation, by etching using a gas, a solution, or the like, or with a sharp knife or a scalpel, so that separation occurs along the interface between the separation layer **302** and the first insulating layer **8104** serving as a protective layer, with the groove used as a trigger.

As the separation method, for example, mechanical force (separation treatment with a human hand or with a gripper, separation treatment by rotation of a roller, or the like) may also be used. Alternatively, a liquid may be dropped into the groove to allow the liquid to be infiltrated into the interface between the separation layer **302** and the first insulating layer **8104**, which may be followed by the separation of the layer **304** to be separated from the separation layer **302**. Further alternatively, a method may be used in which a fluoride gas such as NF_3, BrF_3, or ClF_3 is introduced into the groove and the separation layer **302** is removed by etching with the use of the fluoride gas so that the layer **304** to be separated is separated from the first manufacturing substrate **300** having an insulating surface. Furthermore, the separation may be performed while pouring a liquid such as water during the separation.

As another separation method, when the separation layer **302** is formed using tungsten, separation can be performed while the separation layer is etched by a mixed solution of ammonia water and hydrogen peroxide water.

Next, the first substrate **8100** which is thin, lightweight and has a light-transmitting property is bonded to the layer **304** to be separated using the resin layer **8141** (see FIG. **29**A).

As the first substrate **8100** which is thin, lightweight and has a light-transmitting property, a substrate having flexibility and a light-transmitting property with respect to visible light can be used. For example, it is preferable to use a polyester resin such as polyethylene terephthalate (PET) or polyethylene naphthalate (PEN), a polyacrylonitrile resin, a polyimide resin, a polymethyl methacrylate resin, a polycarbonate (PC) resin, a polyethersulfone (PES) resin, a polyamide resin, a cycloolefin resin, a polystyrene resin, a polyamide imide resin, or a polyvinylchloride resin, or the like. In addition, over the first substrate **8100**, a protective film with low water permeability, such as a film containing nitrogen and silicon, e.g., a silicon nitride film or a silicon oxynitride film, or a film containing nitrogen and aluminum e.g., an aluminum nitride film, may be formed in advance. Note that a structure body in which a fibrous body is impregnated with an organic resin (so-called prepreg) may be used as the first substrate **8100**.

In the case where a fibrous body is included in the material of the first substrate **8100**, a high-strength fiber of an organic compound or an inorganic compound is used as the fibrous body. A high-strength fiber is specifically a fiber with a high tensile modulus of elasticity or a fiber with a high Young's modulus. As a typical example of a high-strength fiber, a polyvinyl alcohol based fiber, a polyester based fiber, a polyamide based fiber, a polyethylene based fiber, an aramid based fiber, a polyparaphenylene benzobisoxazole fiber, a glass fiber, or a carbon fiber can be given. As a glass fiber, there is a glass fiber using E glass, S glass, D glass, Q glass, or the like. These fibers may be used in a state of a woven fabric or a nonwoven fabric, and a structure body in which this fibrous body is impregnated with an organic resin and the organic resin is cured may be used as the first substrate **8100**. When the structure body including the fibrous body and the organic resin is used as the first substrate **8100**, reliability against bending or breaking due to local pressure can be increased, which is preferable.

Note that in the case where the first substrate **8100** includes the above fibrous body, in order to reduce prevention of light emitted from the light-emitting element to the outside, the fibrous body is preferably a nanofiber with a diameter of 100 nm or less. Further, refractive indexes of the fibrous body and the organic resin or the adhesive preferably match with each other.

As the resin layer **8141**, various curable adhesives, e.g., a light curable adhesive such as a UV curable adhesive, a reactive curable adhesive, a thermal curable adhesive, and an anaerobic adhesive can be used. As the material of these adhesives, an epoxy resin, an acrylic resin, a silicone resin, a phenol resin, or the like can be used.

Note that in the case where a prepreg is used as the first substrate **8100**, the layer **304** to be separated and the first substrate **8100** are directly bonded to each other by pressure bonding without using the adhesive. At this time, as the organic resin for the structure body, a reactive curable resin, a thermal curable resin, a UV curable resin, or the like which is better cured by additional treatment is preferably used.

After forming the first substrate **8100**, the second manufacturing substrate **306** and the adhesive layer **305** which can be removed are removed, whereby the first electrode layer **110** is exposed (see FIG. **29**B).

According to the above process, the layer **304** to be separated which includes the thin film transistor **170**, the thin film transistor **180**, and the first electrode layer **110** of the light-emitting element, can be formed over the first substrate **8100**.

Next, the partition **193** covering a part of the first electrode layer **110** is formed. The EL layer **194** is formed over the first electrode layer **110**. The EL layer **194** can be formed using either a low molecular material or a high molecular material. Note that a material forming the EL layer **194** is not limited to a material containing only an organic compound material, and it may partly contain an inorganic compound material. The EL layer **194** needs to have at least a light-emitting layer, and a single-layer structure that is formed using a single light-emitting layer or a stacked-layer structure including layers each having different functions may be used. For example, functional layers such as a hole-injection layer, a hole-transport layer, a carrier-blocking layer, an electron-transport layer, and an electron-injection layer can be combined as appropriate in addition to a light-emitting layer. Note that a layer having two or more functions of the respective functions of the layers may be included.

The EL layer **194** can be formed using either a wet process or a dry process, such as an evaporation method, an inkjet method, a spin coating method, a dip coating method, or a nozzle printing method.

Next, the second electrode layer **195** is formed over the EL layer **194**. The second electrode layer **195** may be formed using a material similar to that of the first electrode layer **110**. Note that in the case where the first electrode layer **110** serves as an anode, the second electrode layer **195** serves as a cathode and in the case where the first electrode layer **110** serves as a cathode, the second electrode layer **195** serves as an anode; therefore, the first electrode layer **110** and the second electrode layer **195** are formed by selecting a material having a work function corresponding to the polarity of the respective electrode layers.

In this embodiment, the first electrode layer **110** is used as an anode, and the EL layer **194** has a structure in which a hole-injection layer, a hole-transport layer, a light-emitting layer, and an electron-injection layer are sequentially stacked from the first electrode layer **110** side. Various kinds of materials can be used for the light-emitting layer. For example, a fluorescent compound which exhibits fluorescence or a phosphorescent compound which exhibits phosphorescence can be used. In addition, as the second electrode layer **195**, a material with a low work function is used.

Since light is emitted through the first electrode layer **110** side, a highly reflective material is selected for the second electrode layer **195**.

Through the above process, the pixel portion **8250** including the thin film transistor **170** and the light-emitting element is formed.

Further, a protective film may be formed over the second electrode layer **195**. For example, the protective film is formed as a single-layer or a multilayer using a material containing nitrogen and silicon such as silicon nitride, silicon nitride oxide, or silicon oxynitride; aluminum oxide; or the like by a sputtering method, a plasma CVD method, a coating method, a printing method, or the like. Alternatively, the above inorganic insulating film and an organic insulating film such as a resin film may be stacked to form the protective film. By forming the protective film, moisture and gas such as oxygen can be prevented from entering the element portion. The thickness of the protective film functioning as a protective layer is preferably 10 nm to 1000 nm, more preferably, 100 to 700 nm. Note that the terminal portions **8254** and **8255** are covered with a shadow mask or the like so that the protective film is not formed thereover (see FIG. **30**).

Next, the second substrate **8144** is bonded to cover the pixel portion **8250** and the driving circuit portion **8252**. The second substrate **8144** is bonded over the pixel portion **8250** and the driving circuit portion **8252** using the resin layer **8142**.

The resin layer **8142** is preferably formed using a material with good adhesion properties. For example, the following materials can be used: an organic compound such as acrylic resins, polyimide resins, melamine resins, polyester resins, polycarbonate resins, phenol resins, epoxy resins, polyacetal, polyether, polyurethane, polyamide (nylon), furan resins, or diallylphthalate resins; inorganic siloxane polymers including a Si—O—Si bond among compounds including silicon, oxygen, and hydrogen, formed by using a siloxane-polymer-based material typified by silica glass as a starting material; or organic siloxane polymers in which hydrogen bonded with silicon is substituted by an organic group such as methyl or phenyl, typified by alkylsiloxane polymers, alkylsilsesquioxane polymers, silsesquioxane hydride polymers, or alkylsilsesquioxane hydride polymers. Further, a fibrous body may be included in these materials of the resin layer **8142**.

The resin layer **8142** can be formed, for example, by applying a composition using a coating method and then drying by heating. Alternatively, a structure body in which a fibrous body is impregnated with an organic resin may be used as the resin layer **8142**.

As the second substrate **8144**, a substrate which is thin and has low water permeability is used. For example, a metal substrate can be used. A material for forming the metal substrate is not limited to a particular material; however, aluminum, copper, nickel, an alloy of metals such as an aluminum alloy or stainless steel, or the like can be preferably used. Note that before bonding, the second substrate **8144** is preferably subjected to baking or plasma treatment in vacuum so as to remove moisture attached to the surface of the metal substrate. A resin film may also be formed on the surface of the second substrate **8144** to protect the second substrate **8144**.

The second substrate **8144** can also be bonded using a laminator. For example, a sheet-like adhesive is applied to the metal substrate using a laminator and the metal substrate may further be bonded to the pixel portion **8250** and the driving circuit portion **8252** using a laminator. Alternatively, the resin layer **8142** is printed on the second substrate **8144** by screen printing or the like and the second substrate **8144** is bonded to the light-emitting element using a laminator. Note that this process is preferably carried out under a reduced pressure, so that bubbles are hardly entered (see FIG. **27**).

In the above-described manner, the light-emitting device, one embodiment of the present invention can be manufactured.

Note that this embodiment shows an example of the method in which the thin film transistor and the first electrode of the light-emitting element and formed in a layer to be separated; however, the invention disclosed in this specification is not limited thereto. The separation and transfer may be performed after the light-emitting element is formed (i.e., after a second electrode of the light-emitting element is formed). Further, the layer to be separated including only the first insulating layer and the first electrode layer may be separated and transferred to the first substrate, and the thin film transistor and the light-emitting element may be manufactured after the transfer. Furthermore, only the first insulating layer may be formed over the manufacturing substrate, and then separated and transferred to a substrate, and the thin film transistor and the light-emitting element may be manufactured thereafter.

The light-emitting device **8400** of this embodiment is formed between the first substrate **8100** which is thin, lightweight and has a light-transmitting property, and the second substrate **8144** which is thin and has low water permeability, so that a light-emitting device which is lightweight, easily handled and has flexibility can be provided. In addition, as a support body of the light-emitting device, the second substrate **8144** with low water permeability is formed using a metal substrate. As a result, moisture is prevented from entering the light-emitting element, and a light-emitting device with a long lifetime can be obtained.

According to this embodiment, a thin film transistor manufactured using a substrate having high heat resistance can be transferred to a first substrate which is thin, lightweight and has a light-transmitting property. Therefore, a thin film transistor with high reliability and excellent electric characteristics can be formed without being restricted by the heat resistance of the first substrate. A light-emitting device in which such a thin film transistor is formed in a pixel portion and a driving circuit portion formed on the same substrate has excellent reliability and operation characteristics.

Note that the structure described in this embodiment can be combined with any of the structures described in other embodiments as appropriate.

Embodiment 7

In this embodiment, in the light-emitting device described in any of Embodiments 1 to 6, an example of manufacturing an active matrix light-emitting display device with the use of a thin film transistor and a light-emitting element utilizing electroluminescence will be described.

Light-emitting elements utilizing electroluminescence are classified according to whether a light-emitting material is an organic compound or an inorganic compound. In general, the former is referred to as an organic EL element, and the latter is referred to as an inorganic EL element.

In the organic EL element, by application of voltage to a light-emitting element, electrons and holes are separately injected from a pair of electrodes into a layer containing a light-emitting organic compound, and thus current flows.

Then, the carriers (electrons and holes) recombine, so that the light-emitting organic compound is excited. The light-emitting organic compound returns to a ground state from the excited state, thereby emitting light. Owing to such a mechanism, such a light-emitting element is referred to as a current-excitation light-emitting element.

The inorganic EL elements are classified according to their element structures into a dispersion-type inorganic EL element and a thin-film inorganic EL element. The dispersion-type inorganic EL element has a light-emitting layer where particles of a light-emitting material are dispersed in a binder, and its light emission mechanism is donor-acceptor recombination type light emission which utilizes a donor level and an acceptor level. The thin-film inorganic EL element has a structure where a light-emitting layer is sandwiched between dielectric layers, which are further sandwiched between electrodes, and its light emission mechanism is localized type light emission that utilizes inner-shell electron transition of metal ions. Note that an example of an organic EL element as a light-emitting element is described here.

FIG. **19** shows an example of a pixel structure to which digital time grayscale driving can be applied, as an example of a light-emitting device.

The structure and operation of a pixel to which digital time grayscale driving can be applied are described. Here, the following example is shown: one pixel includes two n-channel transistors each of which uses an oxide semiconductor layer for a channel formation region.

A pixel **6400** includes a switching transistor **6401**, a driving transistor **6402**, a light-emitting element **6404**, and a capacitor **6403**. A gate of the switching transistor **6401** is connected to a scan line **6406**, a first electrode (one of a source electrode and a drain electrode) of the switching transistor **6401** is connected to a signal line **6405**, and a second electrode (the other of the source electrode and the drain electrode) of the switching transistor **6401** is connected to a gate of the driving transistor **6402**. The gate of the driving transistor **6402** is connected to a power supply line **6407** through the capacitor **6403**. A first electrode of the driving transistor **6402** is connected to the power supply line **6407**. A second electrode of the driving transistor **6402** is connected to a first electrode (pixel electrode) of the light-emitting element **6404**. A second electrode of the light-emitting element **6404** corresponds to a common electrode **6408**. The common electrode **6408** is electrically connected to a common potential line provided over the same substrate.

The second electrode (common electrode **6408**) of the light-emitting element **6404** is set to a low power supply potential. Note that the low power supply potential is a potential which satisfies the low power supply potential<a high power supply potential with reference to the high power supply potential that is set to the power supply line **6407**. As the low power supply potential, GND, 0 V, or the like may be employed, for example. A potential difference between the high power supply potential and the low power supply potential is applied to the light-emitting element **6404** so that current flows through the light-emitting element **6404**, whereby the light-emitting element **6404** emits light. Thus, each potential is set so that the potential difference between the high power supply potential and the low power supply potential is higher than or equal to a forward threshold voltage of the light-emitting element **6404**.

When gate capacitance of the driving transistor **6402** is used as a substitute for the capacitor **6403**, the capacitor **6403** can be omitted. The gate capacitance of the driving transistor **6402** may be formed between a channel region and a gate electrode.

In the case of a voltage-input voltage driving method, a video signal is input to the gate of the driving transistor **6402** so that the driving transistor **6402** is completely turned on or off That is, the driving transistor **6402** operates in a linear region; thus, voltage higher than the voltage of the power supply line **6407** is applied to the gate of the driving transistor **6402**. Note that voltage higher than or equal to (voltage of the power supply line+V_{th} of the driving transistor **6402**) is applied to the signal line **6405**.

In the case of performing analog grayscale driving instead of digital time grayscale driving, the same pixel structure as in FIG. **19** can be used by changing signal input.

In the case where the analog grayscale driving is performed, a voltage higher than or equal to voltage which is the sum of the forward voltage of the light-emitting element **6404** and V_{th} of the driving transistor **6402** is applied to the gate of the driving transistor **6402**. The forward voltage of the light-emitting element **6404** refers to a voltage at which a desired luminance is obtained, and includes at least forward threshold voltage. By inputting a video signal to enable the driving transistor **6402** to operate in a saturation region, current can flow through the light-emitting element **6404**. In order that the driving transistor **6402** can operate in the saturation region, the potential of the power supply line **6407** is set higher than the gate potential of the driving transistor **6402**. With an analog video signal, current in accordance with the video signal flows through the light-emitting element **6404**, and the analog grayscale driving can be performed.

Note that the pixel structure shown in FIG. **19** is not limited thereto. For example, a switch, a resistor, a capacitor, a transistor, a logic circuit, or the like may be added to the pixel shown in FIG. **19**.

Next, structures of the light-emitting element are described with reference to FIGS. **20**A to **20**C. Here, a cross-sectional structure of a pixel is described by taking an n-channel driving TFT as an example. Driving TFTs **7001**, **7011**, and **7021** used in light-emitting devices shown in FIGS. **20**A, **20**B, and **20**C in Embodiments 1 to 5, respectively, can be formed in a manner similar to that of the thin film transistor described in any of Embodiments 1 to 5, and are highly reliable thin film transistors each including an oxide semiconductor layer.

In order to extract light emitted from the light-emitting element, at least one of an anode and a cathode is required to transmit light. A thin film transistor and a light-emitting element are formed over a substrate. A light-emitting element can have a top emission structure in which light is extracted through the surface opposite to the substrate; a bottom emission structure in which light is extracted through the surface on the substrate side; or a dual emission structure in which light is extracted through the surface opposite to the substrate and the surface on the substrate side. The pixel structure can be applied to a light-emitting element having any of these emission structures.

A light-emitting element having the bottom emission structure will be described with reference to FIG. **20**A.

FIG. **20**A is a cross-sectional view of a pixel in the case where the driving TFT **7011** is an n-channel transistor and light is emitted from a light-emitting element **7012** to a first electrode layer **7013** side. In FIG. **20**A, the first electrode layer **7013** of the light-emitting element **7012** is formed over a light-transmitting conductive film **7017** which is electrically connected to the driving TFT **7011**. An EL layer **7014**

and a second electrode layer **7015** are stacked in this order over the first electrode layer **7013**. Note that the conductive film **7017** is electrically connected to a drain electrode layer of the driving TFT **7011** through a contact hole formed in a protective insulating layer **7035**, a protective insulating layer **7032**, and an oxide insulating layer **7031**.

As the light-emitting conductive film **7017**, the following light-transmitting conductive films can be used: film of indium oxide including tungsten oxide, indium zinc oxide including tungsten oxide, indium oxide including titanium oxide, indium tin oxide including titanium oxide, indium tin oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added.

Further, a variety of materials can be used for the first electrode layer **7013** of the light-emitting element. For example, in the case where the first electrode layer **7013** is used as a cathode, a material having a low work function such as an alkali metal such as Li or Cs, an alkaline earth metal such as Mg, Ca, or Sr, an alloy containing any of them (e.g., Mg:Ag, Al:Li), or a rare earth metal such as Yb or Er is preferable. In FIG. **20**A, the first electrode layer **7013** is formed to have a thickness through which light can be transmitted (preferably, approximately 5 nm to 30 nm). For example, an aluminum film with a thickness of 20 nm is used as the first electrode layer **7013**.

Alternatively, a light-transmitting conductive film and an aluminum film may be stacked and then selectively etched so as to form the light-transmitting conductive film **7017** and the first electrode layer **7013**, which is preferable because the etching can be performed using the same mask.

Further, the periphery portion of the first electrode layer **7013** is covered with a partition **7019**. The partition **7019** is formed using a film of an organic resin such as polyimide, acrylic, polyamide, or epoxy, an inorganic insulating film, or organic polysiloxane. It is particularly preferable that the partition **7019** be formed using a photosensitive resin material to have an opening portion over the first electrode layer **7013** so that a sidewall of the opening portion is formed as a tilted surface with continuous curvature. When a photosensitive resin material is used for the partition **7019**, a step of forming a resist mask can be omitted.

Further, the EL layer **7014** formed over the first electrode layer **7013** and the partition **7019** may include at least a light-emitting layer and be formed using a single-layer or a plurality of layers stacked. When the EL layer **7014** is formed using a plurality of layers, an electron-injection layer, an electron-transport layer, a light-emitting layer, a hole-transport layer, and a hole-injection layer are stacked in this order over the first electrode layer **7013** functioning as a cathode. Note that it is not necessary to form all of these layers.

The stacking order is not limited to the above order. The first electrode layer **7013** may function as an anode and a hole-injection layer, hole-transport layer, a light-emitting layer, an electron-transport layer, and an electron-injection layer may be stacked in this order over the first electrode layer **7013**. Note that from a power consumption standpoint, it is preferable to make the first electrode layer **7013** function as a cathode and to stack an electron-injection layer, an electron-transport layer, a light-emitting layer, a hole-transport layer, and a hole-injection layer in this order over the first electrode layer **7013** because increase in driving voltage of the driving circuit portion can be suppressed and thus power consumption can be reduced.

Further, a variety of materials can be used for the second electrode layer **7015** formed over the EL layer **7014**. For example, in the case where the second electrode layer **7015** is used as an anode, a material having a high work function, such as ZrN, Ti, W, Ni, Pt, or Cr, or a transparent conductive material such as ITO, IZO, or ZnO is preferable. Further, over the second electrode layer **7015**, a light-blocking film **7016** is formed using a metal blocking light, a metal reflecting light, or the like. In this embodiment, an ITO film is used as the second electrode layer **7015** and a Ti film is used as the light-blocking film **7016**.

The light-emitting element **7012** corresponds to a region where the EL layer **7014** including a light-emitting layer is sandwiched with the first electrode layer **7013** and the second electrode layer **7015**. In the case of the element structure shown in FIG. **20**A, light is emitted from the light-emitting element **7012** to the first electrode layer **7013** side to pass through a color filter layer **7033** to the outside as indicated by an arrow.

The color filter layer **7033** is formed by a droplet discharge method such as an ink-jet method, a printing method, an etching method with the use of a photolithography technique, or the like.

The color filter layer **7033** is covered with an overcoat layer **7034** and the protective insulating layer **7035** is further formed thereover. Note that although the overcoat layer **7034** is illustrated to have a small thickness in FIG. **20**A, the overcoat layer **7034** has a function of reducing roughness caused by the color filter layer **7033**.

Next, a light-emitting element having the dual emission structure will be described with reference to FIG. **20**B.

In FIG. **20**B, a first electrode layer **7023** of a light-emitting element **7022** is formed over a light-transmitting conductive film **7027** which is electrically connected to the driving TFT **7021**. An EL layer **7024** and a second electrode layer **7025** are stacked in this order over the first electrode layer **7023**. Note that the conductive film **7027** is electrically connected to a drain electrode layer of the driving TFT **7021** through a contact hole formed in a protective insulating layer **7045**, a protective insulating layer **7042**, and an oxide insulating layer **7041**.

As the light-emitting conductive film **7027**, the following light-transmitting conductive film can be used: film of indium oxide including tungsten oxide, indium zinc oxide including tungsten oxide, indium oxide including titanium oxide, indium tin oxide including titanium oxide, indium tin oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added.

A variety of materials can be used for the first electrode layer **7023**. For example, in the case where the first electrode layer **7023** is used as a cathode, a material having a low work function such as an alkali metal such as Li or Cs, an alkaline earth metal such as Mg, Ca, or Sr, an alloy containing any of them (e.g., Mg:Ag, Al:Li), or a rare earth metal such as Yb or Er is preferable. In this embodiment, the first electrode layer **7023** functions as a cathode and is formed to have a thickness through which light can be transmitted (preferably, approximately 5 nm to 30 nm). For example, an aluminum film with a thickness of 20 nm is used as the cathode.

Alternatively, a light-transmitting conductive film and an aluminum film may be stacked and then selectively etched so as to form the light-transmitting conductive film **7027** and the first electrode layer **7023**. In this case, it is preferable that the etching can be performed using the same mask.

Further, the periphery portion of the first electrode layer **7023** is covered with a partition **7029**. The partition **7029** is formed using a film of an organic resin such as polyimide, acrylic, polyamide, or epoxy, an inorganic insulating film, or organic polysiloxane. It is particularly preferable that the partition **7029** be formed using a photosensitive resin mate-

rial to have an opening portion over the first electrode layer **7023** so that a sidewall of the opening portion is formed as a tilted surface with continuous curvature. When a photosensitive resin material is used for the partition **7029**, a step of forming a resist mask can be omitted.

Further, the EL layer **7024** formed over the first electrode layer **7023** and the partition **7029** may include at least a light-emitting layer and be formed using a single-layer or a plurality of layers stacked. When the EL layer **7024** is formed using a plurality of layers, an electron-injection layer, an electron-transport layer, a light-emitting layer, a hole-transport layer, and a hole-injection layer are stacked in this order over the first electrode layer **7023** functioning as a cathode. Note that it is not necessary to form all of these layers.

The stacking order is not limited to the above order. The first electrode layer **7023** may function as an anode and a hole-injection layer, hole-transport layer, a light-emitting layer, an electron-transport layer, and an electron-injection layer may be stacked in this order over the anode. Note that from a power consumption standpoint, it is preferable to make the first electrode layer **7023** function as a cathode and to stack an electron-injection layer, an electron-transport layer, a light-emitting layer, a hole-transport layer, and a hole-injection layer in this order over the cathode because power consumption can be reduced.

Further, a variety of materials can be used for the second electrode layer **7025** formed over the EL layer **7024**. For example, in the case where the second electrode layer **7025** is used as an anode, a material having a high work function, for example, a transparent conductive material such as ITO, IZO, or ZnO, is preferably used. In this embodiment, the second electrode layer **7025** is used as an anode and an ITO film including silicon oxide is formed.

The light-emitting element **7022** corresponds to a region where the EL layer **7024** including a light-emitting layer is sandwiched with the first electrode layer **7023** and the second electrode layer **7025**. In the case of the element structure shown in FIG. **20**B, light is emitted from the light-emitting element **7022** to both the second electrode layer **7025** side and the first electrode layer **7023** side as indicated by arrows.

A color filter layer **7043** is formed by a droplet discharge method such as an ink-jet method, a printing method, an etching method with the use of a photolithography technique, or the like.

In addition, the color filter layer **7043** is covered with an overcoat layer **7044** and the protective insulating layer **7045** is further formed thereover.

Note that when a light-emitting element having a dual emission structure is used and full color display is performed on both display surfaces, light from the second electrode layer **7025** side does not pass through the color filter layer **7043**; therefore, a sealing substrate provided with another color filter layer is preferably formed over the second electrode layer **7025**.

Next, a light-emitting element having a top emission structure will be described with reference to FIG. **20**C.

FIG. **20**C is a cross-sectional view of a pixel in the case where the driving TFT **7001** is an n-channel transistor and light is emitted from a light-emitting element **7002** to a second electrode layer **7005** side. In FIG. **20**C, a first electrode layer **7003** of the light-emitting element **7002**, which is electrically connected to the driving TFT **7001**, is formed. An EL layer **7004** and the second electrode layer **7005** are staked in this order over the first electrode layer **7003**.

Further, a variety of materials can be used for the first electrode layer **7003**. For example, in the case where the first electrode layer **7003** is used as a cathode, a material having a low work function such as an alkali metal such as Li or Cs, an alkaline earth metal such as Mg, Ca, or Sr, an alloy containing any of them (e.g., Mg:Ag, Al:Li), or a rare earth metal such as Yb or Er is preferable.

Further, the periphery portion of the first electrode layer **7003** is covered with a partition **7009**. The partition **7009** is formed using a film of an organic resin such as polyimide, acrylic, polyamide, or epoxy, an inorganic insulating film, or organic polysiloxane. It is particularly preferable that the partition **7009** be formed using a photosensitive resin material to have an opening portion over the first electrode layer **7003** so that a sidewall of the opening portion is formed as a tilted surface with continuous curvature. When a photosensitive resin material is used for the partition **7009**, a step of forming a resist mask can be omitted.

Further, the EL layer **7004** formed over the first electrode layer **7003** and the partition **7009** may include at least a light-emitting layer and be formed using a single-layer or a plurality of layers stacked. When the EL layer **7004** is formed using a plurality of layers, an electron-injection layer, an electron-transport layer, a light-emitting layer, a hole-transport layer, and a hole-injection layer are stacked in this order over the first electrode layer **7003** used as a cathode. Note that it is not necessary to form all of these layers.

The stacking order is not limited to the above order. A hole-injection layer, hole-transport layer, a light-emitting layer, an electron-transport layer, and an electron-injection layer may be stacked in this order over the first electrode layer **7003** used as an anode.

In FIG. **20**C, a hole-injection layer, a hole-transport layer, a light-emitting layer, an electron-transport layer, and an electron-injection layer are stacked in this order over a stacked film in which a Ti film, an aluminum film, and a Ti film are formed in this order, and thereover, a stacked-layer of a Mg:Ag alloy thin film and an ITO film is formed.

Note that when the TFT **7001** is an n-type transistor, it is preferable to stack an electron-injection layer, an electron-transport layer, a light-emitting layer, a hole-transport layer, and a hole-injection layer in this order over the first electrode layer **7003** because increase in voltage of the driving circuit can be suppressed and thus power consumption can be reduced.

As the light-transmitting second electrode layer **7005**, the following light-transmitting conductive film can be used: film of indium oxide including tungsten oxide, indium zinc oxide including tungsten oxide, indium oxide including titanium oxide, indium tin oxide including titanium oxide, indium tin oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added.

The light-emitting element **7002** corresponds to a region where the EL layer **7004** including a light-emitting layer is sandwiched with the first electrode layer **7003** and the second electrode layer **7005**. In the case of the pixel shown in FIG. **20**C, light is emitted from the light-emitting element **7002** to the second electrode layer **7005** side as indicated by an arrow.

Further, in FIG. **20**C, a drain electrode layer of the TFT **7001** is electrically connected to the first electrode layer **7003** through a contact hole formed in an oxide insulating layer **7051**, a protective insulating layer **7052**, and a protective insulating layer **7055**. A planarizing insulating layer **7053** can be formed using a resin material such as polyimide, acrylic, benzocyclobutene, polyamide, or epoxy. In

addition to such resin materials, it is also possible to use a low dielectric constant material (a low-k material), a siloxane-based resin, PSG (phosphosilicate glass), BPSG (borophosphosilicate glass), or the like. Note that the planarizing insulating layer **7053** may be formed by stacking a plurality of insulating films formed using these materials. There is no particular limitation on a method for forming the planarizing insulating layer **7053**. The planarizing insulating layer **7053** can be formed, depending on the material, with a method such as a sputtering method, an SOG method, a spin coating method, a dipping method, a spray coating method, or a droplet discharge method (e.g., an ink-jet method, screen printing, or offset printing), or with a means such as a doctor knife, a roll coater, a curtain coater, or a knife coater.

Further, the partition **7009** is formed to insulate the first electrode layer **7003** from the first electrode layer **7003** of an adjacent pixel. The partition **7009** is formed using a film of an organic resin such as polyimide, acrylic, polyamide, or epoxy, an inorganic insulating film, or organic polysiloxane. It is particularly preferable that the partition **7009** be formed using a photosensitive resin material to have an opening portion over the first electrode layer **7003** so that a sidewall of the opening portion is formed as a tilted surface with continuous curvature. When a photosensitive resin material is used for the partition **7009**, a step of forming a resist mask can be omitted.

In the structure in FIG. **20**C, when full color display is performed, for example, the light-emitting element **7002** is used as a green light-emitting element, one of the adjacent light-emitting elements is used as a red light-emitting element, and the other is used as a blue light-emitting element. Alternatively, a light-emitting display device capable of full color display may be manufactured using four kinds of light-emitting elements, which include a white light-emitting element as well as the three kinds of the light-emitting elements.

Alternatively, in the structure in FIG. **20**C, a light-emitting display device capable of full color display may be manufactured in such a manner that all of the plurality of light-emitting elements which are arranged are white light-emitting elements and a sealing substrate having a color filter or the like is arranged over the light-emitting element **7002**. When a material which exhibits a single color such as white is formed and then combined with a color filter or a color conversion layer, full color display can be performed.

The examples in which the first electrode layer is in direct contact with the thin film transistor are shown in FIGS. **20**A to **20**C; however, as described in Embodiment 4, the drain electrode layer of the thin film transistor may be electrically connected to the first electrode layer through the connection electrode layer. The thin film transistors described in any of Embodiments 2, 3, and 5 may be used as the TFTs **7001**, **7011**, and **7021**.

Needless to say, display of monochromatic light emission can also be performed. For example, a lighting device may be formed with the use of white light emission; alternatively, an area-color type light-emitting device may be formed with the use of monochromatic light emission.

If necessary, an optical film such as a polarizing film including a circularly polarizing plate may be provided.

Note that, although the organic EL element is described here as the light-emitting element, an inorganic EL element can also be provided as a light-emitting element.

Note that the example is described in which the thin film transistor (the driving TFT) which controls the driving of a light-emitting element is electrically connected to the light-emitting element; however, a structure may be employed in which a TFT for current control is connected between a driving TFT and a light-emitting element.

This embodiment can be combined with any of the other embodiments as appropriate.

Embodiment 8

In this embodiment, an example of an element structure of the light-emitting element described in any of Embodiments 1 to 7 will be described.

In the element structure shown in FIG. **21**A, an EL layer **1003** including a light-emitting region is sandwiched between a pair of electrodes (a first electrode **1001** and a second electrode **1002**). Note that the first electrode **1001** is used as an anode and the second electrode **1002** is used as a cathode as an example in the following description of this embodiment.

The EL layer **1003** includes at least a light-emitting layer and may have a stacked structure including a functional layer in addition to the light-emitting layer. As the functional layer other than the light-emitting layer, a layer containing the following substances can be used: substance having a high hole-injection property, a substance having a high hole-transport property, a substance having a high electron-transport property, a substance having a high electron-injection property, a bipolar substance (a substance having high electron-transport and hole-transport properties), or the like. Specifically, functional layers such as a hole-injection layer, a hole-transport layer, an electron-transport layer, and an electron-injection layer can be used in combination as appropriate.

The light-emitting element shown in FIG. **21**A emits light when current flows because of a potential difference generated between the first electrode **1001** and the second electrode **1002**, and holes and electrons are recombined in the EL layer **1003**. That is, a light-emitting region is formed in the EL layer **1003**.

Light emission is extracted outside through one of or both the first electrode **1001** and the second electrode **1002**. Therefore, either or both of the first electrode **1001** and the second electrode **1002** are formed using a light-transmitting substance.

Note that a plurality of EL layers may be stacked between the first electrode **1001** and the second electrode **1002** as shown in FIG. **21**B. In the case where n (n is a natural number of 2 or more) layers are stacked, a charge generation layer **1004** is preferably provided between each m-th (m is a natural number of 1 to n−1) EL layer and each (m+1)-th EL layer.

The charge generation layer **1004** can be formed using a composite material of an organic compound and a metal oxide, a metal oxide, or a composite material of an organic compound and an alkali metal, an alkaline earth metal, or a compound thereof. Alternatively, these materials can be combined as appropriate. The composite material of an organic compound and a metal oxide includes, for example, an organic compound and a metal oxide such as V_2O_5, MoO_3, or WO_3. As the organic compound, various compounds such as an aromatic amine compound, a carbazole derivative, aromatic hydrocarbon, and a high molecular compound (oligomer, dendrimer, polymer, or the like) can be used. As the organic compound, it is preferable to use the organic compound which has a hole-transport property and has a hole mobility of 10^{-6} cm^2/vs or higher. However, substances other than the above-described materials may also be used as long as the substances have higher hole-transport properties than electron-transport properties. These

materials used for the charge generation layer **1004** are excellent in carrier-injection property and carrier-transport property, and thus, a light-emitting element can be driven with low current.

Note that the charge generation layer **1004** may be formed in a combination of a composite material of an organic compound and metal oxide with another material. For example, a layer containing a composite material of the organic compound and the metal oxide may be combined with a layer containing a compound of a substance selected from substances having an electron-donating property and a compound having a high electron-transport property. Moreover, a layer containing a composite material of the organic compound and the metal oxide may be combined with a transparent conductive film

As for a light-emitting element having such a structure, problems such as energy transfer and quenching are unlikely to occur, and a light-emitting element which has both high light emission efficiency and long lifetime can be easily obtained due to expansion in the choice of materials. In addition, a light-emitting element which provides phosphorescence from one of the EL layers and fluorescence from the other of the EL layers can be readily obtained.

Note that the charge generation layer **1004** has a function of injecting holes to one EL layer **1003** which is formed in contact with the charge generation layer **1004** and a function of injecting electrons to the other EL layer **1003** which is formed in contact with the charge generation layer **1004**, when voltage is applied to the first electrode **1001** and the second electrode **1002**.

The light-emitting element shown in FIG. **21**B can provide a variety of emission colors by changing the type of the light-emitting substance that is used for the light-emitting layer. In addition, a plurality of light-emitting substances of different emission colors are used as the light-emitting substance, whereby light emission having a broad spectrum or white light emission can also be obtained.

In the case of obtaining white color light using the light-emitting element shown in FIG. **21**B, as for the combination of a plurality of light-emitting layers, a structure for emitting white light including red light, blue light, and green light may be used. For example, the structure may include a first EL layer containing a blue fluorescent substance as a light-emitting substance and a second EL layer containing green and red phosphorescent substances as light-emitting substances. Alternatively, the structure may include a first EL layer exhibiting red light emission, a second EL layer exhibiting green light emission, and a third EL layer exhibiting blue light emission. Further alternatively, with a structure including light-emitting layers emitting light of complementary colors, white light emission can be obtained. When light emission from the first EL layer and light emission from the second EL layer have complementary colors to each other in an element including two EL layers stacked, the combination of colors are as follows: blue and yellow, blue-green and red, and the like.

Note that in the structure of the above-described stacked element, by providing the charge generation layer between the stacked EL layers, the element can have long lifetime in a high luminance region while keeping the current density low. In addition, the voltage drop due to resistance of the electrode material can be reduced, whereby uniform light emission in a large area is possible.

This embodiment can be implemented in appropriate combination with any of the structures described in Embodiments 1 to 7.

Embodiment 9

In this embodiment, the appearance and a cross section of a light-emitting display panel (also referred to as a light-emitting panel) will be described with reference to FIGS. **22**A and **22**B. FIG. **22**A is a plan view of a panel in which a thin film transistor and a light-emitting element which are formed over a first flexible substrate are sealed between the first flexible substrate and a second flexible substrate with a sealant. FIG. **22**B is a cross-sectional view taken along line H-I in FIG. **22**A.

A sealant **4505** is provided so as to surround a pixel portion **4502**, signal line driving circuits **4503***a* and **4503***b*, and scan line driving circuits **4504***a* and **4504***b* which are provided over a first flexible substrate **4501**. In addition, a second flexible substrate **4506** is provided over the pixel portion **4502**, the signal line driving circuits **4503***a* and **4503***b*, and the scan line driving circuits **4504***a* and **4504***b*. Accordingly, the pixel portion **4502**, the signal line driving circuits **4503***a* and **4503***b*, and the scan line driving circuits **4504***a* and **4504***b* are sealed together with a filler **4507**, by the first flexible substrate **4501**, the sealant **4505**, and the second flexible substrate **4506**. It is preferable that a panel be packaged (sealed) with a protective film (such as a bonding film or an ultraviolet curable resin film) or a cover material with high air-tightness and little degasification so that the panel is not exposed to the outside air.

The pixel portion **4502**, the signal line driving circuits **4503***a* and **4503***b*, and the scan line driving circuits **4504***a* and **4504***b* formed over the first flexible substrate **4501** each include a plurality of thin film transistors. A thin film transistor **4510** included in the pixel portion **4502** and a thin film transistor **4509** included in the signal line driving circuit **4503***a* are shown as an example in FIG. **22**B.

Any of the highly reliable thin film transistors including the oxide semiconductor layers, which are described in Embodiments 1 to 5, can be used as the thin film transistors **4509** and **4510**. As the thin film transistor **4509** for the driving circuit, any of the thin film transistors **180**, **181**, and **182** which are described in Embodiments 1 to 5 can be used. As the thin film transistor **4510** for the pixel, any of the thin film transistors **170**, **171**, and **172** which are described in Embodiments 1 to 5 can be used. In this embodiment, the thin film transistors **4509** and **4510** are n-channel thin film transistors.

A conductive layer **4540** is provided over an insulating layer **4544** so as to overlap with a channel formation region in an oxide semiconductor layer of the thin film transistor **4509** for the driving circuit. By forming the conductive layer **4540** so as to overlap with the channel formation region of the oxide semiconductor layer, the amount of change in the threshold voltage of the thin film transistor **4509** before and after BT test can be reduced. Further, a potential of the conductive layer **4540** may be the same as or different from that of the gate electrode layer of the thin film transistor **4509**. The conductive layer **4540** can function also as a second gate electrode layer. Furthermore, the potential of the conductive layer **4540** may be GND or 0 V, or the conductive layer **4540** may be in a floating state.

Although not illustrated, a protective insulating layer such as the protective insulating layer **106** shown in Embodiment 1 may be provided between an oxide insulating layer **4542** and the insulating layer **4544**.

The thin film transistor **4510** is electrically connected to a first electrode layer **4517**.

The oxide insulating layer **4542** may be formed using a material and method similar to those of the oxide insulating film **107** shown in Embodiment 1.

A color filter layer **4545** is formed over the oxide insulating layer **4542** so as to overlap with a light-emitting region of a light-emitting element **4511**.

In addition, in order to reduce the surface roughness of the color filter layer **4545**, the color filter layer **4545** is covered with an overcoat layer **4543** functioning as a planarizing insulating film.

Further, an insulating layer **4544** is formed over the overcoat layer **4543**. The insulating layer **4544** may be formed using a material and similar to those of the protective insulating layer **109** shown in Embodiment 1.

Reference numeral **4511** denotes a light-emitting element. The first electrode layer **4517** which is a pixel electrode included in the light-emitting element **4511** is electrically connected to a source or drain electrode layer of the thin film transistor **4510**. Note that although the light-emitting element **4511** has a stacked structure of the first electrode layer **4517**, an electroluminescent layer **4512**, and a second electrode layer **4513**, the structure of the light-emitting element **4511** is not limited to the structure described in this embodiment. The structure of the light-emitting element **4511** can be changed as appropriate depending on the direction in which light is extracted from the light-emitting element **4511**, or the like.

A partition **4520** is formed using an organic resin film, an inorganic insulating film, or organic polysiloxane. It is particularly preferable that the partition **4520** be formed using a photosensitive material and an opening be formed over the first electrode layer **4517** so that a sidewall of the opening is formed as a tilted surface with continuous curvature.

The electroluminescent layer **4512** may be formed with a single-layer or a plurality of layers stacked.

A protective film may be formed over the second electrode layer **4513** and the partition **4520** in order to prevent entry of oxygen, hydrogen, moisture, carbon dioxide, or the like into the light-emitting element **4511**. As the protective film, a silicon nitride film, a silicon nitride oxide film, a DLC film, or the like can be formed.

In addition, a variety of signals and potentials are supplied to the signal line driving circuits **4503***a* and **4503***b*, the scan line driving circuits **4504***a* and **4504***b*, or the pixel portion **4502** from FPCs **4518***a* and **4518***b*.

A connection terminal electrode **4515** is formed from the same conductive film as the first electrode layer **4517** included in the light-emitting element **4511**, and a terminal electrode **4516** is formed from the same conductive film as the source and drain electrode layers included in the thin film transistor **4509**.

The connection terminal electrode **4515** is electrically connected to a terminal included in the FPC **4518***a* through an anisotropic conductive film **4519**.

The second flexible substrate located in the direction in which light is extracted from the light-emitting element **4511** needs to have a light-transmitting property. In that case, a light-transmitting material such as a plastic plate, a polyester film, or an acrylic film is used for the second flexible substrate.

Further, as the filler **4507**, an ultraviolet curable resin or a thermosetting resin can be used, in addition to an inert gas such as nitrogen or argon. For example, PVC (polyvinyl chloride), acrylic, polyimide, an epoxy resin, a silicone resin, PVB (polyvinyl butyral), or EVA (ethylene vinyl acetate) can be used. For example, nitrogen is used for the filler.

Furthermore, if needed, an optical film such as a polarizing plate, a circularly polarizing plate (including an elliptically polarizing plate), a retardation plate (a quarter-wave plate or a half-wave plate), or a color filter may be provided as appropriate on a light-emitting surface of the light-emitting element. Further, the polarizing plate or the circularly polarizing plate may be provided with an anti-reflection film. For example, anti-glare treatment may be performed by which reflected light can be diffused by surface roughness so that the glare can be reduced.

The signal line driving circuits **4503***a* and **4503***b* and the scan line driving circuits **4504***a* and **4504***b* may be mounted as driving circuits formed using a single crystal semiconductor film or a polycrystalline semiconductor film over a flexible substrate separately prepared. Alternatively, only the signal line driving circuits or part thereof, or the scan line driving circuits or part thereof may be separately formed and mounted. This embodiment is not limited to the structure shown in FIGS. **22**A and **22**B.

Through the above steps, a highly reliable light-emitting device (display panel) as a semiconductor device can be manufactured.

Embodiment 10

In this embodiment, an example is described below in which at least some of driving circuits and a thin film transistor provided in a pixel portion are formed over one flexible substrate.

The thin film transistor provided in the pixel portion is formed in accordance with Embodiments 1 to 5. The thin film transistors described in Embodiments 1 to 5 are n-channel TFTs; therefore, some of driving circuits which can be formed using n-channel TFTs are formed over one flexible substrate as the thin film transistor of the pixel portion.

FIG. **12**A shows an example of a block diagram of an active matrix display device. The display device includes a pixel portion **5301**, a first scan line driving circuit **5302**, a second scan line driving circuit **5303**, and a signal line driving circuit **5304** over a flexible substrate **5300**. In the pixel portion **5301**, a plurality of signal lines which are extended from the signal line driving circuit **5304** and a plurality of scan lines which are extended from the first scan line driving circuit **5302** and the second scan line driving circuit **5303** are arranged. Note that pixels which include display elements are arranged in matrix in regions where the scan lines and the signal lines are crossed. In addition, the flexible substrate **5300** of the display device is connected to a timing control circuit **5305** (also referred to as a controller or a control IC) through a connection portion such as a flexible printed circuit (FPC).

In FIG. **12**A, the first scan line driving circuit **5302**, the second scan line driving circuit **5303**, and the signal line driving circuit **5304** are formed over one flexible substrate **5300** as the pixel portion **5301**. Therefore, the number of components of a driving circuit which is provided outside and the like is reduced, which leads to cost reduction. Further, if the driving circuit is provided outside the flexible substrate **5300**, wirings would need to be extended and the number of connections of wirings would be increased, but by providing the driving circuit over the flexible substrate **5300**, the number of connections of the wirings can be reduced. Accordingly, improvement in reliability and yield can be achieved.

Note that the timing control circuit **5305** supplies, for example, a first scan line driving circuit start signal (GSP**1**) and a scan line driving circuit clock signal (GCK**1**) to the first scan line driving circuit **5302**. The timing control circuit **5305** supplies, for example, a second scan line driving circuit start signal (GSP**2**, also referred to as a start pulse) and a scan line driving circuit clock signal (GCK**2**) to the second scan line driving circuit **5303**. The timing control circuit **5305** supplies a signal line driving circuit start signal (SSP), a signal line driving circuit clock signal (SCLK), video signal data (DATA, also simply referred to as a video signal), and a latch signal (LAT) to the signal line driving circuit **5304**. Note that each clock signal may be a plurality of clock signals whose phases are shifted or may be supplied together with an inverted clock signal (CKB) obtained by inverting the clock signal. Note that one of the first scan line driving circuit **5302** and the second scan line driving circuit **5303** can be eliminated.

FIG. **12**B shows a structure in which circuits with low driving frequency (e.g., the first scan line driving circuit **5302** and the second scan line driving circuit **5303**) are formed over the same flexible substrate **5300** as the pixel portion **5301** and the signal line driving circuit **5304** is formed over a substrate which is different from the pixel portion **5301**. With this structure, a driving circuit formed over the flexible substrate **5300** can be formed using a thin film transistor with lower field effect mobility as compared to that of a transistor formed using a single crystal semiconductor. Thus, increase in size of the display device, reduction in cost, improvement in yield, or the like can be achieved.

In addition, the thin film transistors described in Embodiments 1 to 5 are n-channel TFTs. FIGS. **13**A and **13**B show an example of a structure and operation of a signal line driving circuit which is formed using n-channel TFTs.

The signal line driving circuit includes a shift register **5601** and a switching circuit **5602**. The switching circuit **5602** includes a plurality of switching circuits **5602_1** to **5602**_N (N is a natural number). The switching circuits **5602_1** to **5602**_N each include a plurality of thin film transistors **5603_1** to **5603**_*k* (k is a natural number). An example where the thin film transistors **5603_1** to **5603**_*k* are n-channel TFTs is described.

A connection relation in the signal line driving circuit is described taking the switching circuit **5602_1** as an example. First terminals of the thin film transistors **5603_1** to **5603**_*k* are connected to wirings **5604_1** to **5604**_*k*, respectively. Second terminals of the thin film transistors **5603_1** to **5603**_*k* are connected to signal lines S**1** to Sk, respectively. Gates of the thin film transistors **5603_1** to **5603**_*k* are connected to a wiring **5605_1**.

The shift register **5601** has a function of sequentially outputting H-level signals (also referred to as H signals or signals at high power supply potential level) to the wirings **5605_1** to **5605**_N and sequentially selecting the switching circuits **5602_1** to **5602**_N.

The switching circuit **5602_1** has a function of controlling a conducting state between the wirings **5604_1** to **5604**_*k* and the signal lines S**1** to Sk (electrical continuity between the first terminals and the second terminals), that is, a function of controlling whether potentials of the wirings **5604_1** to **5604**_*k* are supplied to the signal lines S**1** to Sk. In this manner, the switching circuit **5602_1** functions as a selector. Further, the thin film transistors **5603_1** to **5603**_*k* each have functions of controlling conduction states between the wirings **5604_1** to **5604**_*k* and the signal lines S**1** to Sk, that is, functions of supplying the potentials of the wirings **5604_1** to **5604**_*k* to the signal lines S**1** to Sk. In this manner, each of the thin film transistors **5603_1** to **5603**_*k* functions as a switch.

Note that video signal data (DATA) is input to each of the wirings **5604_1** to **5604**_*k*. The video signal data (DATA) is an analog signal corresponding to an image data or image signal in many cases.

Next, operation of the signal line driving circuit in FIG. **13**A is described with reference to a timing chart in FIG. **13**B. FIG. **13**B shows examples of signals Sout_**1** to Sout_N and signals Vdata_**1** to Vdata_*k*. The signals Sout_**1** to Sout_N are examples of output signals from the shift register **5601**. The signals Vdata_**1** to Vdata_*k* are examples of signals input to the wirings **5604_1** to **5604**_*k*. Note that one operation period of the signal line driving circuit corresponds to one gate selection period in a display device. For example, one gate selection period is divided into periods T**1** to TN. Each of the periods T**1** to TN is a period during which the video signal data (DATA) is written to pixels in a selected row.

Note that as for structures shown in drawings and the like of this embodiment, distortion in signal waveforms and the like are exaggerated for simplicity in some cases. Thus, the scale is not necessarily limited to that illustrated.

In the periods T**1** to TN, the shift register **5601** sequentially outputs H-level signals to the wirings **5605_1** to **5605**_N. For example, in the period T**1**, the shift register **5601** outputs the H-level signal to the wiring **5605_1**. Then, the thin film transistors **5603_1** to **5603**_*k* are turned on, so that the wirings **5604_1** to **5604**_*k* and the signal lines S**1** to Sk are brought into conducting state. In this case, Data (S**1**) to Data (Sk) are input to the wirings **5604_1** to **5604**_*k*, respectively. The Data (S**1**) to Data (Sk) are written to pixels in a selected row in first to k-th columns through the thin film transistors **5603_1** to **5603**_*k*, respectively. Thus, in the periods T**1** to TN, video signal data (DATA) is sequentially written to the pixels in the selected row by k columns.

By writing video signal data (DATA) to pixels by a plurality of columns as described above, the number of video signal data (DATA) or the number of wirings can be reduced. Accordingly, the number of connections to an external circuit can be reduced. In addition, by writing video signals to pixels by a plurality of columns, writing time can be extended and insufficient writing of video signals can be prevented.

Note that as the shift register **5601** and the switching circuit **5602**, a circuit including the thin film transistor described in any of Embodiments 1 to 5 can be used. In that case, the shift register **5601** can be constituted by only n-channel transistors or only p-channel transistors.

The structure of a scan line driving circuit will be described. The scan line driving circuit includes a shift register. The scan line driving circuit may also include a level shifter, a buffer, or the like in some cases. In the scan line driving circuit, a clock signal (CLK) and a start pulse signal (SP) are input to the shift register, whereby a selection signal is generated. The generated selection signal is buffered and amplified in the buffer, and the resulting signal is supplied to a corresponding scan line. Gate electrodes of transistors in pixels of one line are connected to a scan line. Since the transistors in the pixels of one line must be turned on all at once, a buffer which can supply a large amount of current is used.

One embodiment of a shift register which is used for a part of the scan line driving circuit and/or the signal line driving circuit is described with reference to FIGS. **14**A to **14**D and FIGS. **15**A and **15**B.

A shift register of a scan line driving circuit and/or a signal line driving circuit is described with reference to FIGS. **14**A to **14**D and FIGS. **15**A and **15**B. The shift register includes first to N-th pulse output circuits **10_1** to **10**_N (N is a natural number of 3 or more) (see FIG. **14**A). A first clock signal CK**1** from a first wiring **11**, a second clock signal CK**2** from a second wiring **12**, a third clock signal CK**3** from a third wiring **13**, and a fourth clock signal CK**4** from a fourth wiring **14** are supplied in the first to N-th pulse output circuits **10_1** to **10**_N of the shift register shown in FIG. **14**A. In addition, a start pulse SP**1** (a first start pulse) from a fifth wiring **15** is input to the first pulse output circuit **10_1**. Further, a signal from the pulse output circuit **10**__(n−1) of the previous stage (referred to as a previous stage signal OUT (n−1)) is input to the n-th pulse output circuit **10**_*n* (n is a natural number of 2 or more and N or less) in a second or subsequent stage. A signal from the third pulse output circuit **10_3** which is two stages after the first pulse output circuit **10_1** is input to the first pulse output circuit **10_1**. Similarly, a signal from the (n+2)-th pulse output circuit **10**__ (n+2) which is two stages after the n-th pulse output circuit **10**_*n* (referred to as a subsequent stage signal OUT (n+2)) is input to the n-th pulse output circuit **10**_*n* in the second or subsequent stage. Therefore, the pulse output circuits in respective stages output first output signals (OUT (**1**) (SR) to OUT (N) (SR)) which is input to the pulse output circuit in the subsequent stage and/or the pulse output circuit of the stage before the preceding stage. Furthermore, the pulse output circuits in respective stages output second output signals (OUT (**1**) to OUT (N)) which are electrically connected to another wiring or the like. Note that as shown in FIG. **14**A, since the subsequent stage signal OUT (n+2) is not input to the last two stages of the shift register, a second start pulse SP**2** and a third start pulse SP**3** may be separately input to the last two stages of the shift register, for example.

Note that a clock signal (CK) is a signal which oscillates between an H-level signal and an L-level signal (also referred to as L signal or a signal at a low power supply potential level) at regular intervals. Here, the first to fourth clock signals CK**1** to CK**4** are delayed by ¼ cycle sequentially. In this embodiment, by using the first to fourth clock signals CK**1** to CK**4**, control or the like of driving of the pulse output circuits is performed. The clock signal is also referred to as GCK or SCK in accordance with a driving circuit to which the signal is input; however, here, description is made using CK as the clock signal.

A first input terminal **21**, a second input terminal **22**, and a third input terminal **23** are electrically connected to any of the first to fourth wirings **11** to **14**. For example, in FIG. **14**A, the first input terminal **21** of the first pulse output circuit **10_1** is electrically connected to the first wiring **11**, the second input terminal **22** of the first pulse output circuit **10_1** is electrically connected to the second wiring **12**, and the third input terminal **23** of the first pulse output circuit **10_1** is electrically connected to the third wiring **13**. In addition, the first input terminal **21** of the second pulse output circuit **10_2** is electrically connected to the second wiring **12**, the second input terminal **22** of the second pulse output circuit **10_2** is electrically connected to the third wiring **13**, and the third input terminal **23** of the second pulse output circuit **10_2** is electrically connected to the fourth wiring **14**.

Each of the first to N-th pulse output circuits **10_1** to **110**_N includes the first input terminal **21**, the second input terminal **22**, the third input terminal **23**, a fourth input terminal **24**, a fifth input terminal **25**, a first output terminal **26**, and a second output terminal **27** (see FIG. **14**B). In the first pulse output circuit **10_1**, the first clock signal CK**1** is input to the first input terminal **21**; the second clock signal CK**2** is input to the second input terminal **22**; the third clock signal CK**3** is input to the third input terminal **23**; the start pulse is input to the fourth input terminal **24**; the subsequent stage signal OUT (**3**) is input to the fifth input terminal **25**; the first output signal OUT (**1**) (SR) is output from the first output terminal **26**; and the second output signal OUT (**1**) is output from the second output terminal **27**.

In addition to a thin film transistor (TFT) having three terminals, the thin film transistor having four terminals, which is described in the above embodiment, can be used for each of the first to N-th pulse output circuits **10_1** to **10**_N. FIG. **14**C shows the symbol of a thin film transistor **28** having four terminals, which is described in the above embodiment. The thin film transistor **28** in FIG. **14**C corresponds to the thin film transistor having four terminals described in any of Embodiments 1 to 5, and the symbols are used for description below. Note that in this specification, when a thin film transistor has two gate electrodes with a semiconductor layer therebetween, the gate electrode below the semiconductor layer is referred to as a lower gate electrode and the gate electrode above the semiconductor layer is referred to as an upper gate electrode. The thin film transistor **28** is an element that can perform electric control between an IN terminal and an OUT terminal with a first control signal G**1** input to the lower gate electrode and a second control signal G**2** input to the upper gate electrode.

When an oxide semiconductor is used for a semiconductor layer including a channel formation region of a thin film transistor, threshold voltage is shifted in a negative or positive direction in some cases depending on a manufacturing process. Thus, a thin film transistor in which an oxide semiconductor is used for a semiconductor layer including a channel formation region preferably has a structure where threshold voltage can be controlled. The threshold voltage of the thin film transistor **28** shown in FIG. **14**C can be controlled to a desired value in the following manner: a gate electrode is provided on the upper and the lower sides of the channel formation region of the thin film transistor **28** with a gate insulating layer interposed therebetween, and the potential of the gate electrode on the upper and/or lower sides is controlled.

Next, an example of a specific circuit structure of the pulse output circuits is described with reference to FIG. **14**D.

The first pulse output circuit **10_1** has first to thirteenth transistors **31** to **43** (see FIG. **14**D). In addition to the first to fifth input terminals **21** to **25**, the first output terminal **26**, and the second output terminal **27**, signals or power supply potentials are supplied to the first to thirteenth transistors **31** to **43** from a power supply line **51** to which a first high power supply potential VDD is supplied, a power supply line **52** to which a second high power supply potential VCC is supplied, and a power supply line **53** to which a low power supply potential VSS is supplied. Here, a potential relationship of each of the power supply lines in FIG. **14**D is as follows: the first power supply potential VDD is higher than or equal to the second power supply potential VCC, and the second power supply potential VCC is higher than or equal to the third power supply potential VSS. Although the first to fourth clock signals CK**1** to CK**4** are signals which oscillate between an H-level signal and an L-level signal at regular intervals, a potential is VDD when the clock signal is at the H-level, and the potential is VSS when the clock signal is at the L-level. By setting the potential VDD of the power supply line **51** higher than the potential VCC of the

power supply line **52**, a potential applied to the gate electrode of the transistor can be lowered without adversely affecting the operation; thus, the shift of the threshold voltage of the transistor can be reduced and deterioration can be suppressed. Note that as shown in FIG. **14**D, the thin film transistor **28** having four terminals shown in FIG. **14**C is preferably used for the first transistor **31** and the sixth to ninth transistors **36** to **39** among the first to thirteenth transistors **31** to **43**. The first transistor **31** and the sixth to ninth transistors **36** to **39** are required to switch a potential of each node connected to one of electrodes which is to be a source or a drain by a control signal of the gate electrode. The first transistor **31** and the sixth to ninth transistors **36** to **39** can further reduce malfunctions of the pulse output circuits by quick response (sharp rising of on current) with respect to a control signal input to the gate electrode. Therefore, when a thin film transistor **28** having four terminals illustrated in FIG. **14**C is used, the threshold voltage can be controlled and malfunctions of the pulse output circuits can be further reduced. Note that in FIG. **14**D, the first control signal G**1** is the same control signal as the second control signal G**2**; however, the first control signal G**1** and the second control signal G**2** may be different from each other.

In FIG. **14**D, a first terminal of the first transistor **31** is electrically connected to the power supply line **51**, a second terminal of the first transistor **31** is electrically connected to a first terminal of the ninth transistor **39**, and gate electrodes (a lower gate electrode and an upper gate electrode) of the first transistor **31** are electrically connected to the fourth input terminal **24**. A first terminal of the second transistor **32** is electrically connected to the power supply line **53**, a second terminal of the second transistor **32** is electrically connected to the first terminal of the ninth transistor **39**, and a gate electrode of the second transistor **32** is electrically connected to a gate electrode of the fourth transistor **34**. A first terminal of the third transistor **33** is electrically connected to the first input terminal **21**, and a second terminal of the third transistor **33** is electrically connected to the first output terminal **26**. A first terminal of the fourth transistor **34** is electrically connected to the power supply line **53**, and a second terminal of the fourth transistor **34** is electrically connected to the first output terminal **26**. A first terminal of the fifth transistor **35** is electrically connected to the power supply line **53**, a second terminal of the fifth transistor **35** is electrically connected to the gate electrode of the second transistor **32** and the gate electrode of the fourth transistor **34**, and a gate electrode of the fifth transistor **35** is electrically connected to the fourth input terminal **24**. A first terminal of the sixth transistor **36** is electrically connected to the power supply line **52**, a second terminal of the sixth transistor **36** is electrically connected to the gate electrode of the second transistor **32** and the gate electrode of the fourth transistor **34**, and gate electrodes (a lower gate electrode and an upper gate electrode) of the sixth transistor **36** are electrically connected to the fifth input terminal **25**. A first terminal of the seventh transistor **37** is electrically connected to the power supply line **52**, a second terminal of the seventh transistor **37** is electrically connected to a second terminal of the eighth transistor **38**, and gate electrodes (a lower gate electrode and an upper gate electrode) of the seventh transistor **37** are electrically connected to the third input terminal **23**. A first terminal of the eighth transistor **38** is electrically connected to the gate electrode of the second transistor **32** and the gate electrode of the fourth transistor **34**, and gate electrodes (a lower gate electrode and an upper gate electrode) of the eighth transistor **38** is electrically connected to the second input terminal **22**. The first terminal of the ninth transistor **39** is electrically connected to the second terminal of the first transistor **31** and the second terminal of the second transistor **32**, a second terminal of the ninth transistor **39** is electrically connected to a gate electrode of the third transistor **33** and a gate electrode of the tenth transistor **40**, and gate electrodes (a lower gate electrode and an upper gate electrode) of the ninth transistor **39** are electrically connected to the power supply line **52**. A first terminal of the tenth transistor **40** is electrically connected to the first input terminal **21**, a second terminal of the tenth transistor **40** is electrically connected to the second output terminal **27**, and the gate electrode of the tenth transistor **40** is electrically connected to the second terminal of the ninth transistor **39**. A first terminal of the eleventh transistor **41** is electrically connected to the power supply line **53**, a second terminal of the eleventh transistor **41** is electrically connected to the second output terminal **27**, and a gate electrode of the eleventh transistor **41** is electrically connected to the gate electrode of the second transistor **32** and the gate electrode of the fourth transistor **34**. A first terminal of the twelfth transistor **42** is electrically connected to the power supply line **53**, a second terminal of the twelfth transistor **42** is electrically connected to the second output terminal **27**, and a gate electrode of the twelfth transistor **42** is electrically connected to the gate electrodes (the lower gate electrode and the upper gate electrode) of the seventh transistor **37**. A first terminal of the thirteenth transistor **43** is electrically connected to the power supply line **53**, a second terminal of the thirteenth transistor **43** is electrically connected to the first output terminal **26**, and a gate electrode of the thirteenth transistor **43** is electrically connected to the gate electrodes (the lower gate electrode and the upper gate electrode) of the seventh transistor **37**.

In FIG. **14**D, a connection point of the gate electrode of the third transistor **33**, the gate electrode of the tenth transistor **40**, and the second terminal of the ninth transistor **39** is referred to as a node A. In addition, a connection point of the gate electrode of the second transistor **32**, the gate electrode of the fourth transistor **34**, the second terminal of the fifth transistor **35**, the second terminal of the sixth transistor **36**, the first terminal of the eighth transistor **38**, and the gate electrode of the eleventh transistor **41** is referred to as a node B (see, FIG. **15**A).

Note that the thin film transistor is an element which includes at least three terminals: gate, drain, and source electrodes. A channel formation region is provided between the drain region and the source region and current can flow through the drain region, the channel region, and the source region. Here, since the source and the drain of the thin film transistor may change depending on the structure, the operating condition, and the like of the thin film transistor, it is difficult to define which is a source or a drain. Therefore, a region functioning as a source or a drain is not called a source or a drain in some cases. In such a case, for example, one of the source and the drain may be referred to as a first terminal and the other thereof may be referred to as a second terminal.

Note that in FIG. **14**D and FIG. **15**A, a capacitor for performing bootstrap operation by setting the node A floating may be additionally provided. Further, a capacitor having one electrode electrically connected to the node B may be additionally provided in order to hold a potential of the node B.

Here, FIG. **15**B shows a timing chart of a shift register including a plurality of the pulse output circuits shown in FIG. **15**A. Note that in the case where the shift register is a

scan line driving circuit, a period **61** of FIG. **15**B corresponds to a vertical retrace period and a period **62** of FIG. **15**B corresponds to a gate selection period.

Note that as shown in FIG. **15**A, with the ninth transistor **39** whose gate is supplied with the second power supply potential VCC, advantages described below are obtained before and after bootstrap operation.

Without the ninth transistor **39** whose gate is supplied with the second power supply potential VCC, when a potential of the node A is raised by bootstrap operation, a potential of a source which is the second terminal of the first thin film transistor **31** increases to a value higher than the first power supply potential VDD. Then, the first terminal of the first transistor **31**, that is, the terminal on the power supply line **51** side, comes to serve as a source of the first transistor **31**. Therefore, in the first transistor **31**, a high bias voltage is applied and thus significant stress is applied between the gate and the source and between the gate and the drain, which might cause deterioration in the transistor. Thus, with the ninth transistor **39** whose gate electrode is supplied with the second power supply potential VCC, the potential of the node A is raised by bootstrap operation, but at the same time, an increase in the potential of the second terminal of the first transistor **31** can be prevented. In other words, with the ninth transistor **39**, the level of a negative bias voltage applied between the gate and the source of the first transistor **31** can be lowered. Accordingly, with a circuit structure in this embodiment, a negative bias voltage applied between the gate and the source of the first transistor **31** can be lowered, so that deterioration in the first transistor **31**, which is due to stress, can be further restrained.

Note that the ninth transistor **39** is provided so that the first terminal and the second terminal of the ninth transistor **39** are connected between the second terminal of the first transistor **31** and the gate of the third transistor **33**. In the case where a shift register includes a plurality of pulse output circuits of this embodiment, the ninth transistor **39** may be eliminated in a signal line driving circuit which has more stages than a scan line driving circuit, which is advantageous in reducing the number of the transistors.

When an oxide semiconductor is used for each of the semiconductor layers of the first to thirteenth transistors **31** to **43**, the amount of off current of the thin film transistors can be reduced, the amount of on current and field-effect mobility can be increased, and the rate of deterioration can be decreased, whereby malfunctions of the circuit can be reduced. Further, a transistor including an oxide semiconductor has a lower rate of deterioration of the transistor due to application of a high potential to a gate electrode, as compared to a transistor including amorphous silicon. Therefore, even when the first power supply potential VDD is supplied to the power supply line to which the second power supply potential VCC is supplied, similar operation can be performed and the number of power supply lines provided between the circuits can be reduced, whereby size reduction in a circuit can be achieved.

Note that a similar effect is obtained even when a connection relation is changed so that a clock signal which is supplied to the gate electrodes (the lower gate electrode and the upper gate electrode) of the seventh transistor **37** through the third input terminal **23** is a clock signal which is supplied to the gate electrodes (the lower gate electrode and the upper electrode) of the seventh transistor **37** through the second input terminal **22**; and a clock signal which is supplied to the gate electrodes (the lower gate electrode and the upper gate electrode) of the eighth transistor **38** through the second input terminal **22** is a clock signal which is supplied to the gate electrodes (the lower electrode and the upper electrode) of the eighth transistor **38** through the third input terminal **23**. Note that in the shift register shown in FIG. **15**A, the seventh transistor **37** and the eighth transistor **38** are both in an on state, the seventh transistor **37** is turned off and the eighth transistor **38** is kept on, and then the seventh transistor **37** kept off and the eighth transistor **38** is turned off, whereby the decrease in the potential of the node B, which is caused by the decrease in the potentials of the second input terminal **22** and the third input terminal **23**, occurs twice due to the decrease in the potential of the gate electrode of the seventh transistor **37** and the decrease in the potential of the gate electrode of the eighth transistor **38**. On the other hand, in the shift register shown in FIG. **15**A, the seventh transistor **37** and the eighth transistor **38** are both in an on state, the seventh transistor **37** is kept on and the eighth transistor **38** is turned off, and then the seventh transistor **37** is turned off and the eighth transistor **38** is kept off, whereby the decrease in the potential of the node B, which is caused by the decrease in the potentials of the second input terminal **22** and the third input terminal **23**, can be reduced to once due to the decrease in the potential of the gate electrode of the eighth transistor **38**. Accordingly, the connection relation, in which the clock signal CK**3** is supplied to the gate electrodes (the lower electrode and the upper electrode) of the seventh transistor **37** through the third input terminal **23** and the clock signal CK**2** is supplied to the gate electrodes (the lower gate electrode and the upper gate electrode) of the eighth transistor **38** through the second input terminal **22**, is preferable. That is because the number of times of fluctuation of the potential of the node B can be reduced and noise can be reduced.

In this manner, in a period during which the potential of the first output terminal **26** and the potential of the second output terminal **27** are held at the L level, an H level signal is regularly supplied to the node B; therefore, a malfunction of the pulse output circuit can be prevented.

Embodiment 11

A light-emitting device disclosed in this specification can be applied to a variety of electronic devices (including an amusement machine). Examples of electronic devices are a television device (also referred to as a television or a television receiver), a monitor of a computer or the like, a camera such as a digital camera or a digital video camera, a digital photo frame, a mobile phone handset (also referred to as a mobile phone or a mobile phone device), a portable game console, a portable information terminal, an audio reproducing device, a large sized game machine such as a pachinko machine, and the like.

In this embodiment, an example of a mobile phone using the flexible light-emitting device formed according to any of the above embodiments is shown in FIGS. **23**A to **23**D and FIG. **24**.

FIG. **23**C is a front view of a mobile phone; FIG. **23**D, a side view; and FIG. **23**B, a top view. Housings of the mobile phone are a housing **1411***a* and a housing **1411***b*. A light-transmitting supporting member is used for at least of the housing **1411***a* and the housing **1411***b* which is to be a display region. FIG. **23**A is a cross-sectional view of the inside of the housing **1411***a* and the housing **1411***b*. The front of the housing **1411***a* has a rectangular shape with a longer side and a shorter side, which may have a round corner. In this embodiment, a direction parallel to the longer side of the rectangle that is the shape of the front is referred

to as a longitudinal direction and a direction parallel to the shorter side is referred to as a lateral direction.

In addition, the sides of the housing **1411***a* and the housing **1411***b* also have a rectangular shape with a longer side and a shorter side, which may have a round corner. In this embodiment, a direction parallel to the longer sides of the rectangle that is the shape of the side is a longitudinal direction, and a direction parallel to the shorter sides is referred to as a depth direction.

The mobile phone shown in FIGS. **23**A to **23**D includes a display region **1413**, operating buttons **1404**, and a touch panel **1423**, and the housings **1411***a* and **1411***b* include a light-emitting panel **1421** and a wiring board **1425**. The touch panel **1423** may be provided as needed.

As the light-emitting panel **1421**, the light-emitting device (the light-emitting panel or the light-emitting module) described above in Embodiments 1 to 10 may be used.

As shown in FIGS. **23**B and **23**C, the light-emitting panel **1421** is arranged along the shape of the housing **1411***a* so as to cover not only the front region on the viewer side but also part of the top region and the bottom region. Therefore, a display region **1427** can be formed on the top of the mobile phone in the longitudinal direction to be connected to the display region **1413**. That is, the display region **1427** also exists on the top surface of the mobile phone. Accordingly, the display region **1427** can be seen without taking out the mobile phone from, for example, even if in the breast pocket.

On the display regions **1413** and **1427**, incoming mails or calls, dates, phone numbers, personal names, and the like may be displayed. Further, energy consumption can be saved by performing display only in the display region **1427** and not performing display in the other regions as needed.

FIG. **24** shows the cross-sectional view of FIG. **23**D. As shown in FIG. **24**, the light-emitting panel **1421** is continuously formed on the top, front, and bottom of the inside of the housing **1411***a*. A battery **1426** and the wiring board **1425** electrically connected to the light-emitting panel **1421** are arranged in the backside of the light-emitting panel **1421**. In addition, the touch panel **1423** is arranged in the outside of the housing **1411***a* (on the viewer side).

Images and letters can be displayed, whether the mobile phone of this embodiment is placed horizontally or vertically.

The light-emitting panel **1421** is not manufactured separately in the front region and the top region, but manufactured to cover both the front display region **1413** and the top display region **1427**, whereby manufacturing cost and time can be reduced.

The touch panel **1423** is arranged on the housing **1411***a*, and buttons **1414** of the touch panel are displayed on the display region **1413**. By touching the buttons **1414** with a finger or the like, contents displayed on the display region **1413** can be operated. Further, making calls or composing mails can also be performed by touching the buttons **1414** on the display region **1413** with a finger or the like.

The buttons **1414** on the touch panel **1423** may be displayed when needed, and when the buttons **1414** are unneeded, images or letters can be displayed on the entire display region **1413**.

Furthermore, the upper longer side in a cross section of the mobile phone may also have a radius of curvature. When the mobile phone is formed so that the cross section thereof has a radius of curvature in the upper longer side, the light-emitting panel **1421** and the touch panel **1423** also have a radius of curvature in an upper longer side in a cross section. In addition, the housing **1411***a* also has a curved shape. In other words, the display region **1413** on the front is curved outwards.

FIGS. **25**A and **25**B show an example of an electronic book reader using the flexible light-emitting device formed according to any of the above embodiments. FIG. **25**A shows an opened electronic book reader and FIG. **25**B shows a closed electronic book reader. The light-emitting device (the light-emitting panel) formed according to any of the above embodiments can be used for a first display panel **4311**, a second display panel **4312**, and a third display panel **4313**.

A first housing **4305** has the first display panel **4311** including a first display portion **4301**, a second housing **4306** has the second display panel **4312** including an operation portion **4304** and a second display portion **4307**. The third display panel **4313** is a dual display type panel and has a third display portion **4302** and a fourth display portion **4310**. The third display panel **4313** is interposed between the first display panel **4311** and the second display panel **4312**. The first housing **4305**, the first display panel **4311**, the third display panel **4313**, the second display panel **4312**, and the second housing **4306** are connected to each other with a binding portion **4308** in which a driving portion is formed. The electronic book reader of FIGS. **25**A and **25**B includes four display screens of the first display portion **4301**, the second display portion **4307**, the third display portion **4302**, and the fourth display portion **4310**.

The first housing **4305**, the first display panel **4311**, the third display panel **4313**, the second display panel **4312**, and the second housing **4306** are each flexible and has high flexibility. Further, when a plastic substrate is used for each of the first housing **4305** and the second housing **4306**, and a thin film is used for the third display panel **4313**, a thin electronic book reader can be obtained.

The third display panel **4313** is a dual display type panel including the third display portion **4302** and the fourth display portion **4310**. For the third display panel **4313**, a display panel of a dual emission type may be used, or display panels of a one-side emission type may be bonded.

FIG. **26** is an example in which the light-emitting device formed according to any of the above embodiments is used as an indoor lighting device **3001**. Since the light-emitting device shown in the above embodiments can be increased in area, the light-emitting device can be used as a lighting device having a large area. Further, the light-emitting device shown in the above embodiments can be used as a desk lamp **3000**. Note that the lighting equipment includes in its category, a ceiling light, a desk light, a wall light, a lighting for an inside of a car, an emergency exit light, and the like.

As described above, the light-emitting device shown in Embodiments 1 to 10 can be arranged in the display panels of the above various electronic devices; thus, an electronic device with high reliability can be provided.

This application is based on Japanese Patent Application serial no. 2009-215053 filed with Japan Patent Office on Sep. 16, 2009, the entire contents of which are hereby incorporated by reference.

The invention claimed is:

1. An electronic device comprising a display panel having a display region, and a housing incorporating the display panel,

wherein the display panel comprises a display element and a transistor electrically connected to the display element,

wherein the transistor is formed over a first insulating layer,

wherein the display panel includes a region where the display panel is bent,

wherein the display region overlaps with the region where the display panel is bent,

wherein the display panel comprises:

a flexible substrate;

a driving circuit portion over the flexible substrate, comprising:

the transistor comprising:

a gate over the flexible substrate;

a second insulating layer over the gate;

a semiconductor layer over the second insulating layer;

a source over the semiconductor layer;

a drain over the semiconductor layer;

a third insulating layer over the semiconductor layer, the source, and the drain, a part of the third insulating layer being in contact with a part of the semiconductor layer between the source and the drain; and

a conductive layer over the third insulating layer, the conductive layer overlapping with the gate and a channel region of the transistor, wherein the channel region is between the source and the drain; and

a terminal portion comprising:

a first electrode layer over the flexible substrate;

the second insulating layer over the first electrode layer, the second insulating layer including a first contact hole;

a second electrode layer over and in contact with the first electrode layer through the first contact hole;

the third insulating layer over the second electrode layer, the third insulating layer including a second contact hole; and

a third electrode layer over and in contact with the second electrode layer through the second contact hole,

wherein the first electrode layer is formed from a same layer as the gate,

wherein the second electrode layer is formed from a same layer as the source and the drain, and

wherein the third electrode layer is formed from a same layer as the conductive layer.

2. The electronic device according to claim **1**, wherein the transistor comprises a channel formation region which comprises an oxide semiconductor material.

3. The electronic device according to claim **1**, wherein the transistor comprises a channel formation region which comprises polycrystalline silicon.

4. The electronic device according to claim **1**, wherein the electronic device is a mobile phone.

5. The electronic device according to claim **1**, wherein the flexible substrate is a plastic substrate having a light-transmitting property.

6. The electronic device according to claim **1**, wherein the flexible substrate comprises a polyester resin, a polyacrylonitrile resin, a polyimide resin, a polymethyl methacrylate resin, a polycarbonate (PC) resin, a polyethersulfone (PES) resin, a polyamide resin, a cycloolefin resin, a polystyrene resin, a polyamide imide resin, or a polyvinylchloride resin.

7. The electronic device according to claim **1**, wherein the first insulating layer comprises at least one layer selected from the group consisting of a silicon oxide layer, a silicon nitride layer, a silicon oxide layer containing nitrogen, and a silicon nitride layer containing oxygen.

8. An electronic device comprising:

a housing;

a display panel comprising a transistor, wherein the display panel comprises a display region, the display region comprising a first region and a second region, the first region disposed at a front of the housing, and the second region disposed between the first region and an edge of the display panel,

wherein the transistor is formed over a first insulating layer;

wherein the display panel is bent at least in a region between the first region and the second region,

wherein the display region overlaps with the region where the display panel is bent,

wherein the display panel comprises:

a flexible substrate;

a driving circuit portion over the flexible substrate, comprising:

the transistor comprising:

a gate over the flexible substrate;

a second insulating layer over the gate;

a semiconductor layer over the second insulating layer;

a source over the semiconductor layer;

a drain over the semiconductor layer;

a third insulating layer over the semiconductor layer, the source, and the drain, a part of the third insulating layer being in contact with a part of the semiconductor layer between the source and the drain; and

a conductive layer over the third insulating layer, the conductive layer overlapping with the gate and a channel region of the transistor, wherein the channel region is between the source and the drain; and

a terminal portion comprising:

a first electrode layer over the flexible substrate;

the second insulating layer over the first electrode layer, the second insulating layer including a first contact hole;

a second electrode layer over and in contact with the first electrode layer through the first contact hole;

the third insulating layer over the second electrode layer, the third insulating layer including a second contact hole; and

a third electrode layer over and in contact with the second electrode layer through the second contact hole,

wherein the first electrode layer is formed from a same layer as the gate,

wherein the second electrode layer is formed from a same layer as the source and the drain, and

wherein the third electrode layer is formed from a same layer as the conductive layer.

9. The electronic device according to claim **8**, wherein the transistor comprises a channel formation region which comprises an oxide semiconductor material.

10. The electronic device according to claim **8**, wherein the transistor comprises a channel formation region which comprises polycrystalline silicon.

11. The electronic device according to claim **8**, wherein the electronic device is a mobile phone.

12. The electronic device according to claim **8**, wherein the flexible substrate is a plastic substrate having a light-transmitting property.

13. The electronic device according to claim **8**, wherein the flexible substrate comprises a polyester resin, a poly-

acrylonitrile resin, a polyimide resin, a polymethyl methacrylate resin, a polycarbonate (PC) resin, a polyethersulfone (PES) resin, a polyamide resin, a cycloolefin resin, a polystyrene resin, a polyamide imide resin, or a polyvinylchloride resin.

14. The electronic device according to claim **8**, wherein the first insulating layer comprises at least one layer selected from the group consisting of a silicon oxide layer, a silicon nitride layer, a silicon oxide layer containing nitrogen, and a silicon nitride layer containing oxygen.

15. An electronic device comprising:

a housing;

a display panel having a display region, wherein the display panel comprises a display element and a transistor electrically connected to the display element; and

a touch panel,

wherein the transistor is formed over a first insulating layer,

wherein the display panel includes a region where the display panel is bent,

wherein the display region and the touch panel overlap with the region where the display panel is bent,

wherein the display panel comprises:

a flexible substrate;

a driving circuit portion over the flexible substrate, comprising:

the transistor comprising:

a gate over the flexible substrate;

a second insulating layer over the gate;

a semiconductor layer over the second insulating layer;

a source over the semiconductor layer;

a drain over the semiconductor layer;

a third insulating layer over the semiconductor layer, the source, and the drain, a part of the third insulating layer being in contact with a part of the semiconductor layer between the source and the drain; and

a conductive layer over the third insulating layer, the conductive layer overlapping with the gate and a channel region of the transistor, wherein the channel region is between the source and the drain; and

a terminal portion comprising:

a first electrode layer over the flexible substrate;

the second insulating layer over the first electrode layer, the second insulating layer including a first contact hole;

a second electrode layer over and in contact with the first electrode layer through the first contact hole;

the third insulating layer over the second electrode layer, the third insulating layer including a second contact hole; and

a third electrode layer over and in contact with the second electrode layer through the second contact hole,

wherein the first electrode layer is formed from a same layer as the gate,

wherein the second electrode layer is formed from a same layer as the source and the drain, and

wherein the third electrode layer is formed from a same layer as the conductive layer.

16. The electronic device according to claim **15**, wherein the transistor comprises a channel formation region which comprises an oxide semiconductor material.

17. The electronic device according to claim **15**, wherein the transistor comprises a channel formation region which comprises polycrystalline silicon.

18. The electronic device according to claim **15**, wherein the electronic device is a mobile phone.

19. The electronic device according to claim **15**, wherein the flexible substrate is a plastic substrate having a light-transmitting property.

20. The electronic device according to claim **15**, wherein the flexible substrate comprises a polyester resin, a polyacrylonitrile resin, a polyimide resin, a polymethyl methacrylate resin, a polycarbonate (PC) resin, a polyethersulfone (PES) resin, a polyamide resin, a cycloolefin resin, a polystyrene resin, a polyamide imide resin, or a polyvinylchloride resin.

21. The electronic device according to claim **15**, wherein the first insulating layer comprises at least one layer selected from the group consisting of a silicon oxide layer, a silicon nitride layer, a silicon oxide layer containing nitrogen, and a silicon nitride layer containing oxygen.

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