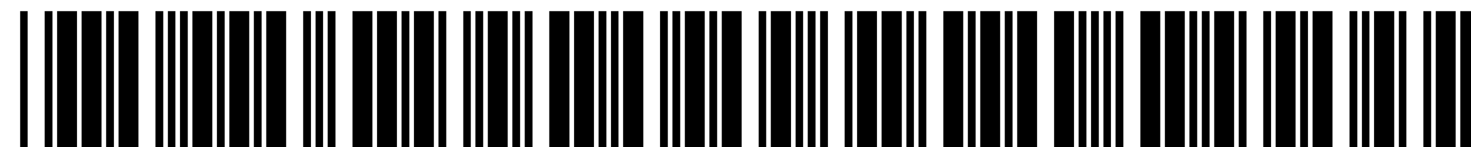

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(12) **United States Patent**
Shatalov et al.

(10) **Patent No.: US 10,297,460 B2**

(45) **Date of Patent: *May 21, 2019**

(54) **STRESS RELIEVING SEMICONDUCTOR LAYER**

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(73) Assignee: **Sensor Electronic Technology, Inc.**, Columbia, SC (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Apr. 25, 2017**

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US 2017/0229611 A1 Aug. 10, 2017

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(51) **Int. Cl.**
H01L 29/15 (2006.01)
H01L 31/0256 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 21/308*** (2013.01); ***H01L 21/0237*** (2013.01); ***H01L 21/0254*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 21/308; H01L 21/02505; H01L 21/0237; H01L 21/02458; H01L 29/2003;
(Continued)

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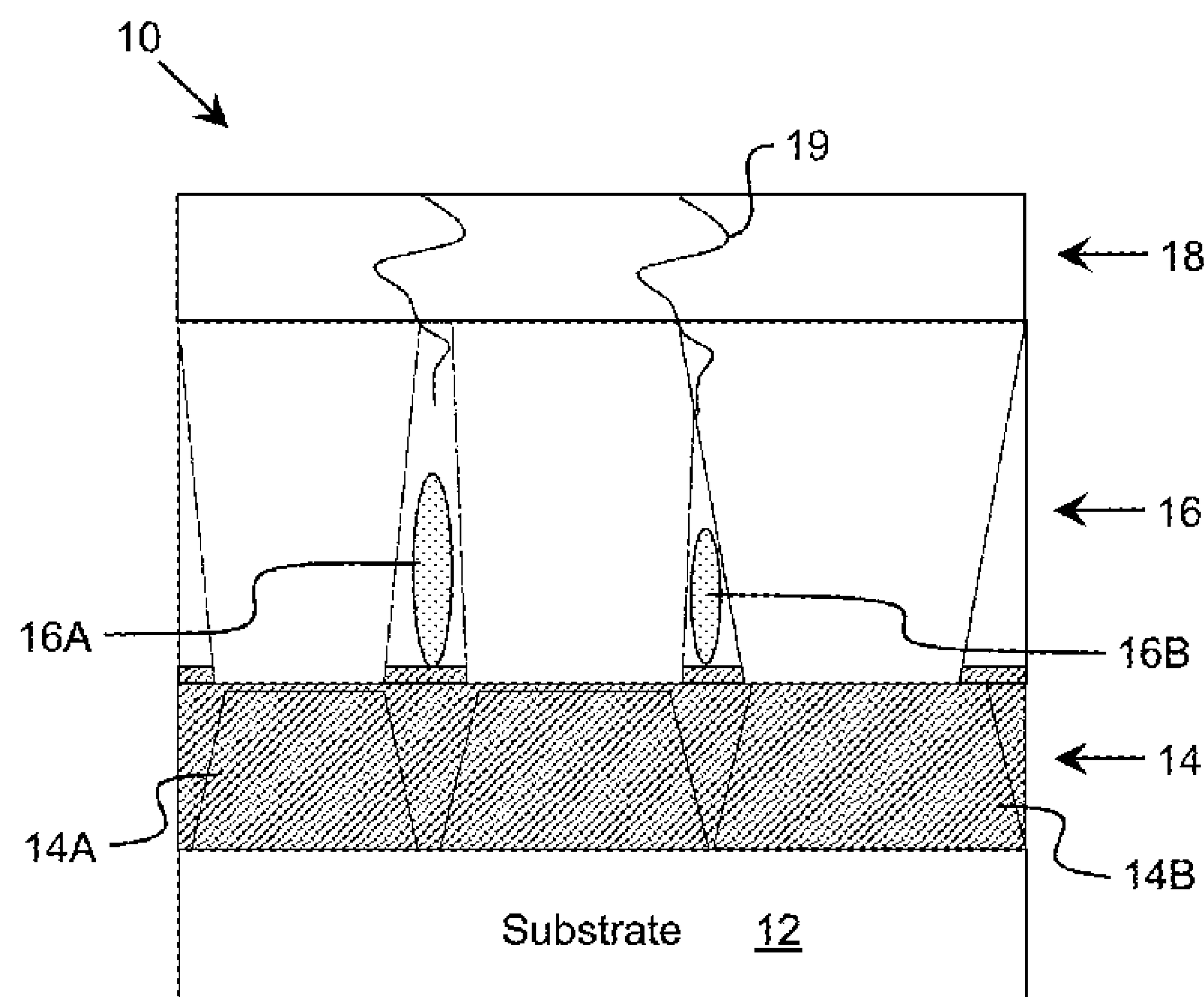
Primary Examiner — Victor A Mandala
(74) *Attorney, Agent, or Firm* — LaBatt, LLC

(57) **ABSTRACT**

A semiconductor structure, such as a group III nitride-based semiconductor structure is provided. The semiconductor structure includes a cavity containing semiconductor layer. The cavity containing semiconductor layer can have a thickness greater than two monolayers and a multiple cavities. The cavities can have a characteristic size of at least one nanometer and a characteristic separation of at least five nanometers.

20 Claims, 15 Drawing Sheets



Related U.S. Application Data

continuation-in-part of application No. 14/266,900, filed on May 1, 2014, now Pat. No. 9,330,906.

(60) Provisional application No. 61/817,970, filed on May 1, 2013.

(51) **Int. Cl.**

H01L 21/308	(2006.01)
H01L 29/66	(2006.01)
H01L 21/02	(2006.01)
H01L 33/12	(2010.01)
H01L 29/20	(2006.01)
H01L 33/00	(2010.01)

(52) **U.S. Cl.**

CPC .. ***H01L 21/02458*** (2013.01); ***H01L 21/02505*** (2013.01); ***H01L 29/158*** (2013.01); ***H01L 29/2003*** (2013.01); ***H01L 29/66075*** (2013.01); ***H01L 33/12*** (2013.01); *H01L 21/0265* (2013.01); *H01L 21/02639* (2013.01); *H01L 33/007* (2013.01)

(58) **Field of Classification Search**

CPC H01L 21/0254; H01L 29/158; H01L 29/66075; H01L 21/0265; H01L 21/02639; H01L 33/12; H01L 33/007

See application file for complete search history.

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FIG. 1

Prior Art

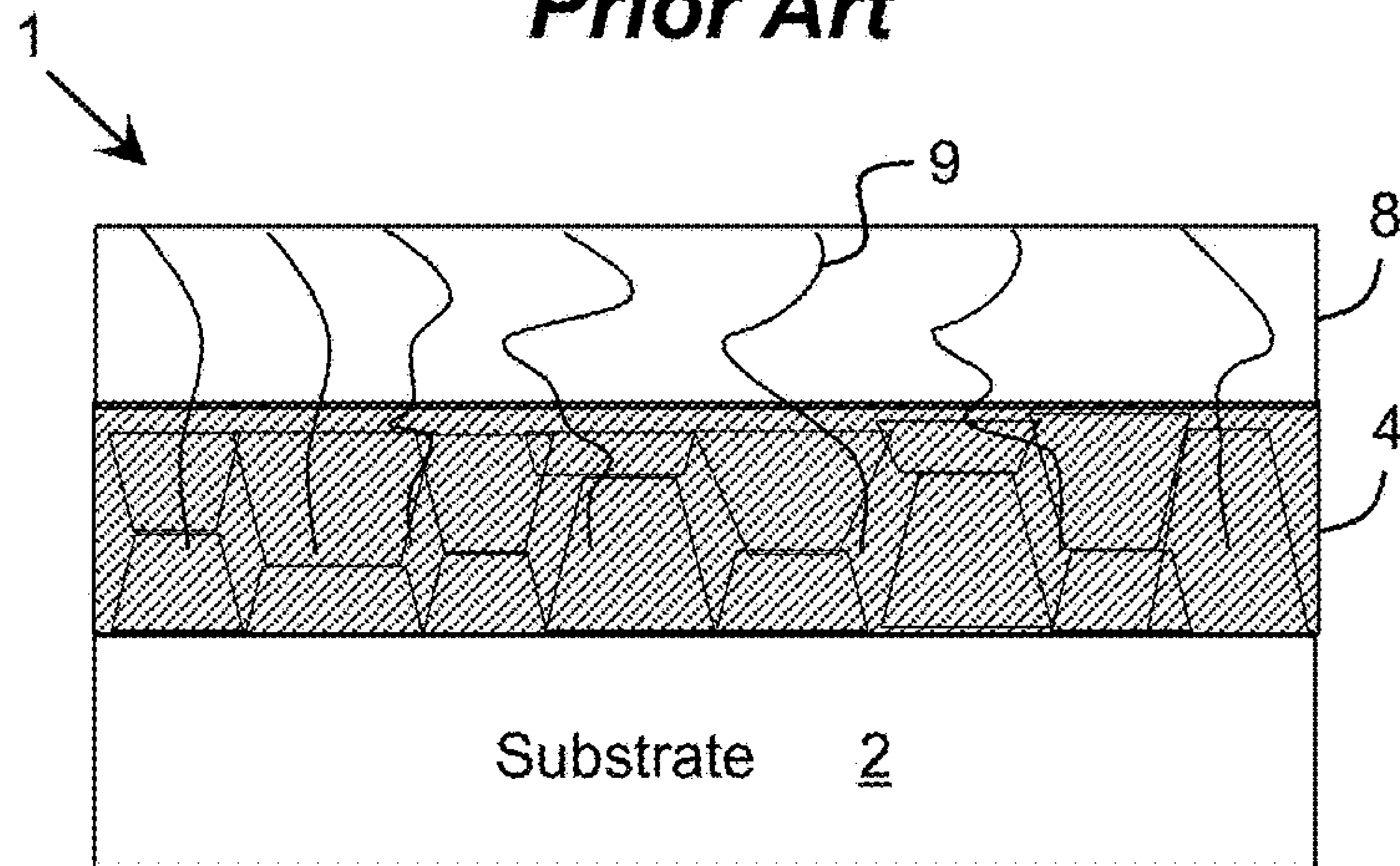


FIG. 2

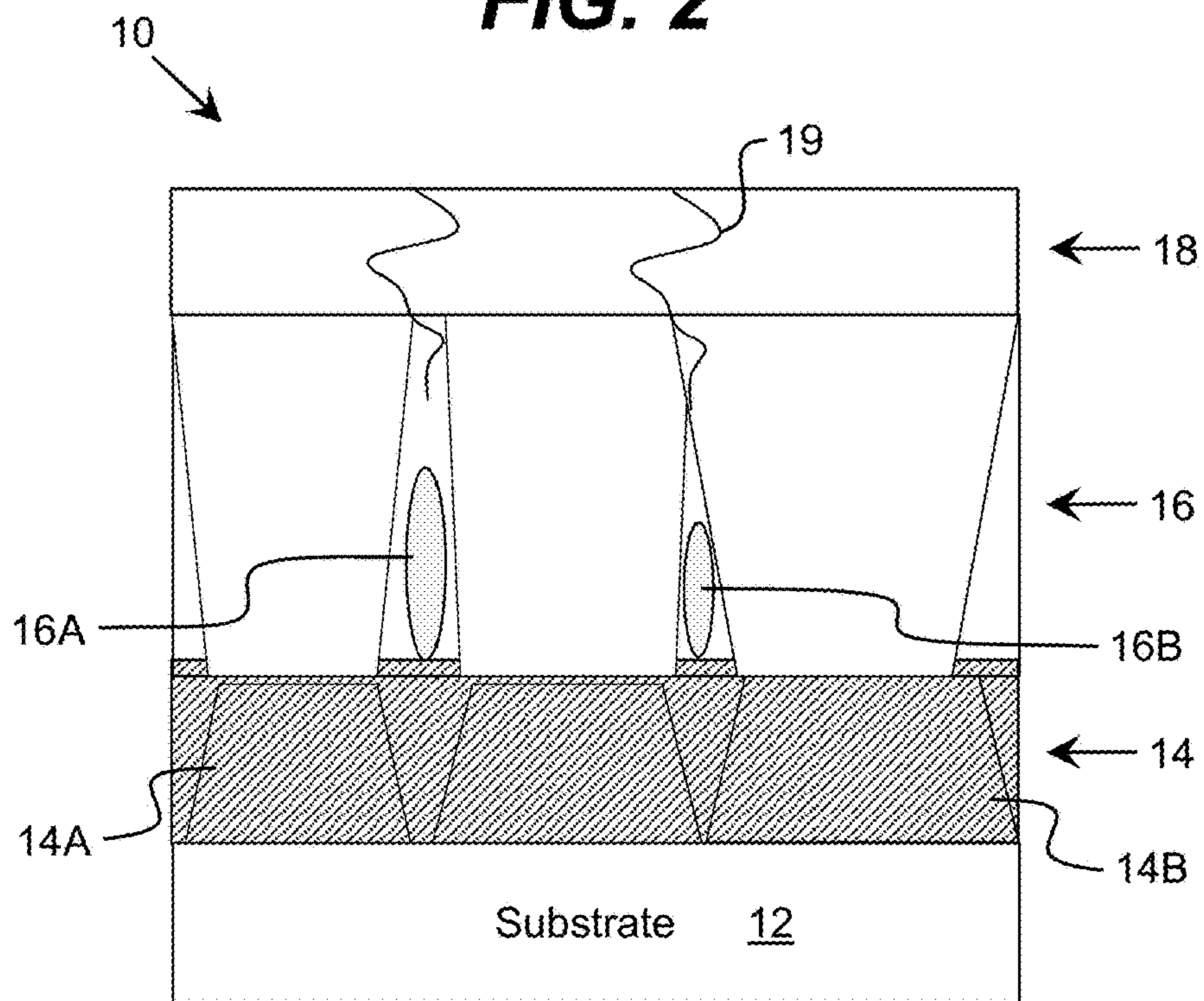


FIG. 3

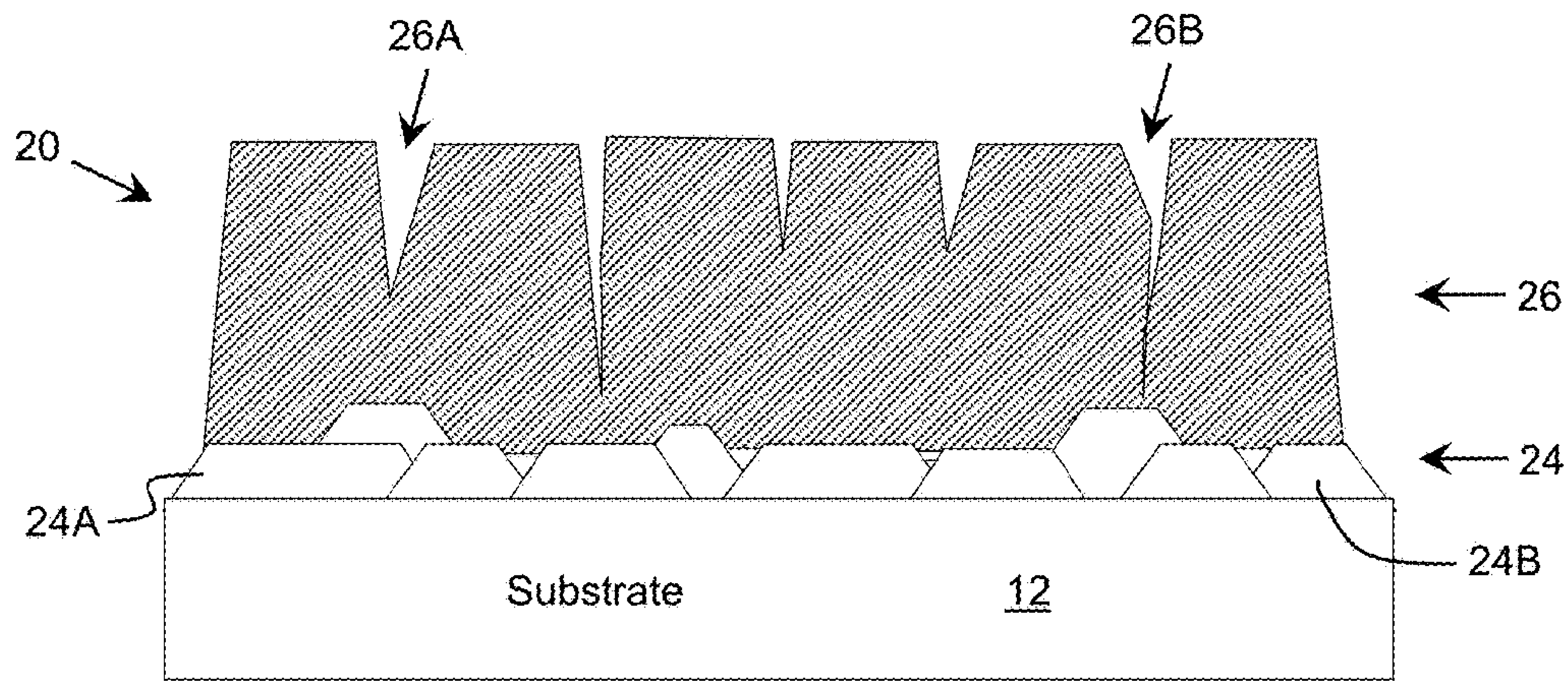


FIG. 4

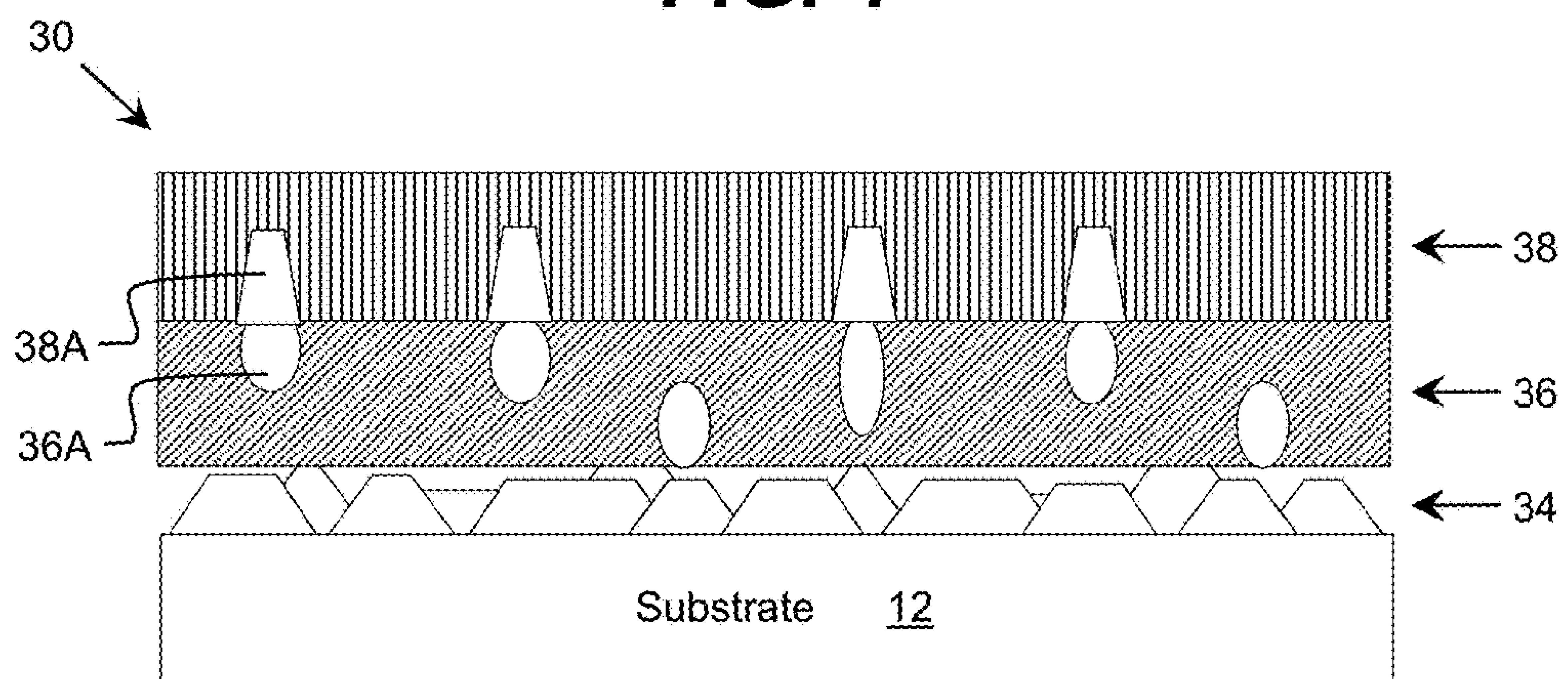


FIG. 5

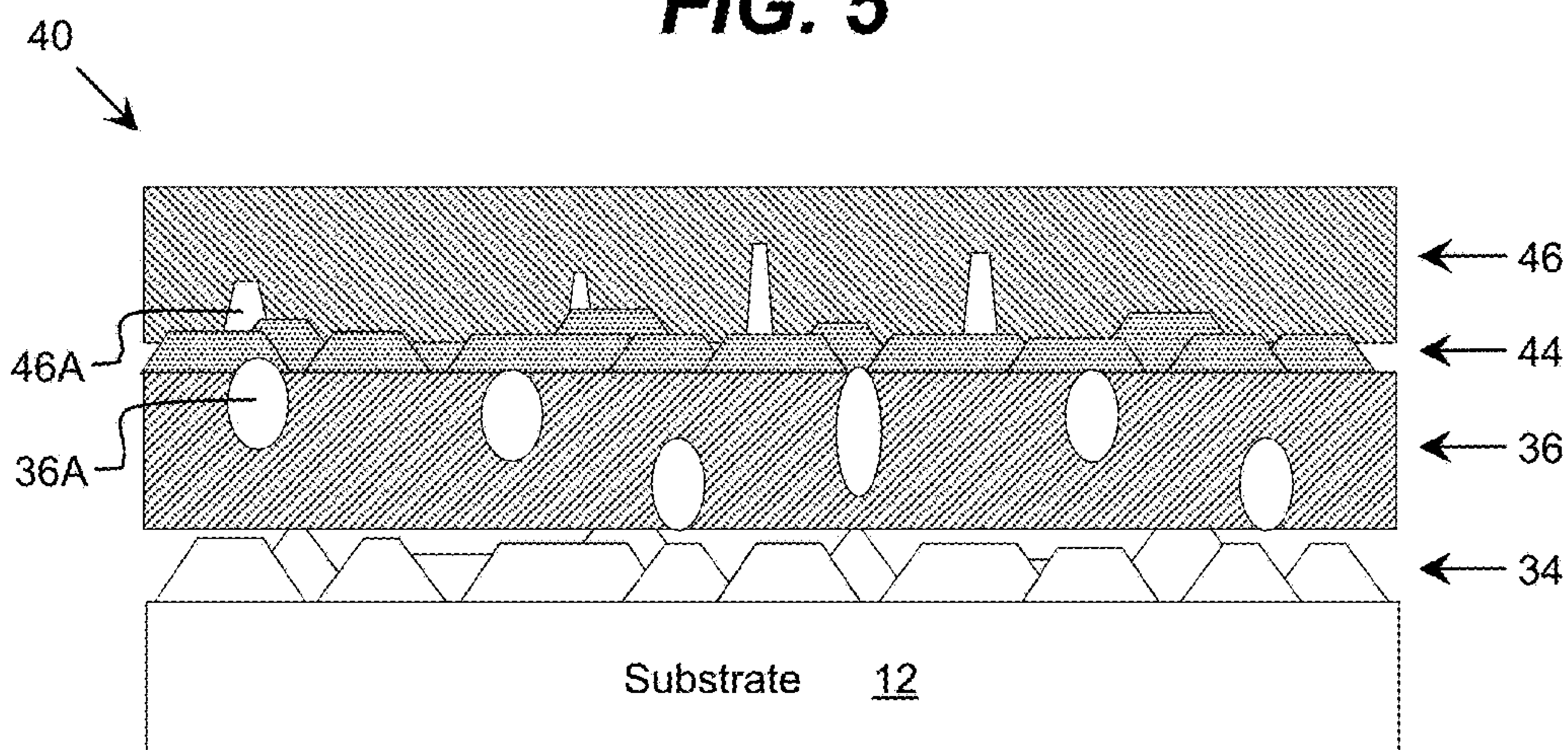


FIG. 6A

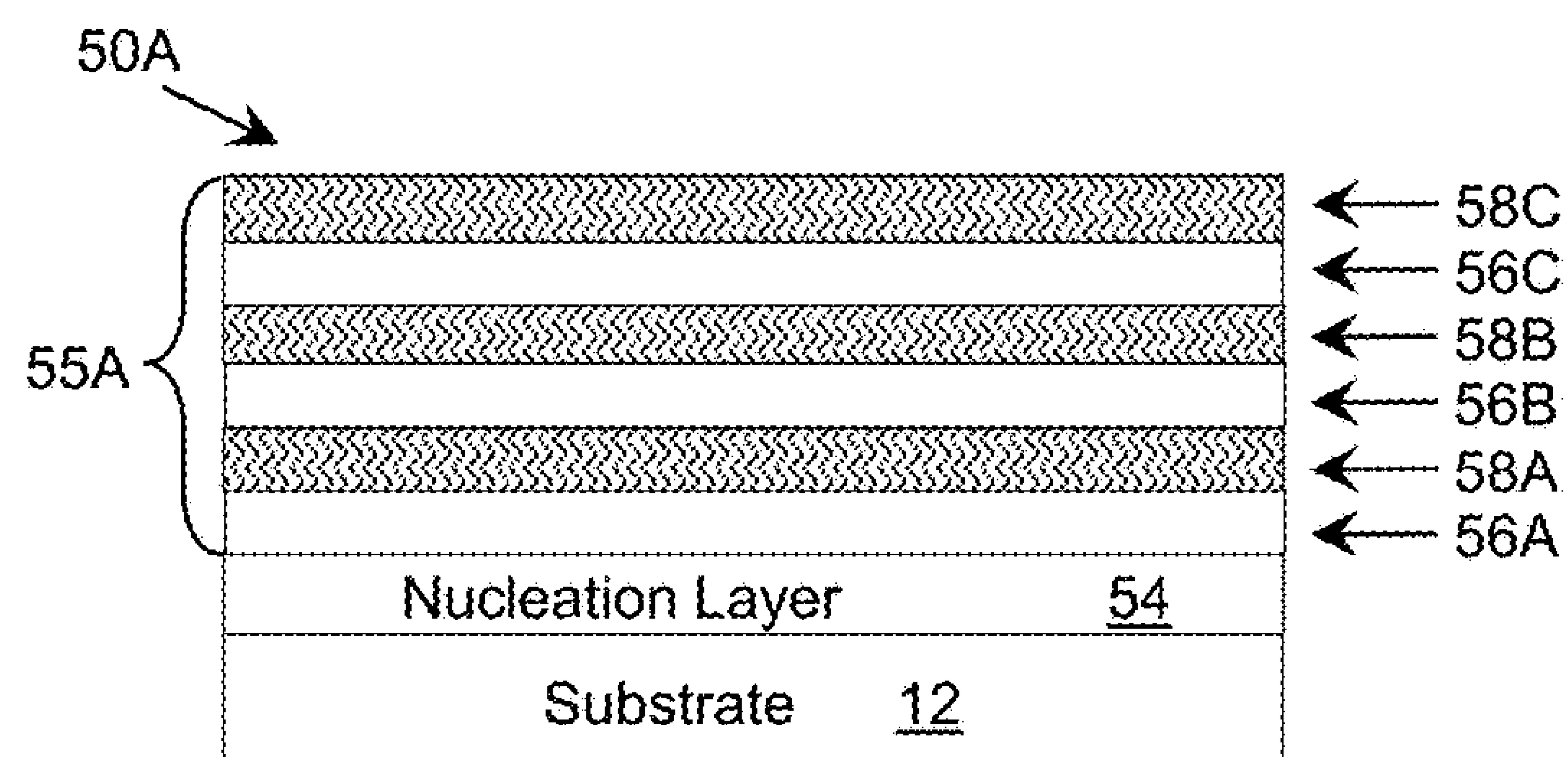


FIG. 6B

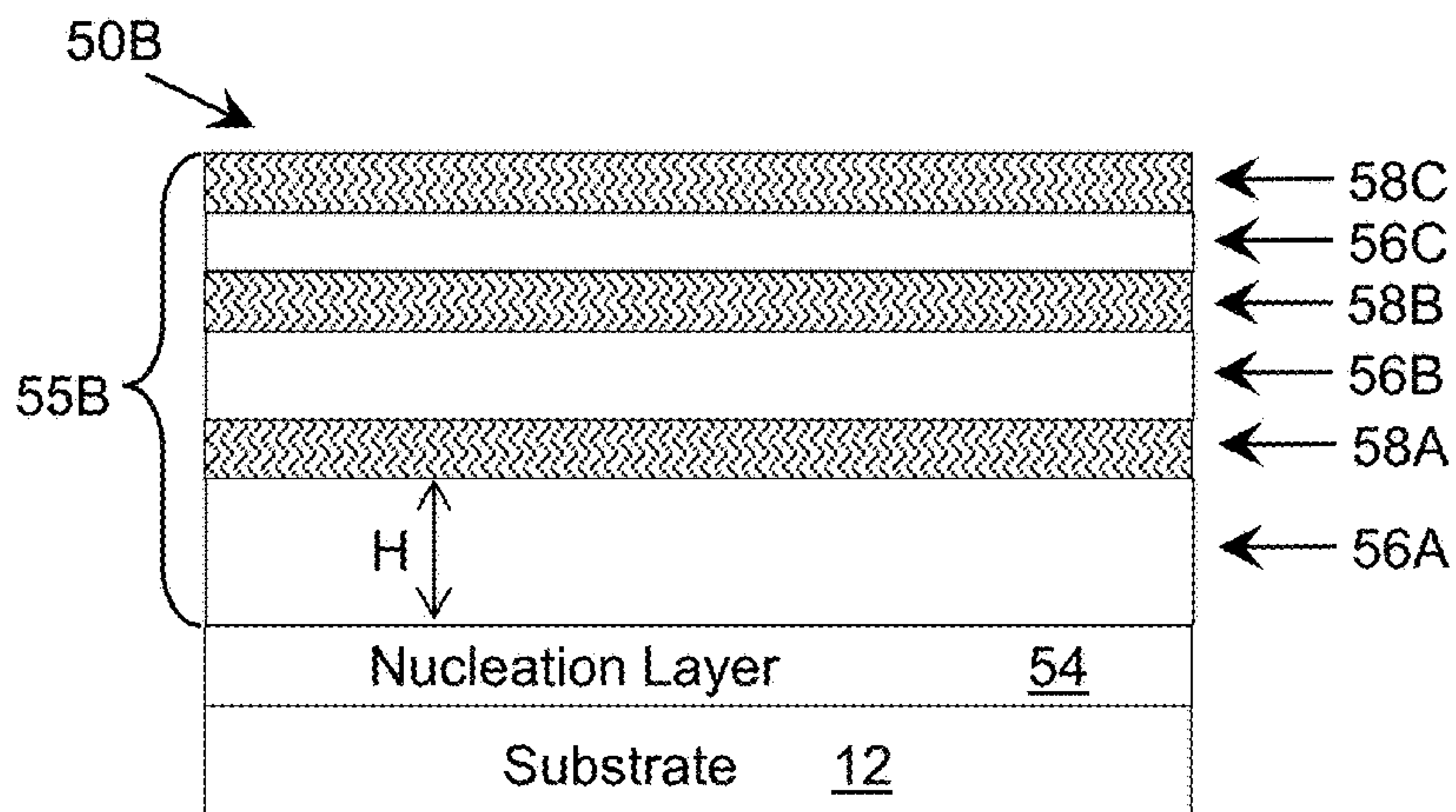


FIG. 6C

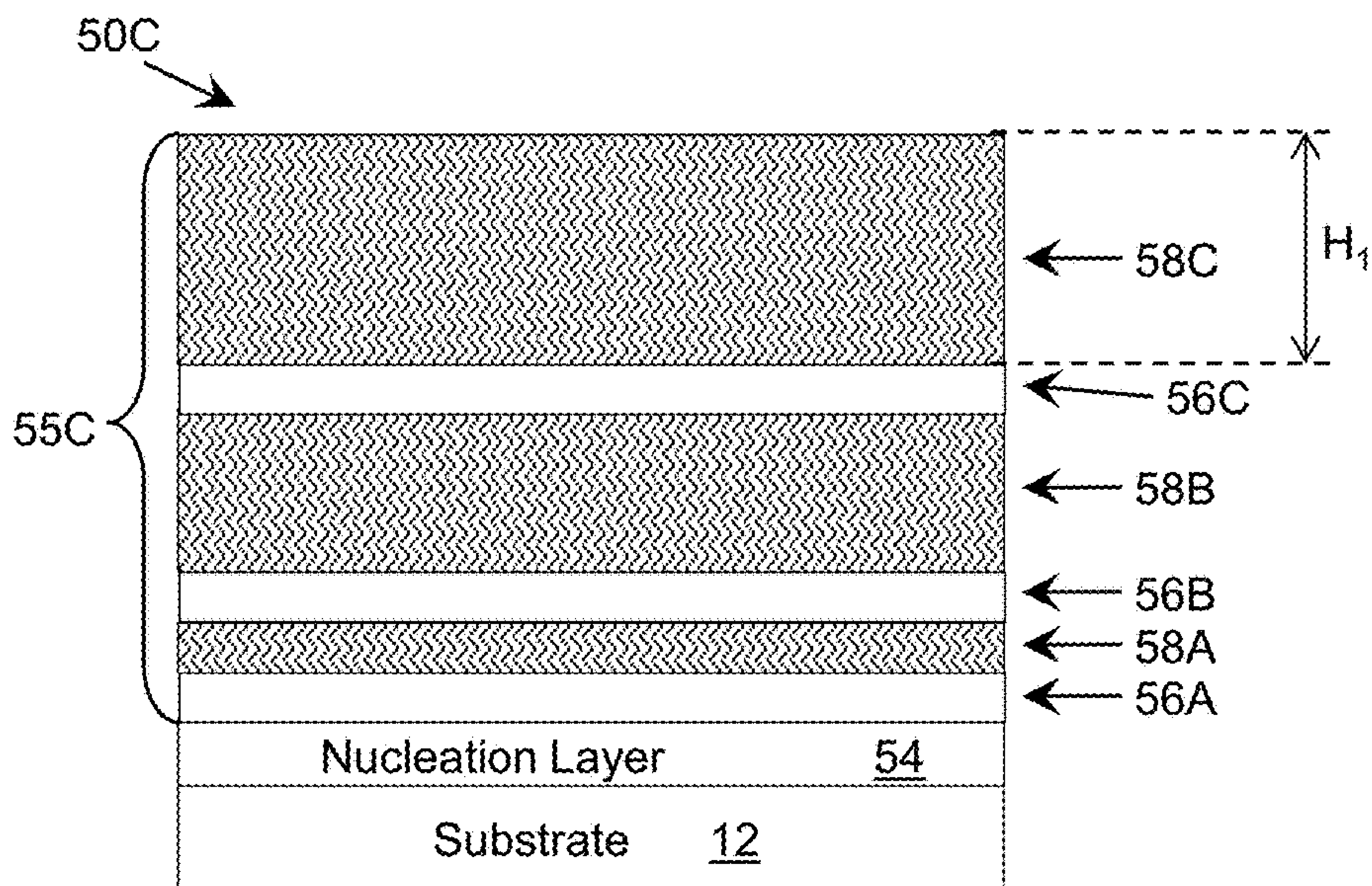


FIG. 7A

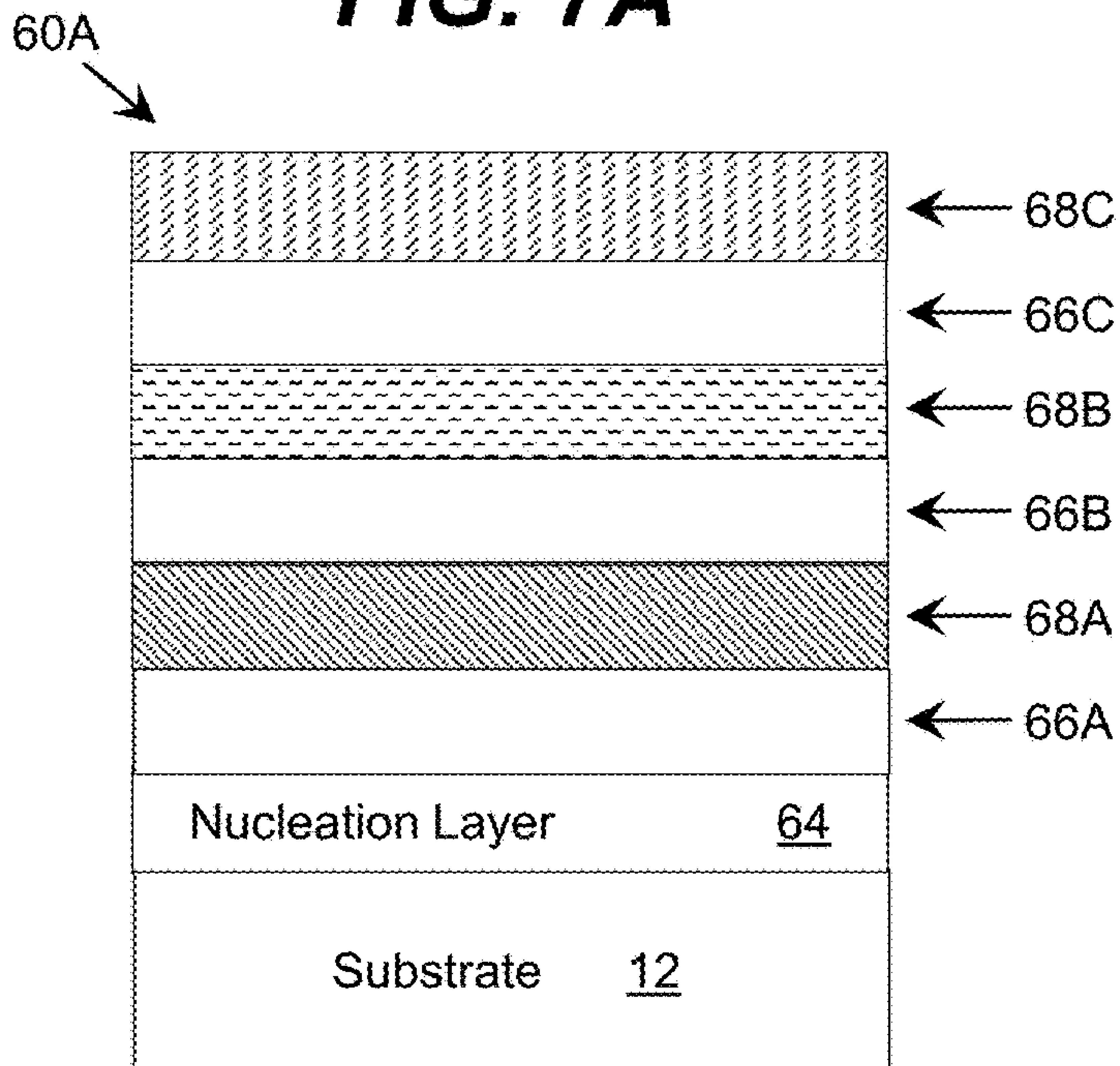


FIG. 7B

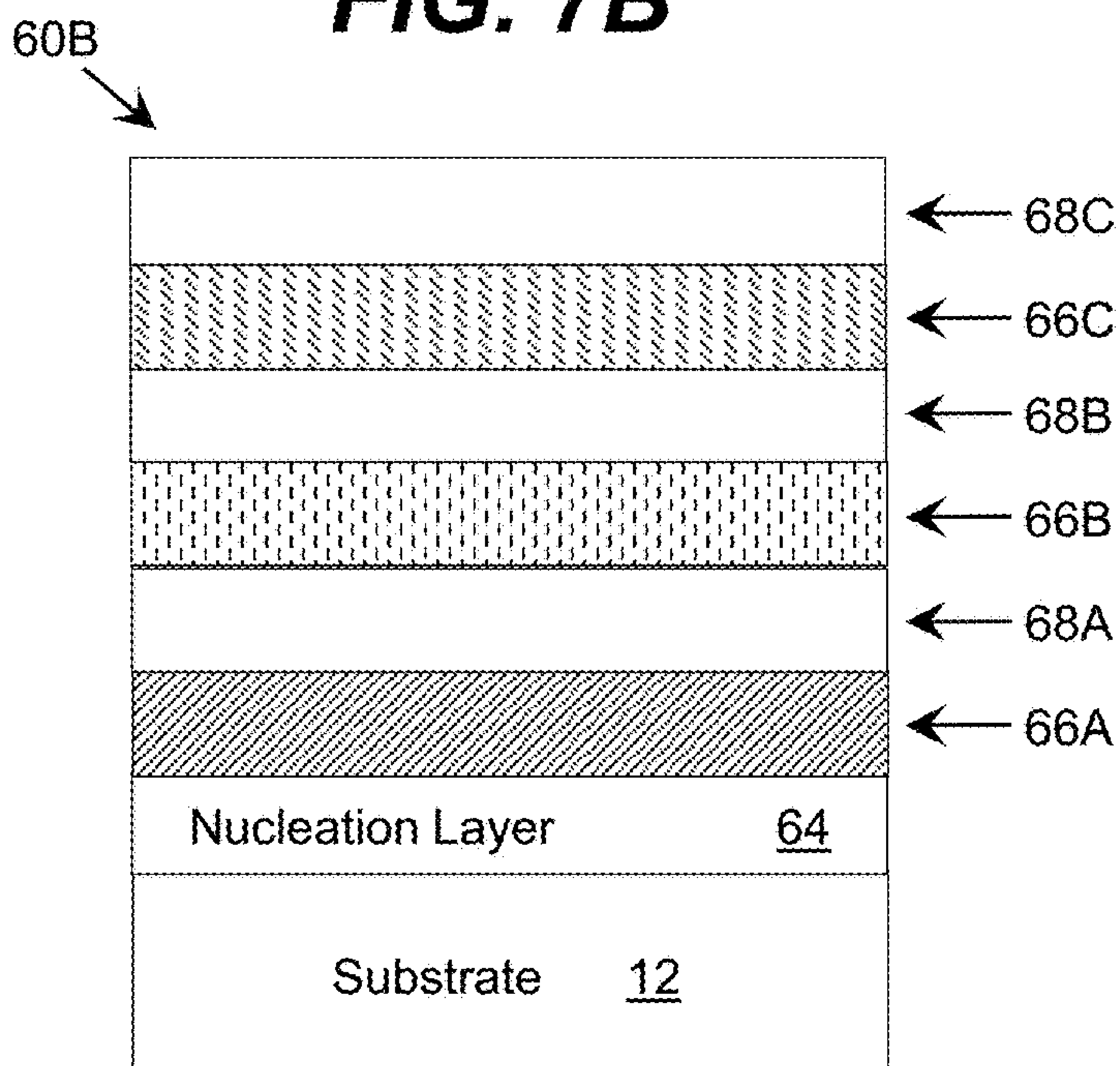


FIG. 8

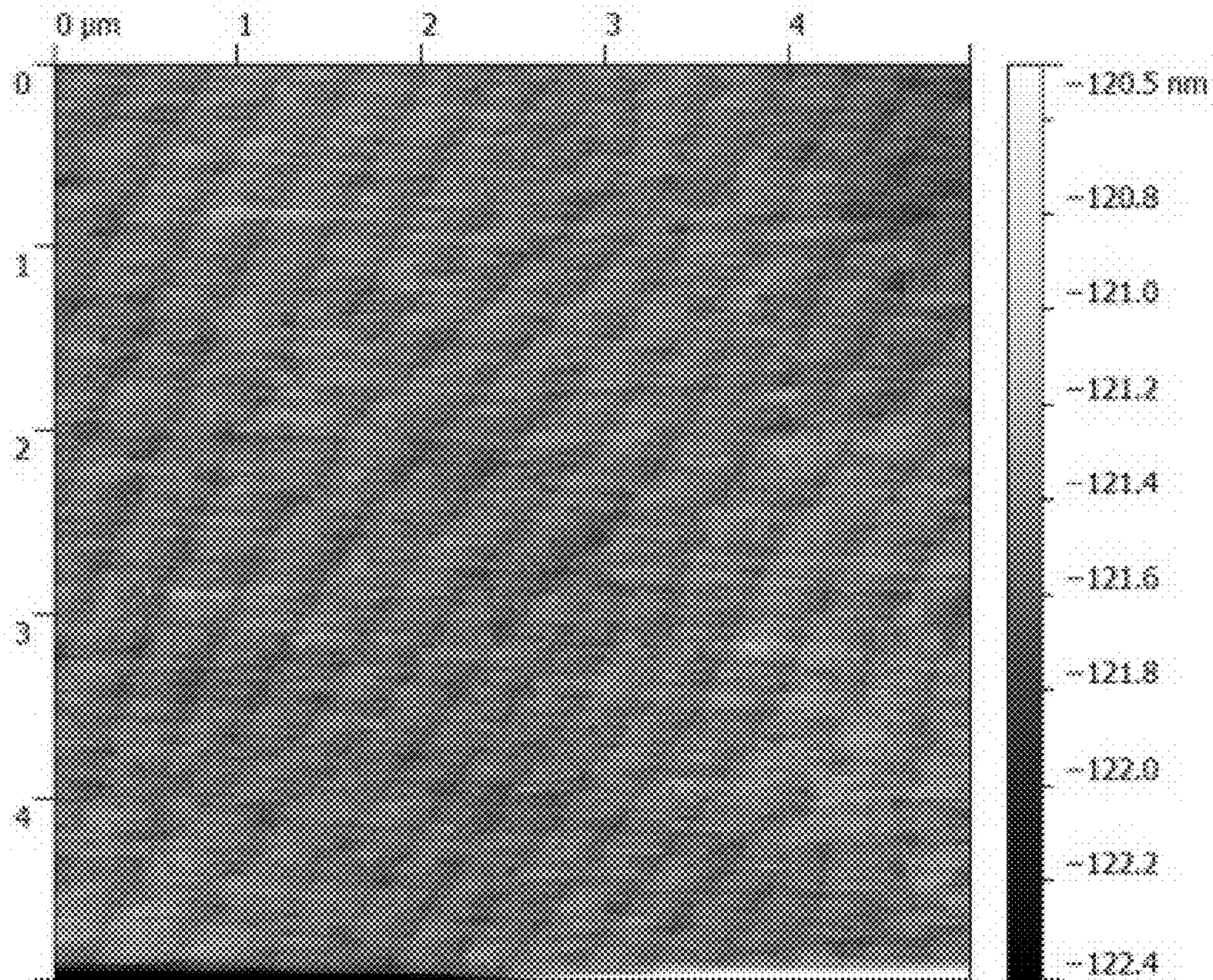
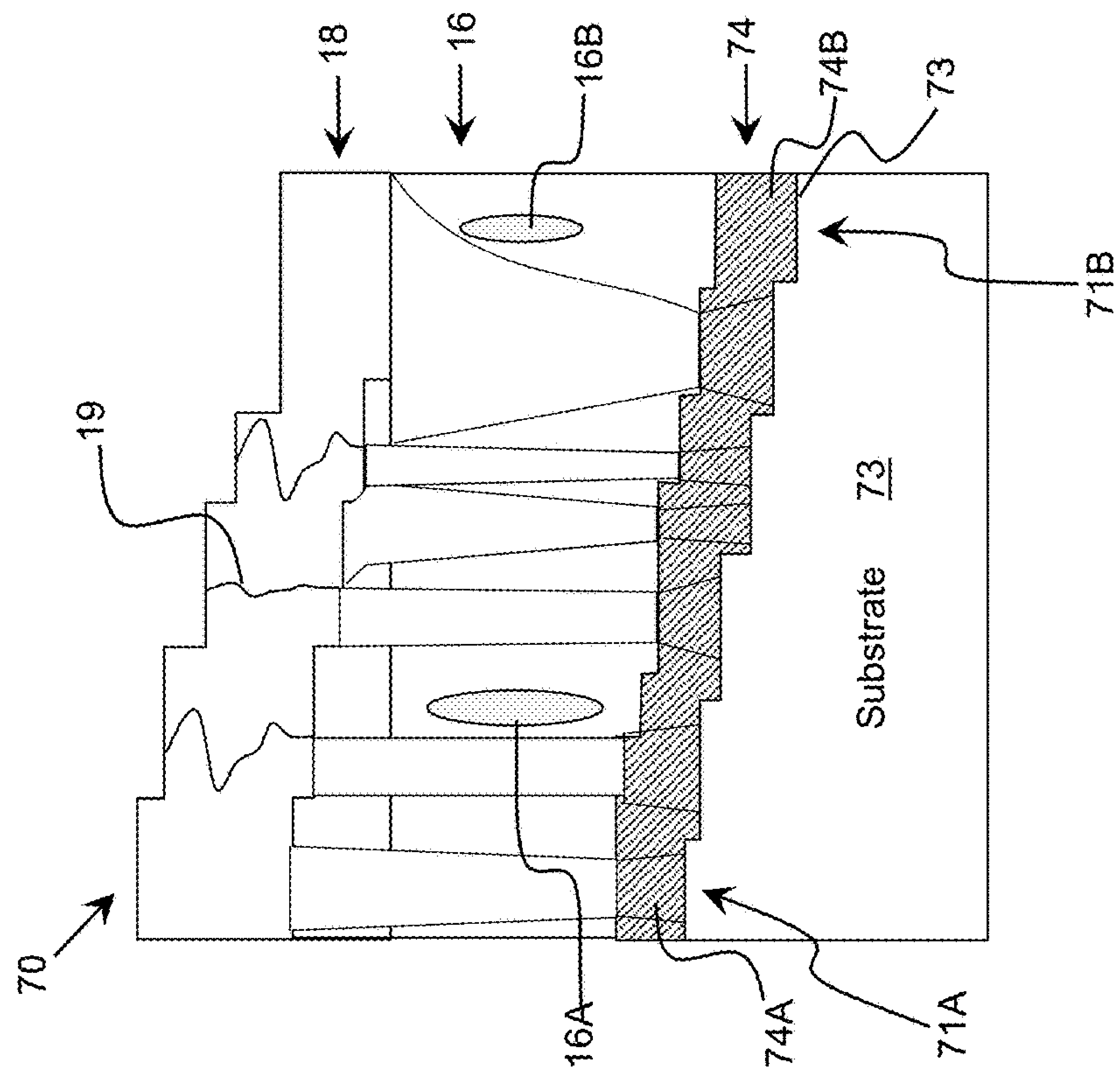


FIG. 9



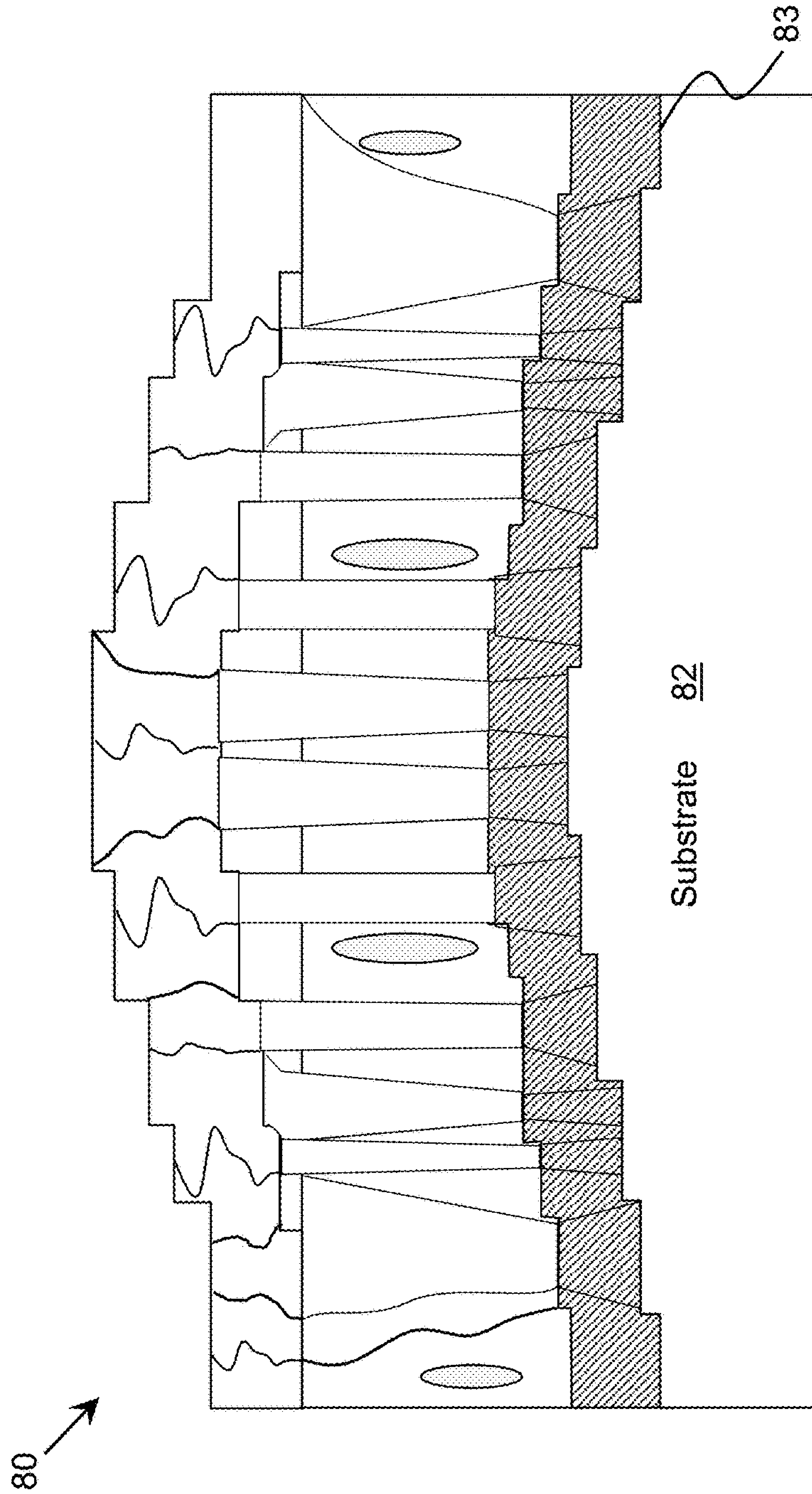


FIG. 10

FIG. 11A

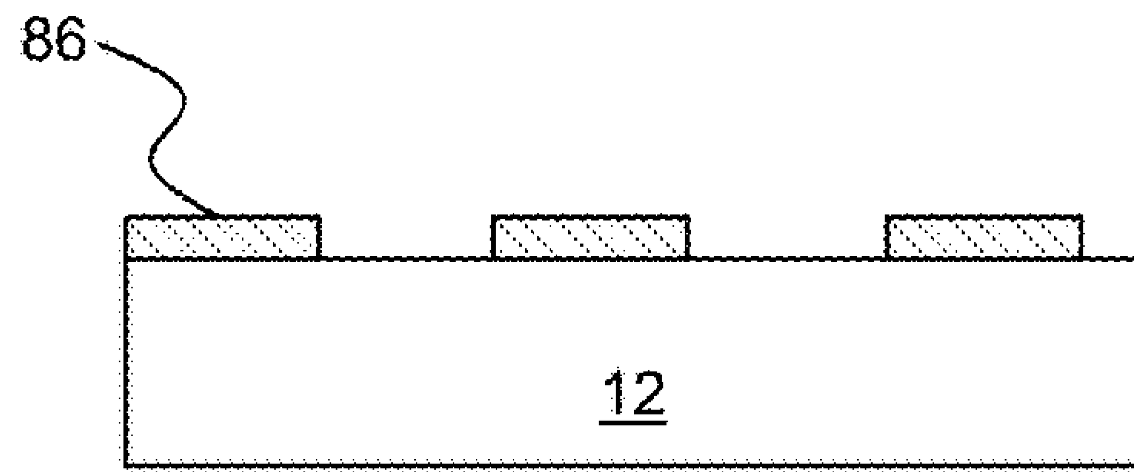


FIG. 11C

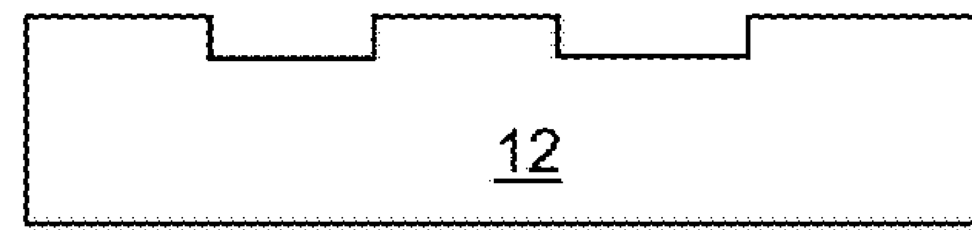


FIG. 11B

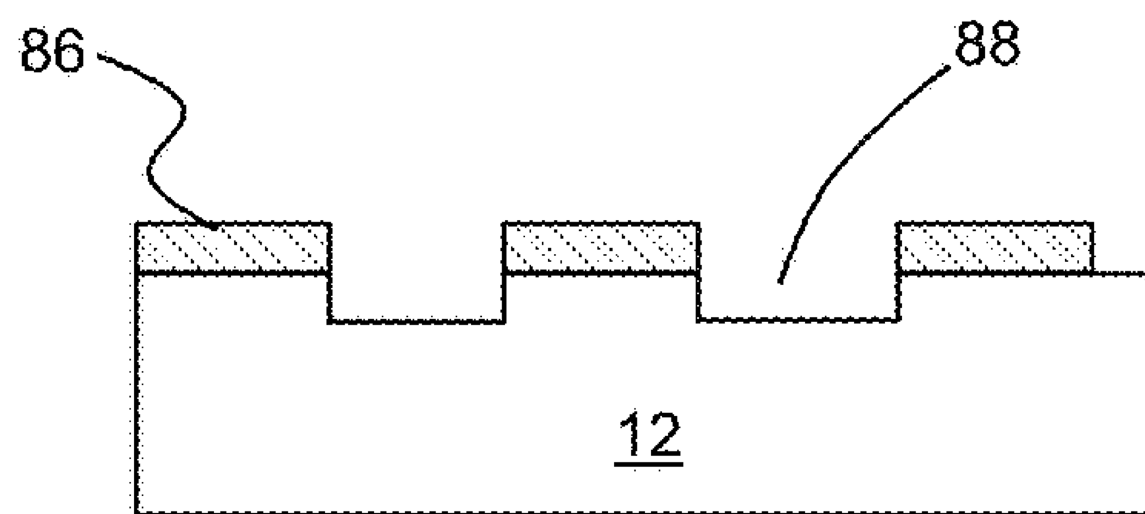


FIG. 11D

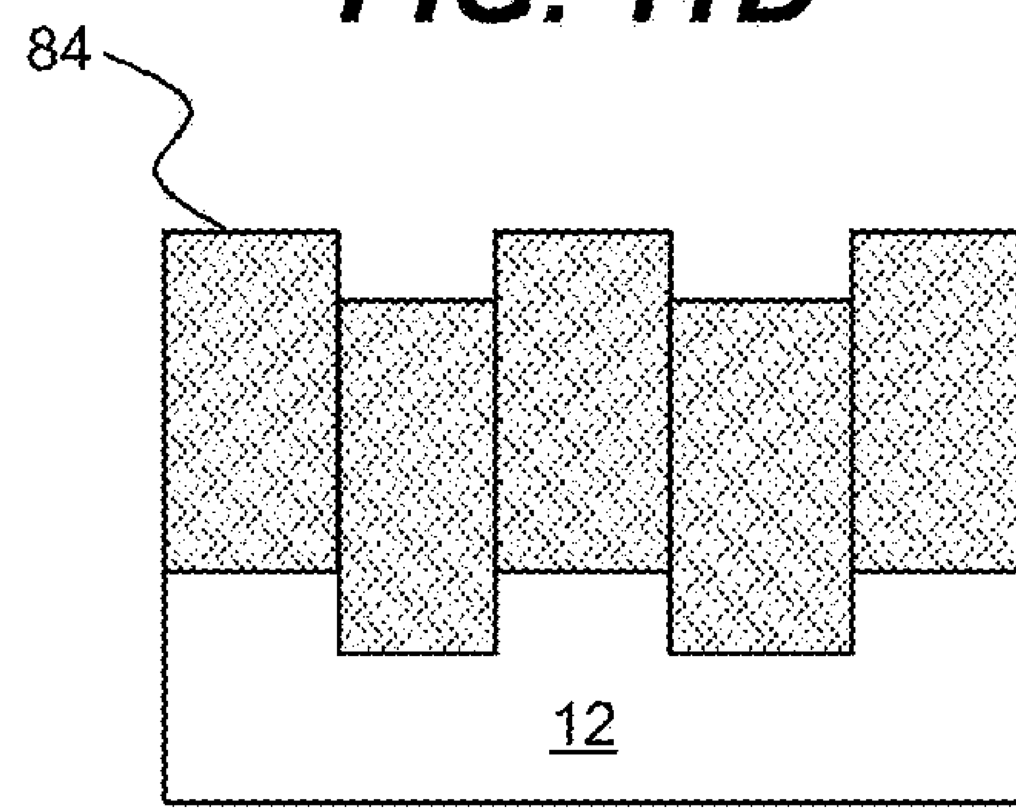


FIG. 12A

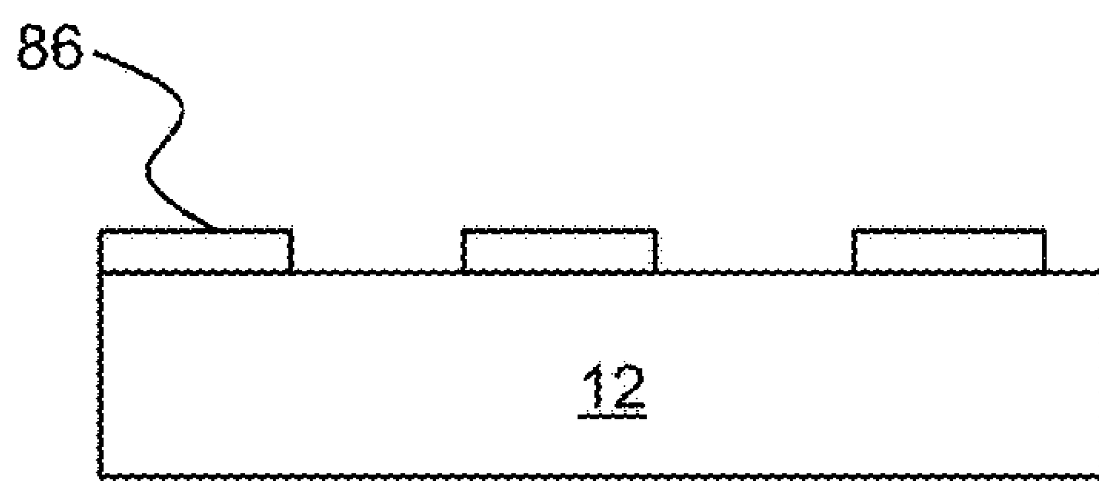


FIG. 12C

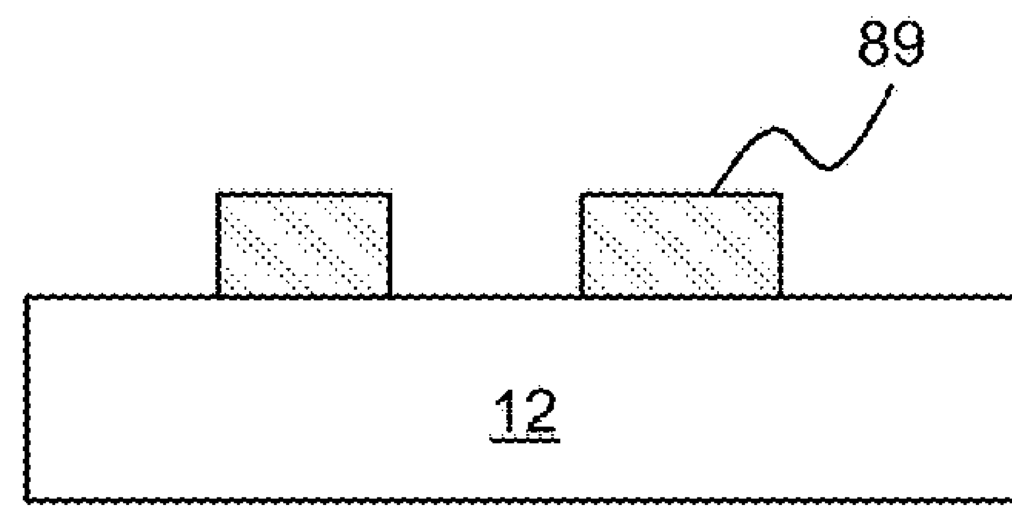


FIG. 12B

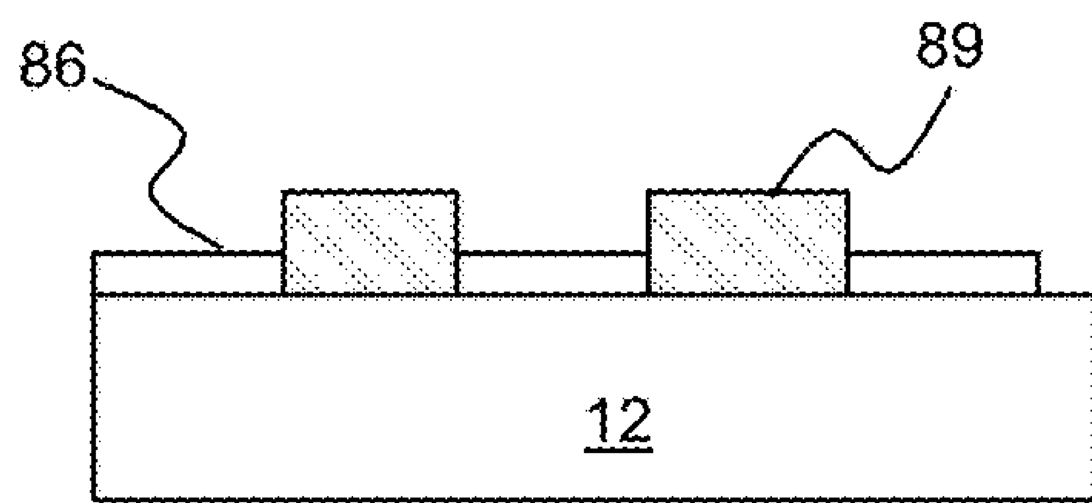


FIG. 12D

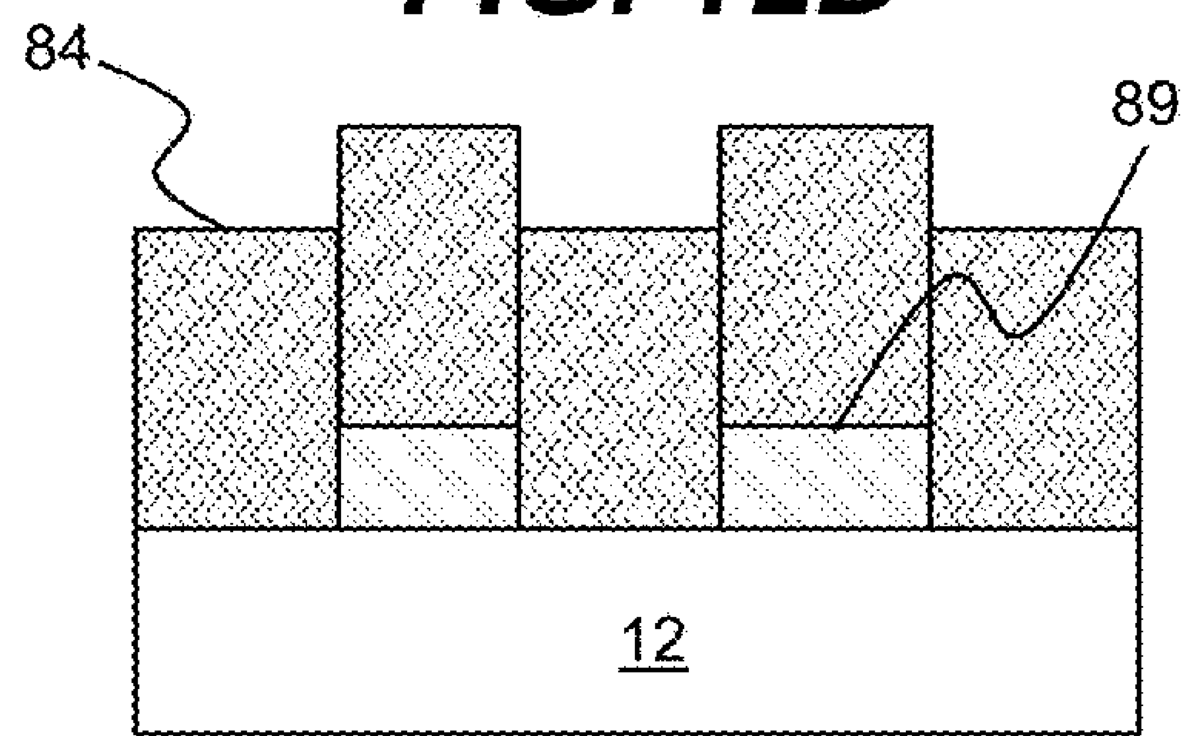


FIG. 13

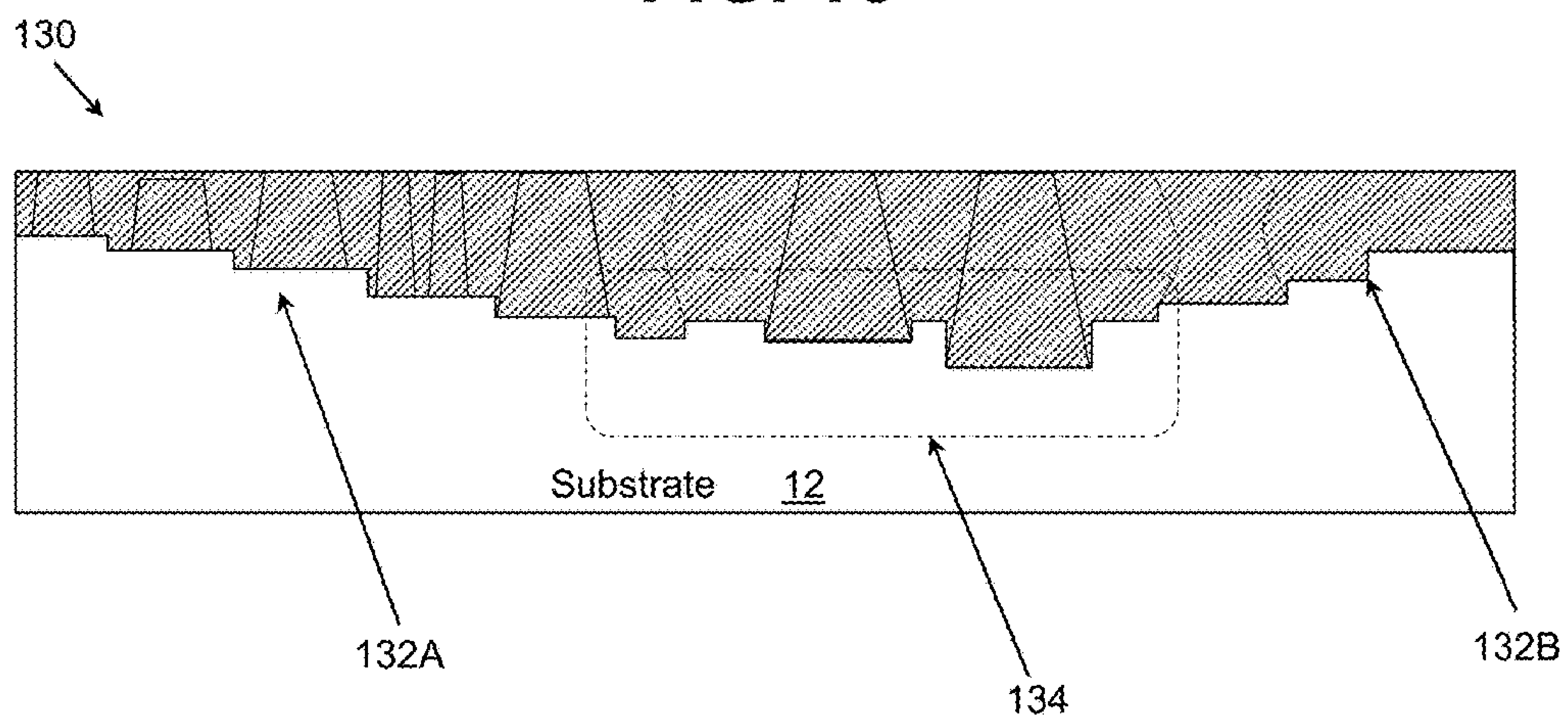


FIG. 14A

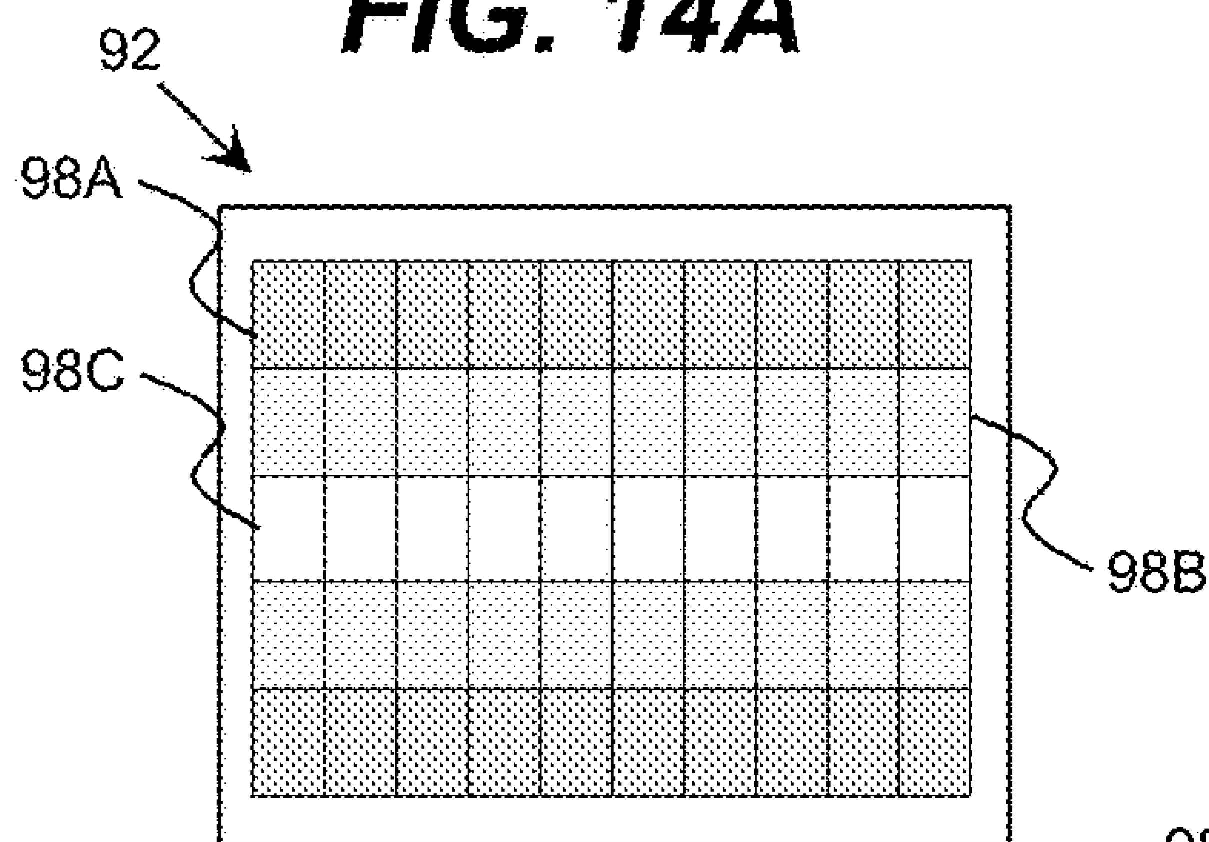


FIG. 14B

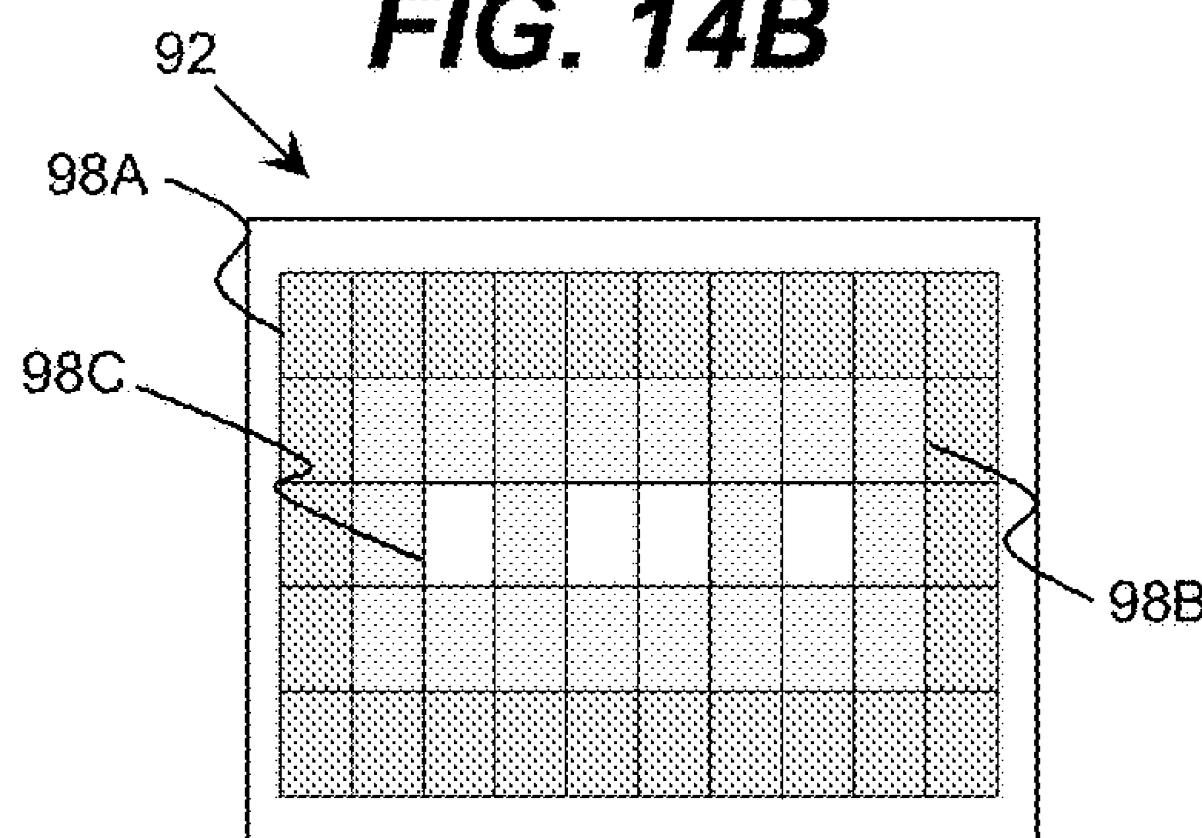


FIG. 14C

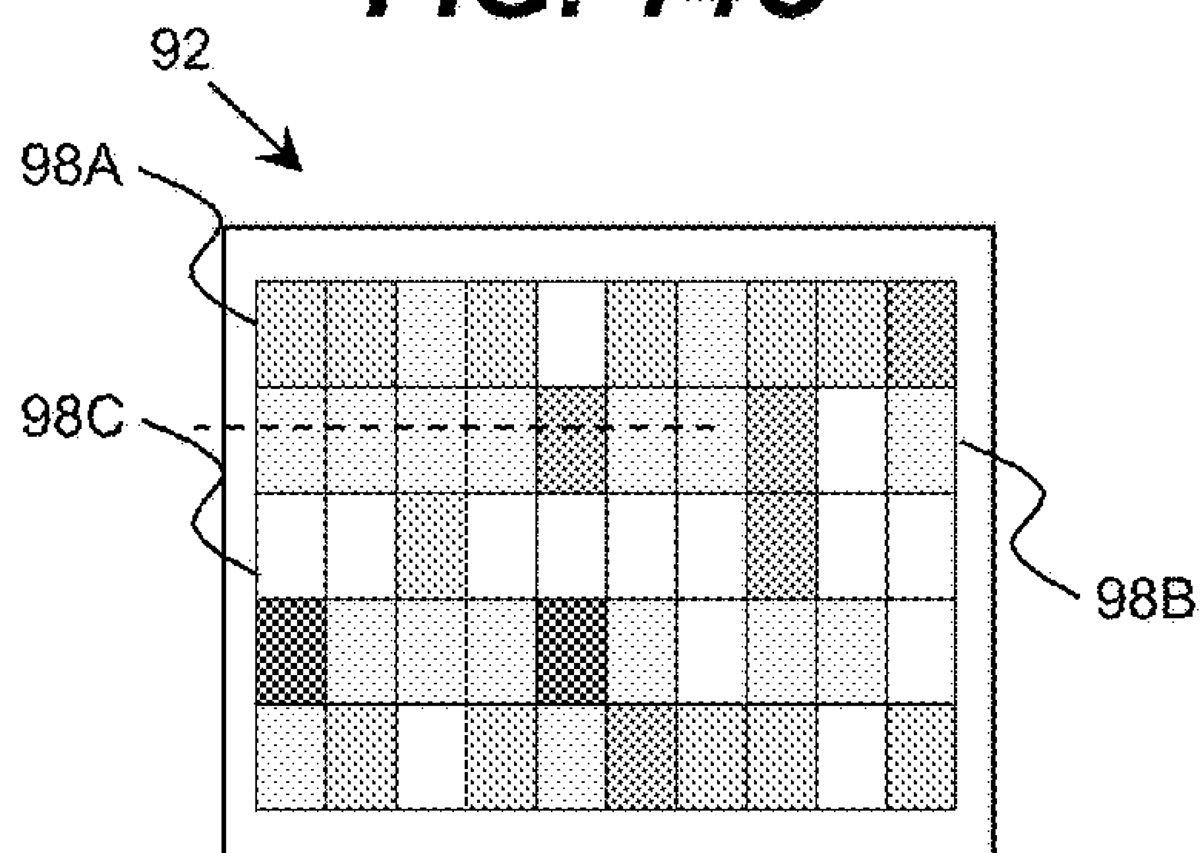


FIG. 14E

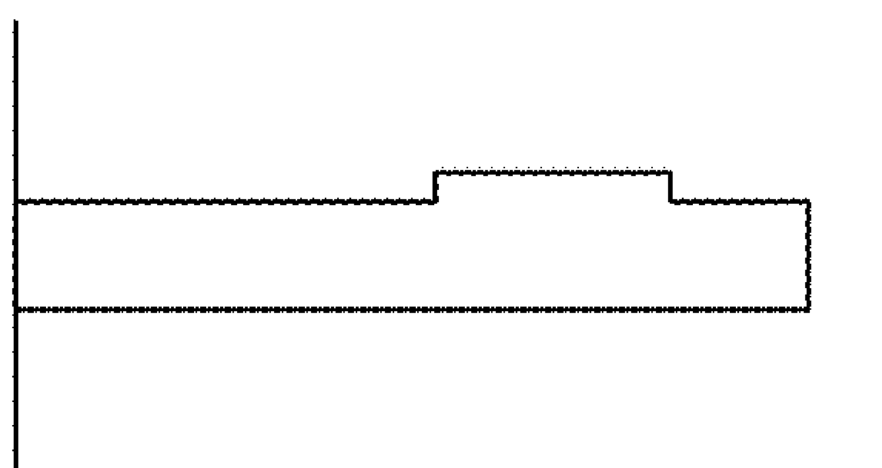
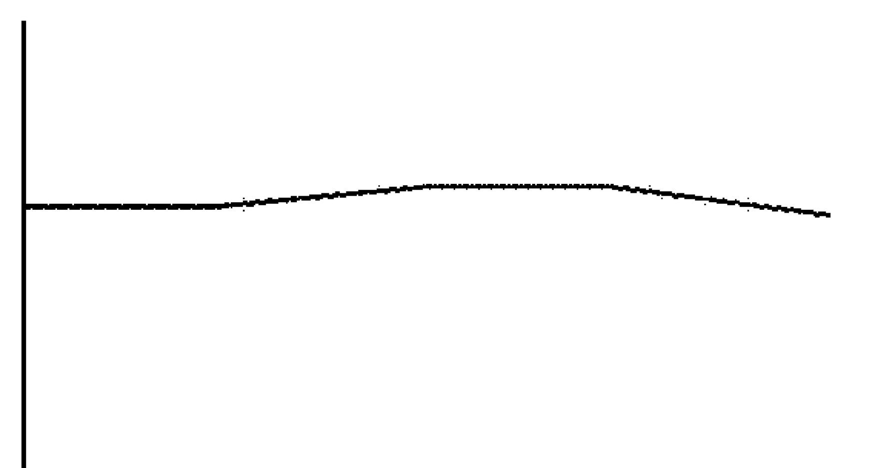


FIG. 14D



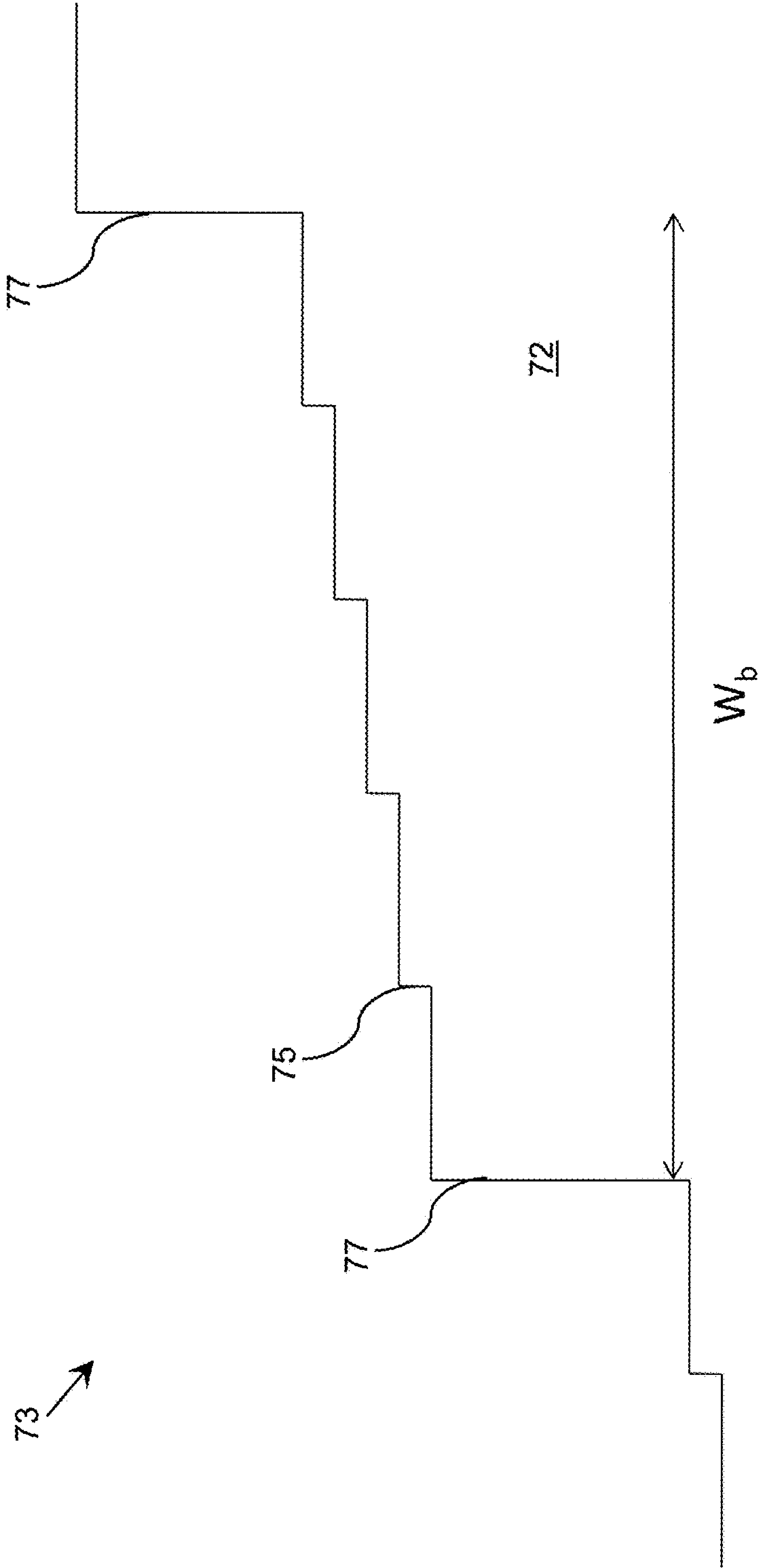


FIG. 15

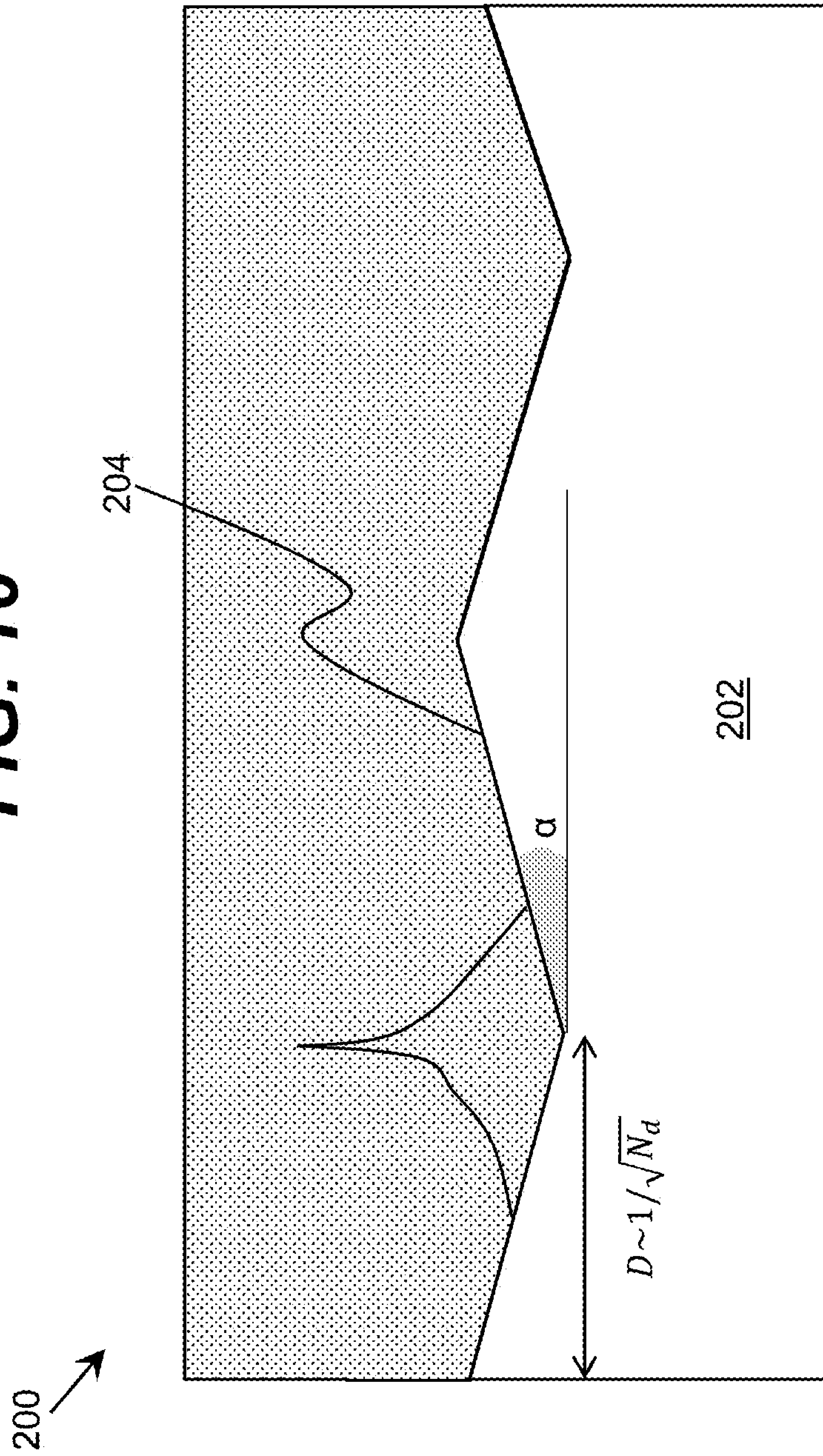


FIG. 16

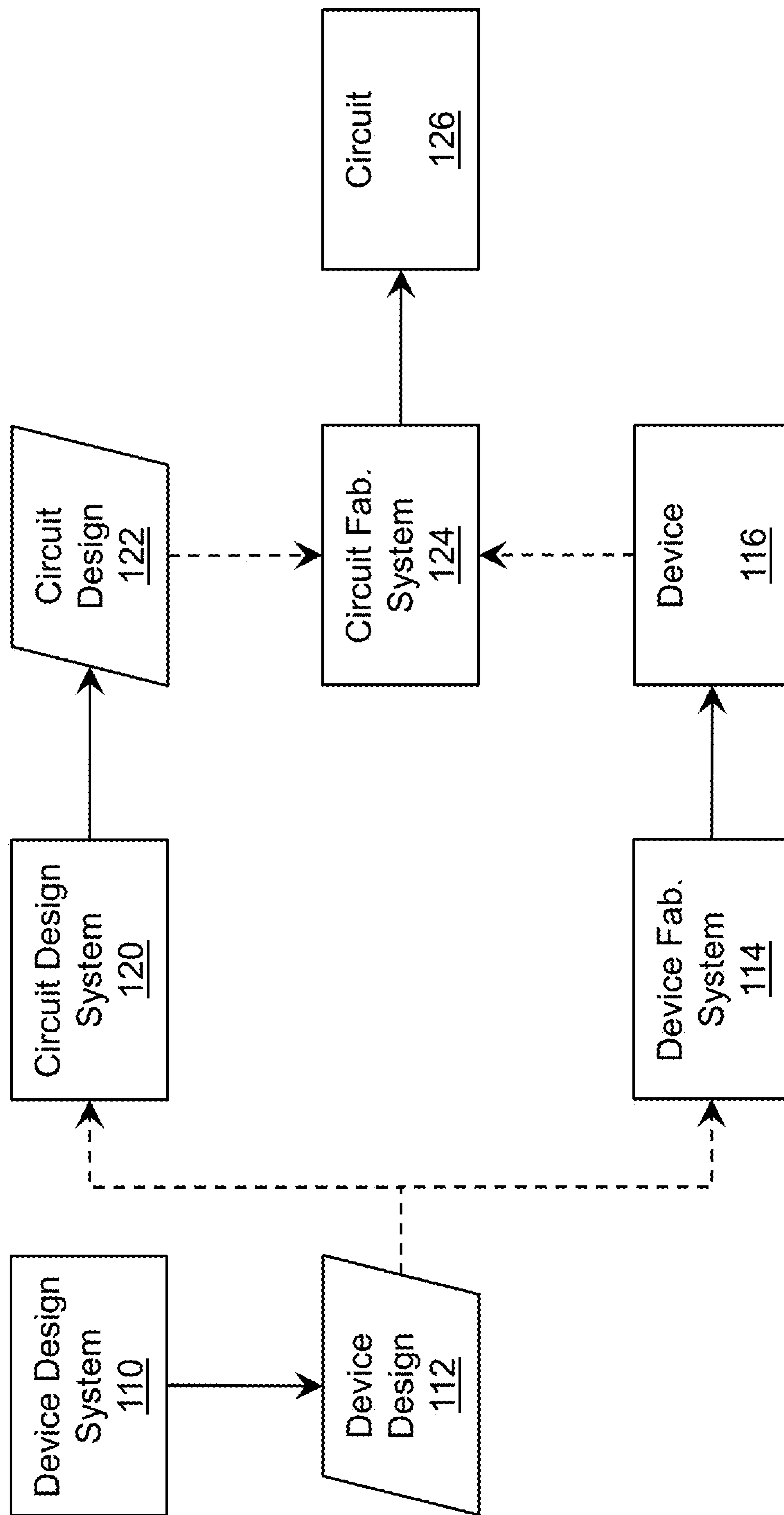


FIG. 17

STRESS RELIEVING SEMICONDUCTOR LAYER

REFERENCE TO RELATED APPLICATIONS

The current application is a continuation application of U.S. patent application Ser. No. 15/144,064, filed on 2 May 2016, which is a continuation-in-part application of U.S. application Ser. No. 14/266,900, now U.S. Pat. No. 9,330, 906, filed on 1 May 2014, which claims the benefit of U.S. Provisional Application No. 61/817,970, filed on 1 May 2013, all of which are hereby incorporated by reference. Aspects of the invention are related to U.S. Pat. No. 8,981, 403, which issued on 17 Mar. 2015, and U.S. patent application Ser. No. 14/150,930, filed on 9 Jan. 2014, both of which are hereby incorporated by reference.

TECHNICAL FIELD

The disclosure relates generally to growth of semiconductor layers, and more particularly, to an improved solution for growing semiconductor layers.

BACKGROUND ART

Group III nitride semiconductors are widely used for efficient blue and ultraviolet light emitting diodes, lasers, ultraviolet detectors, and field effect transistors. Due to a wide band-gap, these materials are one of the primary choices for fabricating deep ultraviolet light emitting diodes (DUV LEDs). In recent years, significant advances have been made in improving the efficiency of DUV LED. However, overall efficiencies of these devices remain low. For fabrication of DUV LEDs, it is crucial to achieve a high quality AlN buffer layer as an underlying layer for the subsequent growth of any Al-rich group III nitride semiconductor layers. However, it is extremely difficult to grow an AlN layer with high crystal quality on sapphire, silicon carbide (SiC), and silicon, which are currently the main substrates for growth of group III nitride devices.

For light emitting devices, such as light emitting diodes (LEDs) and especially deep ultraviolet LEDs (DUV LEDs), minimizing a dislocation density and a number of cracks in the semiconductor layers increases the efficiency of the device. To this extent, several approaches have sought to grow low-defect semiconductor layers on patterned substrates. These approaches typically rely on reducing stresses present in epitaxially grown semiconductor layers.

For example, one approach to reduce stress accumulation in an epitaxially grown layer relies on patterning the underlying substrate using microchannel epitaxy (MCE). Using MCE, a narrow channel is used as a nucleation center containing low defect information from the substrate. An opening in a mask acts as a microchannel, which transfers crystal information to the overgrown layer, while the mask prevents dislocations from transferring to the overgrown layer. As a result, the overgrown layer can become dislocation free. The three-dimensional structure of the MCE also provides another advantage to stress release. The residual stress can be released effectively since the overgrown layer easily deforms. In another approach, a mask is applied at a location of a large concentration of dislocation densities to block their further propagation.

Other approaches rely on epitaxially growing a group III nitride based semiconductor superlattice. The superlattice structure mitigates the strain difference between an aluminum nitride (AlN)/sapphire template and the subsequent thick $Al_xGa_{1-x}N$ (where $0 \leq x \leq 1$) layers. For devices such as DUV LEDs, thick AlGaN epitaxial layers (e.g., of the order of a few micrometers) are desirable to reduce current crowding. Using a superlattice approach, an AlN/AlGaN superlattice was grown to reduce biaxial tensile strain and a 3.0-μm-thick $Al_{0.2}Ga_{0.8}N$ was achieved on sapphire without any cracks. Such a superlattice can be used to minimize the dislocation density due to varying stresses in the sublayers of the superlattice elements.

While the superlattice approaches allow some control of tensile and compressive stresses in epitaxially grown nitride semiconductor layers, the approaches do not enable epitaxial growth of nitride based semiconductor layers with uniform composition. Based on previous experience obtained from GaN growth, lateral epitaxial overgrowth (LEO) has been shown to be an efficient way for significant reduction of dislocation in GaN films. Several other technologies evolved from LEO, such as pendeo-epitaxial, cantilever epitaxy, and facet controlled LEO, have also been developed. While the above approaches work well for epitaxial growth of GaN semiconductor layers, epitaxial growth of AlN layers is more challenging due to small lateral growth of AlN films.

Another leading approach includes growth of AlN films over patterned substrates, such as, for example, patterned sapphire substrate (PSS). While the PSS based approaches generally produce an AlN layer with reduced stress and low dislocation densities, the patterning process and subsequent growth of AlN films is technologically complicated and costly.

One previously described approach proposes to reduce dislocation density between an AlGaN layer and a sapphire substrate by forming a self-organizing porous AlN layer of non-coalescing column-like islands with flat tops on the substrate. In this approach, the self-organizing porous AlN layer is grown at a relatively low V/III ratio of sixty. While the AlN layer is described as being porous, the disclosure does not define any details of such layer, nor does it disclose how the pores are connected or their sizes and densities.

SUMMARY OF THE INVENTION

The inventors propose a growth technology for a group III-V layer, in which the layer is grown at a significantly higher V/III ratio than that disclosed in the prior art. The inventors propose to control the size and density of cavities in the layer through a variable V/III ratio and/or a variable temperature schedule for growth of a nucleation layer, a cavity layer, and a subsequent semiconductor layer containing no cavities. Attributes of an embodiment of the cavity sizes and densities are described herein, and experimentally achieved results are presented in which the cavities are well separated from one another and are morphologically dissimilar to pores described in the prior art.

Aspects of the invention provide a semiconductor structure, such as a group III nitride-based semiconductor structure. The semiconductor structure includes a cavity containing semiconductor layer. The cavity containing semiconductor layer can have a thickness greater than two monolayers and a multiple cavities. The cavities can have a characteristic size of at least one nanometer and a characteristic separation of at least five nanometers.

A first aspect of the invention provides a structure comprising: a cavity containing layer, wherein the cavity containing layer is formed of a semiconductor material, has a thickness greater than two monolayers, and has a plurality of cavities, and wherein the plurality of cavities have a characteristic size of at least one nanometer and a characteristic

separation of at least five nanometers; and a semiconductor layer immediately adjacent to the cavity containing layer, wherein the semiconductor layer contains no large scale cavities, and wherein a molar fraction of a semiconductor element in the semiconductor layer differs from a molar fraction of the semiconductor element in cavity containing layer by at least two percent.

A second aspect of the invention provides a device comprising: a nucleation layer, wherein the nucleation layer has a thickness of at least one nanometer and contains no large scale cavities; a cavity containing layer located directly on the nucleation layer, wherein the cavity containing layer is formed of a semiconductor material, has a thickness greater than two monolayers, and has a plurality of cavities, and wherein the plurality of cavities have a characteristic size of at least one nanometer and a characteristic separation of at least five nanometers; and a semiconductor layer immediately adjacent to the cavity containing layer, wherein the semiconductor layer contains no large scale cavities, and wherein a molar fraction of a semiconductor element in the semiconductor layer differs from a molar fraction of the semiconductor element in cavity containing layer by at least two percent.

A third aspect of the invention provides a method comprising: fabricating a semiconductor structure, wherein the fabricating includes: growing a nucleation layer on a substrate, wherein the nucleation layer has a thickness of at least one nanometer and contains no large scale cavities; forming a cavity containing layer directly on the nucleation layer, wherein the cavity containing layer has a thickness greater than two monolayers and a plurality of cavities; and forming a semiconductor layer directly on the cavity containing layer, wherein the semiconductor layer contains no large scale cavities, and wherein a molar fraction of a semiconductor element in the semiconductor layer differs from a molar fraction of the semiconductor element in cavity containing layer by at least two percent.

The illustrative aspects of the invention are designed to solve one or more of the problems herein described and/or one or more other problems not discussed.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the disclosure will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings that depict various aspects of the invention.

FIG. **1** illustrates a conventional approach for reducing dislocations according to the prior art.

FIG. **2** shows an illustrative structure according to an embodiment.

FIG. **3** shows an illustrative structure according to an embodiment.

FIG. **4** shows an illustrative structure according to an embodiment.

FIG. **5** shows an illustrative structure according to an embodiment.

FIGS. **6**A-**6**C show illustrative structures including superlattices according to embodiments.

FIGS. **7**A and **7**B show illustrative structures according to embodiments.

FIG. **8** shows an image surface morphology of an illustrative cavity containing layer according to an embodiment.

FIG. **9** shows an illustrative structure according to an embodiment.

FIG. **10** shows an illustrative structure according to an embodiment.

FIGS. **11**A-**11**D show an illustrative method of patterning a substrate according to an embodiment.

FIGS. **12**A-**12**D show an illustrative method of patterning a substrate according to an embodiment.

FIG. **13** shows an illustrative structure according to an embodiment.

FIGS. **14**A-**14**C show illustrative top views of a substrate according to embodiments, while FIGS. **14**D-**14**E show illustrative profiles of a substrate according to embodiments.

FIG. **15** shows an illustrative surface of a substrate according to an embodiment.

FIG. **16** shows an illustrative structure according to an embodiment.

FIG. **17** shows an illustrative flow diagram for fabricating a circuit according to an embodiment.

It is noted that the drawings may not be to scale. The drawings are intended to depict only typical aspects of the invention, and therefore should not be considered as limiting the scope of the invention. In the drawings, like numbering represents like elements between the drawings.

DETAILED DESCRIPTION OF THE INVENTION

As indicated above, aspects of the invention provide a semiconductor structure, such as a group III nitride-based semiconductor structure. The semiconductor structure includes a cavity containing semiconductor layer. The cavity containing semiconductor layer can have a thickness greater than two monolayers and a multiple cavities. The cavities can have a characteristic size of at least one nanometer and a characteristic separation of at least five nanometers. The inventors have found that embodiments of such a structure can be configured to reduce internal stresses, threading dislocations, and cracks in the semiconductor layers. Additionally, embodiments can be used to control and/or release built up internal stresses within the structure. As used herein, unless otherwise noted, the term "set" means one or more (i.e., at least one) and the phrase "any solution" means any now known or later developed solution.

FIG. **1** illustrates a conventional approach for reducing dislocations according to the prior art. In this approach, a structure **1** includes a substrate **2** on which a nucleation layer **4** is grown. A semiconductor (e.g., coalescing) layer **8** is grown on the nucleation layer **4**. The nucleation layer **4** is configured to reduce a number of dislocations **9** present in the semiconductor layer **8** as compared to the number of dislocations **9** that would be present were the semiconductor layer **8** grown directly on the substrate **2**.

FIG. **2** shows an illustrative structure **10** according to an embodiment. The structure **10** is shown including a substrate **12**, a nucleation layer **14**, a cavity containing layer **16**, and a semiconductor (e.g., coalescing) layer **18**. The cavity containing layer **16** can act as a stress-relieving layer in the structure **10**. As illustrated, the semiconductor layer **18** can have significantly fewer dislocations **19** than present in the semiconductor layer **8** (FIG. **1**) of the prior art.

In an embodiment, the semiconductor layers **14**, **16**, **18** of the structure **10** are formed of materials selected from the group III-V materials system. In a more particular embodiment, each layer **14**, **16**, **18** is formed of a group III nitride material. The substrate **12** can comprise any suitable substrate material. Illustrative substrate materials for group III nitride layers include sapphire, silicon carbide, silicon, lithium aluminate (γ-$LiAlO_2$), $LiAlO_2$, lithium gallate, spi-

nel ($MgAl_2O_4$), gallium nitride (GaN), aluminum nitride (AlN), Aluminum oxynitride, zinc oxide (ZnO), and/or the like. Each layer **14**, **16**, **18** can have a thickness that is larger than two monolayers. In an embodiment, a thickness of each layer **14**, **16**, **18** is within a range of approximately ten to approximately ten thousand nanometers. A thickness of the cavity containing layer **16** can be selected based on a thickness by which the islands will coalesce, which is highly dependent on the original separation distance of nucleation islands in the nucleation layer **14**. A thickness of the semiconductor layer **18** can be selected to limit cracking. For example, the thickness of the semiconductor layer **18** can be selected to reduce dislocation density by approximately an order of magnitude over that of the prior art. In a more specific illustrative embodiment: a thickness for the nucleation layer **14** is between approximately 5 nanometers and approximately 100 nanometers; a thickness of the cavity containing layer **16** is between approximately 1 micron and approximately 10 microns; and a thickness of the semiconductor layer **18** is between approximately 1 micron and approximately 4 microns.

In an embodiment, each of the layers **14**, **16**, **18** are epitaxially grown on the substrate **12**. For example, the nucleation layer **14** can be epitaxially grown directly on the substrate **12**. Growth of the nucleation layer **14** can include growth of a plurality of nucleation islands **14**A, **14**B at a growth temperature and V/III ratio configured to result in large nucleation islands **14**A, **14**B. For example, the growth temperature can be in a range of approximately 700° C. and approximately 1050° C., and the V/III ratio can be in a range between approximately 1000 and approximately 20000. During growth of the nucleation layer **14**, a typical size of the nucleation islands **14**A, **14**B can be controlled by adjusting a V/III ratio used during the growth. In an embodiment, the nucleation islands **14**A, **14**B have a relatively large lateral size of a few to a few hundred nanometers (e.g., few tens of nanometers), with a similar separation distance between the islands **14**A, **14**B.

The cavity containing layer **16** can be epitaxially grown directly on the nucleation layer **14**. In an embodiment, growth of the cavity containing layer **16** is configured to result in one or more cavities (voids) **16**A, **16**B being present in the cavity containing layer **16**. For example, growth of the cavity containing layer **16** can be performed at a relatively high temperature, which can be approximately a few hundred degrees Celsius higher than a temperature used for growth of the nucleation layer **14**. A characteristic size of the nucleation islands **14**A, **14**B can control a characteristic size and density of cavities **16**A, **16**B present in the cavity containing layer **16** due to a correlation between the size of the nucleation islands **14**A, **14**B and the spacing of cavities. For example, as cavities can form at some, but not necessarily all, boundaries of nucleation islands **14**A, **14**B, larger nucleation islands **14**A, **14**B will cause the cavities to be further apart. By growing the cavity containing layer **16** on a nucleation layer **14** with nucleation islands **14**A, **14**B having large lateral sizes, a density of cavities **16**A, **16**B present in the cavity containing layer **16** can be reduced, which can significantly reduce a number of threading dislocations **19** present in the semiconductor layer **18**.

Furthermore, a temperature and/or V/III ratio used during growth of the cavity containing layer **16** can control a vertical size of the cavities **16**A, **16**B, e.g., by altering a lateral growth rate of the island formations in the cavity containing layer **16**. The presence of the cavities **16**A, **16**B in the cavity containing layer **16** can reduce internal stresses, threading dislocations **19**, and cracks in the semiconductor layers of the structure **10**.

Subsequently, the semiconductor layer **18** can be epitaxially grown directly on the cavity containing layer **16** using any solution. To this extent, growth of the semiconductor layer **18** can be performed at any growth temperature and V/III ratio, configured to result in a coalesced semiconductor layer. In an embodiment, growth of the semiconductor layer **18** uses a lower V/III ratio and a higher growth temperature than those used in growing the cavity containing layer **16**. In an embodiment, the semiconductor layer **18** has a different stoichiometry than the cavity containing layer **16**. A structure **10** including the cavity containing layer **16** with the cavities **16**A, **16**B can reduce stresses associated with heteroepitaxy, which would otherwise be present in the semiconductor layer **18**. As a result, the semiconductor layer **18** will have a reduced number of dislocations **19** and cracks.

As described herein, an embodiment of a semiconductor structure **10** can be fabricated by altering one or more growth conditions (e.g., temperature, pressure, composition, etc.) during formation of the various layers **14**, **16**, **18**. Following is a description of an illustrative method for fabricating a semiconductor structure **10** including layers **14**, **16**, **18** formed of aluminum nitride (AlN)-based materials. While layers **14**, **16**, **18** are described as being distinct layers, when the layers **14**, **16**, **18** are formed of a uniform composition (AlN in the example below), the structure **10** can be considered as having a single layer formed using three distinct growth periods (each of which corresponds to the layers **14**, **16**, **18**). Regardless, it is understood that the example below is only illustrative, and a similar method (but with different ranges for the growth conditions) can be applied to fabricate a semiconductor structure **10** including layers **14**, **16**, **18** formed of any combination of one or more types of compositions, such as any type of $Al_xIn_yB_zGa_{1-x-y-x}N$, where $0 \le x, y, z \le 1$ and $0 \le x+y+z \le 1$, alloy layers. In an illustrative embodiment, the aluminum molar fraction, x, is at least 0.8.

Growth conditions for an AlN-based nucleation layer **14** can be configured to induce three dimensional growth. For example, a growth temperature for the nucleation layer **14** can be in a range between approximately 600° C. and 1300° C. and a V/III ratio can be in a range between approximately 100 and approximately 50000. Use of a higher V/III ratio enhances vertical growth rate and restrains lateral growth. To this extent, the V/III ratio and/or time period for the growth can be adjusted to provide a target characteristic size of the islands in the nucleation layer **14**. Additionally, formation of the nucleation layer **14** can use dissimilar materials including, for example, indium nitride (InN), gallium nitride (GaN), aluminum nitride (AlN), silicon nitride (SiN), any of their alloys, and/or the like.

Growth conditions for an AlN-based cavity containing layer **16** can be configured to induce island growth and the presence of cavities within the cavity containing layer **16**. For example, a growth temperature for the cavity containing layer **16** can be in a range between approximately 800° C. and 1500° C. and a V/III ratio can be more than approximately 100, e.g., in a range between approximately 100 and approximately 10000. The V/III ratio can be adjusted based on a target lateral growth rate, which can adjust a vertical dimension of the cavities. Additionally, additional auxiliary agents (e.g., precursors), such as zinc oxide (ZnO), titanium nitride (TiN), SiN, gallium arsenide (GaAs), aluminum arsenide (AlAs), GaN, InN, and/or the like, can be used to

induce cavities within the cavity containing layer **16**, thereby altering the elastic properties of the cavity containing layer **16**.

Growth conditions for an AlN-based semiconductor layer **18** can be configured to induce coalescence of nucleated islands in the cavity containing layer **16** into a single layer. For example, a growth temperature for the semiconductor layer **18** can be in a range between approximately 1100° C. and 1600° C. and a V/III ratio can be in a range between approximately 1 and approximately 2500. Subsequent growth can result in a fully coalesced, pit-free single-crystalline AlN semiconductor layer. The semiconductor layer **18** can be grown to any desired thickness, e.g., within a range of thicknesses between 1 nanometer and 10000 nanometers. An addition of a small molar fraction of gallium (e.g., one to five percent) within the semiconductor layer **18** can increase the coalescence of the nucleated islands. In an embodiment, a molar fraction of aluminum in the semiconductor layer **18** differs from the molar fraction of aluminum in the cavity containing layer **16** by at least two percent. The pressure used for growing the semiconductor layer **18** can be under 100 torr, and can be kept constant for the entire duration of the growth. The pressure can be balanced by, for example, modifying the amount of hydrogen in the chamber.

Various embodiments of the structure **10** can be achieved by varying one or more of the growth parameters, such as temperature, pressure, V/III ratio, molar concentration of group III elements, and/or the like. Additionally, one or more layers **14**, **16**, **18** can be grown with a flux of one or more additional precursors. Illustrative precursors include: trimethylaluminum, trimethylgallium, trimethylindium, triethylgallium, triethylboron, and/or the like. The precursor fluxes can be delivered at flow rate(s) of at least one micro-moles per minute.

FIG. **3** shows an illustrative structure **20** according to another embodiment. In this case, the structure **20** includes a nucleation layer **24**, which can be epitaxially grown on the substrate **12**, and contain no large scale cavities. In an embodiment, the nucleation layer **24** has a thickness of at least one nanometer. It is understood that the nucleation layer **24** may contain small scale cavities and inhomogeneities due to the nucleation islands **24**A, **24**B forming the layer **24**. As used herein, small scale cavities refers to cavities having a characteristic size (e.g., as determined by a largest lateral cross-section of the cavity) of approximately one nanometer or less.

A cavity containing layer **26** can be grown on the nucleation layer **24** using growth parameters configured to cause the formation of large scale cavities **26**A, **26**B in the cavity containing layer **26**. The cavity containing layer **26** can have any thickness, e.g., in a range between approximately 10 nanometers and 10000 nanometers. The growth conditions for formation of large structures leading to cavity containing layer **26** can be chosen to ensure three-dimensional growth, e.g., by having a high V/III ratio combined with a few hundred degrees Celsius increase in temperature as compared to the temperature used to grow the nucleation layer **24**. The structures are then allowed to coalesce by changing the growth condition to promote two-dimensional growth, which can be accomplished by a reduction of the V/III ratio and a further increase in growth temperature (e.g., by several hundred degrees Celsius).

The cavities **26**A, **26**B can be of various sizes and have various distribution and densities throughout the cavity containing layer **26**. For example, a characteristic size of the large scale cavities **26**A, **26**B can exceed approximately one nanometer. In a more particular illustrative embodiment, a characteristic size of the large scale cavities **26**A, **26**B can range between approximately 10 nanometers and approximately 4000 nanometers. Furthermore, the cavities **26**A, **26**B can have any of various characteristic separations. In an embodiment, a characteristic separation of the cavities **26**A, **26**B (e.g., as determined by a shortest distance between the edges of two adjacent cavities) can range between approximately 5 nanometers and approximately 1 micron (e.g., approximately a few hundred nanometers in an illustrative embodiment). Regardless, as described herein, the characteristic size of the cavities **26**A, **26**B present in the cavity containing layer **26** is determined by the growth parameters, such as growth temperature, pressure, V/III ratio, and/or the like, used during epitaxial growth of the cavity containing layer **26**.

In an embodiment, the growth parameters differ between adjacent layers in the semiconductor structure **20**. For example, each semiconductor layer in a semiconductor structure can be grown at a temperature at least five percent different from the temperature used during growth of the adjacent layer(s). Similarly, each semiconductor layer in a semiconductor structure can be grown at a V/III ratio at least five percent different from the temperature used during growth of the adjacent layer(s). One or more portions of the epitaxial growth described herein can be reapplied and/or applied repeatedly to produce various structures with semiconductor layers and/or superlattices for modifying elastic/plastic characteristics of the semiconductor layers and for releasing internal buildup stresses.

For example, FIG. **4** shows an illustrative structure **30** according to still another embodiment. In this case, the structure **30** includes a nucleation layer **34** grown directly on a substrate **12** and a cavity containing layer **36** grown directly on the nucleation layer **34**. As described herein, growth conditions used during growth of the cavity containing layer **36** can be configured to cause a plurality of cavities **36**A to be present in the layer **36**. As shown in FIG. **2**, a layer grown on the cavity containing layer **36** (e.g., the semiconductor layer **18**) can be grown using growth conditions in which no large scale cavities will be present. Alternatively, as shown in FIG. **4**, a second cavity containing layer **38** is grown directly on the cavity containing layer **36** using growth conditions configured to induce cavities **36**A present in the cavity containing layer **36** (e.g., those present at the top of the cavity containing layer **36**) to extend into the second cavity containing layer **38**. As a result, the second cavity containing layer **38** also includes a plurality of cavities **38**A, which are substantially aligned with cavities **36**A present in the cavity containing layer **36**. Such cavities **38**A can vary in shape and/or size from the cavities **36**A present in the cavity containing layer **36**, e.g., due to use of one or more different growth conditions for the second cavity containing layer **38**.

FIG. **5** shows still another illustrative structure **40** according to an embodiment. In this case, similar to the structure **30** shown in FIG. **4**, a nucleation layer **34** is located directly on a substrate **12**, and a cavity containing layer **36** is located directly on the nucleation layer **34**. However, the structure **40** also includes a second nucleation layer **44**, which is grown on the cavity containing layer **36**, and a second cavity containing layer **46**, which is grown on the second nucleation layer **44**. To this extent, the structure **40** includes multiple nucleation layers **34**, **44** and multiple cavity containing layers **36**, **46**. While the structure **40** is shown including two nucleation layers **34**, **44** and two cavity

containing layers **36**, **46**, it is understood that a structure **40** can include any number of nucleation and/or cavity containing layers.

As illustrated, the cavities **36**A, **46**A present in the respective cavity containing layers **36**, **46** can have different sizes, different densities, and/or the like, depending on the growth conditions used for the layers **36**, **46**. Furthermore, the cavities **36**A, **46**A present in the respective cavity containing layers **36**, **46** may not have any particular alignment and can be misaligned. In an embodiment, a structure **40** includes a cavity containing layer, such as the cavity containing layer **46**, with cavities **46**A having one or more characteristic dimensions (e.g., lateral size, vertical size, density, separation, and/or the like) that differs by at least five percent from the corresponding characteristic dimension(s) of the cavities **36**A present in the previous cavity containing layer **36**.

Since the presence of cavities **36**A, **46**A affects the elastic properties of the corresponding semiconductor layers **36**, **46**, a multilayered semiconductor structure **40** containing multiple semiconductor layers **36**, **46** with variable cavity sizes and densities can allow for control of elastic properties of the semiconductor layers throughout the vertical dimension of the semiconductor structure **40**. Additional control of elastic properties of a semiconductor structure can be provided by a superlattice of semiconductor layers, in which semiconductor layers with cavities are interchanged with semiconductor layers having no large scale cavities.

To this extent, FIGS. **6**A-**6**C show illustrative structures **50**A-**50**C including superlattices **55**A-**55**C, respectively, according to embodiments. Each structure **50**A-**50**C is shown including a substrate **12** and a nucleation layer **54** located thereon, each of which can be configured as described herein. Each superlattice **55**A-**55**C can be grown on the nucleation layer **54**. Each superlattice **55**A-**55**C includes cavity containing layers **56**A-**56**C interchanged with semiconducting layers **58**A-**58**C having no large scale cavities. While the structures **50**A-**50**C are shown as including superlattices **55**A-**55**C, each with six layers, it is understood that a superlattice described herein can include any number of layers. Additionally, it is understood that an embodiment can provide structures with similar layer configurations as shown in FIGS. **6**A-**6**C, which are not part of a superlattice.

Regardless, a superlattice **55**A-**55**C can have any of various possible configurations. For example, as illustrated in FIG. **6**A, each of the layers **56**A-**56**C, **58**A-**58**C in the superlattice **55**A can have substantially similar vertical thicknesses. In an embodiment, the superlattice includes multiple pairs of layers, where each pair includes a cavity containing layer, such as layer **56**A, and an adjacent semiconducting layer **58**A. One or more attributes of one or both layers in a pair can vary from one side of the superlattice to the other side of the superlattice. For example, in FIG. **6**B, the superlattice **55**B includes cavity containing layers **56**A-**56**C having variable thicknesses H throughout the superlattice **55**B. In an embodiment, the thickness H of each cavity containing layer **56**A-**56**C decreases with distance from the nucleation layer **54**. Similarly, as shown in FIG. **6**C, the superlattice **55**C includes semiconducting layers **58**A-**58**C having variable thicknesses H_1 throughout the superlattice **55**C. In an embodiment, the thickness H_1 of each semiconducting layer **58**A-**58**C increases with distance from the nucleation layer **54**. In a more particular illustrative embodiment, the thicknesses H and/or H_1 of layers in adjacent pairs of layers differ by at least five percent.

The various layers described herein can be formed of a substantially uniform composition. Alternatively, a composition of one or more layers can be altered during formation of the layer. For example, FIGS. **7**A and **7**B show illustrative structures **60**A, **60**B according to embodiments. Each structure **60**A, **60**B is shown including a substrate **12** and a nucleation layer **64** located thereon, each of which can be configured as described herein. A series of layers can be grown on the nucleation layer **64**, and include cavity containing layers **66**A-**66**C interchanged with semiconducting layers **68**A-**68**C having no large scale cavities. In an embodiment, the series of layers **66**A-**66**C, **68**A-**68**C forms a superlattice.

In FIG. **7**A, the semiconducting layers **68**A-**68**C in the structure **60**A have compositions that differ from each other by at least one percent. In an embodiment, the compositions of the layers **68**A-**68**C can result in band gaps for the layers **68**A-**68**C that differ from each other by at least two percent. The composition of a group III nitride layer **68**A-**68**C can be determined based on a molar fraction of aluminum in the layer **68**A-**68**C. In an embodiment, the composition of the layers **68**A-**68**C can be chosen to be roughly an average between 1 and a molar fraction of an n-type contact layer in the structure. For example, if the n-type contact layer contains a molar fraction of aluminum, x=0.6, then the average composition of the superlattice layers **68**A-**68**C can be about x=0.8, with the composition of individual superlattice layers chosen to maintain such an average composition. For instance, the superlattice layers can comprise $Al_{0.65}Ga_{0.35}N$ layers interchanged with AlN of an appropriate thickness to yield an average composition of 0.8 within such superlattice.

Furthermore, one or more of the layers **68**A-**68**C can have a graded composition in which a molar fraction of one or more elements in the layer **68**A-**68**C varies throughout the layer **68**A-**68**C. For example, for a group III nitride layer **68**A-**68**C, an aluminum molar fraction can vary between different layers **68**A-**68**C and/or within a layer **68**A-**68**C. To this extent, formation of a group III nitride layer **68**A-**68**C can include a series of growth steps, with each growth step having at least one of: a change in V/III ratio or a change in growth temperature. In an embodiment, such change(s) differ from the V/III ratio and/or growth temperature used in a previous growth step by at least one percent. Alternatively, growth of a group III nitride layer **68**A-**68**C can use a continuously changing (e.g., monotonic, pulsed, or periodic) V/III ratio and/or growth temperature. In an embodiment, a molar fraction of an element, such as an aluminum molar fraction in a graded group III nitride layer, differs by at least one percent from one side of the layer to the opposing side of the layer. The grading can vary, for example, from a high aluminum content closer to an AlN layer on a side of the structure **60**A to a low aluminum content on a side of the structure **60**A closer to an n-type contact layer. Similarly, in FIG. **7**B, the cavity containing layers **66**A-**66**C in the structure **60**B can have compositions that differ from each other by at least one percent and/or have graded compositions. Furthermore, the cavities within each of the cavity containing layers **66**A-**66**C can have a characteristic density (e.g., separation) and/or a characteristic size that differs from those of the cavities in the other cavity containing layers **66**A-**66**C by at least one percent.

While illustrative scenarios of varying attributes (e.g., thicknesses, compositions, cavities, etc.) are separately shown and described in FIGS. **6**A-**6**C and **7**A-**7**B. It is understood that a structure can include any combination of varying attributes. Furthermore, the attributes can be varied in an alternative manner to those shown in FIGS. **6**A-**6**C and **7**A-**7**B. For example, thicknesses can vary in an alternative

direction, vary in a non-sequential manner, and/or the like. Regardless, the attributes of the various layers can be configured to achieve a target distribution of elastic properties of the semiconductor layers in a structure, and as a result, a target distribution of stresses throughout the structure.

The inclusion of one or more cavity containing layers in a semiconductor structure can be combined with other known techniques for manipulating stresses within semiconductor layers. For example, a structure described herein can include semiconductor layers having alternating tensile and compressive stresses combined with cavity containing layers. Tensile and compressive stresses can be varied, for example, by adjusting a V/III ratio used in growing the layers. In an embodiment, a structure described herein can include a set of semiconductor layers grown (e.g., epitaxially) over the one or more cavity containing layers. The set of semiconductor layers can be grown using a set of epitaxial growth periods. For example, a first semiconductor layer can be epitaxially grown over the one or more cavity containing layers that has one of: a tensile stress or a compressive stress. Next, a second semiconductor layer can be epitaxially grown directly over the first semiconductor layer. The second semiconductor layer can have one of: a tensile stress or a compressive stress, whichever is the opposite of the stress of the first semiconductor layer.

A structure can include any number of semiconductor layers of alternating tensile and compressive stresses, which are epitaxially grown on the one or more cavity containing layers. The stresses of the set of semiconductor layers can be controlled using any method. In an embodiment, the stresses of the set of semiconductor layers can be controlled by varying the molar ratio of group V precursors to group III precursors used during growth of each semiconductor layer. For example, the first semiconductor layer can be epitaxially grown using a first molar ratio of group V precursors to group III precursors, while the second semiconductor layer can be epitaxially grown using a second molar ratio of group V precursors to group III precursors that differs from the first molar ratio. In an embodiment, the molar ratios between adjacent semiconductor layers can differ by at least ten percent. In another embodiment, the stress of the set of semiconductor layers can be controlled using differing molar ratios of the semiconductor alloy composition of each semiconductor layer. For example, the first semiconductor layer can have a first molar ratio x of $Al_xGa_{1-x}N$, while the second semiconductor layer can have a second molar ratio y of $Al_yGa_{1-y}N$, where $y \neq x$. In an embodiment, the first molar ratio x and the second molar ratio y (e.g., aluminum molar ratios for adjacent layers) can differ by at least five percent.

The inventors have formed and analyzed structures described herein. FIG. **8** shows an image illustrating surface morphology of an illustrative cavity containing layer according to an embodiment. The cavity containing layer was epitaxially grown using a method described herein. The image was captured using an atomic force microscope (AFM) and shows a five micron by five micron area of the surface. As illustrated, the atomic step shows an extremely flat surface with an RMS of approximately 1.0 Angstroms.

A structure described herein can be implemented as part of any of various types of optoelectronic or electronic devices. An embodiment provides a device formed using group III nitride semiconductor layers. In such a case, controlling stress characteristics can be important for reducing cracks and dislocations. In a more particular embodiment, the device is a light emitting device, such as a diode, in which the control of stress and dislocations within and in proximity of the active layer can provide improved device operation and extended lifetime of the device. Illustrative devices include: a laser diode, a light emitting diode, a photodiode, a deep ultraviolet light emitting diode, a high mobility electron transistor, a field effect transistor, a p-n diode, a Schottky diode, and/or the like.

In an embodiment, a structure described herein, such as the structure **10** (FIG. **2**) or the structure **20** (FIG. **3**), is used as a template for subsequent formation of any of various types of devices. In this case, the template can be formed and subsequently provided for growth of one or more layers of any combination of various types of semiconductor devices on the template. To this extent, the formation of the semiconductor device can include: epitaxial growth of a n-type contact layer on the semiconductor structure (e.g., template); epitaxial growth of an active layer (e.g., including quantum wells and barriers) on the n-type contact layer; and epitaxial growth of a p-type contact layer on the active layer. In another embodiment, the substrate can be removed, e.g., by laser, along the cavity regions to create a structure of free-standing semiconductor layers. During the epitaxial growth of the active layer, the active layer can include a set of quantum wells alternating with a set of barriers. In an embodiment, a quantum well in the active layer can include a bandgap that is lower than the bandgap of a barrier by at least an optical phonon. In the epitaxial growth of the n-type contact layer, the n-type contact layer can comprise $Al_xGa_{1-x}N$, where the molar ratio x is at least 0.3.

In an embodiment, a structure described herein, such as the structure **10** (FIG. **2**) or the structure **20** (FIG. **3**), can be formed on a substrate that is inclined at an angle. For example, FIG. **9** shows an illustrative structure **70** according to an embodiment. The structure **70** is shown including a cavity containing layer **16** and a semiconductor layer **18** located thereon, each of which can be configured as described herein. The cavity containing layer **16** can be grown on a nucleation layer **74** and a substrate **72** as described herein. In this embodiment, the substrate **72** can comprise sapphire, silicon carbide, aluminum nitride, gallium nitride, zinc oxide, lithium gallate, lithium niobate, diamond, silicon, and/or the like. The substrate **72** can include an incline at a (0001) surface **73** at an angle equal to or greater than 0.6 degrees and equal to or less than 3 degrees.

In an embodiment, the angled surface **73** can be inclined in a stepwise manner, a uniform linear manner, a non-uniform varying manner, and/or the like. In the embodiment shown, the angled surface **73** of the substrate **72** is inclined in a stepwise manner so that the surface **73** of the substrate **72** includes a plurality of terraces **71**A, **71**B. In an embodiment, each terrace **71**A, **71**B can include a characteristic height of 1 or several atomic step heights in the range of approximately 2.6 Angstroms (Å) to approximately 30 Å and a characteristic width that is in the range of approximately 20 Å to approximately 10,000 Å. The difference in the height between adjacent terraces **71**A, **71**B is selected to control the incline of the substrate **72** in order to minimize the number of dislocations that propagate through the cavity containing layer **16** to the semiconductor layer **18** (e.g., an active layer). For example, the difference in the height between adjacent terraces **71**A, **71**B can be selected to result in an inclination of approximately 1 to approximately 5 degrees for the surface **73** of the substrate **72**. In an embodiment, the height of the tallest terrace is at most 1000% of the height of the shortest terrace.

The nucleation layer **74** can include a plurality of nucleation islands **14**A, **14**B, as described herein. As described

herein, the size and number of a plurality of nucleation islands **74**A, **74**B in the nucleation layer **74** can be controlled during the growth of the nucleation layer **74**. In an embodiment that includes an inclined substrate, such as the substrate **72** shown in FIG. **9**, the inclined substrate **72** can also control the size and number of nucleation islands. For example, a first nucleation island **74**A located at the end of the incline can include a smaller vertical height than a second nucleation island **74**B located at the start of the incline. However, other embodiments of an angled surface for a substrate are possible. For example, turning to FIG. **10**, a structure **80** can include a substrate **82** that has a symmetric profiled surface **83**. The symmetric profiled surface **83** can allow for symmetric distribution of the dislocation density about the center of a wafer including the structure **80**.

A surface of an inclined substrate according to an embodiment can be engineered through substrate polishing, e.g., by polishing the substrate at a targeted angle. In another embodiment, the surface can be patterned by shallow patterning of the substrate and/or patterning the nucleation layer grown over the substrate. The patterned substrate can lead to similar effects as the polished substrate, but can be engineered through the application of patterning, e.g., using etching techniques. For example, FIGS. **11**A-**11**D show an illustrative method for patterning a substrate according to an embodiment. In FIG. **11**A, a substrate **12** can be masked by a set of masking regions **86** formed of silicon dioxide (SiO_2) or other similar masking materials known in the art. Next, in FIG. **11**B, the substrate **12** can be etched in areas **88** between each of the set of masking regions **86** and, in FIG. **11**C, the masking regions **86** can be removed. In FIG. **11**D, a layer, such as the nucleation layer **84**, can be grown on the substrate **82**. This method of patterning and etching can be used to produce an inclined surface on the substrate **82**.

In another embodiment, a surface of the substrate does not need to be etched. For example, FIGS. **12**A-**12**D show an illustrative method for patterning a substrate according to an embodiment. In FIG. **12**A, similar to the approach in FIG. **11**A, the substrate **12** is masked by a set of masking regions **86**. However, in FIG. **12**B, a semiconductor layer **89** can be epitaxially grown in the areas between each of the set of masking regions **86**. In an embodiment, the semiconductor layer **89** can comprise an AlN buffer layer. By epitaxially growing the semiconductor layer **89** between each the set of masking regions **86**, the surface of the substrate **12** would not need to be etched. In FIG. **12**C, the set of masking regions **86** are removed and the nucleation layer **84** can be grown over the substrate **12** and the semiconductor layer **89** as shown in FIG. **12**D. In an embodiment, the nucleation layer **84** and the semiconductor layer **89** can be formed of the same material, but grown using different parameters (e.g., temperature, V/III ratio, growth rate, and/or the like) in order to have different properties.

Regardless of the method used to pattern the substrate surface, the direction and forms of the set of masking regions **86** can be selected to have edge directions that are aligned with the crystal planes of the subsequently grown semiconductor layer (e.g., semiconductor layer **89** and the nucleation layer **84**). The alignment of the set of masking regions **86** allows for further control of the twist (e.g., the alignment of the set of nucleation islands) and inclination of the set of nucleation islands in the nucleation layer **84**.

In an embodiment, substrate polishing can be combined with substrate patterning. For example, turning to FIG. **13**, an illustrative structure **130** according to an embodiment is shown. In this embodiment, substrate polishing can be used to form a set of inclined areas **132**A, **132**B on the substrate **12**, while substrate patterning (e.g., the methods shown in FIGS. **11**A-**11**D and FIG. **12**A-**12**D) can be used to form a patterned area **134**. A structure that includes both a patterned and an inclined substrate can allow for more control over growth.

The surface of a substrate can be patterned to have a surface of any configuration. For example, FIGS. **14**A-**14**C show illustrative top views of a substrate **92** according to embodiments. The surface of the substrate **92** can include sets of regions **98**A-**98**C and each region **98**A-**98**C on the substrate **92** corresponds to an area on the surface of the substrate **92**. Each set of regions **98**A-**98**C can correspond to a depth of depression that is etched into the surface of the substrate **92**. The sets of regions **98**A-**98**C can be configured on the surface of the substrate **92** in any manner in order to form the plurality of terraces **71**A, **71**B (FIG. **9**). To this extent, the sets of regions **98**A-**98**C can be periodically or aperiodically distributed in depth and dimension on the surface of the substrate **92**. For example, in FIG. **14**A, the sets of regions **98**A-**98**C are ordered in rows. In FIG. **14**B, the sets of regions **98**A-**98**C are configured so that the depth of depression into the surface of the substrate **92** can increase or decrease towards the center of the substrate **92**. In FIG. **14**C, the sets of regions **98**A-**98**C form a random pattern. In an embodiment, the set of regions **98**A-**98**C can also correspond to an elevation of the surface of the substrate **92** (e.g., depending on the method of patterning the substrate). In this case, each area of each region **98**A-**98**C can have a different height than the height of each immediately adjacent area. Furthermore, the sets of regions **98**A-**98**C can include any shape and size. FIG. **14**D shows an illustrative profile of a substrate, while FIG. **14**E shows an illustrative profile of a patterned substrate.

As described herein, the substrate can include a plurality of steps at the growth surface. Turning now to FIG. **15**, an illustrative portion of a patterned surface, such as the patterned surface **73** (FIG. **9**), is shown. The patterned surface **73** of a substrate according to an embodiment can include a plurality of steps that can either be atomic **75** or bunched **77**. If the inclined surface **73** of a substrate is only a few tenths of a degree or a few hundredths of a degree, then the formation of steps is rare, and only a few atomic steps may be present over several microns of a lateral length of the surface **73**. As the angle of the inclined surface **73** increases, the formation and frequency of the atomic steps **75** can increase. At some specific angle of the inclined surface **73**, the formation of bunched steps **77** can become thermodynamically beneficial. In an embodiment, a bunched step **77** is higher, and can be wider, than an atomic step **75**. If the angle of the inclined surface **73** continues to increase, the formation of bunched steps **77** along the surface **73** can become more frequent.

It is understood that the formation and frequency of atomic steps **75** and bunched steps **77** can depend on the thermodynamic parameters of the method of patterning the substrate **72**, such as the temperature, growth rate, the morphology of the buffer layer, which can be epitaxially grown over the set of atomic steps **75** of the substrate **72**, the lattice mismatch stress between the substrate **72** and an epitaxially grown semiconductor layer, the tensile stresses associated with epitaxial growth of the nucleation layer, and/or the like. In an embodiment, a substrate including an inclined surface **73** will have one bunched step **77** per micron, which would allow for dislocation inclination and interaction without causing any significant number of new dislocations. Using the parameter of one bunched step per micron, the offcut angle of the inclined surface **73** can be

selected. Furthermore, there is a relationship between the offcut angle and the atomic step width. In an embodiment, the relationship between the atomic step height (H), the atomic step width (W_a), and offcut angle α can correspond to the following equation: α=a tan(H/W_a)*180/π, where the atomic step height H for an atomic step is 2.6 Å. Illustrative values for the offcut angles as a function of the atomic step width are shown in the following table:

TABLE 1

offcut angle α	atomic step width W_a (A)	# of steps in 1 micron	step bunched
0.015	10000	1	no
0.15	1000	10	no
0.15-1.5	1000-100	10-100	step bunch starts
1.5	100	100	yes

When the atomic step number exceeds a threshold number, step bunching can begin to occur on the inclined surface. As illustrated, when the offcut angle α increases into the range of 0.15-1.5, step bunching begins to occur. For a bunched step, the equation for the offcut angle α is slightly modified: α=arctan (H/W_b), where H is the total height between two bunched steps and W_b, as shown in FIG. **15**, is the width between two bunched steps. That is H=2.6*(N+A), where N is the number of atomic steps in the bunched step and A is the number of atomic steps between the bunched steps. In the embodiment shown in FIG. **15**, each bunched step **77** has a height equivalent to approximately 6 atomic steps (N=6) and there are 4 atomic steps (A=4) between the bunched steps **77**. The determination of the number of bunched steps within a layer per unit of lateral length can be performed using scanning electron microscopy (SEM) or transmission electron microscopy (TEM) techniques.

A structure described herein can include multiple inclined sections. For example, FIG. **16** shows a portion of an illustrative structure **200** including a substrate **202** with a plurality of inclined surface sections **204**. In an embodiment, each of the plurality of inclined surface sections **204** can include an angle α that is greater than or equal to 0.6 degree and less than or equal to 3 degrees. In an embodiment, the length (D) of each section **204** is selected to be approximately $D\sim1/(N_d)^{1/2}$, where N_d is the dislocation density in a typical semiconductor layer epitaxially grown on a flat substrate. For example, when a typical dislocation density is approximately 10^8 cm^{-2}, the length of a section **204** is approximately 1 micron. It is understood that this proposed selection for the length D for each section **204** is only an approximation and that the length of each section **204** can vary in the range of 0.1D to 10D.

It is understood that a structure as described herein can include a substrate that is patterned to comprise a plurality of protruding regions, which is disclosed in U.S. Pat. No. 8,981,403, which issued on 17 Mar. 2015 and is hereby incorporated by reference. Furthermore, a structure as described herein can include a partially relaxed semiconductor layer, which is disclosed in U.S. patent application Ser. No. 14/150,930, filed on 9 Jan. 2014, which is hereby incorporated by reference. In an embodiment, the structure can include a partially relaxed semiconductor layer that is grown over a cavity containing layer. The partially relaxed semiconductor layer can be formed using a three-dimensional (3D) growth technique to facilitate the formation of dislocations. For example, the 3D growth technique can include a set of growth conditions that result in an initial formation of islands of the material used for the partially relaxed semiconductor layer at the interface of an adjacent layer. The set of growth conditions can include a high growth temperature, a high growth rate, and/or the like. During the growth of the partially relaxed semiconductor layer, the islands can coalesce and form a dislocation rich layer with dislocations present at the island boundaries.

In one embodiment, the invention provides a method of designing and/or fabricating a circuit that includes one or more of the devices designed and fabricated as described herein (e.g., including one or more devices fabricated using a semiconductor structure described herein). To this extent, FIG. **17** shows an illustrative flow diagram for fabricating a circuit **126** according to an embodiment. Initially, a user can utilize a device design system **110** to generate a device design **112** for a semiconductor device as described herein. The device design **112** can comprise program code, which can be used by a device fabrication system **114** to generate a set of physical devices **116** according to the features defined by the device design **112**. Similarly, the device design **112** can be provided to a circuit design system **120** (e.g., as an available component for use in circuits), which a user can utilize to generate a circuit design **122** (e.g., by connecting one or more inputs and outputs to various devices included in a circuit). The circuit design **122** can comprise program code that includes a device designed as described herein. In any event, the circuit design **122** and/or one or more physical devices **116** can be provided to a circuit fabrication system **124**, which can generate a physical circuit **126** according to the circuit design **122**. The physical circuit **126** can include one or more devices **116** designed as described herein.

In another embodiment, the invention provides a device design system **110** for designing and/or a device fabrication system **114** for fabricating a semiconductor device **116** as described herein. In this case, the system **110**, **114** can comprise a general purpose computing device, which is programmed to implement a method of designing and/or fabricating the semiconductor device **116** as described herein. Similarly, an embodiment of the invention provides a circuit design system **120** for designing and/or a circuit fabrication system **124** for fabricating a circuit **126** that includes at least one device **116** designed and/or fabricated as described herein. In this case, the system **120**, **124** can comprise a general purpose computing device, which is programmed to implement a method of designing and/or fabricating the circuit **126** including at least one semiconductor device **116** as described herein.

In still another embodiment, the invention provides a computer program fixed in at least one computer-readable medium, which when executed, enables a computer system to implement a method of designing and/or fabricating a semiconductor device as described herein. For example, the computer program can enable the device design system **110** to generate the device design **112** as described herein. To this extent, the computer-readable medium includes program code, which implements some or all of a process described herein when executed by the computer system. It is understood that the term "computer-readable medium" comprises one or more of any type of tangible medium of expression, now known or later developed, from which a stored copy of the program code can be perceived, reproduced, or otherwise communicated by a computing device.

In another embodiment, the invention provides a method of providing a copy of program code, which implements some or all of a process described herein when executed by a computer system. In this case, a computer system can process a copy of the program code to generate and transmit,

for reception at a second, distinct location, a set of data signals that has one or more of its characteristics set and/or changed in such a manner as to encode a copy of the program code in the set of data signals. Similarly, an embodiment of the invention provides a method of acquiring a copy of program code that implements some or all of a process described herein, which includes a computer system receiving the set of data signals described herein, and translating the set of data signals into a copy of the computer program fixed in at least one computer-readable medium. In either case, the set of data signals can be transmitted/received using any type of communications link.

In still another embodiment, the invention provides a method of generating a device design system **110** for designing and/or a device fabrication system **114** for fabricating a semiconductor device as described herein. In this case, a computer system can be obtained (e.g., created, maintained, made available, etc.) and one or more components for performing a process described herein can be obtained (e.g., created, purchased, used, modified, etc.) and deployed to the computer system. To this extent, the deployment can comprise one or more of: (1) installing program code on a computing device; (2) adding one or more computing and/or I/O devices to the computer system; (3) incorporating and/or modifying the computer system to enable it to perform a process described herein; and/or the like.

The foregoing description of various aspects of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are possible. Such modifications and variations that may be apparent to an individual in the art are included within the scope of the invention as defined by the accompanying claims.

What is claimed is:

1. A structure comprising:

a cavity containing layer, wherein the cavity containing layer is formed of a semiconductor material, has a thickness greater than two monolayers, and has a plurality of cavities, and wherein the plurality of cavities have a characteristic size of at least one nanometer and a characteristic separation of at least five nanometers; and

a semiconductor layer immediately adjacent to the cavity containing layer, wherein a molar fraction of a semiconductor element in the semiconductor layer differs from a molar fraction of the semiconductor element in the cavity containing layer by at least two percent.

2. The structure of claim **1**, further comprising:

a substrate; and

a nucleation layer located on the substrate, wherein the nucleation layer has a thickness of at least one nanometer, and wherein the cavity containing layer is located directly on the nucleation layer.

3. The structure of claim **2**, wherein a surface of the substrate adjacent to the nucleation layer is inclined at an angle.

4. The structure of claim **3**, wherein the angle is equal to or greater than 0.6 degrees and equal to or less than 3 degrees.

5. The structure of claim **2**, wherein a surface of the substrate adjacent to the nucleation layer is patterned to include a plurality of regions, wherein each region corresponds to an etched area of the substrate having a different height than each immediately adjacent etched area of the substrate.

6. The structure of claim **5**, wherein the plurality of regions are ordered so that the surface of the substrate declines towards a center of the substrate.

7. The structure of claim **3**, wherein the surface of the substrate includes a plurality of atomic steps and a plurality of bunched steps.

8. The structure of claim **3**, wherein the surface of the substrate includes a plurality of inclined surface sections.

9. The structure of claim **2**, wherein the semiconductor layer is formed of a plurality of layers, wherein a first layer of the plurality of layers includes one of: a tensile or a compressive stress and a second layer of the plurality of layers includes one of: a tensile or a compressive stress that is opposite of the first layer.

10. The structure of claim **9**, wherein the first layer includes a first molar ratio of group V precursors to group III precursors and the second layer includes a second molar ratio of group V precursors to group III precursors different from the first molar ratio, and a difference between the first molar ratio and the second molar is at least ten percent.

11. The structure of claim **9**, wherein the first layer comprises $Al_xGa_{1-x}N$ and the second layer comprises $Al_yGa_{1-y}N$, where x and y differ by at least five percent.

12. A device comprising:

an aluminum nitride nucleation layer, wherein the nucleation layer has a thickness of at least one nanometer and comprises a plurality of nucleation islands;

a cavity containing layer located directly on the nucleation layer, wherein the cavity containing layer is formed of a semiconductor material, has a thickness greater than two monolayers, and has a plurality of cavities, and wherein the plurality of cavities have a characteristic size of at least one nanometer and a characteristic separation of at least five nanometers; and

a semiconductor layer immediately adjacent to the cavity containing layer, wherein a molar fraction of a semiconductor element in the semiconductor layer differs from a molar fraction of the semiconductor element in the cavity containing layer by at least two percent.

13. The device of claim **12**, further comprising a substrate immediately adjacent to the nucleation layer, wherein a surface of the substrate adjacent to the nucleation layer is inclined at an angle equal to or greater than 0.6 degrees and equal to or less than 30 degrees.

14. The device of claim **12**, wherein the cavity containing layer comprises aluminum nitride.

15. The device of claim **12**, wherein a surface of a substrate adjacent to the nucleation layer is patterned to include a plurality of regions, wherein each region corresponds to an etched area of the substrate having a different height than each immediately adjacent etched area of the substrate.

16. The device of claim **12**, wherein the cavity containing layer has a thickness in a range of 1 micron to 10 micron.

17. The device of claim **12**, wherein the semiconductor layer is formed of a plurality of layers, wherein a first layer includes one of: a tensile or a compressive stress and a second layer includes one of: a tensile or a compressive stress that is opposite of the first layer.

18. The device of claim **17**, wherein the first layer includes a first molar ratio of group V precursors to group III precursors and the second layer includes a second molar ratio of group V precursors to group III precursors, and a difference between the first molar ratio and the second molar is at least ten percent.

19. A method comprising:

fabricating a semiconductor structure, wherein the fabricating includes:

growing an aluminum nitride nucleation layer on a substrate, wherein the nucleation layer has a thickness of at least one nanometer;

forming a cavity containing layer directly on the nucleation layer, wherein the cavity containing layer has a thickness greater than two monolayers and a plurality of cavities; and

forming a semiconductor layer directly on the cavity containing layer, wherein a molar fraction of a semiconductor element in the semiconductor layer differs from a molar fraction of the semiconductor element in cavity containing layer by at least two percent.

20. The method of claim **19**, wherein the fabricating further comprises:

patterning a surface of the substrate, wherein the patterning includes:

masking a plurality of regions on the substrate; and

etching the substrate between the plurality of regions, such that the surface of the substrate is inclined at an angle that is equal to or greater than 0.6 degrees and equal to or less than 3 degrees.

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