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(54) **PLASMA PROCESSING APPARATUS**
(71) Applicant: **TOKYO ELECTRON LIMITED**,
Tokyo (JP)
(72) Inventors: **Akinori Miyata**, Miyagi (JP); **Shigeru Senzaki**, Miyagi (JP); **Hirofumi Haga**, Miyagi (JP); **Nobutaka Nakao**, Miyagi (JP)
(73) Assignee: **TOKYO ELECTRON LIMITED**,
Tokyo (JP)

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CPC .. **H01L 21/67017** (2013.01); **H01J 37/32449** (2013.01); **H01J 37/32834** (2013.01); **H01L 21/6719** (2013.01)

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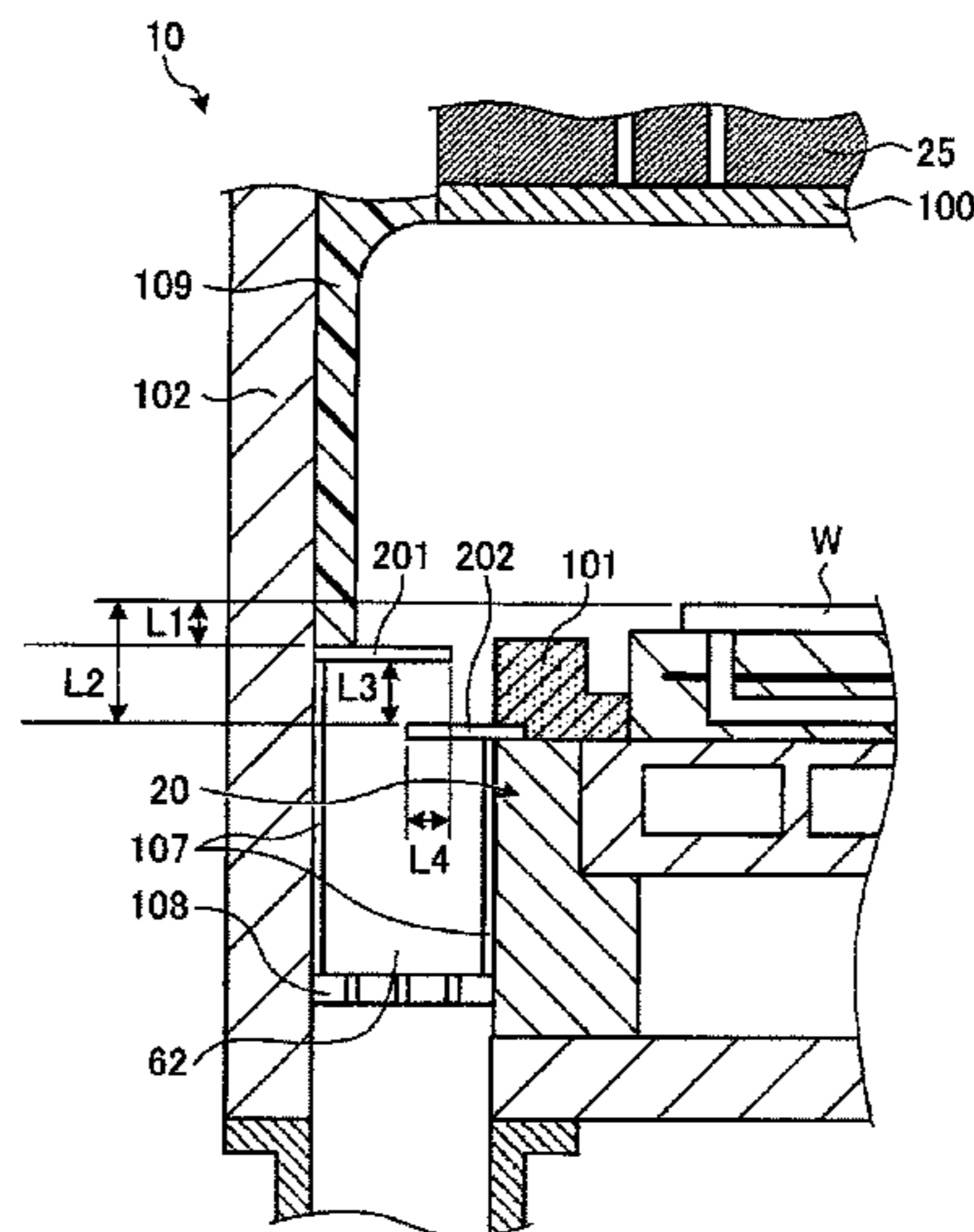
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Primary Examiner — Rudy Zervigon
(74) *Attorney, Agent, or Firm* — Rothwell, Figg, Ernst & Manbeck, P.C.

(57) **ABSTRACT**
A plasma processing apparatus includes: a processing container; a processing gas supply unit; a mounting table configured to mount a to-be-processed substrate thereon; an upper electrode provided above the mounting table; a plasma generation unit configured to supply a high frequency power to generate plasma of the processing gas; an exhaust flow path formed by a side wall of the processing container and a side surface of the mounting table; a conductive rectification plate configured to adjust a flow of the processing gas discharged to outside of the processing container; a conductor arranged in the exhaust flow path at a position higher than the rectification plate and lower than the to-be-processed substrate to face at least a part of the upper electrode. A distance of the conductor in the height direction in relation to the to-be-processed surface of the substrate is set to be within a predetermined range.

3 Claims, 7 Drawing Sheets



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FIG. 1

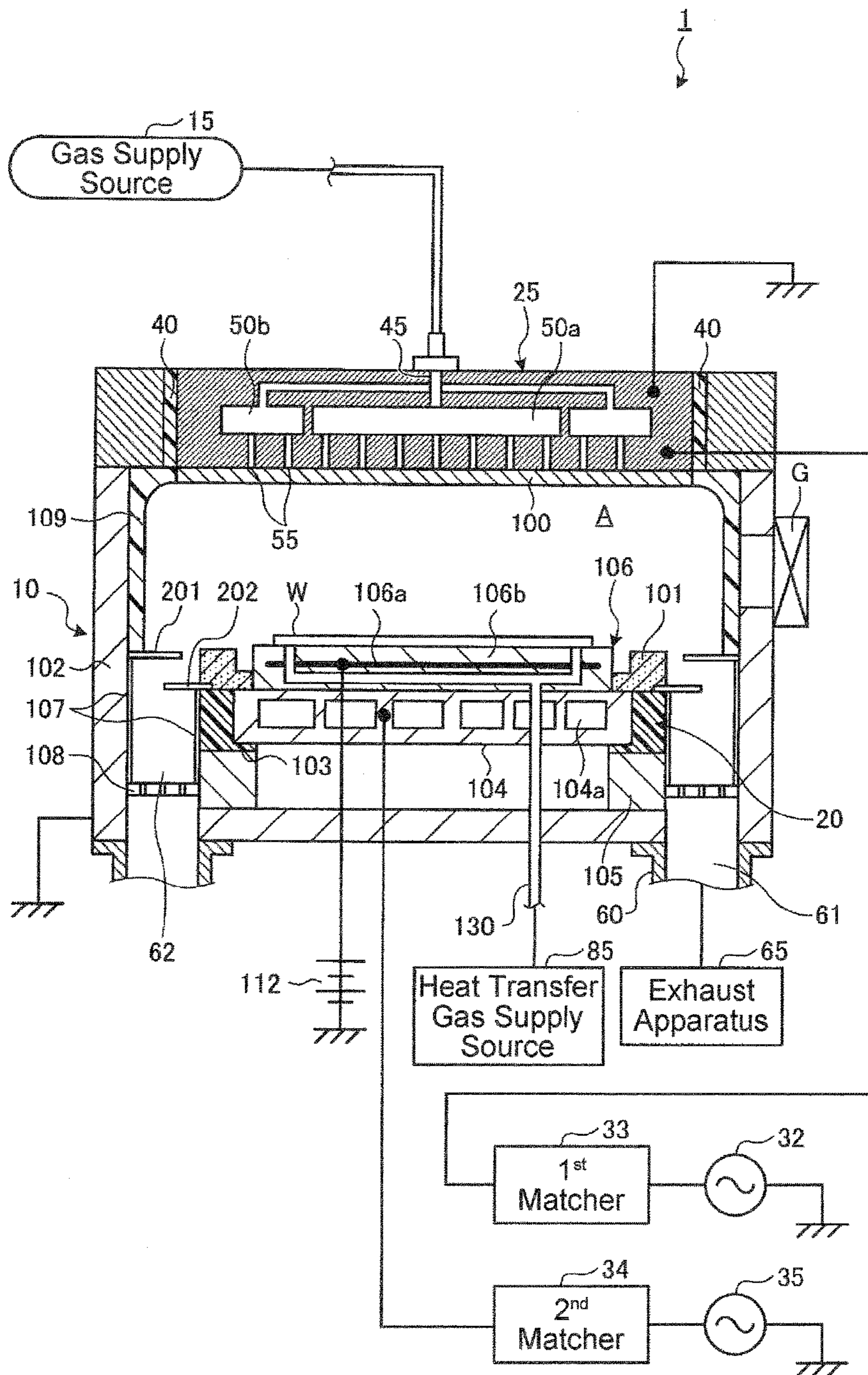


FIG. 2A

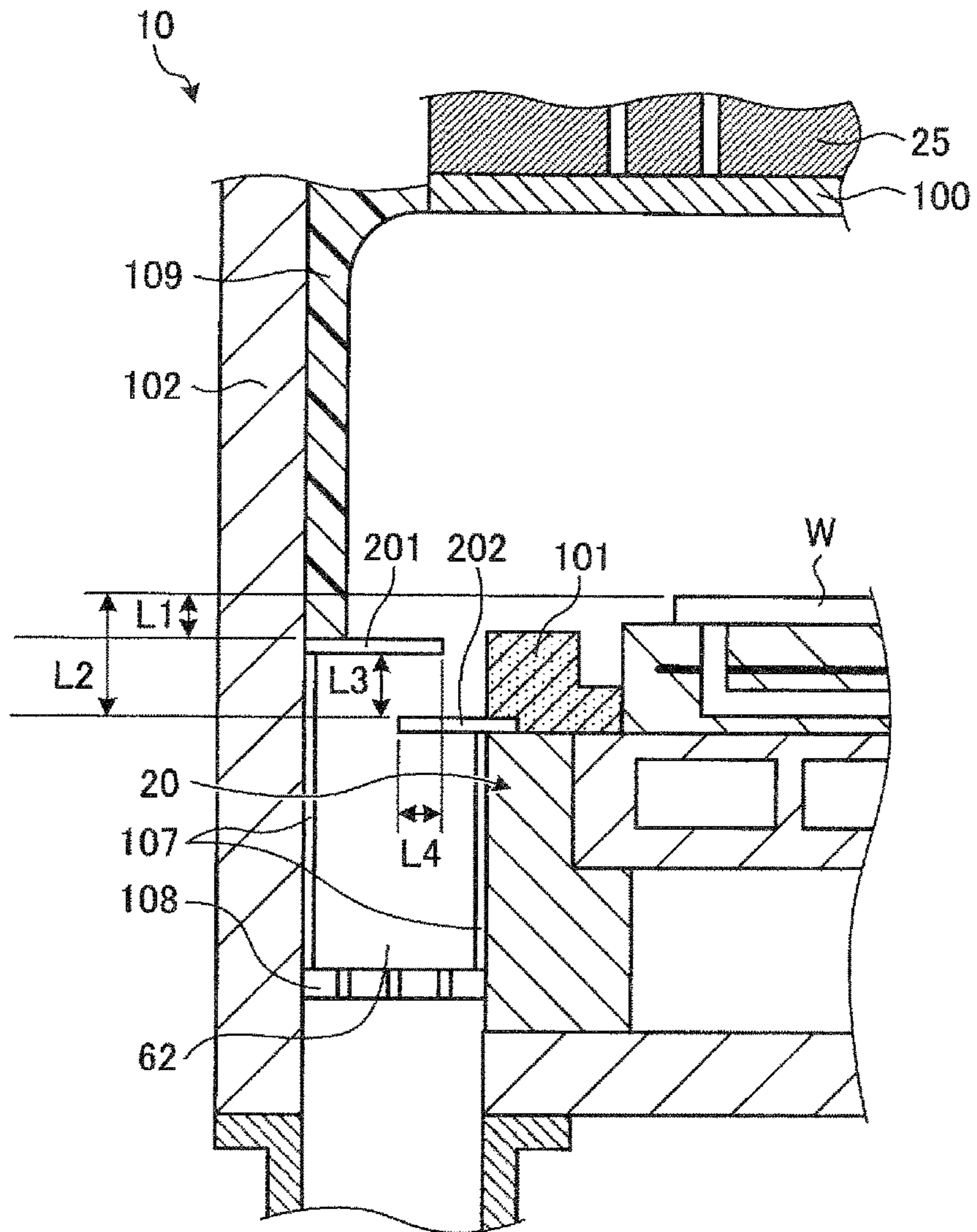


FIG.2B

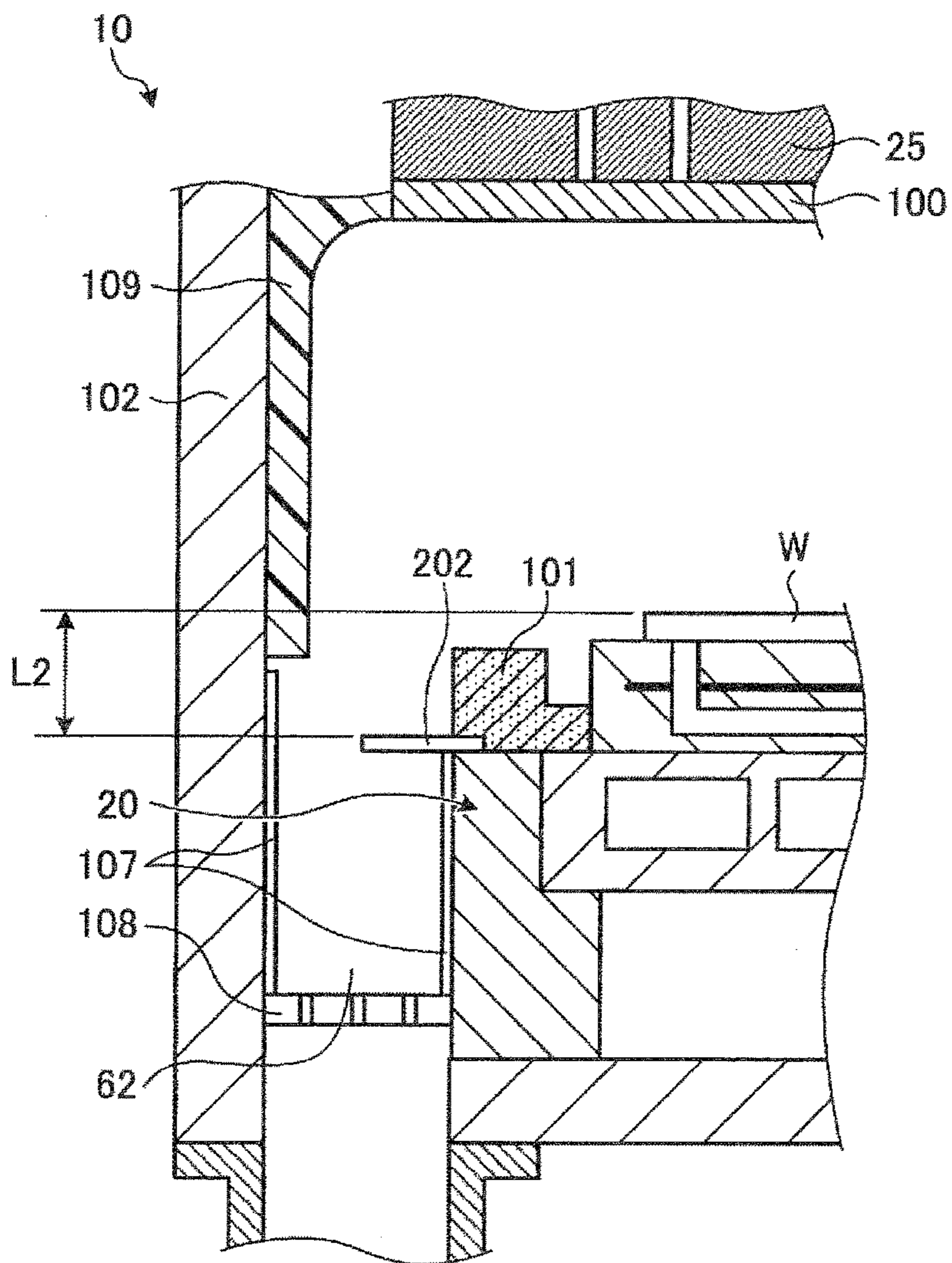


FIG.3

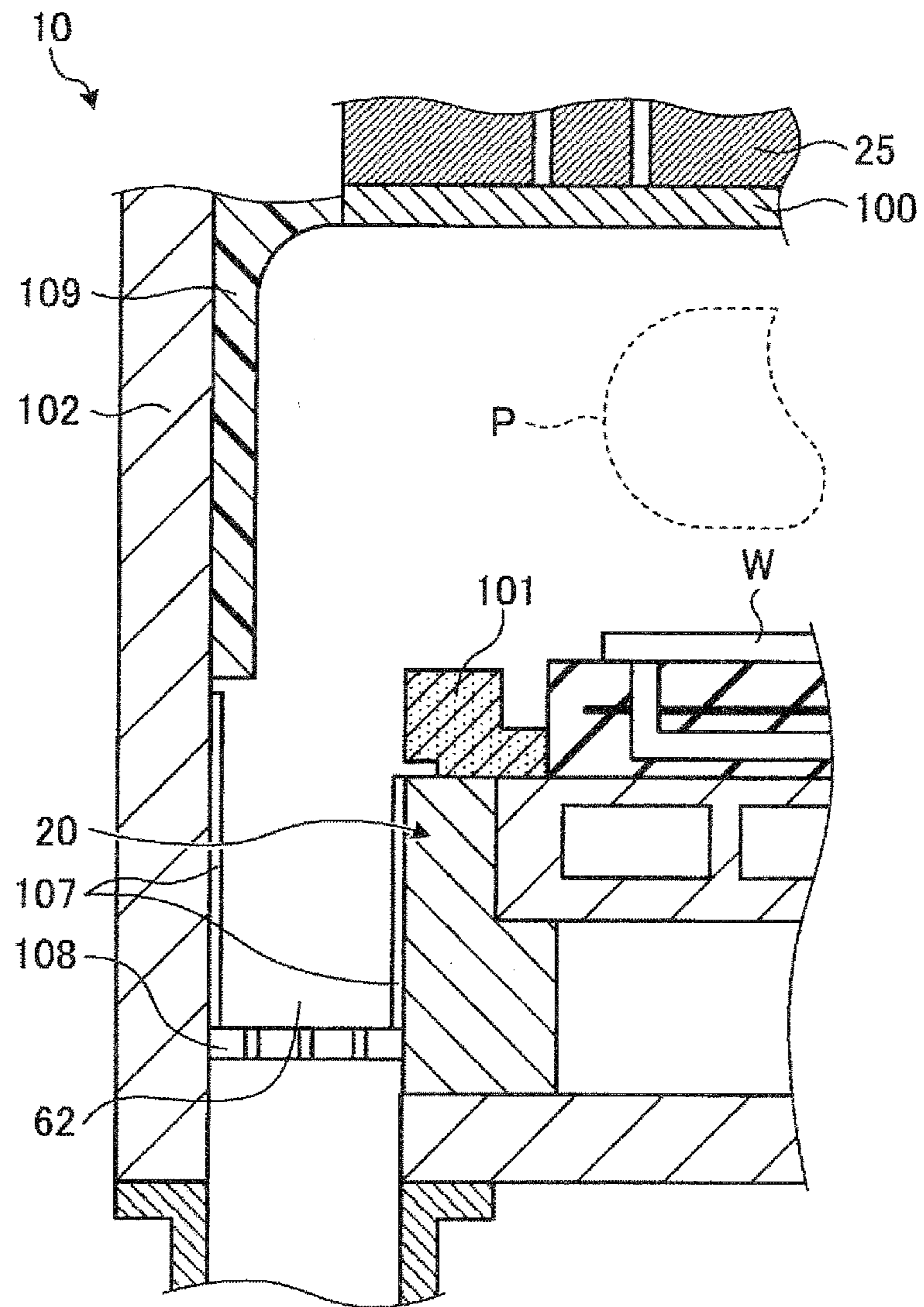


FIG. 4

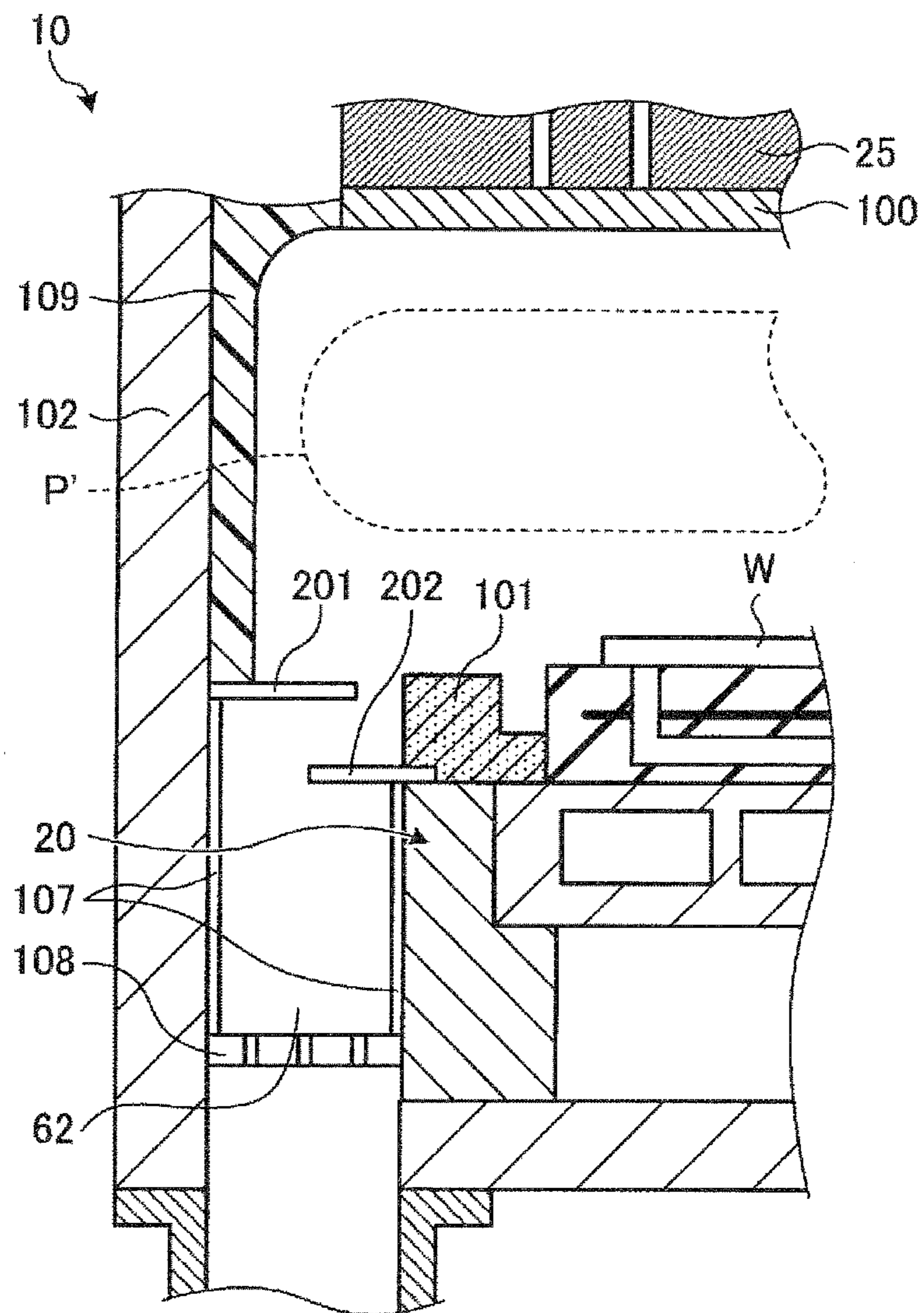
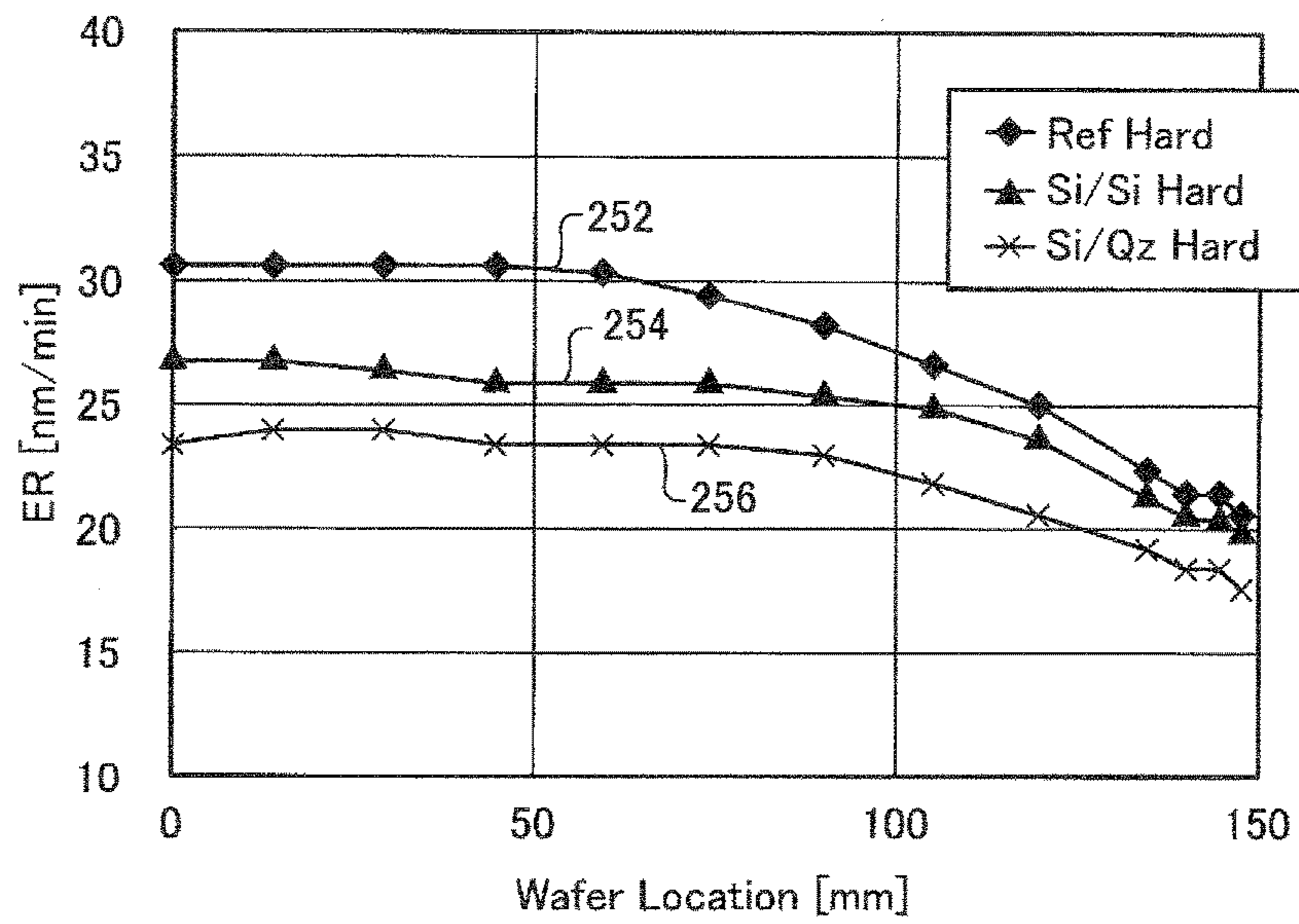
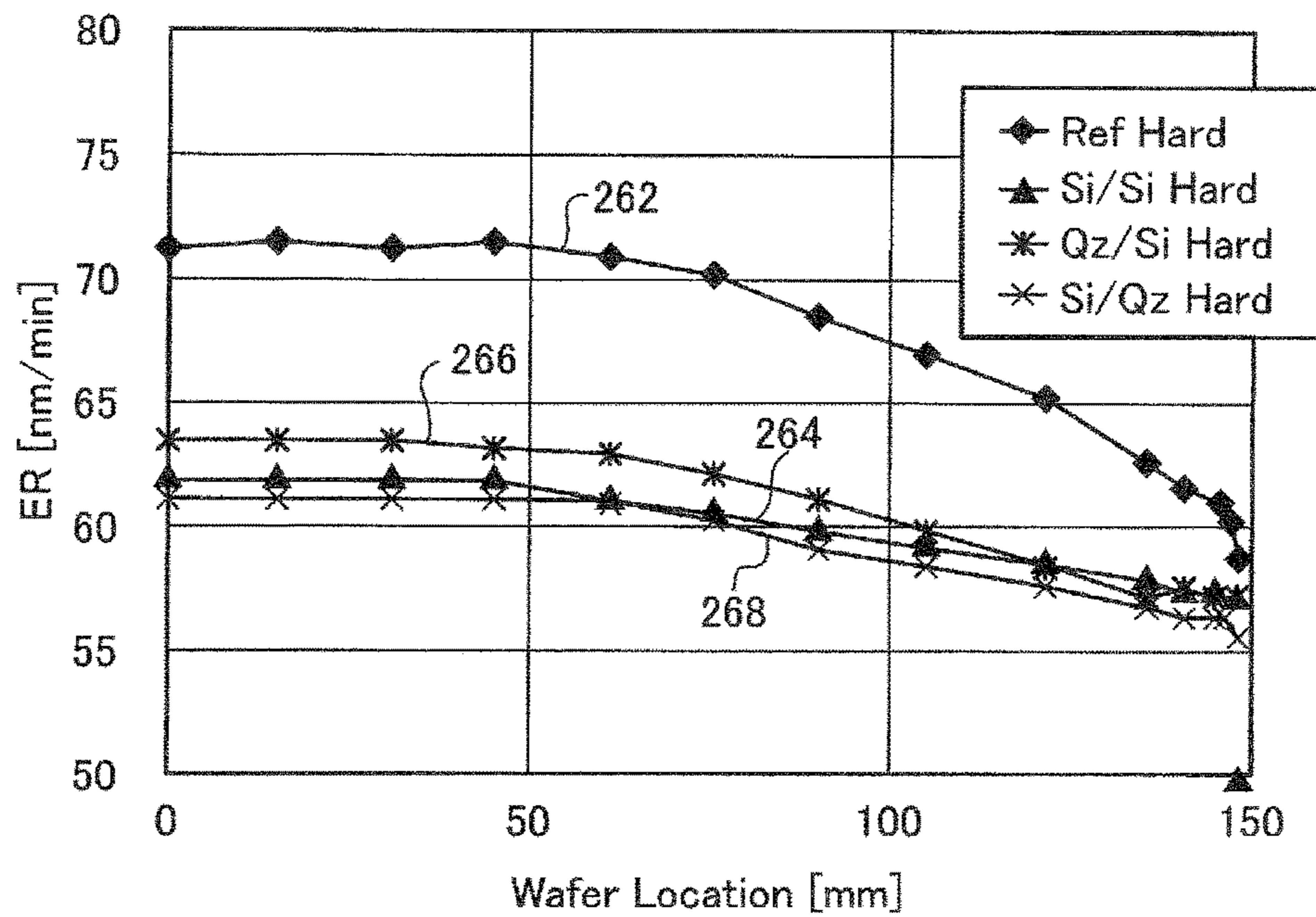


FIG.5



| | |
|-------|--------------------|
| Ref | 25.9nm/min ± 23.8% |
| Si/Si | 23.9nm/min ± 17.9% |
| Si/Qz | 21.2nm/min ± 19.4% |

FIG. 6



| | |
|-------|--------------------|
| Ref | 66.1nm/min ± 10.9% |
| Si/Si | 59.3nm/min ± 4.4% |
| Qz/Si | 59.7nm/min ± 7.3% |
| Si/Qz | 58.6nm/min ± 5.8% |

PLASMA PROCESSING APPARATUS**CROSS-REFERENCE TO RELATED APPLICATIONS**

This application is based on and claims priority from Japanese Patent Application No. 2014-254376, filed on Dec. 16, 2014, with the Japan Patent Office, the disclosure of which are incorporated herein in its entirety by reference.

TECHNICAL FIELD

Various aspects and exemplary embodiments disclosed herein relate to a plasma processing apparatus.

BACKGROUND

In a semiconductor manufacturing process, a plasma processing apparatus that executes a plasma processing for the purpose of, for example, deposition of a thin film or etching has been widely used. As the plasma processing apparatus, a plasma chemical vapor deposition (CVD) apparatus that performs a deposition processing of a thin film or a plasma etching apparatus that performs an etching processing may be exemplified.

The plasma processing apparatus includes a processing container configured to define a plasma processing space, a mounting table configured to mount a to-be-processed substrate thereon within the processing container, an upper electrode provided above the mounting table, and a gas supply system configured to introduce a processing gas required for a plasma reaction into the processing container. In addition, in order to turn the processing gas within the processing chamber into plasma, the plasma processing apparatus includes, for example, a plasma generation mechanism configured to supply electronic energy such as for example, microwaves or RF waves. In addition, in the plasma processing apparatus, an exhaust flow path for exhausting the processing gas to the outside of the processing container is formed by the side wall of the processing container and the side surface of the mounting table. In the exhaust flow path, a baffle plate is provided to adjust the flow of the processing gas. The baffle plate functions to rectify the gas within the processing container so as to cause the gas to be uniformly exhausted. In addition, the baffle plate usually has conductivity.

However, in the plasma processing apparatus, it has been known that electrons in the generated plasma are drawn to the conductive baffle plate and produce a reaction product on the surface of the baffle plate. Thus, a conductor is provided in the exhaust flow path in order to block the electrons. For example, there is a prior art in which a ground electrode made of a conductor is arranged in the exhaust flow path at a position that is higher than the baffle plate and lower than a to-be-processed substrate mounted on the mounting table so as to cause the electrons in the plasma to escape to the ground electrode. See, for example, Japanese Patent Laid-Open No. 2007-258471.

SUMMARY

A plasma processing apparatus according to the present disclosure includes: a processing container; a gas supply unit configured to supply a processing gas into the processing container; a mounting table provided within the processing container, and configured to mount a to-be-processed substrate thereon; an upper electrode provided at an upper side

of the mounting table; a plasma generation unit configured to supply a high frequency power to at least one of the upper electrode and the mounting table to generate plasma of the processing gas within the processing container; an exhaust flow path formed by a side wall of the processing container and a side surface of the mounting table; a conductive rectification plate provided in the exhaust flow path, and configured to adjust a flow of the processing gas that is discharged to outside of the processing container by the exhaust flow path; a conductor arranged in the exhaust flow path at a position higher than the rectification plate and lower than the to-be-processed substrate mounted on the mounting table to face at least a part of the upper electrode. A distance of the conductor in a height direction in relation to a to-be-processed surface of the to-be-processed substrate is set to be within a predetermined range.

The foregoing summary is illustrative only and is not intended to be in any way limiting. In addition to the illustrative aspects, embodiments, and features described above, further aspects, embodiments, and features will become apparent by reference to the drawings and the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a vertical cross-sectional view illustrating a plasma processing apparatus according to an exemplary embodiment.

FIG. 2A is a view illustrating an exemplary installation aspect of conductors.

FIG. 2B is a view illustrating a state in which a conductor is only provided on a side surface of a mounting table.

FIG. 3 is a view illustrating a state in which plasma is generated in a plasma processing apparatus of a comparative example.

FIG. 4 is a view illustrating a state in which plasma is generated in the plasma processing apparatus of the present exemplary embodiment.

FIG. 5 is a view illustrating etching rates in a case where organic films of wafers were etched by a predetermined processing gas.

FIG. 6 is a view illustrating an etching rate in a case where oxide films of wafers were etched by a predetermined processing gas.

DETAILED DESCRIPTION

In the following detailed description, reference is made to the accompanying drawings, which form a part hereof. The illustrative embodiments described in the detailed description, drawing, and claims are not meant to be limiting. Other embodiments may be utilized, and other changes may be made without departing from the spirit or scope of the subject matter presented here.

In the prior art described above, an electrode facing the upper electrode does not exist in the exhaust flow path. Therefore, the generated plasma is concentrated to the central portion of the to-be-processed substrate mounted on the mounting table so that the etching rate in the central portion of the substrate is high and the etching rate in the peripheral portion is lowered. As a result, there is a problem in that the uniformity of the etching rate of the to-be-processed substrate is deteriorated.

In one exemplary embodiment, a plasma processing apparatus disclosed herein includes: a processing container; a gas supply unit configured to supply a processing gas into the processing container; a mounting table provided within the

processing container, and configured to mount a to-be-processed substrate thereon; an upper electrode provided at an upper side of the mounting table; a plasma generation unit configured to supply a high frequency power to at least one of the upper electrode and the mounting table to generate plasma of the processing gas within the processing container; an exhaust flow path formed by a side wall of the processing container and a side surface of the mounting table; a conductive rectification plate provided in the exhaust flow path, and configured to adjust a flow of the processing gas that is discharged to outside of the processing container by the exhaust flow path; a conductor arranged in the exhaust flow path at a position higher than the rectification plate and lower than the to-be-processed substrate mounted on the mounting table to face at least a part of the upper electrode. A distance of the conductor in a height direction in relation to a to-be-processed surface of the to-be-processed substrate is set to be within a predetermined range.

In addition, in one exemplary embodiment of the plasma processing apparatus disclosed herein, the conductor is provided in the exhaust flow path on at least one of the side wall side of the processing container and the side surface side of the mounting table.

According to various aspects and exemplary embodiments of the present disclosure, a plasma processing apparatus is realized which is capable of improving in-plane uniformity of etching of a to-be-processed substrate.

Hereinafter, various exemplary embodiments will be described in detail with reference to the accompanying drawings. The same or corresponding parts in each of the drawings will be denoted by the same reference numerals.

[Overall Configuration of Plasma Processing Apparatus]

First, an overall configuration of a plasma processing apparatus **1** according to an exemplary embodiment will be described with reference to FIG. **1**. FIG. **1** is a vertical cross-sectional view illustrating a plasma processing apparatus according to an exemplary embodiment. In the present exemplary embodiment, by way of an example, a parallel flat plate type plasma processing apparatus **1** will be described in which a lower electrode (mounting table **20**) and an upper electrode **25** (shower head) are arranged to face each other within the processing container **10**, and a gas is supplied to the inside of the processing container **10** from the upper electrode **25**.

As illustrated in FIG. **1**, the plasma processing apparatus **1** includes, for example, a processing container **10** that is formed of a conductive material such as, for example, aluminum having a surface subjected to an alumite treatment (anodizing treatment), and a gas supply source **15** configured to supply a gas into the processing container **10**. The processing container **10** is grounded. The processing container **10** defines a plasma processing space A therein. In the inner wall of the processing container **10**, a portion facing the plasma processing space A is covered with a volatile material **109** such as, for example, silicon or quartz. The processing container **10** is an example of the processing container. The gas supply source **15** supplies a specific gas in each plasma processing step such as, for example, etching or cleaning. The gas supply source **15** is an example of the gas supply unit.

The processing container **10** is electrically grounded, and includes a mounting table **20** therein so as to mount a wafer W thereon. The wafer W is an example of the to-be-processed substrate, and is applicable to, for example, a flat panel substrate. The mounting table **20** functions as a lower electrode. In the ceiling portion, an upper electrode **25** is provided to face the mounting table **20**.

On the top surface of the mounting table **20**, an electrostatic chuck **106** is provided to electrostatically attract the wafer W. The electrostatic chuck **106** is formed in a structure in which a chuck electrode **106a** is sandwiched between insulation members **106b**. A direct current (DC) voltage source **112** is connected to the chuck electrode **106a**, and when a DC voltage is applied to the chuck electrode **106a** from the DC voltage source **112**, the wafer W is attracted to the electrostatic chuck **106** by a Coulomb force. On the peripheral edge of the electrostatic chuck **106**, a focus ring **101** formed of, for example, silicon, is disposed in order to enhance the in-plane uniformity of etching.

The mounting table **20** is supported by an electrode (lower electrode) **104** of a conductor such as, for example, aluminum. Within the lower electrode **104**, a coolant flow path **104a** is formed. In the coolant flow path **104a**, for example, cooling water is circulated as a proper coolant so as to cool the wafer W.

A heat transfer gas supply source **85** causes a heat transfer gas such as, for example, helium gas (He) or argon gas (Ar), to pass through a gas supply line **130** so as to supply the heat transfer gas to the space between the electrostatic chuck **106** and the wafer W. With this configuration, the electrostatic chuck **106** is subjected to a temperature control by the cooling water circulated in the coolant flow path **104a**, and the heat transfer gas supplied to the rear surface of the wafer W.

The mounting table **20** is supported on the support member **105** via a holding member **103**. The support member **105** is formed of an insulating material, and places the lower electrode **104** in a floating state by insulating it from the processing container **10**.

A first high frequency power supply **32** is electrically connected to the upper electrode **25** via a first matcher **33**. A second high frequency power supply **35** is electrically connected to the lower electrode **104** via a second matcher **34**. The first high frequency power supply **32** supplies a first high frequency power of for example, 60 MHz to the upper electrode **25**. The second high frequency power supply **35** supplies a second high frequency power of, for example, 13.56 MHz to the lower electrode **104**. The high frequency power connection type may be a lower two-frequency type or any other type, besides the upper and lower two-frequency type.

The first and second matchers **33**, **34** are intended to match a load impedance to internal (or output) impedances of the first and second high frequency power supplies **32**, **35**, respectively, and function to make the internal impedances of the first and second high frequency power supplies **32**, **35** apparently coincide with the load impedance when plasma is generated within the processing container **10**.

The first and second high frequency power supplies **32**, **35** are examples of the power supplies that apply the energy of electromagnetic waves to the processing container **10**. As another example of the power supply that applies the energy of electromagnetic waves to the processing container **10**, microwave plasma and inductively coupled plasma (ICP) may be exemplified.

The upper electrode **25** is attached to the ceiling portion of the processing container **10** via a shield ring **40** that covers the periphery of the upper electrode **25**. The upper electrode **25** is electrically grounded. A portion of the upper electrode **25** that faces the plasma processing space A is covered with a volatile material **100** such as, for example, silicon or quartz.

The upper electrode **25** includes a gas inlet **45** formed therein so as to introduce the gas from the gas supply source

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15. In addition, the upper electrode **25** is provided with a center side diffusion chamber **50a** and an edge side diffusion chamber **50b** therein. The center side diffusion chamber **50a** and the edge side diffusion chamber **50b** are branched from the gas inlet **45** and diffuse the gas.

A plurality of gas supply holes **55** are formed in the upper electrode **25** to supply the gas from the diffusion chambers **50a**, **50b** to the inside of the processing container **10**. Each gas supply hole **55** is arranged to supply the gas to the space between the wafer **W** mounted on the lower electrode and the upper electrode **25**.

The gas from the gas supply source **15** is supplied to the diffusion chambers **50a**, **50b** through the gas inlet **45**, diffused in the diffusion chambers **50a**, **50b** to be distributed to respective gas supply holes **55**, and then introduced into the processing container **10** toward the lower electrode from the gas supply holes **55**. With this configuration, the upper electrode **25** also functions as a gas shower head that supplies a gas.

An annular exhaust flow path **62** is formed between the side wall **102** of the processing container **10** and the side surface of the mounting table **20**. The inner peripheral surface of the exhaust flow path **62** is covered with a sprayed coating **107** that contains yttrium oxide. The exhaust flow path **62** is provided with a rectification plate (baffle plate) **108**. The rectification plate (baffle plate) **108** adjusts the flow of the processing gas discharged to the outside of the processing container **10** by the exhaust flow path **62**. The rectification plate (baffle plate) **108** is formed of a conductive material such as, for example, a metal. An exhaust pipe **60** that forms an exhaust port **61** is provided in the bottom portion of the exhaust flow path **62**. An exhaust apparatus **65** is connected to the exhaust pipe **60**. The exhaust apparatus **65** decompresses the processing space within the processing container **10** to a predetermined vacuum degree with a vacuum pump (not illustrated).

In the exhaust flow path **62**, a conductor **201** and a conductor **202** are provided on the side wall **102** of the processing container **10** and the side surface of the mounting table **20**, respectively. The conductor **201** and the conductor **202** are arranged annularly to be orthogonal to the exhaust flow path **62**. The conductor **201** and the conductor **202** are formed of a conductor such as, for example, silicon. In addition, the conductors **201** and **202** may be formed of, for example, polysilicon, SiC, or glassy carbon. The installation aspect of the conductor **201** and the conductor **202** will be described below.

On the side wall of the processing container **10**, a gate valve **G** is provided. The gate valve **G** opens/closes a carry-in/out port when a wafer **W** is carried into or carried out from the processing container **10**.

A plasma processing is performed on a wafer **W** by the plasma processing apparatus **1** configured as described above. For example, in the case where an etching processing is performed, the opening/closing of the gate valve **G** is controlled first, and the wafer **W** is carried into the processing container **10** and mounted on the mounting table **20** by electrostatic attraction. Subsequently, an etching gas is introduced, and the first high frequency power and the second high frequency power are supplied to the upper electrode **25** and the lower electrode **104**, respectively, so that plasma is generated. A desired processing such as, for example, the plasma etching, is performed on the wafer **W** by the generated plasma. After the processing, the opening/closing of the gate valve **G** is controlled, and the wafer **W** is carried out from the processing container **10**.

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Next, descriptions will be made on the installation aspect of the conductor **201** and the conductor **202** illustrated in FIG. 1. FIG. 2A is a view illustrating an exemplary installation aspect of the conductors. As illustrated in FIG. 2A, the conductor **201** and the conductor **202** are arranged in the exhaust flow path **62** at a position that is higher than the baffle plate **108** and lower than the wafer **W** mounted on the mounting table **20** to face at least a part of the upper electrode **25**. In addition, the conductor **201** and the conductor **202** may be arranged to overlap with each other in the central area of the exhaust flow path **62**. More specifically, the conductor **201** is provided on the side wall **102** of the processing container **10**, and arranged at a position that is higher than the baffle plate **108** and lower than the wafer **W** mounted on the mounting table **20** to face at least a part of the upper electrode **25**. The distance **L1** between the conductor **201** and the to-be-processed surface of the wafer **W** along the height direction in relation to the to-be-processed surface of the wafer **W** may be, for example, 1 mm to 70 mm. The distance **L1** is set to be within a range where the conductor **201** is made to function as a ground electrode for the upper electrode **25**. In addition, the conductor **202** is provided on the side surface of the mounting table **20**, and arranged at a position that is higher than the baffle plate **108** and lower than the wafer **W** mounted on the mounting table **20** to face at least a part of the upper electrode **25**. The distance **L2** between the conductor **202** and the to-be-processed surface of the wafer **W** along the height direction in relation to the to-be-processed surface of the wafer **W** may be 15 mm to 85 mm. The distance **L2** is set to be within a range where the conductor **202** is made to function as a ground electrode for the upper electrode **25**. In addition, the distance **L3** between the conductor **201** and the conductor **202** along the height direction in relation to the to-be-processed surface of the wafer **W** may be 20 mm to 40 mm.

In addition, the conductor **201** and the conductor **202** may be arranged to partially overlap with each other when viewed in the height direction in relation to the to-be-processed surface of the wafer **W**. By this, it is possible to avoid the infiltration of the particles existing in the exhaust flow path **62** into the plasma processing space **A** of the processing container **10**. In the case where the conductor **201** and the conductor **202** are arranged to partially overlap with each other, the ratio of the width **L4** of the overlapping portion between the conductor **201** and the conductor **202** in relation to the conductor **201** or the conductor **202** may be set to 1.5% to 22.5%, preferably 1.5% to 15%. When the conductor **201** and the conductor **202** are arranged in the exhaust flow path **62** within the above-mentioned ranges, respectively, the exhaust within the processing container **10** can be uniformly and efficiently performed. In addition, because the plasma region generated within the processing container **10** is uniformly widened while increasing an anode/cathode (A/C) ratio, the processing on the wafer **W** can be uniformly performed.

In addition, while the foregoing description has illustrated an example in which the conductor **201** and the conductor **202** are arranged to partially overlap with each other when viewed in the height direction in relation to the to-be-processed surface of the wafer **W**, the conductor **201** and the conductor **202** may be arranged not to partially overlap with each other.

Here, the function of the conductor **201** and the conductor **202** as a ground electrode will be described.

First, as a comparative example, descriptions will be made on a plasma processing apparatus that does not include a conductor in the exhaust flow path **62**. FIG. 3 is a view

illustrating a state in which plasma is generated in the plasma processing apparatus of the comparative example. The plasma processing apparatus of the comparative example is different from the plasma processing apparatus **1** of the present exemplary embodiment in that it does not include a conductor in the exhaust flow path **62**, and the other features are the same as those of the plasma processing apparatus **1** of the present exemplary embodiment. Thus, in FIG. **3** to be described below, the same components as those of the present exemplary embodiment will be denoted by the same reference numerals.

The plasma processing apparatus of the comparative example does not include a conductor in the exhaust flow path **62**. In other words, in the exhaust flow path **62**, the upper electrode **25** and a counter electrode are positioned far away from each other (while the baffle plate is apparently illustrated as a counter electrode, a function as the counter electrode is not acting). For this reason, as illustrated in FIG. **3**, in the case where plasma P is generated within the processing container **10**, the generated plasma P wraps around in the direction of the conductive baffle plate **108** provided in the exhaust flow path **62**, and is concentrated to a position above the central portion of the wafer W mounted on the mounting table **20**. As a result, the difference between the etching rate corresponding to the central portion of the wafer W and the etching rate corresponding to the peripheral edge of the wafer W may increase, which may deteriorate the uniformity of the etching rate of the wafer W.

With respect to this, descriptions will be made on the plasma processing apparatus **1** of the present exemplary embodiment. FIG. **4** is a view illustrating a state in which plasma is generated in the plasma processing apparatus of the present exemplary embodiment. In the plasma processing apparatus **1** of the present exemplary embodiment, the conductor **201** and the conductor **202** are arranged in the exhaust flow path **62** at a position that is higher than the baffle plate **108** and lower than the wafer W mounted on the wafer W to face at least a part of the upper electrode **25**. For example, etching was performed by setting the distances L1, L2, L3, and L4 to 30 mm, 66 mm, 30.5 mm, and 6.5 mm, respectively, so that the conductor **201** and the conductor **202** were set within the range that allows the conductor **201** and the conductor **202** to function as a ground electrode for the upper electrode **25**.

As illustrated in FIG. **4**, in the case where plasma P' is generated within the processing container **10**, the generated plasma P' expands to the upper side of the central portion of the wafer W and the upper side of the conductor **201** and the conductor **202** without warping around in the direction of the conductive baffle plate **108** provided in the exhaust flow path **62**. As a result, the difference between the etching rate corresponding to the central portion of the wafer W and the etching rate for the peripheral edge of the wafer W is suppressed so that the in-plane uniformity of the wafer W is improved.

In addition, while FIG. **2A** illustrates an example in which the conductor **201** is provided on the side wall **102** of the processing container **10**, and the conductor **202** is provided on the side surface of the mounting table **20**, the technique disclosed herein is not limited thereto. For example, only the conductor **201** may be provided on the side wall **102** of the processing container **10**, or only the conductor **202** may be provided on the side surface of the mounting table **20**. For example, a conductor may be provided in an annular shape in the exhaust flow path **62** on at least one of the side wall **102** of the processing container **10** and the side surface of the mounting table **20** such that the conductor is orthogonal to

the cross-section of the exhaust flow path **62**. FIG. **2B** illustrates, as an example, a state in which the conductor **201** is omitted and only the conductor **202** is provided on the side surface of the mounting table **20**.

In addition, in terms of increasing an anode/cathode (A/C) ratio, the conductors may be provided on both the side wall **102** of the processing container **10** and the side surface of the mounting table **20** in the exhaust flow path **62**, respectively. The A/C ratio increases as the area of the anode side increases in relation to the area of the cathode side. When the conductors are provided on both the side wall **102** of the processing container **10** and the side surface of the mounting table **20**, respectively, in the exhaust flow path **62**, the apparent area of the anode side increases so that the A/C ratio increases. On the contrary, a sputtering force to the side wall **102** of the processing container **10**—the anode—decreases, and as a result, the consumption of a member is suppressed.

Next, descriptions will be made on an effect (etching rate) obtained by the plasma processing apparatus of the present exemplary embodiment. FIG. **5** is a view representing etching rates when organic films of wafers were etched by using a predetermined processing gas.

In FIG. **5**, the horizontal axis represents a diametric location [mm] on a wafer W with reference to the position of the center of the wafer W, and the vertical axis represents an etching rate [nm/min] in the case where an organic film on the wafer

W was etched by a predetermined processing gas.

In addition, in FIG. **5**, Graph **252** is a graph representing an etching rate in the case where an organic film of a wafer W was etched by using a plasma processing apparatus of the comparative example which did not include a conductor in the exhaust flow path **62**. Graph **254** is a graph illustrating an etching rate in the case where an organic film of a wafer W was etched by using the plasma processing apparatus **1** of the present exemplary embodiment in which the conductor **201** and the conductor **202** were provided on the side wall **102** of the processing container **10** and the side surface of the mounting table **20** in the exhaust flow path **62**, respectively. In addition, in Graph **254**, the conductor **201** and the conductor **202** were arranged such that the distances L1, L2, L3, and L4 were set to 30 mm, 66 mm, 30.5 mm, and 6.5 mm, respectively. Graph **256** is a graph representing an etching rate in the case where an organic of a wafer W was etched by using the plasma processing apparatus **1** of the present exemplary embodiment in which the conductor **202** was provided on the side surface of the mounting table **20** in the exhaust flow path **62** and a dielectric was provided on the side wall **102** of the processing container **10** instead of the conductor **201**. In addition, the dielectric provided instead of the conductor **201** is formed by a dielectric such as, for example, quartz. In addition, in Graph **256**, the conductor **201** and the dielectric were arranged such that the distances L1, L2, L3, and L4 were set to 30 mm, 66 mm, 30.5 mm, and 6.5 mm, respectively.

As represented by Graph **252** in FIG. **5**, in the plasma processing apparatus of the comparative example which did not include a conductor in the exhaust flow path **62**, the average etching rate along the diametric direction of the wafer W was 25.9 nm/min, and the deviation from the mean etching rate was $\pm 23.8\%$. Both the average etching rate and the deviation did not satisfy a predetermined allowable specification.

Whereas, as represented by Graph **254** in FIG. **5**, in the plasma processing apparatus **1** of the present exemplary embodiment in which the conductor **201** and the conductor

202 were provided on the side wall 102 of the processing container 10 and the side surface of the mounting table 20 in the exhaust flow path 62, respectively, the average etching rate along the diametric direction of the wafer W was 23.9 nm/min, and the deviation from the average etching rate was $\pm 17.9\%$. Both the average etching rate and the deviation satisfied a predetermined allowable specification. In addition, as represented by Graph 256 in FIG. 5, in the plasma processing apparatus 1 of the present exemplary embodiment in which the conductor 202 was provided on the side surface of the mounting table 20 in the exhaust flow path 62 and the dielectric plate was provided on the side wall 102 of the processing container 10 instead of the conductor 201, the average etching rate along the diametric direction of the wafer W was 21.2 nm/min, and the deviation from the average etching rate was $\pm 19.4\%$. Both the average etching rate and the deviation satisfied a predetermined allowable specification. That is, in the case where a conductor was provided on at least one of the side wall 102 of the processing container 10 and the side surface of the mounting table 20 in the exhaust flow path 62, the uniformity of the etching rate of the wafer W was improved as compared to the case where no conductor was provided in the exhaust flow path 62. This is thought to have been resulted from the fact that in the case where the conductor is provided on at least one of the side wall 102 of the processing container 10 and the side surface of the mounting table 20 in the exhaust flow path 62, the plasma is spread to the upper side of the central portion of the wafer W and to the upper side of the conductor 201 and the conductor 202 by the function of the conductor as a ground electrode.

FIG. 6 is a view illustrating an etching rate in a case where an oxide film of a wafer was etched by a predetermined processing gas. In FIG. 6, the horizontal axis represents a diametric position [mm] of a wafer W with reference to the central position thereof, and the vertical axis represents an etching rate [nm/min] in a case where an oxide film of a wafer W was etched by a predetermined processing gas.

In addition, in FIG. 6, Graph 262 is a graph that represents an etching rate in the case where an oxide film of a wafer W was etched by using a plasma processing apparatus of a comparative example in which no conductor was provided in the exhaust flow path 62. Graph 264 is a graph that represents an etching rate in the case where an oxide film of a wafer W was etched by using the plasma processing apparatus 1 of the present exemplary embodiment in which the conductor 201 and the conductor 202 were provided on the side wall 102 of the processing container 10 and the side surface of the mounting table 20 in the exhaust flow path 62, respectively. In addition, in Graph 264, the conductor 201 and the conductors 202 were arranged such that the distances L1, L2, L3, and L4 were set to 30 mm, 66 mm, 30.5 mm, and 6.5 mm, respectively. Graph 266 is a graph that represents an etching rate in the case where an oxide film of a wafer W was etched by using a plasma processing apparatus 1 of the present exemplary embodiment in which the conductor 201 was provided on the side wall 102 of the processing container 10, and the dielectric was provided on the side surface of the mounting table 20, instead of the conductor 202. In addition, the dielectric that replaced the conductor 202 was formed of a dielectric material such as, for example, quartz. In addition, in Graph 266, the conductor 201 and the dielectric were arranged such that the distances L1, L2, L3, and L4 were set to 30 mm, 66 mm, 30.5 mm, and 6.5 mm, respectively. Graph 268 is a graph that represents an etching rate in the case where an oxide film of a wafer W was etched by using the plasma processing apparatus 1 of

the present exemplary embodiment in which the conductor 202 was provided on the side surface of the mounting table 20 in the exhaust flow path 62, and in addition, the dielectric was provided on the side wall 102 of the processing container 10 instead of the conductor 201. In addition, the dielectric that replaces the conductor 201 is formed of a dielectric material such as, for example, quartz. In addition, in Graph 268, the dielectric and the conductor 202 were arranged such that the distances L1, L2, L3, and L4 were set to 30 mm, 66 mm, 30.5 mm, and 6.5 mm, respectively.

As represented by Graph 262 of FIG. 6, in the plasma processing apparatus of a comparative example that did not include a conductor in the exhaust flow path 62, the average etching rate along the diametric direction of the wafer W was 66.1 nm/min, and the deviation from the average etching rate was $\pm 10.9\%$. Both the average etching rate and the deviation did not satisfy the predetermined allowable specifications.

On the contrary, as represented by Graph 264 in FIG. 6, in the plasma processing apparatus 1 of the present exemplary embodiment in which the conductor 201 and the conductor 202 were provided on the side wall 102 of the processing container 10 and the side surface of the mounting table 20 in the exhaust flow path 62, respectively, the average etching rate according to the diametric direction of the wafer W was 59.3 nm/min, and the deviation from the average etching rate was $\pm 4.4\%$. Both the average etching rate and the deviation satisfied the predetermined allowable specifications. In addition, as represented by Graph 266 in FIG. 6, in the plasma processing apparatus 1 of the present exemplary embodiment in which the conductor 201 was provided on the side wall 102 of the processing container 10, and a dielectric plate was provided on the side surface of the mounting table 20 instead of the conductor 202, the average etching rate according to the diametric direction of the wafer W was 59.7 nm/min and the deviation from the average etching rate was $\pm 7.3\%$. Both the average etching rate and the deviation satisfied the predetermined allowable specification. In addition, as represented by Graph 268 in FIG. 6, in the plasma processing apparatus 1 of the present exemplary embodiment in which the conductor 202 was provided on the side surface of the mounting table 20 in the exhaust flow path 62 and the dielectric plate was provided on the side wall 102 of the processing container 10, instead of the conductor 201, the average etching rate along the diametric direction of the wafer W was 58.6 nm/min and the deviation from the average etching rate was $\pm 5.8\%$. Both the average etching rate and the deviation satisfied the predetermined allowable specifications. That is, in the case where a conductor was provided on at least one of the side wall 102 of the processing container 10 and the side surface of the mounting table 20 in the exhaust flow path 62, the uniformity of the etching rate of the wafer W was improved as compared to a case in which no conductor is provided in the exhaust flow path 62. It is believed that this is resulted from the fact that in the case where the conductor is provided on at least one of the side wall 102 of the processing container 10 and the side surface of the mounting table 20 in the exhaust flow path 62, plasma is spread to the upper side of the central portion of the wafer W and to the upper side of the conductor 201, 202 due to the function of the conductor as a ground electrode.

As described above, in the plasma processing apparatus 1 of the present exemplary embodiment, the conductor 201 and the conductor 202 were arranged in the exhaust flow path 62 to face at least a part of the upper electrode 25, and the distance of the conductors in the height direction in

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relation to the to-be-processed surface of the wafer W was set to be within a predetermined range. By this, when plasma P' is generated within the processing container 10, the generated plasma P' is spread to the upper side of the central portion of the wafer W and to the upper side of the conductor 201 and the conductor 202 without warping around in the direction of the conductive baffle plate 108 provided in the exhaust flow path 62. As a result, a difference between the etching rate that corresponds to the central portion of the wafer W and the etching rate that corresponds to the peripheral edge of the wafer W is suppressed such that the uniformity of the etching rate of the wafer W can be improved.

From the foregoing, it will be appreciated that various exemplary embodiments of the present disclosure have been described herein for purposes of illustration, and that various modifications may be made without departing from the scope and spirit of the present disclosure. Accordingly, the various exemplary embodiments disclosed herein are not intended to be limiting, with the true scope and spirit being indicated by the following claims.

What is claimed is:

1. A plasma processing apparatus comprising:

a processing container;

a gas supply unit configured to supply a processing gas into the processing container;

an electrostatic chuck located within the processing container, and configured to mount a to-be-processed substrate thereon;

a mounting table located below the electrostatic chuck and is configured to support the electrostatic chuck;

an upper electrode located at an upper side of the electrostatic chuck;

a plasma generation unit configured to supply a high frequency power to at least one of the upper electrode

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and the mounting table to generate plasma of the processing gas within the processing container;
an exhaust flow path formed by a side wall of the processing container and a side surface of the mounting table;

an electrically conductive rectification plate located in the exhaust flow path, and configured to adjust a flow of the processing gas that is discharged to outside of the processing container by the exhaust flow path; and

a first electrical conductor and a second electrical conductor arranged in the exhaust flow path at a position higher than the rectification plate and lower than the to-be-processed substrate to face at least a part of the upper electrode, a distance of the first electrical conductor and the second electrical conductor in a height direction in relation to a to-be-processed surface of the to-be-processed substrate being set to be within a predetermined range,

wherein the first electrical conductor is located on the side surface of the mounting table and separate from the side wall of the processing container,

wherein the second electrical conductor is located on the side wall of the processing container and separate from the side surface of the mounting table, and

wherein the first electrical conductor and the second electrical conductor are arranged to overlap with each other in a central area of the exhaust flow path.

2. The plasma processing apparatus of claim 1, wherein the first electrical conductor is located at a position lower than the first electrical conductor.

3. The plasma processing apparatus of claim 1, wherein a distance between the first electrical conductor and the second electrical conductor along the height direction is within a range of 20 mm to 40 mm.

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