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(54) **PIXEL DRIVER CIRCUIT WITH
LOAD-BALANCE IN CURRENT MIRROR
CIRCUIT**

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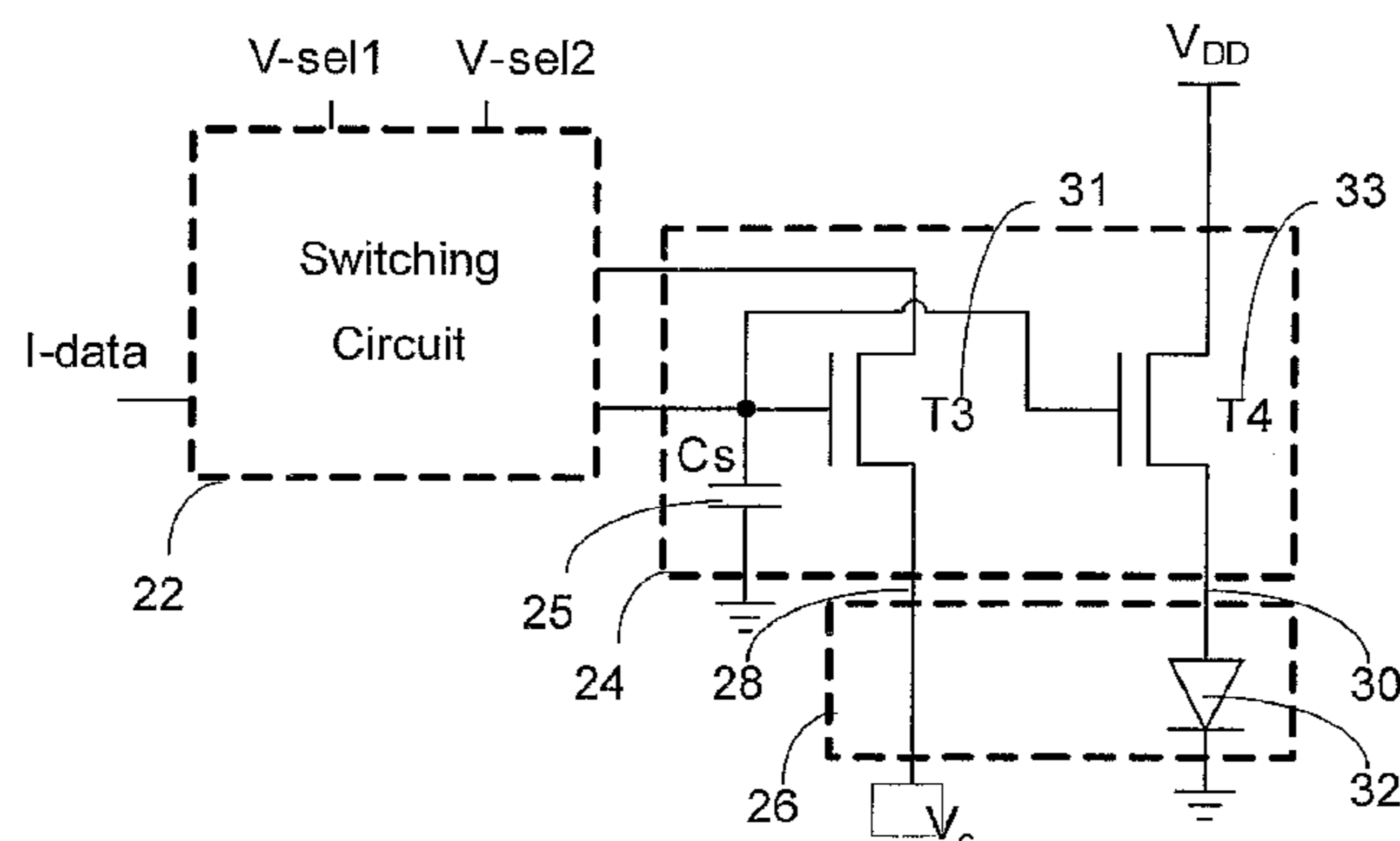
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ABSTRACT

A pixel circuit for use in a display comprising a plurality of
pixels is provided. The load-balanced current mirror pixel
circuit can compensate for device degradation and/or mis-
match, and changing environmental factors like temperature
and mechanical strain. The pixel circuit comprises a pixel
drive circuit comprising, switching circuitry, a current mir-
ror having a reference transistor and a drive transistor, the
reference transistor and the drive transistor each having a
first and second node and a gate, the gate of the reference
transistor being connected to the gate of the drive transistor;
and a capacitor connected between the gate of the reference
transistor and a ground potential, and a load connected
between the current mirror and a ground potential, the load
having a first load element and a second load element, the
first load element being connected to the first node of the
reference transistor and the second load element being
connected to the first node of the drive transistor.

19 Claims, 15 Drawing Sheets



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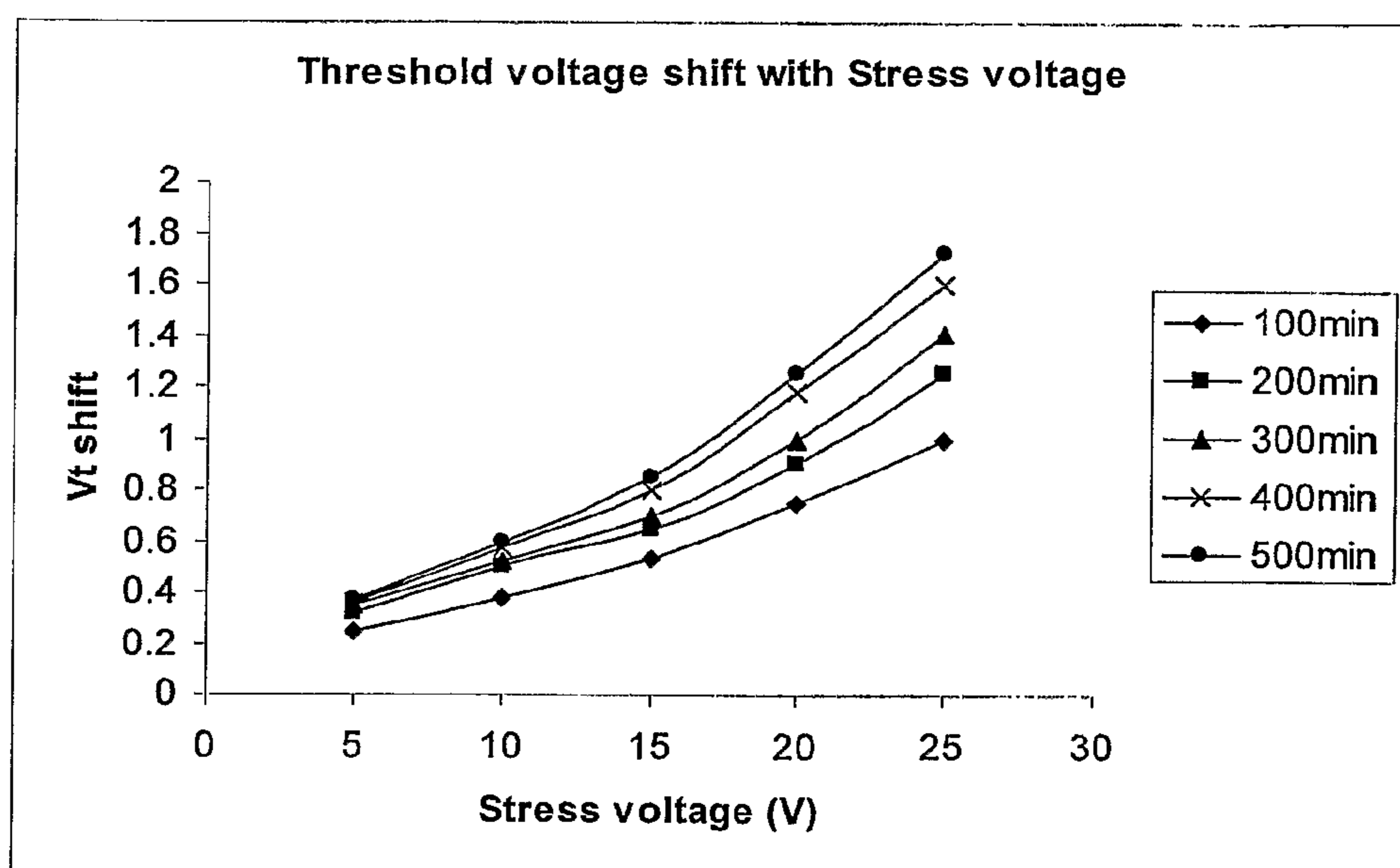


Figure 1 (PRIOR ART)

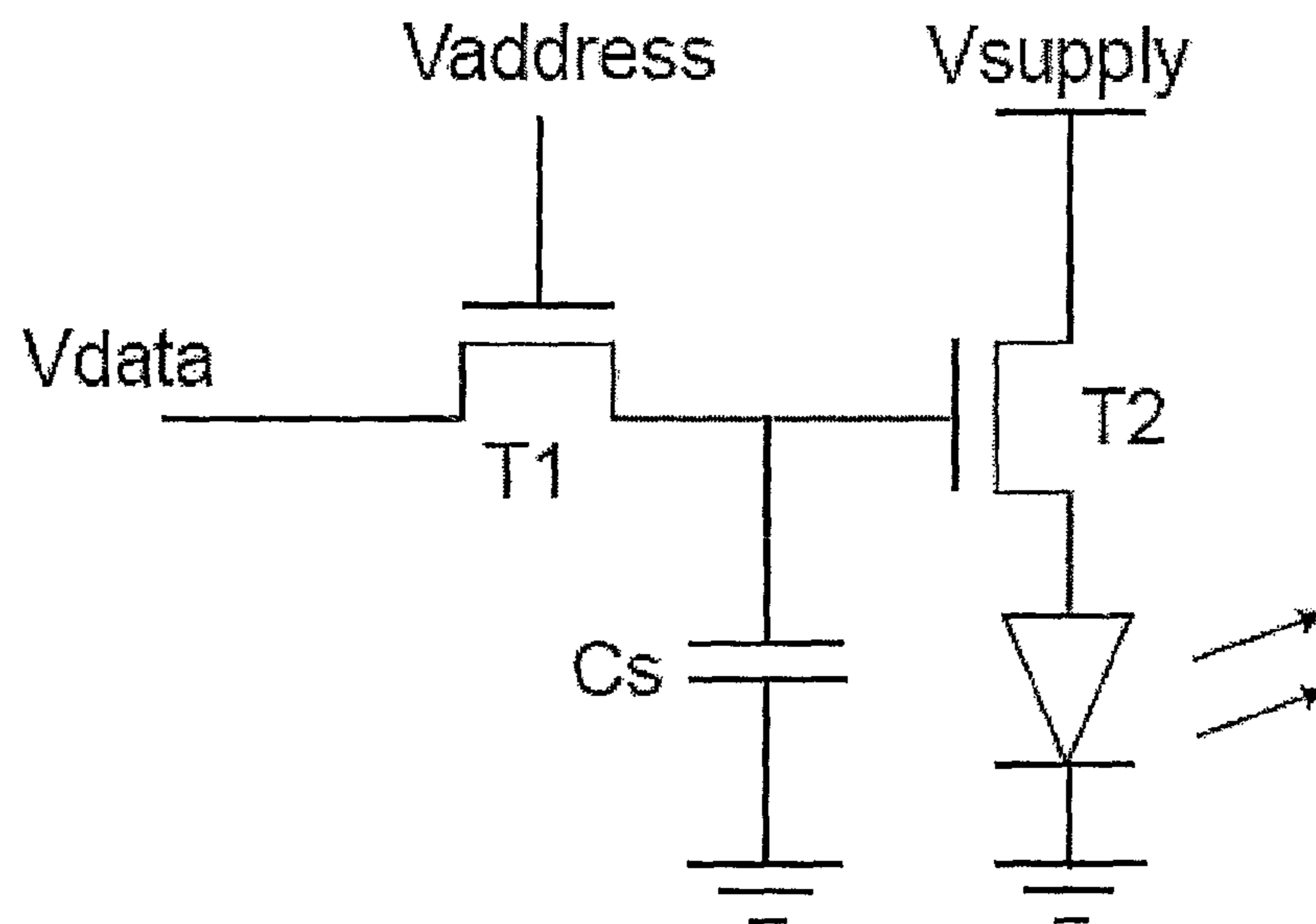


Figure 2 (PRIOR ART)

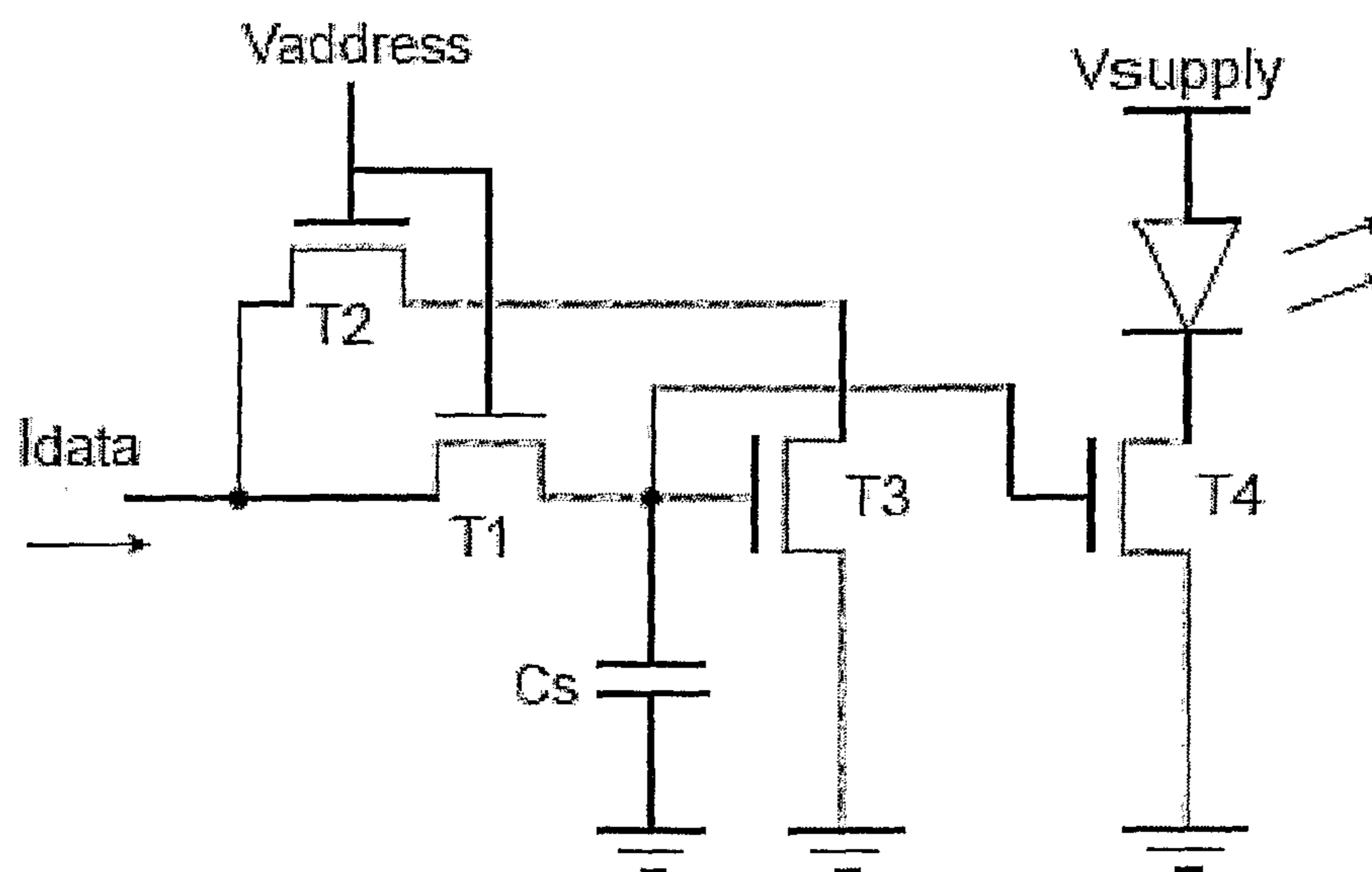


Figure 3 (PRIOR ART)

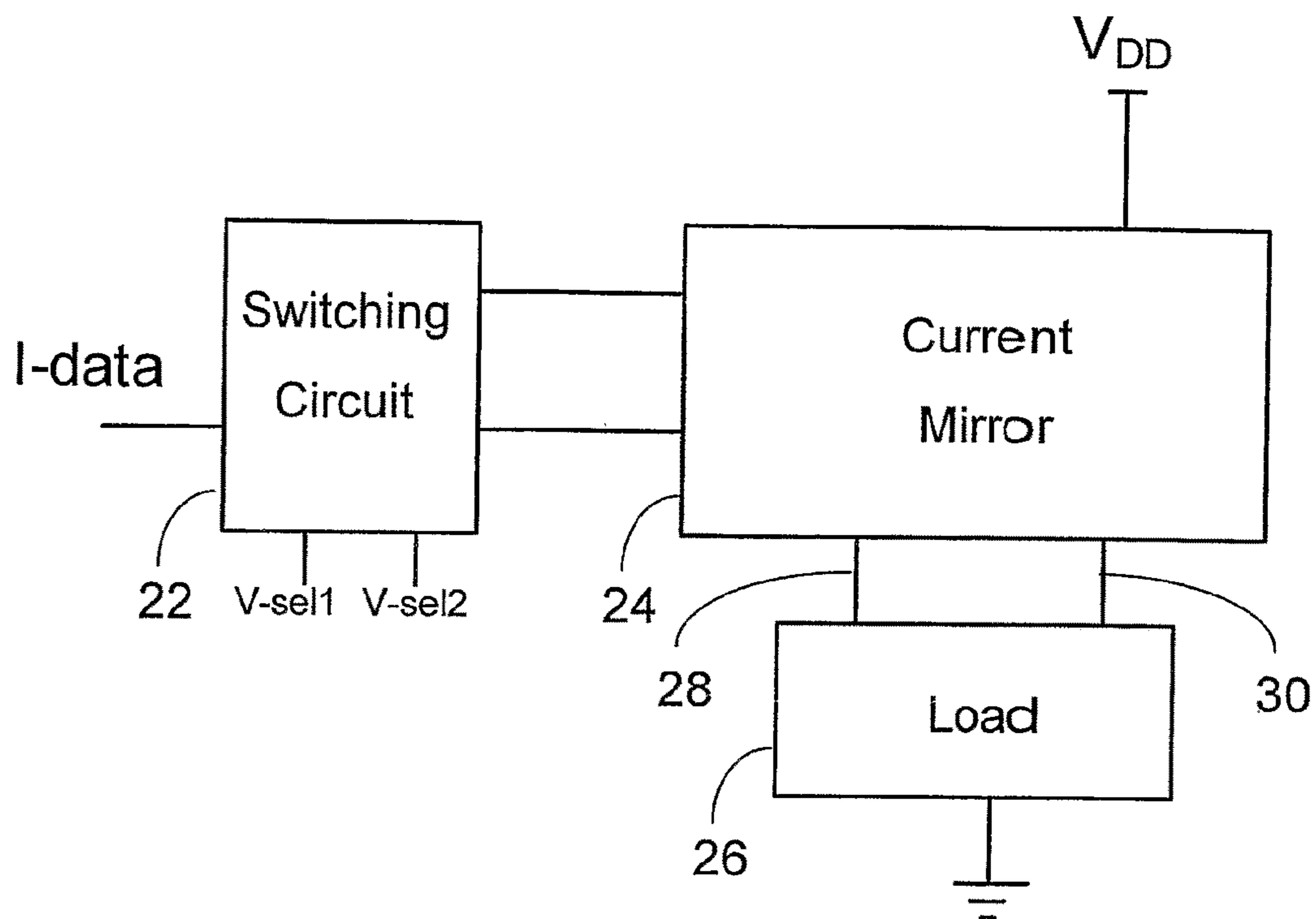


Figure 4

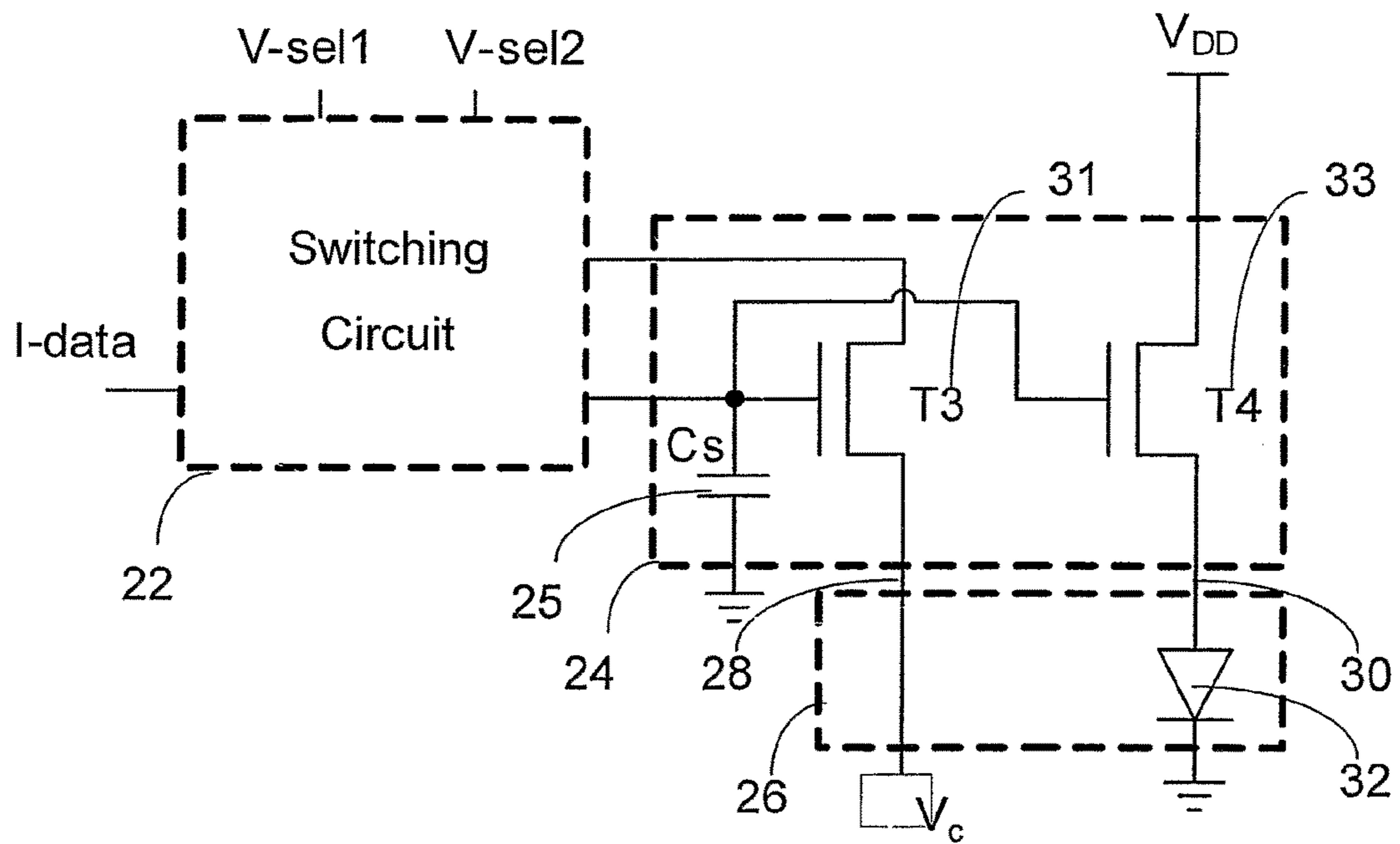


Figure 5A

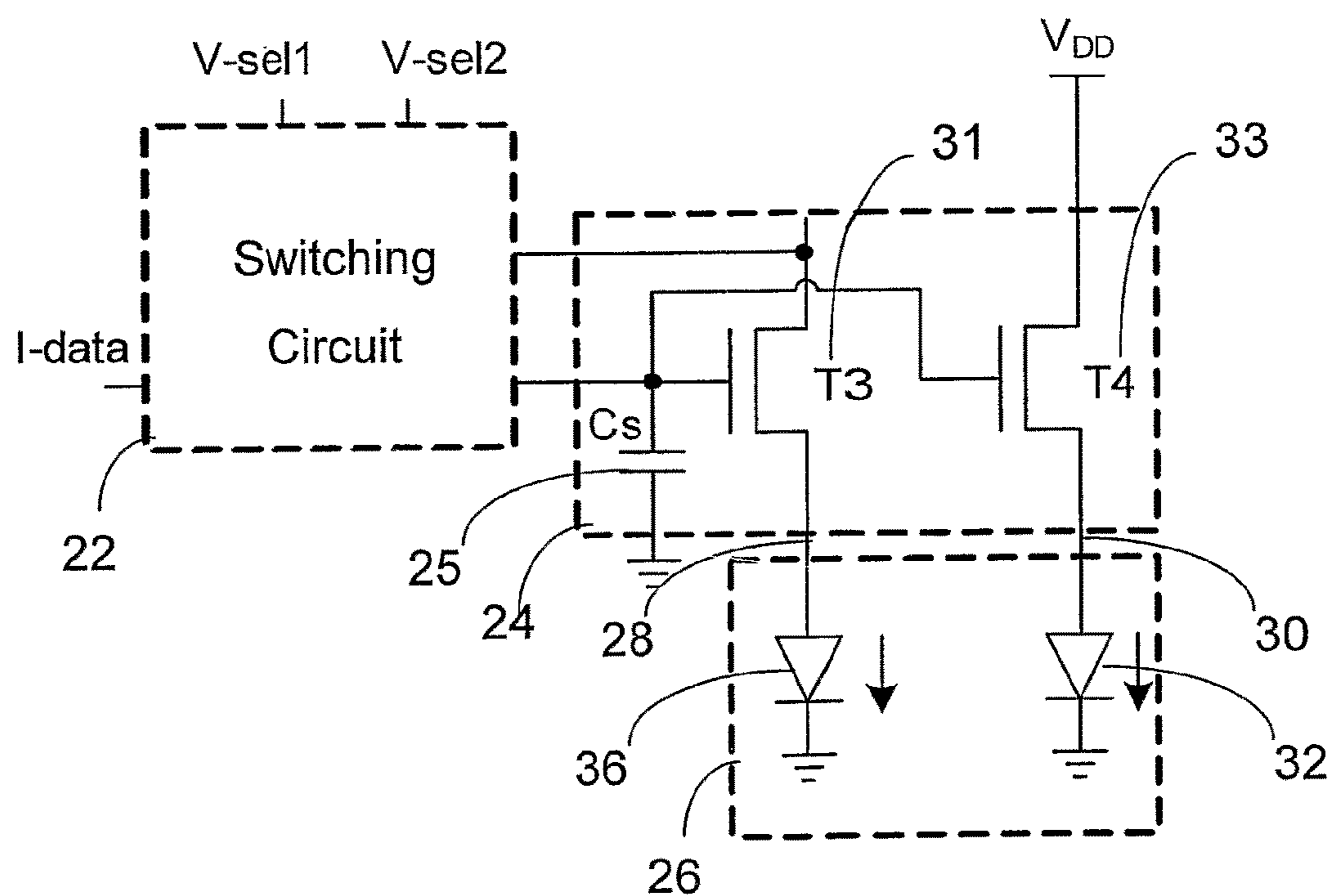


Figure 5B

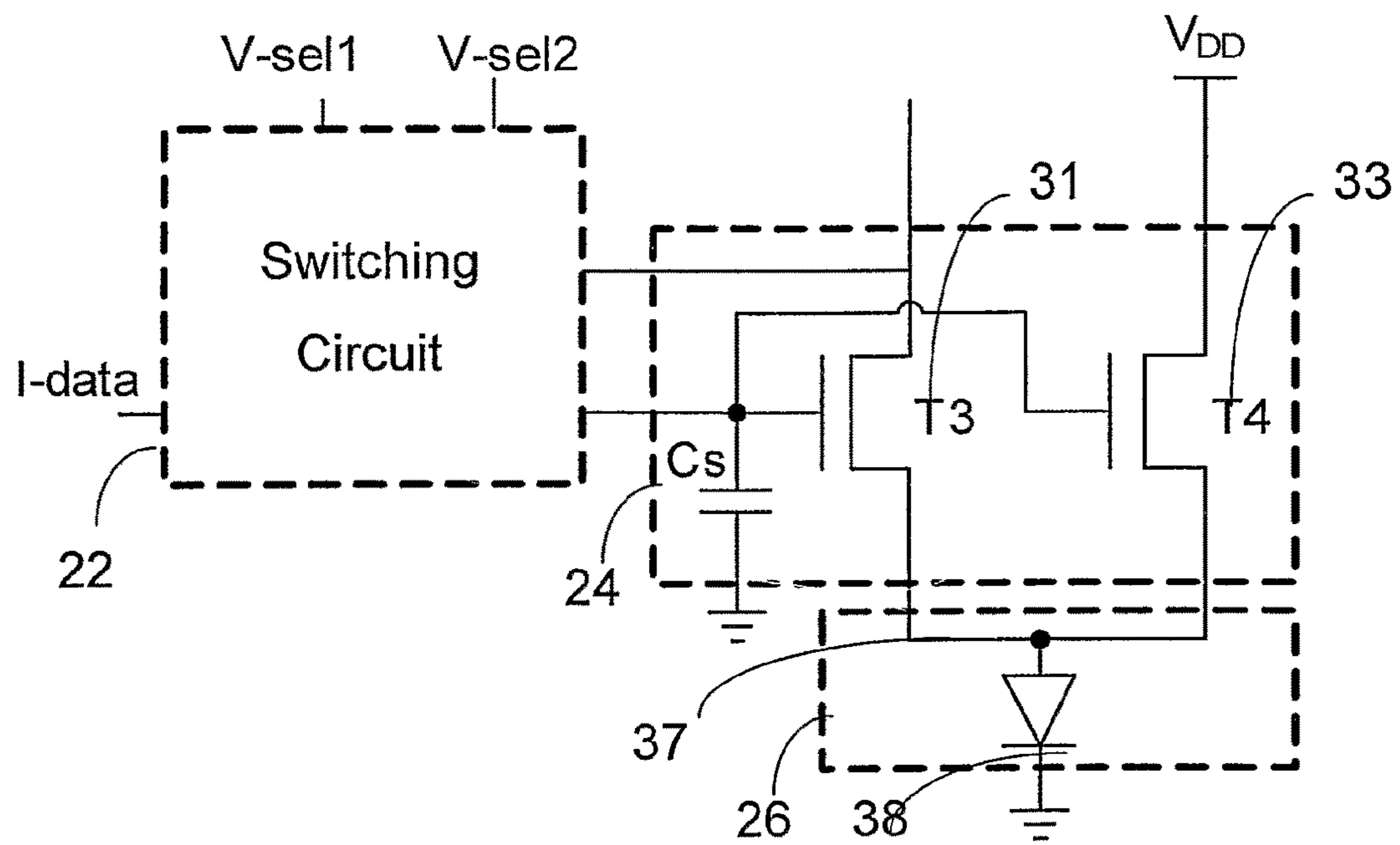


Figure 5C

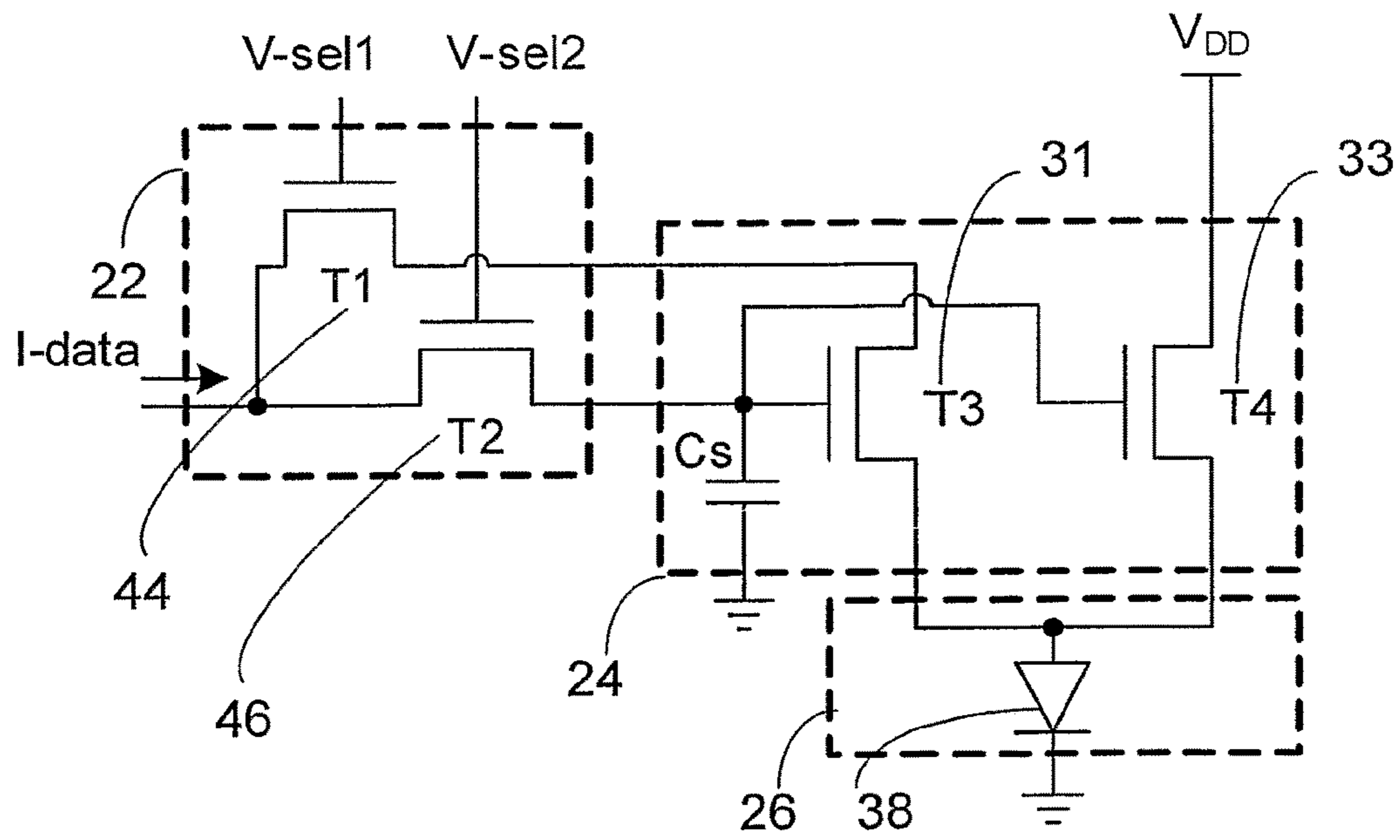


Figure 6A

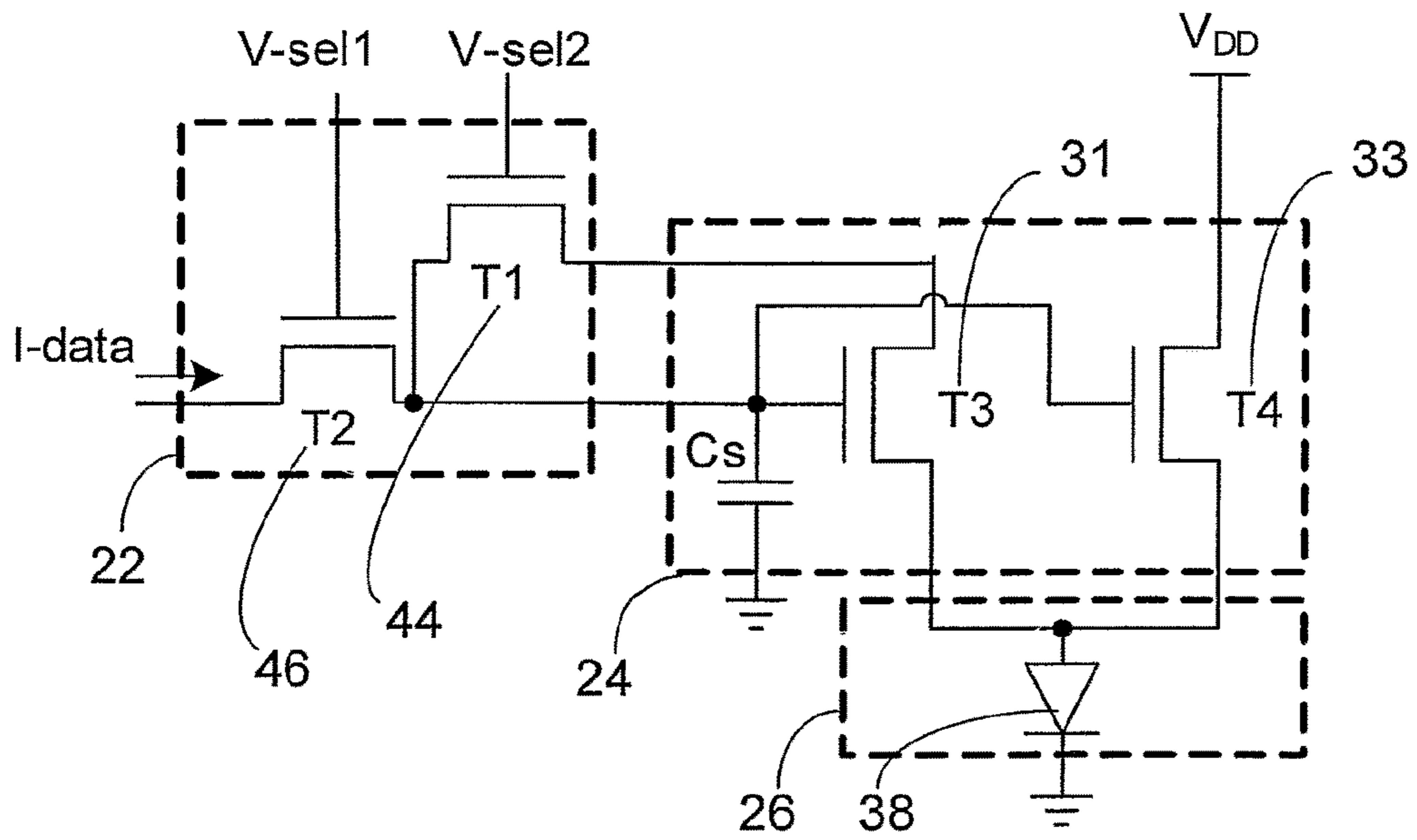


Figure 6B

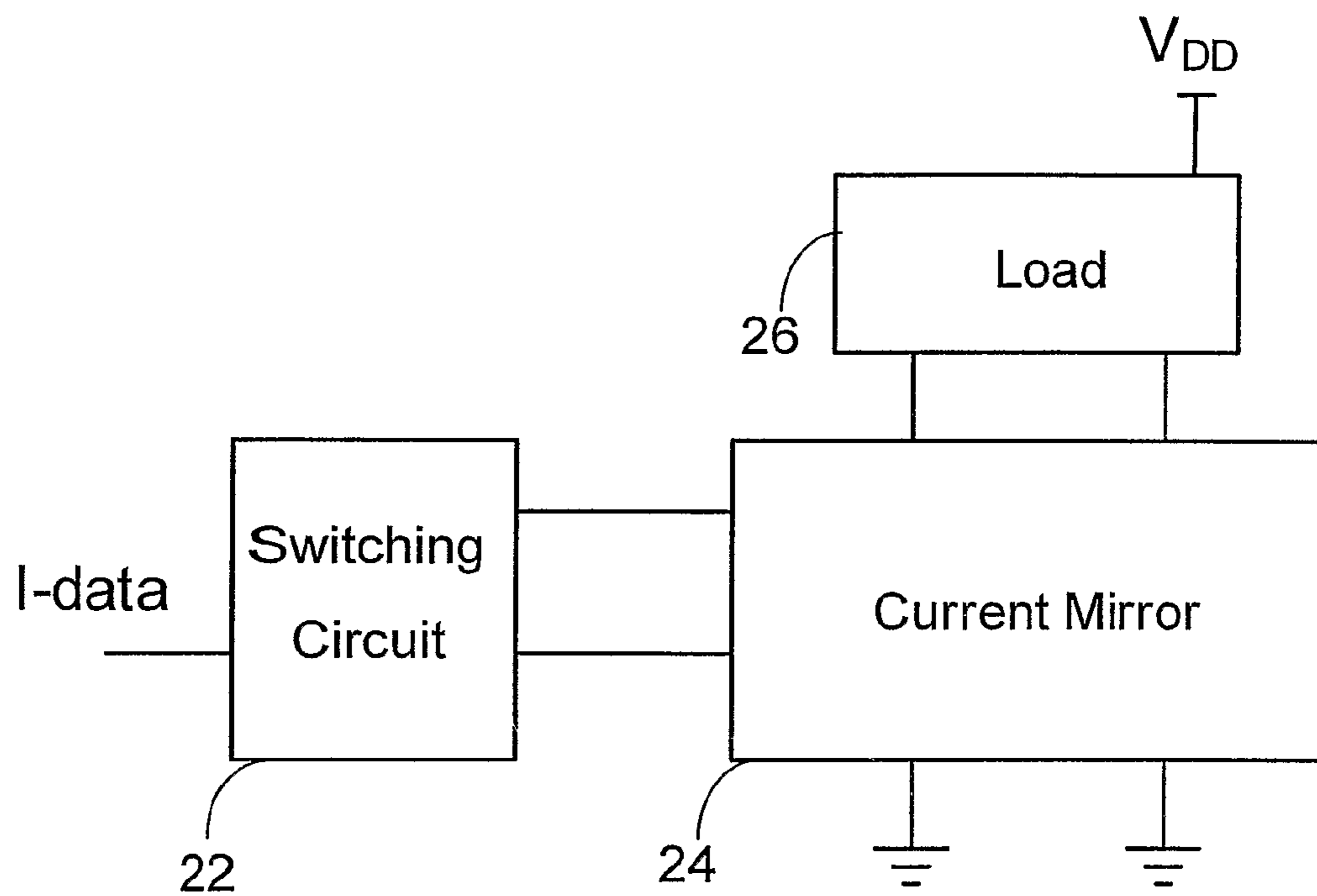


Figure 7A

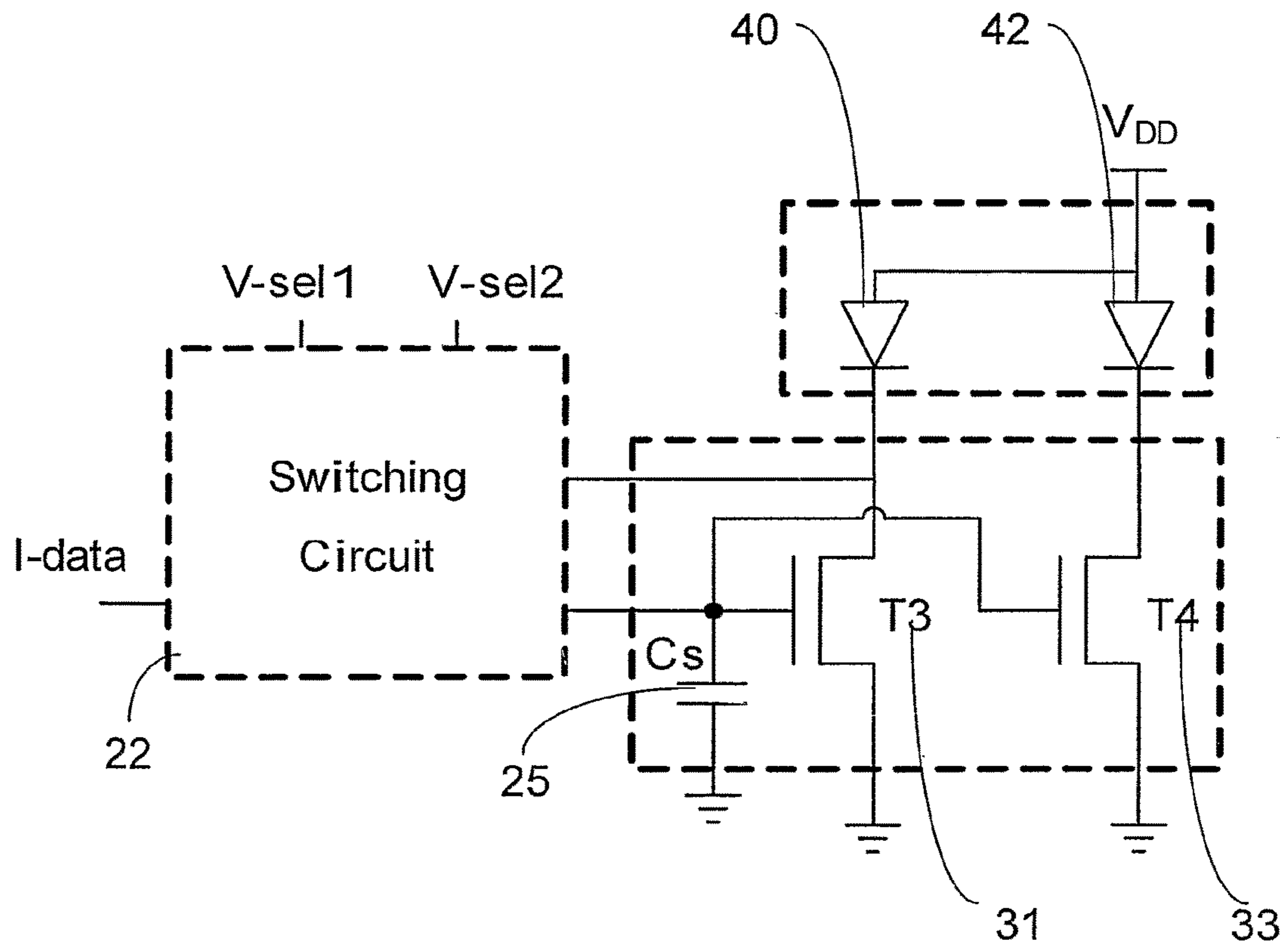


Figure 7B

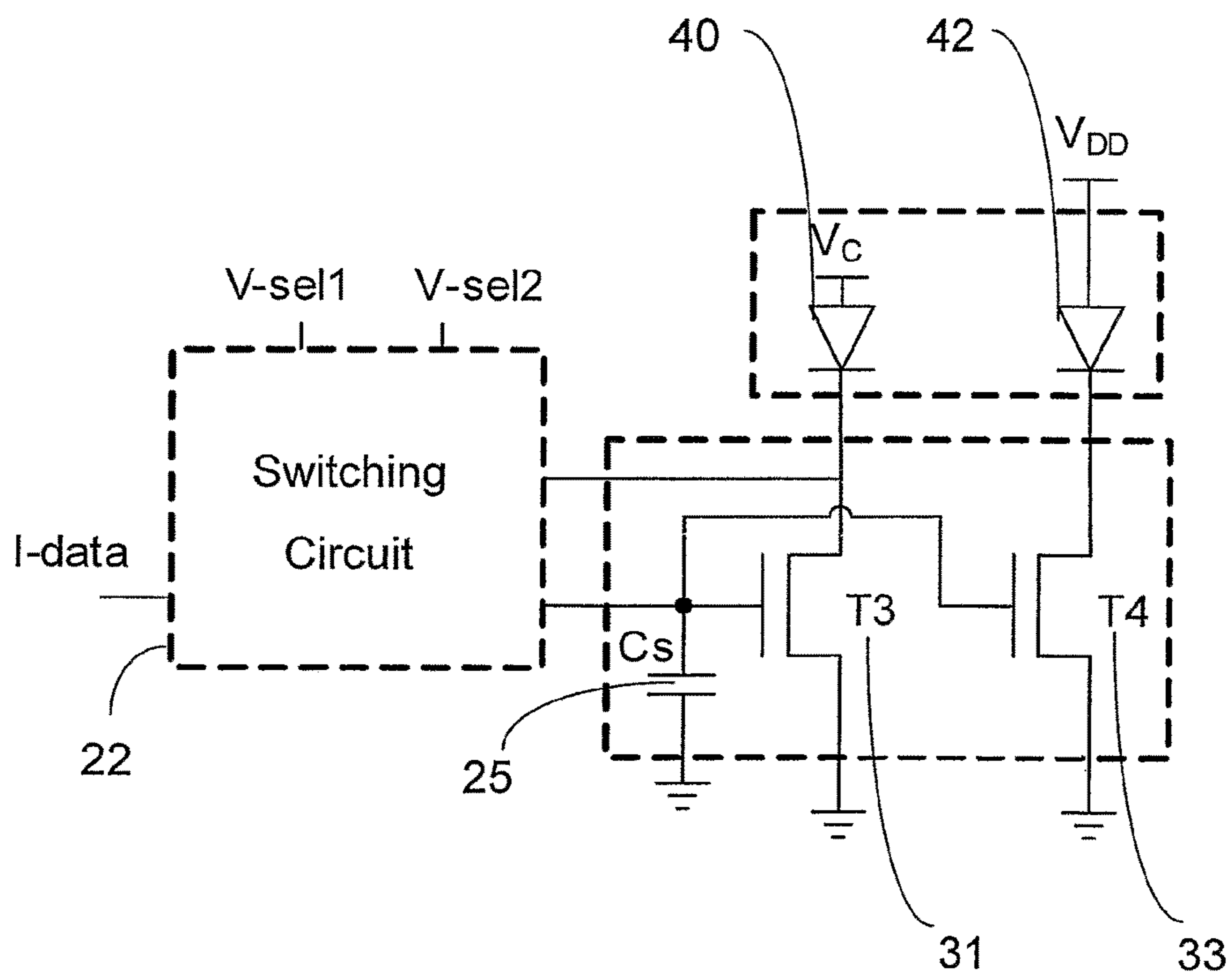


Figure 7C

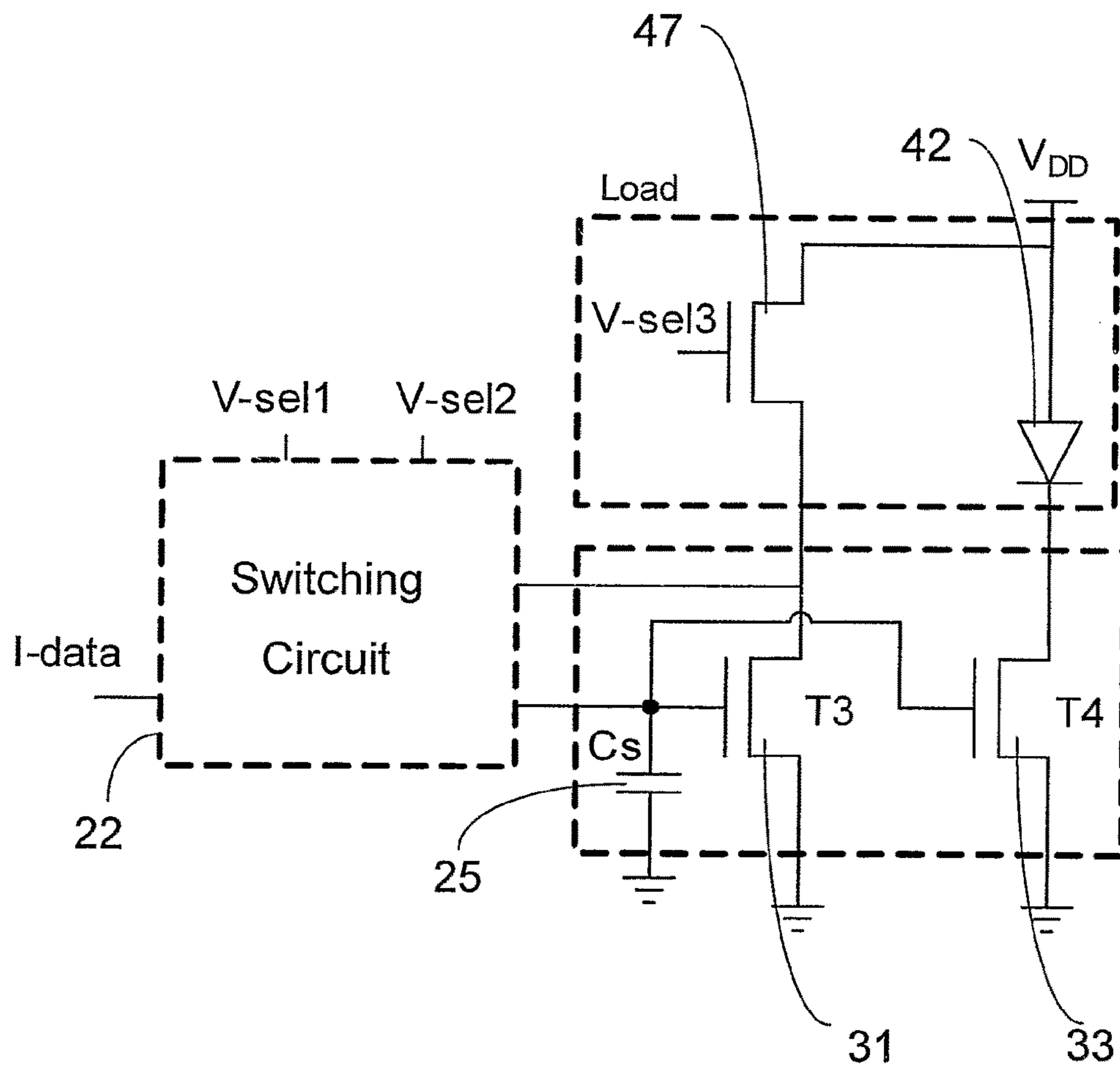


Figure 7D

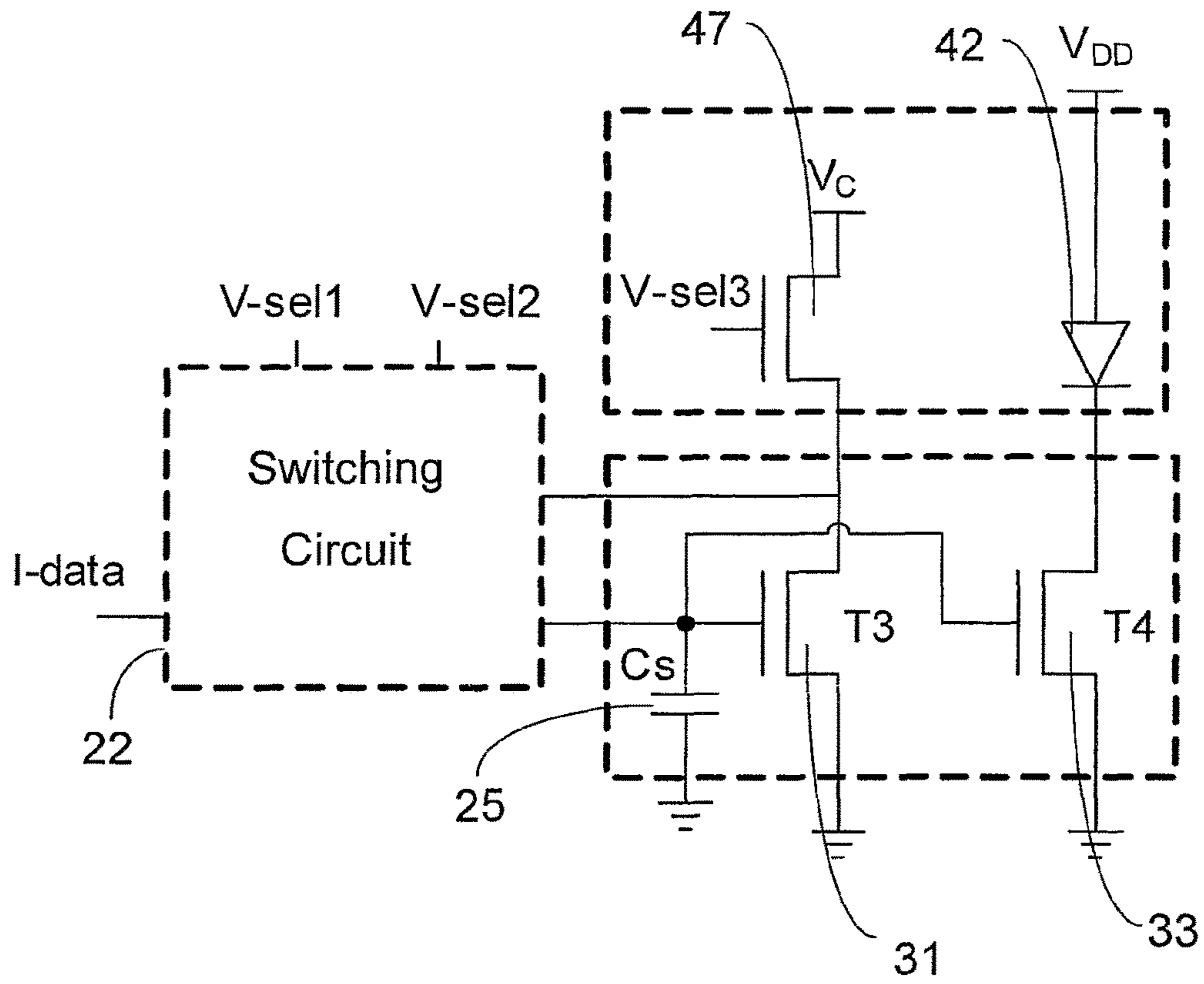


Figure 7E

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PIXEL DRIVER CIRCUIT WITH LOAD-BALANCE IN CURRENT MIRROR CIRCUIT

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of pending U.S. application Ser. No. 13/933,554, filed Jul. 2, 2013, which is a continuation of U.S. application Ser. No. 10/554,795, filed Jun. 15, 2006, now U.S. Pat. No. 8,502,751, which is a U.S. National Stage of International Application No. PCT/CA2004/001741, filed Sep. 23, 2004, which claims the benefit of Canadian Patent Application No. 2,443,206, filed Sep. 23, 2003, all of which are incorporated herein by reference in their entireties.

FIELD OF INVENTION

The present invention relates to circuitry for use in an active matrix display, and more particularly to a current drive circuitry used to drive the electro-luminescent elements.

BACKGROUND OF THE INVENTION

OLED based displays have gained significant interest recently for many display applications because of their faster response times, larger viewing angles, higher contrast, lighter weight, lower power, and amenability to flexible substrates, as compared to liquid crystal displays (LCDs).

The simplest way of addressing an OLED display is to use a passive matrix format. Although passive matrix addressed OLED displays are already in the marketplace, they do not support the resolution needed for next generation displays, which use high information content (HIC) formats. HIC formats are only possible with an active matrix addressing scheme.

Active matrix addressing involves a layer of backplane electronics, based on thin-film transistors (TFTs). These thin film transistors provide the bias voltage and drive current needed in each OLED pixel and may be fabricated using amorphous silicon (a-Si:H), polycrystalline silicon (poly-Si), organic, polymer, or other transistor technologies. When compared to passive matrix addressing, active matrix addressing uses a lower voltage on each pixel and the current throughout the entire frame period is a low constant value. Thus, active matrix addressing avoids the excessive peak driving and leakage currents associated with passive matrix addressing. This increases the lifetime of the OLED.

LCDs are electric field driven devices. OLEDs, on the other hand, are current driven devices. Thus, the brightness and stability of the light emitted by a given OLED used in a display is dependent on the operation of the TFTs in the current drive circuit. Thus AMOLED displays are far more sensitive to TFT instabilities including, spatial and temporal variations in transistor threshold voltage, mobility instability, and mismatch issues. These instabilities need to be addressed for widespread use of OLED based displays.

FIG. 1 presents a graph of threshold voltage shift vs. stress voltage for various times for amorphous silicon based TFTs. It is readily apparent from FIG. 1 that the threshold voltage of the transistors varies over time. If these transistors were used in a display, the variation in threshold voltage would likely result in variation in the brightness of the OLED across the array and/or a decrease in brightness over time, both of which are unacceptable.

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A simple pixel driver circuit is shown in FIG. 2. This "2T" circuit is a voltage programmed circuit. Such a circuit is not practical for OLED displays as such a circuit can not compensate for variations in transistor threshold voltage.

One solution to this variation in threshold voltage is to use a current programmed circuit to drive the OLED of the pixels. Current programming is a good method for driving AMOLED displays since the OLED is a current driven device, and its brightness is approximately linearly dependent upon the current flowing through it.

One such current programmed circuit is presented in FIG. 3. This circuit incorporates a current-mirror which compensates for any shift or mismatch in the threshold voltage of the drive transistor **12** which ensures that the brightness of the OLED **14** does not decrease over time. This feature of the circuit allows its drive characteristics to be much improved as compared to the 2T circuit of FIG. 2.

When programming the circuit of FIG. 3, $V_{ADDRESS}$ is high and a current I_{DATA} is applied. This current initially flows through transistor **T1** and charges capacitor C_S . As the capacitor voltage rises, **T3** begins to turn on and I_{DATA} starts to flow through **T2** and **T3** to ground. The capacitor voltage stabilizes at the point when all of I_{DATA} flows through **T2** and **T3**, and none through **T1**. This process is independent of the threshold voltage V_T of transistors **T3** and **T4**.

The gates of **T3** and **T4** are connected, so the current flowing through **T3** is mirrored in **T4**. This topology allows us to have on-pixel current gain or attenuation depending on the sizing of **T3** and **T4**, so that the respective data current can be proportionately smaller or larger than the OLED current. In an active matrix array, pixels are scanned and programmed in a row-by-row fashion. The time taken to scan all rows (one frame) is called the frame time. During array operation, the switching TFTs (**T1** and **T2**) are ON only once in the frame time.

However, existing current programmed circuits do not adequately address long-term stability in the OLED drive current due to differential V_t -shift and other bias, temperature, or mechanical stress related degradations and mismatches in the current mirror.

SUMMARY OF THE INVENTION

The present invention relates to a circuit for driving light emitting elements in a display and more particularly relates to a current drive circuit that implements a current mirror wherein each transistor of the current mirror is connected to a load.

It is an object of the invention to provide improved AMOLED Display Backplanes and Pixel Driver Circuits.

Accordingly, it is an object of the present invention to provide pixel current driver circuits for active matrix organic light emitting displays (AMOLED), capable of providing stable and predictable drive currents, in the presence of device degradation and/or mismatch, and changing environmental factors like temperature and mechanical strain. The latter is particularly important for mechanically flexible AMOLED displays.

According to an aspect of the invention a pixel circuit for use in a display comprising a plurality of pixels is provided. The pixel circuit comprises a pixel drive circuit comprising, switching circuitry, a current mirror having a reference transistor and a drive transistor, the reference transistor and the drive transistor each having a first and second node and a gate, the gate of the reference transistor being connected to the gate of the drive transistor; and a capacitor connected between the gate of the reference transistor and a ground

potential, and a load connected between the current mirror and a ground potential, the load having a first load element and a second load element, the first load element being connected to the first node of the reference transistor and the second load element being connected to the first node of the drive transistor.

According to another aspect of the invention a pixel circuit for use in a display comprising a plurality of pixels is provided. The pixel circuit comprises a pixel drive circuit comprising, switching circuitry, a current mirror having a reference transistor and a drive transistor, the reference transistor and the drive transistor each having a first and second node and a gate, the gate of the reference transistor being connected to the gate of the drive transistor, the second node of the reference and drive transistors connected to a ground potential, and a capacitor connected between the gate of the reference transistor and a ground potential, and a load connected between the current mirror and a potential.

This summary of the invention does not necessarily describe all features of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

FIG. 1 shows a graph of threshold voltage shift v. gate stress voltage for various times for thin film transistors made from amorphous silicon;

FIG. 2 shows a schematic diagram of a 2T voltage-programmed pixel driver circuit;

FIG. 3 shows a schematic diagram of a 4T current-programmed driver circuit;

FIG. 4 shows a block diagram of a current-programmed driver circuit according to an embodiment of the invention;

FIG. 5A shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

FIG. 5B shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

FIG. 5C shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

FIG. 6A shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

FIG. 6B shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

FIG. 6C shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

FIG. 7A shows a block diagram of a current-programmed driver circuit according to an embodiment of the invention;

FIG. 7B shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

FIG. 7C shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention;

FIG. 7D shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention; and

FIG. 7E shows a schematic diagram of a current-programmed driver circuit according to an embodiment of the invention.

The above objects and features of the present invention will become more apparent by the following description of the preferred embodiments with reference to the attached drawings.

DETAILED DESCRIPTION

It has been found that the long-term stability of the OLED drive current can be addressed by providing a load to each transistor of the current mirror of a current based drive circuit.

A block diagram of a pixel driver circuit according to one aspect of the invention is shown in FIG. 4. The driver circuit can generally be considered to include a switching circuit 22, a current mirror 24 and a load 26. Of particular note is that the load 26 is configured, with respect to the current mirror 24, such that the two transistors of the current mirror 24 have a load connected to them. In the configuration shown in FIG. 4 the load 26 is connected between the current mirror 24 and ground with connections 28 and 30. Where the connections 28 and 30 are each connected to a node of a transistor of the current mirror and the load 26. This architecture provides for a balancing of the load between the transistors of the current mirror. Embodiments of the invention that implement this architecture will now be presented.

In the embodiment presented in FIG. 4 the switching circuit 22 is connected to two select lines, namely V-sel1 and V-sel2. The embodiments presented in FIGS. 5A-5C, 6A-6C and 7A-7E likewise have two select lines. The switching circuit 22 is further connected to a single data line, I-data.

The circuits presented in FIGS. 5A to 5C have the same basic architecture as the circuit presented in FIG. 4, i.e. both transistors of the current mirror are connected to the load 26. The circuits of FIGS. 5A to 5C present type and configuration variations for the load 26.

In FIG. 5A the current mirror 24 includes a reference transistor 31, a drive transistor 33. The transistors 31 and 33 are thin film transistors which have an amorphous silicon channel. A storage capacitor 25 is included in the current mirror 24. The gates of the transistor 31 and the transistor 33 are tied together and both connected to a plate of the storage capacitor 25. The other plate of the storage capacitor Cs is connected to ground. The source of the reference transistor 31 is connected to potential Vc and the drain is connected to the switching circuit 22. Connecting the source to the potential Vc allows the two sides of the current mirror to be balanced with proper biasing. The source of the drive transistor 33 is connected to a light emitting diode 32 and the drain is connected to V_{DD}. In this embodiment the light emitting diode 32 is an organic light emitting diode (OLED).

FIG. 5B is a schematic diagram of a pixel driver circuit according to another embodiment of the invention. In this embodiment the source of the reference transistor 31 and the drive transistor 33 are connected to light emitting diodes 36 and 32, respectively.

FIG. 5C presents the currently preferred configuration for the load 26. The transistors 31 and 33 are tied together using a connection 37. In FIG. 5C the connection 37 is pictorially located within the load 26. The current embodiment is not limited by this representation. A single OLED 37 is connected to the common connection 37.

FIGS. 6A to 6C present embodiments of the invention wherein the current mirror 24 and the load 26 are the same as the embodiment presented in FIG. 5C while various configurations of the switching circuitry are provided. The switching circuits presented in FIGS. 6A to 6C each have a feedback transistor 44 and a switch transistor 46.

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In the circuit presented in FIG. 6A one terminal of the feedback transistor 44 and one terminal of the switch transistor 46 are connected to data line I-data. The second terminal of the feedback transistor 44 is connected to the drain of reference transistor 31 while the second terminal of the switch transistor 46 is connected to the gate of the reference and drive transistors 31 and 33, respectively. Finally, the gate of the feedback transistor 44 and switch transistor 46 is connected to the select line V-sel1 and select line V-sel2, respectively.

In the embodiment presented in FIG. 6B the first terminal of the switch transistor 46 is connected to the data line I-data while the first terminal of the feedback transistor 44 is connected to the second terminal of the switch transistor 46 which is connected to the gate of the reference and drive transistors 31 and 33, respectively. The second terminal of the feedback transistor 44 is connected to the drain of the reference transistor 31. Finally, the gate of the feedback transistor 44 and switch transistor 46 is connected to the select line V-sel2 and select line V-sel1, respectively.

In the embodiment presented in FIG. 6C the first terminal of the switch transistor 46 is connected to the data line I-data while the first terminal of the feedback transistor 44 is connected to the second terminal of the switch transistor 46 which is connected to the drain of the reference transistor 31. The second terminal of the feedback transistor 44 is connected to the gate of the reference and drive transistors 31 and 33, respectively. Finally, the gate of the switch transistor 46 and feedback transistor 44 is connected to the select line V-sel1 and select line V-sel2, respectively.

The circuits that have been considered are embodiments of the circuit presented as a block diagram in FIG. 4. An alternative embodiment of the circuit architecture of FIG. 4 is presented in FIG. 7A. The organization of the switching circuit 22 and the current mirror 24 is the same as the embodiment presented in FIG. 4. In this embodiment the load 26 is arranged such that it is between the potential V_{DD} and the current mirror 24. FIG. 7B-7E present embodiments of the invention based on the block diagram of FIG. 7A. These embodiments implement the same circuit for the current mirror 24 while the configuration of the load 26 varies.

In the embodiment presented in FIG. 7B the load 26 includes light emitting diodes 40 and 42. The diodes 40 and 42 are connected between the potential V_{DD} and the drain of reference transistor 31 and drive transistor 33, respectively. The sources of the reference transistor 31 and the drive transistor 33 are connected to ground. The gates of the reference transistor 31 and the drive transistor 33 are tied together and connected to both the switching circuit 22 and a plate of the storage capacitor 25. In the embodiment presented in FIG. 7C the light emitting diode 40 is connected to a potential V_C and the diode 42 is connected to the potential V_{DD} . The embodiments presented in FIGS. 7D and 7E differ from the embodiments of FIGS. 7B and 7C, respectively, in that the light emitting diode 40 is replaced with a transistor 47. The gate of transistor 47 is connected to a third select line V-sel3, a first terminal is connected to a potential and a second terminal is connected to the source terminal of reference transistor 32.

In the schematic diagram of FIGS. 5B, 7B, and 7C there are two OLEDs in each pixel. Such a double OLED structure is formed by partitioning the bottom electrode of the OLED of each pixel into two electrodes. Partitioning of the electrode provide for the formation of two OLEDs in each pixel. One of the OLEDs is connected to the drive transistor and the other is connected to the reference transistor. Therefore

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the load of reference and drive transistors is the same, resulting in a minimization of mismatches between these two transistors. It is noted that the ratio between the areas of the two OLEDs and the gain of the current mirror can be engineered to achieve desired circuit performance.

According to an alternative embodiment of the invention the transistors can be any appropriate material for the fabrication of thin film transistors including polycrystalline silicon, polymer and organic materials. In particular this embodiment considers appropriate changes for including p-type TFTs that are relevant to persons skilled in the art.

According to another alternative embodiment of the invention the pixel drive circuits do not include the capacitor Cs.

According to another alternative embodiment of the invention the switching circuit 22 is appropriate for the use with a single select line.

According to another alternative embodiment of the invention the transistors of the pixel driver circuits may have more than one gate. In particular the transistors may be dual gate transistors.

According to another alternative embodiment of the invention there is more than one driver circuit for a given pixel. In particular there may be three pixel driver circuits as would be appropriate for pixels in an RGB or colour display.

The present invention has been described with regard to one or more embodiments. However, it will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

What is claimed is:

1. A pixel driver circuit for use in a display, comprising:
 - a light emitting device (LED) comprising a first terminal connected to a source of a first potential and at least one second terminal;
 - a current mirror configured to provide a drive current to the LED based on a reference current; and,
 - a switching circuit configured to convey the reference current to the current mirror;
 wherein the current mirror comprises:
 - a reference transistor comprising a source terminal, a gate terminal connected to the switching circuit, and a drain terminal connected to the switching circuit,
 - a drive transistor comprising a gate terminal connected to the gate terminal of the reference transistor, a source terminal, and a drain terminal, the drive transistor configured to convey the drive current to the LED;
 wherein one of the drain terminal and the source terminal of the reference transistor and a corresponding one of the drain terminal and the source terminal of the drive transistor are connected to the at least one second terminal of the LED; and
 - a capacitor connected to the gate terminal of the reference transistor for accumulating a program voltage while the reference current is conveyed to the reference transistor.
2. The pixel driver circuit of claim 1, wherein the switching circuit comprises:
 - a switch transistor comprising a gate terminal connected to a first select line, a first terminal connected to a data line, and a second terminal; and
 - a feedback transistor comprising a gate terminal connected to the first select line or a second select line, a first terminal connected to one of the first terminal or the second terminal of the switch transistor, and a second terminal;

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wherein one of the second terminal of the switch transistor and the second terminal of the feedback transistor is connected to the gate terminal of the reference transistor, and the other of the second terminals of the switch transistor and the feedback transistor is connected to the drain terminal of the reference transistor.

3. The pixel driver circuit of claim 1, wherein the source terminal of the reference transistor and the source terminal of the drive transistor are connected to a common node, and wherein the at least one second terminal of the LED is connected to said common node.

4. The pixel driver circuit of claim 1, wherein the at least one second terminal of the LED comprises two LED terminals connected to the source terminal of the reference transistor and the source terminal of the drive transistor, respectively.

5. The pixel driver circuit of claim 4, wherein the LED comprises a light emitting diode having a bottom electrode partitioned to form the two LED terminals.

6. The pixel driver circuit of claim 4, wherein the LED comprises a first light emitting diode connected between the source terminal of the reference transistor and the source of the first potential, and a second light emitting diode connected between the source terminal of the drive transistor and the source of the first potential.

7. The pixel driver circuit of claim 1, wherein the at least one second terminal of the LED comprises two LED terminals connected to the drain terminal of the reference transistor and the drain terminal of the drive transistor, respectively.

8. The pixel driver circuit of claim 4, wherein the LED comprises a light emitting diode having a bottom electrode partitioned to form the two LED terminals.

9. The pixel driver circuit of claim 7, wherein the LED comprises a first light emitting diode connected between the drain terminal of the reference transistor and the source of the first potential, and a second light emitting diode con-

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nected between the drain terminal of the drive transistors and the source of the first potential.

10. The pixel driver circuit of claim 7, wherein the LED comprises a first light emitting diode connected between the drain terminal of the reference transistor and a source of a second potential, and a second light emitting diode connected between the drain terminal of the drive transistors and the source of the first potential.

11. The pixel driving circuit of claim 7, wherein the first potential is a biasing potential that is sufficient to operate the drive transistor in a saturation regime.

12. The pixel driving circuit of claim 11, wherein the source terminal of the drive transistor and the source terminal of the reference transistor are connected to a source of a ground potential.

13. The pixel driving circuit of claim 3, wherein the first potential is a ground potential and wherein the drain terminal of the drive transistor is connected to a source of supply voltage that is sufficient to operate the drive transistor in a saturation regime.

14. The pixel driving circuit of claim 4, wherein the first potential is a ground potential and wherein the drain terminal of the drive transistor is connected to a source of supply voltage that is sufficient to operate the drive transistor in a saturation regime.

15. The pixel driver circuit according to claim 1, wherein the reference and drive transistors are thin film transistors.

16. The pixel driver circuit according to claim 15, wherein the thin film transistors are formed using amorphous silicon or polycrystalline silicon or an organic material.

17. The pixel driver circuit according to claim 15, wherein the reference and drive transistors are p-type.

18. The pixel driver circuit according to claim 15, wherein the reference and drive transistors are n-type.

19. The pixel driver circuit according to claim 1, incorporated in an active matrix organic light emitting display (AMOLED).

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